Ultrathin Organic Thin-Film Transistors : Investigating Hybrid Gate Dielectrics and Stable Semiconductor Monolayers

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Dedicated to Late Dr. G. N. Acharya;
Scientist, Role model, Grandfather, Friend.

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Abstract

Organic electronics is an emerging field of research which includes the investigation of novel materials such as organic semiconductors and the development of devices such as organic thin-film transistors (TFTs). The unique properties of organic semiconductors, such as the ability to process them at relatively low temperatures, enable the development of potential applications of organic TFTs in flexible and wearable electronics such as rollable and foldable displays, conformable sensors and electronic skin. In order to facilitate the portable and lightweight nature of flexible electronics by powering them with small batteries or solar cells, a low operating voltage and an overall low power consumption are some of the main requirements of organic TFTs. High-capacitance gate dielectrics, such as hybrid gate dielectrics with an ultrathin metal oxide and an organic self-assembled monolayer (SAM), are an essential choice towards fulfilling these operation requirements. Organic TFTs are fabricated by depositing different materials as thin films by a variety of processes, and the individual film properties of the different components influence the overall electrical characteristics of organic TFTs. The main contribution of this thesis is to establish a correlation between the material properties of the individual components and the electrical properties of the organic TFTs, and moreover, suitably modify the fabrication process to achieve better electrical characteristics in organic TFTs.

In this thesis, hybrid gate dielectrics consisting of an ultrathin aluminum oxide (AlO_x) film and a phosphonic acid SAM are investigated. The AlO_x films are fabricated by exposing the surface of the underlying aluminum gate electrode to an oxygen plasma, and the SAMs are processed from solution. Phosphonic acid molecules with an alkyl or a fluoroalkyl chain with different chain lengths have been chosen to form the SAMs. Two small-molecule organic semiconductors are selected as the active material in the organic TFTs: dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT).

The significance of both components of the hybrid gate dielectric in simultaneously achieving a leakage-current density of 10^{-7}A/cm^2 as well as an operating voltage of 3 V has been established. The thickness of the AlO_x films was measured by Transmission Electron Microscopy and the films were characterized by Electron Energy Loss Spectroscopy and Atom Probe Tomography to determine the thin-film composition. Depending on the parameters of the oxygen-plasma process, AlO_x films with a thickness ranging between 4 nm and 7 nm were fabricated, and consequently, organic TFTs with

a gate-dielectric capacitance between 1 μF/cm^2 and 1.6 μF/cm^2. In particular, charge-carrier mobilities ranging from 1.8 to 2.3 cm^2/Vs were obtained for a number of favorable combinations of the plasma power and plasma duration that produce AlO_x films with a small surface roughness and thus promote the formation of high-quality SAMs and well-ordered DNTT films on these gate dielectrics. The influence of the thickness of the SAM by employing different chain-length phosphonic acid molecules on different TFT characteristics such as the threshold voltage, gate-leakage current, charge-carrier mobility and the subthreshold swing has been examined in DNTT and DPh-BTBT TFTs. By employing the medium-chain-length phosphonic acid molecules, an optimum charge-carrier mobility of 2 cm^2/Vs for the DNTT TFTs, and a turn-on voltage of 0 V for the DPh-BTBT TFTs was achieved. The growth and morphology of the organic semiconductor DNTT on different gate-dielectric surfaces was observed by Scanning Electron Microscopy and Atomic Force Microscopy and was correlated with surface properties of the SAMs and the electrical characteristics of TFTs based on those films.

The stability of ultrathin films with a thickness of one-two molecular monolayers of the organic semiconductor DNTT was investigated, and spontaneous morphological changes occurring in the films were observed and correlated with the stability of organic TFTs based on these films. The structural reconfiguration of the ultrathin DNTT films and the degradation of the charge-carrier mobility of organic TFTs based on these films were prevented to a certain extent by cryogenic cooling and in-situ encapsulation.

The hybrid gate dielectric with its two components, the organic semiconductor and the gate dielectric-semiconductor interface are the focal points in this thesis. The material and surface properties of the individual components of the gate dielectric have been correlated with the film properties of the organic semiconductor and further with the electrical characteristics of organic TFTs.

Zusammenfassung

Organische Elektronik ist ein aufkommendes Forschungsgebiet, das die Untersuchung neuartiger Materialien wie organischer Halbleiter und die Entwicklung von Bauelementen wie organischen Dünnschichttransistoren (TFTs) umfasst. Die einzigartigen Eigenschaften organischer Halbleiter, wie beispielsweise die Fähigkeit, sie bei relativ niedrigen Temperaturen zu verarbeiten, ermöglichen die Entwicklung potenzieller Anwendungen organischer TFTs in flexibler und tragbarer Elektronik wie rollbare und faltbare Displays, anpassungsfähige Sensoren und elektronische Haut. Um die tragbare und leichte Natur flexibler Elektronik zu ermöglichen, indem sie mit kleinen Batterien oder Solarzellen betrieben wird, sind niedrige Betriebsspannung und allgemein geringer Stromverbrauch einige der Hauptanforderungen an organische TFTs. Gate-Dielektrika mit hoher Kapazität, wie z. B. hybride Gate-Dielektrika, bestehend aus einem ultradünnen Metalloxid und einer organischen selbstorganisierten Monolage (SAM), sind eine wesentliche Voraussetzung für die Erfüllung dieser Betriebsanforderungen. Organische TFTs werden durch die Abscheidung verschiedener Materialien in Form von dünnen Schichten durch eine Vielzahl von Verfahren hergestellt, und die individuellen Material- und Schichteigenschaften der verschiedenen Komponenten beeinflussen die elektrischen Gesamteigenschaften der organischen TFTs.

Der Hauptbeitrag dieser Arbeit besteht darin, eine Korrelation zwischen den Materialeigenschaften der einzelnen Komponenten und den elektrischen Eigenschaften der organischen TFTs herzustellen und darüber hinaus den Herstellungsprozess geeignet zu modifizieren, um bessere elektrische Eigenschaften in organischen TFTs zu erreichen. In der vorliegenden Arbeit werden hybride Gate-Dielektrika untersucht, die aus einer ultradünnen Schicht Aluminiumoxid (AlO_x) und einer Phosphonsäure-SAM bestehen. Die AlO_x-Schicht wird hergestellt, indem die Oberfläche der darunterliegenden Aluminium-Gate-Elektrode einem Sauerstoffplasma ausgesetzt wird, und die SAMs werden aus einer Lösung verarbeitet. Für die SAM wurden Phosphonsäuremoleküle mit einer Alkylkette oder einer Fluoralkylkette mit unterschiedlichen Kettenlängen gewählt. Als aktives Material für die organischen TFTs wurden zwei organische Halbleiter ausgewählt: Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) und 2,7-Diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT).

Die Rolle der beiden Bestandteile des hybriden Gate-Dielektrikums für das gleichzeitige Erreichen einer Leckstromdichte von 10^{-7} A/cm^2 sowie einer Betriebsspannung

von 3 V wurde festgestellt. Die AlO_x-Schichten wurden mittels Transmissionselektronenmikroskopie, Elektronenenergieverlustspektroskopie und Atomsondentomographie charakterisiert, um die Dicke und Zusammensetzung der Dünnschicht zu bestimmen. Je nach den Parametern des Sauerstoff-Plasma-Prozesses wurden AlO_x-Schichten mit einer Dicke zwischen 4 nm und 7 nm hergestellt und folglich organische TFTs mit einer Gate-Dielektrizitätskapazität zwischen 1 μF/cm^2 und 1,6 μF/cm^2. Insbesondere wurden Ladungsträgermobilitäten im Bereich von 1,8 bis 2,3 cm^2/Vs für eine Reihe günstiger Kombinationen von Plasmaleistung und Plasmadauer erreicht, die AlO_x-Filme mit geringer Oberflächenrauhigkeit erzeugen und so die Bildung hochwertiger SAMs fördern und wohlgeordnete DNTT-Filme auf diesen Gatedielektrika. Insbesondere wurden Ladungsträgermobilitäten im Bereich von 1,8 bis 2,3 cm^2/Vs für eine Reihe günstiger Kombinationen von Plasmaleistung und Plasmadauer erreicht, die AlO_x-Filme mit geringer Oberflächenrauhigkeit erzeugen und so die Bildung hochwertiger SAMs und wohlgeordneter DNTT-Filme auf diesen Gatedielektrika fördern. Die Auswirkung der Dicke der SAM durch die Verwendung von Phosphonsäuremolekülen unterschiedlicher Kettenlänge auf verschiedene TFT-Eigenschaften wie Schwellenspannung, Gate-Leckstrom, Ladungsträgermobilität und Schwingung unterhalb der Schwelle wurde in DNTT- und DPh-BTBT-TFTs untersucht. Durch die Verwendung der mittelkettigen Phosphonsäuremoleküle wurde eine optimale Ladungsträgermobilität von 2 cm^2/Vs für die DNTT-TFTs und eine Einschaltspannung von 0 V für die DPh-BTBT-TFTs erreicht. Das Wachstum und die Morphologie des organischen Halbleiters DNTT auf verschiedenen Gate-Dielektrikum-Oberflächen wurden mittels Rasterelektronenmikroskopie und Rasterkraftmikroskopie analysiert und mit den Oberflächeneigenschaften der SAMs und den elektrischen Eigenschaften der auf diesen Filmen basierenden TFTs korreliert.

Die Stabilität von ultradünnen DNTT-Filmen, mit einer Dicke von 1-2 molekularen Monolagen, wurde untersucht und spontane Veränderungen der Morphologie in den DNTT-Filmen mit der Stabilität von organischen TFTs korreliert. Die Stabilität von ultradünnen Filmen mit einer Dicke von 1-2 molekularen Monolagen des organischen Halbleiters DNTT wurde untersucht und spontan auftretende morphologische Veränderungen in den Filmen wurden beobachtet und mit der Stabilität von organischen TFTs basierend auf diesen Filmen korreliert. Weiterhin wurde untersucht, inwieweit die strukturelle Neuanordnung der ultradünnen DNTT-Filme und die Abnahme der Ladungsträgermobilität der organischen TFTs, die auf diesen ultradünnen DNTT-Filmen basieren, durch kryogene Abkühlung und In-situ-Verkapselung verhindert werden können.

Das hybride Gate-Dielektrikum mit seinen beiden Komponenten, dem organischen Halbleiter und der Gate-Dielektrikum-Halbleiter-Grenzschicht, steht im Mittelpunkt dieser

Arbeit. Insbesondere wurden die Material- und Oberflächeneigenschaften der einzelnen Komponenten des Gatedielektrikums mit den Filmeigenschaften des organischen Halbleiters und weiter mit den elektrischen Eigenschaften organischer TFTs korreliert.

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Abbreviations

AlO_x aluminum oxide, unknown stoichiometry

a-Si:H hydrogenated-amorphous silicon

AFM atomic force microscopy

AMLCD active-matrix liquid-crystal display

C_{60} Buckminster fullerene

DNTT dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene

DPh-BTBT 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene

EELS electron energy loss spectroscopy

FIB focused ion beam

HHCF height-height correlation function

HOMO highest occupied molecular orbital

LUMO lowest unoccupied molecular orbital

MOSFET metal-oxide semiconductor field-effect transistor

ODPA octadecylphosphonic acid

ODTS octadecyltrichlorosilane

OFET organic field-effect transistor

OLED organic light-emitting diode

OTS octadecylsilane

PEN poly(ethylene)2,6-naphthalate

PTFE polytetrafluoroethylene

$\mathbf{R_{RMS}}$ root-mean-square surface roughness

SAM self-assembled monolayer

SEM scanning electron microscopy

TEM transmission electron microscopy

TFT thin-film transistor

TiOPc titanyl phthalocyanine

ToF-SIMS time-of-flight secondary ion mass spectrometry

Symbols

μ	charge-carrier mobility	m^2/Vs
μ_0	intrinsic charge-carrier mobility	m^2/Vs
σ	electrical conductivity	S/m
θ	liquid contact angle	°
ε_0	absolute permittivity	F/m
L	channel length	m
W	channel width	m
k	dielectric constant (or relative permittivity)	
C	capacitance	F
C_{diel}	area-normalized gate-dielectric capacitance	F/m^2
E_F	Fermi energy level	eV
I_G	gate current	A
I_D	drain current	A
k_B	Boltzmann constant	$m^2 kg\ s^{-2} K^{-1}$
T_{sub}	substrate temperature	°C
V_{th}	threshold voltage	V
V_{DS}	drain-source voltage	V
V_{GS}	gate-source voltage	V

Chapter 1

Introduction

The widespread use of digital electronics and the undeniable reliance on them are an inseparable part of human life in today's hyper-connected, fast-paced world. Coupled with the powers of the internet, there is a perpetual demand for frequent breakthroughs which lead to a larger bandwidth, newer technological advancements and which branch out into alternate, diverse applications. In such an environment, there is a continuous effort to explore and develop unique innovations that will improve the quality of life in previously unthinkable ways.

The discovery of semiconducting properties in materials and fabrication of electrical devices employing them has been one of the most important developments of the 20th century. The transistor is the fundamental building block of modern electronic systems and is used to amplify and switch electrical signals using a semiconductor as the active material. The electronics industry has come a long way to develop the modern gadgets and advanced technology available today, following a long history of decades of intense research and development. The first ideas of the transistor date back to Julius E. Lilienfeld [1] (1930) and to Oskar Heil [2] (1935), who both patented devices which resemble modern-day field-effect transistors. They also noted that the active material in such a device, key to its functionality, would have to be a semiconductor, but were unfortunately unable to fabricate a working device, most likely due to the lack of high-quality semiconductors. A major breakthrough was achieved with the first successful and reproducible demonstrations of the transistor by John Bardeen and Walter Brattain [3] (1947) and William Shockley [4] (1948) at Bell Labs, for which they later jointly received the 1956 Nobel Prize in Physics for "their research on semiconductors and their discovery

of the transistor effect". The transistors fabricated were, respectively, a point-contact transistor and a bipolar-junction transistor, which are both almost obsolete in modern-day electronics. The next most impactful development occurred with the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) by Martin Mohamed Atalla [5](1960) and Dawon Kahng [6] (1963). The characteristic feature in the MOSFET was the surface passivation of the crystalline silicon wafer with an insulating layer of controlled, thermally-grown silicon dioxide [7], which gave MOSFETs several advantages such as a higher degree of scalability, lower power consumption and a higher integration density as compared to bipolar-junction transistors. Due to all these benefits, the MOSFET quickly superseded all its predecessors in terms of its performance and made it possible to build high-density integrated circuits. The MOSFET was the first truly compact transistor that was miniaturized and mass produced and became the most common type of transistor to be used in computers, electronics, and communications, having a profound impact on the development of digital electronics. Although other semiconductor materials such as germanium and gallium arsenide have better electrical properties than silicon, the ability to form high-quality semiconductor-insulator interfaces makes silicon the champion semiconductor material in modern electronics. However, the material properties and processing conditions required to fabricate silicon-based MOSFETs make them unsuitable for applications envisioned outside of the current conventional single-crystalline silicon electronics domain. Alongside, another major breakthrough included the development of the thin-film transistor (TFT) which was first developed by Paul Weimer in 1962 using cadmium selenide (CdSe) as the semiconductor [8]. In this device configuration, all the materials are deposited as thin films onto an independent surface, thus broadening the choice of the substrate beyond silicon wafers to those substrate materials compatible with the fabrication process. This invention was followed by pioneering work by T. Peter Brody and coworkers in the development of indium arsenide (InAs) [9] and CdSe TFTs, which were later used to demonstrate the most common application of the TFT, the active-matrix liquid-crystal display (AMLCD) [10]. In 1979, P.G. le Comber, W.E. Spear and A. Ghaith developed the first functional hydrogenated-amorphous silicon (a-Si:H) TFT with a silicon nitride (SiN) gate dielectric [11], after which it was soon realized that a-Si:H TFTs are better suited for large area AMLCDs, which went on to be mass produced as a common display technology. Apart from amorphous silicon, polycrystalline silicon was also extensively researched for fabricating TFTs for display applications. Low-temperature polycrystalline silicon (LTPS) is crystallized

at a relatively lower temperature (∼ 450 °C) compared to the traditional temperature of 900 °C and above for single-crystalline silicon. LTPS TFTs are commonly used to drive displays based on organic light-emitting diodes (OLEDs) and are beneficial for large glass displays which are likely to undergo deformation at elevated temperatures. When the semiconductor is deposited as a thin film for TFT applications, it lacks the high degree of crystallinity of the active material in MOSFETs, and thus has a relatively lower performance. However, the independent choice of the substrate, separate from the semiconductor material, makes TFTs the ideal choice for large-area applications with low-frequency requirements, such as in displays.

Apart from silicon, other semiconductor technologies are also being explored and investigated, e.g. oxide semiconductors (e.g. ZnO, In_2O_3) [12–14], transition metal dichalcogenides (e.g. WS_2, MoS_2) [15–17], carbon nanotubes [18–20], nanowires (e.g. Si, GaAs, InAs/InP, In_2O_3) [21–26], and of course, central to this thesis, organic materials.

Although the synthesis of conductive organic materials (carbon-hydrogen based materials) can be dated back to the late 19th century [27, 28], the first instances of observing electrical conductivity in organic materials only occurred in the 1950s and 1960s [29,30]. The first real breakthrough was achieved in 1977 when Alan J. Heeger, Alan MacDiarmid, Hideki Shirakawa and coworkers discovered high-conductivity polymers by synthesizing oxidized iodine-doped polyacetylene [31]. They were jointly awarded the 2000 Nobel Prize in Chemistry which catapulted progress in the field of organic electronics.

Since inorganic semiconductors like silicon are the most widely used materials in modern electronics today, the relatively newer organic semiconductors are often viewed in comparison to them, to recognize the unique benefits provided by the latter. Inorganic semiconductors are relatively very brittle and require advanced processing conditions in order to maintain the high quality of semiconductors necessary for high performance. The temperature at which different semiconductors are processed during fabrication of TFTs and other devices is the most important and distinguishing factor to be considered. All popular semiconductors prevalent today are processed at relatively high temperatures, which limits the choice of substrates or surfaces on which devices and circuits can be fabricated, to only those which can withstand such high temperatures and limits the functionality range of the substrates available. In contrast, organic-semiconductor materials can be processed at much lower temperatures, which are much closer to room temperature. This enables the possibility of using a wide variety of alternative and new substrates, which are not compatible with high-temperature processing, but can

provide unique advantages when used to fabricate organic-semiconductor devices. For example, plastic foils can be used for mechanical flexibility in bendable or rollable applications [32–34], glass substrates can provide optical transparency [35,36], and electronic devices and circuits can potentially be fabricated on paper [37–40], textiles and fabrics [41,42] and even human skin [43,44]. Thus, a widened choice of possible substrates opens up a new dimension of possible applications with different advantages such as large-area fabrication, roll-to-roll processing along with high-throughput fabrication.

Considering the different mechanism of charge conduction in organic materials as compared to their inorganic counterparts, the electrical conductance of organic semiconductors is usually much smaller, which limits their use for high-performance circuit design. Moreover, the weaker bonding mechanisms in organic materials make them less stable against electronic noise and thermal fluctuation. There is also a higher variation between individual devices which results in a lower integration density. All these factors make it impossible for organic semiconductors to replace silicon in MOSFETs, and that is an unrealistic goal for the future development of organic semiconductors in electronic devices. Instead, the fundamental idea is the targeted development of niche applications benefiting from the unique advantage of organic semiconductors, i.e. the availability of alternative substrates to fabricate devices and circuits on.

Another major distinguishing factor with the development of organic semiconductors for electronic devices is the wide variety of materials which are chemically synthesized and investigated, instead of a single material system. This gives the possibility of selectively synthesizing and tailoring the properties of semiconductor materials depending on the target application along with other materials or processes used in device fabrication.

The emerging field of organic electronics can be categorized based on the target applications of organic materials: 1) organic light-emitting diodes (OLEDs) [45–47], 2) organic solar cells [48–50] and 3) organic field-effect transistors (OFETs). OLEDs have been extensively researched and have already been commercialized to be used in digital displays in all major electronic gadgets like television screens, computer monitors, smartphones, etc. Organic solar cells are promising, competitive devices currently facing certain hurdles towards being manufactured commercially and research is ongoing in improving their efficiencies, stability and overall performance.

In contrast, organic field-effect transistors are still much further behind in terms of research and development towards commercial products. However, a few small-scale applications have been rolled out into the market. Although significant work was done

in the 1980s for field-effect measurements in organic films, their performance was still quite poor, quantified usually in terms of the charge-carrier mobility. It was only in the 1990s, after significant efforts, that the performance of organic transistors was improved and charge-carrier mobilities became comparable to those of a-Si:H TFTs (∼ 0.1-1 cm^2/Vs). Today, organic transistors have consistently reached significantly larger charge-carrier mobilities, in the range of 1-10 cm^2/Vs, and are promising candidates for a variety of potential applications. However, there are still significant obstacles on that path in terms of device stability, reliability, reproducibility and uniformity. There is also a major gap in the fundamental understanding of the operation principles of organic transistors. Additionally, a large portion of the research efforts are also consumed in finding the optimum combination of materials, process parameters and device configurations from the wide selection variety available.

One of the primary target applications for OFETs is in the active-matrix OLED display [51], which currently uses TFTs based on LTPS and indium gallium zinc oxide (IGZO) to drive the backplane. Apart from that, other potential applications include conformable sensors [52, 53], foldable displays (e.g. e-books or e-paper) [54], soft or smart bionic and robotic devices [55–57], wearable or implantable medical devices [58], etc. Most of these target applications, if not all, are designed with a portable or wearable nature in mind and will be powered by small batteries or solar cells to ensure their lightweight nature. For this very reason, the organic transistors driving these devices have a key requirement to operate at low supply voltages. The operating voltage of a transistor is largely dictated by the capacitance of the gate dielectric, making the gate dielectric a crucial component in their development. The importance of the gate dielectric is also extended to the interface with the organic semiconductor and can have a huge impact on the overall functioning of the device. Properties of the organic-semiconductor component of the organic transistor are a subject of major focus, since charge transport in the device takes place in this region. A wide range of material and film properties are instrumental towards effective charge transport in the device, and establishing a connection between the material properties of the organic semiconductor and electrical properties of the organic transistor is of vital importance. The aspect of film thickness for these two components of the organic transistor, viz. the gate dielectric and the organic semiconductor, is a focal point in this work.

This thesis focuses on investigating ultrathin, high-capacitance, hybrid gate dielectrics and the stability of ultrathin semiconductor layers for low-voltage

organic thin-film transistors. The two components of the hybrid gate dielectric, i.e. the inorganic gate oxide and the organic self-assembled monolayer, and different aspects pertaining to them, are studied. Extending to the gate dielectric-semiconductor interface, there is a focus on the growth and morphology of organic semiconductors and the stability of ultrathin semiconductor layers at this interface.

This thesis is organized as follows. Chapter 2 provides a theoretical framework for organic semiconductors, charge transport in organic thin-film transistors and their basic operation. In addition, an introduction to dielectric properties as well as nucleation and growth properties of organic semiconductors are discussed. A basic description of all the characterization techniques used in the thesis is also detailed. Chapter 3 introduces the concept of hybrid gate dielectrics along with the significance and operating role of each component of the hybrid gate dielectric. Chapter 4 investigates the process parameters used to prepare the gate oxide, i.e. aluminum oxide (AlO_x), the first component of the hybrid gate dielectric and investigates the optimum parameter combination required to fabricate an ultrathin and dense AlO_x film as the gate oxide required for high-performance hybrid dielectrics. The relationship between surface properties of the AlO_x film and the electrical properties of the organic transistor is also established. Chapter 5 describes an in-depth characterization of the AlO_x component of the gate dielectric using advanced techniques with an atomic-scale resolution. The AlO_x films investigated in Chapter 5 are prepared using the optimum process parameters as determined in Chapter 4 and are characterized for the thickness as well as the composition of the AlO_x films. Chapter 6 investigates the second component of the hybrid gate dielectric, i.e. the self-assembled monolayer (SAM), particularly the effect of changing the thickness of the SAM using two different types of molecules used to form the SAM, and its effects on the performance of organic thin-film transistors. Chapter 6 also examines the nucleation and growth of organic-semiconductor films on gate-dielectric surfaces and the influence of different dielectric surface properties. Thereafter, Chapter 7 investigates ultrathin semiconductor layers, time-dependent morphological changes occurring in them and their stabilization using either cryogenic cooling or in-situ encapsulation towards the fabrication of ultrathin organic TFTs. Chapter 8 provides a summary of the work in this thesis and provides an outlook for the future development of organic transistors.

Chapter 2

Theory

2.1 Organic semiconductors

The unique chemistry of elemental carbon facilitates the formation of a large variety of hydrocarbon compounds, the study of which constitutes the field of organic chemistry. The family of aromatic compounds, identified by their characteristic conjugated systems, i.e. alternating single and double bonds are particularly important for the electronic properties of organic molecules. The ground state configuration of electrons in a carbon atom can be represented as: $1s^2$ $2s^2$ $2p^2$, with the four valence electrons located in the doubly-occupied $2s^2$ and the singly-occupied $2p_x$ and $2p_y$ atomic orbitals. However, carbon atoms also have the ability to form hybridized electronic configurations, in which atomic orbitals in the ground state can be imagined to be combining together and modifying themselves to form hybrid orbitals. For example, in an sp^2 hybridized configuration found in carbon atoms in conjugated systems, one 2s and two 2p ground state orbitals combine to form three sp^2 hybrid orbitals, as depicted in Fig.2.1(a). The four valence electrons of the carbon atom in an sp^2 hybridized configuration are now distributed in three singly-occupied sp^2 hybrid orbitals and one unhybridized $2p_z$ orbital. The three sp^2 hybrid orbitals are located trigonally in a single plane, while the $2p_z$ orbital is located perpendicular to this plane, as shown schematically in Fig.2.1(b).

In a typical conjugated system where carbon atoms are in the sp^2 hybridized state, each carbon atom forms two single bonds and a double bond with its neighboring atoms. The single bond is formed by the overlap of sp^2 orbitals, also known as a σ (sigma) bond, and is localized to the overlap region of the sp^2 orbitals. A double bond consists of a

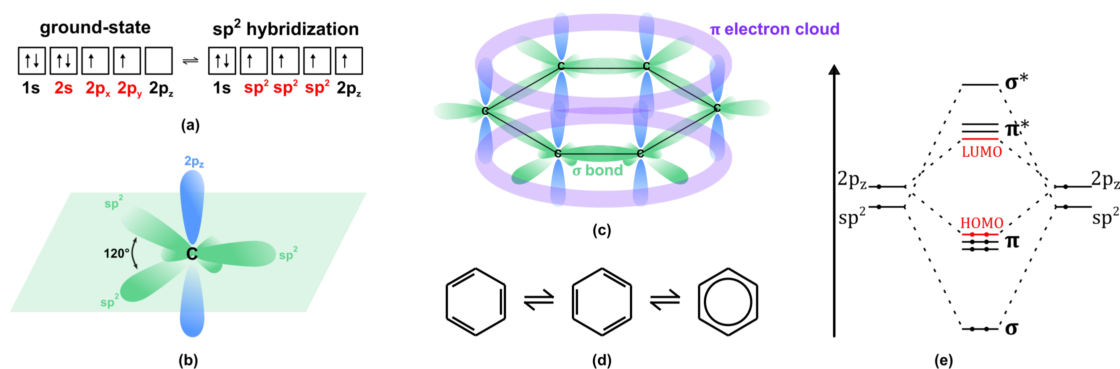


Figure 2.1: (a) Electronic configuration for a carbon atom in the ground state and after sp^2 hybridization (b) Trigonal geometry of atomic orbitals in an sp^2 hybridized carbon atom (c) σ-π bonding in a benzene molecule and delocalization of π electrons, visualized as a π electron cloud (d) Resonance structures of benzene (e) Energy level diagram depicting the energy-level splitting during bonding in a benzene molecule and the formation of HOMO-LUMO energy levels

σ bond by the overlapping sp^2 orbitals *and* a π (pi) bond formed due to the overlap of $2p_z$ orbitals.

The molecule benzene is the simplest aromatic compound and the main building block for small molecules used in organic electronics. The six carbon atoms in a benzene molecule form twelve σ bonds with the overlap of sp^2 orbitals and three π bonds by the overlap of $2p_z$ orbitals. Since the $2p_z$ orbitals are located perpendicular to the plane of the atoms, the overlap between the two lobes occurs laterally and there is zero electron density at the shared nodal plane, passing through the two bonded nuclei. As a result, compared to a σ bond, the π bond overlap is relatively weaker and the electrons in the π bonds (or π electrons) are largely delocalized among all six $2p_z$ orbitals [59]. Thus, the π electrons in a benzene molecule can be visualized as an electron cloud delocalized in the planes above and below the plane of the atoms, as shown schematically in Fig.2.1(c). The molecule benzene can be represented as either of the resonance structures shown in Fig.2.1(d) to signify delocalization of π electrons within the molecule. This delocalization of π electrons is essential to the charge transport properties of aromatic compounds. During the formation of the σ bond, the strong overlap between the sp^2 hybrid orbitals causes a large splitting of the sp^2 energy level into a bonding σ and an antibonding σ^* molecular orbital. In comparison, the energy level splitting during the formation of the π bond is much smaller because of the weak overlap of $2p_z$ orbitals, and the resulting π and π^* molecular orbitals have a much smaller energy difference. In benzene, the $2p_z$ orbital overlap leads to energetic splitting into three bonding π orbitals which are

occupied by electrons and three antibonding π^* orbitals which are vacant. The π molecular orbital with the highest energy is also called as the Highest Occupied Molecular Orbital (HOMO) and is analogous to the valence band in inorganic solids. Similarly, the π^* molecular orbital with the lowest energy is called the Lowest Unoccupied Molecular Orbital (LUMO), analogous to the conduction band. By extension, the energy difference between the HOMO and LUMO energy levels is analogous to the band gap in inorganic solids. The formation of molecular orbitals due to the energetic splitting of atomic orbitals upon bonding and the subsequent HOMO-LUMO energy levels can be seen schematically in Fig.2.1(e). The HOMO-LUMO energy difference in benzene is approximately 6.8 eV [60], making it an insulator. In the family of acenes, as the aromatic chain length increases with more benzene rings fused together, the number of $2p_z$ orbitals which overlap with each other also increases. This leads to an increased energetic splitting between the bonding and further between the antibonding molecular orbitals. As a result, a larger number of π and π^* molecular orbitals reduces the HOMO-LUMO energy difference and leads to an increased delocalization of π electrons [60]. Pentacene, which was initially one of the most popular and prominent organic semiconductors, has five benzene rings fused together and a HOMO-LUMO energy difference of approximately 2.2 eV [61–63].

The two primary classes of organic semiconductors are small molecules and polymers [64]. Small molecules, such as acenes, typically have a low molar mass which makes it easy to purify them and they are most commonly deposited by gas-phase processes such as thermal sublimation. They can also be synthesized as single crystals to study intrinsic charge transport processes [65–68]. Alternatively, their properties can be tailored with functional groups such as side chains to make them soluble for solution-processed deposition techniques. Some of the commonly used, high-performance small-molecule organic semiconductor molecules used to fabricate p-channel (hole-conducting) organic transistors are shown in Fig.2.2. The second class of organic semiconductors are polymers, which typically have a very large molecular weight and are commonly processed exclusively from solution [69–71]. The two organic semiconductors employed in this thesis are:

1. DNTT : dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
   (HOMO-LUMO energy difference = 3 eV) [72]

2. DPh-BTBT: 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (HOMO-LUMO energy difference = 3.2 eV) [73]

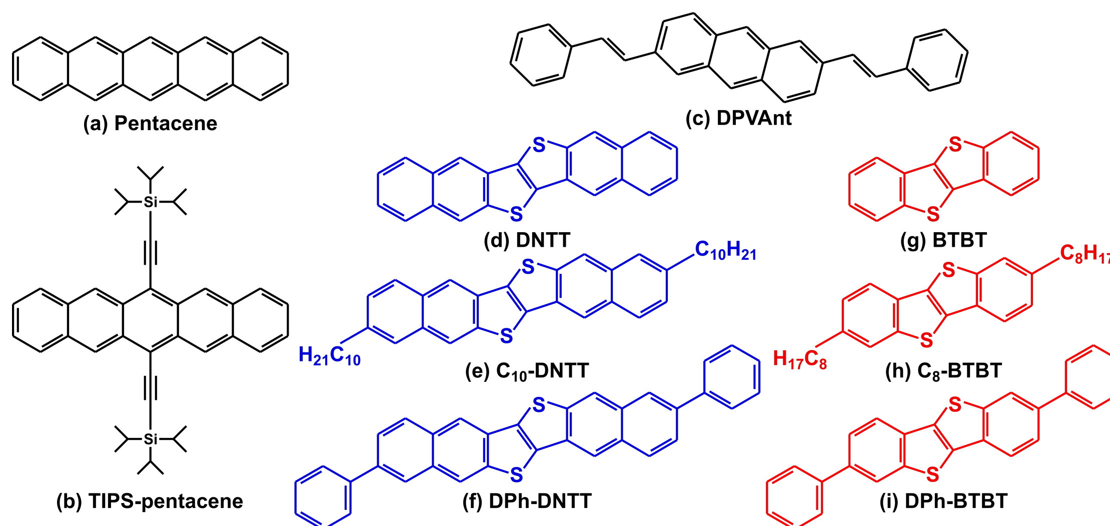


Figure 2.2: Commonly used high-performance small-molecule organic semiconductors for p-channel organic transistors (a) pentacene (b) TIPS-pentacene (c) DPVAnt (di(phenylvinyl)anthracene) (d) DNTT (dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene) and its derivatives (shown in blue) (e) C_{10}-DNTT (f) DPh-DNTT (g) BTBT (benzothieno[3,2-b][1]benzothiophene) and its derivatives (shown in red) (h) C_8-BTBT (i) DPh-BTBT

2.2 Charge transport in organic semiconductors

The delocalized nature of π orbitals in a conjugated carbon system allows for charge carriers to be transported along the molecule, i.e. *intra*molecular charge transport. However, since the dimensions of organic transistors are much larger than individual organic semiconductor molecules, *inter*molecular charge transport needs to be established as well. Essentially, efficient charge transport in the conducting channel of the organic transistor depends on the degree of π molecular orbital overlap between neighboring molecules over the length of the channel [74]. The various factors contributing to charge transport, the different attempts at modeling charge-transport behavior and strategies to enhance it based on this knowledge are further explored in this section.

In order to describe different aspects of charge transport in organic semiconductors throughout this thesis, it is important to define certain fundamental parameters associated with it. Upon applying an external electric field E, charge carriers are accelerated to a drift velocity v_{D}, and the parameter used to describe the efficiency with which electronic charges are transported through the solid is defined as the charge-carrier mobility

μ:

$$\mu = \frac{\partial v_{\mathrm{D}}}{\partial E}$$

The electrical-current density j as a result of the transport of charge carriers is determined by the charge-carrier density n and the drift velocity v_{D}:

$$\begin{aligned} j &= e \cdot n \cdot v_{\mathrm{D}} \\ &= e \cdot n \cdot \mu \cdot E \end{aligned}$$

where e is the elementary electronic charge. The electrical conductivity σ of the system, which is the ratio of the current density to the applied electric field is defined as:

$$\sigma = \mu \cdot n \cdot e$$

The conducting channel in an organic transistor is made up of several organic semiconductor molecules organized in a more or less ordered fashion, ideally with a suitable processing technique to encourage the overlap of π molecular orbitals of neighboring molecules and subsequently, efficient charge transport. The overlap of molecular orbitals during bonding leads to the splitting of discrete orbital energies, and depending on the number and proximity of neighboring molecules, the dispersion of energy levels may form an energy continuum, or an energy band. In inorganic semiconductors such as single-crystalline silicon and gallium arsenide (GaAs), atoms are bound by relatively strong covalent bonds resulting in very strong electronic orbital overlap. As a result, electronic wave functions (Bloch waves) are delocalized over large distances in the lattice and broad energy bands are formed and the charge-transport mechanism can be described as band transport. During band transport, the charge-carrier mobility decreases with increasing temperature due to phonon scattering, and transport is characterized by the temperature dependence of mobility following a power law behavior:

$$\mu \propto T^{-n} \ldots (n > 0)$$

In contrast, organic semiconductors form largely polycrystalline or even amorphous layers with molecules bound by relatively weak Van der Waals forces with greater intermolecular distances and weaker intermolecular orbital overlaps. Moreover, organic

semiconductor thin films are characterized by a lot of defects, impurities and most importantly, grain boundaries which break the periodicity of the lattice, and formation of energy bands or band transport are highly unlikely. Instead, all impurities and defects form localized states in the HOMO-LUMO energy gap, which act as charge-carrier traps. Charge transport in organic semiconductor films is therefore largely dominated by the presence and distribution of localized states.

In the case of completely amorphous organic solids, charge transport occurs by a *hopping* mechanism, where charge carriers are transported through the solid by hopping from one localized state to another. In this case, the charge-carrier mobility increases with increasing temperature and the temperature dependence of mobility in this case follows an Arrhenius equation:

$$\mu \propto exp\frac{-\Delta E_a}{k_B T}$$

where ΔE_{a} is the activation energy, i.e the energy that a localized charge carries has to absorb in order the leave the localized state and contribute to charge transport, $\mathrm{k_B}$ is the Boltzmann constant and T is the temperature.

Charge transport in polycrystalline solids, which is the form most organic semiconductor films assume, is thus a combination of coherent transport within a delocalized transport band (as observed exclusively in single crystals) and incoherent transport by thermally-activated hopping between localized states (as observed in disordered or amorphous solids).

Charge Transport Models

In order to understand and favorably tailor the electrical properties of organic thin-film transistors, it is important to develop a theoretical framework of charge transport in organic semiconductor films. However, this is extremely challenging due to the complex structure-property relationships and a wide variety of available organic semiconductors [75]. Furthermore, different fabrication processes and slight variations in the process parameters form organic semiconductor films with largely varying properties and a varying degree of impurities or defects. Therefore, no single coherent model has been developed yet to completely understand and explain the charge transport in

organic semiconductor films, like the band theory of transport for inorganic semiconductors. Nevertheless, certain models have been proposed which explain certain aspects of charge transport in specific conditions quite well, and are detailed below.

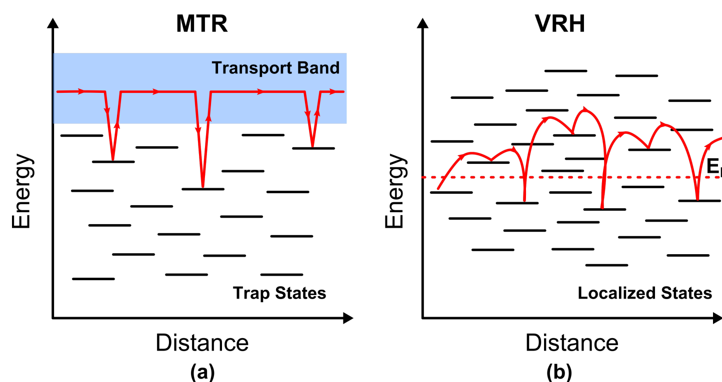


Figure 2.3: Schematic description of (a) the Multiple Trap and Release (MTR) and (b) the Variable Range Hopping (VRH) charge-transport models

Multiple Trap and Release (MTR)

The multiple trap and release model is best suited to systems with a relatively large degree of order present, i.e. a largely polycrystalline semiconductor thin film, with a minority presence of impurities, defects and grain boundaries. The model combines aspects of delocalized band transport and the presence of localized states. It assumes that charge transport takes place in an extended, narrow transport band formed by the large majority of delocalized states with localized states present in the HOMO-LUMO energy gap acting as trap states. Charge carriers in the transport band can be trapped in the localized states but with enough thermal stimulation can be released back into the transport band to contribute to charge transport, as shown schematically in Fig.2.3(a). This model was originally developed to describe the charge transport in amorphous or polycrystalline silicon TFTs and was later extended to organic semiconductors as well [76].

Variable Range Hopping (VRH)

The variable range hopping model is ideally suited to describe systems with increased disorder in the lattice, i.e. largely disordered or amorphous semiconductor films [77] in which a majority or all states are localized and there is no large-scale delocalization over

several molecules or the entire film. In this case, charges hop from one localized state to another and are transported through the solid, as represented in Fig.2.3(b).

The temperature dependence of charge transport, or the charge-carrier mobility, is closely related to the degree of molecular order and the energy distribution of electronic states in the solid. In highly pure organic single crystals, similar to inorganic semiconductors, the charge-carrier mobility increases with a decrease in temperature. This is primarily because charge-carrier transport is predominantly coherent and the influence of phonon scattering on the mean free path of charge carriers decreases with decreasing temperature. On the other hand, in amorphous layers, the charge-carrier mobility decreases with decreasing temperature because charge transport takes place exclusively by thermally activated hopping between localized states. For organic semiconductors which are most commonly fabricated into polycrystalline layers, different temperature dependencies are observed based on the degree of molecular order and amount of defects or impurities present. The temperature dependence of the mobility observed in organic solids can be described by the following equation:

$$\mu(T) = \mu_o\Big(\frac{T}{T_o}\Big)^{-n} exp\Big[\frac{-E_a}{k_B T}\Big]$$

where E_a is the *activation energy*, i.e. the energy that a localized charge carrier has to absorb in order to leave the localized state and contribute to charge transport, and μ_0 is the intrinsic charge-carrier mobility of the semiconductor.

The morphology of the organic semiconductor films and the orientation of molecules within is thus of extreme importance as the crystallinity of the film determines the degree of π orbital overlap and efficiency of charge transport. Different approaches can be utilized towards obtaining a suitable film morphology, and for a particular organic semiconductor, optimizing the deposition process plays a very important role. The influence of different parameters during the deposition process and their suitable manipulation towards high-quality semiconductor films is explained in Section 2.5.4. A second approach entails designing and synthesizing new organic semiconductor molecules by modifying their chemical structure to suitably tailor the crystalline nature and thereby the electronic properties of organic semiconductor films. Examples of this approach are given

below.

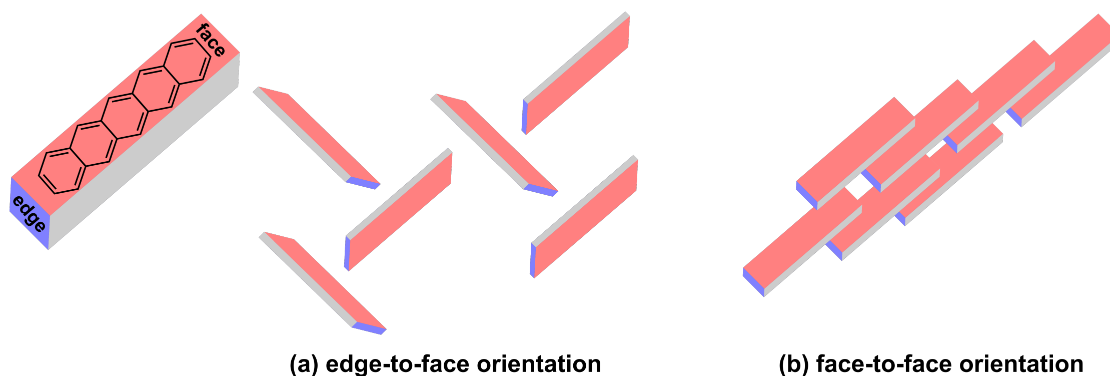


Figure 2.4: Schematic representation of the different molecular orientations: (a) edge-to-face and (b) face-to-face orientations of the organic semiconductor molecule pentacene

- The organic semiconductor molecule pentacene has two different possible molecular orientations, viz. 'edge-to-face' and 'face-to-face', in which the the face-to-face orientation leads to more efficient charge transport due to a larger degree of π orbital overlap. The molecule pentacene was modified by introducing bulky side groups at the 6, 13 positions to synthesize the molecule TIPS-pentacene (6,13-bis(2-(tri-isopropylsilyl)ethynyl)pentacene) [78], shown in Fig.2.2. The targeted synthesis of TIPS-pentacene suppressed the occurrence of edge-to-face molecular orientations and increased the degree of π-orbital overlap, improving the charge-transport properties [79]. However, the preferred 'face-to-face' packing mode is only obtained by a very specific solution-processing technique and TIPS-pentacene cannot be used to fabricate organic TFTs in which the organic semiconductor is vacuum-deposited.

- The ionization potential refers to the energy difference between the HOMO energy level and the vacuum level, i.e. the energy necessary to withdraw an electron from the HOMO energy level to ionize the molecule. Increasing the ionization potential of an organic semiconductor increases its stability against undesired and often irreversible oxidation reactions, and the loss of delocalized molecular orbitals due to oxidation is prevented. Within the family of unsubstituted acenes, the ionization potential increases as the number of aromatic rings decreases, i.e. the size of the molecule decreases. However, a reduction in the size of the molecule is unsuitable as it significantly reduces the molecular interactions, the quality of crystal formation and the semiconducting property of the molecule. A better approach

to increase the ionization potential of organic semiconductor molecules without decreasing their size is to synthesize molecules with several weakly coupled aromatic π systems as shown in Fig.2.2, e.g. the organic semiconductor molecule DPVAnt (di(phenylvinyl)anthracene) [80, 81]. Similarly, the molecules DNTT and BTBT were synthesized to obtain a larger ionization potential and hence better air-stability along with an improved crystal structure as compared to pentacene. Several derivatives of DNTT (dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene) [72] and BTBT (benzothieno[3,2-b][1]benzothiophene) [73] have comparable, if not larger, charge-carrier mobilities than pentacene and are among the most popular small-molecule organic semiconductors today, and will also feature in this work.

2.3 Organic thin-film transistors

Organic transistors are fabricated as thin-film transistors (TFTs), which are field-effect transistors with all the different components deposited sequentially as thin films. In an organic TFT, the active component is an organic semiconductor (discussed in Section 2.1), with the organic semiconductor molecules usually deposited as a polycrystalline thin film. To establish field-effect behavior, the organic semiconductor film is separated from the gate electrode by an insulating layer, called the gate dielectric. There are two other electrodes in contact with the semiconductor layer, namely the source contact and the drain contact, for the injection and extraction of charge carriers respectively. Depending on the order of depositing the various components and their relative arrangement with each other, there are four different TFT architectures possible, schematically shown in Fig.2.5: (a) bottom-gate (inverted) staggered (b) bottom-gate (inverted) coplanar (c) top-gate staggered and (d) top-gate coplanar.

The choice of the TFT structure influences the available area for charge carriers to be transported and subsequently other TFT performance characteristics. This thesis includes the two bottom-gate (inverted) structures, either in top-contact (inverted-staggered) or in bottom-contact (inverted-coplanar) architectures, shown schematically in Fig.2.5(a) and (b) respectively. The different components and the basic parameters involved in TFT operation can be seen in Fig.2.6. Typically, by applying a voltage V_{GS} to the gate electrode with respect to the grounded source electrode, an electric field is created in the semiconductor due to charge polarization in the gate dielectric. Thus,

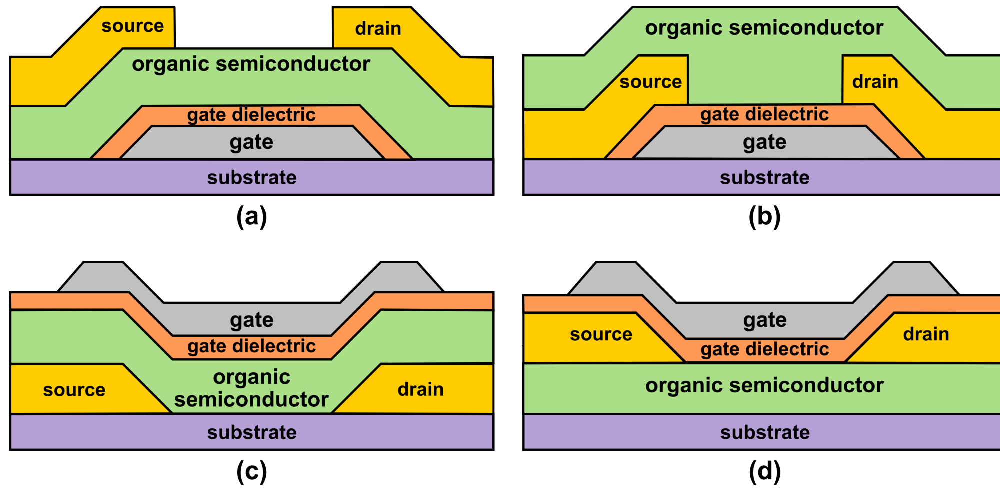


Figure 2.5: Schematic representation of organic TFT architectures: (a) bottom-gate (inverted) staggered (b) bottom-gate (inverted) coplanar (c) top-gate staggered and (d) top-gate coplanar

the operation of the transistor resembles the charging of a capacitor which results in the accumulation of mobile charge carriers in the semiconductor layer to form a conductive path, or the conducting channel in the TFT. The formation of the channel and operation of the transistor are thus controlled by the application of the voltage V_{GS}, establishing the switching characteristic of the transistor. The flow of charge carriers from the source contact to the drain contact, i.e. the drain current I_D, is controlled by a second voltage V_{DS} applied to the drain contact with respect to the grounded source contact. The magnitude of the drain current and thereby the different operation regimes are controlled by the voltage V_{DS}.

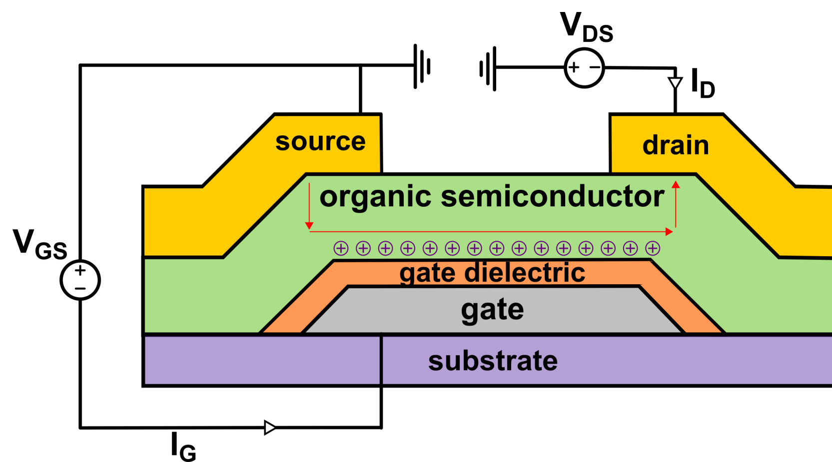


Figure 2.6: Schematic representation of an organic TFT with the basic components, electrical parameters and formation of the conduction channel displayed

In contrast to transistors with inorganic semiconductors (e.g. MOSFETs), organic transistors are not specifically doped to facilitate the transport of one type of charge carrier in the channel. The semiconductor films are usually intrinsic, both in the channel as well as at the contacts. Instead, the type of charge carriers and thereby the polarity of the transistor is decided by the relative position of the Fermi energy level (E_F) of the contact material and the HOMO/LUMO energy levels of the organic semiconductor, as shown in Fig.2.7. If the energy barrier between the Fermi energy level of the contact and the HOMO energy level of the organic semiconductor is sufficiently small, holes can be efficiently injected and extracted and the transistor is a p-channel transistor. Similarly, if the energy barrier between the Fermi energy level of the contact and the LUMO energy level of the organic semiconductor is sufficiently small, it is easier to inject and extract electrons in the channel, and the transistor is an n-channel transistor. To avoid undesired charge injection of the opposite charge carriers at the drain contact, it is preferred to have the largest possible energy barrier between the contacts and the opposite energy level of the semiconductor. That is, for a p-channel transistor, a large energy barrier between the LUMO level and the contacts is desired and for an n-channel transistor, there should a large energy barrier between the HOMO level of the semiconductor and the contacts. For many organic semiconductors, the energy difference between the HOMO

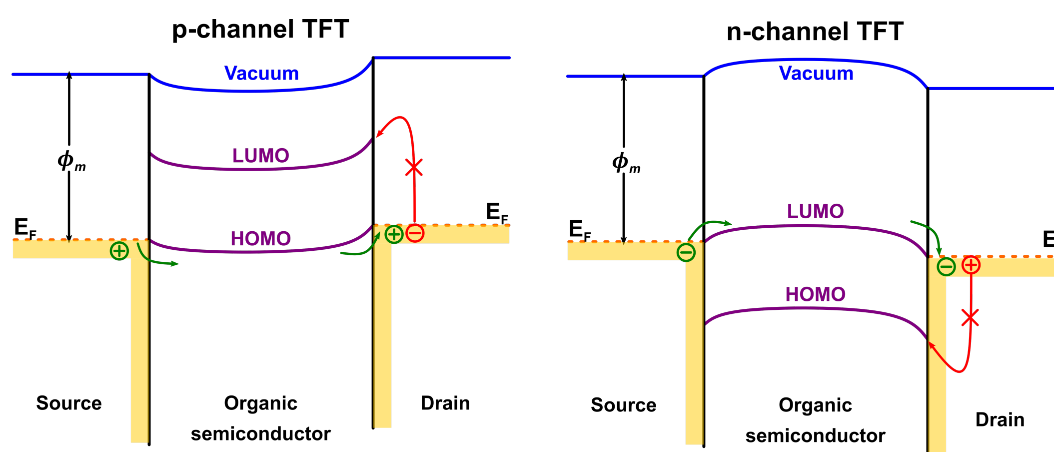


Figure 2.7: Relative alignment of energy levels between the Fermi energy level (E_F) of the contact material and HOMO-LUMO energy levels of the organic semiconductor in p-channel and n-channel organic TFTs

and LUMO energy levels is reasonably large so that only one type of charge carrier can be efficiently injected and extracted. For example, the HOMO level for pentacene is approximately -5 eV [61–63] and approximately -5.44 eV for DNTT [72], when used with gold contacts, where gold has a normal work function of around 5.2 ± 0.1 eV, with

possible variations due to exposure to air or other layers in the device [82] and makes this combination suitable for a p-channel transistor.

2.3.1 Current-voltage characteristics

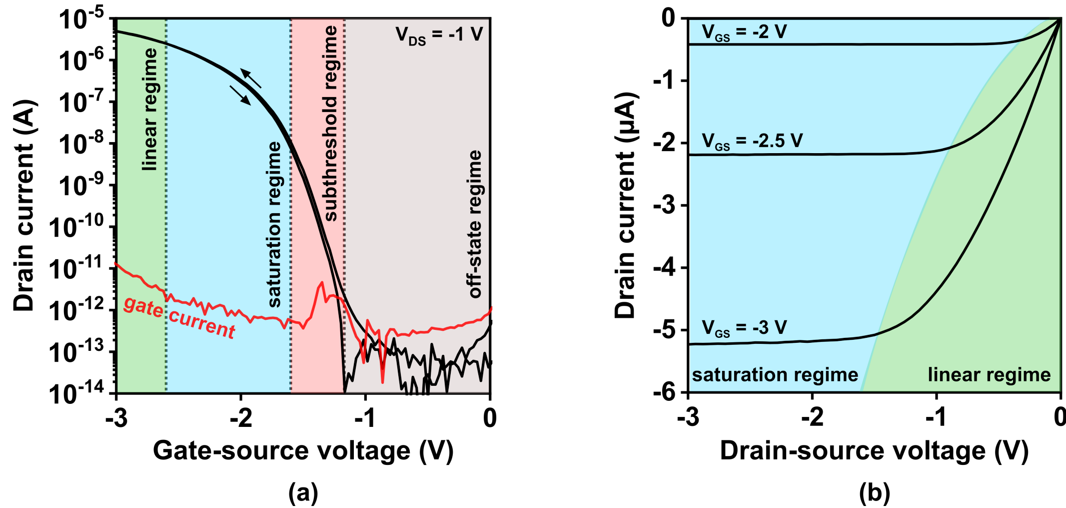


Figure 2.8: Current-voltage characteristics of a p-channel organic transistor with different operation regimes (a) A sample transfer curve, i.e. the drain current I_D as a function of the gate-source voltage V_{GS} at a constant drain-source voltage V_{DS}. The gate current is shown in red. (b) A sample output curve, i.e. the drain current I_D as a function of the drain-source voltage V_{DS} for a set of constant gate-source voltage V_{GS} values

Since only p-channel TFTs will be investigated in this thesis, the transistor operation of a p-channel TFT will be discussed in detail in this section, but the same equations also apply to n-channel TFTs by reversing the polarity of the charge carriers. On applying the voltage V_{GS} between the gate electrode and the source contact, charge carriers are accumulated in the semiconductor due to charge coupling across the dielectric close to the semiconductor-dielectric interface. Since organic semiconductors are normally intrinsic and the polarity of the channel is decided according to the relative energy levels of the semiconductor and the contact material, the accumulation of charge carriers is the formation of the conduction channel of the transistor. This conducting channel is situated only in the first few monolayers of the organic semiconductor layer, close to the semiconductor-dielectric interface [83, 84], i.e. the thickness of the channel relative to the semiconductor layer thickness is extremely small. The charge-sheet model assumes the thickness of the channel is zero [85] and simplifies the problem so that the metal-insulator-semiconductor structure is modeled as a parallel-plate capacitor, with the gate

electrode and the semiconductor layer acting as the two *plates*, separated by the dielectric insulator.

The voltage V_{GS} creates an electric field, which modulates the resistance at the interface between the organic semiconductor and the dielectric. Considering a resistance dR over a short distance dx in the channel :

$$dR = \frac{dx}{W\mu Q(x)} \tag{2.1}$$

where W is the channel width and Q(x) is the surface-charge density. For the organic TFT, the potential at the source contact is V_{GS}, and on application of the voltage V_{DS}, the potential at the drain contact is V_{GS}-V_{DS}. In general, the potential in the channel at any position x will be V_{GS}-V(x). Thus, the charge density in the channel Q_s(x) can be expressed as a function of the capacitance and the potential in the channel as :

$$Q_{\mathrm{s}}(x) = C_{\mathrm{diel}}[V_{\mathrm{GS}} - V(x)]$$

In real devices, the semiconductor layer is often characterized by impurities, defects and grain boundaries which act as charge-trapping sites. In addition, a work-function difference and donor/acceptor states at the interface result in an offset voltage required to be overcome for the accumulation of mobile charge carriers in the channel. This is termed as the **threshold voltage $\mathbf{V_{th}}$**. Thus, to describe the charge density in real devices, Q_s(x) is expressed as:

$$Q_{\mathrm{s}}(x) = C_{\mathrm{diel}}[V_{\mathrm{GS}} - V_{\mathrm{th}} - V(x)] \tag{2.2}$$

Substituting $dR = dV/dI$, and Eqn.2.1 in Eqn.2.2, and integrating x over the channel length L:

$$I_D \int_0^L dx = \mu C_{\mathrm{diel}} W \int_0^{V_{\mathrm{DS}}} dV[V_{\mathrm{GS}} - V_{\mathrm{th}} - V(x)]$$

Under the given potentials at the source and drain contacts respectively as discussed above, and integrating the above equation, we obtain the expression for the drain current I_D in this operation regime:

$$\begin{gathered} I_{D,lin} = \mu C_{\mathrm{diel}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{th}} - \frac{V_{\mathrm{DS}}}{2}) V_{\mathrm{DS}} \\ \text{for } |V_{\mathrm{GS}} - V_{\mathrm{th}}| > |V_{\mathrm{DS}}| > 0 \end{gathered} \tag{2.3}$$

The following assumptions have also been made in deriving the above equation:

1. Gradual Channel Approximation : The variation of the electric field along the channel (which drives the drain current) is assumed to be much smaller in comparison to the variation of the electric field perpendicular to the channel from the gate to the semiconductor (which determines the accumulation of charge carriers). [85, 86].
2. The charge-carrier mobility μ is independent of the drain-source voltage V_{DS}.

The above derivation of the transistor's current-voltage characteristics is a simpler version allowed by the assumptions made [87]. A more complex derivation of transistor characteristics can be found in [88, 89].

2.3.2 Operation Regimes

Linear Regime

Eqn.2.3 describes the drain current I_D for the condition: $|V_{GS} - V_{th}| >> |V_{DS}|$, in which the conducting channel is nearly uniform and can be modeled as a resistor as described above. Considering Eqn.2.3 and the assumed condition, the magnitude of $\frac{V_{DS}}{2}$ is negligible in comparison to the magnitude of (V_{GS}-V_{th}) and the equation can be simplified to assume a linear dependence of I_D on V_{DS} and operation under this condition is termed as the linear operation regime. For practical measurements, for larger values of V_{DS} at the end of the linear regime, I_D has a parabolic dependence on V_{DS} at a constant V_{GS}, as can be observed in Fig.2.8(b).

Saturation Regime

When V_{DS} is increased further in magnitude than in the linear regime, the slope $\frac{\partial I_D}{\partial V_{DS}}$ gradually decreases due to a smaller number of accumulated charges on the drain side, until I_D reaches a maximum value at the condition V_{GS}-V_{th}=V_{DS}. At this point, there are almost no accumulated charges at the drain-contact side, which is termed as the *pinch-off point*. With a further increase in V_{DS}, the pinch-off point moves slightly further away from the drain contact but still in close proximity as compared to the

source contact, and there is no accumulation of charge carriers at the drain contact in this state. By substituting $V_{DS}=V_{GS}-V_{th}$ in Eqn.2.3, the expression for the drain current in the saturation regime can be obtained:

$$I_{\mathrm{D,sat}} = \mu C_{\mathrm{diel}} \frac{W}{2L}(V_{\mathrm{GS}} - V_{\mathrm{th}})^2 \quad \text{for } |V_{\mathrm{DS}}| > |V_{\mathrm{GS}} - V_{\mathrm{th}}| > 0 \tag{2.4}$$

This operation regime is called the saturation regime because the drain current is *saturated*, i.e. it no longer depends on the drain-source voltage V_{DS}, as seen in Fig.2.8(b).

Off-state Regime

The equations for the drain current in the linear and the saturation regimes are only valid upon formation of a charge-sheet layer, i.e. only if $V_{GS} > V_{th}$, since V_{th} is the voltage required to overcome all the obstacles to accumulate charge carriers in the channel. When V_{GS} is much smaller than V_{th}, the transistor is in the *off-state* and the current in this operating condition is determined by the band gap or the doping condition. The current in this transistor operation regime, the *off-state current* I_{Off} should be as small as possible to reduce the power consumption of the transistor.

Subthreshold Regime

When the gate-source voltage V_{GS} is slightly smaller than the threshold voltage V_{th}, but larger than the switch-on voltage, the free carrier concentration in the channel is quite small. The switch-on voltage V_{so} is the gate-source voltage at which the drain current starts increasing beyond the off-state. The drain current in the subthreshold regime is due to charge carriers which are injected in the semiconductor layer by thermal excitation and have crossed the energy barrier at the source contact and have diffused to the drain contact. The drain current depends exponentially on V_{GS} in this regime, given by the following expression:

$$|I_{\mathrm{D}}| = I_{\mathrm{o}} exp\Big(\frac{e|V_{\mathrm{GS}}|}{nk_B T}\Big) \tag{2.5}$$

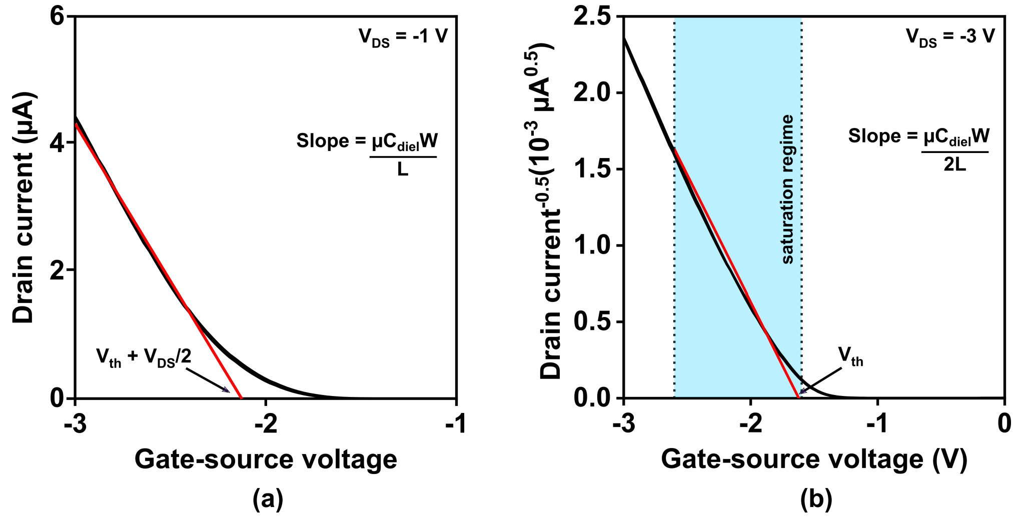


Figure 2.9: Extraction of the charge-carrier mobility and the threshold voltage from the slope and the intercept of experimentally measured transistor characteristics in (a) the linear operation regime and (b) the saturation operation regime

2.3.3 TFT Operation Parameters

Charge-carrier mobility

The charge-carrier mobility can be extracted by fitting the measured transfer curves according to Eqn.2.3 and Eqn.2.4, if the curves for $I_D(V_{GS})$ in the linear regime and $\sqrt{I_D}(V_{GS})$ in the saturation regime are straight lines. In that case, the mobility can be calculated from the slope of the curves as shown in Fig.2.9.

In case the extracted curves are not straight lines, it is better to calculate the differential charge-carrier mobility pointwise in the respective regimes according to the following equations:

$$\mu_{\text{lin}}(V_{\text{GS}}) = \frac{L}{WC_{\text{diel}}V_{\text{DS}}}\left(\frac{\partial I_D}{\partial V_{\text{GS}}}\right) \tag{2.6}$$

$$\mu_{\text{sat}}(V_{\text{GS}}) = \frac{2L}{WC_{\text{diel}}}\left(\frac{\partial \sqrt{I_D}}{\partial V_{\text{GS}}}\right)^2 \tag{2.7}$$

The charge-carrier mobility μ is one of the most important parameters for quantifying the performance of organic TFTs. The mobility can depend on a wide range of parameters such as the degree of π orbital overlap between neighboring molecules, the chemical purity of the organic semiconductor, the degree of molecular order in the semiconductor layer and the density and energy distribution of trap states. The influence of some of

these factors as modulated at the dielectric-semiconductor interface are examined in detail in this thesis.

Threshold voltage

An ideal gate dielectric has a large energy band gap with no electronic states present either within the gate dielectric layer or at the interface with the semiconductor. However, in reality, the structural and chemical defects in the dielectric layer lead to the formation of trap states in the semiconductor layer as well as at the dielectric-semiconductor interface. Along with this, there is often a mismatch in energy levels between the semiconductor and the gate-electrode metal. A non-zero gate-source voltage, defined as the threshold voltage, must be applied to overcome these effects to generate charge carriers in the channel, i.e. to fill the trap states and shift energy levels to reduce charge injection barriers. More detailed accounts of the threshold voltage and its significance can be found in the following research articles [90–92]. There are several methods proposed to determine the threshold voltage for organic TFTs [93–96]. Commonly, the threshold voltage can be extracted from the transfer curves by fitting the Eqn.2.3 and Eqn.2.4, as shown in Fig.2.9. The threshold voltage will be an important parameter in discussing the function of self-assembled monolayers in hybrid dielectrics in Chapter 6.

Subthreshold swing

As mentioned in subsection 2.3.2, the subthreshold regime is characterized by a diffusion-dominated current in the channel and the drain current depends exponentially on the gate-source voltage. The reciprocal of the slope of the transfer curve in this region, i.e. $\frac{\partial V_{\mathrm{GS}}}{\partial \log I_{\mathrm{D}}}$ is defined as the subthreshold swing.

$$\begin{aligned} S &= \frac{\partial V_{\mathrm{GS}}}{\partial \log I_{\mathrm{D}}} \\ &= \ln 10 \frac{k_B T}{e}\left(1 + \frac{e N_{\mathrm{it}}}{C_{\mathrm{diel}}}\right) \end{aligned} \tag{2.8}$$

where $\mathrm{N_{it}}$ is the concentration of electrically active impurities at the gate dielectric-semiconductor interface. The subthreshold swing is an indication of the quality of the gate dielectric and the dielectric-semiconductor interface and is considered as an important parameter to qualify the dielectric in this thesis.

Current on-off ratio

The current on-off ratio is the ratio of the drain current in the on-state to the drain current in the off-state. The on-state current is the drain current at the maximum value of the gate-source voltage (in magnitude) and the off-state current is measured at the start point of the V_{GS} sweep. A large value of the current on-off ratio is desired for low power consumption and large noise margins of circuits with the organic TFTs.

Gate current

The gate current is a result of leakage through the gate dielectric, shown in red in Fig.2.8 and should be as small as possible. The gate current is quantified at the largest value of the gate-source voltage applied (in magnitude), as often the gate leakage current is higher with higher values of the gate-source voltage applied. The gate current will be used as an important parameter to determine the quality of the gate dielectric in this thesis.

2.4 Dielectric properties

A large part of this thesis focuses on the gate dielectric component of the organic TFT and the effect of dielectric properties on TFT performance. For this purpose, it is important to review some basic principles of dielectric materials and their properties. The gate dielectric material employed in Si-MOSFETs for the longest time was SiO_2 and the strategy for improving circuit performance was circuit element shrinkage till the fundamental limits of the material were reached, leading to a requirement for new materials. Particularly in the case of SiO_2, the need for high gate-dielectric capacitance for submicron devices and circuits required the aggressive scaling down of the dielectric thickness because of the relatively small dielectric constant of SiO_2 ($k = 3.9$). Unfortunately in ultrathin SiO_2 films, the tunneling current increases exponentially. It dominates the leakage current, heavily compromises the device performance and leads to a large power dissipation [97]. Similarly for organic TFTs, the strategy towards low operating voltages is to enhance the gate-dielectric capacitance by using high-k materials. This section will

examine basic dielectric properties and their operating principles. A more detailed explanation about the requirements of dielectric materials for organic TFTs, the different materials used and strategies explored in this thesis are given in Chapter 3.

A dielectric or insulator is defined as a material with an absence of charge transport, i.e. a material with ideally a large band gap and in principle, no electronic states in the band gap for valence electrons to be excited into. An ideal insulator environment can only be found in a vacuum dielectric. When a reasonable amount of electric field is applied to non-ideal insulators, there is a shift in charge distribution which leads to field-induced polarization that characterizes dielectric behavior. The figure of merit for a dielectric material is the capacitance per unit area (C_{diel}), i.e. the ability to store electrical charge at a given voltage. On applying a voltage V to two electrodes separated by a distance d in vacuum, an electric field E is created :

$$E = \frac{V}{d}$$

The charge per unit area Q created is then proportional to the electric field:

$$\begin{aligned} Q &= \varepsilon_0 E \\ &= \frac{\varepsilon_0 V}{d} \end{aligned}$$

where ε_0 is the absolute dielectric permittivity in vacuum. If a dielectric material with a relative permittivity (also know as the dielectric constant) of k is introduced between the electrodes, the capacitance can then be defined as :

$$\begin{aligned} C_{\text{diel}} &= \frac{Q}{V} \\ &= \frac{\varepsilon_0 k}{d} \end{aligned} \tag{2.9}$$

(The relative permittivity k for vacuum is 1)

The dielectric properties of a material and its dielectric response to an electric field depend on the frequency of the electric field. The charge-density fluctuations developed as a response depend on the nature of the material and the dominant polarization mechanism operating according to the frequency of the applied electric field. The main types of polarization mechanisms are as follows.

- **Electronic polarization** occurs at frequencies up to 10^{15} Hz and occurs when

the applied electric field distorts the negative electronic cloud around the positive atomic nuclei in the direction opposite to the field. For crystals in which the atoms are well locked into the lattice structure, electronic polarization dominates the polarization mechanism.

- **Ionic polarization**, as the name suggests, typically occurs in ionic compounds and responds to field frequencies up to 10^{12} Hz. Upon applying an electric field, the cations and anions are displaced in opposite directions, leading to charge separation and field-induced polarization.

- **Orientational polarization** arises when the material contains a permanent dipole moment, typically found in polymers and dipolar moieties in polymers as well as in complex oxides, which rearranges on application of an electric field. For most polymers, a combination of orientational polarization and chain relaxation dominate the dielectric behavior. The relaxation frequencies for orientational polarization range from 10^8-10^{10} Hz.

- **Interfacial polarization** contributes to dielectric behavior at relatively lower frequencies (10^6 Hz) and is usually observed in polycrystalline solids and hybrid systems. It occurs when there is charge accumulation at an interface in a heterogeneous system and affects both bound as well as free charges. Interfacial polarization is most relevant to the dielectric materials and material systems discussed in this thesis.

- **Electrode or electric-double-layer (EDL) polarization** also occurs at extremely low frequencies, lower than 10^3 Hz. All electric or ionic conducting systems contain free charges and/or ions which move toward the electrode or the sample interface upon applying an electric field. This movement leads to the formation of electric double layers (EDLs) in these regions which constitute the thickness of the capacitor. This form of polarization is most relevant for electrolyte insulators, which are frequently used in organic transistors aimed towards bioelectronics applications.

The frequency response of areal capacitance depends on the relative permittivity (k) of the material, as shown in Fig.2.10 [98]. In high-quality low-k materials ($k \leq 3.9$), the capacitance is stable over a large range of frequencies because the major contribution

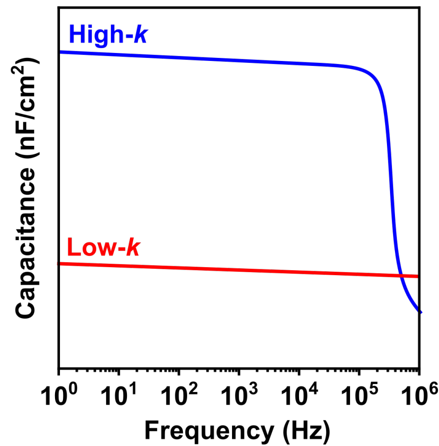


Figure 2.10: Comparison of the frequency-dependent areal capacitance of high-k and low-k dielectric films. Adapted from [98]

comes from electronic polarization. However, for high-k materials ($k > 3.9$), the capacitance may decrease at higher frequencies because the polarization in high-k materials may be unable to follow the change of a high-frequency electric field. This is particularly important when choosing dielectric materials for high-frequency applications of organic transistors.

For inorganic dielectrics, such as metal oxides or nitrides, the band gap (E_g) is approximately inversely proportional to the relative permittivity (k), which plays a crucial role in choosing an appropriate material for the dielectric. For higher capacitances, i.e. higher charge-storing abilities at lower voltages, a larger dielectric constant k is desired, but this might mean choosing a dielectric material with a narrower band gap. Although a smaller band gap can be chosen to enhance k, a large band gap is desired to suppress charge injection from the electrodes and to reduce charge generation due to thermal and photoexcitation processes.

2.4.1 Capacitance Measurement

A schematic representation of the method used to measure the gate-dielectric capacitance of gate dielectrics in organic transistors employed in this thesis is shown in Fig.2.11(a). A small AC signal of known frequency and amplitude is applied to the capacitor. The displacement current (I_{disp}) is converted to an AC voltage using a low-noise amplifier,

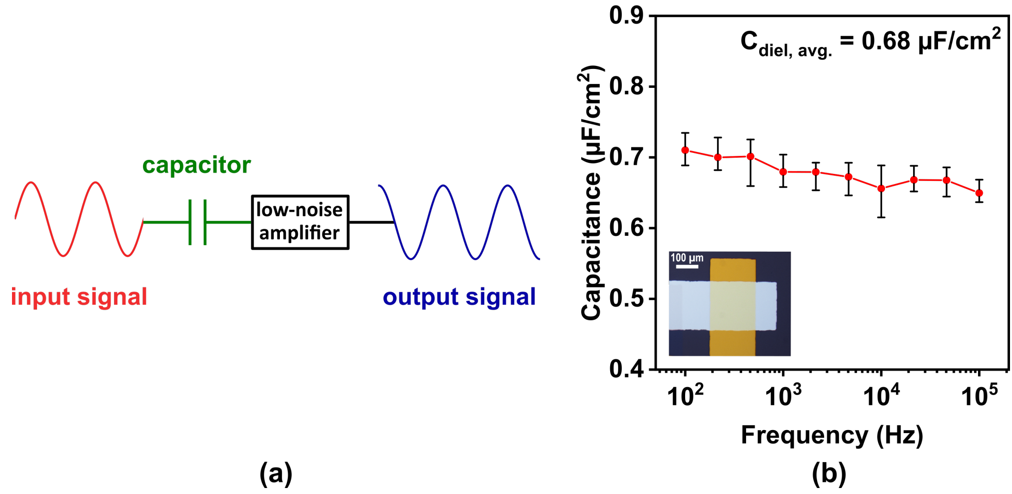


Figure 2.11: (a)Schematic representation of the capacitance measurement setup (b) An example of a frequency-dependent capacitance measurement performed on an AlO_x/phosphonic acid-SAM hybrid gate dielectric with an optical image of a capacitor (inset)

and the capacitance (C) can be calculated using the following equation:

$$I_{\mathrm{disp}} = C\frac{dV}{dt} \tag{2.10}$$

It is important to note here that the displacement current does not actually flow through the gate dielectric due to a potential difference such as in a resistive current, but instead is a result of a change in the potential difference and flows only between the gate dielectric and the power source, as indicated by Eqn.2.10. The measurement is performed multiple times by varying the frequency over a defined range suitable for the dielectric, and the calculated values of the capacitance are averaged over this range and normalized for the area of the capacitor. A sample measurement performed on a hybrid gate dielectric can be seen in Fig.2.11(b).

Ideally, when dielectric materials are used in electrical devices like transistors, they should be completely insulating against electrical conduction, because of the absence of electronic states in the band gap for valence electrons to be excited into. However, in reality, dielectric materials have localized states near the Fermi energy level (E_F), with the electronic wave functions decaying exponentially over the scale of the localization length. In real devices, upon applying an electric field, these states contribute to a current flow through the dielectric material known as the leakage current, or gate current I_G in transistors. Conduction through the dielectric material occurs through certain mechanisms, briefly described below:

- **Direct or quantum tunneling** occurs through very thin dielectric layers where the thickness of the dielectric layer is comparable to the localization length and charge carriers tunnel directly across the dielectric. The rate of coherent tunneling decreases exponentially with an increase in the dielectric thickness, and this process is independent of the temperature. Under high electric fields, which exceed the barrier height, the tunneling rate increases and field emission is induced. This specific type of mechanism is referred to as Fowler-Nordheim tunneling and the rectangular barrier in direct tunneling is modified to a triangular shaped one. direct tunneling is usually applicable for transport through self-assembled monolayers, which are considered in gate dielectrics in this thesis.

- **Indirect or diffusive tunneling** occurs in the case of thick dielectric barriers and a high density of localized states, in which electrons tunnel through consecutive states in a series of discrete steps. This tunneling mechanism is also temperature independent and is predominant in thick dielectric layers at extremely low temperatures.

- **Hopping** is a thermally activated electron transfer process which is dominant at low electric fields and moderate temperatures. Similar to diffusive tunneling, electrons travel between one or more sites and the process follows a classic Arrhenius temperature dependence. The rate of conduction by hopping depends inversely on the thickness of the dielectric. For thicker dielectrics, the distance is too great for cohesive tunneling, but electrons can travel more efficiently by hopping between sites.

- The **Poole-Frenkel effect** accounts for charge-carrier traps in hopping electron transport and is attributed to the lowering of Coulombic trapping barriers within the molecule by the applied electric field. The Poole-Frenkel effect explains electrical conduction in organic semiconductors when trapped electrons contribute to the electric current. This effect usually occurs at high temperatures and intermediate electric fields.

- **Schottky emission** explains the electron transfer mechanism at interfaces. A Schottky barrier is formed due to misaligned energy levels of two materials at an interface and a partial charge transfer occurs from one layer to the other. The formation of a Schottky barrier leads to the generation of a depletion layer and

electrostatic charges in which electrons can be injected through the interface once they have sufficient thermal energy to surmount the potential height.

When the voltage applied across a dielectric is increased beyond a certain threshold, it imparts sufficient energy for the electrons to be excited into the band. This voltage is called the breakdown voltage and the capacitor loses its dielectric properties at this voltage. For certain dielectric materials, a sharp breakdown voltage cannot be observed and the traditional definition of the breakdown voltage is not a useful metric. In these cases, the breakdown voltage is determined when the current through the dielectric crosses a certain threshold, at which point the dielectric loses its insulating properties. The desired threshold for the current through the dielectric and the voltage at which this phenomenon occurs must be taken into account while choosing a material for certain device and circuit design applications.

2.5 Growth and morphology of organic semiconductor films

Similar to inorganic semiconductors, organic semiconductors in the form of aromatic hydrocarbons, can also be synthesized as molecular crystals. However, the intermolecular Van der Waals bonding in organic single crystals is much weaker and negatively impacts their periodic arrangement and size. As a result, the chemical purity and crystalline quality of even the best organic single crystals cannot be compared to those of inorganic semiconductors. Instead, organic semiconductors are best suited for the production of polycrystalline layers, either from solution or by vacuum-deposition methods. Particularly small-molecule organic semiconductors, such as unsubstituted acenes, are practically insoluble in organic solvents and are almost always deposited as thin layers with relative ease by thermal sublimation and de-sublimation in vacuum. Since only vacuum-deposition techniques for small-molecule organic semiconductor films are discussed in this thesis, only those will be considered for an in-depth analysis.

As discussed in section 2.2, charge transport is promoted by molecular orbital overlap between neighboring molecules, and therefore, the morphology of organic molecules in a polycrystalline film must be conducive to molecular orbital overlap and superior charge transport properties. The underlying surface for organic semiconductor deposition is of utmost importance in this respect, as depicted schematically in Fig.2.12.

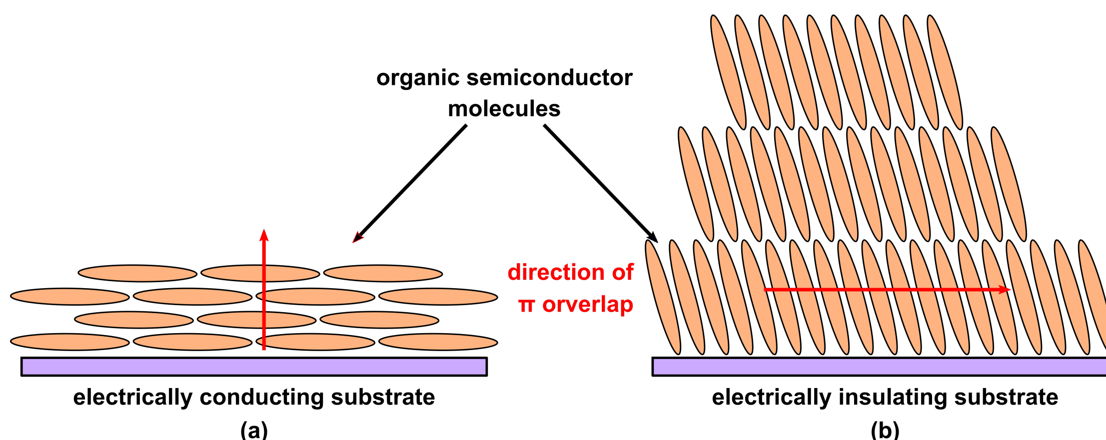


Figure 2.12: Schematic representation of the orientation of organic semiconductor molecules on (a) an electrically conducting and (b) an electrically insulating substrate with the direction of π-orbital overlap in each case depicted in red

If we consider the organic semiconductor pentacene, the molecules lie flat on an electrically conductive substrate (e.g. metals) due to the strong interactions between the molecules and the substrate. However, on an electrically non-conductive substrate, the molecule-substrate interactions are relatively weaker and the longitudinal axis of the molecules is now perpendicular to the substrate surface. In this configuration, where the molecules are standing upright on the surface, the direction of π overlap is parallel to the substrate, and this configuration of molecules is most suitable for charge transport. Since the organic semiconductor is deposited on the gate dielectric surface, the dielectric-semiconductor interface and the surface properties of the dielectric play a vital role in the growth and morphology of the semiconductor film. The nucleation and growth processes of these films and thereby their thin-film morphology are crucial to the charge-transport properties of organic transistors. This section will examine the different growth mechanisms, influential factors for suitable film morphology and the relationship between the structural and electronic properties of organic semiconductor films.

2.5.1 Thermodynamic considerations of vapor nucleation and growth

Considering the nucleation of organic semiconductor molecules for film growth, the basic thermodynamic driving force is the difference between the chemical potential ($\Delta\mu$) of molecules in the vapor phase (μ_{v}) and the chemical potential of molecules in the crystalline phase (μ_{c}). For nucleation to occur without a heterogeneous substrate to catalyze

crystal formation, the vapor phase must be supersaturated, i.e.: $\mu_{\mathrm{v}} > \mu_{\mathrm{c}}$.
The nucleation process is a competition between the thermodynamic driving force and the energy costs associated with the creation of new surfaces. The thermodynamic driving force is also influenced by volume effects and the enthalpic free energy lowering by beneficial intermolecular interactions. The free energy required to form a finite-sized crystal formed of j molecules can be expressed as:

$$\Delta G(j) = -j\Delta\mu + j^{2/3}\sum_{i}\gamma_{\mathrm{i}}A_{\mathrm{i}} \tag{2.11}$$

where γ_{i} is the surface energy of a surface with area $\mathrm{A_i}$ and $\Delta\mu = \Delta\mu_{\mathrm{c}} - \Delta\mu_{\mathrm{v}}$.
Since organic molecules are usually highly anisotropic, there are many different possible surfaces with different surface energies, and the above equation represents only the macroscopic relationship between the total free energy, crystal size and surface energies. Eqn.2.11 highlights the importance of the surface and the relevant interfacial energies which lead to differences in the free energy and thereby the different growth modes of the film. The barrier to nucleation $\Delta\mathrm{G}^*$ can be obtained by:

$$\left(\frac{\partial\Delta G(j)}{\partial j}\right)_{\mathrm{T,P}} = 0$$

where $\Delta\mathrm{G}^*$ is $\Delta\mathrm{G(j)} = \Delta\mathrm{G(i)}$ and i is the critical cluster size, i.e. the size of the cluster at which the addition of one more molecule stabilizes the cluster. Therefore, $\Delta\mathrm{G}^*$ is the barrier to nucleation at which the surface energy effects are the greatest. At this point, the addition of more molecules to the cluster will increase the intermolecular enthalpic interactions and lower the total energy. In other words, the intermolecular effects will dominate the surface effects to create a stable island. The importance of ΔG^* can be expressed by considering its strong influence on the density of stable nuclei which can be expected to survive long enough to contribute to crystal growth by the following association:

$$N^* = n_{\mathrm{s}}exp\left(\frac{-\Delta G^*}{k_{\mathrm{B}}T_{\mathrm{s}}}\right) \tag{2.12}$$

Even though thermodynamic models are valid for treating nucleation and growth mechanisms, several kinetic and scaling models adopted from classic nucleation theories developed for inorganic materials have also been applied to model the growth of organic semiconductors like pentacene.

2.5.2 Kinetics of nucleation and growth

Thermodynamic equilibrium is defined by the condition of detailed balance, in which all participating processes are proceeding at equal rates in opposite directions. In such a condition, there is no net growth. Although the system can be described by unchanging macroscopic variables such as the pressure or temperature, microscopically the system is continuously changing via processes which balance each other out.

Atomistic processes

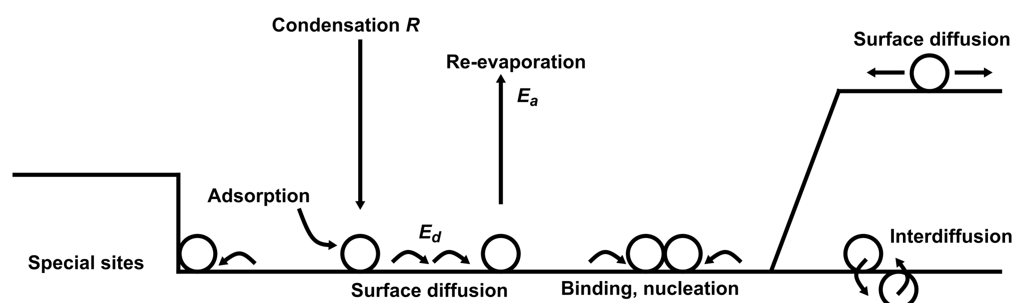


Figure 2.13: The various atomistic processes contributing to the adsorption and crystal growth process during vapor deposition

Fig.2.13 shows the different atomistic processes contributing to the adsorption and crystal growth processes during vapor deposition. Atoms arrive at the surface with a rate of arrival R, as determined by the evaporation source and the experimental conditions. Considering a substrate with N_0 sites per unit area, and a number density of $n_1(t)$ single atoms arriving on the surface, the single-atom concentration is n_1/N_0. Upon arrival at the surface, the single atoms diffuse over the surface until they are captured by one of the several processes, such as re-evaporation, nucleation of clusters, capture by existing clusters, dissolution into the substrate or capture at special sites which include defects. The probability of each of these processes depends on the single-atom concentration and the coverage, and in cases of thermally-activated processes, on the activation energies (e.g. re-evaporation energy E_a, diffusion energy E_d). The formation of clusters of critical size and their growth thereafter to larger clusters depends on these individual processes. Considering the different atomistic processes, it is clear that the two independent experimental variables, viz. the rate of condensation R and the temperature T are extremely important towards influencing the nucleation and growth of atomic clusters on the surface. In addition, the presence of defects on the substrate surface in forms of ledges,

kinks, dislocation and point defects is also very significant and these defects have a strong influence on the binding of single atoms and formation of small clusters on the surface.

Crystal growth is a non-equilibrium kinetic process, and the kinetics of the growth process must be considered. The various reaction processes indicated above and their relative influence determine the final macroscopic state kinetically, although it may not be the most stable state. The rate of nucleation is therefore dependent on various factors such as the rate of deposition, the substrate temperature, surface properties of the substrate, intermolecular interactions, and molecule-surface interactions, which will be explored in detail throughout this thesis.

The rate of nucleation is the number of nuclei of a critical size forming on a substrate per unit area and per unit time and depends on the rate at which the adsorbed atoms attach to it, given by the expression:

$$N = N^{*} A^{*} \omega \tag{2.13}$$

where N^{*} is the equilibrium concentration of stable nuclei, A^{*} is the critical nucleus area and ω is the rate of atom impingement onto critical nuclei.

Considering the individual dependencies of ω on the re-evaporation energy E_{a} and the diffusion energy E_{d}, as well as the dependency of N^{*} on $\Delta \mathrm{G}^{*}$ according to Eqn.2.12 and the critical area, the nucleation rate can be expressed as:

$$N = 2\pi r^{*} a_{0} sin\theta \frac{P N_{\mathrm{A}}}{(2\pi M R T)^{1/2}} n_{\mathrm{s}} exp\Big(\frac{E_{\mathrm{a}} - E_{\mathrm{d}} - \Delta G^{*}}{k_{\mathrm{B}} T_{\mathrm{s}}}\Big) \tag{2.14}$$

where r^{*} is the critical nucleus radius, a_{0} is the lattice parameter, θ is the contact angle, n_{s} is the total nucleation site density, E_{a} is the re-evaporation energy barrier, and E_{d} is the surface diffusion energy.

Evidently, three important energetic barriers directly influence the nucleation density. A larger degree of surface mobility and thereby a greater chance for molecules to encounter each other and form a stable cluster are achieved by a smaller barrier for diffusion. In general, the surface chemistry and roughness determine the lateral corrugation in the molecule-substrate interaction potential which influences the barrier to diffusion. A

larger barrier for desorption or re-evaporation means that the molecule is more tightly bound to the surface and has more time to form n-mers with other molecules to form a stable cluster. Each of these molecular processes is also a function of the molecule-substrate interaction strength, and the implications of these factors will be considered in section 2.5.4.

2.5.3 Growth modes

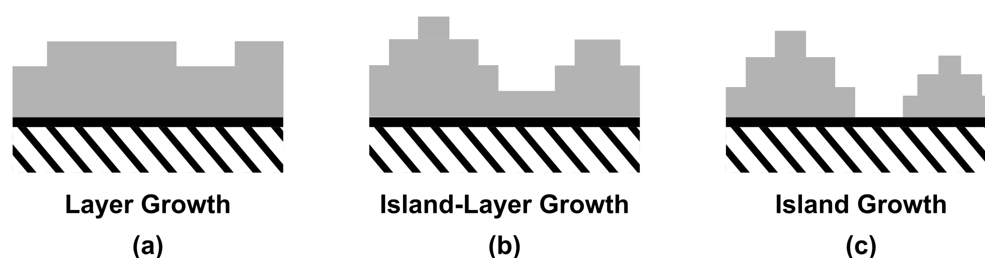


Figure 2.14: The three most common growth modes during thin-film growth: (a) 2D layer-by-layer (Frank-van der Merwe) growth, (b) 2D monolayer followed by 3D growth (Stranski–Krastanow) and (c) 3D island growth (Volmer-Weber)

As previously mentioned, the growth mode of the organic semiconductor films must be conducive to charge transport by increasing the degree of π orbital overlap between neighboring molecules. The growth mode of films can be, in general, differentiated into 2D-like layer-by-layer growth, 3D island growth or a combination of island-layer growth, as shown in Fig.2.14. Layer growth (also called Frank-van der Merwe type of growth) occurs when the molecules are more strongly bound to the substrate than to each other and the first molecules to condense from the vapor phase form a complete monolayer on the surface. During island growth (also known as Volmer-Weber type of growth), small clusters are nucleated directly on the substrate surface and these clusters grow into islands of the condensed phase. This growth mode occurs when the deposited molecules are more strongly bound to each other than to the substrate. For organic transistors with large charge-carrier mobilities, a 2D-layer growth mode is preferred for organic semiconductor films since a 3D-island growth mode can give rise to voids and a larger number of grain boundaries in the film. Usually, organic semiconductor molecules form films with an intermediate growth mode, the island-layer (or Stranski-Krastanov) type of growth, in which layer growth after the formation of the first monolayer (or a few monolayers) is unfavorable. Layer growth is maintained if the binding of each subsequent layer to the bulk of the crystal decreases monotonically.

A mismatch in lattice parameters or certain molecular orientations may result in a high free energy at the intermediate layer interface and disturb this monotonic decrease in binding energy in consecutive layers, causing subsequently deposited molecules to form islands on the top of the intermediate layer. The growth mode is determined by competing interlayer interaction energies and molecule-substrate energies. The stronger the molecule-substrate interactions, the greater the tendency for 2D growth. It must be noted that each type of semiconductor and the type of surface have unique interactions, and any generalizations made about the hydrophobicity, surface energy or the surface chemistry may not be entirely accurate.

2.5.4 Factors influencing growth and morphology of organic films

Based on the theoretical considerations for the optimum growth of organic semiconductor films, this section details the experimental factors and their influence during fabrication.

- **Rate of deposition**
  The rate of deposition is an important parameter to control during thermal sublimation in vacuum. Generally, an increase in the deposition rate increases the rate of nucleation in the film growth process, leading to smaller crystallites, smaller grains and thereby a larger density of grain boundaries in the polycrystalline film. A drastic increase in the rate of deposition greatly increases the tendency for supersaturation, and thermodynamic considerations for the nucleation in films may no longer be applicable. At extremely high deposition rates, film growth is completely kinetically dominated and the films fabricated may become completely amorphous with a glass-like nature. Therefore, in general, a relatively small deposition rate is preferred for organic semiconductor film growth to reduce the nucleation density and increase the overall grain size.

- **Substrate temperature**
  The overall barrier to heterogeneous nucleation decreases with an increase in the substrate temperature. Although the free energy G is only weakly dependent on the temperature, all individual energy barriers (e.g. for desorption, diffusion) follow an Arrhenius temperature dependence. An increase in the substrate temperature motivates surface mobility and molecules to diffuse on the substrate to find

low-energy sites and promotes the formation of larger, circular grains. However, when exceeded beyond an optimum limit, an increased substrate temperature can lead to increased desorption or re-evaporation of molecules from the surface. In an extreme case, when the substrate temperature exceeds the sublimation temperature, nucleation is thermodynamically impossible. Therefore, the ideal substrate temperature is balanced between the temperatures required for increasing surface diffusion and for decreasing desorption. Within this optimum range for the substrate temperature, in which the sticking coefficient for molecules is sufficiently high for nucleation, an increase in the substrate temperature decreases the chemical potential difference ($\Delta\mu = \mu_{\mathrm{c}} - \mu_{\mathrm{v}}$), and an overall tendency for the preferred 2D-layer growth mode is higher. Often new organic semiconductor molecules synthesized require the investigation of an optimum substrate temperature on different substrates. An example of such an investigation can be seen in Appendix C.

- **Substrate surface properties**
  The effect of surface properties of the gate dielectric in the organic transistor is of great importance for the fabrication of high quality semiconductor films, particularly, the effect of the surface energy and the surface roughness of the gate dielectric surface. The surface energy characterizes the wettability of the surface which has a possible influence on the probability and size of the formation of nucleating clusters from the deposited molecules. The surface roughness of the dielectric can be instrumental in suitably increasing the coordination between the deposited molecules and the surface. The rough areas on the surface decrease the barrier for nucleation and increase the barrier to desorption. However, on extremely rough surfaces, the grain quality of the films is negatively affected, leading to small, mis-oriented grains and poor device performances. The surface energy and surface roughness are considered in detail, particularly in Chapter 6 to establish a relationship between the interfacial properties at the dielectric-semiconductor interface and the electrical properties of the organic transistors.

2.5.5 Thickness of organic semiconductor films

The thickness of the organic semiconductor film has potentially a strong influence on their growth and morphology and on the device performance. Depending on the device

configuration and the relative position of the contacts to the organic semiconductor, the thickness of the semiconductor layer influences the injection and extraction of charge carriers. A majority of the charge transport in organic transistors takes place in the first one or two monolayers of the organic semiconductor layer, close to the dielectric-semiconductor interface. Typically, organic semiconductor films are deposited with a thickness corresponding to multiple (10-20) monolayers to stabilize the initial charge-transporting monolayers. The impact of the film thickness on its stability and morphology is discussed in detail in Chapter 7.

2.6 Thin-film characterization techniques

Apart from the electrical characterization of organic transistors, the semiconductor and dielectric layers were also characterized for various surface and film properties. This section briefly describes the basic working principle of the various characterization techniques used in this thesis.

2.6.1 Contact angle goniometry

The surface energy was measured by static contact angle goniometry. In this method, a liquid drop is placed on the surface of interest, and the static contact angle is measured using an optical microscope. By measuring the wettability of two different liquids, a polar and a non-polar liquid, the surface energy is calculated using the Owens-Wendt method [99].

2.6.2 Atomic force microscopy

Atomic force microscopy (AFM) is a type of a scanning probe microscopy technique used for topographic imaging with a resolution of the order of a fraction of a nanometer. A schematic of the basic operational setup can be seen in Fig.2.15. A cantilever beam with a sharp tip oscillates at a resonance frequency, and a laser beam is reflected off the top of the cantilever to a split photodetector. The sharp tip probes the sample surface and the forces between them change the amplitude of oscillation, with the deflection in the cantilever corresponding to the topography of the surface. In this work, AFM has

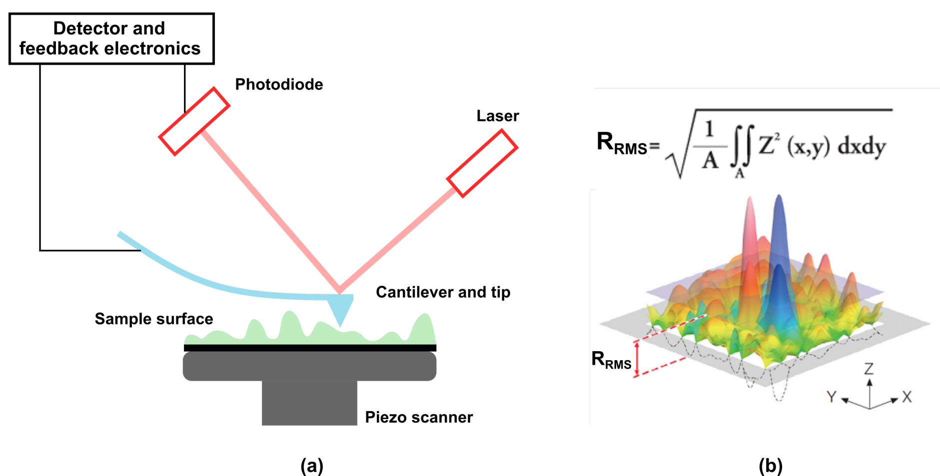


Figure 2.15: Schematic representation of (a) an Atomic Force Microscopy (AFM) measurement and (b) the R_{RMS} surface roughness parameter, adopted from www.olympus-ims.com

been used to collect morphology information of organic semiconductor films as well as observe any changes in the morphology with time by using repeated scans of the same area. In addition, surface roughness information from the dielectric and semiconductor surfaces has been collected using AFM.

R_{RMS} surface roughness

The parameter used to characterize the roughness of the surface from the topological information collected by the AFM is the Root-Mean-Square Roughness (R_{RMS}), as shown in Fig.2.15(b). The root-mean-square surface roughness is calculated as follows. All topographical features collected by the AFM are converted to profiles by considering the absolute values of all amplitudes or the profile height from the mean plane (**Z**). These profile heights are squared, which accentuates all prominent features on the sample surface. The squared values are integrated over the entire surface and averaged to obtain a mean value. Finally, a square root value is obtained to compensate for the initial squaring of profile height values, which determines the R_{RMS} surface roughness. By selecting R_{RMS} as the parameter of choice to characterize the surface roughness of films, any contribution from features and surface elements contributing to rough surfaces is appropriately measured.

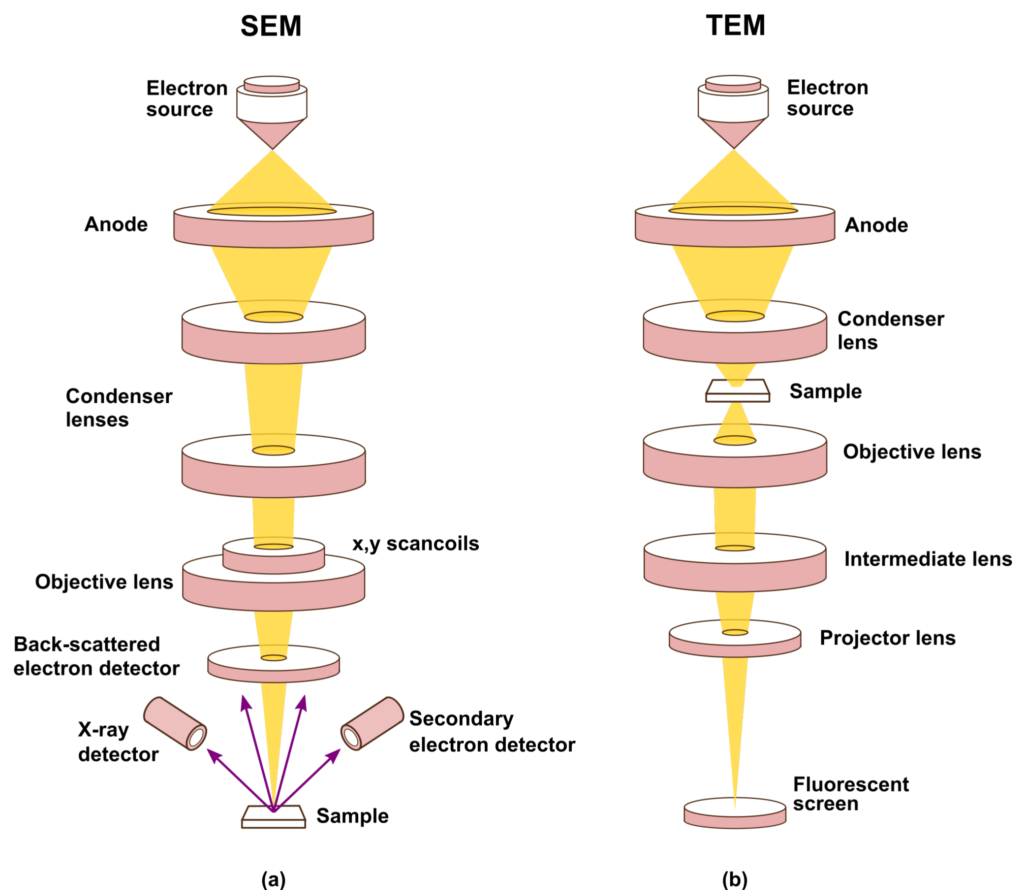


Figure 2.16: Schematic representations of (a) Scanning Electron Microscopy (SEM) and (b) Transmission Electron Microscopy (TEM) techniques

2.6.3 Scanning Electron Microscopy

Scanning Electron Microscopy (SEM) utilizes a fine beam of focused electrons to scan a sample surface, and the interaction between the electrons and the sample surface is recorded to create a highly magnified image (with a resolution of 1-20 nm). A basic schematic of the inside of an SEM with its different components can be seen in Fig.2.16(a). The electron source emits a beam of high-energy electrons which is focused using electromagnetic lenses and is incident on the sample surface. Upon interaction with the sample surface, secondary electrons, backscattered electrons and X-rays are emitted, collected by various detectors and can be used to access information about the surface topography and elemental composition. The contrast in SEM images is created due to a difference in atomic weights of different elements on the sample surface, creating a stark contrast between the organic semiconductor and the dielectric films. SEM images have been used to analyze the growth of organic semiconductors on dielectric surfaces in this thesis.

2.6.4 Transmission Electron Microscopy

Transmission Electron Microscopy (TEM) uses an electron beam, as the name suggests, transmitted through an atomically-thin sample to create an image of the internal structure to collect information about the morphology, composition and crystal structure. A basic schematic of the functioning principle of a TEM with its different components can be seen in Fig.2.16(b). Samples investigated in the TEM must be extremely thin ($\leq$ 150 nm) to allow electrons to pass through them to be collected at a detector and analyzed to create a 2D image, often with a resolution below 1 nm. In this thesis, TEM has been used to measure the thickness of ultrathin gate oxide films.

2.6.5 X-ray Diffraction

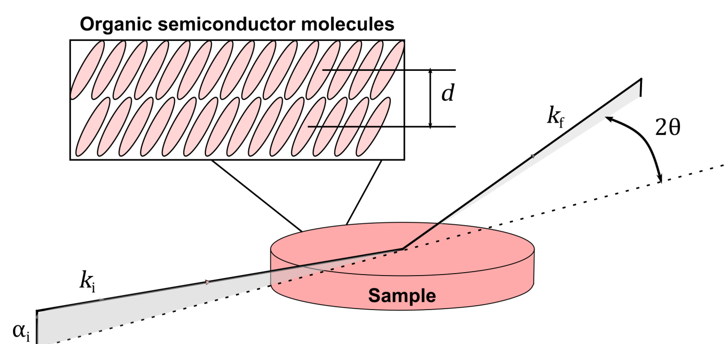


Figure 2.17: Schematic representation of a grazing incidence X-ray diffraction measurement with an incident X-ray beam (k_i) at an incident angle α_i, and the diffracted beam (k_f) at a diffraction angle of 2θ, used to measure the interlayer spacing d of the organic semiconductor layer

Grazing incidence X-ray diffraction is a surface sensitive technique used to analyze the crystallinity of the sample. An X-ray beam probes the sample at an extremely small angle of incidence with respect to the sample plane to limit the penetration of the beam to the surface layers. The angles and intensities of the diffracted X-ray beams give information about the position of the molecules and thereby the crystalline nature of the layer. In this thesis, grazing incidence X-ray diffraction is used to analyze the d-spacing between the semiconductor layers, the orientation of the molecules with respect to the surface and the quality of the layer-by-layer packing in organic semiconductor layers.

Chapter 3

Hybrid gate dielectrics in organic thin-film transistors

A majority of the efforts in the development of organic thin-film transistors (TFTs) have been focused on improving the electrical performance in the conducting channel of the transistor. One of the ways this was achieved was by synthesizing organic semiconductors of higher quality, i.e. with higher intrinsic mobilities and better air stability [100–104]. Another important area of focus was the development of deposition methods of organic-semiconductor films with a sufficiently low density of structural and electronic defects [105, 106]. However, in addition to the semiconductor, the gate dielectric also plays a vital role in the organic transistor, with a primary function of isolating the organic semiconductor from the gate electrode, and has several requirements for desirable organic TFT operation.

As detailed in Chapter 2, the gate dielectric is polarized upon applying a voltage across it, and the internal charge separation and electric field buildup lead to the accumulation of charge carriers in the organic semiconductor layer. The principle function of the gate dielectric is thus, to effectively couple the charge applied to the gate electrode to form the conduction channel in the transistor. The thickness and the relative permittivity of the gate-dielectric layer determine the gate-dielectric capacitance (given by Eqn.2.9), which in turn determines the operating voltage of the transistor. In order to enable several portable and lightweight device applications, it is necessary to operate organic TFTs at a relatively low voltage, which can be achieved by a high gate-dielectric capacitance. The primary ways to obtain a high gate-dielectric capacitance are to either reduce

the thickness of the gate-dielectric film or to use gate-dielectric materials with a large relative permittivity. Several potential device applications based on organic transistors are designed to be powered by small batteries or solar cells, which require an overall low power consumption along with low-voltage operation. It is important that the gate dielectric is able to withstand the electric field generated on applying the gate-source voltage, without incurring a significant leakage current density to maintain an overall low power consumption.

Considering organic TFTs in the inverted-device architecture (as shown in Fig.2.4), the gate dielectric provides a surface on which the organic semiconductor is deposited. The conducting channel of the transistor is confined to the first few monolayers of the organic semiconductor layer, located in close proximity to the dielectric-semiconductor interface [83, 84, 107]. Surface properties of the gate dielectric are a potential factor influencing the growth and morphology of the organic semiconductor layer and thereby the charge-transport characteristics of the organic TFT. As an example, the surface roughness of the gate dielectric can be correlated with the undesirable formation of nanoscopic interfacial grain boundaries and sites for charge scattering [108]. As another example, a gate-dielectric surface with an increased surface energy may facilitate semiconductor deposition by certain solution-processed techniques by providing a favorable hydrophilic surface for that particular technique [109]. On the other hand, chemical functionalities contributing to high surface energy may act as charge-trapping sites, negatively impacting the charge transport in the organic TFT [110]. The surface properties of the gate dielectric are thus a crucial aspect in correlating the material properties of the organic semiconductor to the electrical properties of the organic transistor, and will be a key consideration in this thesis to analyze different aspects of TFT performance based on their material and design configuration.

The gate dielectric also has an influence, either directly or indirectly, on several transistor operation characteristics including but not limited to the charge-carrier mobility, the threshold voltage and the threshold-voltage shift. For example, molecules with fluorine or amino groups are used in self-assembled monolayers in the gate dielectric to shift the threshold voltage to more positive or more negative values respectively [111]. The design and choice of the gate dielectric thus becomes crucial towards operation of the transistor and circuit design aimed for specific applications.

The long-term stability of organic TFTs remains an ongoing challenge and a key concern towards the development and integration of organic TFTs in commercial electronic

applications. Similar to other components in the organic TFT, the gate dielectric must also be compatible with the entire fabrication process and be stable against electrical or environmental degradation. Hence, along with the electrical properties of the dielectric, the mechanical and chemical properties also play a role in the choice of the gate dielectric for organic TFTs.

The most popular and common choice for the gate dielectric in organic TFTs is thermally grown silicon dioxide (SiO_2) on silicon wafer substrates. This choice is particularly useful for testing new organic semiconductors because of the uniformity of the gate dielectric and the simplicity of the TFT-fabrication process in which no additional steps are required to deposit and pattern the gate dielectric. However, the fact that high-quality silicon dioxide can be produced only on single-crystalline silicon wafers, unsuitable for flexible TFT applications, as well as the low dielectric constant of SiO_2 ($\sim$3.9) and the inability to pattern the dielectric prevent the fabrication of high-performance, advanced devices and circuits. Apart from thermally grown SiO_2, other gate insulators employed in organic TFTs can be broadly classified into the following categories based on their material classes: inorganic metal oxides, insulating polymers and electrolyte insulators. Metal oxides such as Al_2O_3 [112,113], TiO_2 [114,115], ZrO_2 [116,117], HfO_2 [118–120], Ta_2O_5 [121] and even perovskites such as $Ba_xSr_yTiO_3$ [122, 123] have been widely investigated. Deposition techniques such as sputtering, atomic layer deposition, pulsed laser deposition, anodization, electron-beam evaporation and even several solution-processing techniques such as spin/spray/bar-coating are popularly employed, with the method of deposition chosen to suit the other materials and techniques used in the TFT fabrication process. Vapor deposition techniques are extremely successful in producing high-quality, defect-free films, while solution-processing techniques offer advantages such as large-area fabrication and low processing temperatures suitable for alternative substrates. Polymers investigated most frequently as gate dielectrics for organic TFTs include poly(vinyl alcohol) [124], polyimide, poly(vinylphenol) [125, 126], poly(methyl methacrylate) [127, 128], photoresists, etc. There are two main approaches for fabricating polymer dielectrics, either by depositing the polymer solution followed by evaporating the solvent, or formation of the polymer from the monomer directly on the gate electrode. Polymer dielectrics are most commonly deposited by solution-processing techniques such as spin or spray coating, inkjet printing, etc. Although ideal for a lot of TFT configurations and applications, polymer dielectrics often suffer from a lack of

thermal and chemical stability for patterning the dielectric and therefore hinder the possibility of fabricating complex devices and circuits. Polymer dielectrics are most suited for applications in which a solution-processing approach is adopted and benefit from advantages like roll-to-roll and scalable fabrication.

An emerging class of gate dielectrics for organic TFTs is electrolyte insulators, particularly developed towards bioelectronics applications [129, 130]. The primary types of electrolytes employed as gate dielectrics include polymer electrolytes, polyelectrolytes, ionic liquids and ion-gels [131–133]. Electrolyte insulators function by the formation of electric double layers (EDLs), i.e. the displacement of oppositely charged ions at the electrolyte/electrode interfaces in response to an electric field. Since the capacitance of the electrolyte layer depends on the formation of the EDLs and not the physical thickness of the electrolyte layer, very large capacitances (1-10 μF/cm^2) can be achieved. Consequently, a large charge-carrier density can be generated at the interface, which is the primary motivation [134]. However, it must be noted that the capacitance of the electrolyte insulator is frequency-dependent and often charge-carrier mobilities reported are largely overestimated [135]. Besides, thick films of the electrolytes (1-10 μm) are required to prevent undesired leakage currents, which remains a major issue.

Considering the advantages of each of the above mentioned dielectric material classes, a unique approach is to employ "hybrid dielectrics", which comprise of more than one type of dielectric material. For example, blends of low-k polymers with high-k fillers such as perovskites [barium titanate (BT), barium zirconate (BZ), aluminum titanate (AT), barium strontium titanate (BST)] and metal oxides [ZrO_2, HfO_2, Ta_2O_5, Y_2O_3, TiO_2] are an effective method to increase the average relative permittivity of the composite [136, 137].

This thesis explores the use of hybrid gate dielectrics with two components, i.e. an ultrathin metal-oxide film in combination with an organic self-assembled monolayer. An important aspect regarding hybrid dielectrics is the concept of self-assembled monolayers (SAMs), which will be further elaborated on in Section 3.1. The materials, fabrication techniques and the choices thereof have been detailed in Section 3.2, along with the multi-fold advantages and benefits of this approach.

3.1 Self-assembled monolayers

George Whitesides and Bartosz Grzybowski defined self-assembly as "the autonomous organization of components into patterns and structures without human intervention" [138]. A self-assembled monolayer (SAM) is a molecular structure formed spontaneously on the surface by adsorption and organization into more or less ordered domains, with its thickness chemically limited to one monolayer. Molecules which are used to form SAMs are usually composed of three main components (as shown in Fig.3.1): a head group, which binds to the underlying surface, a backbone made up of either an aliphatic chain or aromatic oligomers and responsible for molecular ordering, and a terminal or tail group which determines the topography and surface properties of the SAM. The process of molecules assembling into a SAM proceeds usually through the adsorption of the head group on the substrate, followed by the slow organization of backbone and tail groups. The individual components of the molecules have a strong influence on determining the properties of the SAM. For example, a strong chemisorption of the head group brings about a high stability of the SAM, and the interactions between the aliphatic chain backbone determine the molecular ordering and packing density of the SAM.

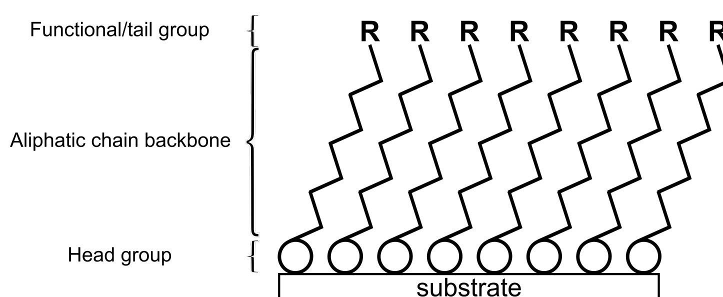


Figure 3.1: Schematic representation of molecules assembling into self-assembled monolayers (SAMs) with the different components of the molecules contributing to self assembly

In this section, we will focus on SAMs used for gate dielectrics in organic TFTs. The most popular molecules used to form SAMs and particularly the molecules discussed in detail in this thesis are shown in Fig.3.2, denoted by abbreviations either commonly used in literature or as abbreviated in this thesis (complete list in the Abbreviations section).

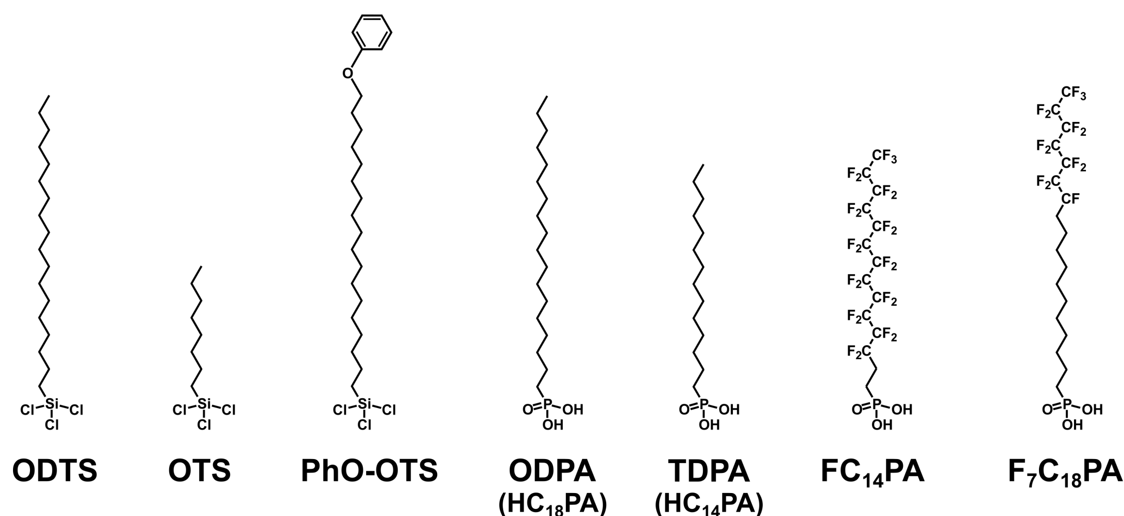


Figure 3.2: Commonly used molecules for self-assembled monolayers (SAMs) in gate dielectrics in organic TFTs

The potential application of SAMs for gate dielectrics in organic TFTs was first developed by the Vuillaume group by fabricating metal-insulator-semiconductor (MIS) structures with an octadecyltrichlorosilane (ODTS) SAM assembled on the native SiO_2 surface as well as alkyltrichlorosilanes with three different chain lengths (12, 16 and 18 carbon atoms) as the insulator [139, 140]. It was demonstrated that the leakage current density (10^{-8}-10^{-11} A/cm^2) through the MIS structure was greatly reduced, by about 4-5 orders of magnitude in comparison to an oxide or nitride insulator of similar thickness. The beneficial effect of the SAM was ascribed to an increase in the energy barrier and the packing density of the SAM. This approach was further extended to fabricate thin-film transistors with alkyltrichlorosilane SAMs with different functional terminal groups assembled on native SiO_2 as the gate insulator [141, 142], exhibiting very low leakage current densities (10^{-5}-10^{-8} A/cm^2). This seminal work established the advantage of using SAMs to achieve low operating voltages in organic TFTs by reducing the thickness of the gate dielectric without incurring significant leakage current losses. This encouraged the wide investigation of alkyltrichlorosilane SAMs for gate dielectrics towards fabrication of low-voltage organic TFTs, exploring the different aspects of the SAM and its impact on the performance of the organic TFT. Halik et. al investigated a series of oligothiophene-organic semiconductor transistors with an ODTS dielectric by varying the number of thiophene units and alkyl side-chain substitutions on the semiconductor [143]. A phenoxy-terminated SAM, PhO-ODTS was used as the gate dielectric to fabricate pentacene TFTs, with the strong $\pi-\pi$ interactions of the terminal phenyl groups preventing the penetration of the pentacene molecules in the

SAM and defining a better semiconductor-dielectric interface [144]. The use of SAMs with solution-processed organic semiconductors was also demonstrated by Park et. al by fabricating a regioregular poly(3-hexylthiophene) (P3HT) organic TFT with a docosyltrichlorosilane SAM as the gate dielectric demonstrating a significant reduction of the operating voltage and power consumption [145].

Apart from alkyltrichlorosilane SAMs, another major category of molecules for SAMs as gate dielectrics are phosphonic acids, which were introduced by Klauk et. al by fabricating both p-channel and n-channel organic TFTs using the organic semiconductors pentacene and hexadecafluorocopperphthalocyanine ($F_{16}CuPc$), as well as low-power complementary circuits [35]. The gate dielectric in use was an octadecylphosphonic acid (ODPA) SAM with a thickness of 2.1 nm in combination with a plasma-grown ultrathin aluminum oxide (AlO_x), which was determined to be 3.6 nm thick. Despite the overall small thickness of the dielectric, the leakage current density was reduced by 3 orders of magnitude in comparison to a standalone oxide dielectric without the SAM. In addition, the ODPA SAM demonstrated a lower leakage current density compared to the ODTS SAM which was assigned to its better packing density, as measured by X-ray photoelectron spectroscopy measurements.

Molecules are assembled into SAMs on the surface of interest most commonly by immersion of the substrate into a solution of the molecules with a suitable solvent. Recently, formation of SAMs by vacuum-evaporation techniques has also been reported [146,147]. The adsorption of alkylphosphonic acids on aluminum oxide surfaces proceeds through the interaction of the phosphonic acid head group with the hydroxyl groups (-OH) present on the aluminum oxide surface. A mono-, bi- or tri-dentate adsorption mechanism anchors the phosphonic acid group via one, two or three P-O-Al bonds via a stepwise condensation reaction as shown in Fig.3.3 [148–150].

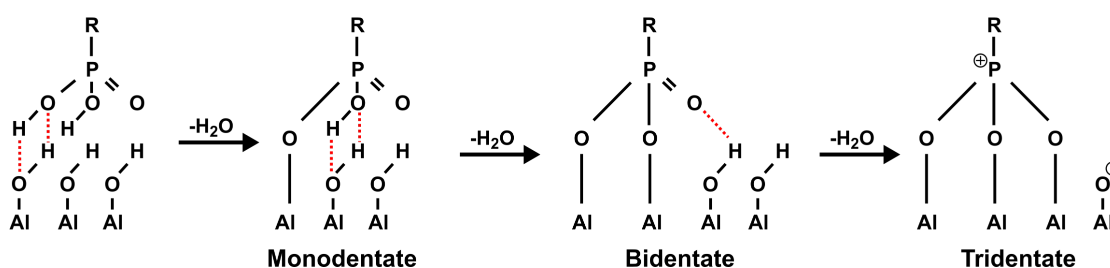


Figure 3.3: Assembly of phosphonic acids on aluminum oxide via mono, bi or tridentate bonding mechanisms through condensation reactions

Several factors influence the adsorption of the phosphonic acid molecules and formation

of the SAM which include the presence of hydroxyl groups, surface roughness of the substrate, temperature of the substrate, the chain length and chain type of the molecule, the type, concentration and incubation time of the solvent and suitable preparation of the substrate surface. Of the various influencing factors, the influence of the backbone chain length of alkyl- and fluoroalkyl phosphonic acid molecules will be discussed in detail in Chapter 6.

SAMs employed as gate dielectrics influence the functionality and performance of organic TFTs in several ways. Primarily, as described above, SAMs enable low-voltage operation of organic TFTs by reducing the gate-dielectric thickness while maintaining a significantly low leakage current, which would otherwise require oxide dielectrics of a large thickness. In organic TFTs with hybrid gate dielectrics, SAMs introduce a buffer layer between the oxide and the organic semiconductor, thereby suppressing the formation of Fröhlich polarons and charge trapping at the interface [151]. This phenomenon will be demonstrated and discussed in detail in Chapter 4. A major contribution of SAMs lies in modifying the surface reactivity, preventing water adsorption, passivating the surface from undesired reactions and thereby defining the surface energy of the dielectric. This has been instrumental in improving the bias-stress stability of organic TFTs [152, 153]. A predominant influence of the SAM in modification of the dielectric surface properties is linked with the deposition of the organic semiconductor on the top of the SAM in bottom-gate TFT architectures. The choice and quality of the SAM has potentially a strong impact on the nucleation, growth and morphology of the organic semiconductor layer, and thereby the charge-transport properties of the organic TFT. This will be further elaborated in Chapter 6. A number of organic-TFT characteristics can be suitably tailored by customizing the type of the SAM. For example, a well-ordered and densely packed SAM promotes an optimum organic-semiconductor morphology and a large charge-carrier mobility [154]. By nature of their dipole character and suitable terminal groups, SAMs can be instrumental in altering the threshold voltage of organic TFTs significantly and purposefully, according to operation requirements [155, 156]. An example of this phenomenon will be discussed in detail in Chapter 6 with fluorine-substituted phosphonic acid molecules used to form the SAM. Furthermore, a mixture of alkyl and fluoroalkyl phosphonic acid molecules can be used to tune the threshold voltage of organic TFTs suitably for optimum circuit design of complementary inverters [157, 158].

3.2 Hybrid gate dielectrics for low-voltage organic TFTs

High-k metal oxides were sought as an alternative to SiO_2 to overcome the constraint related to its low dielectric constant. However, most metal-oxide films, including SiO_2, have certain unfavorable properties which can have adverse effects on device performance. These properties include the presence of surface hydroxyl groups (-OH) which act as charge-carrier traps, ionic polarization between the charge carriers in the semiconductor and the metal-oxide lattice and a relatively high surface roughness. Therefore, the concept of surface modification of metal-oxide films by an additional dielectric layer was introduced as a method to counter these adverse effects. Several reports in literature refer to organic layers such as polymers or self-assembled monolayers (SAMs) employed for this purpose as *surface-modification layers* for metal-oxide gate dielectrics. Since the thickness of the polymer layers or SAMs is comparable to the oxide thickness, the combination of inorganic/organic bilayer dielectrics will be referred to as hybrid gate dielectrics in this thesis.

A wide variety of polymers were used in combination with metal oxides to form hybrid gate dielectrics to improve the performance of organic TFTs in terms of increased charge-carrier mobilities, increased on-off current ratios and decreased leakage currents. Some notable examples include PMMA/Ta_2O_5 [159], PMMA/Al_2O_3 [160], PVA/SiO_2 [161], crosslinked PVP/Ta_2O_5 [162], crosslinked PVP/TiO_2 [163], etc. A more in-depth review of polymer/metal oxide hybrid gate dielectrics can be found in [164]. Although the addition of the polymer layers improved the device performance in most cases and increased the charge-carrier mobilities by the action of the polymer (for example, by reducing the surface roughness), the polymer layers deposited required relatively large thicknesses to form a uniform, conformable layer. This resulted in large operating voltages as compared to single-layer oxide dielectrics, which was a considerable disadvantage in spite of the advantageous larger charge-carrier mobilities.

Self-assembled monolayers, by virtue of their monolayer thickness, are a suitable substitute to polymers as surface modification or the second component of hybrid gate dielectrics in addition to metal oxides. Hybrid gate dielectrics composed of a metal oxide and a self-assembled monolayer are instrumental in simultaneously achieving a low operating voltage and a low leakage current density, which is difficult to attain through the manipulation of single-material gate dielectrics. The comparison of thick metal oxide, thin metal oxide and hybrid gate dielectrics is shown schematically in Fig.3.4. In

the case of single-material gate dielectrics, such as metal oxides, a small thickness can successfully achieve a low operating voltage but might lead to large leakage currents and vice-versa, a large thickness suppresses large leakage currents but increases the operating voltage of the transistor. The advantage of the hybrid dielectric is then apparent, where a thin metal oxide layer is used in combination with the organic SAM, providing multi-fold benefits of a low operating voltage, a reduced gate-leakage current as well as the possibility of surface property modification by the SAM.

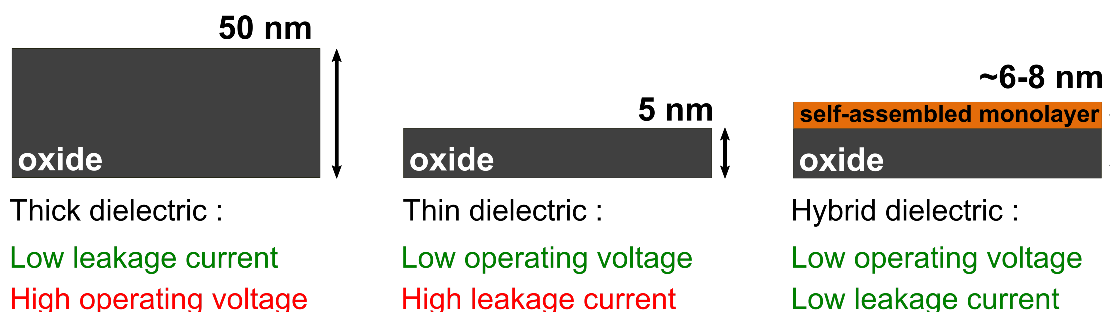


Figure 3.4: Schematic representation and comparison of thick and thin oxide dielectrics with hybrid gate dielectrics composed of a thin oxide layer and a self-assembled monolayer

As previously mentioned in Section 3.1, the two primary categories of molecules used to form SAMs for gate dielectrics in organic TFTs are silane-based molecules and phosphonic acid-based molecules. Organosilane molecules form SAMs on surfaces bearing -OH groups, e.g. silica, aluminum oxide, zinc oxide, etc. The most popular and widely studied molecules include ODTS (octadecyltrichlorosilane), OTS (octadecylsilane), OTMS (octadecyltrimethoxysilane), HMDS (hexamethyldisilazane), and a wide variety of techniques have been used to form SAMs such as dipping [165,166], immersion [167], stamp printing [168], Langmuir-Blodgett technique [169], spin-casting [170], and even vapor deposition [171,172]. Silane-based SAMs have shown a targeted improvement in organic-TFT performance by influencing the growth mode of organic semiconductors like pentacene, C_{60}, etc. and improving charge-transport properties.

Phosphonic acid SAMs assemble on a large range of inorganic oxide dielectrics by multidentate binding of strong covalent P-O-M anchoring where M is the metal atom. The most popular combination for phosphonic acid SAMs is with an AlO_x film as the metal oxide component, but phosphonic acid molecules have also been used in combination with HfO_2 films prepared by a sol-gel technique [119,120,173,174]. The underlying AlO_x film can be prepared by a variety of methods such as atomic layer deposition (ALD) [175],

anodization [176], spin coating [177, 178], UV/ozone assisted oxidation [179, 180] and plasma-assisted oxidation [37, 181–184]. An extremely detailed review can be found in [185].

As mentioned above, this thesis investigates an ultrathin, hybrid gate dielectric composed of an inorganic metal oxide and an organic self-assembled monolayer (SAM). This approach utilizes the benefits of both components to provide a unique advantage for low-voltage organic TFTs. For the metal oxide component, an aluminum oxide (AlO_x) film is fabricated by oxidizing the surface of the underlying aluminum gate electrode in a radio-frequency generated oxygen plasma. The SAM component constitutes phosphonic acid molecules with an aliphatic chain, either an unsubstituted alkyl chain or a substituted fluoroalkyl chain, assembled from solution.

3.3 Importance of individual components of a hybrid gate dielectric

After reviewing the different types of gate dielectrics from literature, this section shows the original work in this thesis of fabricating organic TFTs with different gate dielectric configurations. The aim is to highlight the importance and action of each of the two components in a hybrid gate dielectric, i.e. the metal oxide and the self-assembled monolayer, and outline their contributions to the overall benefit and application of hybrid gate dielectrics in organic TFTs.

Fig.3.5 and Fig.3.6 show transfer characteristics and gate currents of TFTs employing the following two small-molecule organic semiconductors:

- dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT)
- 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT)

Three different gate-dielectric configurations were selected for the organic TFTs with each of the organic semiconductors-

- **(a) SAM dielectric**: the gate dielectric was formed only using the solution-processed SAM directly on the native oxide of the aluminum gate electrode, i.e. without exposing the aluminum gate electrode to an oxygen plasma.

- **(b) Oxide dielectric**: the gate dielectric was formed by exposing the aluminum gate electrode to an oxygen plasma, but without the solution-processed SAM.

- **(c) Hybrid gate dielectric**: the gate dielectric was formed by both, the oxygen plasma treatment to form the aluminum oxide film as well as the solution-processed SAM.

An alkyl phosphonic acid molecule with 14 carbon atoms, n-tetradecylphosphonic acid ($HC_{14}PA$), was chosen to form the SAM for the DNTT TFTs and a fluoroalkyl phosphonic acid molecule with 10 carbon atoms, 1H,1H,2H,2H-perfluorodecylphosphonic acid ($FC_{10}PA$), was chosen to form the SAM for the DPh-BTBT TFTs. The choice of the molecule for the SAMs for the respective organic semiconductor TFTs is further explained in Chapter 6 and Appendix D. By fabricating transistors with individual components of the gate dielectric and comparing them with the hybrid gate dielectric-TFTs, the importance and significance of each of these is established.

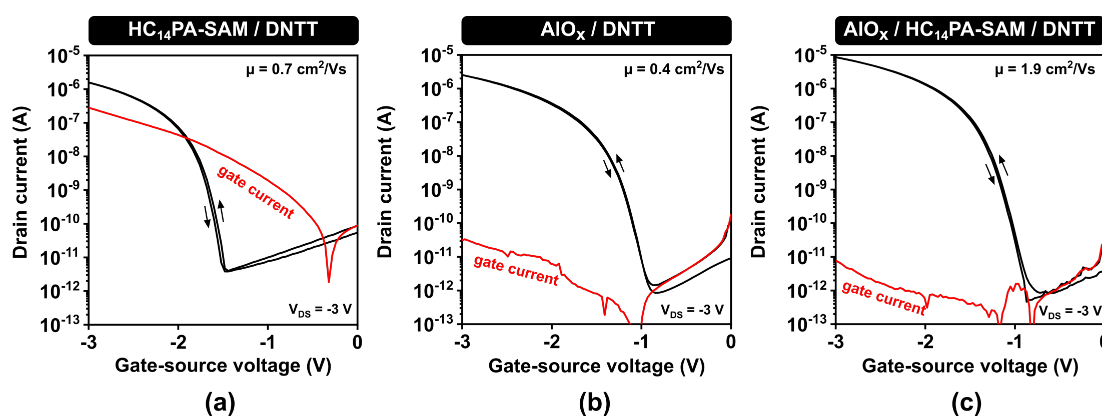


Figure 3.5: Transfer characteristics and gate currents of DNTT TFTs fabricated with either (a) a SAM dielectric (without oxygen plasma), (b) a bare-AlO_x dielectric (without SAM) and (c) a hybrid AlO_x/SAM gate dielectric. The molecule chosen to form the SAM is $HC_{14}PA$

3.3.1 The oxide component of the hybrid gate dielectric

Considering the DNTT TFTs in Fig.3.5, the importance of the oxygen-plasma process for the formation of the AlO_x film as well as towards the overall functioning of the gate dielectric is evident. It can be observed in Fig.3.5(a) that the gate leakage current is several orders of magnitude higher when the oxygen-plasma process was skipped. In the absence of the oxygen-plasma process, the native AlO_x film serves as the gate oxide and

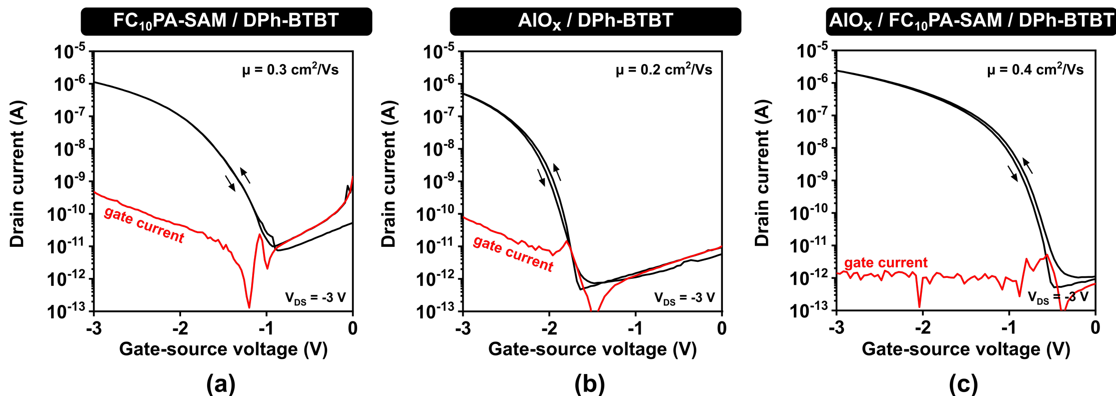


Figure 3.6: Transfer characteristics and gate currents of DPh-BTBT TFTs fabricated with either (a) a SAM dielectric (without oxygen plasma), (b) a bare-AlO_x dielectric (without SAM) and (c) a hybrid AlO_x/SAM gate dielectric. The molecule chosen to form the SAM is $FC_{10}PA$

density of surface hydroxyl groups (-OH) is low. In such a case, the adsorption of the phosphonic acid molecules is also hindered and the overall thickness of the gate dielectric is extremely small, essentially limited to that of the native AlO_x film. The small thickness and poor quality of the gate dielectric in this case explains the large leakage current (10^{-7} A) as seen in Fig.3.5(a). For the DNTT TFT shown in Fig.3.5(b), the plasma-oxidized AlO_x film acts as the gate dielectric, and even without the solution-processed SAM, the gate current through the gate dielectric can be limited to approximately 10^{-11} A. Both these instances establish the importance of the oxygen-plasma process in forming a high quality AlO_x film as well as creating a sufficient density of surface hydroxyl groups for the formation of the SAM.

The importance of the oxygen plasma and the AlO_x component for DPh-BTBT TFTs, employing a fluoroalkyl phosphonic acid SAM, is not as significant as the DNTT TFTs, but nevertheless also important enough to cause a variation in the gate current. Without the oxygen-plasma grown AlO_x film, the gate current in the transistor (as seen in Fig.3.6(a)) is almost 10^{-9} A, which is one to three orders of magnitude higher than the TFTs employing the oxygen-plasma grown AlO_x film in the gate dielectric.

The AlO_x film in these DNTT and DPh-BTBT TFTs was formed by exposing the underlying aluminum gate electrode to an oxygen plasma with the following plasma process parameters: oxygen flow rate 30 sccm, oxygen partial pressure 0.01 mbar, RF power 200 W and duration 30 seconds. Chapter 4 investigates the effect of varying the plasma power and plasma duration between 10 W-300 W and 10 s-1800 s respectively on the resulting AlO_x film properties and thereby the electrical properties of the TFTs. Chapter 5 further investigates the thickness and the composition of the plasma-oxidized AlO_x

films.

3.3.2 The SAM component of the hybrid gate dielectric

Fig.3.5(b) shows the transfer characteristics and gate current of a DNTT TFT with a gate dielectric composed of only the plasma-grown AlO_x, i.e. without the solution-processed SAM. Comparing the performance of this TFT to the one displayed in Fig.3.5(c), it can be observed that employing the SAM in the hybrid gate dielectric reduces the overall gate current by almost an order of magnitude from 10^{-10} A to 10^{-11} A. More significantly, it can be observed that the TFT with the hybrid gate dielectric has a charge-carrier mobility of 1.9 cm^2/Vs, which is much larger than the charge-carrier mobility of the TFT with only the AlO_x dielectric, which has a mobility of 0.4 cm^2/Vs. This is likely due to the action of the SAM, which helps in creating a suitable surface for the growth of the organic semiconductor (DNTT in this case), as well as screening the polaronic charge formation between the AlO_x and the charge carriers in the organic semiconductor channel. These phenomenon will be further discussed in Chapter 4 and Chapter 6.

Considering the DPh-BTBT TFTs with the different gate-dielectric configurations, it can be observed that by employing the fluoroalkyl phosphonic acid SAM in the hybrid gate dielectric, shown in Fig.3.6(c), the gate leakage current through the dielectric is reduced to a minimum value of 10^{-12} A, significantly lower than the gate current of either of the two single-component dielectric TFTs in Fig.3.6(a) or Fig.3.6(b). It can be observed that DPh-BTBT as an organic semiconductor is relatively less sensitive to the dielectric in terms of the charge-carrier mobility of the TFTs. However, an important advantage and function of using functionalized SAMs can be observed. By employing the fluoroalkyl phosphonic acid SAM in the gate dielectric, either by itself or as a part of the hybrid dielectric, as shown in Fig.3.6(a) and Fig.3.6(c) respectively, the threshold voltage of the transistor can be shifted to more positive values. This is an important function of SAMs in hybrid gate dielectrics for organic TFTs and will be explored in depth in Chapter 6.

In general, it can be observed that the AlO_x component formed by the oxygen plasma helps in minimizing the gate current of the transistor by forming a dense oxide dielectric and providing a surface for the SAM to assemble while the SAM contributes not only to

reduction in the gate leakage current but also in increasing the charge-carrier mobility in DNTT TFTs and favorably shifting the threshold voltage in DPh-BTBT TFTs.

3.4 Experimental

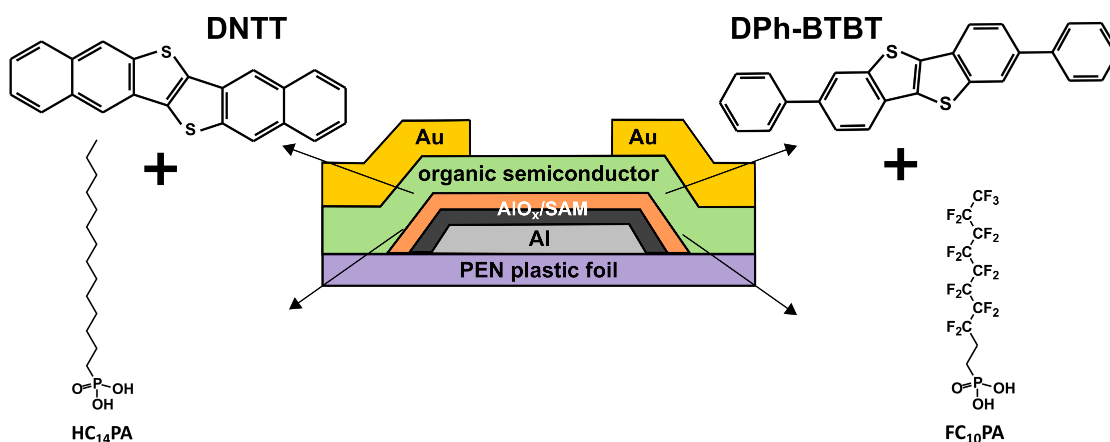


Figure 3.7: Schematic cross-section of the organic TFTs fabricated in this thesis chapter along with the chemical structures of the organic semiconductors DNTT and DPh-BTBT and the different alkyl and fluoroalkyl phosphonic acid molecules chosen to form SAMs in the hybrid gate dielectrics

The TFTs demonstrated in Fig.3.5 and Fig.3.6 were fabricated on flexible, 125 μm-thick polyethylene naphthalate (PEN) substrates. For the gate electrode of the TFTs, aluminum films with a thickness of 30 nm were deposited by thermal evaporation in vacuum with a rate of about 20 Å/s. AlO_x films were produced by plasma oxidation in pure oxygen with a partial pressure of 0.01 mbar using the capacitively coupled plasma mode with an excitation frequency of 13.56 MHz. The RF power applied to generate the plasma was 200 W and the duration was limited to 30 s. After the plasma oxidation, SAMs were formed by immersing the substrates into a 2-propanol solution with a concentration of 1 mM for a minimum of 3 hours of the respective molecules used to form the SAM.

For the TFTs in Fig.3.5, n-tetradecylphosphonic acid, ($HC_{14}PA$; PCI Synthesis, Newburyport, MA, USA) molecules was used to form a self-assembled monolayer. The small-molecule organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich) was deposited by thermal sublimation in vacuum with a deposition rate of 0.3 Å/s and with a nominal thickness of 25 nm. During the DNTT deposition, the substrate was held at a constant temperature of 60 °C.

For the TFTs in Fig.3.6, 1H,1H,2H,2H-perfluorodecylphosphonic acid, ($FC_{10}PA$; Specific

Polymers) molecules was used to form a self-assembled monolayer. The small-molecule organic semiconductor 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT; Sigma Aldrich) was deposited by thermal sublimation in vacuum with a deposition rate of 0.3 Å/s and with a nominal thickness of 25 nm. During the DPh-BTBT deposition, the substrate was held at a constant temperature of 25 ℃.

For the source-drain contacts of the TFTs, gold films with a thickness of 30 nm were deposited by thermal evaporation in vacuum with a rate of 0.3 Å/s. The metals and the organic semiconductors were patterned using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany). The TFTs have a channel length of 20 μm and a channel width of 100 μm. All electrical measurements were performed in ambient air at room temperature under yellow laboratory light.

3.5 Summary and outlook

This chapter has introduced the hybrid gate dielectric that will be further explored in this thesis, i.e. a combination of aluminum oxide and phosphonic acid SAMs. It has been shown that hybrid dielectrics are hugely successful in forming high-quality gate dielectrics with low leakage-current densities to enable low-voltage and low-power organic TFT operation. The contribution of each of the components forming the hybrid dielectric has been emphasized. Apart from the work in this thesis, a deeper investigation into the characterization of the SAMs (for their packing density and molecular order), precise control of TFT properties using SAMs, multiple combinations of SAMs and organic semiconductors and a comprehensive influence of the SAM on the organic semiconductor would greatly contribute to the understanding of the precise functioning of SAMs and the development of organic TFTs.

Chapter 4

Optimizing plasma oxidation for aluminum oxide films in hybrid gate dielectrics

The first component of the hybrid gate dielectrics investigated in this thesis is an ultrathin aluminum oxide (AlO_x) film fabricated by the plasma-assisted oxidation of the surface of the underlying aluminum gate electrode in organic TFTs. As already mentioned in Chapter 3, there are several methods of forming or depositing metal-oxide films for gate dielectrics in organic TFTs, with techniques such as atomic layer deposition [112, 175], anodic oxidation [176, 186], UV/ozone-assisted oxidation [179, 180], and plasma-assisted oxidation used to fabricate AlO_x films. By exposing the surface of the aluminum gate electrode to an oxygen plasma, the high-energy oxygen ions in the plasma impinge on and diffuse into the aluminum film, and oxidize the surface to form a thin film of aluminum oxide in a self-limiting process. The plasma-assisted oxidation process has several advantages and is extremely well-suited for the purpose of fabricating high-capacitance gate dielectrics in low-voltage organic TFTs. The plasma-oxidation process helps to greatly simplify the fabrication process because unlike in anodic oxidation, electrical contact to the gate metal is not required [187]. Another main advantage is that the plasma-oxidation process is area-selective, i.e. the oxide is formed only where the aluminum film is present and where the oxide is required for TFT operation. This eliminates the need of any additional subtractive patterning process to open vias for

interconnects [188]. The greatest advantage is the formation of a high-quality, native interface between the gate metal and the gate oxide, which minimizes hysteresis in the current–voltage characteristics and the subthreshold swing of the TFTs [189, 190]. In addition, the plasma-oxidation process is also compatible with alternative substrates such as flexible plastic foils and paper, suitable for the potential applications of organic TFTs.

There have been several reports of using plasma-assisted oxidation to fabricate AlO_x films as components of hybrid gate dielectrics in organic TFTs on a variety of substrates such as silicon wafers [183, 184], glass [35, 182, 191], flexible plastic foils [181] and paper [37]. However, in the absence of a direct control of the oxide film properties during plasma oxidation, the influence of the different process parameters on the properties of the AlO_x films and thereby on the organic TFT characteristics needs to be investigated. In this chapter, the process of plasma oxidation to prepare the AlO_x films is optimized to determine the ideal process parameters, specifically the plasma power and the duration of plasma exposure. Different combinations of the plasma power and the plasma duration were selected to fabricate AlO_x films as gate dielectrics in capacitors as well as in organic TFTs based on the small-molecule organic semiconductor DNTT. The influence of these parameters on the material and film properties of the AlO_x films, either as bare-AlO_x gate dielectrics or hybrid AlO_x/SAM gate dielectrics are investigated and are correlated to subsequent effects on the semiconductor morphology and the electrical properties of organic TFTs.

Among the surface properties of the gate dielectric, the surface roughness has a large influence on the morphology of the semiconductor in bottom-gate devices and the overall performance of organic TFTs. Several reports in literature have shown the negative impact of the surface roughness of the gate dielectric on the charge-carrier mobility of organic TFTs, i.e. an increased surface roughness of the gate dielectric decreases the charge-carrier mobility in the transistor [108, 192–196]. This effect is mainly attributed to a lower quality of the semiconductor film on rougher gate dielectric surfaces, for example, the semiconductor film has an increased density of grain boundaries, reduced crystallinity, etc. Several strategies have been employed to tune the surface roughness of the dielectric such as modifying the substrate temperature during deposition of the underlying gate electrode [197], adding a polymeric smoothening layer on the rough dielectric [198], annealing [199], etc [200–202]. In this chapter, the influence of the plasma process parameters on the surface roughness of the gate dielectric, and subsequently on

the semiconductor morphology will be investigated in detail.

When an aluminum metal film is exposed to air, a native aluminum oxide film is spontaneously formed on the surface due to air-oxidation. However, this native oxide film is extremely thin (∼1-3 nm [203]) and inadequate as a high-quality gate oxide. Fig.4.1(a) shows the transfer characteristics and gate current for an organic TFT with the native aluminum oxide film as the single gate dielectric, i.e. neither an oxygen-plasma process nor a solution-processed SAM was used. There is no observable field-effect behavior in the device and additionally, a large gate leakage current can be observed (10^{-7} A at a gate-source voltage of -3 V). Fig.4.1(b) shows an AFM micrograph of the organic semiconductor DNTT deposited on the native AlO_x surface and it can be seen that the semiconductor does not form a complete film, but only individual, disconnected islands instead. This indicates that the native AlO_x film is not sufficiently thick as a gate dielectric and also does not provide a suitable surface for the deposition of the organic semiconductor.

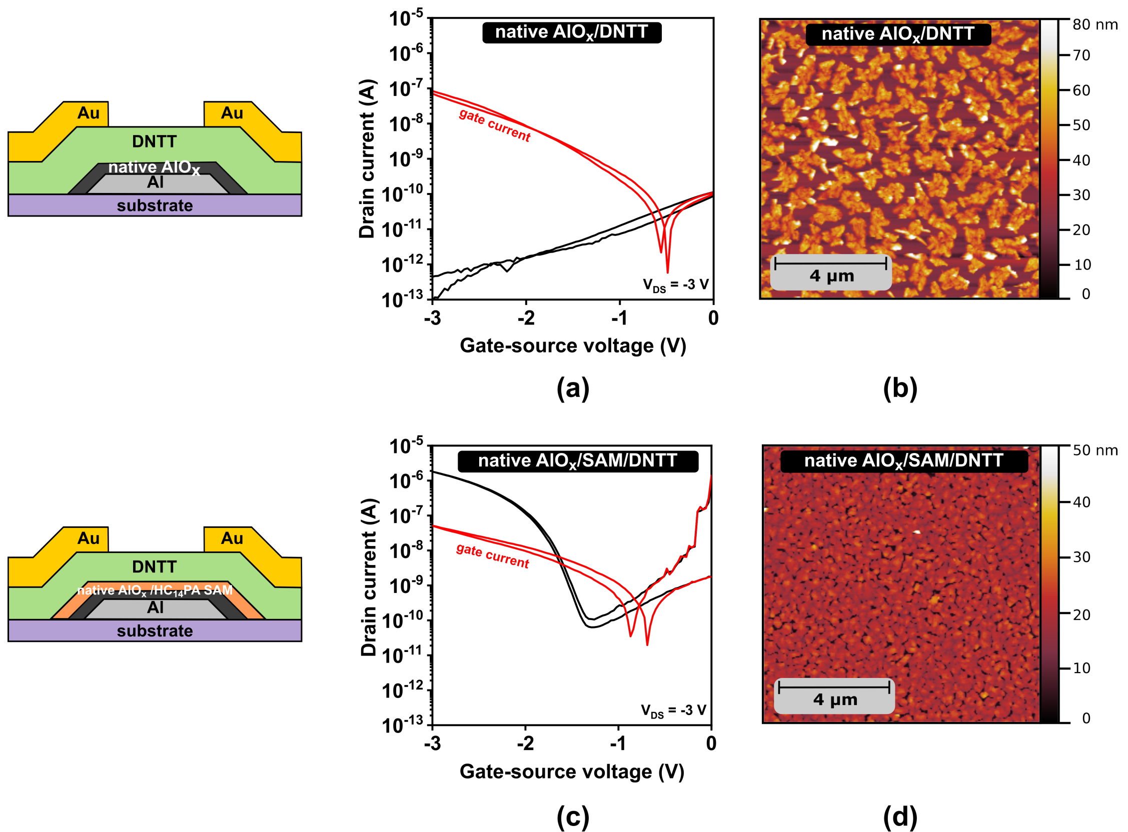


Figure 4.1: Transfer characteristics and gate currents of DNTT TFTs fabricated using native aluminum oxide (obtained without plasma process) either as (a) the gate dielectric or (c) as part of a hybrid AlO_x/SAM gate dielectric. AFM micrographs of DNTT films deposited onto (b) the bare native AlO_x and (d) the hybrid AlO_x/SAM gate dielectric are also shown.

Fig.4.1(c) shows the transfer characteristics and gate current of an organic TFT in which the gate dielectric is a combination of the native AlO_x film and an alkyl phosphonic acid SAM ($HC_{14}PA$), i.e. no oxygen-plasma process was used but the SAM was formed on the native oxide surface from solution. The transfer curve shows the presence of a field effect in the device, but the gate current is still extremely large (10^{-8} A at a gate-source voltage of -3 V). Fig.4.1(d) shows an AFM micrograph of the organic semiconductor DNTT deposited on the surface of the SAM and a connected, albeit with gaps, semiconductor film can be observed. Although the hybrid gate dielectric formed by the native AlO_x and the SAM forms a suitable surface for organic semiconductor deposition and field-effect behavior can be achieved in the transistor, the gate dielectric is of extremely poor quality as evidenced by the large gate current. A high density of hydroxyl groups is required to facilitate the adsorption of the SAM. Without the oxygen plasma, there are fewer groups present, which results in a low-quality gate dielectric.

This shows the requirement for the oxygen-plasma process to produce a thin, yet high-quality AlO_x film on the surface of the underlying aluminum gate electrode to form high-quality hybrid gate dielectrics in organic TFTs.

4.1 Thickness of plasma-grown AlO_x films

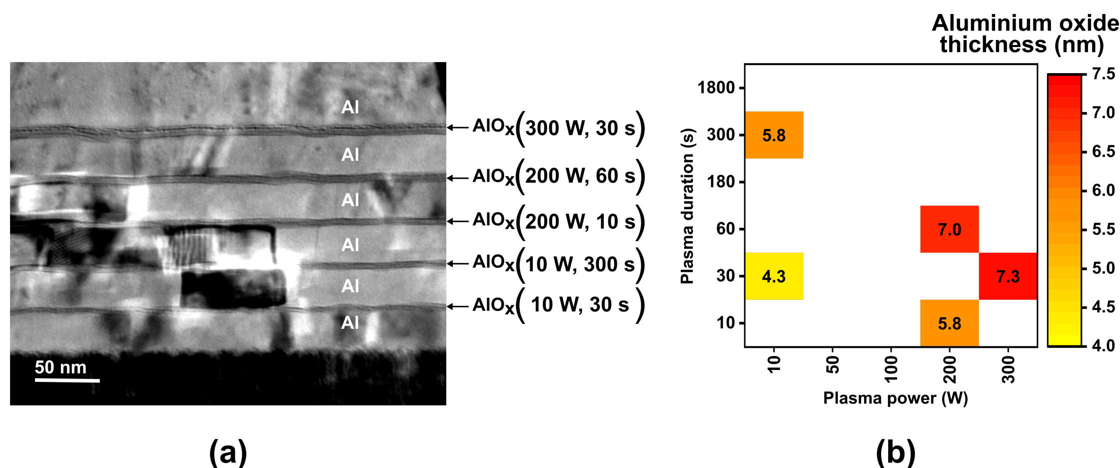


Figure 4.2: Thickness of plasma-grown AlO_x films. (a) Cross-sectional TEM (Transmission electron microscopy) image indicating the thicknesses of five AlO_x films produced sequentially by the plasma-assisted surface oxidation of aluminum using five different combinations of plasma power and plasma duration. (b) Summary of the results

Plasma power (W)	**Plasma duration (s)**	**Aluminum oxide thickness (nm)**
10	30	4.3 ± 0.2
10	300	5.8 ± 0.3
200	10	5.8 ± 0.1
200	60	7 ± 0.3
300	30	7.3 ± 0.4

Table 4.1: Thickness of AlO_x films (with error margins) prepared by different combinations of the plasma power and plasma duration as determined by TEM

The thickness of the gate dielectric in a transistor is of extreme importance as it determines the capacitance of the gate dielectric and thereby the operating voltage of the transistor. In certain fabrication techniques there is higher degree of control over the film thickness. For example, during atomic layer deposition (ALD), the thickness of the deposited films can be controlled by the number of cycles in the process. In thermal or electron-beam evaporation, the thickness is controlled by monitoring the rate of deposition using a quartz microbalance. With plasma oxidation, there is no such direct control of the film thickness during the growth process. Hence, there is a need to identify means of controlling the film thickness in an indirect manner. Five combinations of the plasma power and the plasma duration were chosen in five different processes to prepare AlO_x films of varying thicknesses. Fig.4.2(a) shows a cross-sectional TEM (transmission electron microscopy) image of a specimen prepared on a silicon substrate by repeating the deposition of 30-nm-thick aluminum and the plasma-assisted oxidation of the aluminum surface five times, each time with a different combination of the plasma power and plasma duration. The five combinations of process parameters selected were: (1) 10 W, 30 s (2) 10 W, 300 s (3) 200 W, 10 s (4) 200 W, 60 s and (5) 300 W, 30 s. During each transfer of the substrate from the metal-deposition system to the plasma system, the aluminum surface was necessarily exposed to ambient air, causing the spontaneous formation of a native oxide film with a thickness of approximately 3 nm on the aluminum surface [203]. The thickness of the five different AlO_x films along with the error margin as determined from the TEM image are given in Table 4.1. The TEM image indicates that after the plasma-assisted oxidation, the aluminum oxide films have a thickness of approximately 4.3 nm to 7.3 nm, depending on the plasma parameters. (The method of extracting the thickness of the AlO_x films from the TEM image is detailed in Section 4.6). The lower limit of this thickness range (4.3 nm) is thus larger by approximately 1.3 nm than the thickness of the native oxide. Although this increase in the oxide thickness produced by the plasma process is quite small, it is of critical

importance for the proper operation of organic TFTs in which these dielectrics are used as the gate insulator, as seen in the previous section. The relation between the plasma parameters and the thickness of the plasma-grown AlO_x films extracted from the TEM image is also illustrated in Fig.4.2(b). As expected, both a larger plasma power (by virtue of a higher kinetic energy of the oxygen radicals impinging on the oxide surface) and a longer plasma duration (by virtue of a larger number of incident radicals) result in thicker AlO_x films. Thus, an AlO_x film of a desired thickness within the available range of 4.3 nm to 7.3 nm can be fabricated using the plasma-assisted oxidation process by selecting a suitable combination of parameters as seen in Fig.4.2(b).

4.2 Dielectric properties of plasma-grown AlO_x films

One of the most important figures of merit for a gate dielectric is the gate-dielectric capacitance, because a large gate-dielectric capacitance makes it possible to operate the transistor with low operating voltages. This section examines the electrical properties of oxygen-plasma grown AlO_x films employed in metal-insulator-metal capacitors, either as bare-AlO_x dielectrics or as hybrid AlO_x/SAM dielectrics. Fifteen different combinations of plasma power (ranging from 10 to 300 W) and plasma duration (ranging from 10 to 1800 s) were selected to fabricate the AlO_x films. A schematic cross-section of the capacitors, the materials and techniques utilized to fabricate them and a photograph are included in Section 4.6.

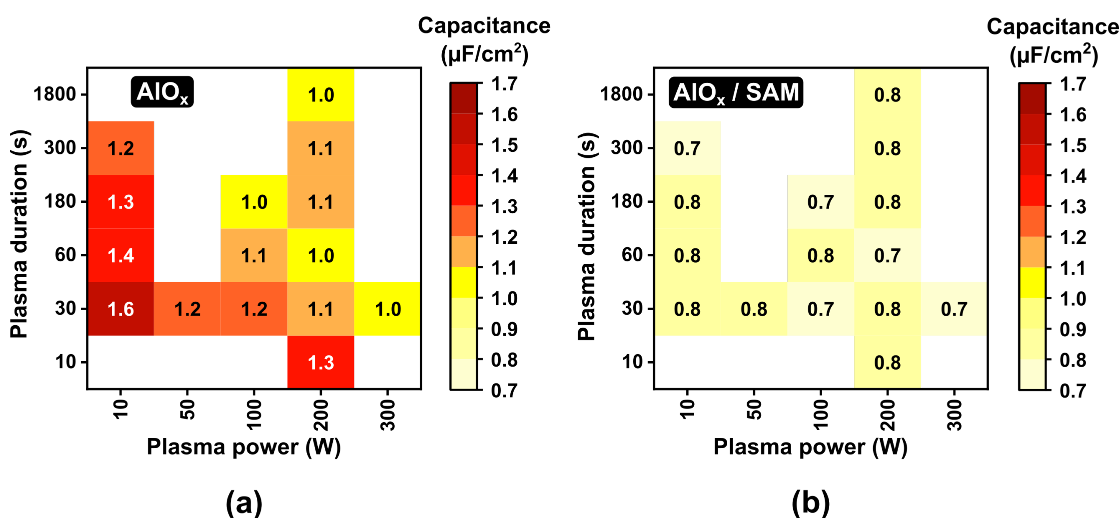


Figure 4.3: Measured unit-area capacitance of capacitors with (a) a bare-AlO_x dielectric and (b) a hybrid AlO_x/SAM dielectric as a function of plasma power and plasma duration

The measured unit-area capacitance of the capacitors with a bare-AlO_x dielectric is plotted as a function of the plasma power and the plasma duration in Fig.4.3(a). Depending on these parameters, the unit-area capacitance varies from 1 to 1.6 $\mu F/cm^2$, with the general trend of a higher power and a longer duration producing AlO_x films with a smaller capacitance. Fig.4.3(a) reveals that the influence of the plasma duration on the capacitance is relatively small, as long as the plasma power is at least 50 W and the duration is at least 30 s. For example, for a plasma power of 200 W, a unit-area capacitance of 1 $\mu F/cm^2$ is obtained for a plasma duration of one minute, as well as for a much longer plasma duration of half an hour. Although it is possible to use the bare, plasma-grown AlO_x films as the gate dielectric for organic TFTs [156, 204, 205], hybrid gate dielectrics composed of the plasma-grown AlO_x and a phosphonic acid-based self-assembled monolayer (SAM) are far more advantageous, as already discussed in Section 3.3. Fig.4.3(b) shows the unit-area capacitance of the capacitors with a hybrid AlO_x/SAM dielectric, plotted as a function of the plasma power and plasma duration. Due to the additional contribution of the SAM, the capacitance of the hybrid AlO_x/SAM dielectric (0.7–0.8 $\mu F/cm^2$) is smaller than that of the bare-AlO_x dielectric (1–1.6 $\mu F/cm^2$) and shows a notably smaller dependence on the plasma power and duration.

A few important conclusions can be drawn by combining the results from the unit-area capacitance measurements and the TEM results. The thickness of the plasma-grown AlO_x films is observed to saturate at a value of approximately 7 nm after a plasma duration of 30 to 60 seconds, provided the plasma power is at least 50 W. The self-limiting behavior of the growth of the oxide films can be explained by the Cabrera-Mott model [206], in which the low electronic conductivity of aluminum oxide and the small diffusivity of oxygen in aluminum oxide prevent oxygen from reaching the metal surface, once the oxide thickness has reached a certain value determined mainly by the plasma power [207, 208]. Compared with the dependence of the capacitance on the plasma duration, its dependence on the plasma power appears to be more monotonic, but overall, the range over which the capacitance of the plasma-grown AlO_x can be tuned is nevertheless quite small (less than a factor of two). One benefit of this small range of accessible capacitances is that it renders the fabrication process more robust by suppressing the effects of unintended process-parameter variations on the resulting TFT characteristics. Fig.4.4 illustrates the unit-area capacitance measured for each of the five parameter combinations for which the AlO_x thickness was determined by TEM (Fig. 4.2) plotted as a function of the inverse of that thickness. The error bars reflect the accuracy of the

method by which the oxide thickness was extracted from the TEM image (Section 4.6). Since it was not possible to include all fifteen combinations of the plasma power and plasma duration for the TEM measurement, the five combinations were chosen to cover both the extremes and the center of the range of thicknesses and capacitances as much as possible. By fitting the measurement data with the theoretical relationship between the unit-area capacitance C_{ox} and the oxide thickness t_{ox}:

$$C_{\mathrm{ox}} = \varepsilon_0 \varepsilon_{ox} \frac{1}{t_{\mathrm{ox}}} \tag{4.1}$$

(where ε_0 is the vacuum permittivity and ε_{ox} the relative permittivity of the plasma-grown oxide) and forcing the linear fit through the origin ($1/t_{ox} = 0$; $C_{ox} = 0$), the relative permittivity of the plasma-grown AlO_x is determined to be **8 ± 0.2**. This result is in good agreement with the relative permittivity reported in the literature for aluminum oxide films produced by various methods [209–211].

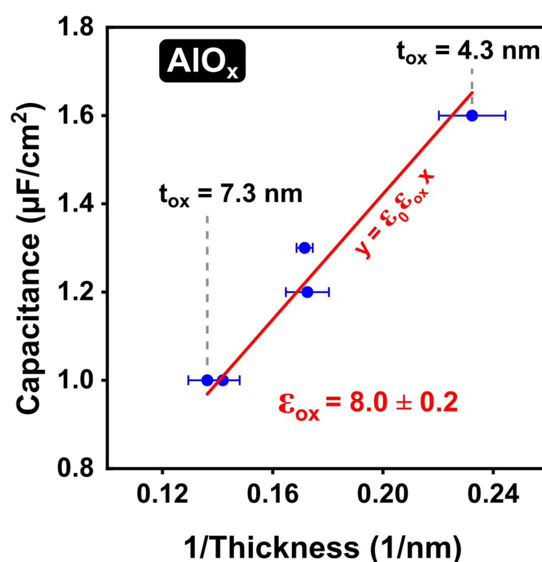


Figure 4.4: Calculation of the relative permittivity of plasma-grown AlO_x: Unit-area capacitance of bare-AlO_x dielectrics plotted as a function of the inverse of the AlO_x thickness determined by TEM to calculate the relative permittivity of the plasma-grown AlO_x. The red line is a linear fit of Eqn.4.1 that was forced to pass through the origin ($1/t_{ox} = 0$; $C_{ox} = 0$).

The total capacitance of the hybrid AlO_x/SAM gate dielectric (C_{diel}) can be considered as a combination of the two individual capacitances in parallel:

$$\begin{aligned} \frac{1}{C_{\mathrm{diel}}} &= \frac{1}{C_{\mathrm{ox}}} + \frac{1}{C_{\mathrm{SAM}}} \\ &= \frac{t_{\mathrm{ox}}}{\varepsilon_0 \varepsilon_{\mathrm{ox}}} + \frac{t_{\mathrm{SAM}}}{\varepsilon_0 \varepsilon_{\mathrm{SAM}}} \end{aligned} \tag{4.2}$$

(where C is the unit-area capacitance, t is the thickness, with the subscript ox referring to the oxide and SAM referring to the SAM. ε_0 is the absolute permittivity.)

The reported value of the relative permittivity of the SAM ($\varepsilon_{\mathrm{SAM}}$) is 2.5 [139], which is much smaller than the relative permittivity of the oxide as calculated above ($\varepsilon_{ox} = 8$). Comparing these values in the context of Eqn.4.2, the term $\dfrac{1}{C_{\mathrm{SAM}}}$ dominates the value of the total gate-dielectric capacitance, and the influence of the oxide capacitance is minimized. This explains why the hybrid gate-dielectric capacitance does not vary much with the plasma power and plasma duration in Fig.4.3(b).

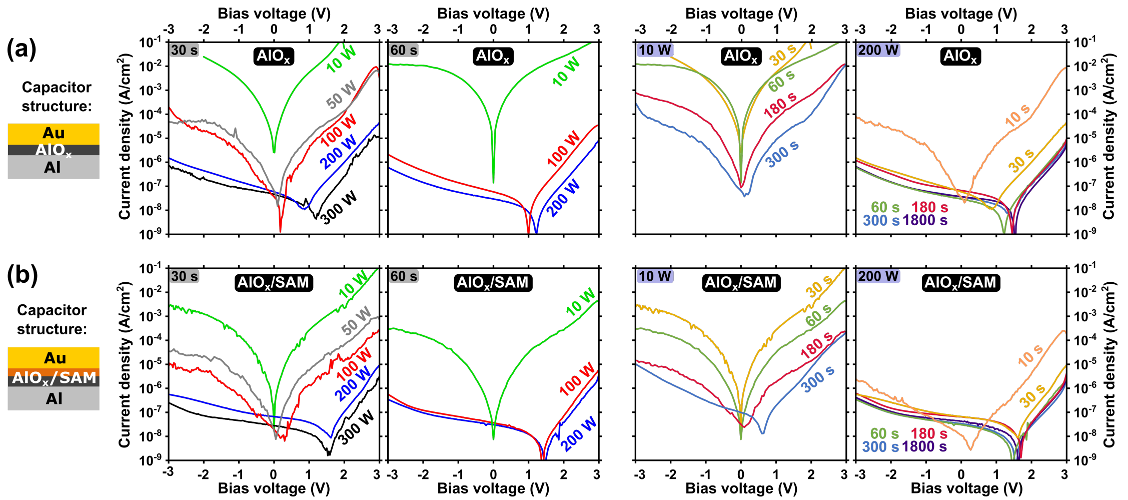


Figure 4.5: Current density measured as a function of applied voltage through capacitors with (a) a bare-AlO_x dielectric and (b) a hybrid AlO_x/SAM dielectric for various combinations of plasma power and plasma duration.

In addition to the capacitance, the current–voltage characteristics of the capacitors were also measured to analyze the influence of the plasma power and duration on the leakage-current density through the dielectrics. The results for the capacitors with a bare-AlO_x dielectric are summarized in Fig.4.5(a). The general trend is similar to the one seen for the capacitance in Fig.4.3(a) and is consistent with the TEM results: a higher plasma

power and a longer plasma duration lead to thicker AlO_x films characterized by smaller leakage-current densities. When the plasma power is smaller than about 50 to 100 W and the plasma duration is shorter than about 30 to 60 s, the leakage-current density through the bare-AlO_x films exceeds 10^{-4} A/cm^2 at ±3 V. On the other hand, for a plasma power of 200 W and a plasma duration of 60 s, the current density through the bare-AlO_x dielectrics is below 10^{-5} A/cm^2 at ±3 V. Fig. 4.5(a) also shows that it is not possible to produce bare-AlO_x dielectrics by plasma oxidation that provide leakage-current densities significantly below 10^{-6} A/cm^2 at ±3 V. The results of the measurements of the current density through the hybrid AlO_x/SAM dielectric are summarized in Fig.4.5(b). As can be seen, the leakage-current density through the hybrid AlO_x/SAM dielectrics is smaller by approximately an order of magnitude than the current density through the bare-AlO_x dielectrics, regardless of the plasma parameters. For a plasma power of 200 W and a duration of 60 s, the leakage-current density through the hybrid AlO_x/SAM dielectric drops below 10^{-6} A/cm^2. While this confirms the beneficial effect of the SAM in improving the insulating properties of the gate dielectric for low-power organic TFTs, the results in Fig.4.5(b) also clearly demonstrate the critical importance of providing an optimized AlO_x film, even when complementing it with a SAM.

4.3 Electrical properties of organic TFTs with plasma-grown AlO_x films as gate dielectrics

On the same substrates as the capacitors discussed above, bottom-gate, top-contact DNTT TFTs were also fabricated with either a bare-AlO_x or a hybrid AlO_x/SAM gate dielectric produced with the same fifteen combinations of plasma power and duration as discussed above. Fig.4.6 (bare-AlO_x gate dielectric) and Fig.4.7 (hybrid AlO_x/SAM gate dielectric) show the measured transfer characteristics and gate currents of TFTs fabricated with three of these plasma-parameter combinations. The complete set of results is shown in Appendix B.

One observation from Fig.4.6 and Fig.4.7 is that a plasma power of 10 W is insufficient to suppress the gate-leakage current to an acceptable level, regardless of the plasma duration and regardless of whether or not the AlO_x film is complemented with a SAM. The minimum plasma power required to obtain AlO_x films with sufficient thickness and

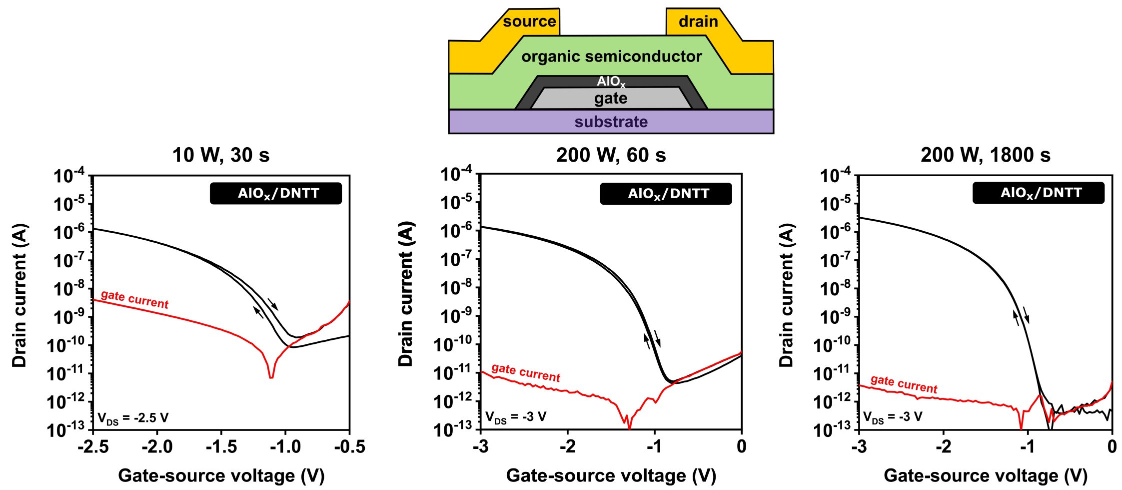


Figure 4.6: Transfer characteristics and gate currents of DNTT TFTs fabricated with a bare-AlO_x gate dielectric for three combinations of plasma power and plasma duration. (Appendix B shows the complete set of results)

sufficient quality is 50 W, which limits the gate current to 10^{-11} A over the range of gate-source voltages considered here (0 to -3 V). For a plasma power in the range of 100 to 200 W, both the bare-AlO_x and the hybrid AlO_x/SAM gate dielectric are able to provide gate currents not exceeding 10^{-11} A and on/off current ratios of 10^6. The optimum plasma duration for this range of plasma power is dictated by whether or not the AlO_x is complemented by a SAM: For the bare-AlO_x gate dielectric, the optimum plasma duration is $\geq$ 300 s, whereas for the hybrid AlO_x/SAM gate dielectric, the optimum plasma duration is in the range of 30 to 60 s (for a plasma power ranging from 100 to 200 W).

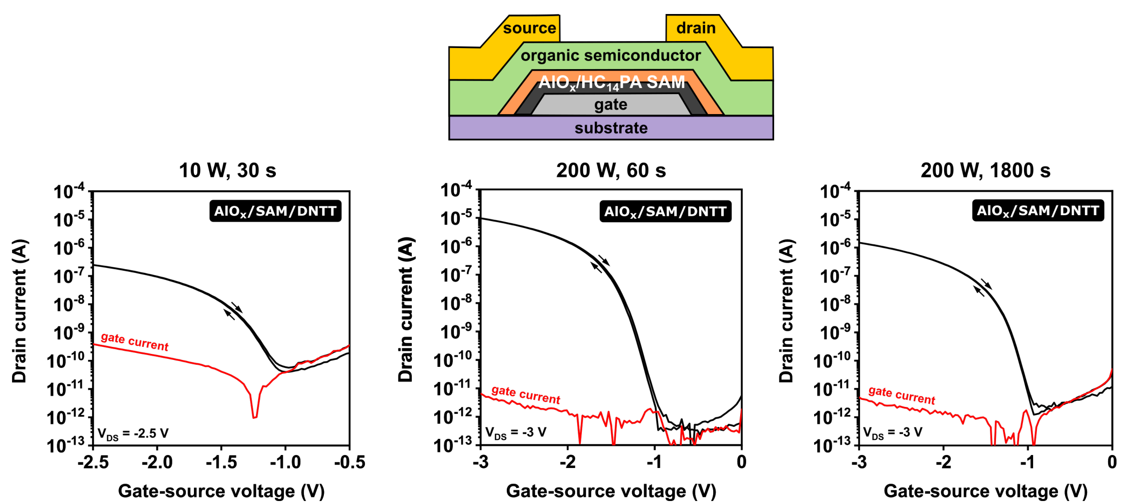


Figure 4.7: Transfer characteristics and gate currents of DNTT TFTs fabricated with a hybrid AlO_x/SAM gate dielectric for three combinations of plasma power and plasma duration. (Appendix B shows the complete set of results)

In Fig.4.8(a), the effective charge-carrier mobility extracted from the measured transfer characteristics of the DNTT TFTs with a bare-AlO_x gate dielectric is plotted as a function of the plasma power and the plasma duration. As can be seen, the carrier mobility of these TFTs is rather small, between 0.1 and 0.6 cm^2/Vs, which is possibly related to charge trapping and the formation of Fröhlich polarons, due to the fact that the organic semiconductor is in direct contact with the aluminum oxide [151, 212]. The dependence of the carrier mobility of the TFTs with a hybrid AlO_x/SAM gate dielectric on the plasma parameters is summarized in Fig.4.8(b). The beneficial contribution of the SAM, in providing a hydrophobic surface with a greatly reduced density of water-related trap sites and effective screening of the organic-semiconductor film from the high-permittivity oxide, leads to notably larger carrier mobilities of up to 2.3 cm^2/Vs. Closer inspection of Fig.4.8(b) shows that carrier mobilities of approximately 2 cm^2/Vs are obtained along a track from the upper left to the lower right corner of the graph, i.e., from low-power/long-duration to high-power/short-duration combinations. For parameter combinations outside of this corridor, the carrier mobilities are notably smaller, as small as 0.2 cm^2/Vs. The reasons for this distinctive parameter-dependence pattern will be elucidated in the following section.

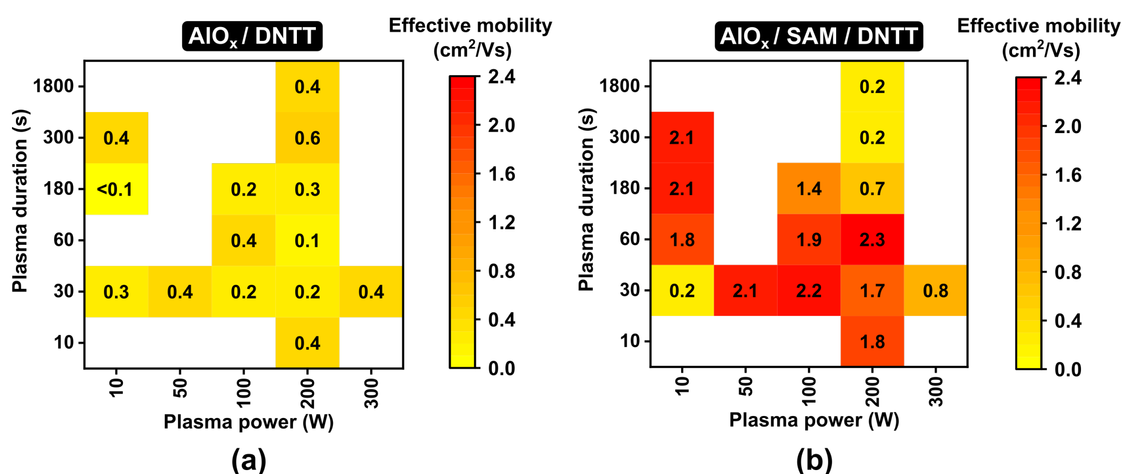


Figure 4.8: Effective charge-carrier mobilities extracted from the measured transfer characteristics of DNTT TFTs fabricated with either (a) a bare-AlO_x gate dielectric or (b) a hybrid AlO_x/SAM gate dielectric as a function of plasma power and plasma duration

4.4 Surface properties

The performance of field-effect transistors in general and of organic TFTs in particular is greatly dependent on the properties of the interface between the semiconductor and the gate dielectric [185]. In the case of bottom-gate TFTs, as considered here, this highlights the critical importance of the properties of the gate-dielectric surface. The surface energy and the surface roughness of the bare-AlO_x and the hybrid AlO_x/SAM dielectrics has been measured for each of the fifteen combinations of plasma power and plasma duration discussed above.

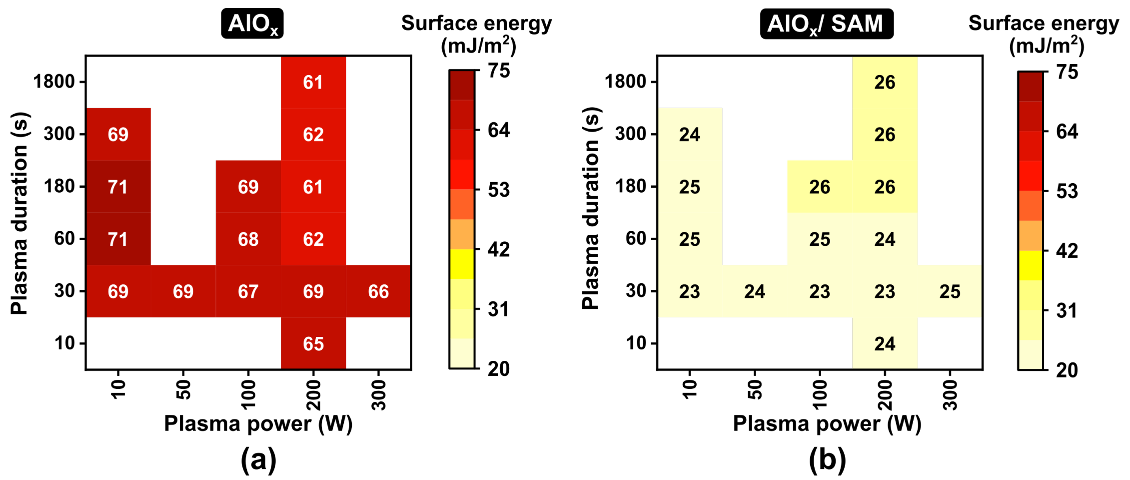


Figure 4.9: Surface energy of (a) bare-AlO_x dielectrics and (b) hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration

The surface energies of both the bare-AlO_x and the hybrid AlO_x/SAM gate dielectrics show only very small variations and no systematic dependence on the plasma parameters, as shown in Fig.4.9. The surface energy of the bare-AlO_x dielectric varies between 61 and 71 mJ/m^2, and that of the hybrid AlO_x/SAM dielectric between 23 and 26 mJ/m^2, similar to previous reports [120, 155].

The surface roughness, on the other hand, shows a clear correlation with the plasma parameters. Prior to the plasma-oxidation process, the vacuum-deposited aluminum has a root-mean-square (RMS) surface roughness of 0.9 nm [197]. After the plasma-oxidation process, the RMS surface roughness of the bare AlO_x ranges from 0.34 to 0.91 nm, depending on the plasma parameters (shown in Fig.4.10(a)). The general trend seen in Fig.4.10(a) is that higher plasma power and longer plasma duration lead to smoother AlO_x films. Given the difference between the RMS surface roughness of the aluminum

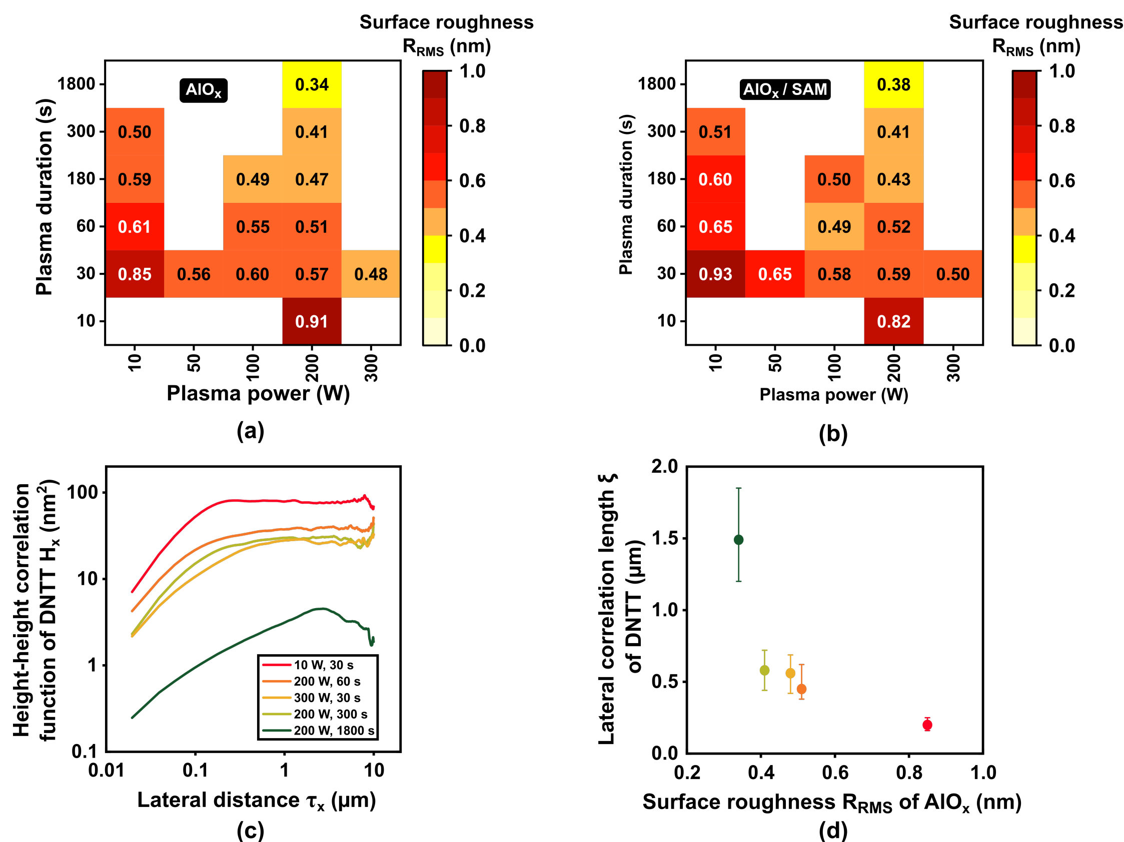


Figure 4.10: Root-mean-square surface roughness of (a) bare-AlO_x dielectrics and (b) hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration. (c) Height-height correlation functions (HHCF) of DNTT films deposited onto bare-AlO_x dielectrics for five combinations of plasma power and plasma duration. (d) Lateral correlation length ξ of the DNTT films as a function of the surface roughness of the bare-AlO_x dielectric.

prior to plasma oxidation (0.9 nm) and the RMS surface roughness of the plasma-grown AlO_x (0.34 to 0.91 nm), it appears that the plasma-oxidation process smoothens the surface, most prominently for sufficiently high plasma powers and sufficiently long durations. This effect was not observed in a similar study [197], in which an almost identical RMS surface roughness of 0.9 nm was measured for both the vacuum-deposited aluminum and the gate dielectric. However, that study did not explore the use of high plasma powers or long plasma durations, which might explain why no smoothening was observed.

The RMS surface roughness of the hybrid AlO_x/SAM gate dielectrics as a function of plasma power and duration is shown in Fig.4.10(b). Comparing Fig.4.10(a) and Fig.4.10(b) shows that the functionalization of the AlO_x surface with the SAM has no measurable effect on the roughness, i.e., the SAM covers the AlO_x surface in a conformal manner, as expected.

The degree of the surface roughness of the gate dielectric affects the properties of the organic-semiconductor film deposited onto it [197]. DNTT films were deposited on the different AlO_x and AlO_x/SAM surfaces, and the morphology was recorded using AFM (shown in Fig.4.11). To evaluate the DNTT thin-film morphology in a quantitative manner, the height-height correlation function (HHCF) was calculated from the AFM data using the following equation [213]:

$$H_{\mathrm{x}}(\tau_{\mathrm{x}} = \frac{1}{N(M-m)} \sum_{l=1}^{N} \sum_{n=1}^{M-1} \left(z_{\mathrm{n+m,l}} - z_{\mathrm{n,l}}\right)^2 \tag{4.3}$$

(where N and M are the number of measured rows and columns, z is the height of a measurement point, Δx is the sampling interval along the x direction, m an integer ($0 \leq m \leq M$), and τx is the lateral distance (τx = m Δx).)
The HHCF has two distinct regimes, as seen in Fig.4.10(c): over short lateral distances, the heights are correlated and the HHCF increases linearly with distance. Over long distances, the heights are uncorrelated and the HHCF saturates at a value proportional to $2R_{RMS}^2$, where R_{RMS} is the root-mean-square surface roughness [214]. The lateral distance at which the crossover between the two regimes occurs is the lateral correlation length ξ. In Fig.4.10(d), the lateral correlation length determined for each of the DNTT films deposited onto bare AlO_x (Fig.4.10(a)) is plotted as a function of the RMS surface roughness of the AlO_x. As can be seen, the lateral correlation length of the DNTT films shows a monotonic dependence on the AlO_x surface roughness, increasing from 0.2 nm for the largest surface roughness to 1.5 nm for the smoothest surface. However, these trends are not reflected in the measured charge-carrier mobilities of the TFTs in which these bare-AlO_x films serve as the gate dielectric (Fig.4.8(a)), since the carrier mobility in these DNTT films is greatly suppressed, presumably by charge trapping and polaronic effects resulting from the close proximity of the DNTT and the aluminum oxide.

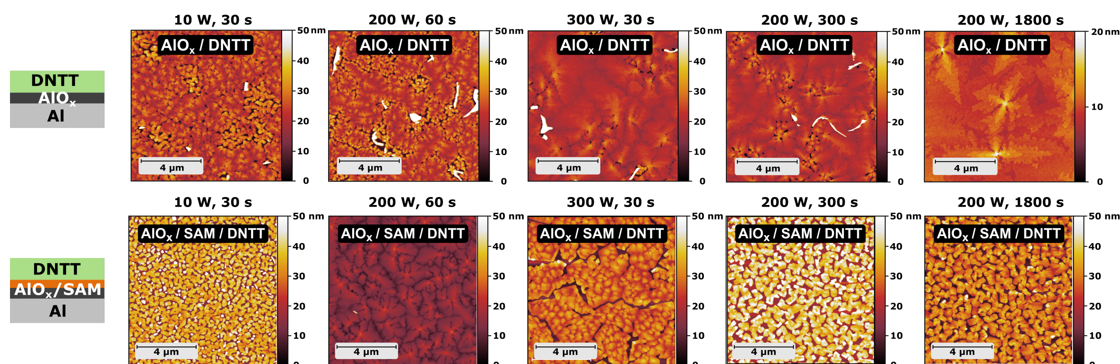


Figure 4.11: Morphology of DNTT films, imaged by AFM, deposited onto bare-AlO_x dielectrics and hybrid AlO_x/SAM dielectrics for five combinations of plasma power and plasma duration

The influence of the variation in surface roughness of the gate dielectric on the thin-film morphology of the semiconductor can be seen in Fig.4.11, in which AFM images show the morphology of DNTT deposited onto bare-AlO_x and hybrid AlO_x/SAM gate dielectrics produced using different plasma parameters. When DNTT is deposited onto a smooth dielectric surface, the DNTT film exhibits a pronounced terrace-like structure, whereas deposition onto a rough dielectric surface results in a notably smaller terrace size. Considering the DNTT films on the AlO_x/SAM hybrid gate dielectric surface, the plasma-parameter combination of 10 W, 30 s, which yielded a surface roughness of 0.93 nm (Fig.4.10(b)), leads to an island-like formation in the DNTT morphology, unsuitable for high-performance organic TFTs. On the other hand, for the plasma-parameter combination of 200 W, 60 s, which yielded a surface roughness of 0.52 nm (Fig.4.10(b)), an optimum terrace-like structure in a complete, continuous DNTT film can be seen. With an increase in either the plasma power or the plasma duration beyond this combination, a degradation in the DNTT film morphology can be observed, with either cracks appearing in the film, or an island-like discontinuous film structure.

4.5 Correlation of surface properties of the dielectric with electrical properties of the TFTs

The extent to which the carrier mobility of the TFTs with the hybrid AlO_x/SAM gate dielectric correlates with its surface roughness can be seen in Fig.4.12. The largest RMS surface roughness (0.93 nm; obtained with low plasma power/short duration; indicated in grey in Fig.4.12(c)) leads to a disordered DNTT film with small grains that shows a

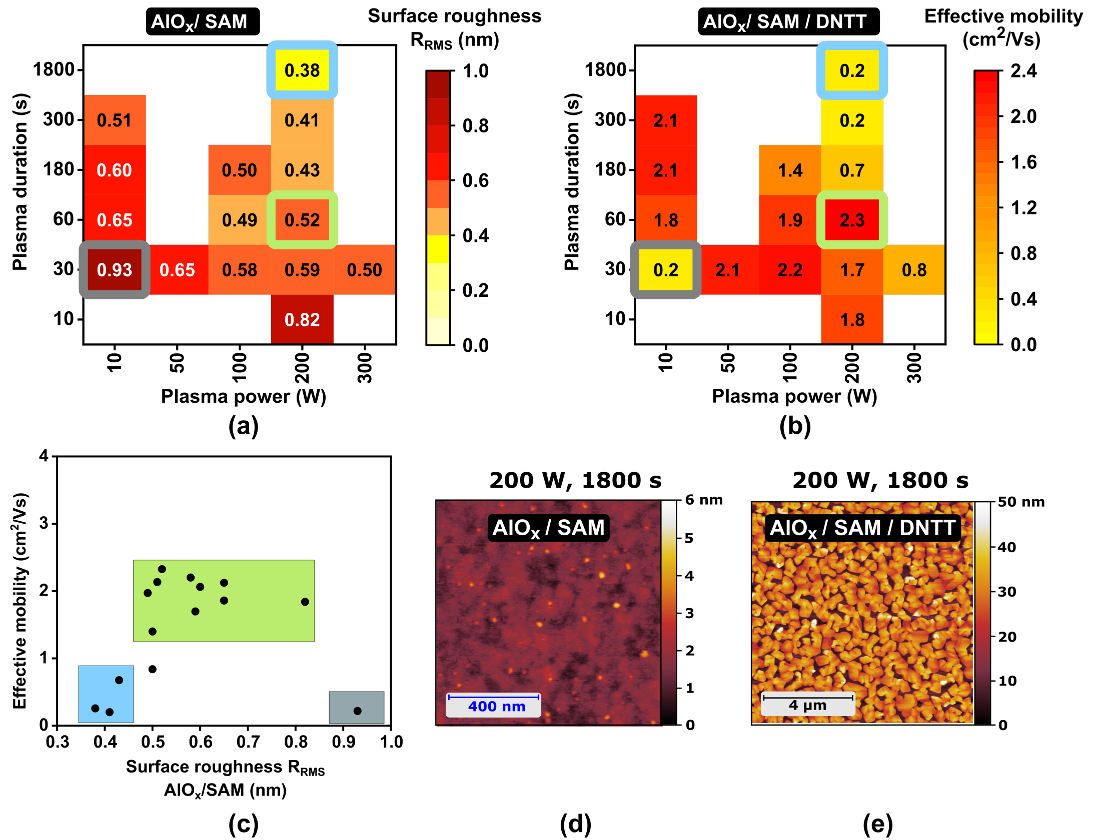


Figure 4.12: (a) Root-mean-square surface roughness of hybrid AlO_x/SAM dielectrics as a function of plasma power and plasma duration (b) Carrier mobilities extracted from the measured transfer characteristics of DNTT TFTs fabricated with a hybrid AlO_x/SAM gate dielectric as a function of plasma power and plasma duration (c) Carrier mobility plotted as a function of the RMS surface roughness (d), (e) AFM images of representative morphologies on the indicated surfaces with the indicated plasma parameters

very small carrier mobility (0.2 cm^2/Vs), as expected. The largest carrier mobilities ($\geq$ 2 cm^2/Vs) are obtained only when the RMS surface roughness is below approximately 0.65 nm (indicated in green in Fig.4.12(c)), so that the DNTT morphology shows a pronounced terrace-like structure; this is also in line with expectations. On the other hand, the smallest RMS surface roughness (0.38 nm; obtained with medium power/long duration; indicated in blue in Fig.4.12(c)) does not lead to the largest carrier mobility, as one might have expected, but instead to a very small mobility (0.2 cm^2/Vs). The reason for this anomaly is revealed by the AFM image of this dielectric (Fig.4.12(d)), in which a large density of small, tall features can be seen protruding from the surface. These features do not significantly contribute to the calculated RMS surface roughness, but they influence the DNTT morphology in an unfavorable manner, as seen in Fig.4.12(e). The specifics of these tall features are unknown, but the fact that they appear only for long plasma durations ($\geq$ 300 s) suggests that they mark some form of mechanical

damage created on the AlO_x surface by prolonged plasma exposure. AFM images of DNTT films deposited onto hybrid AlO_x/SAM dielectrics for all fifteen combinations of plasma power and plasma duration are collected in Appendix B.

4.6 Experimental

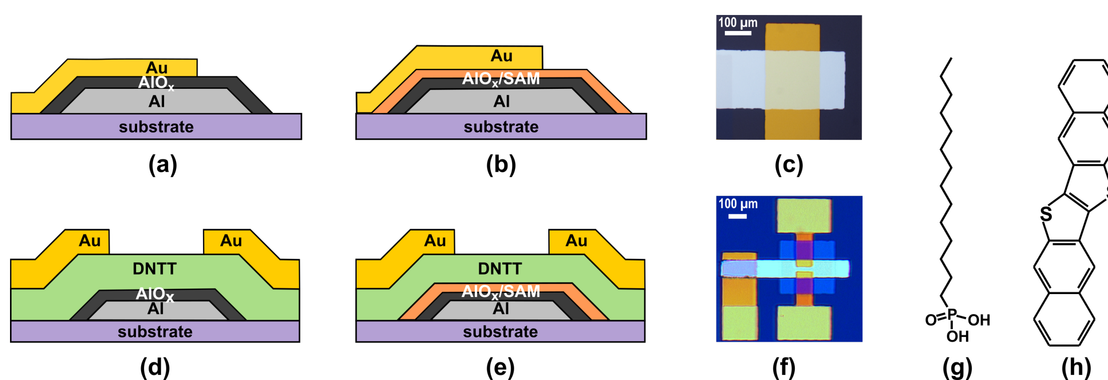


Figure 4.13: Schematic cross sections and photographs of metal–insulator–metal capacitors and bottom-gate, top-contact TFTs in which the insulator or gate dielectric is either a film of plasma-grown AlO_x or a combination of plasma-grown AlO_x and an n-tetradecylphosphonic acid ($HC_{14}PA$) SAM. Also shown are the chemical structure of n-tetradecylphosphonic acid ($HC_{14}PA$) and of the organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT)

Fabrication of capacitors and TFTs on silicon substrates

Metal–insulator–metal capacitors and inverted staggered (bottom-gate, top-contact) TFTs were fabricated on silicon substrates coated with 100-nm-thick thermally grown silicon dioxide. For the bottom electrode of the capacitors and the gate electrode of the TFTs, aluminum with a thickness of 30 nm and a root-mean-square surface roughness of less than 1 nm (measured by AFM) was deposited by thermal evaporation in vacuum with a rate of about 20 Å/s. AlO_x films were produced by plasma oxidation in an Oxford Instruments ProLab100 Cobra system in pure oxygen with a partial pressure of 0.01 mbar using the capacitively-coupled-plasma mode with an excitation frequency of 13.56 MHz. Substrates with fifteen different combinations of plasma power (ranging from 10 to 300 W) and duration (ranging from 10 to 1800 s) were fabricated. After the plasma oxidation, each substrate was cleaved into two halves. One half was immersed into a 2-propanol solution of n-tetradecylphosphonic acid ($HC_{14}PA$; PCI Synthesis, Newburyport, MA, USA)

to form a self-assembled monolayer and hence a hybrid AlO_x/SAM gate dielectric. The other half remained without SAM (bare-AlO_x gate dielectric). Onto both halves of each substrate, the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich) was deposited by thermal sublimation in vacuum with a deposition rate of 0.3 Å/s and with a nominal thickness of 25 nm. During the DNTT deposition, the substrate was held at a constant temperature of 80 °C. For the top electrode of the capacitors and the source/drain contacts of the TFTs, gold with a thickness of 30 nm was deposited by thermal evaporation in vacuum with a rate of 0.3 Å/s. The metals and the DNTT were patterned using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany). The capacitors have an area of 200 μm × 200 μm. The TFTs have a channel length of 20 μm and a channel width of 100 μm. For each of the fifteen combinations of plasma power and plasma duration, capacitors and TFTs were fabricated on the same substrate to minimize the effects of unintentional parameter variations.

TEM characterization

The TEM specimen was prepared on a silicon substrate by repeating the deposition of 30-nm-thick aluminum and the plasma-induced oxidation of its surface five times, each time with a different combination of plasma power and plasma duration. Preparing all five AlO_x films on the same substrate, rather than on five separate substrates, was helpful in minimizing the time required for thinning the specimen in preparation for cross-sectional microscopy. The TEM specimen was fabricated by conventional focused ion beam (FIB) lift-out using a Thermo Fisher Scientific FEI Scios DualBeam instrument equipped with a gallium source. A platinum strip was deposited to protect the films from ion-beam damage. A lamella with a size of approximately 20 μm × 10 μm was released from the substrate and glued to a copper TEM lift-out grid. The lamella was then thinned to a thickness of less than 100 nm using an acceleration voltage of 30 kV and an ion current of initially 500 pA that was successively decreased to 100 pA. Afterwards, the lamella was cleaned using a low-voltage cleaning step with an acceleration voltage of 5 kV and an ion current of 48 pA to remove gallium-beam damage. The TEM image was recorded in bright-field (BF) mode using a Philips CM-200 FEG TEM operated with an acceleration voltage of 200 kV.

TEM Analysis

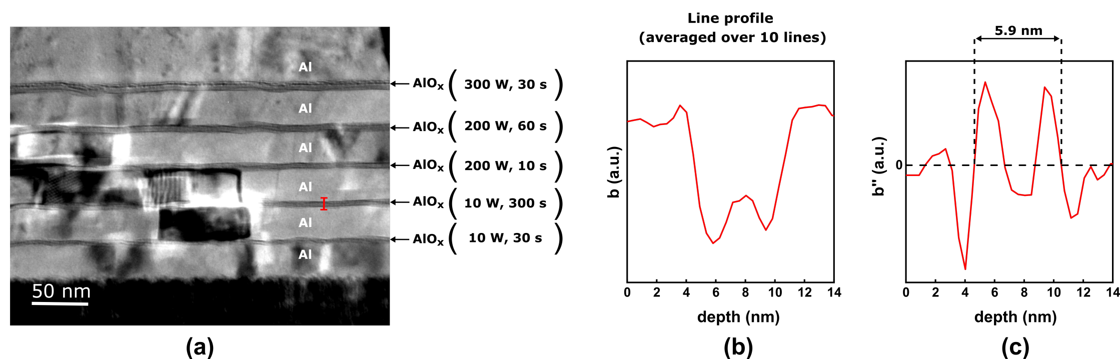


Figure 4.14: Analysis of the cross-sectional TEM image to extract the thicknesses of the AlO_x films produced using five different combinations of plasma power and plasma duration: (10 W, 30 s), (10 W, 300 s), (200 W, 10 s), (200 W, 60 s), (300 W, 30 s).

From the digital data representing the TEM image (Fig.4.14(a)), a depth profile (having a line width of 10 pixels) through the AlO_x film (starting and ending a few nanometers above and below the Al/AlO_x interfaces) representing the average pixel brightness (denoted as "b") was extracted using the image software Gwyddion (Fig.4.14(b)). In the depth profile, the materials Al and AlO_x are distinguished by larger and smaller values of the pixel brightness b, respectively. The second derivative of b with respect to the depth was calculated and plotted as a function of depth to identify the points of inflection (b" = 0) in the depth profile, and the distance between these points was measured as the thickness of the AlO_x film (Fig.4.14(c)). For each of the five AlO_x films, this process was repeated 10 times in various locations across the TEM image.

Electrical characterization

All electrical measurements were performed in ambient air at room temperature under yellow laboratory light. The capacitance measurements were performed using a Hameg HM8118 LCR meter by applying an alternating voltage with an amplitude of 0.2 V and a frequency of 1 kHz. The current– voltage measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer and the measurement software "SweepMe!" (https:// sweep-me.net).

Surface characterization

AFM images were recorded in air using a Bruker Dimension Icon Atomic Force Microscope in peak force tapping mode (for the DNTT films) or in tapping mode

(for the gate dielectrics). Data processing was performed using the AFM analysis software Gwyddion. Static contact-angle measurements were performed using a Krüss contact angle measurement system. The contact angles of water and hexadecane on the AlO_x dielectrics were measured immediately after the plasma treatment of the aluminum films. The contact angles of water and hexadecane on the AlO_x/SAM hybrid dielectrics were measured immediately after the SAM treatment. The surface energies were calculated using the Owens–Wendt method [99].

4.7 Summary and Outlook

Ultrathin, high-capacitance hybrid gate dielectrics based on oxygen-plasma-grown aluminum oxide films in combination with an alkyl phosphonic acid SAM are fabricated for the realization of low-voltage organic TFTs. Depending on the plasma power and the duration of the plasma exposure, the thickness of the plasma-grown AlO_x films can be tuned to values between approximately 4.3 and 7.3 nm. The lower limit of the range of accessible thicknesses is dictated by the thickness of the native aluminum oxide film (approximately 3 nm) that forms spontaneously when the substrates are exposed to ambient air prior to the plasma-oxidation process, while the upper boundary is set by the inherently self-limiting oxidation kinetics of aluminum oxide close to room temperature. The relative permittivity of the oxygen-plasma-grown AlO_x films is approximately 8 ± 0.2, and the capacitance of the bare-AlO_x films thus falls into the range from 1 to 1.6 μF/cm2. By allowing a high-quality monolayer of an alkyl phosphonic acid with a medium alkyl-chain length to self-assemble on the freshly grown AlO_x surface, a hybrid AlO_x/SAM dielectric is obtained, the capacitance of which varies between 0.7 and 0.8 $\mu F/cm^2$. The leakage-current density through the hybrid AlO_x/SAM dielectrics was found to be smaller by about an order of magnitude than the current density through bare-AlO_x dielectrics. The importance of optimizing the underlying AlO_x film with suitable plasma parameters to achieve an overall reduced leakage-current density in the AlO_x/SAM hybrid dielectric is established. The effective charge-carrier mobility of DNTT TFTs with a bare-AlO_x gate dielectric is no greater than 0.6 cm^2/Vs, and shows little dependence on the plasma parameters. In TFTs with a hybrid AlO_x/SAM gate dielectric, carrier mobilities ranging from 1.8 to 2.3 cm^2/Vs were obtained for a number of favorable combinations of plasma power and plasma duration that produce AlO_x films

with low surface roughness and thus promote the formation of high-quality SAMs and well-ordered DNTT films on these dielectrics. The largest carrier mobility equaling 2.3 cm^2/Vs was obtained for a plasma-parameter combination of 200 W and 60 s.

An important finding of this chapter is the correlation between the surface properties of the gate dielectric and the electrical properties of the organic TFT. The plasma-assisted oxidation process can be used to form a high-quality gate oxide film, and more importantly, to tune the surface roughness of the AlO_x film. An optimum surface roughness obtained by a medium plasma power and a medium plasma duration promotes a favorable organic semiconductor morphology, which is best suited for high charge-carrier mobilities in organic TFTs. However, while the properties of the plasma-grown AlO_x films can be tuned over a certain range without negatively affecting the charge-transport properties in the organic-semiconductor films deposited onto them, this is only true as long as the plasma power and the plasma duration do not exceed values beyond which the quality of the plasma-grown oxide films suffers from surface damage. The nature and extent of this surface damage must be characterized and surface properties other than the surface roughness need to be investigated. This will enrich our understanding of the effect of extreme plasma process parameters on the AlO_x surface, as well as on the performance of organic TFTs.

Chapter 5

Investigating the thickness and composition of plasma-grown aluminum oxide films in hybrid dielectrics

The importance of the ultrathin aluminum oxide (AlO_x) film as the gate oxide in the hybrid gate dielectric, as well as the optimization of the plasma-oxidation process to fabricate the AlO_x film has been established in previous chapters. In Chapter 3, the importance of the AlO_x film towards suppressing the leakage-current density and providing a suitable surface for the SAM to adsorb on was discussed. A range of film deposition and growth techniques are used to fabricate AlO_x films for gate dielectrics in organic TFTs, such as atomic layer deposition (ALD) [112, 175, 215], plasma-enhanced chemical vapor deposition (PE-CVD) [216], sputtering, pulsed laser deposition (PLD) [217], anodization [115, 218], along with solution-processing techniques such as spin-coating [219–221], bar-coating [222], etc. Compared to those techniques, the plasma-oxidation process produces a self-patterned, ultrathin and dense AlO_x film with a high-quality native interface with the underlying aluminum gate electrode. In addition, it is also compatible with alternative substrates such as plastic foils and paper, intended for use in organic TFT applications.

However, the plasma process also has certain shortcomings compared to the other deposition and thin-film fabrication techniques. Due to the nature of the process, there is a limited degree of control over the thin-film properties during the plasma-oxidation process, although certain properties of the AlO_x film and their influence on the electrical properties of organic TFTs have already been examined in Chapter 4. For example, AlO_x films of varying thicknesses were fabricated by changing the plasma power and the duration of plasma exposure. The influence of the plasma process on the surface properties of the AlO_x films, particularly the surface roughness was also demonstrated. It has been established that the AlO_x film fabricated by the plasma-oxidation process forms a high-quality gate oxide in hybrid gate dielectrics for low-voltage organic TFTs, making it a worthwhile endeavor to further characterize this film. Knowledge of the film properties such as the thickness of the film and the film composition can lead to a better understanding of the role of the gate dielectric, and can potentially provide better control over the electrical performance in organic TFTs. The standard characterization techniques employed to investigate the thickness and chemical composition of metal oxide films are: X-ray Photoelectron Spectroscopy (XPS), Atomic Emission Spectroscopy (AES), X-Ray Diffraction (XRD), etc. However, due to the nature of the AlO_x film prepared by the plasma-oxidation process, in particular, its small thickness and its proximity to the underlying aluminum gate electrode, several of the above mentioned techniques are rendered impractical for characterization, and access to the thin-film properties of the AlO_x films is quite challenging. Nevertheless, the thin-film composition has been investigated using two different techniques : Electron Energy Loss Spectroscopy (EELS), in combination with Transmission Electron Microscopy (TEM) and Atom Probe Tomography (APT). The preliminary results from these two measurement techniques and the challenges faced during measurement are detailed in this chapter. Chapter 4 already discussed the effect of the plasma-process parameters on the electrical characteristics of organic TFTs. Certain combinations of the plasma power and the plasma duration were instrumental in forming AlO_x films with an optimum surface roughness ((R_{RMS}) $\pm$ 0.5 nm), and hence organic TFTs with high charge-carrier mobilities. One of these combinations, i.e. a plasma power of **200 W** and a plasma duration of **30 s** has been selected to fabricate AlO_x films in this chapter and further characterize them in terms of the thickness of the film and its chemical composition. This plasma-parameter combination was also chosen to fabricate AlO_x films in the organic TFTs studied in the further chapters, and is thus most suitable to be considered

for further characterization here.

5.1 Thickness of plasma-grown AlO_x films

In order to operate organic thin-film transistors (TFTs) at low supply voltages, the overall thickness of the hybrid gate dielectric must be limited to a minimum value. The thickness of the hybrid gate dielectric is mainly controlled by the thickness of the oxide, since the thickness of the self-assembled monolayer (SAM) is limited to one molecular length of the particular molecule selected and does not have much scope for variation.

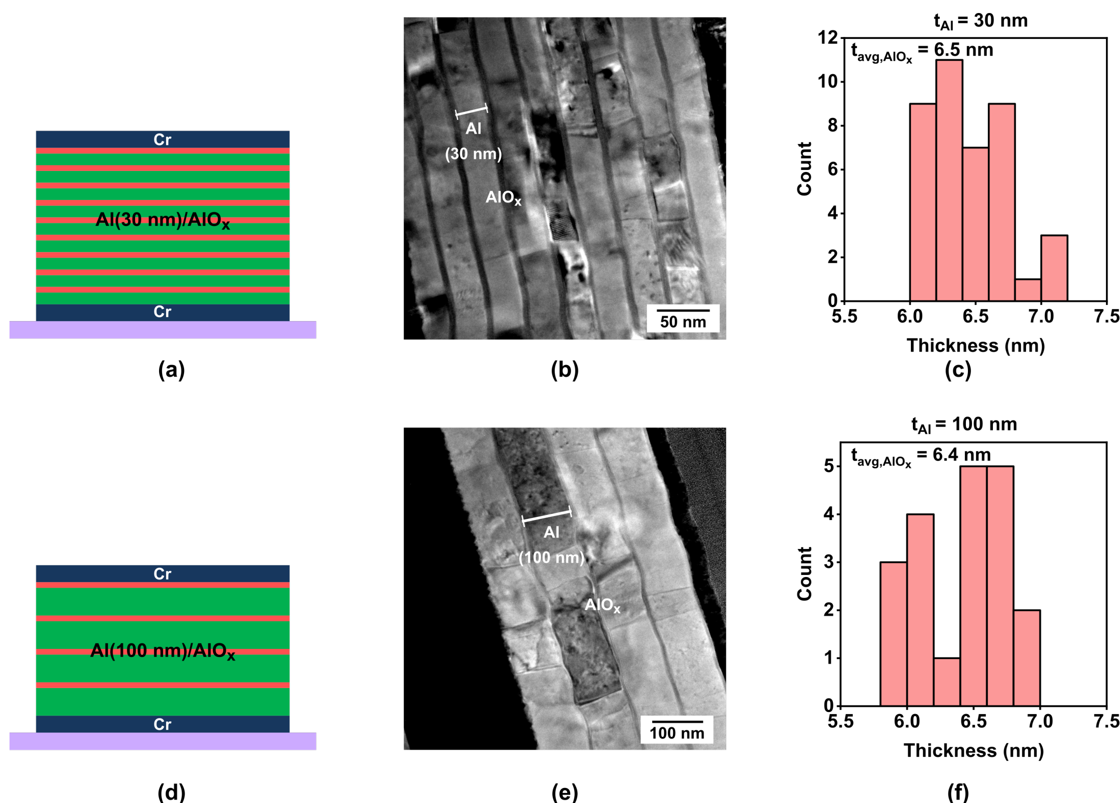


Figure 5.1: Thickness of plasma-grown AlO_x films as measured by transmission electron microscopy (TEM) in a multilayer Al/AlO_x structure. The AlO_x films were prepared by oxidizing the surface of aluminum films of two different nominal thicknesses, 30 nm and 100 nm

The plasma-oxidation process is extremely effective in forming an ultrathin AlO_x film, with the thickness of the film determined by the self-limiting nature of the process. In Chapter 4, the thickness of the AlO_x film was varied between approximately 4 nm and 7 nm using different combinations of the plasma-process parameters. In this section, AlO_x films have been fabricated with a plasma power of 200 W and a plasma duration of 30

s to measure the thickness of the films and examine the reproducibility of the plasma process. As shown in Fig.5.1, two different multilayer structures were fabricated by sequentially depositing aluminum films, and the surface of the aluminum was oxidized in an oxygen plasma. Aluminum films with nominal thicknesses of 30 nm and 100 nm were deposited to examine the influence of the thickness of the underlying aluminum film on the thickness of the subsequently formed AlO_x film. Chromium films with a nominal thickness of 100 nm were deposited before and after the Al/AlO_x multilayers to protect them from ion-milling damage while fabricating samples for transmission electron microscopy (TEM).

Fig.5.1(a) shows a schematic of the multilayer structure with nine aluminum thin films, each with a nominal thickness of 30 nm and the respective AlO_x films at the surface of each aluminum film. Fig.5.1(b) shows the TEM image of this Al/AlO_x multilayer structure, and the results are summarized in Fig.5.1(c), which were obtained from image analysis as explained in Chapter 4, Section 4.6. From a total of 40 positions, the average thickness of the AlO_x films measured is **6.5 ± 0.5 nm**. Similarly, Fig.5.1(d) shows the schematic of the multilayer structure with four aluminum films with a nominal thickness of 100 nm and the respective AlO_x films, and the TEM image in Fig.5.1(e). The average thickness of the AlO_x films, when measured in 20 positions, is **6.4 ± 0.4 nm**, as summarized in Fig.5.1(f).

Considering both multilayer structures, the thickness of the AlO_x films has a narrow deviation from the average value, which confirms the reproducible and reliable nature of the oxygen-plasma process to fabricate ultrathin AlO_x films with a particular thickness. By observing the effect of the plasma process on aluminum films of distinctly different thicknesses, it can be concluded that the thickness of the plasma-grown AlO_x films can be varied only by varying the plasma-process parameters, and the thickness of the underlying aluminum film has virtually no influence on it.

The gate-dielectric capacitance of a metal-insulator-metal structure with an AlO_x film prepared using the plasma-parameter combination 200 W, 30 s is approximately 1.1 $\mu F/cm^2$, as shown in Fig.4.3(a). According to the relationship between the thickness of the gate-dielectric film and the gate-dielectric capacitance given by Eqn.2.9, and the relative permittivity of the plasma-oxidized AlO_x film determined in Chapter 4 (8 ± 0.2), the theoretical value of the thickness of the AlO_x film from the measured capacitance is calculated to be 6.4 nm, which is in good agreement with the measured thickness by TEM.

5.2 Composition of plasma-grown AlO_x films

As already mentioned in Chapter 3, several metal oxides are popular choices for gate dielectric materials in organic TFTs. The thin-film characterization of metal oxide films is important for determining their suitability as a gate dielectric and correlating the film properties of the metal oxide to the electrical properties of organic TFTs. One of the most important thin-film properties is the chemical composition, particularly for metal oxide gate dielectric films. A metal oxide with a perfect stoichiometric chemical composition is best suited as a gate dielectric material, while any disparity within the composition may affect its dielectric properties. For example, if a non-stoichiometric metal oxide film has a disproportionately large metal contribution, the film will display a stronger metallic behavior and be less effective as a gate dielectric in the transistor.

Among the various thin-film deposition and fabrication techniques, the group of chemical vapor deposition methods rely on a chemical reaction with precursors of the desired material to react with the surface of the substrate to fabricate a thin film in a controlled and self-limiting manner. Due to the chemical nature of the process, the resultant thin film has an almost stoichiometric composition, i.e. aluminum oxide films fabricated by ALD have a oxygen-aluminum ratio between 1.5 and 2 [223]. Similarly, in physical vapor deposition techniques such as sputtering and thermal evaporation, the thin film is deposited by condensation of a gas phase from a target material and the composition of the final thin film can be controlled by the composition of the target material. In such processes, a perfect stoichiometric Al_2O_3 film can be deposited to form the gate dielectric in transistors.

In contrast, the plasma-oxidation process does not afford a direct control of the thin-film composition of the fabricated AlO_x film. The fabrication of the AlO_x film proceeds through oxygen ions and electrons in the oxygen plasma impinging on and reacting with the underlying aluminum surface. It has already been established in Chapter 3 that the AlO_x film prepared by the oxygen-plasma process serves as an excellent gate dielectric for low-voltage organic TFTs. The investigation of the composition of the AlO_x film is thus required to correlate it with the electrical performance of the organic TFTs, and possibly, further improve the gate-dielectric properties of the AlO_x films.

However, as it will be explained in the following sections, the characterization of the plasma-grown AlO_x films is not as straightforward as standard thin-film composition investigations. The plasma-oxidized AlO_x film has two relevant aspects which influence

the thin-film characterization, viz. the thickness of the film is relatively very small, approximately 6.5 nm, and the AlO_x film is in close proximity with the underlying aluminum film.

Certain photoelectron spectroscopy techniques are traditionally used to characterize thin films for elemental composition, such as X-ray Photoelectron Spectroscopy (XPS) or Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS). XPS is a surface-sensitive technique which uses X-rays to probe the surface of interest and the kinetic energy of the emitted electrons can be used to identify and quantify the elemental composition and electronic state of the atoms in the material. The depth of analysis of XPS is approximately 10 nm from the surface, which exceeds the typical thickness of the plasma-grown AlO_x films. Since the AlO_x films are always in close contact with the underlying aluminum films, the analysis depth of XPS extends into the aluminum, and a strong background signal makes it difficult to isolate the characterization of the AlO_x film. On the other hand, ToF-SIMS uses a finely focused ion beam to excite the surface material to emit secondary ions and ion clusters, whose exact mass and time-of-flight is instrumental in identifying the elements or molecular fragments in the material. However, the depth of analysis in this technique is approximately 1 nm, which is much smaller than the typical thickness of the AlO_x film, and an ion milling technique will be required in conjunction to probe the entire depth of the AlO_x film. In addition, there are also problems with the exact quantification of elements, which will hinder the possibility of finding the exact composition of the AlO_x film using ToF-SIMS.

For these reasons, techniques with a higher spatial resolution, closer to an atomic scale, are required to characterize the plasma-grown AlO_x films. The two techniques chosen in this work are (1) Electron Energy Loss Spectroscopy (EELS), in combination with Transmission Electron Microscopy (TEM) and (2) Atom Probe Tomography (APT).

5.3 Qualitative measurement by TEM-EELS

Electron Energy Loss Spectroscopy (EELS) is a high-resolution analytical technique implemented along with High-Resolution TEM in which the transmitted beam of electrons through the material is analyzed for the energy loss of electrons that occurs due to inelastic scattering during transmission. The amount of energy loss, as measured by a spectrometer, can be interpreted and assigned to the different causes of the energy

loss, such as inelastic interactions, phonon excitations, inter and intra-band transitions, plasmon excitations, inner shell ionizations, etc. to spatially map the elemental composition from the same specimen region, as observed by TEM. Fig.5.2 shows a schematic representation of the process, in conjunction with a TEM apparatus.

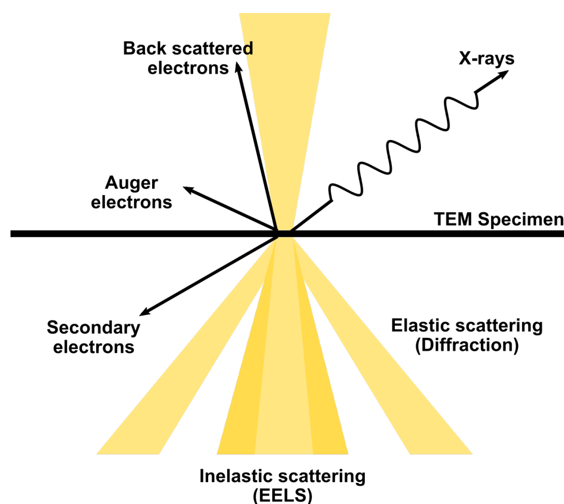


Figure 5.2: Schematic representation of the different electron beam interactions in a transmission electron microscope and the inelastically scattered electrons which are relevant for Electron Energy Loss Spectroscopy (EELS)

The data collected from EELS can be depicted in two different ways, an energy loss spectrum and TEM images with contrast which convey spectral information in a spatially resolved manner, also referred to as energy-filtered TEM images. These images are useful in mapping the elemental distribution in a sample and extracting other material properties. The energy-loss spectrum typically has three different regions:

- **Zero-loss peak**: This part corresponds to electrons which have not lost any energy, i.e. electrons which haven't been scattered and electrons which have been elastically scattered after interaction with the atomic nuclei.
- **Low-loss region**: This part corresponds to energy losses less than 50 eV and represents beam electrons which have interacted with the weakly bound electrons in the sample. This part of the spectrum typically gives information about the band structure and the dielectric properties of the material.
- **High-loss or core-loss region**: This part of the spectrum is reserved for higher energy losses, greater than 50 eV where the beam electrons have interacted with the tightly bound core electrons of the atoms in the sample, and the overall number

of inelastically scattered electrons is much lower. This region in the spectrum contains characteristic features called 'ionization edges', which have element-specific characteristics.

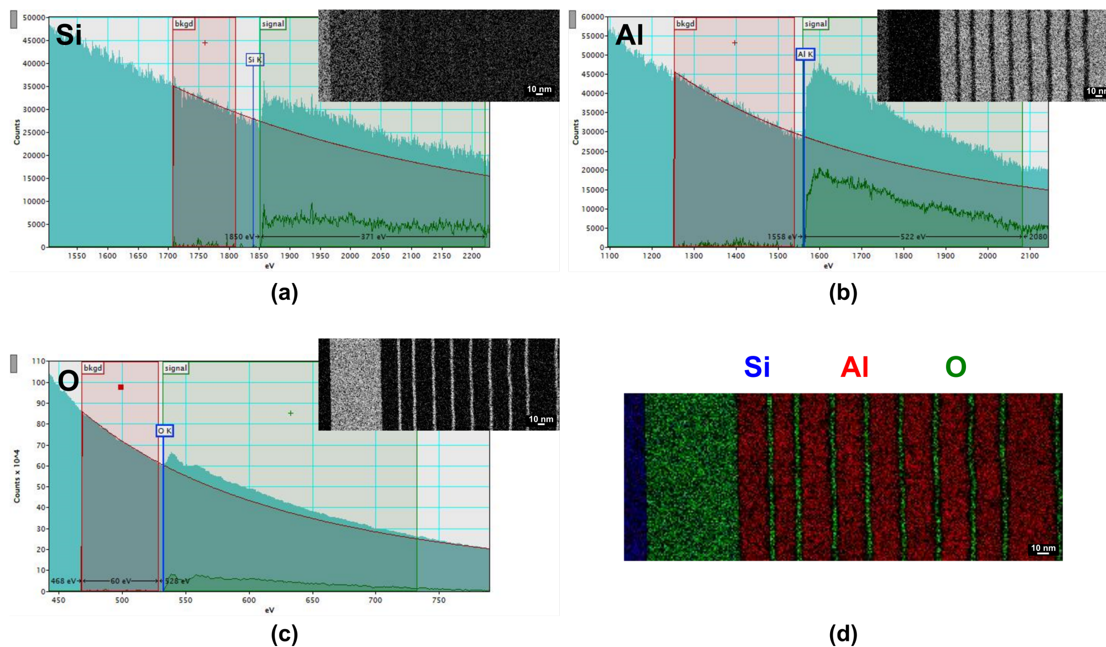
5.3.1 Experimental

A multilayer sample structure (similar to the one shown in Fig.5.1(a)) was chosen for analysis by EELS, i.e. a multilayer structure with aluminum films sequentially deposited and the surface oxidized in an oxygen plasma to form the respective AlO_x films. A silicon substrate with a thermally grown, 100 nm thick SiO_2 film, was chosen as the substrate on which the Al/AlO_x multilayer structure was fabricated.[1]

5.3.2 Results

A typical EELS spectrum consists of the signal intensity plotted as a function of the energy loss of the transmitted electrons. As mentioned above, the region of the spectrum with an energy loss greater than 50 eV is called the 'high-loss region' and appears as a smoothly falling *background* with characteristic features superimposed on it, known as **ionization edges**. Ionization edges are formed when an inner shell electron in the sample material absorbs enough energy from a beam electron to be excited into a state above the Fermi level energy, and have element-specific energies. Fig.5.3 shows the ionization edges found in the EELS spectrum obtained for the sample and the three specific elements identified: silicon, aluminum and oxygen. The specific elements were identified based on their K-edge ionization energies, as they appear in the spectrum: **silicon at 1839 eV, aluminum at 1560 eV and oxygen at 532 eV.** Based on the intensity of the signal obtained, the element specific characteristics can be spatially mapped in the TEM image, to identify which element is located at which position in the sample. Inset images in each of the spectra show energy-filtered TEM images with silicon, aluminum and oxygen mapped, based on the respective ionization energies. These three images are composed into an RGB image with the following color code: blue for silicon, red for aluminum, and green for oxygen, as seen in Fig.5.3(d). Based on this image, the silicon substrate, the SiO_2 layer and the alternating layers of aluminum and

[1]The preparation of the substrates using a Focused Ion Beam apparatus and the measurement using TEM-EELS were performed by Julia Deuschle, Yi Wang and Robin Lingstädt from the Max Planck Institute for Solid State Research.



(a)

(b)

(c)

(d)

Figure 5.3: High-loss region of the EELS spectrum with element specific ionization edges for (a) silicon, (b) aluminum and (c) oxygen with energy-filtered TEM images in the insets. (d) Composite RGB image depicting the spatially mapped elements in the TEM image

aluminum oxide can be clearly identified in a spatially mapped manner.

Apart from the high-energy-loss region of the spectrum, the low-loss region can also be analyzed for information, as shown in Fig.5.4. Fig.5.4(a) shows the low-loss region of the spectrum along with the zero-loss peak. The TEM image in the inset shows the position on the sample where the spectrum was collected, which was focused on one of the aluminum films. The zero-loss peak represents the beam electrons which haven't lost any energy and is always the tallest and most prominent feature of an EELS spectrum. The shape and size of the zero-loss peak is an indication of the energy resolution of the spectrum. In any measured spectrum, the zero-loss peak is spread over energies around 0 V and has a finite energy width due to the energy resolution of the spectrometer as well as the energy spread of the beam electrons, along with thermal diffusion scattering which occurs at an energy loss equal to approximately 10 meV. Because of these reasons, it is difficult to distinguish between electrons which have lost no energy from those electrons which have lost a small amount of energy. In Fig.5.4(a), the zero-loss peak has a spread of 1 eV around the 0 V mark, which is a fairly narrow energy width. This means that the probability of resolving finer details of the EELS spectrum is much higher, as compared to a zero-loss peak with a broader energy width.

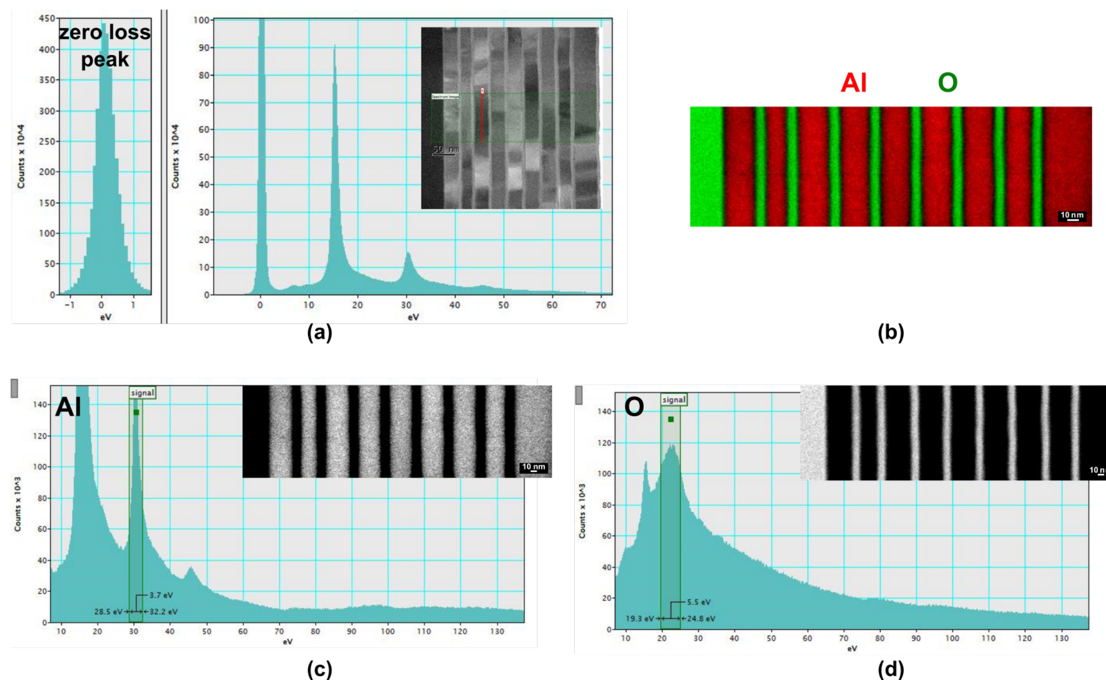


Figure 5.4: (a) Low-loss region of the EELS spectrum with the zero-loss peak and the position of measurement in the sample, (b) composite image with the spatially mapped elements in the TEM image and element specific peaks for (c) aluminum and (d) oxygen with energy filtered TEM images in the respective insets

The features in the energy loss spectrum in the low-loss region result from the excitation of the valence or conduction band electrons. Similar to the high-energy ionization edges, the low-loss peaks in the spectrum are also element-specific and can be used to spatially map the elements present in the sample. Fig.5.4(c) shows the characteristic low-loss peak for the element aluminum obtained from one of the aluminum layers in the sample, at an energy loss equal to 30 eV. Similarly, Fig.5.4(d) shows the characteristic peak for oxygen at an energy loss of 23 eV, which was obtained from one of the AlO_x layers in the sample. From the entire spectrum, a color coded Red-Green image was constructed, as shown in Fig.5.4(b), which represents the alternating Al/AlO_x layers.

The low-loss peak for oxygen is slightly broader in comparison to the peak for aluminum, and the broad energy width of the oxygen peak restricts the energy resolution of the EELS spectrum. Fig.5.5(c) shows a characteristic X-ray spectrum obtained in conjunction with the EELS measurement. When core electrons in the sample material are ejected by beam electrons, the holes created are filled with energetically higher outer-shell electrons, emitting characteristic X-rays in the process. Fig.5.5(a) shows the region of the sample in which a line-scan was measured, with alternating Al/AlO_x multilayers and Fig.5.5(b) shows the spatial position of the line scan vs the X-ray energy detected. The characteristic energy for elemental aluminum can be observed for the entire line scan at an energy of 1.5 keV as aluminum is present in both the aluminum and the AlO_x films. In the AlO_x films, traces of oxygen can be observed at an X-ray energy of 0.5 keV.

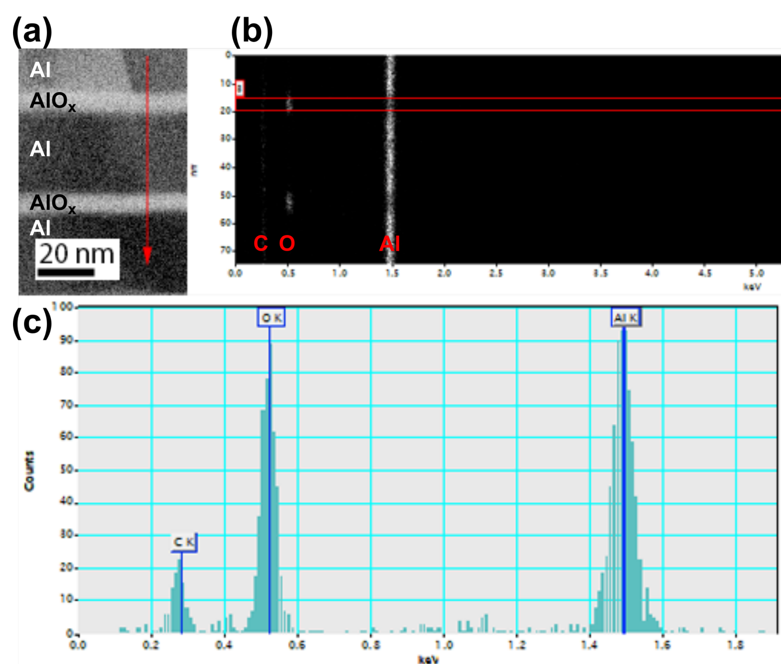


Figure 5.5: X-ray spectrum obtained in conjunction with the EELS measurement. (a) Position of line scan in the sample (b) Spatial position of the line scan vs energy of X-rays detected and (c) characteristic X-ray spectrum showing presence of elemental aluminum, oxygen and carbon in the sample

Apart from detecting the presence of elemental aluminum and oxygen as expected in the X-ray spectrum, traces of elemental carbon are also detected at an energy of approximately 0.3 keV. This suggests the presence of contamination during the EELS measurement which limits the scope of the measurement. The carbon contamination

limits the exposure time during the measurement, and therefore the necessary spectral quality and resolution is below optimum.

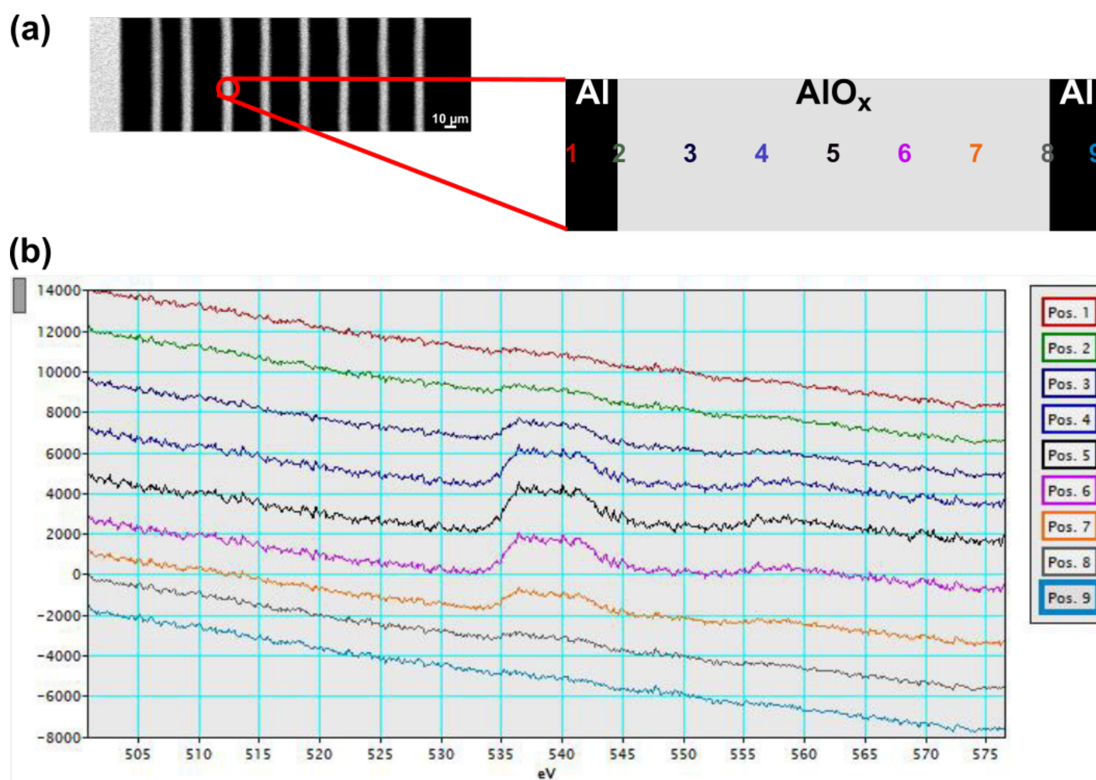


Figure 5.6: Multiple EEL spectra collected in the AlO_x film with (a) the positions of measurement and (b) the individual spectra averaged and smoothened using principle-component analysis

The effect of this contamination can be observed in Fig.5.6 in which individual spectra were collected from different positions located in one of the AlO_x layers. The positions were 1.5 nm apart and the spectra were averaged and smoothened using principle-component analysis. The objective behind collecting these spectra was to resolve the fine structure of the spectral peaks representing oxygen at 532 nm to investigate its electronic state in this part of the sample. The electronic state of oxygen would ideally convey information about the composition of AlO_x. However, as can be seen in the spectra, no finer details can be resolved due to insufficient exposure times and the electronic state of oxygen in the AlO_x film cannot be determined.
Since the electronic state of oxygen could not be resolved further from the EEL spectrum due to insufficient exposure, the oxidation state of aluminum in the AlO_x film was investigated, in an attempt to determine the composition of the plasma-oxidized aluminum oxide film.

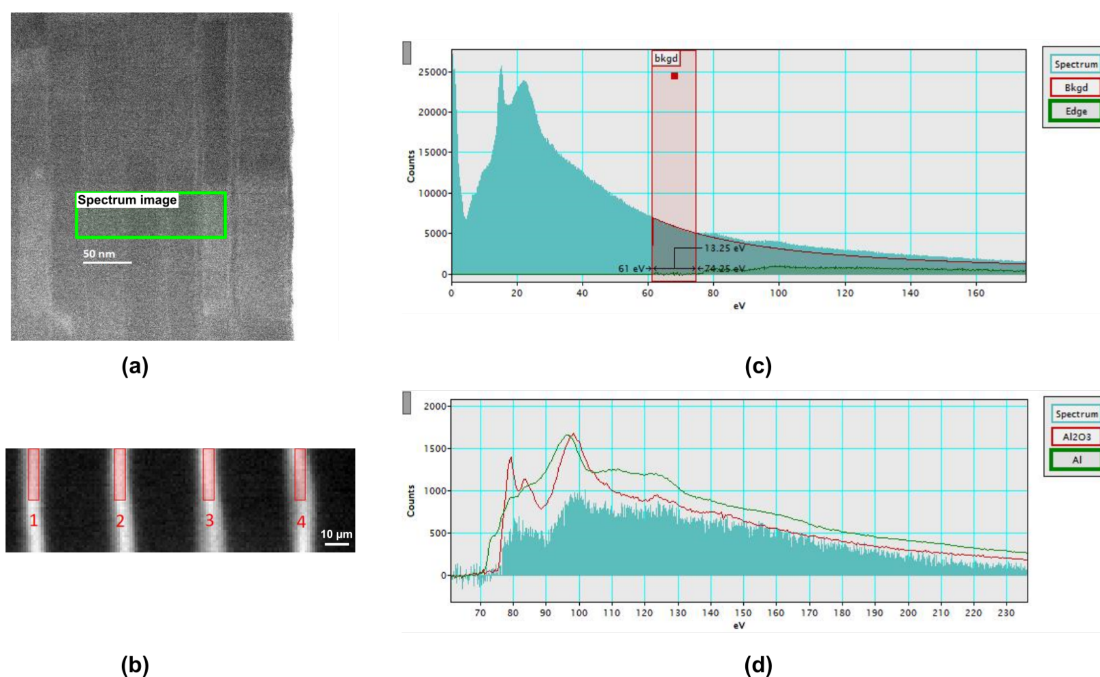


Figure 5.7: (a) Position in the sample and (b) position in the AlO_x layers where the EELS measurement was conducted. (c) EELS spectrum measured and (d) comparison of measured spectrum with reference spectra for elemental aluminum (in green) and Al_2O_3 (in red)

Fig.5.7(a) shows the general region of the sample considered for the EELS measurement, and Fig.5.7(b) shows the 4 positions in the AlO_x films in which the EEL spectra were collected. The spectra were acquired and investigated in the range of aluminum $L_{2,3}$ ionization edges around an energy loss of 90 eV, as shown in Fig.5.7(c).

Although the sample was freshly prepared in the nanomill before mounting in the TEM, the presence of contamination limited the resolution of the spectra severely and the oxidation states of aluminum could not be resolved. However, an attempt was made to qualitatively assess the oxidation state of aluminum by comparing the acquired spectrum with reference spectra. Fig.5.7(d) shows three different spectra, the acquired one (in cyan), a reference spectrum for polycrystalline aluminum (in green), and a reference spectrum for Al_2O_3 (in red). By comparing these three spectra, it can be concluded that the acquired spectra bears more resemblance with the spectrum for Al_2O_3 than with the one for elemental aluminum. Thus, it can be induced that on a qualitative basis, the oxidation state of Al in the AlO_x is much closer to Al_2O_3 than to metallic aluminum.

5.3.3 Outlook

The analytical technique Electron Energy Loss Spectroscopy was employed in an attempt to identify the composition of the plasma-oxidized AlO_x films. Although the technique has a promising potential to analyze the chemical composition of thin films, on a resolution similar to that of TEM, it could not be implemented conclusively for plasma-oxidized AlO_x films. The main hurdle in this measurement and its analysis was the contamination of the sample of interest by carbon. Although extreme care was taken while preparing the TEM sample in a Focused Ion Beam (FIB) apparatus, and the measurement was carried out almost immediately after sample preparation, the level of contamination was significant enough to prevent long exposure times and limit the resolution required to resolve the electron energy loss spectra. One major reason for this is likely the high reactivity of aluminum, which might have been contaminated by hydrocarbons upon exposure to air during sample transfer from the FIB to the TEM. In order to overcome these problems of contamination, possible solutions include sample transfer in vacuum and cryogenic cooling during measurement. However, the implementation of these solutions will require more advanced instrumentation.

5.4 Quantitative measurement by Atom Probe Tomography

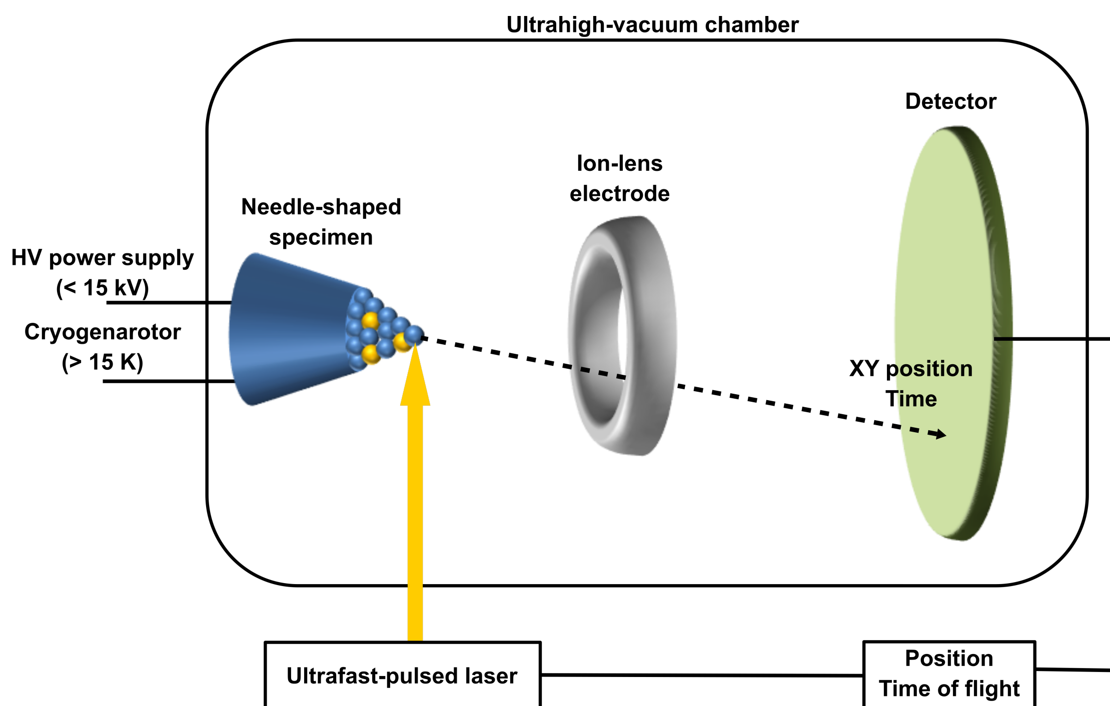


Figure 5.8: Schematic representation of the setup for an atom probe tomography measurement with the main components involved and a representation of the basic measurement principle

Atom Probe Tomography (APT) is a microscopy technique with single-particle detection capability, and extremely effective in investigating several phenomena in materials science [224–227]. A schematic representation of the basic components of the measurement setup and the operating principle is shown in Fig.5.8. Individual atoms are field-evaporated from a specimen through layer-by-layer erosion and collected at a position-sensitive detector. Field evaporation is the process of removing atoms from the surface they are bonded to by overcoming local bonding forces. The original position of the surface atoms at the sample surface is later derived from the impact coordinates of the evaporated species onto the detector using a point-projection law. The chemical identity of the evaporated species is determined by time-of-flight mass spectrometry. After the measurement, a digital reconstruction of the original position and chemical identity of individual atoms is used to analyze various material properties on an atomic scale.
A high electric field is required for the field evaporation of atoms, to overcome the local bonding forces at the surface. This is achieved by applying a very high electric voltage

between the specimen and a counter electrode. The specimen is shaped in the form of a very sharp needle. Typically, the tip radius of the specimen is approximately 50 nm and the high curvature of the tip creates the necessary large electric field. The field-evaporated ions close to the tip surface have a diverging projection during flight which contributes to the extremely high magnification and spatial resolution of the instrument. For the chemical identification of the atoms, time-of-flight mass spectrometry requires a pulsed-field evaporation. This is achieved by either thermal pulsing (applying a pulsed laser) or by field pulsing (applying a pulsed voltage). Additionally, the sample tip is also cooled to cryogenic temperatures (20-150 K) because of which the evaporation process is mostly thermally activated.

Atom probe tomography is an extremely useful technique for the chemical analysis of alloys, studying solid-state reactions [228, 229], characterization of complex nanostructures [230–232] and even studying biomaterials and soft matter [233,234]. This technique has been chosen to study the properties of the plasma-oxidized AlO_x films with the expectation that its atomic resolution and three-dimensional volume analysis will prove useful in overcoming the shortcomings of the other characterization techniques and give insights into the Al/AlO_x layers for organic transistors.

5.4.1 Experimental

As mentioned above, the material of interest must be shaped into a very sharp needle geometry with a quasi-hemispherical end shape, in which a small radius of curvature is required to produce the mandatory high electric field at the surface. As a preliminary attempt, thin aluminum wires were electropolished and oxidized in the oxygen plasma to obtain the particular Al/AlO_x layers in a sharp tip-shaped geometry. However, this method was not successful in forming the desired tip geometry and the AlO_x film was exposed to air, causing contamination. Therefore, a more advanced lift-out technique was employed using a Focused Ion Beam (FIB) apparatus.

The various steps in this process as well as the corresponding SEM images are shown in Fig.5.9. The bulk specimen chosen for the lift-out technique was a multilayer Al/AlO_x structure, similar to the one shown in Fig.5.1(a). The first step in the process is to deposit a rectangular block of platinum on the surface of the bulk specimen to isolate the feature of interest from the sample.

As a next step, two rectangular regions with increasing depth towards the platinum

block are removed by ion milling with the gallium ion beam. By milling these parts away, the region of interest, hereafter referred to as the *lamella*, can be successfully isolated for further processing. Thereafter, the ion beam is used to remove material from two positions in the sample: one on the side of the platinum block, in which the incision is deep enough to reach the material of interest, and the other is positioned at the bottom of the isolated lamella. Essentially, the lamella is then connected to the rest of the bulk specimen only on one side, analogous to a cantilever beam. A micromanipulator is a device used in FIB systems which supports a very sharp needle or a gripping device with a high level of precision of movement. Once the lamella is separated from the specimen from two sides, a micromanipulator is attached to the free end using a temporary welding process by platinum deposition. After the micromanipulator is firmly attached, the lamella is milled from the other end, essentially freeing it from the bulk specimen. Using the micromanipulator movement, the lamella is pulled away from the bulk specimen, lifted out, and transferred to a supporting structure, which in this case, is a tungsten stub. The lamella is attached to the tungsten stub using a small amount of platinum deposition, and a part of the lamella is milled so that the remaining part can be utilized to make more sample tips.[2]

[2] The preparation of the sample tips using the Focused Ion Beam apparatus and expert technical assistance during the atom probe measurement were provided by Helena Solodenko from the University of Stuttgart.

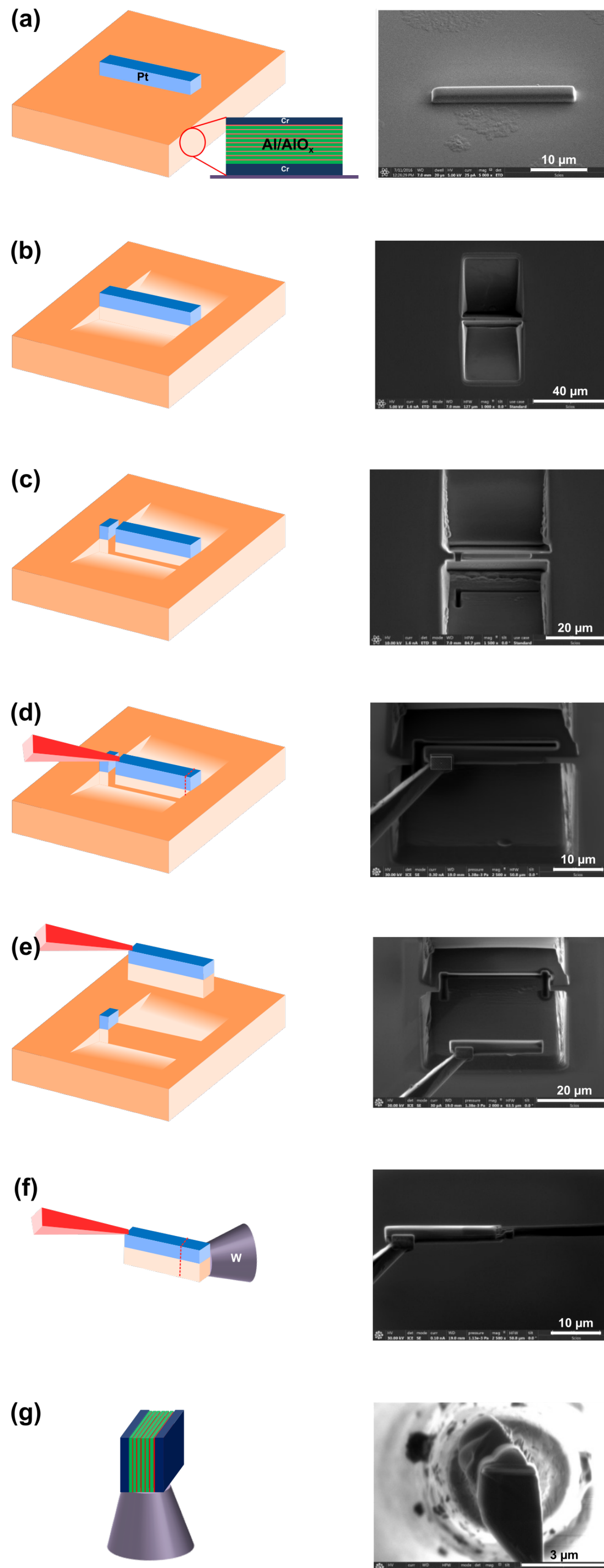


Figure 5.9: Schematic representation and corresponding SEM images of the various stages of fabrication of tips, i.e needle-shaped samples from a bulk specimen for the atom probe measurement using a focused ion beam

The relative orientation of the lamella with respect to the tungsten stub is crucial for the geometry of the final sample tip, which will be measured in the atom probe instrument. In this case, the lamella was attached with its horizontal axis parallel to the tungsten stub. Due to this chosen orientation, the Al/AlO_x multilayers are aligned vertically on the final tip. At this stage, the sample of interest has been attached to the sample tip, but the tip must be further processed to produce a sharp needle-shaped geometry for measurement. This is achieved by milling the tip in concentric circles with reducing radii, as shown in Fig.5.10. At the end of this entire process, the sample is ready in a sharp tip with a radius of approximately 50 nm.

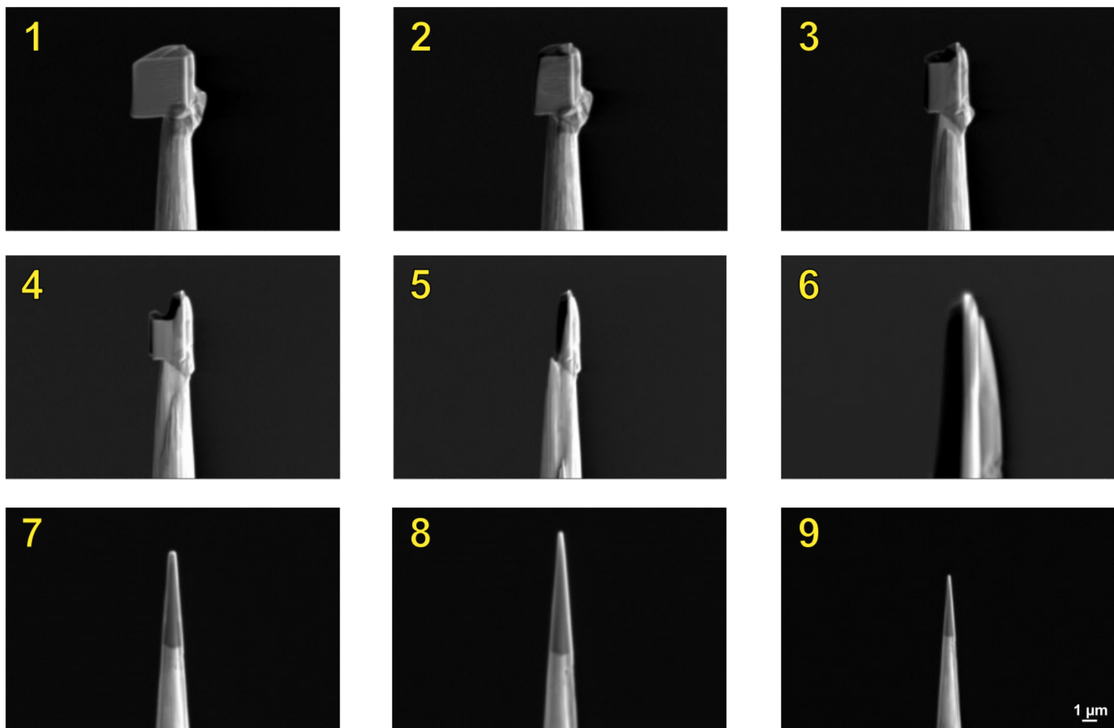


Figure 5.10: Successive stages of ion milling to sharpen the tip radius depicted through SEM images in the focused ion beam with a final tip radius of approximately 50 nm

5.4.2 Results

During the atom probe measurement, atoms at the surface of the tip are field evaporated and collected at the position-sensitive detector where their chemical identity is characterized by time-of-flight mass spectrometry. This data is recorded in the form of a mass spectrum, shown in Fig.5.11. The mass spectrum shows the species identified during the measurement, which in this case are atomic aluminum, chromium, oxygen and fragments of the aluminum oxide, AlO, Al_2O, and Al_2O_2 in different ionization states. It is important to note here that the formation of these ionized species is a result of the breaking of physical bonds in the specimen, and these ionized species are not necessarily representative of stoichiometric compounds. With the chemical identity of the species known, and using information from the position-sensitive detector, a three-dimensional image of the original tip geometry can be reconstructed to analyze the material properties further.

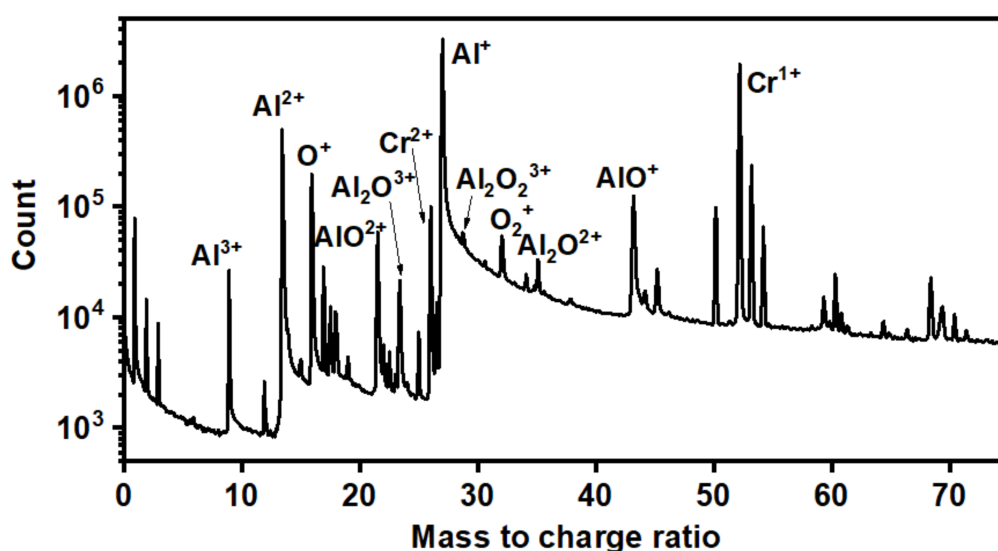


Figure 5.11: Mass spectrum depicting the different ionized fragments identified during the atom probe measurement

Fig.5.12(a) shows **Reconstructed View A**, a cylindrical portion of the sample tip. This reconstructed view corresponds to a cross-section of two aluminum layers and one AlO_x layer in between, with its estimated position in the bulk specimen depicted in Fig.5.12(b). A cylindrical profile along this reconstructed view is chosen to analyze the composition along this cylinder, shown in Fig.5.12(d).

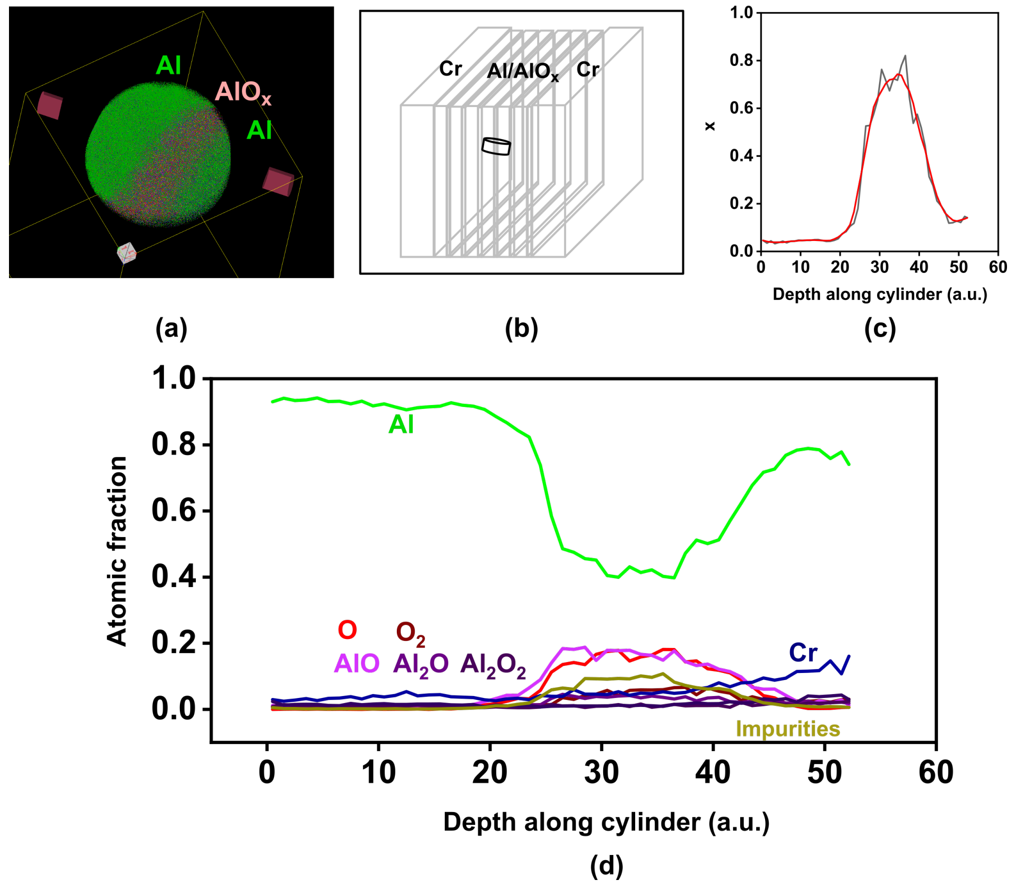


Figure 5.12: Reconstructed View A (a) Cylindrical reconstructed view depicting $Al/AlO_x/Al$ layers (b) Estimated location of the cylinder in the bulk specimen (c) Numerical value of x in AlO_x along the cylindrical reconstruction as derived from (d) the composition profile as extracted from the reconstructed view

It can be seen from the reconstructed view as well as the composition profile that the oxide layer is situated between two aluminum layers. In the aluminum oxide region of the reconstructed view, fragments of Al, O and AlO, Al_2O, Al_2O_2 can be observed. Analyzing the respective contributions of aluminum and oxygen, the value of x, in AlO_x can be plotted along the composition profile, shown in Fig.5.12(c). As expected, in the aluminum portion of the reconstructed view, x is almost equal to 0, as in the aluminum layer, the content of oxygen is negligible. In the AlO_x layer, the value of x is calculated to equal approximately 0.8, i.e. there are 8 parts of oxygen to every 10 parts of aluminum in the AlO_x film.

Fig.5.13 shows a second **Reconstructed View B** from the same measurement on the same tip specimen. This particular reconstruction, which shows three layers, corresponds to the AlO_x layer which was fabricated last, below the top chromium layer in the

multilayer bulk specimen, with its location in the bulk specimen shown in Fig.5.13(b).

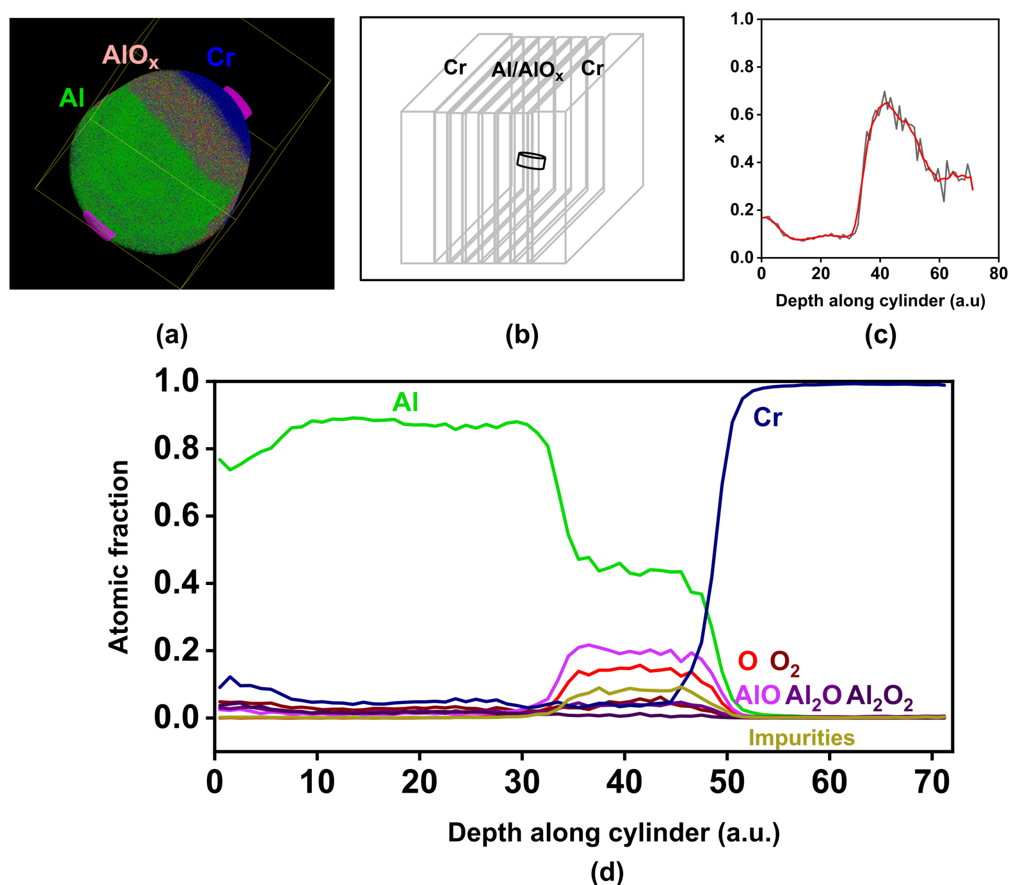


Figure 5.13: Reconstructed View B (a) Cylindrical reconstructed view depicting $Al/AlO_x/Cr$ layers (b) Estimated location of the cylinder in the bulk specimen (c) Numerical value of x in AlO_x along the cylindrical reconstruction as derived from (d) the composition profile as extracted from the reconstructed view

The advantage of this particular reconstruction is that because of the asymmetrical nature of the multilayer structure, it is evident that the AlO_x layer measured was formed by oxidizing the aluminum layer in the reconstructed view. Fig.5.13(d) shows the relative compositions of the fragments measured along a cylindrical profile in the reconstructed view. The three layers identified are aluminum, aluminum oxide and chromium, as evident by the almost unity atomic fractions of aluminum and chromium respectively. Similar to the first reconstructed view, the relative contribution of oxygen to aluminum was analyzed to determine the value of x along the composition profile. In this reconstructed view, the value of x is similar, approximately 0.65, i.e 6.5 parts of oxygen for every 10 parts of aluminum. In both reconstructions, although it was possible to reconstruct the aluminum and chromium layers with greater accuracy, the composition of

AlO_x does not correlate with the expected value of 1.5, and seems much lower than that. Particularly, the oxygen content in both cases is significantly lower than the expected stoichiometric value, i.e. 15 parts of oxygen to 10 parts of aluminum, and the detected composition of the AlO_x films suggests a more metallic character.

5.4.3 Challenges

There were several challenges faced during the atom probe measurement which compromise the reliability of the results obtained. There were multiple instances of the sample tip breaking during the measurement when transitioning from the aluminum layer to the aluminum oxide layer. This is possibly because of different measurement conditions required for the two different materials. It was not possible to adjust the combination of cryogenic cooling and local spatial heating (caused by the pulsed laser) for the aluminum and aluminum oxide films simultaneously. Moreover, due to the small thickness of the AlO_x film, the sample tip did not have sufficient buffer time to adjust the measurement settings, and brittle fracture of the oxide layer caused the tip to break. In the rare occasion where the temperature of the tip was kept relatively high to prevent the brittle fracture of the tip, the measurement detailed above has been carried out. As can be seen in the mass spectrum in Fig.5.11, the signal-to-noise ratio is severely compromised, and the mass peak for aluminum has a strong tailing feature. Secondly, there is a strong suspicion that a majority of the oxygen in the AlO_x film might have escaped the system as O_2 gas, without being ionized, and hence would not feature in the mass spectrum. This could be one of the primary reasons why the measured composition value appears to be oxygen-deficient and does not reflect an accurate composition for the plasma-oxidized AlO_x film. A better control of the laser power through a systematic variation and the applied voltage is required to ensure that oxygen content in the AlO_x film is accurately measured.

5.5 Summary and Outlook

Ultrathin plasma-oxidized films of aluminum oxide are excellent gate dielectric films in hybrid gate dielectrics for organic thin-film transistors. However, due to the nature of the plasma process, the film properties of the AlO_x films need further characterization

for better control of the film properties. The most important properties from the gate dielectric perspective are the film thickness and the film composition, and an effort has been made to examine the properties of the AlO_x films. For a plasma-process-parameter combination of 200 W and 30 s, the thickness of the AlO_x films was measured to be 6.5 nm using transmission electron microscopy. The thickness of the films was found to be relatively reproducible and consistent and was independent of the thickness of the underlying aluminum films.

An attempt was made to measure the composition of the AlO_x films by two different characterization techniques: Electron Energy Loss Spectroscopy (EELS) (in conjunction with TEM) and Atom Probe Tomography. Through EELS, the respective elements aluminum and oxygen were spatially mapped to reveal successive Al/AlO_x films as fabricated. By comparing the oxidation states of aluminum in the AlO_x film, it was qualitatively concluded that the composition of the plasma-oxidized AlO_x films is closer to Al_2O_3. The quantitative measurement of the AlO_x was unfortunately not successful, due to a significant amount of carbon contamination which limited the exposure time and hence the resolution of the EEL spectra.

Through atom probe tomography, the different Al/AlO_x layers were measured with atomic resolution and reconstructed on an atomic scale. Although this technique shows great potential for determining the composition of the AlO_x films, further tuning of the measurement conditions would be required to find a more accurate measurement of the composition. A calibration measurement with standardized sapphire samples (composition of Al_2O_3) and a variation of the laser power to measure its effect on the amount of gaseous oxygen ionized will improve the ability of this technique to accurately measure the composition of the AlO_x films.

A successful measurement of the composition of the plasma-oxidized AlO_x films would enable a better understanding of the properties of the AlO_x films as gate dielectrics and also opportunities for improving the electrical properties of the organic transistors further by improving the material properties of the AlO_x gate dielectric films.

Chapter 6

Influence of self-assembled monolayer thickness in hybrid gate dielectrics: Alkyl and fluoroalkyl phosphonic acids

The second component of the hybrid gate dielectrics investigated in this thesis is a molecular self-assembled monolayer (SAM) formed by phosphonic acid molecules, assembled from solution on the plasma-grown aluminum oxide (AlO_x) surface in organic thin-film transistors (TFTs). The role of the SAM in the hybrid gate dielectric as well as in the overall functioning of organic TFTs has been well established in numerous previous studies and summarized in Chapter 3. The primary function of SAMs is to enable low-voltage operation of organic TFTs by reducing the gate-dielectric thickness, while simultaneously maintaining a low leakage current density [35]. In addition, the possibility of employing different SAMs to modify the threshold voltage [157, 235, 236], surface properties, organic-semiconductor morphology and overall organic-TFT characteristics has also been widely explored.

The gate dielectric-semiconductor interface is extremely important for the electrical characteristics of the organic TFT, since the conducting channel is situated in close proximity to this interface. A well-established strategy to obtain a suitable organic-semiconductor morphology in bottom-gate transistor configurations, is to modify the

surface of the gate dielectric onto which the organic semiconductor is deposited. Several different types of SAMs, as well as polymer gate dielectrics [237], have been used for this purpose. However, a *suitable* morphology of the organic semiconductor is challenging to define narrowly and may depend on the semiconductor/gate dielectric combination in question. In general, a suitable semiconductor morphology promotes a larger area of percolation for the charge carriers and a lower density of charge-carrier traps. Often, the semiconductor morphology is characterized by the grain size of a polycrystalline organic-semiconductor layer at its complete thickness of several monolayers. A straightforward understanding of the semiconductor morphology prefers a larger grain size so that a lower density of grain boundaries implies a lower density of charge-carrier traps. This correlation between the grain size of the semiconductor layer and the electrical performance of the organic TFT has been established in several reports [118]. Nevertheless, this does not completely explain the influence of the semiconductor morphology as there are also several contradictory reports, in which a larger grain size has resulted in a decreased effective charge-carrier mobility [169]. To gain a better understanding of the semiconductor morphology, the growth mode of the semiconductor must also be considered in addition to the grain size. The growth mode of the organic semiconductor influences the percolation path for the charge carriers, especially in the first few layers close to the gate dielectric, i.e. in the conducting channel and gives a deeper insight into the influence of the organic-semiconductor morphology on the electrical characteristics of organic TFTs.

An important parameter regarding the surface properties of the gate dielectric, especially in bottom-gate organic TFTs, is the surface energy. Chapter 4 discussed the importance of the surface roughness and the manner in which the gate oxide and the plasma process to fabricate the gate oxide, are instrumental in tuning the surface roughness of the gate dielectric. It was also seen in Chapter 4 that the plasma process has no effect on the surface energy of the gate dielectric, and the surface energy of the bare AlO_x surface was changed only upon formation of the SAM. Several previous reports have investigated the effect of changing the surface energy of the gate dielectric on the wettability of the gate-dielectric surface and thereby the growth mode and the morphology of the semiconductor layer, and subsequently the performance of the organic TFT [118, 238]. Among SAMs, different strategies have been used to modify the surface energy, such as employing different functional groups [155, 175], inserting polar atoms in the alkyl chain [239], using hybrid multilayers [240, 241], etc. With the choice of AlO_x as the

inorganic gate oxide component of the hybrid gate dielectric, the optimum choice for the SAM is a molecule with a phosphonic acid head group to assemble on the AlO_x surface [35, 242].

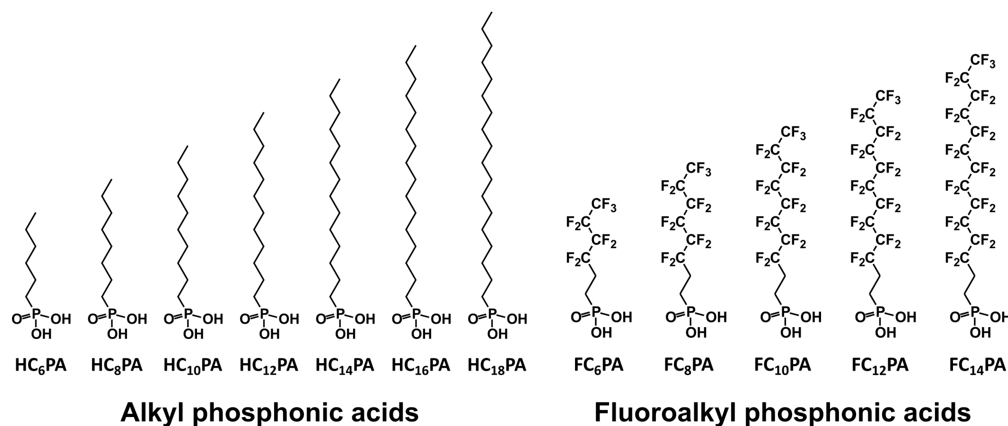


Figure 6.1: Alkyl and fluoroalkyl phosphonic acid molecules of different chain lengths selected to form SAMs in hybrid gate dielectrics

This chapter explores two different types of phosphonic acid molecules, viz. alkyl phosphonic acids (**H**C_xPA) and fluoroalkyl phosphonic acids (**F**C_xPA), where x is the number of carbon atoms in the aliphatic chain of the phosphonic acid molecule. The chemical structures of the phosphonic acid molecules of different chain lengths are given in Fig.6.1. By employing molecules with a different number of carbon atoms in the aliphatic backbone of the molecule, the thickness of the SAM is systematically changed and the influence of the changing thickness of the gate dielectric on the electrical and surface properties of hybrid gate dielectrics in organic TFTs is investigated. Furthermore, the nucleation and growth of the organic semiconductor DNTT on four different surfaces was recorded to observe changes in the growth mode of the semiconductor. Along with the growth mode, the semiconductor morphology for two different semiconductors (DNTT and DPh-BTBT) of different thicknesses on different SAMs has also been investigated. This chapter aims to understand the effect of the alkyl chain length of phosphonic acid molecules on the formation and properties of the SAM, as reflected in its surface properties, and a resulting influence on the growth and morphology of organic semiconductors and the electrical properties of organic TFTs.

6.1 Background

The influence of the chain length of phosphonic acid molecules used in SAMs for hybrid gate dielectrics towards low-voltage organic TFTs has been explored in several other literature accounts, as summarized in Table 6.1. Acton and co-workers used alkyl phosphonic acid molecules with chain lengths from six to eighteen carbon atoms in combination with a gate oxide consisting of SiO_2 with a thickness of 2.5 nm and a high-k oxide HfO_2 with a thickness of 8 nm [120]. By employing ATR-FTIR (Attenuated Total Reflectance-Fourier Transform Infrared Spectroscopy) and studying the morphology of the organic semiconductor pentacene deposited onto the different SAM surfaces, they concluded that the ordering in the phosphonic acid SAMs increases steadily with an increase in chain length. The largest grain size for pentacene was observed for the medium-chain-length molecules from HC_8PA to $HC_{14}PA$, and was correlated to the largest charge-carrier mobilities. Jedaa and co-workers investigated alkyl phosphonic acids in combination with plasma-grown AlO_x oxide films, fabricated with two different plasma processes, to study the effect of the underlying AlO_x film on the resulting SAM formation [191]. They concluded that for longer chain lengths of the phosphonic acid molecule, the SAM compensates for a lower quality of the AlO_x thin film, and that the electrical properties of the organic TFTs at higher electrical fields are dominated by the SAM and not by the oxide. Fukuda and co-workers also investigated the different alkyl phosphonic acids in combination with a plasma-grown AlO_x thin film, and performed bias-stress measurements along with studying the semiconductor morphology of pentacene deposited onto the different SAMs [154]. The highest charge-carrier mobility was found for the TFT with the $HC_{14}PA$ SAM, and was attributed to its low surface roughness (as determined by X-ray reflectivity measurements), resulting in the largest grain size of pentacene on the $HC_{14}PA$ SAM. Hill and co-workers used SiO_2 with a thickness of 100 nm as the gate oxide, which means that the TFTs had to be operated with high voltages, but characterized the SAMs using water contact-angle measurements and analyzed the subthreshold performance of the organic TFTs to study the behavior of different SAMs [243]. This study found an optimum organic-TFT performance for phosphonic acid molecules with eight and ten carbon atoms with a minimum trap density at the gate dielectric and thereby an improved subthreshold swing and threshold voltage. Hannah and co-workers used a novel vapor-deposition technique to form the phosphonic acid SAMs, instead of the usual solution-processing method, and also characterized the

Reference	Molecules investigated (HC_xPA)	Substrate	Gate oxide	Organic Semiconductor	Mobility optimum
[120] Acton et al.	x = 6, 8, 10, 12, 14, 16, 18	Silicon	2.5 nm SiO_2 + 8 nm HfO_2 (sol-gel)	Pentacene	HC_8PA-$HC_{14}PA$
[191] Jedaa et al.	x = 2, 6, 10, 1, 18	Glass	AlO_x, mild air and oxygen plasma	Pentacene	$HC_{14}PA$
[154] Fukuda et al.	x = 6, 10, 14, 16, 18	Silicon	AlO_x, oxygen plasma	Pentacene	$HC_{14}PA$
[243] Hill et al.	x = 6, 8, 10, 12, 14, 16, 18	Silicon	100 nm SiO_2	Pentacene	HC_8PA - $HC_{10}PA$
[244] Hannah et al.	x = 8, 10, 12, 14, 16, 18 (vacuum-processed)	Glass	AlO_x, UV/ ozone	DNTT	$HC_{18}PA$
This work	HC_xPA, x = 6, 8, 10, 12, 14, 16, 18	flexible PEN	AlO_x, oxygen plasma	DNTT	$HC_{14}PA$
This work	FC_yPA, y = 6, 8, 10, 12, 14	flexible PEN	AlO_x, oxygen plasma	DPh-BTBT	$FC_{10}PA$

Table 6.1: Summary of literature reports investigating the influence of chain length in phosphonic acid molecules in hybrid gate dielectrics

SAMs formed using FTIR measurements and DFT (Density Functional Theory) calculations to analyze the packing density and ordering within the monolayers [244]. An increased molecular order within the SAM was observed with an increase in the chain length of the molecule, thereby improving the performance of the organic TFTs. Most of these studies found that an optimum charge-carrier mobility was obtained by using a medium chain-length phosphonic acid SAM (between ten and fourteen carbon atoms) and attributed it to the medium chain-length SAMs forming the most densely packed and well-ordered monolayers. This was then verified by several characterization techniques, either by spectroscopic measurements of the SAMs, or by observing the resulting organic-semiconductor morphology on these SAM surfaces.

This chapter explores the influence of the chain length of two different phosphonic acid molecules, in combination with two high performance organic semiconductors, DNTT and DPh-BTBT, which are more air-stable than pentacene. Organic TFTs have been

fabricated on flexible PEN (polyethylene naphthalate) foils, in comparison to the rigid glass or silicon wafer substrates used in previous studies. For the first component of the hybrid gate dielectric, a consistent combination of 200 W and 30 s was selected to fabricate the plasma-grown AlO_x films with a thickness of approximately 6.5 nm. The choice of the particular phosphonic acid molecule in combination with the particular organic semiconductor is explained in Appendix D. The fluoroalkyl phosphonic acid SAMs were used in combination with the organic semiconductor DPh-BTBT because this combination yielded a turn-on voltage much closer to 0 V, which is beneficial from a technological point of view. Seven different alkyl phosphonic acid molecules (from six to eighteen carbon atoms) and five different fluoroalkyl phosphonic acid molecules (six to fourteen carbon atoms) were used to form SAMs. The fluoroalkyl phosphonic acid molecules were chosen in which the entire alkyl chain (except two carbon atoms) has been fluorinated. Partially fluorinated phosphonic acids with longer chains (e.g. eighteen carbon atoms) were not included, since these are not commercially available. The electrical properties of the organic TFTs with the different SAMs and the morphology of the semiconductors on the respective SAMs is investigated, and correlated to the surface properties of the different SAMs.

6.2 Dielectric properties of hybrid gate dielectrics with self-assembled monolayers

It has already been established in Chapter 4 that the overall gate-dielectric capacitance of the hybrid dielectric is dominated by the capacitance of the SAM due to the influence of its low dielectric constant. Any variation in the gate-dielectric capacitance of oxide dielectrics obtained by modifying the aluminum oxide layer is overpowered after introducing the SAM and results in an almost constant capacitance of the hybrid gate dielectrics. This means that for hybrid gate dielectrics with the same molecule forming the SAM, very little variation in the gate-dielectric capacitance is possible due to the large contribution of the SAM to the overall gate-dielectric capacitance. Hence, the possibility of using molecules with different chain lengths to form SAMs of different thicknesses has been explored to modify the overall gate-dielectric capacitance of hybrid gate dielectrics.

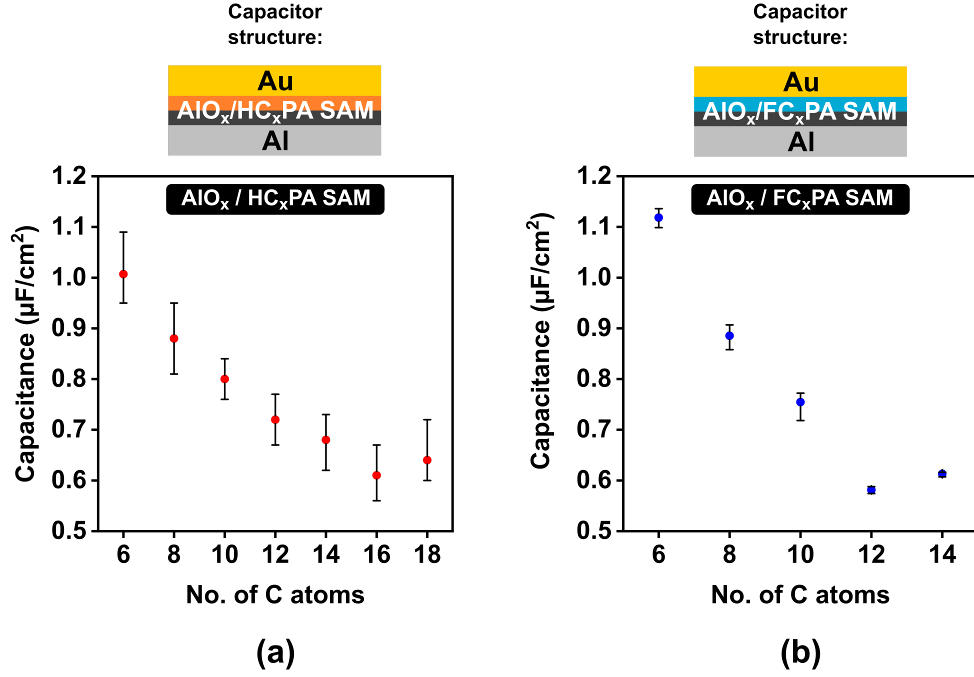


Figure 6.2: Measured gate-dielectric capacitance of (a) AlO_x/HC_xPA SAM and (b)AlO_x/FC_xPA SAM hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

Fig.6.2 shows the variation of the measured gate-dielectric capacitance of metal-insulator-metal capacitors with the different chain-length phosphonic acid molecules, with Fig.6.2(a) showing the variation for alkyl phosphonic acid molecules from six carbon atoms to eighteen carbon atoms in the alkyl chain and Fig.6.2(b) for fluoroalkyl phosphonic acid molecules with six to fourteen carbon atoms in the aliphatic backbone. For the alkyl phosphonic acid SAMs, the gate-dielectric capacitance of hybrid AlO_x/SAM gate dielectrics can be varied between 0.6 and 1 $\mu F/cm^2$ and for the fluoroalkyl phosphonic acids, the gate-dielectric capacitance varies between 0.6 and 1.1 $\mu F/cm^2$. It can be observed that a longer alkyl chain in both phosphonic acid molecules, which signifies an increase in the thickness of the SAM (t_{SAM}), results in a steady decrease in the gate-dielectric capacitance C_{diel}. This is in accordance with the theoretical equation:

$$\frac{1}{C_{diel}} = \frac{t_{ox}}{\varepsilon_0 \varepsilon_{ox}} + \frac{t_{SAM}}{\varepsilon_0 \varepsilon_{SAM}} \tag{6.1}$$

where t_{ox} is the thickness of the AlO_x layer, ε_0 is the absolute permittivity, ε_{ox} is the permittivity of AlO_x, and ε_{SAM} is the relative permittivity of the SAM.

A similar effect of the chain length of the phosphonic acid molecules on the gate-dielectric capacitance was also observed by Acton et al. [120] and Hannah et al. [244], and the

gate-dielectric capacitance values were used to calculate the thickness of the SAMs for the different chain-length phosphonic acid molecules. The thickness of the SAM for alkyl phosphonic acid molecules from HC_6PA to $HC_{18}PA$ was calculated to be between 0.8 nm and 2.4 nm. However, it must be noted that the thickness of the SAM does not correspond to the chain length of the molecule as the phosphonic acid molecules usually assemble with a tilt angle of 20°-30°with respect to the gate-dielectric surface. It can also be observed in Fig.6.2 that for the longest chain-length molecules, the gate-dielectric capacitance does not decrease monotonically, i.e. the gate-dielectric capacitance corresponding to SAMs with $HC_{16}PA$ and $HC_{18}PA$ is approximately 0.6 $\mu F/cm^2$ and similarly for the fluoroalkyl $FC_{12}PA$ and $FC_{14}PA$ molecules. This indicates the possibility that even with an increase in the chain length of the molecule, the thickness of the SAM does not change proportionally, especially for the longer chain length molecules. This aspect will be revisited again while discussing the morphology and ordering of the SAMs in Section 6.4.2.

Thus, by modifying the chain length of the phosphonic acid molecules, the capacitance of the hybrid gate dielectric can be varied between 0.6 and 1 $\mu F/cm^2$, which was not possible by varying the plasma parameters of the AlO_x fabrication process. In general, a large gate-dielectric capacitance is preferred for low operating voltages in the organic TFT, thus making smaller chain length phosphonic acid molecules more desirable. However, the effect of the different molecules on the electrical characteristics of organic TFTs and the surface properties of the gate dielectric must be considered before selecting an optimum range of chain lengths of the phosphonic acid molecules.

6.3 Electrical properties of organic TFTs with self-assembled monolayer hybrid gate dielectrics

The importance of the SAM in hybrid gate dielectrics in organic TFTs is the central theme of this chapter. Hence, the different phosphonic acid molecules were employed in hybrid gate dielectrics in organic TFTs to observe the influence of the chain length of the molecules on TFT performance. Throughout this section, the effect of AlO_x/HC_xPA SAM hybrid gate dielectrics on DNTT TFTs and AlO_x/FC_xPA SAM hybrid gate dielectrics on DPh-BTBT TFTs will be considered in parallel.

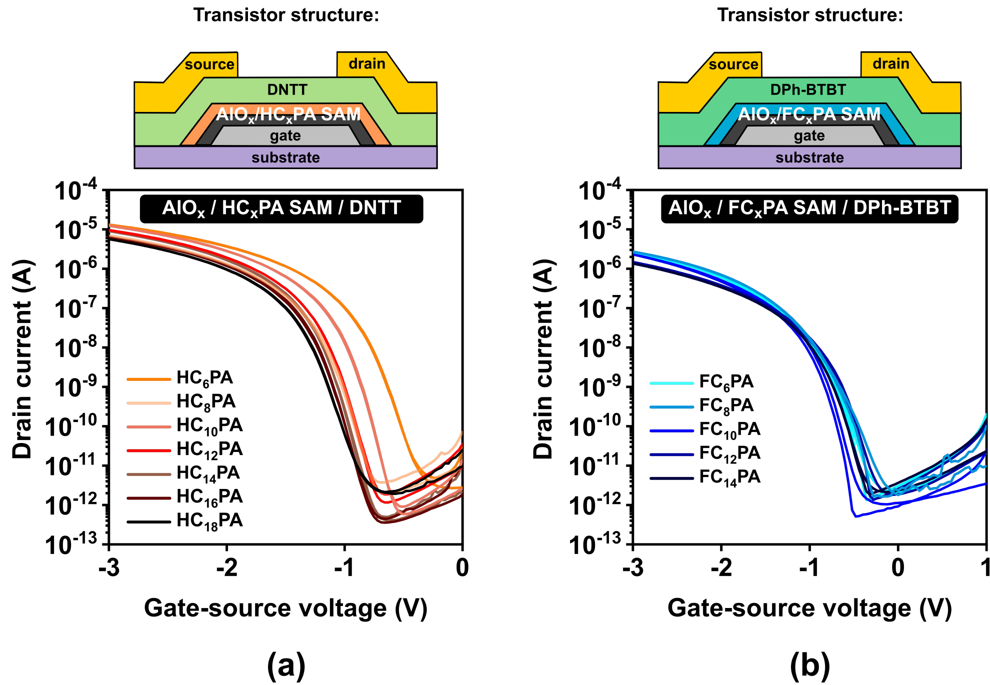


Figure 6.3: Transfer characteristics of (a) DNTT TFTs with AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics for all the different phosphonic acid molecules forming the SAMs. The TFTs have a channel length of 20 μm and a channel width of 100 μm

The measured transfer characteristics of organic TFTs (the drain current I_D as a function of the gate-source voltage V_{GS}) with the phosphonic acid molecules of different chain lengths superimposed can be seen in Fig.6.3(a) for DNTT TFTs with alkyl phosphonic acid SAMs and in Fig.6.3(b) for DPh-BTBT TFTs with fluoroalkyl phosphonic acid SAMs. The different phosphonic acid molecules considered are all suitable to form hybrid gate dielectrics in functional organic TFTs. Among the alkyl phosphonic acid SAMs, there is a slight variation for the shorter chain length molecules (HC_6PA and $HC_{10}PA$), but mostly all molecules lead to similar transfer characteristics of the TFTs with the alkyl and fluoroalkyl phosphonic acid SAMs. To observe a more detailed effect of the chain length, individual TFT-performance characteristics obtained from the transfer curves as a function of the chain length of the phosphonic acid molecules are compared below.

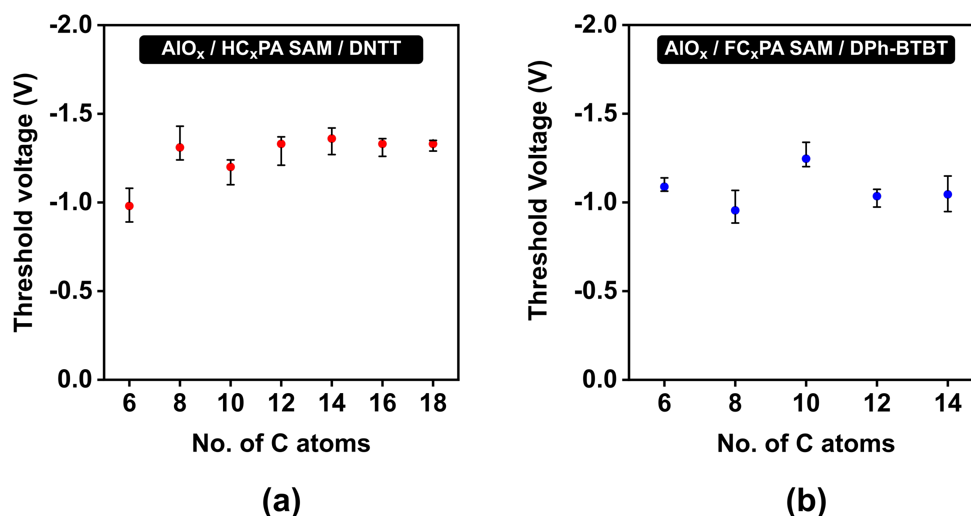


Figure 6.4: Threshold voltage of (a) DNTT TFTs with AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

The threshold voltage of organic TFTs is defined as the minimum gate-source voltage at which charge carriers are accumulated in the conducting channel and gives an insight into the density of charge-carrier traps in the gate dielectric and at the dielectric-semiconductor interface. The threshold voltage is plotted as a function of the chain length of the respective phosphonic acid SAMs in the DNTT and DPh-BTBT TFTs in Fig.6.4. For the DNTT TFTs with the alkyl phosphonic acid SAMs, the threshold voltage varies between approximately -1 V and -1.5 V, while for the DPh-BTBT TFTs with the fluoroalkyl phosphonic acid SAMs, the threshold voltage is more or less constant at approximately -1 V. Although two different phosphonic acid molecules were used for the SAMs, the threshold voltage for both types of TFTs is almost consistent, because the threshold voltage range is unique for each semiconductor-gate dielectric combination. The influence of the different functional groups on the threshold-voltage shift has been reported previously [155, 157, 175] and is also detailed in Appendix D by employing different SAMs with the same semiconductor, i.e. DNTT to fabricate organic TFTs.

A slight variation in the threshold voltage depending on the chain length can be observed for the alkyl phosphonic acid molecules, with an increase in the chain length leading to more negative threshold voltages (higher in magnitude). However, this effect cannot be observed for the fluoroalkyl phosphonic acid molecules, which suggests that the chain length of the molecules has little to no effect on the density of defects and charge-carrier traps in the fluoroalkyl phosphonic acid SAMs.

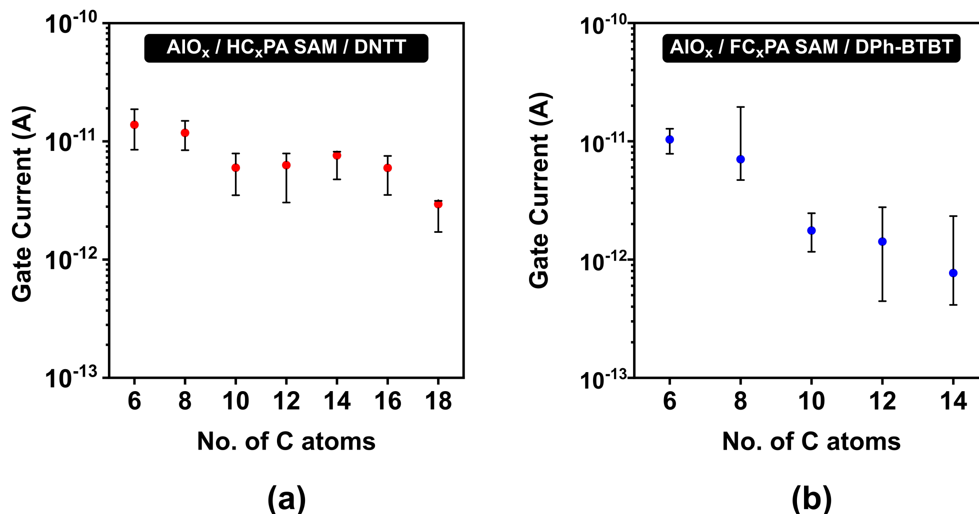


Figure 6.5: Gate-leakage current of (a) DNTT TFTs with hybrid AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

The gate current is the leakage current through the gate dielectric in an organic TFT, and the primary advantage of hybrid gate dielectrics is to maintain a low leakage current due to the SAM. The influence of the chain length of the phosphonic acid molecules on the gate current in the respective TFTs can be seen in Fig.6.5. For both the alkyl and the fluoroalkyl phosphonic acids, the gate current varies between approximately 10^{-11} A and 10^{-12} A, with a steady decrease in the gate current with an increase in the chain length of the phosphonic acid molecule. This relationship is consistent with the typical correlation between the gate-dielectric thickness and the gate current in a transistor, i.e. a larger gate-dielectric thickness leads to a smaller gate leakage current. As smaller leakage currents are desirable for better transistor characteristics, the longer chain length molecules are more suitable for SAMs in hybrid gate dielectrics towards low-power organic TFTs.

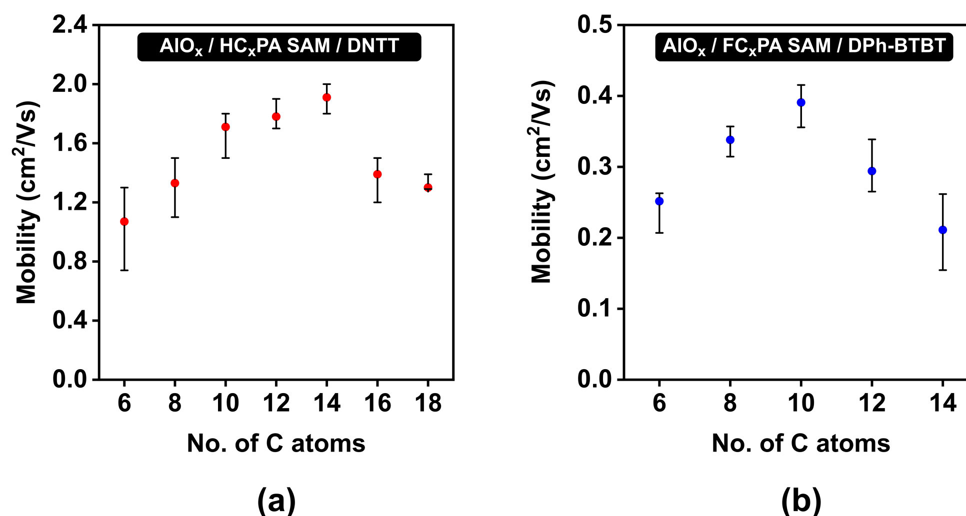


Figure 6.6: Charge-carrier mobility of (a) DNTT TFTs with AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

The charge-carrier mobility of an organic TFT is one of the most important TFT characteristics and is plotted as a function of the chain length of the respective phosphonic acid SAMs in Fig.6.6. It can be observed that the range of charge-carrier mobilities of the DNTT TFTs is much higher (0.8 cm^2/Vs - 2 cm^2/Vs) than those of the DPh-BTBT TFTs (0.2 cm^2/Vs - 0.4 cm^2/Vs), most likely due to a higher intrinsic mobility for the semiconductor DNTT. Nevertheless, a trend in the charge-carrier mobility with the chain length of the phosphonic acid molecule can be seen for both cases. As the chain length of the phosphonic acid molecule initially increases, the charge-carrier mobility also increases. Considering the range of molecules studied in this case, the carrier mobility reaches a maximum for the medium chain length molecules: 2 cm^2/Vs for the DNTT TFTs with $HC_{12}PA$ and $HC_{14}PA$ SAMs and 0.4 cm^2/Vs for the DPh-BTBT TFT with the $FC_{10}PA$ SAM. Thereafter, as the chain length of the phosphonic acid molecule increases, the carrier mobility decreases for both sets of TFTs. To explain the above trend seen for the charge-carrier mobility, the growth and morphology of the respective organic semiconductors will be considered along with the surface properties of the SAM in the following sections.

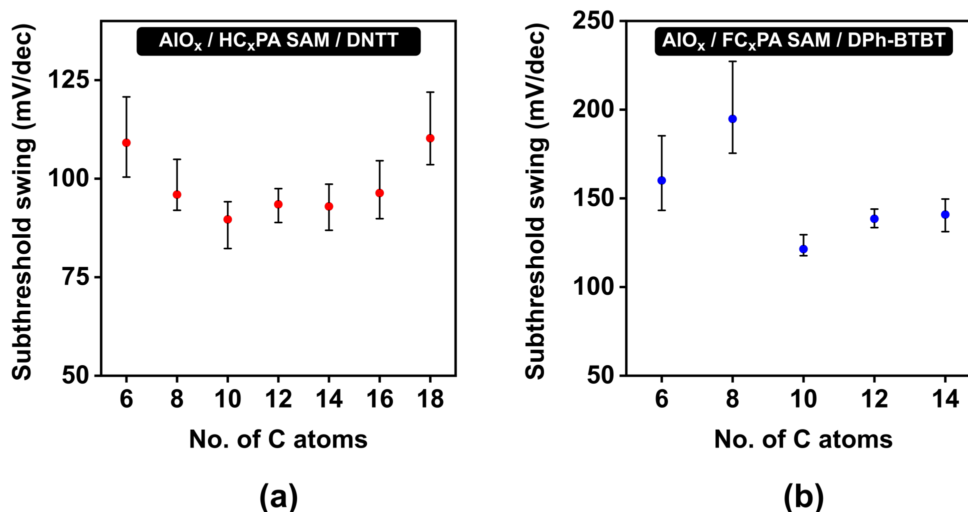


Figure 6.7: Subthreshold swing of (a) DNTT TFTs with AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

The subthreshold swing, as defined in Chapter 2, characterizes the subthreshold region of TFT operation and is largely defined by the density of electrically active impurities at the gate dielectric-semiconductor interface. Fig.6.7 shows the variation of the subthreshold swing as a function of the chain length of the respective phosphonic acid molecules in DNTT and DPh-BTBT TFTs. A smaller subthreshold swing indicates a smaller density of trap states in the gate dielectric as well as at the dielectric-semiconductor interface. A smaller subthreshold swing for the alkyl phosphonic acid SAMs can be observed for the medium-chain length $HC_{10}PA$-$HC_{14}PA$ molecules (89 mV/dec - 92 mV/dec). Similarly, the smallest subthreshold swing for the fluoroalkyl phosphonic acid SAMs is obtained for the medium chain length $FC_{10}PA$ molecule (125 mV/dec).

According to Hill et al., the chain length of the molecule forming the SAM influences the density of trap states at the dielectric-semiconductor interface [243]. If the chain length is too short, an interaction with the underlying gate oxide may lead to deep electron trap states. On the other hand, long chain length molecules produce surface disorder, leading to shallow trap states at the surface. In both cases, the increased density of trap states leads to a higher subthreshold swing. This is a likely explanation for medium-chain-length phosphonic acid molecules forming SAMs with a lower subthreshold swing, as observed in Fig.6.7.

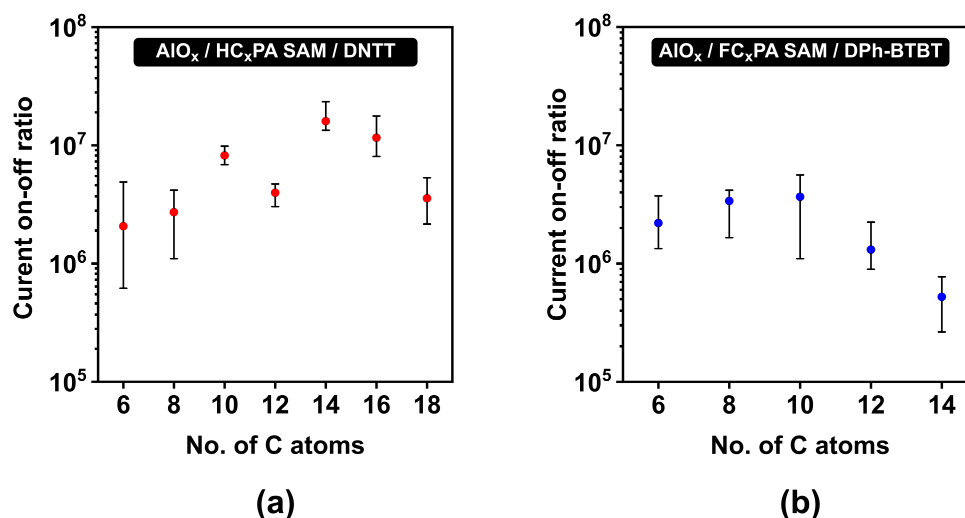


Figure 6.8: Current on-off ratio of (a) DNTT TFTs with AlO_x/HC_xPA hybrid gate dielectrics and (b) DPh-BTBT TFTs with AlO_x/FC_xPA hybrid gate dielectrics as a function of the phosphonic acid molecule chain length (number of carbon atoms)

The current on-off ratio is defined as the ratio between the drain current (I_D) in the on-state of transistor operation (measured at a gate-source voltage of -3 V) and the drain current in the off-state (measured at a gate-source voltage of 0 V) and is plotted in Fig.6.8 as a function of the respective phosphonic acid molecule chain length. With the exception of the $HC_{12}PA$ SAM for the alkyl phosphonic acid molecules, the general trend of the current on-off ratio with the varying chain length of the phosphonic acid molecules is similar to that observed for the carrier mobility and the subthreshold swing, i.e. a preferred large current on-off ratio is obtained for the medium-chain-length molecules. The largest values are obtained for the $HC_{14}PA$ SAM in the alkyl phosphonic acids (1.6×10^7) and for the $FC_{10}PA$ SAM in the fluoroalkyl phosphonic acids (3×10^6).

The different TFT characteristics suggest that the medium-chain-length molecules of the available range of alkyl and fluoroalkyl phosphonic acid molecules are an optimum choice for SAMs in hybrid dielectrics from a technological point of view. The next sections examine the properties of the SAMs as a function of the chain length of the phosphonic acid molecule, and the organic-semiconductor layer properties to correlate them with the TFT characteristics observed above.

6.4 Surface properties

6.4.1 Surface roughness and Surface energy

As was observed in Chapter 4, the surface properties of the gate dielectric are influential in modifying the organic-semiconductor morphology and thereby the electrical properties of the organic TFTs. In Chapter 4, the different combinations of the plasma-process parameters were instrumental in modifying the surface roughness of the AlO_x surface and thereby the surface of the conformal SAM. The surface roughness of the different phosphonic acid SAMs is plotted in Fig.6.9(a) for the AlO_x/HC_xPA hybrid gate dielectrics, i.e. the alkyl phosphonic acid SAMs and in Fig.6.9(b) for the AlO_x/FC_xPA hybrid gate dielectrics, i.e. the fluoroalkyl phosphonic acid SAMs.

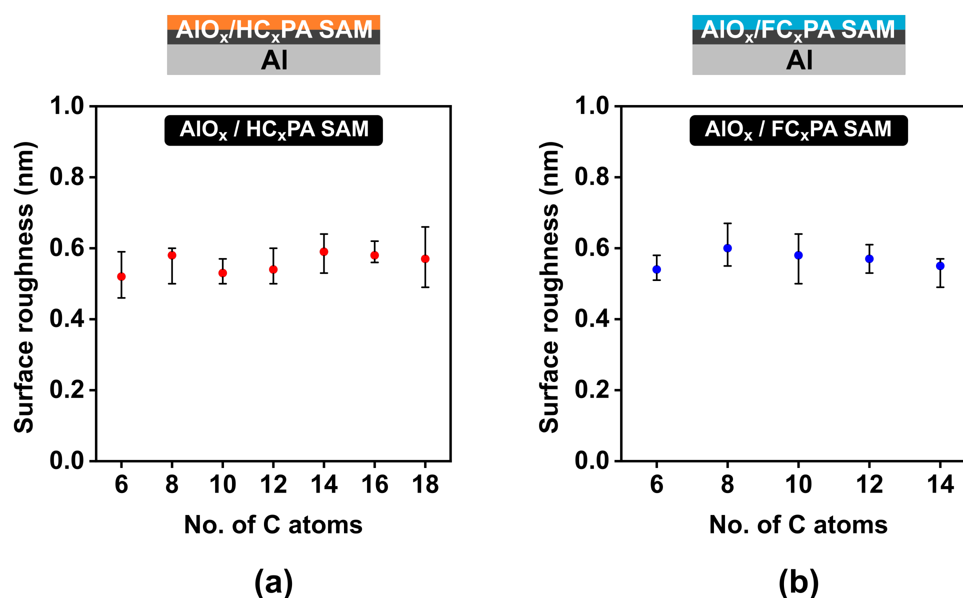


Figure 6.9: Surface roughness of (a) AlO_x/HC_xPA and (b)AlO_x/FC_xPA surfaces as a function of the phosphonic acid molecule chain length (number of carbon atoms) as measured by atomic force microscopy

It was observed in Chapter 4, that the surface roughness of an AlO_x surface prepared using the plasma parameter combination 200 W, 30 s was approximately 0.57 nm(Fig.4.10(a)). It was also observed that due to the conformal nature of the $HC_{14}PA$ SAM, there was no change in the surface roughness for the respective AlO_x and AlO_x/SAM surfaces. Since the underlying AlO_x films were fabricated by the identical plasma-parameter combination (200 W, 30 s), the surface roughness of all the AlO_x films before forming the different SAMs can be assumed to be constant. Fig.6.9 shows that for all

the different SAMs, whether the alkyl phosphonic acid or fluoroalkyl phosphonic acid SAMs, the surface roughness has almost no variation with the chain length and is constant at approximately 0.56 nm, similar to the bare AlO_x surface. This suggests that there is no variation in the surface roughness of the SAM surface with the chain length of the molecule and that all phosphonic acid molecules discussed here, form a conformal layer on the underlying AlO_x surface.

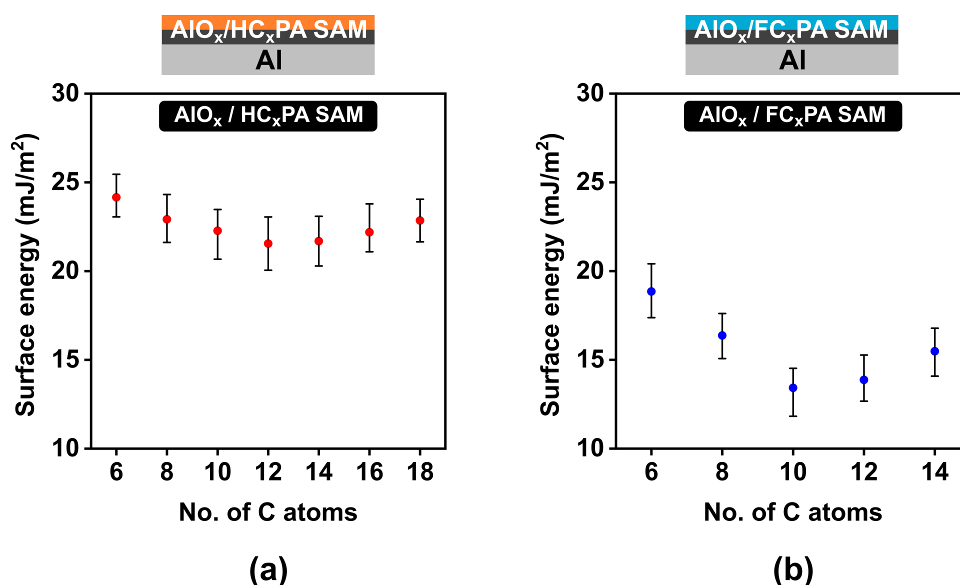


Figure 6.10: Surface energy of (a) AlO_x/HC_xPA and (b)AlO_x/FC_xPA surfaces as a function of the phosphonic acid molecule chain length (number of carbon atoms) as determined by contact-angle measurements and calculated using the Owens-Wendt method

It was also observed in Chapter 4 that the plasma conditions have virtually no effect on the surface energy of the AlO_x or the AlO_x/SAM surfaces. The surface energy as a function of the chain length of the different phosphonic acid molecule SAMs in plotted in Fig.6.10(a) for the the AlO_x/HC_xPA SAM surfaces and in Fig.6.10(b) for the AlO_x/FC_xPA SAM surfaces. The first important observation is that the surface energy for the fluoroalkyl phosphonic acids is between 13 mJ/m^2 and 18 mJ/m^2, which is on an average lower than that for the alkyl phosphonic acids, which is between 21 mJ/m^2 and 24 mJ/m^2. This is an effect of the strong electronegative fluorine atom substitutions and has also been observed in other literature reports investigating fluoroalkyl phosphonic acid SAMs [155].

The surface energy of the medium-chain-length $HC_{14}PA$ SAM is 21.5 mJ/m^2 and of the long chain $HC_{18}PA$ SAM is approximately 22.8 mJ/m^2, showing that the surface energy has a systematic variation with the chain length of the alkyl phosphonic acid SAMs. For

the fluoroalkyl phosphonic acid SAMs, a larger degree of variation is observed with the chain length of the molecules and the lowest surface energy of 13 mJ/m^2 is observed for the $FC_{10}PA$ SAM. Similar to other properties discussed above, the surface energy which was unaffected by the properties of the AlO_x layer, can be varied by the chain length and the type of the phosphonic acid molecule. The possibility of the surface energy affecting the growth and morphology of the organic-semiconductor layer will be discussed in the next section.

6.4.2 Morphology of SAMs as determined by the chain length of the individual molecules

Apart from the surface roughness and the surface energy of the SAMs, another important aspect of SAMs is the packing density and the molecular ordering of the individual molecules within the SAM. Several studies have characterized different types of SAMs using techniques such as contact-angle measurements, spectroscopic ellipsometry, infrared spectroscopy and X-ray photoelectron spectroscopy. Based on these in-depth studies, a basic idea of the morphology of SAMs dependent on the chain length of the individual molecules is presented below.

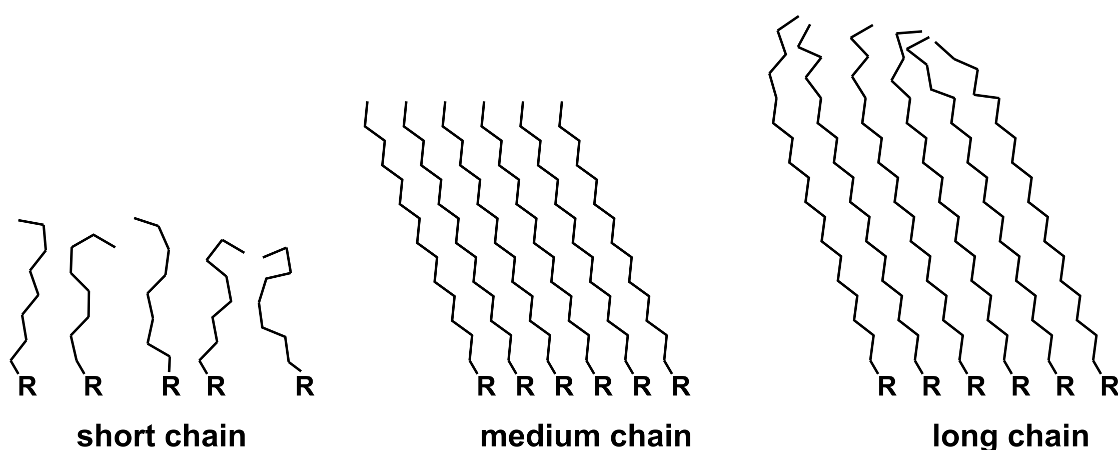


Figure 6.11: Schematic representation of the molecular ordering and packing density of SAMs dependent on the chain length of the individual molecules

After the almost instantaneous adsorption of the head group on the substrate, the aliphatic chains of the individual molecules start to align themselves by Van der Waals bonding forces among them to form the SAM. Based on the extensive studies of different SAMs, it can be deduced that the extent of the bonding forces among the aliphatic

chains depends on the chain length of the molecule. A schematic representation of the proposed morphology of the SAMs can be seen in Fig.6.11. For short chain length molecules (chain length shorter than 12 atoms), the interaction between the chains is smaller and the molecular chains are largely disordered. As the chain length increases, the bonding forces of the medium chain length molecules also increase and the SAM becomes more well-ordered and the packing density within the SAM increases. An increased interaction among the individual aliphatic chains is also expected to lower the surface energy of the SAM, as is also observed in Fig.6.10, in which the medium-chain-length molecules form SAMs with the lowest surface energy. For a further increase in the chain length of the molecule, it has been reported that the aliphatic chains are not stable enough to maintain the ordered nature of the SAM. Typically, gauche defects and surface disorder are observed at the surface of the SAMs with long-chain-length molecules. In such a case, the thickness of the SAM may not linearly increase with the chain length of the molecules, as seen with the trend in the gate-dielectric capacitance (Fig.6.2) of hybrid gate dielectrics. An increase in the disorder within the SAM, either for short-chain-length or long-chain-length molecules is also expected to increase the surface energy of the SAM, as observed in Fig.6.10 for the fluoroalkyl phosphonic acid SAMs.

The packing density and molecular ordering of the SAM is reported to influence the growth mode of the organic-semiconductor layer, besides the influence of other surface properties of the gate dielectric. A spectroscopic investigation of the SAMs to quantitatively measure the molecular ordering is beyond the scope of this thesis, but the general understanding of the morphology of the SAMs as explained above can be corroborated further by investigating the growth and morphology of organic semiconductors on different SAM surfaces.

6.5 Growth and morphology of organic semiconductors on self-assembled monolayers

The growth mode of the organic semiconductor on the gate-dielectric surface is crucial for the electrical properties of the organic TFT, and depends on a variety of factors such as the surface properties of the gate dielectric, and deposition parameters such as the deposition rate, the substrate temperature during deposition, etc. The organic

semiconductor molecules are deposited by thermal sublimation in a vacuum chamber. The organic-semiconductor material is placed in a container, which is resistively heated in order to sublimate the molecules for deposition. The substrate on to which the molecules are to be deposited is placed at a certain distance away from the material source, and is initially covered with a metal plate, hereafter referred to as the shutter. Once a suitable and stable rate of deposition is obtained, the metal shutter is moved away from the substrate to expose it to the sublimated organic-semiconductor molecules. The thickness of the film is controlled by a quartz microbalance and once the desired thickness is deposited, the metal shutter is moved to cover the substrate and stop the deposition process.

The organic-semiconductor morphology is usually observed by microscopy techniques, in which each observation of a microscopy image may take up to a few minutes. Due to the different time scales of observation with the microscopy techniques, and the growth process of the organic semiconductor, as well as the absence of a combined equipment for deposition and imaging, it is practically impossible to monitor the growth process of the organic semiconductor in situ. Therefore, the regular deposition process needed to be altered in order to make it possible to observe the growth mode of the organic semiconductor on different gate-dielectric surfaces. This was achieved by altering the deposition process and the movement of the shutter during the semiconductor deposition. Instead of a semiconductor film of a uniform thickness, the organic semiconductor was deposited with an increasing thickness along the length of the substrate. By imaging the organic semiconductor film with a thickness gradient, it was possible to observe the organic semiconductor with consecutively increasing thicknesses, i.e. at the different stages of growth and compare the growth mode of the organic semiconductor on different gate dielectric surfaces.

6.5.1 Growth of the organic semiconductor DNTT on different surfaces

The growth mode of the small-molecule organic semiconductor DNTT was observed by modifying the deposition setup of the thermal sublimation process. Usually, a metal shutter covers the substrate and is moved completely when a suitable deposition rate is obtained, to expose the substrate for semiconductor deposition. In the modified setup, a

motor was attached to the shutter to gradually move it during the semiconductor deposition, to deposit the organic semiconductor with a thickness gradient along the length of the substrate. The details of this experimental setup are given in Section 6.6. All other factors, including the rate of deposition and the substrate temperature during deposition were kept constant. Four different terminating surfaces were chosen as the substrate to deposit the semiconductor DNTT on: (a) bare AlO_x (Fig.6.12), (b) $AlO_x/HC_{14}PA$ SAM (Fig.6.13), (b) $AlO_x/HC_{18}PA$ SAM (Fig.6.14), and (d) $AlO_x/FC_{14}PA$ SAM (Fig.6.15). The growth mode of the semiconductor was observed by scanning electron microscopy (SEM) by imaging the sample at different positions located equidistant from each other. The different stages of growth are marked as 1-12, corresponding to different thicknesses of the semiconductor DNTT along the thickness gradient, and together show the progression of growth as the thickness of the semiconductor increases. Due to a difference in the atomic weight of the materials forming the dielectric and the semiconductor, it is clear that the darker regions represent the semiconductor and the lighter background is the underlying gate dielectric surface.

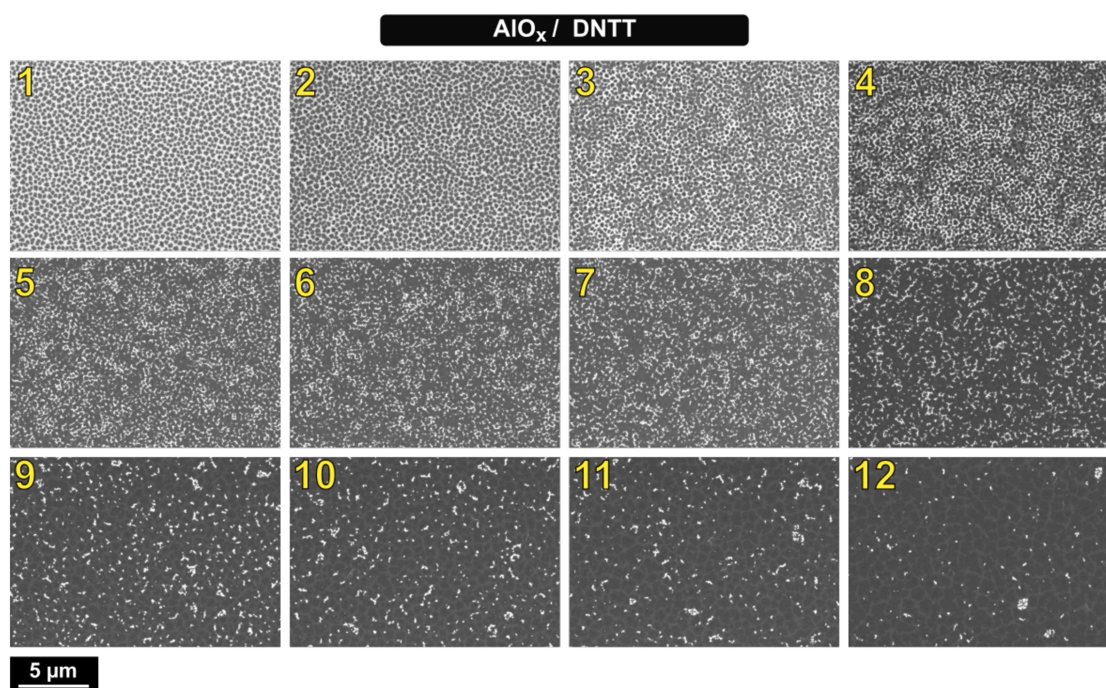


Figure 6.12: Progression of growth of the organic semiconductor DNTT on a **bare-AlO_x** surface observed by depositing a thickness gradient of DNTT and imaged by scanning electron microscopy at equidistant locations. The different stages (1-12) denote the different thicknesses of DNTT from a nominal thickness of approximately 1 nm to 7 nm deposited along the thickness gradient

The surface energy of the bare AlO_x surface is approximately 65 $mJ/^2$, the largest of

all four surfaces considered, and the AlO_x surface is extremely hydrophobic. On this bare AlO_x surface, the DNTT molecules nucleate as relatively small islands, which continue to grow and connect with each other. It can be observed in Fig.6.12, in stages 8 and 9, that before the first monolayer is formed as a complete layer, more islands are formed on top as the second monolayer. Towards the end of the observed growth process, the second monolayer islands can be seen on top of the disconnected first monolayer. This type of growth can be characterized as the island type, or 2D form of growth. The two alkyl phosphonic acid molecules considered in this section, $HC_{14}PA$ and $HC_{18}PA$, form SAMs with a very small difference in their surface energies (21.5 mJ/m^2 and 22.8 mJ/m^2 respectively). However, as can be seen in Fig.6.13 and Fig.6.14, the semiconductor DNTT has significantly different growth patterns on the two surfaces. On the medium chain length $HC_{14}PA$ SAM, the semiconductor DNTT has a typical island-layer growth (Stranski-Krastanov growth mode) where the islands which have nucleated in the initial stages, grow and coalesce to form a complete monolayer (as seen in Stages 5 and 6). Subsequently, the second monolayer starts growing as islands on the first complete monolayer (Stages 7 and 8). The isolated islands seen in Stages 6, 7 and 8 on the exposed gate dielectric surface are a result of spontaneous morphological changes occurring in ultrathin semiconductor films. This phenomenon is explained in detail in Chapter 7. It is important to note that these structures have formed as a result of the morphological changes, and are not part of the growth process. The evidence of the second monolayer of DNTT molecules forming as islands on top of the first complete monolayer film can be seen in growth stages 7 and 8, confirming that the growth mode is an island-layer (Stranski-Krastanov) type of growth.

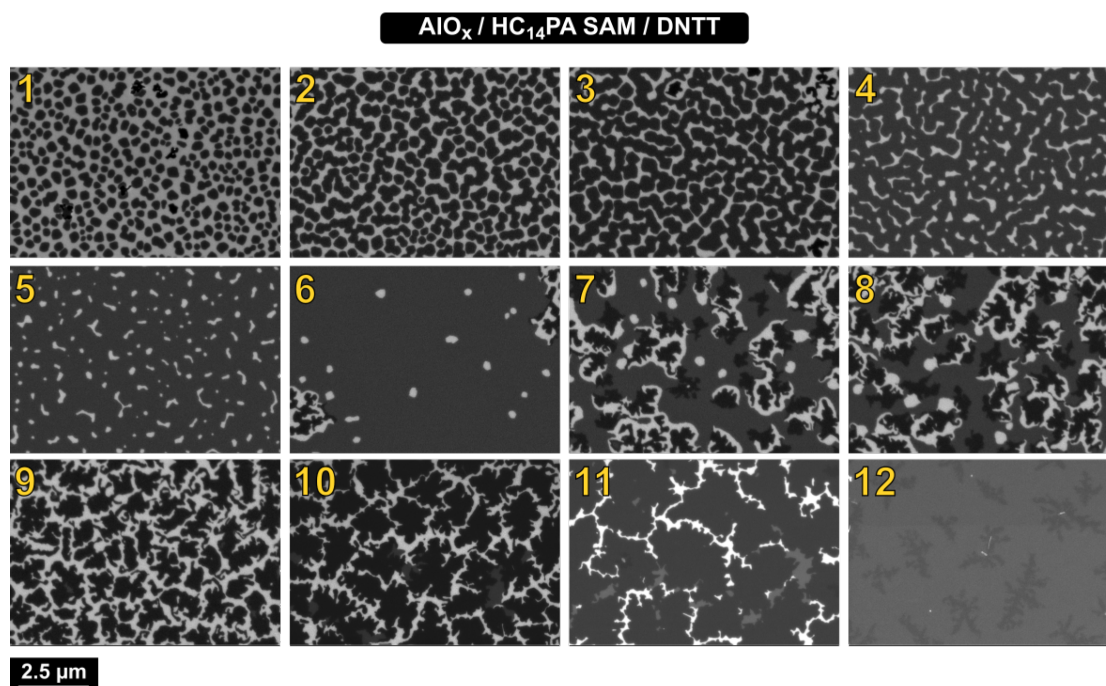


Figure 6.13: Progression of growth of the organic semiconductor DNTT on an **AlO_x/HC_{14}PA** surface observed by depositing a thickness gradient of DNTT and imaged by scanning electron microscopy at equidistant locations. The different stages (1-12) denote the different thicknesses of DNTT from a nominal thickness of approximately 1 nm to 7 nm deposited along the thickness gradient

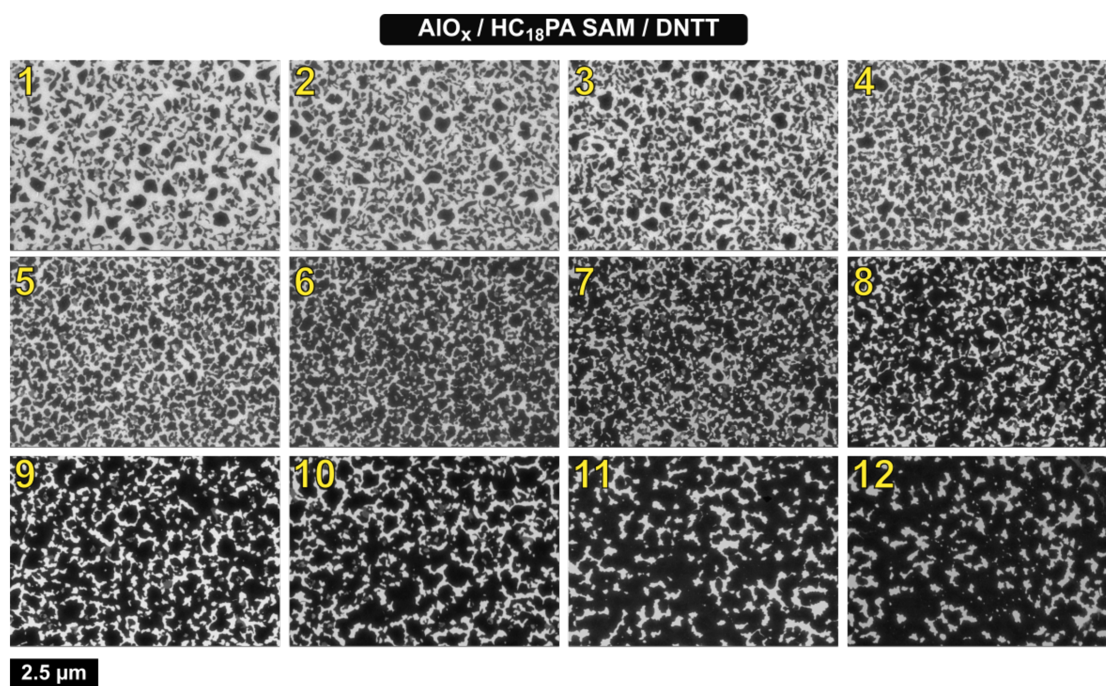


Figure 6.14: Progression of growth of the organic semiconductor DNTT on an **AlO_x/HC_{18}PA** surface observed by depositing a thickness gradient of DNTT and imaged by scanning electron microscopy at equidistant locations. The different stages (1-12) denote the different thicknesses of DNTT from a nominal thickness of approximately 1 nm to 7 nm deposited along the thickness gradient

It can also be observed that the initial nucleated islands on the surface of the $HC_{14}PA$ SAM, as seen in Stage 1, are the largest in size as compared to the other surfaces, signifying a smaller nucleation density. In contrast, the growth pattern of the semiconductor DNTT on the surface of the $HC_{18}PA$ SAM is notably different. The initial nucleation of islands is relatively irregular and has a higher nucleation density. The growth can still be characterized as island-layer type of growth as the islands are seen to grow and proceed towards forming a complete monolayer, without a second monolayer starting to nucleate. However, it must be noted that for the same thickness of the semiconductor deposited as on the $HC_{14}PA$ SAM, the first monolayer of DNTT on the $HC_{18}PA$ SAM is still incomplete and shows a significant exposure of the underlying gate dielectric.

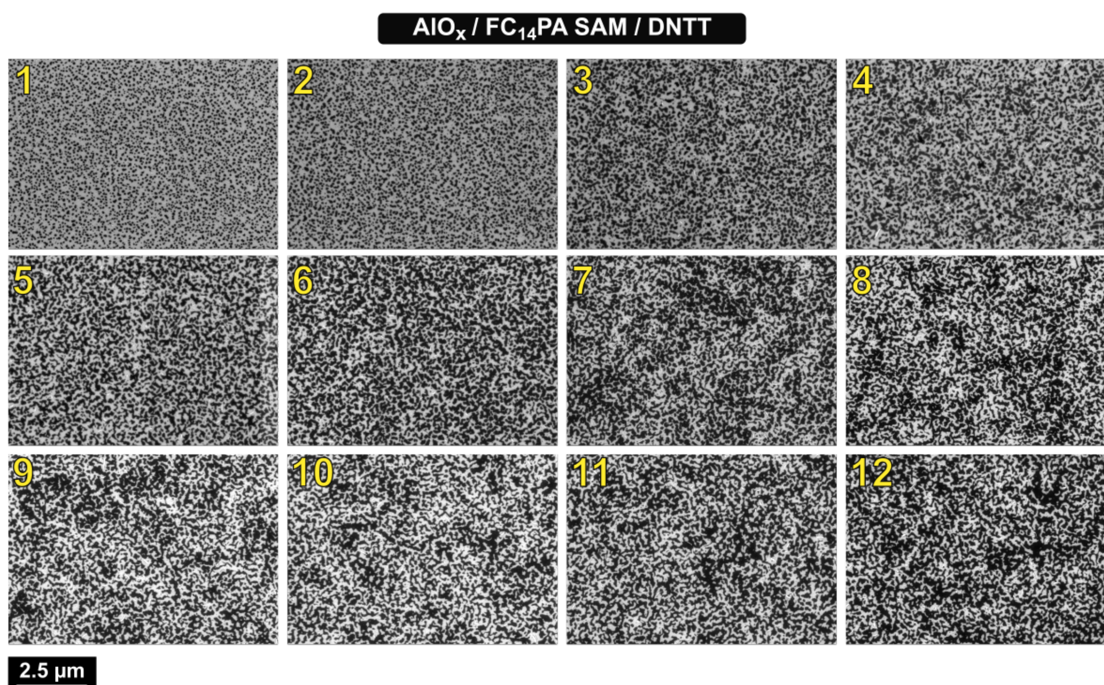


Figure 6.15: Progression of growth of the organic semiconductor DNTT on an **$AlO_x/FC_{14}PA$** surface observed by depositing a thickness gradient of DNTT and imaged by scanning electron microscopy at equidistant locations. The different stages (1-12) denote the different thicknesses of DNTT from a nominal thickness of approximately 1 nm to 7 nm deposited along the thickness gradient

The $AlO_x/FC_{14}PA$ SAM has the lowest surface energy of the four surfaces considered in this section (15 mJ/m^2). When the semiconductor DNTT is deposited onto the $AlO_x/FC_{14}PA$ SAM surface, as can be seen in Fig.6.15, it has an extremely high nucleation density with a large number of nuclei of extremely small size forming in the first stage. As the semiconductor deposition progresses, it appears that the islands grow in size towards coalescing and forming a complete film, but a complete monolayer is not

Substrate	Surface energy (mJ/m^2)	Charge-carrier mobility (cm^2/Vs)	DNTT growth mode
AlO_x	65	0.4	island
$AlO_x/HC_{14}PA$	21.6	2	island-layer
$AlO_x/HC_{18}PA$	22.8	1.2	island-layer
$AlO_x/FC_{14}PA$	15	0.6	unclear

Table 6.2: Summary of surface energy of different gate dielectrics, the charge-carrier mobility of DNTT TFTs, and the growth mode of the semiconductor DNTT on those gate dielectric surfaces as observed by scanning electron microscopy

formed. Due to the small size and large density of the nuclei, it is unclear whether a second monolayer starts nucleating before the first monolayer is complete, and hence the growth mode cannot be clearly defined. Nevertheless, it is clear that for the same nominal amount of the organic semiconductor deposited, the molecule DNTT does not form a complete film on the fluorinated $FC_{14}PA$ SAM surface, and the degree of percolation within the initial monolayer is significantly lower, compared to the other surfaces studied.

Table 6.2 tabulates the four different gate dielectrics considered above, their surface energy, the charge-carrier mobility of DNTT TFTs with the particular gate dielectric and a nominal DNTT thickness of 25 nm and the growth mode of DNTT on the surface as observed above. The charge-carrier mobility was extracted from the transfer characteristics (given in Appendix D) of DNTT TFTs, which were fabricated with all other components and conditions identical except the gate dielectric, for comparison. It is evident from this table and from observing the growth pattern of DNTT on the four different surfaces that there is no systematic correlation between the surface energy of the gate dielectric and the charge-carrier mobility of the organic TFT, in case of the phosphonic acid SAM-DNTT combination. A drastic change in the surface energy from a hydrophobic surface to a hydrophilic surface is likely to influence the growth of the semiconductor due to a change in the wettability of the surface, as is observed with the island growth of DNTT on the bare-AlO_x surface. This effect has also been reported previously in other studies. However, in an attempt to overcome the hurdle of a high surface energy, an uncontrolled reduction in surface energy does not seem to be the solution. As can be seen on the $FC_{14}PA$ SAM surface, which has the lowest surface energy, the semiconductor DNTT does not show a favorable growth pattern, and the DNTT TFT also has a lower charge-carrier mobility. Instead, there exists a complex

relationship between the surface properties of the gate dielectric, the growth mode of the organic semiconductor and thereby the electrical properties of the organic TFT. It must also be noted that each combination of an organic semiconductor and the substrate is unique, and these correlations can very rarely be generalized.

Apart from the surface energy (and the surface roughness), other aspects of SAMs have been reported to influence the growth and morphology of the organic semiconductor, such as the chemical nature, packing density, molecular ordering and defects within the SAM. For example, Virkar et al. showed that the organic semiconductor pentacene showed a change in the growth mode and subsequent quality depending on the density of the underlying OTS (octadecylsilane) SAM. OTS SAMs with a higher packing density and molecular order led to pentacene TFTs with a higher charge-carrier mobility. This was, quite contrary to common belief, attributed to a 2D-island-type growth in pentacene films which resulted in a smaller grain size, but a more complete film coverage in the first monolayer. Based on energetic calculations at the interface, they concluded that a higher ordering in the underlying SAM led to better-quality pentacene films, due to a more suitable growth mode at the gate dielectric-semiconductor interface. For DNTT films observed above on the two alkyl phosphonic acid SAMs, with almost identical surface energies, a similar reasoning can be expected. Surface disorder in the $HC_{18}PA$ SAM may lead to an unfavorable DNTT growth on the surface and a subsequent smaller charge-carrier mobility in the transistor.

Virkar et. al also performed extensive calculations of the interlayer interaction energies and the difference in chemical potentials of the vapor and condensed phases to show that the condition for 2D growth is mathematically satisfied [169]. In this process, along with experimental factors such as the rate of deposition and the substrate temperature which influence the semiconductor growth, other quantities were used from literature, such as the enthalpy of sublimation for pentacene, and the interlayer molecular-substrate energy, determined elsewhere. To establish the exact mechanisms at play for the combination of the semiconductor DNTT and the phosphonic acid SAMs, similar thermodynamic energies will need to be experimentally determined, which is beyond the scope of this current work.

Nevertheless, the growth mode of the semiconductor DNTT on the different surfaces can be interpreted to draw several important conclusions. Firstly, correlations between the charge-carrier mobilities and characteristics such as island/island-layer growth or the grain size of the complete polycrystalline film are incomplete. An organic-semiconductor

film might show an island type of growth mode, or a large density of nuclei, and therefore a large density of grain boundaries and yet form a high-quality film, yielding a large carrier mobility. Therefore, not just the density of grain boundaries, but also the nature of those grain boundaries are important. From the SEM images of the growth mode of DNTT and the charge-carrier mobility values in Table 6.2, the percolation path in the first monolayer of the organic semiconductor, i.e. the formation of a complete monolayer appears to be of utmost importance to the charge-transport properties of the organic TFT. The highest charge-carrier mobility is obtained for the DNTT TFT with the $HC_{14}PA$ SAM in the hybrid gate dielectric, and DNTT forms a completely closed monolayer film on the gate-dielectric surface, as observed in Fig.6.13. The energetic reasons for having a highly dense percolation path and thereby a complete monolayer seem to be multifold, and need to be carefully investigated for individual gate dielectric-semiconductor combinations.

6.5.2 Morphology of organic semiconductors DNTT and DPh-BTBT on phosphonic acid SAMs of different chain lengths

Along with the growth of the semiconductor on different surfaces, it is equally important to assess the morphology of the organic-semiconductor layer as it is deposited for transistor operation.

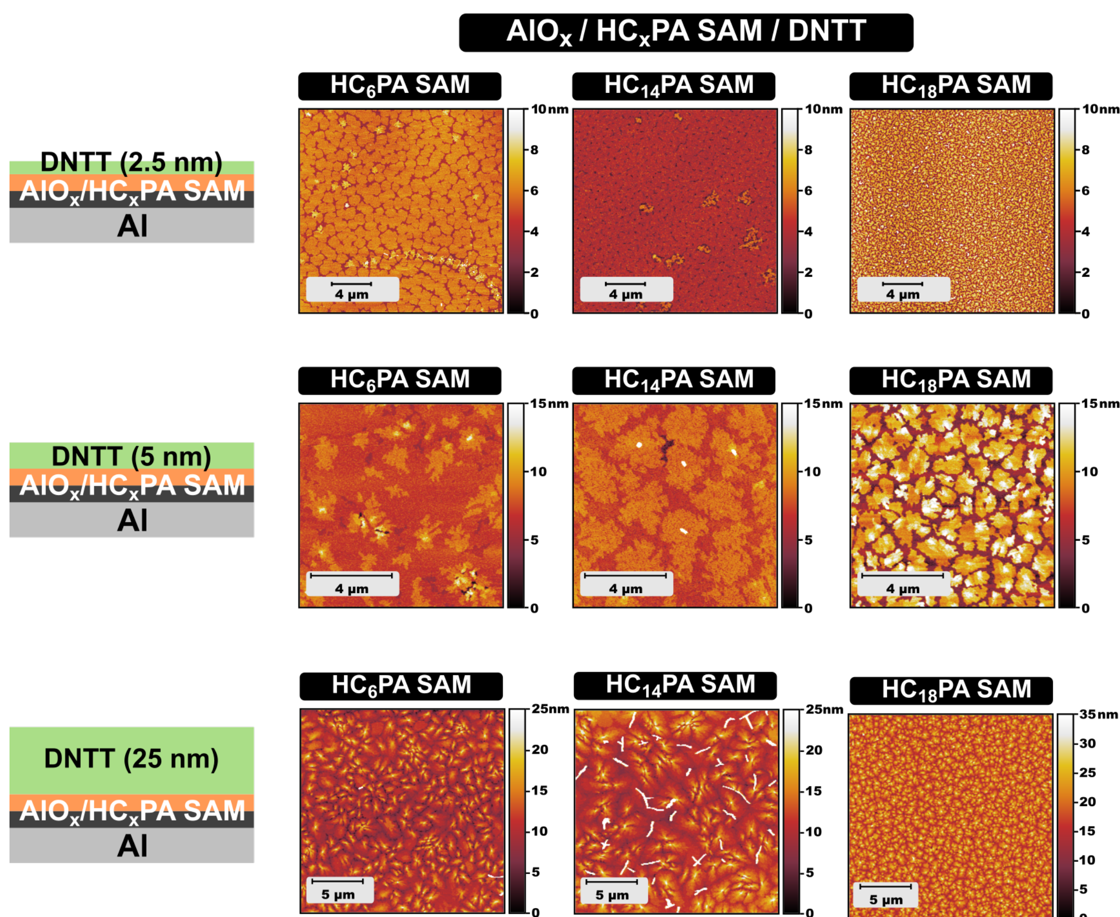


Figure 6.16: Morphology of the organic semiconductor DNTT with a nominal thickness of 2.5 nm, 5 nm and 25 nm on three alkyl phosphonic acid SAMs as imaged by atomic force microscopy

As each gate dielectric-organic semiconductor combination must be considered individually, this section investigates the morphology of the organic semiconductors used to study the electrical properties of organic TFTs in this chapter, i.e. DNTT with different chain-length alkyl phosphonic acid SAMs and DPh-BTBT with different chain-length fluoroalkyl phosphonic acid SAMs. Different thicknesses of the organic semiconductor were deposited onto the respective SAM surfaces, closer to the dielectric-semiconductor interface and at its full thickness, and imaged using atomic force microscopy (AFM).

Fig.6.16 shows the AFM micrographs of nominally 2.5 nm, 5 nm and 25 nm-thick DNTT films on three different alkyl phosphonic acid SAMs: the shortest-chain-length HC_6PA, the medium-chain-length $HC_{14}PA$ and the longest-chain-length $HC_{18}PA$. Considering the nominally 2.5 nm-thick DNTT films, an initial growth pattern of the semiconductor DNTT can be observed on the three surfaces, as was observed in the previous section. The semiconductor forms a complete, uniform film on the medium chain length $HC_{14}PA$ SAM, while a relatively more disconnected monolayer film with taller islands on the other two SAMs. It can also be observed that the island size is relatively large on the HC_6PA SAM as compared to that of the $HC_{18}PA$ SAM. For the nominally 5 nm-thick films of DNTT, a second-monolayer morphology can be observed, and the largest grain size for DNTT is seen on the $HC_{14}PA$ SAM. A continuation of this distinction can also be seen in the nominally 25 nm thick DNTT films as they are deposited for transistor operation. Although all films show a dendritic terrace-like structure, the largest grain size and thereby the relatively smallest density of grain boundaries for the semiconductor DNTT can be observed on the medium-chain-length $HC_{14}PA$ SAM.

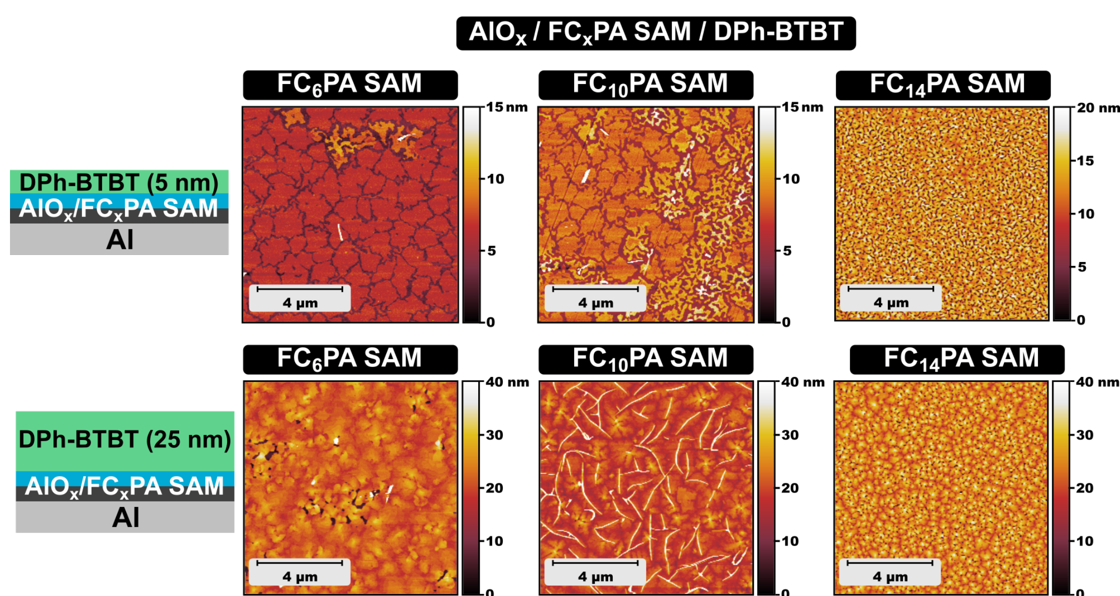


Figure 6.17: Morphology of the organic semiconductor DPh-BTBT with a nominal thickness of 5 nm and 25 nm on three fluoroalkyl phosphonic acid SAMs as imaged by atomic force microscopy

Similarly, for the DPh-BTBT TFTs with the different fluoroalkyl phosphonic acid SAMs, Fig.6.17 shows the morphology of nominally 5 nm and 25 nm-thick films of DPh-BTBT on three SAMs with the respective fluoroalkyl phosphonic acid molecules: FC_6PA,

$FC_{10}PA$ and $FC_{14}PA$. Considering the nominally 5 nm-thick DPh-BTBT films, the formation of the second monolayer can be seen during the semiconductor growth process. It can be observed that the grain size of the DPh-BTBT layer is relatively the smallest on the long chain length $FC_{14}PA$ SAM. The AFM images of the nominally 25 nm-thick DPh-BTBT films, as they are deposited for TFT operation, give a much clearer picture of the film quality. The DPh-BTBT film on the short-chain-length FC_6PA SAM shows an almost amorphous film structure with no distinct grains or terrace-like structures. There are also minor discontinuities in the film which can be observed. For the medium-chain-length $FC_{10}PA$ SAM, a favorable semiconductor morphology can be observed, with a dendritic grain structure and relatively large-sized terraces. In contrast, the DPh-BTBT film on the long-chain $FC_{14}PA$ SAM shows a relatively smaller grain size with a larger density of grain boundaries in the film.

The growth of the semiconductor DNTT and the film morphology of the semiconductors DNTT and DPh-BTBT on different phosphonic acid SAMs provide useful insights into the correlation between the chain length of the phosphonic acid molecules and electrical characteristics of the organic TFTs. Although the correlation between the grain size of an organic-semiconductor film and the charge-carrier mobility of an organic TFT cannot be generalized, it appears that in the combination of materials studied in this work, a larger grain size in the films of DNTT and DPh-BTBT is beneficial for larger charge-carrier mobilities. In both cases, it was observed that for the long-chain-length molecules ($HC_{18}PA$ and $FC_{14}PA$), the grain size of the semiconductor films was relatively very small. This effect may be a result of the surface disorder in long-chain phosphonic acid molecules. The highest charge-carrier mobility in DNTT TFTs was found for the medium-chain-length $HC_{14}PA$ SAM and in DPh-BTBT TFTs for the medium-chain-length $FC_{10}PA$ SAM, which in both cases had the largest grain size and the smallest density of grain boundaries. A number of tall features can be observed in the DNTT films on the $HC_{14}PA$ SAM as well as the DPh-BTBT films on the $FC_{10}PA$ SAM, which are characteristic of high-mobility semiconductor films, although the exact origin and nature of these features will need further investigation. It can be concluded for this particular case, a large grain size and more importantly, the formation of a complete film in the initial monolayer is vital for high-quality organic TFTs. Although specific reasons behind these layer properties will need more investigation, the optimum choice of phosphonic acid molecules for these organic TFTs from a technological point of view has been identified.

6.6 Experimental

Fabrication of capacitors and TFTs

Using phosphonic acid molecules of different chain lengths shown in Fig.6.18, SAMs of different thicknesses were investigated. For each type of phosphonic acid molecule, capacitors and organic TFTs with hybrid gate dielectrics consisting of AlO_x and the phosphonic acid SAM were fabricated.

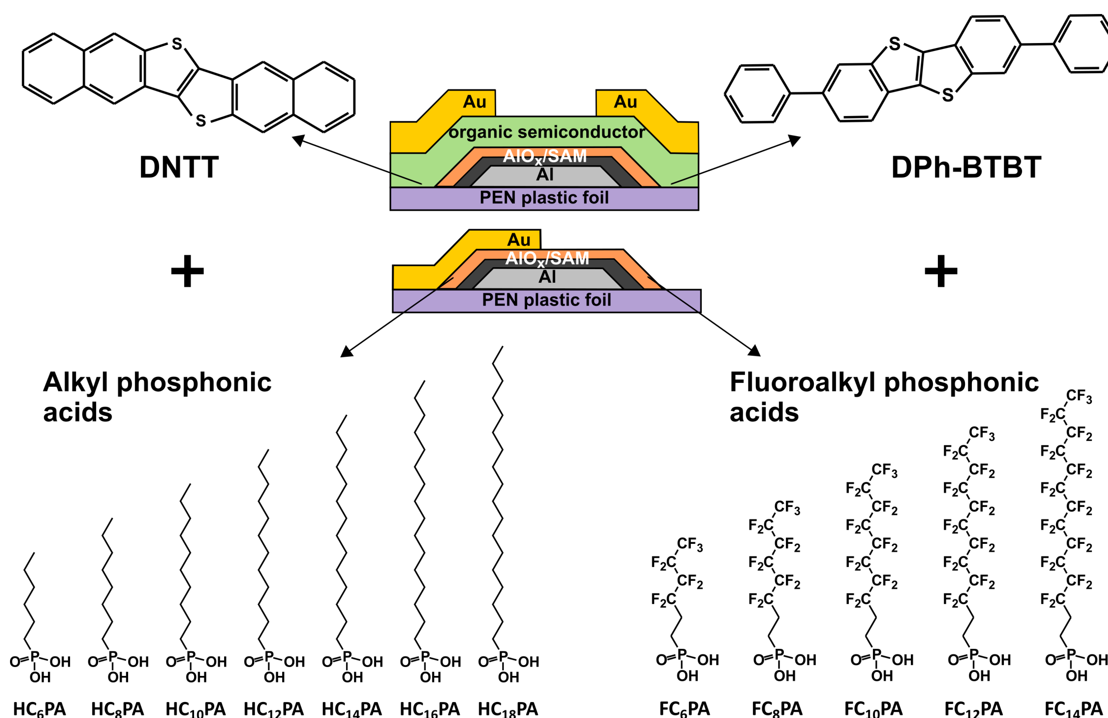


Figure 6.18: Schematic cross-section of the organic TFTs and capacitor structures fabricated in this thesis chapter along with the chemical structures of the organic semiconductors DNTT and DPh-BTBT and the different alkyl and fluoroalkyl phosphonic acid molecules used to form SAMs in the hybrid gate dielectrics

All devices were fabricated on flexible poly(ethylene)2,6-naphthalate (PEN) plastic substrates (PEN provided kindly by William A. Macdonald from Du Pont Teijin Films, Wilton, UK). The PEN substrates were annealed at 80°C beforehand in order to avoid any shrinking effects or changes in geometry during the fabrication process. Metal-insulator-metal capacitors and inverted staggered (bottom-gate, top-contact) TFTs were fabricated on the flexible PEN substrates. As a first step, 20 nm thick gold contact pads were deposited to make electrical contact with the gate electrode later possible. For the bottom electrode of the capacitors and the gate electrode of the TFTs, aluminum films with a nominal thickness of 30 nm were deposited by thermal evaporation in vacuum

with a rate of about 2 nm/s. AlO_x films were produced by plasma oxidation using a capacitively coupled plasma mode with a partial oxygen pressure of 0.01 mbar and an oxygen flow rate of 30 sccm. The plasma power selected was 200 W and the duration of plasma exposure was limited to 30 s. After formation of the AlO_x component of the gate dielectric, the substrates were immersed into a solution of a particular phosphonic acid molecule in 2-propanol to allow the molecules to assemble into a monolayer, i.e. the self-assembled monolayer (SAM). Each substrate was kept immersed in solution for 3 hours, after which it was rinsed with isopropanol to remove any non-chemisorbed molecules, dried with dry nitrogen and subsequently exposed to 80°C for 10 minutes to stabilize the monolayer.

Alkyl phosphonic acid molecules of seven different chain lengths, from six carbon atoms to eighteen carbon atoms in the aliphatic chain were used, the chemical names are given below: (Alkyl phosphonic acid molecules were procured from PCI Synthesis, Newburyport, MA, USA).

- HC_6PA : hexylphosphonic acid
- HC_8PA : octylphosphonic acid
- $HC_{10}PA$: decylphosphonic acid
- $HC_{12}PA$: dodecylphosphonic acid
- $HC_{14}PA$: tetradecylphosphonic acid
- $HC_{16}PA$: hexadecylphosphonic acid
- $HC_{18}PA$: octadecylphosphonic acid

The alkyl phosphonic acid molecules were used to fabricate organic TFTs in combination with the small-molecule organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; Sigma Aldrich).

Fluoroalkyl phosphonic acid molecules of five different chain lengths, from six carbon atoms to fourteen carbon atoms in the aliphatic chain were used, the chemical names are given below: (Fluoroalkyl phosphonic acid molecules were procured from Specific Polymers).

- FC_6PA : 1H,1H,2H,2H-perfluorohexylphosphonic acid

- FC_8PA : 1H,1H,2H,2H-perfluorooctylphosphonic acid
- $FC_{10}PA$: 1H,1H,2H,2H-perfluorodecylphosphonic acid
- $FC_{12}PA$: 1H,1H,2H,2H-perfluorododecylphosphonic acid
- $FC_{14}PA$: 1H,1H,2H,2H-perfluorotetradecylphosphonic acid

The fluoroalkyl phosphonic acid molecules were used to fabricate organic TFTs in combination with the small-molecule organic semiconductor 2,7-diphenyl[1]-benzothieno[3,2-b][1]benzothiophene (DPh-BTBT; Sigma Aldrich).

Once the SAM had been formed and the fabrication of the hybrid gate dielectric was complete, the particular small-molecule organic semiconductor was deposited by thermal sublimation in vacuum in a Leybold Univex300 vacuum evaporator system at a base pressure of 10^{-5} mbar, with a deposition rate of 0.03 nm/s and with a nominal thickness of 25 nm. During the DNTT deposition, the substrate was held at a constant temperature of 60 °C, while the substrates were not heated during the DPh-BTBT deposition and kept at room temperature (25 °C). For the top electrode of the capacitors and the source/drain contacts of the TFTs, gold with a thickness of 30 nm was deposited by thermal evaporation in vacuum with a rate of 0.03 nm/s. The metals and the organic semiconductors were patterned using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany). The capacitors have an area of 200 μm × 200 μm. The TFTs have a channel length of 20 μm and a channel width of 100 μm. For each of the phosphonic acid molecules, capacitors and TFTs were fabricated on the same substrate to minimize the effects of unintentional parameter variations. Substrates were stored in ambient air at room temperature under yellow laboratory light before electrical measurement.

Experimental setup for observing the growth mode of the organic semiconductor on different gate dielectric surfaces

Silicon substrates with a 100 nm-thick thermally grown silicon dioxide layer with dimensions 9 cm x 2 cm were used to investigate the growth mode of the organic semiconductor DNTT on different surfaces. The experimental setup is shown schematically in Fig.6.19.

The aluminum, aluminum oxide, SAMs and DNTT films were deposited as described above.

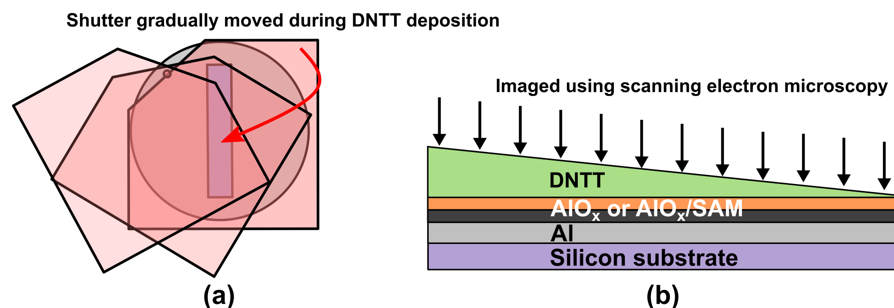


Figure 6.19: Schematic representation of the experimental setup for observing the growth process of the organic semiconductor on different gate dielectric surfaces

Four different substrates were used to deposit the DNTT on: (a) bare AlO_x, (b) $AlO_x/HC_{14}PA$ (c)$AlO_x/HC_{18}PA$ and (d)$AlO_x/FC_{14}PA$. The deposition setup was modified with a motor attached to the shutter covering the substrate during deposition inside the vacuum chamber. With the assistance of the motor, the shutter was gradually moved at a rate of 0.75 mm/s to gradually expose the substrate along its length during the semiconductor deposition. The semiconductor DNTT was deposited by thermal sublimation at a rate of 0.06 nm/s. The substrate was imaged using a Zeiss Merlin scanning electron microscope (SEM).

Electrical characterization

All electrical measurements were performed in ambient air at room temperature under yellow laboratory light. The capacitance measurements were performed by applying an alternating voltage with an amplitude of 0.2 V and a frequency of 1 kHz. The current–voltage measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer.

Surface characterization

Static contact-angle measurements were performed using a Krüss contact angle measurement system. The contact angles of water and hexadecane on the AlO_x/SAM hybrid dielectrics were measured immediately after the SAM treatment. The surface energies were calculated using the Owens–Wendt method [99]. AFM images were recorded in air using a Bruker Dimension Icon Atomic Force Microscope in peak force tapping mode. Data processing was performed using the AFM analysis software Gwyddion.

6.7 Summary and Outlook

The aliphatic chain length of molecules used to form SAMs is an important aspect influencing the properties of hybrid gate dielectrics and organic TFTs. Two different phosphonic acid molecules, i.e. molecules with an unsubstituted alkyl chain and molecules with a fluorine-substituted fluoroalkyl chain were investigated with different chain lengths (number of carbon atoms in the aliphatic backbone). With a change in the chain length of the phosphonic acid molecules, the thickness of the SAM can be modified, and the capacitance of the gate dielectric can be varied, which is not possible by varying the thickness of the underlying AlO_x film. Organic TFTs were fabricated with the different chain-length phosphonic acid SAMs, with two different organic semiconductors. The performance characteristics of the TFTs were studied as a function of the chain length and the medium-chain-length molecules for both types of phosphonic acids showed an optimum TFT performance in terms of the charge-carrier mobility, subthreshold swing and the current on-off ratio. The surface properties of the different SAMs were investigated in terms of the surface roughness and the surface energy. The chain length of the molecule had no measurable effect on the surface roughness of the SAMs, unlike the effect observed by changing the plasma parameters of the AlO_x fabrication process. The surface energy of the SAMs changed drastically by changing the type of the molecule from alkyl phosphonic acid molecules to fluoroalkyl phosphonic acid molecules, with a further slight variation with the chain length of the fluoroalkyl phosphonic acids. The morphology of the organic semiconductors DNTT and DPh-BTBT on the different phosphonic acid SAMs revealed that the medium-chain-length phosphonic acid molecules ($HC_{14}PA$ and $FC_{10}PA$) led to the largest grain size in the polycrystalline organic semiconductor films and can be correlated with the largest charge-carrier mobilities in the respective organic TFTs. The growth of the organic semiconductor DNTT on different gate-dielectric surfaces revealed no systematic correlation with the surface energy of the gate-dielectric surface. However, it can be concluded that a well-connected initial monolayer and a dense percolation path for charge carriers during the growth of the semiconductor is essential for high-performance organic TFTs. A further study of the properties of the SAMs with respect to their packing density and molecular order with spectroscopic techniques would improve the understanding of the different growth modes of organic semiconductors and give better control over the electrical properties of organic TFTs.

Chapter 7

Stability of ultrathin organic-semiconductor films and fabrication of ultrathin organic transistors

The previous chapters have all focused on the different components of the hybrid gate dielectric and the influence of the gate dielectric on the electrical properties of organic thin-film transistors (TFTs). Chapter 6 also discussed the effect of the gate-dielectric surface on the growth and morphology of the organic-semiconductor film and in-turn the electrical performance of the organic TFT. In this chapter, the organic-semiconductor layer, specifically the part in close proximity with the gate dielectric will be studied in detail. Apart from the many technological applications, the organic TFT is also a favorable system to explore new organic semiconductors and corresponding device physics. For typical organic TFTs with vacuum-processed organic semiconductors, as have been discussed in this thesis, the semiconductor film is usually several monolayers (MLs) thick. The influence of the semiconductor-layer thickness on different TFT characteristics, especially the charge-carrier mobility, has been extensively investigated by both theoretical simulations as well as experimental studies [245–249]. It has also been demonstrated how a variety of factors like the choice of the semiconductor molecule,

TFT architecture (top-contact or bottom-contact) and semiconductor-deposition parameters influence the growth of the organic-semiconductor layer and the development of the semiconductor-gate dielectric interface. Studies with TFTs based on thiophene oligomers reveal that the gate-field-induced conducting channel in a thin-film transistor, and hence majority of the charge transport, is positioned in the first one to two monolayers of the organic semiconductor thin film closest to the gate dielectric [83, 84, 250]. For studies with pentacene TFTs, the charge-carrier mobility saturated after six monolayers of pentacene had been deposited [251].

Although great progress has been made in the development of organic TFTs in terms of their performance and stability, there is further scope in terms of exploring the dynamic relationship between the organic-semiconductor-layer thickness and transistor performance to gain further insight into the structure-property relationship at the semiconductor-gate dielectric interface. Fabricating stable and reliable organic TFTs with ultrathin (less than 5 nm thick) semiconductor layers could lead to further development towards understanding intrinsic charge transport, exploring new and unique applications and low-cost device fabrication [252]. Since the conductive channel in bottom-gate architectures would be located at the surface in ultrathin-film transistors, these devices would make it possible to investigate charge transport and the morphology of the semiconductor in the channel using surface-sensitive techniques as opposed to the channel being buried under additional layers for transistors with several monolayer-thick semiconductor layers. Ultrathin devices with a range of semiconductors have also been used to study aspects of transistor performance such as contact resistance, threshold-voltage shifts, and trap densities and their correlation to the semiconductor thickness. Ultrathin TFTs are also suitable for the fabrication of highly sensitive sensors and could be developed into new applications [53]. There is also a great economic advantage of lowering the overall cost of fabrication by minimizing the material consumption by depositing the semiconductor as an ultrathin layer, especially those fabricated by vacuum deposition techniques which entail a considerable loss of excess material.

In order to fabricate ultrathin organic TFTs for both technological and investigative purposes, it is necessary to have devices with a suitably long stability and reliable, reproducible performance characteristics. One key hurdle in the past concerning the stability of organic thin-film transistors was the environmental stability of small-molecule organic semiconductors, such as pentacene. Pentacene undergoes rapid oxidation when exposed to air, thereby losing its π-conjugation and ability to transport charge, and as

a result, a rapid decrease in the charge-carrier mobility of pentacene TFTs is observed upon exposure to air [253–255]. To overcome this, molecules with a higher ionization potential, and hence higher air-stability, were synthesized [101]. These included molecules such as di(phenylvinyl)anthracene (DPVAnt) [81] and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [72,256]. DNTT is a particularly promising small-molecule organic semiconductor for the fabrication of organic-TFT-based active-matrix displays [257,258], sensor arrays [259, 260], and integrated circuits [261–264]. As demonstrated in previous chapters of this thesis, DNTT TFTs are p-channel transistors that typically have charge-carrier mobilities up to 3 cm^2/Vs. In terms of stability against oxidation, chemical decomposition, elevated temperature and formation of defect states, DNTT is one of the most stable organic semiconductors [101,176,189,265,266]. It was also shown in Chapter 6, that on suitable gate-dielectric surfaces, as the $AlO_x/HC_{14}PA$ hybrid gate dielectric, DNTT films typically grow in a Stranski–Krastanov (island-layer) mode, much like films based on other small-molecule organic semiconductors with similar chemical structures. The molecules adopt an upright-standing molecular orientation both in the complete monolayer(s) that initially cover(s) the substrate surface as well as in the islands that are formed beyond a critical film thickness to minimize mechanical strain. This molecular orientation was verified using X-ray diffraction measurements, and the results are given in Appendix A. This upright-standing orientation is generally the preferred molecular arrangement for the purpose of fabricating organic TFTs, as it promotes π-orbital overlap and efficient charge transport in the lateral direction.

However, Breuer et al. recently observed that DNTT films with a nominal thickness of one to two molecular monolayers spontaneously undergo a rapid structural reconfiguration at room temperature within minutes after deposition that proceeds by lateral and vertical mass transport and leads to a rearrangement of the initially closed (or at least connected) single-monolayer-thick DNTT films into disconnected islands with a thickness of several layers [267]. In analogy to the behavior of thin liquid films on solid surfaces [268], this process is also referred to as post-deposition dewetting [269,270] or rapid roughening [271], and it has been observed in ultrathin films based on a variety of organic materials, such as polystyrene [270], diindenoperylene [271] and pentacene [272, 273]. When a molecular monolayer of, for example, DNTT is deposited onto a solid surface, this monolayer will form during a non-equilibrium phase of the film-growth process and will thus be characterized by significant mechanical strain that results from the competition between adsorption and intermolecular forces [274]. If the molecule–substrate

interactions are weaker than the intermolecular interactions, thermally activated molecular diffusion will cause this initially closed (or at least connected) molecular monolayer to break up, and a combination of lateral and vertical mass transport will lead to the formation of tall, disconnected islands. This can be considered similar to the Ostwald ripening process often observed during annealing processes, where large, stable droplets grow at the expense of smaller, less stable droplets [275], in order to reduce the contribution of interfacial energy. While temporal morphological changes have also been observed for thick DNTT films (with a nominal thickness of 40 nm) [267], these occur on much larger time scales of weeks or months, due to the substantially larger mass transport involved in such thick films, and will not be considered in this particular thesis.

The focus of this chapter is on the spontaneously occurring structural reconfiguration of ultrathin DNTT films and its effect on the electrical characteristics of organic TFTs based on such films. Furthermore, the extent to which this structural reconfiguration can be prevented by cryogenic cooling or in-situ encapsulation has also been explored. For this purpose, organic TFTs based on ultrathin DNTT films have been fabricated, and unlike in the previous chapters, the TFT architecture of choice is inverted coplanar, i.e. bottom-gate, bottom-contact (Schematic shown in Fig.2.4). This investigation is motivated by the need for a better understanding of the dynamics of the morphological changes that occur in ultrathin films of vacuum-deposited small-molecule semiconductors and of the effects that these morphological changes have on the long-term stability of ultrathin devices, such as highly sensitive chemical, physical or biological sensors.

An important prerequisite for this investigation is the ability to unambiguously assign the changes observed in the electrical properties of the ultrathin semiconductor films to the mass transport and resulting changes in morphology, as opposed to any other processes, such as any chemical reactions, e.g. the oxidation or decomposition of the molecules during exposure to air and humidity. This makes DNTT the perfect choice for this study, as DNTT is one of the most stable organic semiconductors with respect to long-term exposure to ambient air and elevated temperatures. Owing to its excellent chemical stability, the changes in the measured electrical properties of the ultrathin DNTT films can be unequivocally assigned to the morphological changes observed.

7.1 Ultrathin films of the organic semiconductor DNTT

7.1.1 Determining the minimum nominal DNTT thickness required for functional TFTs

Before observing the morphological changes in ultrathin films of the organic semiconductor DNTT, it is necessary to determine the smallest nominal DNTT thickness for which functional TFTs can be obtained. Four different DNTT films with nominal thicknesses of 1, 1.5, 2 and 2.5 nm were deposited on to an $AlO_x/HC_{14}PA$ SAM hybrid gate-dielectric surface by sublimation in vacuum. Immediately after the DNTT deposition, the substrates were removed from the vacuum system, and the morphology of the DNTT films was examined by atomic force microscopy (AFM). Fig.7.1 shows the AFM images of nominally 1, 1.5, 2 and 2.5 nm thick DNTT films, each obtained within 15 minutes of deposition. The AFM images indicate that a nominal thickness of 1 nm results in disconnected islands, and although the islands appear to be progressively more connected for nominal thicknesses of 1.5 and 2 nm, a closed film is clearly identified only for a nominal thickness of 2.5 nm.

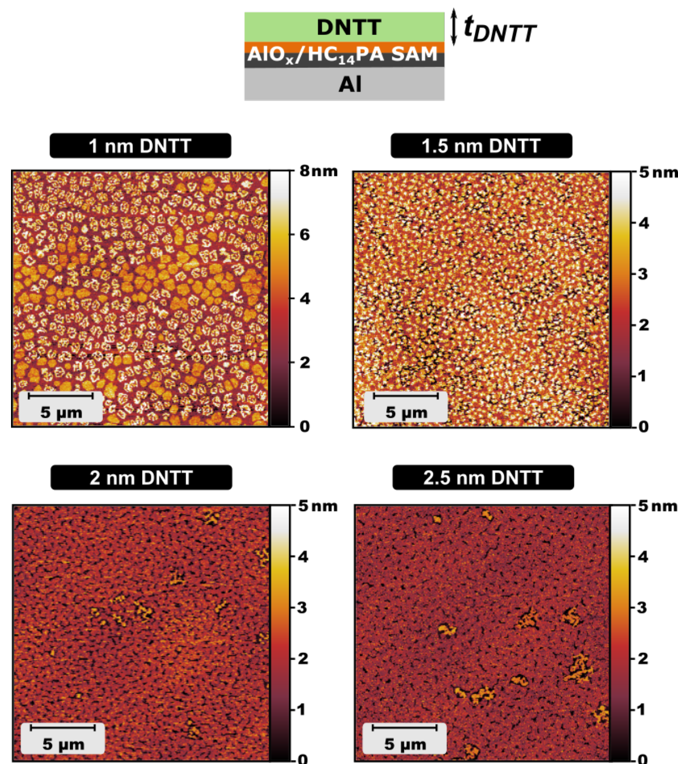


Figure 7.1: Thin-film morphology of DNTT films with nominal thicknesses of 1, 1.5, 2 and 2.5 nm deposited onto a hybrid $AlO_x/HC_{14}PA$ SAM gate dielectric, observed by AFM within 15 minutes after completion of the DNTT deposition

Based on these results, the minimum nominal thickness for DNTT ultrathin films was chosen to be 2.5 nm. Based on the fact that the DNTT molecules have a length of approximately 1.6 nm [72] and stand approximately upright on an electrically insulating surface (as confirmed by the height profile shown in Appendix A), a nominal thickness of 2.5 nm corresponds to less than two complete molecular monolayers. As the nominal DNTT thickness is increased from 1.0 to 2.5 nm, the RMS surface roughness decreases from 1.86 nm to 0.69 nm (as measured by AFM), indicating a more planar and uniform film morphology with increasing nominal thickness.

7.1.2 Temporal changes in the morphology of ultrathin DNTT films

Having determined the minimum nominal DNTT thickness required for functional TFTs to be 2.5 nm, the time-dependent changes in the morphology of these films were monitored. For this purpose, AFM images were recorded on a nominally 2.5 nm-thick DNTT film in a quasi-continuous manner by repeatedly scanning the same area on the surface of the DNTT film over a period of 12 hours. This made it possible to observe the process of the spontaneous structural reconfiguration essentially in real time.

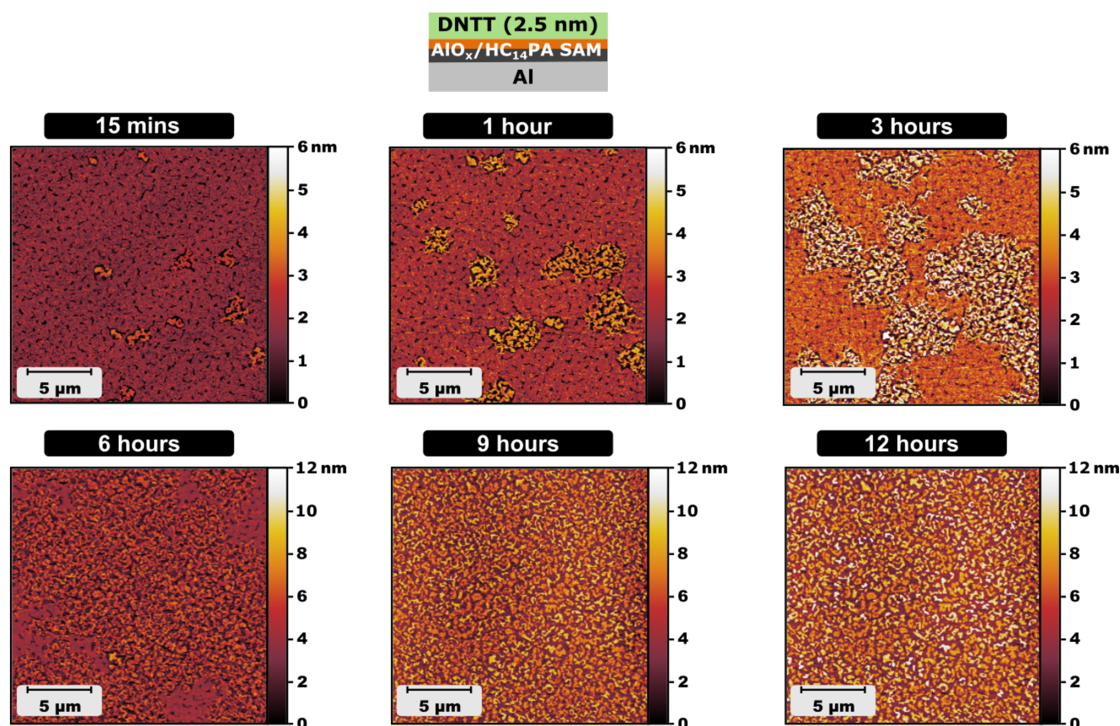


Figure 7.2: Spontaneously occurring morphological changes in a DNTT film with a nominal thickness of 2.5 nm deposited onto a hybrid $AlO_x/HC_{14}PA$ SAM gate dielectric, observed by AFM over a period of 12 hours

Fig.7.2 shows six snapshots obtained in intervals of three hours, with the first image taken within 15 minutes after completion of the DNTT deposition. To rule out that the morphological changes seen in these AFM images were caused by the force of the AFM tip, an identical substrate was prepared on which AFM images were taken only at 15 minutes after completion of the DNTT deposition and again at 12 hours after deposition, and these images indicate the same time-dependent changes in the morphology of the DNTT films. The AFM images confirm the spontaneous rearrangement of the ultrathin DNTT films, as reported by Breuer et al [267]. The maximum height of the DNTT film evolves from 3.18 nm (about 2 molecular monolayers), 15 minutes after deposition to 10.9 nm (about 6 to 7 molecular monolayers), 12 hours after deposition. The root-mean-square surface roughness increases from 0.69 to 2.61 nm (as measured by AFM) in the same duration. This increase in the maximum height and RMS surface roughness is accompanied by the appearance of tall, disconnected islands and by a substantial reduction of the surface coverage, i.e. by the appearance of larger and larger areas of the gate-dielectric surface not covered with DNTT molecules.

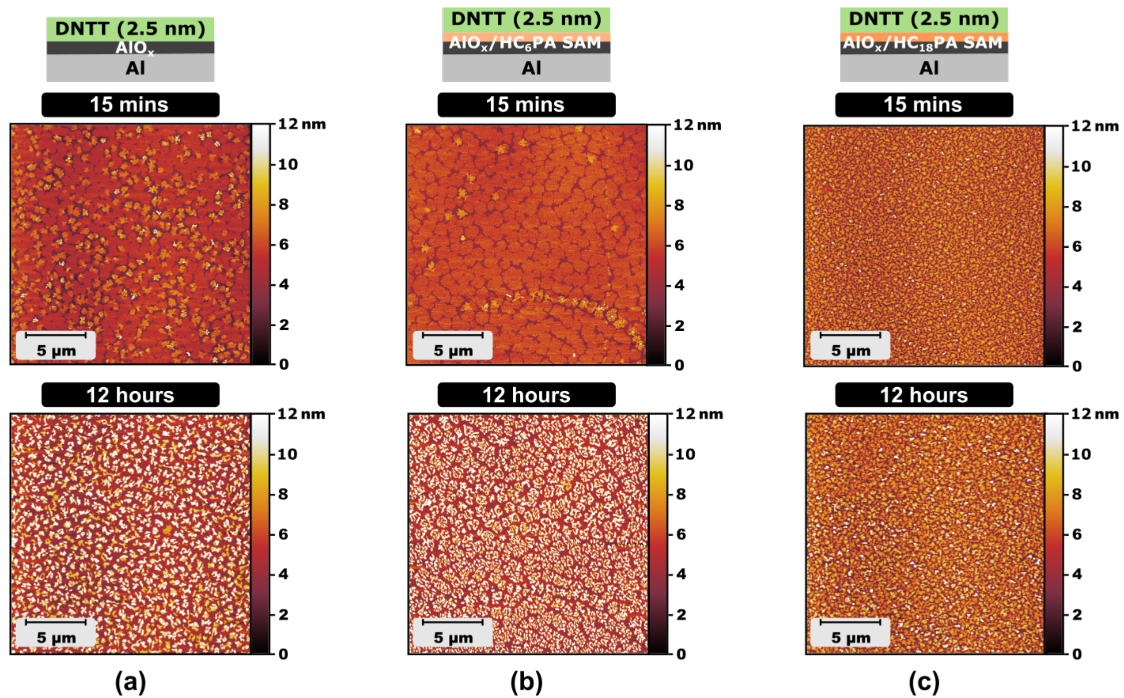


Figure 7.3: Evolution of the morphology of nominally 2.5-nm-thick DNTT films deposited onto (a) bare AlO_x (without SAM); (b) AlO_x/HC_6PA SAM (c) $AlO_x/HC_{18}PA$ SAM. The AFM images were recorded within 15 minutes after the completion of the DNTT deposition and again after 12 hours

The measurements in Fig.7.2 were performed on a DNTT film deposited onto an $AlO_x/HC_{14}PA$ SAM gate-dielectric surface, as this was determined to be the optimum choice of SAM

for TFT performance and the growth of the semiconductor in Chapter 6. Since morphological changes in ultrathin DNTT films were previously also observed on other insulating surfaces, it was necessary to observe ultrathin DNTT films on other gate-dielectric surfaces relevant to organic TFTs. DNTT films with a nominal thickness of 2.5 nm were deposited onto bare AlO_x, and two hybrid gate-dielectric surfaces with the shortest and longest available alkyl phosphonic acid SAMs: AlO_x/HC_6PA SAM and $AlO_x/HC_{18}PA$ SAM, and the morphological changes over time were observed in a similar way. The results are summarized in Fig.7.3. Although there are some differences in the initial morphology of the ultrathin DNTT films on these surfaces, as is already detailed in Chapter 6, the morphological changes in the ultrathin DNTT films are quite similar, suggesting that they are not significantly affected by the surface energy of the substrate. As it has been suggested in previous reports which have studied similar morphological changes in ultrathin organic-semiconductor films, the reorganization of the molecules occurs due to the relatively stronger molecule-molecule interactions as compared to the substrate-molecule interactions. Therefore, in order for the substrate to influence the morphological changes towards stabilizing the organic-semiconductor monolayer, the substrate-molecule interactions would have to be stronger than those observed for the gate-dielectric surfaces considered in Fig.7.3. However, it must also be noted that with stronger substrate-molecule forces, there is a high probability of the organic-semiconductor molecules adopting a horizontal orientation, parallel to the substrate, which is not conducive to charge transport in organic TFTs.

7.1.3 Influence of the changes in the DNTT thin-film morphology on TFT characteristics

To investigate how the spontaneous morphological changes in the DNTT films described above affect the performance of TFTs in which such films serve as the semiconductor, organic TFTs were fabricated in the inverted coplanar (bottom-gate, bottom-contact) architecture. This TFT configuration was particularly chosen so that the deposition of the organic semiconductor is the last step in the TFT fabrication process, and that the TFTs can be electrically measured on the same time scale as the morphological changes occurring in the semiconductor films.

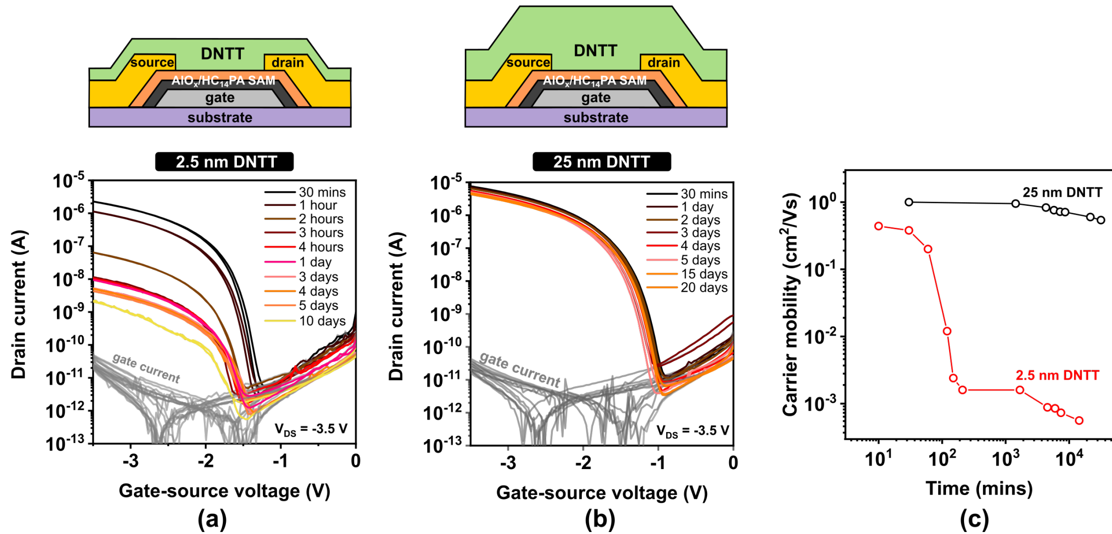


Figure 7.4: Influence of the nominal thickness of vacuum-deposited DNTT films on the evolution of the electrical characteristics of TFTs based on these films (a) Measured transfer curves of TFTs with an ultrathin DNTT film (nominal thickness of 2.5 nm) measured repeatedly over a period of 10 days after TFT fabrication (b) Transfer curves of TFTs with a thick DNTT film (nominal thickness of 25 nm) measured over a period of 20 days after fabrication. (c) Evolution of the effective charge-carrier mobility extracted from the measured transfer curves

The organic TFTs were fabricated with two different thicknesses of the DNTT semiconductor films, nominally 2.5 nm and 25 nm-thick films to compare the effect of the morphological changes in the ultrathin films with the relatively stable thick films on the electrical characteristics of organic TFTs, with the results summarized in Fig.7.4. The initial TFT characteristics for both TFTs are quite similar, with effective charge-carrier mobilities and threshold voltages of 0.4 cm^2/Vs and -1.5 V for a nominal DNTT thickness of 2.5 nm and 1 cm^2/Vs and -1.7 V for a nominal DNTT thickness of 25 nm. This confirms that it is indeed possible to fabricate functional TFTs based on vacuum-deposited DNTT films with a nominal thickness of less than two molecular monolayers. However, the evolution of the effective charge-carrier mobility, as shown in Fig.7.4(c), is dramatically different for the two nominal DNTT thicknesses. While the effective charge-carrier mobility of the TFTs with the thick DNTT film decreases by less than 20% over a period of 20 days, the effective carrier mobility of the TFTs with the ultrathin DNTT film decreases far more rapidly and far more dramatically, from initially 0.4 to 0.0007 cm^2/Vs (a 99.9% decrease) within the first five days. The rapid decrease of the effective charge-carrier mobility of the TFTs with the ultrathin DNTT film seen in Fig.7.4(c) is consistent with the rapid reduction of the surface coverage of the semiconductor and the degree of percolation through the ultrathin DNTT film during the

spontaneous rearrangement of the initially closed (or at least connected) ultrathin film into disconnected islands seen in Fig.7.2. Although the morphological changes commence immediately after the completion of the DNTT deposition, their cumulative impact on the surface coverage and the degree of percolation appears to be most pronounced during the period between about one hour and about six hours after the DNTT deposition, which explains the observation that the drop in the effective charge-carrier mobility is most prominent during this period. The results confirm the severe impact of the spontaneous morphological changes of ultrathin DNTT films reported by Breuer et al. [267] on the effective charge-transport characteristics of organic TFTs based on the ultrathin DNTT films.

The thick DNTT films, with a nominal thickness of 25 nm, are far more stable than the ultrathin DNTT films, both in terms of the film morphology as observed by AFM, as seen in Fig.7.5, and in terms of the electrical TFT characteristics, as seen in Fig.7.4(b). This was already reported by Breuer et al. [267] and indicates that the spontaneous disaggregation of the first molecular monolayer into disconnected islands seen in Fig.7.2 is effectively prevented when this first molecular monolayer is covered with a sufficient amount of additional material.

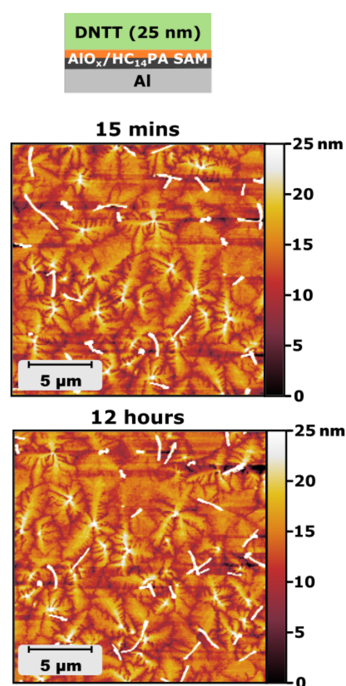


Figure 7.5: Morphology of a nominally 25-nm-thick thick DNTT film deposited onto a hybrid $AlO_x/HC_{14}PA$ SAM surface. The AFM images were recorded within 15 minutes after the completion of the DNTT deposition and again after 12 hours

7.2 Effect of cryogenic cooling of ultrathin DNTT films

To confirm that the spontaneously occurring mass transport within the ultrathin DNTT films that leads to the disaggregation of the initially closed monolayer is indeed thermally activated, a substrate with an ultrathin DNTT film was cooled to a temperature of 193 K in dry nitrogen, immediately after completion of the DNTT deposition and stored at this temperature for a duration of 18 days[1]. Prior to cooling the substrate, the morphology of the film was recorded immediately after deposition, as shown in Fig.7.6. After cryogenic cooling for 18 days, the morphology of this ultrathin film was recorded immediately after allowing the substrate to warm up to room temperature, shown in Fig.7.6(b). An identical substrate with an identical ultrathin DNTT film served as a reference on which an AFM image was recorded immediately after the DNTT deposition and which was kept in ambient air at room temperature for a period of two weeks, after which another AFM image was taken, shown in Fig.7.6(c).

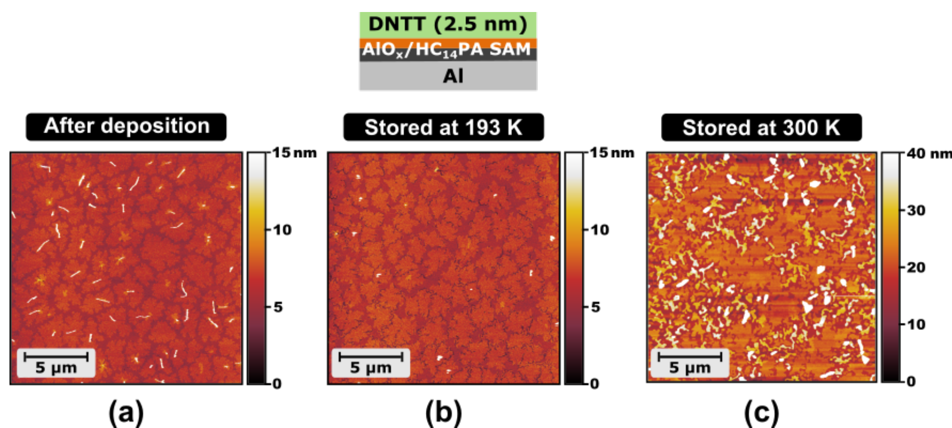


Figure 7.6: Effect of cryogenic cooling on the spontaneously occurring morphological changes in ultrathin DNTT films, observed by AFM at room temperature (a) DNTT morphology immediately after completion of the DNTT deposition (b) DNTT morphology after the substrate had been stored at a temperature of 193 K for 18 days (c) DNTT morphology on a reference substrate stored at room temperature for two weeks

Immediately after the DNTT deposition, the DNTT ultrathin film indicates the initial closed-monolayer morphology (with a second monolayer seen as yet-disconnected islands). Fig.7.6(b) confirms that this closed-monolayer morphology is perfectly preserved during storage at a cryogenic temperature for 18 days. For comparison, the reference substrate as seen in Fig.7.6(c), which was stored at room temperature in ambient air,

[1]The cryogenic cooling and AFM imaging thereafter were performed by Tobias Breuer and Darius Günder at the Philipps-Universität Marburg.

shows the break-up of the initially closed DNTT monolayer into tall, disconnected islands. This effect and similar morphological changes were also observed on the substrate that had been stored at a cryogenic temperature within less than a day after it had been returned to room temperature. These observations strongly support the hypothesis that these morphological changes in the ultrathin DNTT films are indeed thermally activated.

7.3 In-situ encapsulation of ultrathin DNTT films

As discussed previously, the morphological changes in the ultrathin DNTT films proceed by lateral and vertical mass transport that causes a rearrangement of the initially closed (or at least connected) single-monolayer-thick films into disconnected islands. While the results in Fig.7.6 confirm that this mass transport is indeed thermally activated, the results in Fig.7.4(b) and Fig.7.5 show that it can be prevented by covering the ultrathin films with additional material (in the case of Fig.7.5 with additional DNTT). The following sections explore the extent to which this can also be accomplished using encapsulation materials other than DNTT. The choice of encapsulation materials is dictated by the requirement to deposit the encapsulation immediately (within one to two minutes) following the completion of the deposition of the ultrathin DNTT film in the same vacuum-deposition system and without breaking the vacuum. The requirement of encapsulating the ultrathin DNTT films without breaking vacuum is based on the time-delay and subsequent morphological changes in the films during changing the vacuum system, and not related to any influence of vacuum or air exposure on the morphological changes themselves. This ruled out virtually all popular organic-TFT-encapsulation materials, such as Al_2O_3 [276], Cytop [277] and parylene [278], as none of these can be deposited in the vacuum-deposition system in which the DNTT films are deposited. The three materials selected for the in-situ encapsulation of ultrathin DNTT films are polytetrafluoroethylene (PTFE), C_{60} and titanyl phthalocyanine (TiOPc).

7.3.1 Encapsulation using vacuum-deposited polytetrafluoroethylene (PTFE)

Polytetrafluoroethylene (PTFE) is a synthetic fluoropolymer available as a powder that can be deposited by thermal sublimation in vacuum. PTFE is an excellent electrical

insulator and has been used previously to encapsulate pentacene TFTs [279]. PTFE films with a nominal thickness of either 2.5 nm or 10 nm were deposited directly onto ultrathin DNTT films having a nominal thickness of 2.5 nm. The PTFE deposition was started within one to two minutes after completion of the DNTT deposition in the same vacuum-deposition system without breaking vacuum, by using one sublimation source for the DNTT deposition and another for the PTFE deposition.

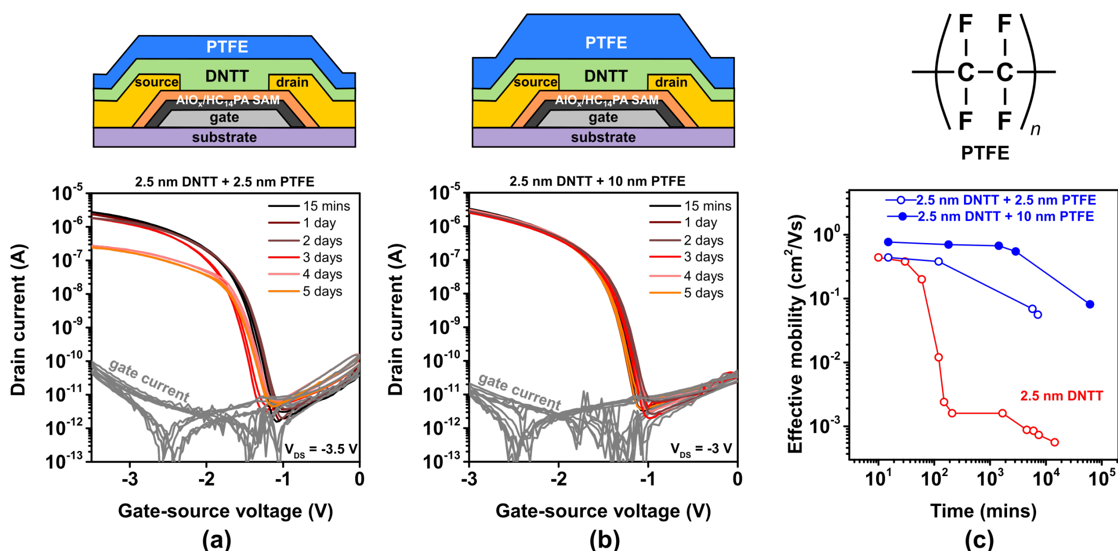


Figure 7.7: Effect of in-situ encapsulation of ultrathin, vacuum-deposited DNTT films (having a nominal thickness of 2.5 nm) with vacuum-deposited PTFE on the evolution of the TFT characteristics. Transfer curves of TFTs encapsulated with a nominally (a) 2.5 nm-thick and (b) 10 nm-thick PTFE film, measured repeatedly over a period of 5 days after TFT fabrication (c) Evolution of the effective charge-carrier mobility extracted from the measured transfer curves

The results of the TFT measurements are summarized in Fig.7.7. As can be seen, the initial TFT characteristics are not significantly affected by the PTFE encapsulation, but the degradation of the charge-carrier mobility is notably decelerated by the PTFE encapsulation, especially for the larger PTFE thickness (10 nm). However, even with the nominally 10 nm-thick PTFE encapsulation, the charge-carrier mobility of the TFTs still decreases by approximately one order of magnitude (from 0.8 to 0.08 cm^2/Vs) within two months. Analysis of thin PTFE films deposited onto surfaces other than DNTT suggests that PTFE films also undergo morphological changes, and assuming these changes also occur in PTFE films deposited onto DNTT, this might explain the limited effectiveness of the PTFE encapsulation observed here. Nevertheless, as it is apparent that increasing the PTFE thickness from 2.5 to 10 nm increases the encapsulation effectiveness, PTFE

encapsulation with a nominal thickness of more than 10 nm was also attempted. However, this turned out to be quite challenging and prohibitively time-consuming in the deposition system, due to the unfavorable combination of the high vapor pressure of the PTFE powder and the limited through-put of the vacuum pump.

7.3.2 Encapsulation using vacuum-deposited C_{60}

As an alternative to PTFE, C_{60} was also tested for the encapsulation of ultrathin DNTT films. The vapor pressure of C_{60} is substantially smaller than that of PTFE, so that thick C_{60} films can be easily deposited by sublimation in vacuum. Other potential benefits of C_{60} for the purpose of encapsulating ultrathin DNTT films are the superior thermal and mechanical stability of C_{60} films [280] and the fact that C_{60} does not form undesirable Diels–Alder adducts with DNTT [281]. A substantial drawback of C_{60} for this purpose is the fact that it is an electron-transporting semiconductor and thus expected to adversely affect the current–voltage characteristics of the DNTT TFTs, especially their off-state behavior, due to the uncontrollable flow of electrons from the drain contact through the C_{60} film to the source contact. C_{60} films with a nominal thickness of either 2.5 nm or 25 nm were directly deposited onto ultrathin DNTT films having a nominal thickness of 2.5 nm.

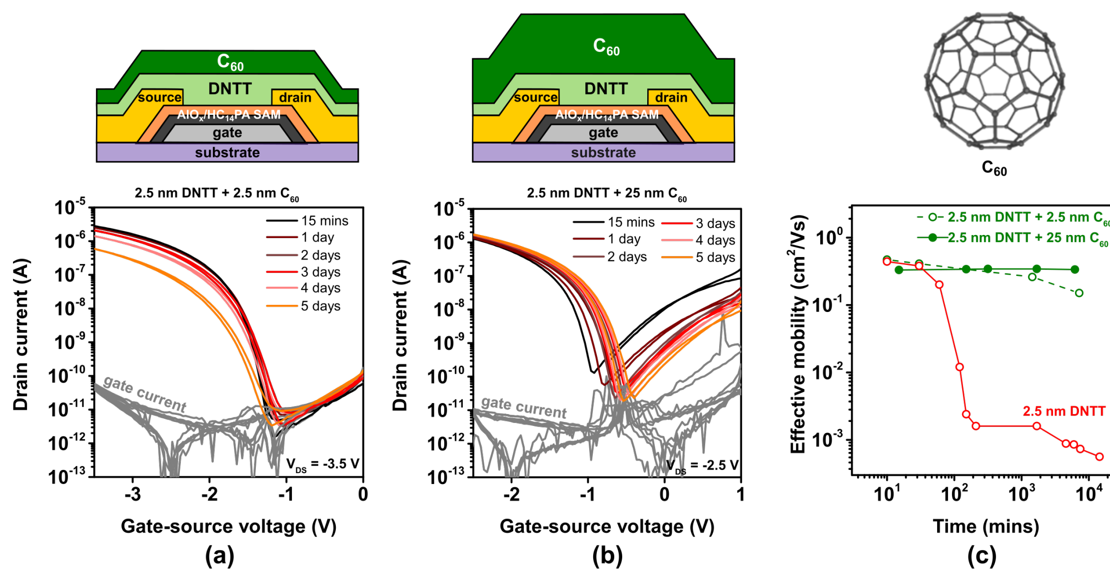


Figure 7.8: Effect of in-situ encapsulation of ultrathin, vacuum-deposited DNTT films (having a nominal thickness of 2.5 nm) with vacuum-deposited C_{60} on the evolution of the TFT characteristics. Transfer curves of TFTs encapsulated with a nominally (a) 2.5 nm-thick and (b) 25 nm-thick C_{60} film, measured repeatedly over a period of 5 days after TFT fabrication (c) Evolution of the effective charge-carrier mobility extracted from the measured transfer curves

The results are summarized in Fig.7.8. As can be seen in Fig.7.8(b), the deposition of a nominally 25-nm thick film of C_{60} indeed causes ambipolar behavior, which is highly undesirable, as it increases the off-state leakage current of the TFTs and thus the static power consumption and the noise margins of logic circuits based on ambipolar TFTs. However, the degradation of the hole mobility in the ultrathin DNTT film is notably decelerated by the C_{60} encapsulation, which suggests that the morphology of the ultrathin DNTT film is indeed greatly stabilized by the C_{60} encapsulation. A workable compromise between the beneficial effect of stabilizing the morphology of the ultrathin DNTT films and the drawback of increasing the leakage current is the use of a C_{60} encapsulation with a smaller thickness, as shown in Fig.7.8(a). With a nominally 2.5 nm-thick C_{60} encapsulation, the off-state drain current of the ultrathin-DNTT TFTs is approximately 10^{-10} A, which is similar to that of ultrathin-DNTT TFTs without encapsulation (Fig.7.4(a)) or with an electrically insulating encapsulation (Fig.7.7(a)). However, the suppression of the degradation of the hole mobility in the ultrathin DNTT film is not quite as pronounced as in the case of the nominally 25 nm-thick C_{60} encapsulation (Fig.7.8(c)). This is mainly due to the fact that the deposition of nominally 2.5 nm-thick C_{60} does not lead to the formation of a closed C_{60} film on the surface of the ultrathin DNTT film, but rather to edge decoration (similar to previous reports for C_{60} deposited on pentacene [282]).

7.3.3 Encapsulation using vacuum-deposited titanyl phthalocyanine (TiOPc)

TiOPc is a hole-transporting small-molecule semiconductor [283]. TiOPc molecules usually adopt a flat-lying orientation when deposited onto metals [284], but an upright-standing molecular orientation when deposited onto electrically-insulating surfaces or organic-semiconductor films [285]. A potential benefit of TiOPc for the purpose of encapsulating ultrathin DNTT films is its excellent chemical robustness and thermal stability. A drawback of TiOPc for this purpose is that the possibility of hole transport in the TiOPc film in parallel to the ultrathin DNTT film cannot be ruled out. This makes it impossible to monitor the electrical behavior of the DNTT film exclusively. TiOPc films with a nominal thickness of either 2.5 or 25 nm were deposited directly onto ultrathin DNTT films. The results are summarized in Fig.7.9.

The first observation is that the current–voltage characteristics of the ultrathin-DNTT

TFTs with the TiOPc encapsulation (Fig.7.9(a) and (b)) are exactly the same as those of the ultrathin-DNTT TFTs without encapsulation (Fig.7.5(a)).

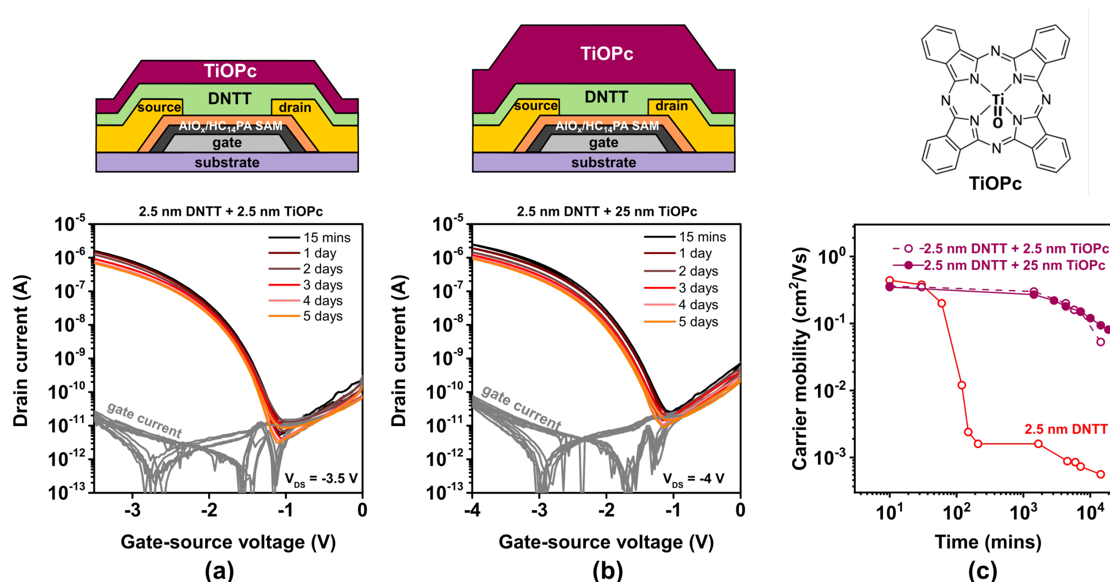


Figure 7.9: Effect of in-situ encapsulation of ultrathin, vacuum-deposited DNTT films (having a nominal thickness of 2.5 nm) with vacuum-deposited TiOPc on the evolution of the TFT characteristics. Transfer curves of TFTs encapsulated with a nominally (a) 2.5 nm-thick and (b) 25 nm-thick TiOPc film, measured repeatedly over a period of 5 days after TFT fabrication (c) Evolution of the effective charge-carrier mobility extracted from the measured transfer curves

This suggests that the TiOPc film does not participate in the charge transport, which is in contradiction to the results reported previously for TFTs based on a heterostructure of ultrathin dihexyl-sexithiophene and TiOPc, but this may be due to the fact that the intrinsic carrier mobility in DNTT is significantly larger than that in both TiOPc and dihexyl-sexithiophene. The second observation is that the TiOPc encapsulation slows down the degradation of the charge-carrier mobility of the TFTs, similar to encapsulation with PTFE and C_{60}. However, in stark contrast to PTFE (Fig.7.7) and C_{60} (Fig.7.8), this effect is virtually independent of the thickness of the TiOPc encapsulation. Nevertheless, the charge-carrier mobility of the TiOPc-encapsulated TFTs still decreases by approximately one order of magnitude within two weeks.

7.3.4 Summary of encapsulation results

The results from the encapsulation experiments are summarized in Fig.7.10. The transfer curves of the TFTs with and without the various encapsulation films recorded within

30 minutes after the last deposition are summarized in Fig.7.10(a). The TFTs with the thick DNTT films (nominal thickness 25 nm) initially have an effective carrier mobility of 1 cm^2/Vs (Fig.7.10(b)), which is similar to previous reports of bottom-gate, bottom contact DNTT TFTs [257]. The effective mobility of these TFTs degrades from 1 to 0.8 cm^2/Vs within 5 days and to 0.5 cm^2/Vs within 23 days (as also seen in Fig.7.5(c)).

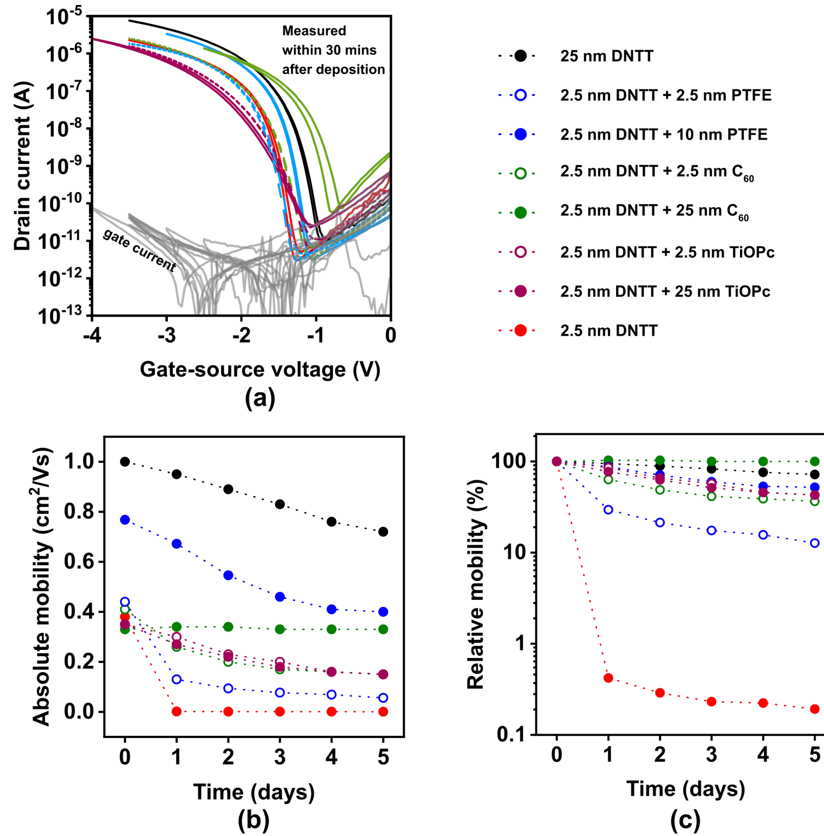


Figure 7.10: (a) Transfer curves of TFTs based on vacuum-deposited DNTT films with nominal thicknesses of 2.5 and 25 nm with and without encapsulation, recorded within 30 minutes after the completion of the last deposition. (b) Absolute value of the effective carrier mobility (c) Effective carrier mobility normalized to the mobility measured immediately after TFT fabrication

This degradation in effective mobility is notably more rapid than the mobility degradation in top-contact DNTT TFTs, but for the experiments described here, it was necessary to fabricate the TFTs in the bottom-contact architecture in order to minimize the delay between the completion of the DNTT deposition and the first measurement of the current–voltage characteristics. The long-term stability of bottom-contact DNTT TFTs has yet to be systematically investigated. The reasons for the relatively rapid degradation of the effective mobility observed here is not known, but it may be related

to a degradation of the interface between the source/drain contacts and the vacuum-deposited DNTT film.

The TFTs with the ultrathin DNTT films (nominal thickness 2.5 nm) initially have effective carrier mobilities between 0.3 and 0.4 cm^2/Vs, regardless of whether they were encapsulated or not and, if so, regardless of the encapsulation material (PTFE, C_{60}, TiOPc) and the nominal thickness of the encapsulation film (Fig.7.10(b)). The only exception is the TFT in which the ultrathin DNTT film was encapsulated with a nominally 10 nm-thick PTFE film, which has a somewhat larger initial mobility (0.7 cm^2/Vs). The reason for this discrepancy is unknown, but it may be the result of unavoidable substrate-to-substrate variations in the fabrication process. The results confirm that it is indeed possible to fabricate functional TFTs based on vacuum-deposited DNTT films with a nominal thickness of less than two molecular monolayers. Encapsulation of these films has a pronounced effect on their stability: while the effective mobility of unencapsulated ultrathin DNTT films decreases by two orders of magnitude within a day, the mobility of encapsulated films decreases by less than one order of magnitude within five days (Fig.7.10(c)). The mechanism by which the encapsulation of the ultrathin DNTT films decelerates the degradation of the carrier mobility in these films is not by protecting the DNTT molecules from ambient air (given the outstanding chemical stability of DNTT during long-term exposure to air and humidity), but by stabilizing the fragile morphology of the ultrathin DNTT films by burying it under a thick film of additional mass. Although it is not possible to inspect the morphology of the aged ultrathin DNTT films buried underneath the thick encapsulation films by AFM measurements, it can be hypothesized that the deceleration of the mobility degradation observed here is a direct result of preventing mass transport within the ultrathin DNTT films by the encapsulation film. This hypothesis is supported by the observation that for two of the three encapsulation materials, thicker encapsulation films provide better stability (Fig.7.10(c)). The interesting question for how long the encapsulation can delay the break-up of the initially closed DNTT monolayer is beyond the scope of the present study.

The choice of the encapsulation material is dictated by a number of considerations. Since the spontaneous structural reconfiguration of the ultrathin DNTT films commences immediately after the DNTT deposition, it is necessary to start the deposition of the encapsulation film immediately after the completion of the DNTT deposition. This limits the choice of encapsulation materials to such materials that can be deposited in the

same high-vacuum system in which the ultrathin DNTT films are deposited, without breaking vacuum and without time-consuming substrate transfers. If the purpose of the experiments is an investigation of the charge transport in ultrathin DNTT films, the choice of encapsulation materials should be limited to materials that do not participate in the charge transport. Of the three materials that have been tested here, this obviously eliminates C_{60} (and possibly also TiOPc, although Fig.7.9 seems to indicate that the TiOPc films do not participate in charge transport). The observation that the stabilizing effect of the encapsulation increases with increasing thickness of the encapsulation film calls for materials that can be easily deposited as thick films. Unfortunately, this essentially eliminates PTFE, due to its unfavorably high vapor pressure.
Another aspect to be considered in the choice of the encapsulation material is the homogeneity and long-term morphological stability of the encapsulation film, which would likely benefit from choosing materials with a higher molecular weight and thus smaller diffusivity on the DNTT surface, and possibly also from performing the deposition of the encapsulation film at cryogenic temperatures to promote homogeneous coverage of the encapsulating material.

7.4 Experimental

7.4.1 Film characterization

Samples for film characterization were prepared on silicon substrates. Silicon was chosen as the substrate to provide the smallest possible surface roughness. Aluminum with a thickness of 30 nm and a root-mean-square surface roughness of less than 1 nm [197] was deposited by thermal evaporation in vacuum at a rate of 2 nm/s. The aluminum surface was exposed to a capacitively coupled oxygen plasma with a partial oxygen pressure of 0.01 mbar and an oxygen flow rate of 30 sccm. The plasma power selected was 200 W and the duration of plasma exposure was limited to 30 s to increase the thickness of the native aluminum oxide (AlO_x) to approximately 6 nm. On some substrates, ultrathin DNTT (Sigma-Aldrich) was deposited directly onto bare AlO_x. On other substrates, a monolayer of $HC_{14}PA$, HC_6PA, or $HC_{18}PA$ (PCI Synthesis, Newbury- port, MA, USA) was allowed to self-assemble on the AlO_x surface by immersing the substrates into a 1 mM-solution of the phosphonic acid in 2-proponal for a duration of 12 hours, after which

the substrates were rinsed with 2-proponal, dried with nitrogen and heated to a temperature of 80 °C for 10 minutes to stabilize the monolayer. DNTT was deposited by thermal sublimation in vacuum at a rate of 2 nm/min (without heating the substrate to avoid the unnecessary acceleration of the morphological changes). AFM images were acquired in tapping mode (in ambient air at room temperature) using a Bruker Nanoscope III MultiModes or an Agilent SPM 5500 and cantilevers with resonance frequencies between 200 and 500 kHz and a typical tip radius of 8 nm.

7.4.2 TFT fabrication and characterization

TFTs were fabricated in the inverted coplanar (bottom-gate, bottom-contact) architecture on silicon substrates coated with 100 nm-thick thermally grown silicon dioxide. This device architecture was chosen to minimize the delay between the completion of the semiconductor deposition and the first measurement of the current–voltage characteristics. Aluminum gate electrodes with a thickness of 30 nm were deposited by thermal evaporation in vacuum at a rate of 2 nm/s. The gate dielectric consists of a thin, oxygen-plasma-grown film of AlO_x and a solution-processed $HC_{14}PA$ SAM and has a capacitance of about 0.7 $\mu F/cm^2$. For the source and drain contacts, titanium with a thickness of 0.2 nm (to improve adhesion) and gold with a thickness of 30 nm were sequentially deposited by thermal evaporation in vacuum. To minimize the contact resistance, the surface of the Au source/drain contacts was functionalized with a monolayer of pentafluorobenzenethiol (PFBT). DNTT was deposited by thermal sublimation in vacuum (base pressure 10^{-6} mbar; substrate temperature 20 °C) at a rate of 2 nm/min. PTFE (Sigma-Aldrich, free- flowing powder, particle size < 12 mm), C_{60} (Sigma-Aldrich) or TiOPc (Sigma-Aldrich) encapsulation films were deposited by thermal sublimation in vacuum within one to two minutes after completion of the DNTT deposition. Deposition rate and nominal thickness of all vacuum-deposited films were measured using a quartz-crystal microbalance positioned in close proximity to the substrate holder. Gate electrodes, source/drain contacts, organic semiconductor and encapsulation films were all patterned using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany). The TFTs have a channel length of 20 μm and a channel width of 100 μm. The electrical measurements were performed in ambient air at room temperature using a manual probe station and an Agilent 4156C Semiconductor Parameter Analyzer. The first measurement was performed within 15 minutes after the completion

of the last vacuum deposition, and the substrates were stored in ambient air at room temperature between measurements.

7.5 Summary and Outlook

The thickness of the organic-semiconductor layer is an important parameter towards understanding the operation of organic TFTs and their further development. Ultrathin films of organic semiconductors are particularly significant, as the conductive channel in organic TFTs is limited to the first few monolayers of the semiconductor, in close proximity to the gate dielectric. The spontaneous occurring morphological changes in the thin-film morphology of vacuum-deposited ultrathin DNTT films have been observed by AFM. The influence of this spontaneous structural reconfiguration on the electrical characteristics of TFTs based on such films has been analyzed. The results confirm that the observed transition from an initially closed (or at least connected) monolayer to tall, isolated islands and the associated loss of percolation through the films cause a rapid and substantial degradation of the effective charge-carrier mobility of the TFTs. Of the available gate-dielectric surfaces studied in this thesis, including bare-AlO_x and several different phosphonic acid SAMs, a similar progression of the morphological changes can be seen in ultrathin DNTT films. Whether the structural reconfiguration of ultrathin DNTT films has to be prevented by changing the type of the substrate, gate-dielectric materials with functional groups similar to the chemical structure of the organic semiconductor will have to be considered. For example, phosphonic acid molecules containing benzyl functional groups will potentially increase the substrate-molecule interactions and possibly stabilize the ultrathin DNTT films.

In this work, the morphological changes observed in ultrathin DNTT films were controlled using cryogenic cooling and in-situ encapsulation. By showing that the morphological changes are prevented by keeping the substrates at cryogenic temperatures, it has been confirmed that this structural reorganization is indeed thermally activated. The extent to which encapsulation of ultrathin DNTT films is able to stabilize the morphology has been tested using three different materials: PTFE, C_{60} and TiOPc. Although the morphological changes were not stopped entirely, it has been shown that in-situ encapsulation can slow the rate of degradation quite significantly. The ability to fabricate TFTs based on vacuum-deposited ultrathin organic–semiconductor films with sufficient

long-term stability is potentially of interest for interface and charge-transport investigations. Future investigations could lead to the further improvement of the stability and performance of ultrathin organic TFTs. These include investigating other materials as potential encapsulation materials which meet the requirements of encapsulation in ultrathin organic TFTs and which provide a higher stability to the ultrathin semiconductor films. The ultrathin organic TFTs in this work were fabricated in a bottom-gate, bottom-contact (inverted coplanar) configuration, in order to encapsulate the ultrathin DNTT films, while still maintaining contact with the source and drain contacts. In the currently available device fabrication techniques, it is not possible to fabricate ultrathin organic TFTs in the top-contact configuration with simultaneous contact with the electrodes as well as encapsulation. Since the inherent stability of top-contact organic TFTs is higher than that of bottom-contact organic TFTs, top-contact TFTs with a new fabrication technique and design in which the source-drain contacts are deposited sequentially at the end and are still in contact with the ultrathin semiconductor films with in-situ encapsulation would further improve the stability of ultrathin organic TFTs. These efforts would be advantageous towards the development of highly sensitive chemical or biological sensors due to the benefits of ultrathin organic TFTs.

Chapter 8

Conclusion

Organic semiconductors are a widely researched class of materials due to their unique properties such as low-temperature processing and targeted synthesis to develop electronic devices such as organic light-emitting diodes and organic thin-film transistors (TFTs). Organic TFTs in particular, are being developed for flexible electronics applications, such as rollable displays, conformable sensors and electronic skin. Among the many electrical characteristics, an important requirement for organic TFTs is low-voltage operation, for the realization of portable or wearable applications. The operating voltage of the TFT is determined by the gate-dielectric capacitance, and ultrathin, hybrid gate dielectrics are an excellent choice for high-capacitance gate dielectrics. Hybrid gate dielectrics are extremely advantageous in simultaneously achieving a low operating voltage as well a a low leakage current in organic TFTs. This thesis investigates hybrid gate dielectrics with two components, an ultrathin aluminum oxide (AlO_x) film in combination with an organic self-assembled monolayer (SAM). In this thesis, the different components of the hybrid gate dielectric, the organic semiconductor layer as well as the gate dielectric-semiconductor interface have been investigated and their material properties have been correlated to the electrical properties of organic TFTs.

The first component of the hybrid gate dielectric, the AlO_x film, is fabricated by exposing the surface of the underlying aluminum gate electrode to a capacitively-coupled oxygen plasma in a self-limiting growth process. The plasma-oxidation process has several benefits for the fabrication of organic TFTs, including but not limited to producing a self-patterned, ultrathin and dense AlO_x film with a high-quality interface with the underlying aluminum gate electrode. In the absence of the plasma-oxidation process,

the native aluminum oxide on the underlying aluminum gate is an insufficient and inadequate gate oxide and leads to organic TFTs with suboptimal electrical characteristics. The AlO_x film has several critical roles in the hybrid gate dielectric and the overall electrical performance of organic TFTs. By virtue of the plasma process, the AlO_x film provides a suitable surface for the SAM to adsorb onto and thus ensures a low leakage current through the gate dielectric.

The thin-film properties of the plasma-oxidized AlO_x film, namely the thickness and the chemical composition were investigated. The thickness of the film was measured using transmission electron microscopy and was varied between 4 nm and 7 nm, depending on the plasma power and the duration of plasma exposure during the fabrication process. In particular, for a plasma power of 200 W and a plasma duration of 30 s, the thickness of the AlO_x film was determined to be about 6.5 nm. By measuring the thickness and the gate-dielectric capacitance of different AlO_x films fabricated using different process parameters, the relative permittivity of the plasma-oxidized AlO_x was determined to be approximately 8. These properties are crucial to the dielectric properties of the AlO_x films, and a process to fabricate AlO_x films with a particular thickness makes it possible to deterministically control the gate-dielectric capacitance, and in turn the operating voltage of the TFT. In this work, the gate-dielectric capacitance of AlO_x gate dielectrics was varied between 1 and 1.6 $\mu F/cm^2$ by varying the plasma power and plasma duration. The fabrication of AlO_x films thinner than 4 nm or thicker than 7 nm, by further varying the plasma-process parameters or other aspects of the plasma process, might potentially grant a better and more precise control of the gate-dielectric capacitance and the operating voltage.

Along with the thickness of the AlO_x film, the thin-film composition was also investigated. Using electron energy loss spectroscopy, the presence of elemental aluminum and oxygen was spatially mapped in an Al/AlO_x layer configuration. With the help of atom probe tomography, a three-dimensional reconstruction of the Al/AlO_x films was obtained with an atomic-scale resolution. Based on these measurements, the thin-film composition can be qualitatively assessed and resembles stoichiometric Al_2O_3 films. However, further efforts with the measurement parameters of these techniques, or alternative analytical ones, are required to quantitatively determine the chemical composition of the plasma-oxidized AlO_x films. Fabricating perfectly stoichiometric Al_2O_3 films with the plasma-oxidation process will ideally improve the electrical characteristics of organic TFTs.

Apart from the thickness of the AlO_x films, the oxygen-plasma process was instrumental in tailoring several other material and thin-film properties, which influence the electrical properties of organic TFTs. The most important impact of the plasma power and the plasma duration was observed on the surface roughness of the AlO_x films. An optimum surface roughness, of approximately 0.52 nm, was obtained for a combination of medium plasma powers (100-200 W) and medium plasma durations (30-60 s), which facilitated an optimum organic-semiconductor morphology and high charge-carrier mobilities in the organic TFTs. The exact mechanism behind modifying the surface roughness of the metal oxide film using an oxygen plasma will need further investigation. It was also observed that long plasma exposure times ($\geq$ 1800 s) lead to thicker AlO_x films with a damaged surface unsuitable for organic semiconductors to be deposited onto, despite a lower surface roughness. Further characterization of these films beyond the parameter of surface roughness would improve the understanding of the influence of the plasma-oxidation process on the surface properties of AlO_x films.

Self-assembled monolayers (SAMs) are molecular assemblies of individual molecules which adsorb on a suitable surface and align themselves into a monolayer film through Van der Waals interactions. SAMs have been a popular choice in hybrid gate dielectrics and provide a variety of advantages for the properties of organic TFTs. Phosphonic acid molecules of two different aliphatic chains, an unsubstituted alkyl chain and a functionalized fluoroalkyl chain, were assembled from solution to form the SAM on the plasma-oxidized AlO_x films. Several benefits of employing SAMs in the hybrid gate dielectric were observed throughout this work. A leakage current density of the order of 10^{-11} A was achieved for organic TFTs operating at a supply voltage as low as 3 V. Compared to organic TFTs with bare-AlO_x gate dielectrics, the TFTs with hybrid AlO_x/SAM gate dielectrics had higher charge-carrier mobilities, due to the contribution of the SAM in screening polaronic charges and providing a suitable surface for the growth of the organic semiconductor. The organic semiconductor DNTT was used to fabricate TFTs with alkyl as well as fluoroalkyl phosphonic acid SAMs and a threshold-voltage shift was observed in the organic TFTs with the two different SAMs. The fluoroalkyl phosphonic acid SAMs were used in combination with the organic semiconductor DPh-BTBT for fabricating ultralow-voltage organic TFTs.

The most important aspect of the SAMs studied in this work is the thickness of the SAM as a function of the chain length of the phosphonic acid molecule. By employing molecules of different chain lengths, electrical characteristics of the organic TFTs such

as the gate-dielectric capacitance, the charge-carrier mobility, the subthreshold swing and the current on-off ratio were modified. In particular, the chain length of the phosphonic acid molecules was instrumental in modifying the gate-dielectric capacitance of hybrid gate dielectrics, which is not possible by varying the thickness of the AlO_x film. An optimum electrical performance in terms of the TFT characteristics was obtained for the medium-chain-length phosphonic acids of the available range of molecules, i.e. $HC_{10}PA$-$HC_{14}PA$ and $FC_{10}PA$ SAMs.

With the formation of the SAM on the AlO_x surface, the surface energy of the hybrid gate dielectric can be modified, and the hydrophilic AlO_x surface can be modified into a preferable, hydrophobic surface. In addition, the surface energy of the hybrid gate dielectric can be further varied as a function of the type of the phosphonic acid molecule as well as its chain length. Apart from the surface energy, the properties of the SAM as a function of the chain length affect the growth and morphology of the organic semiconductor deposited onto the surface. Although no direct correlation was made with the growth pattern of the semiconductor DNTT and the surface energy of the phosphonic acid SAMs, it was identified that an optimum growth mode is obtained for DNTT deposited on the $HC_{14}PA$ SAM, i.e. an island-layer type of growth with maximum semiconductor coverage obtained in the initial monolayers during the growth process. A preferred growth mode of the semiconductor as well as a large density of grain boundaries in the thin-film morphology were correlated with a large charge-carrier mobility in the organic TFTs.

The influence of the surface properties at the gate dielectric-semiconductor interface, on the film properties of the organic semiconductor are thus established. Depending on the surface roughness of the AlO_x film, the surface energy of the SAM and the type of the phosphonic acid molecule forming the SAM, an optimum growth mode and morphology of the organic semiconductor was determined and correlated with high charger-carrier mobilities in the organic TFTs. A further investigation of the film properties of the SAM and the hybrid gate dielectric, beyond the surface roughness and the surface energy, is required. Particularly, the packing density and molecular ordering of individual molecules within the SAM will promote the deposition of high-quality organic semiconductor films. Extending the observations made for the organic semiconductor DNTT in terms of the optimum SAM to other organic semiconductors will also benefit the development of organic TFTs.

The part of the semiconductor layer in close proximity to the gate dielectric is extremely

crucial because the conducting channel in the transistor is located in this region. Ultrathin films of the organic semiconductor, of the order of one or two molecular monolayers, were investigated. It was observed that ultrathin films undergo rapid structural reorganization and morphological changes in which an initially closed or connected monolayer develops into individual, disconnected islands over time. Functional organic TFTs with ultrathin organic semiconductor films were fabricated, and a drastic decrease in the charge-carrier mobility with time was observed and correlated with the morphological changes observed. The ultrathin semiconductor films were partially stabilized by cryogenic cooling and in-situ encapsulation using different encapsulation materials, which showed that encapsulation is a promising concept and investigating other encapsulation materials along with exploring new device configurations will further improve the stability of ultrathin organic TFTs and their development for a variety of sensors and studying device physics.

Due to the construction of organic TFTs with different materials deposited in the form of thin films and a variety of material combinations, fabrication methods and process parameters, it is extremely important to establish a relationship between the material properties of the different components and the electrical properties of the organic TFTs. The gate dielectric, the organic semiconductor and the interface between the two has been studied in detail in this thesis. The essential relationship between the thin-film and surface properties of the gate dielectric, morphology of the organic semiconductor and the electrical properties of the organic TFT was established. Extending the understanding of this relationship to other materials and processes will advance the development of organic thin-film transistors and promote the realization of unique electronic applications.

Appendix A

Additional characterization of DNTT films

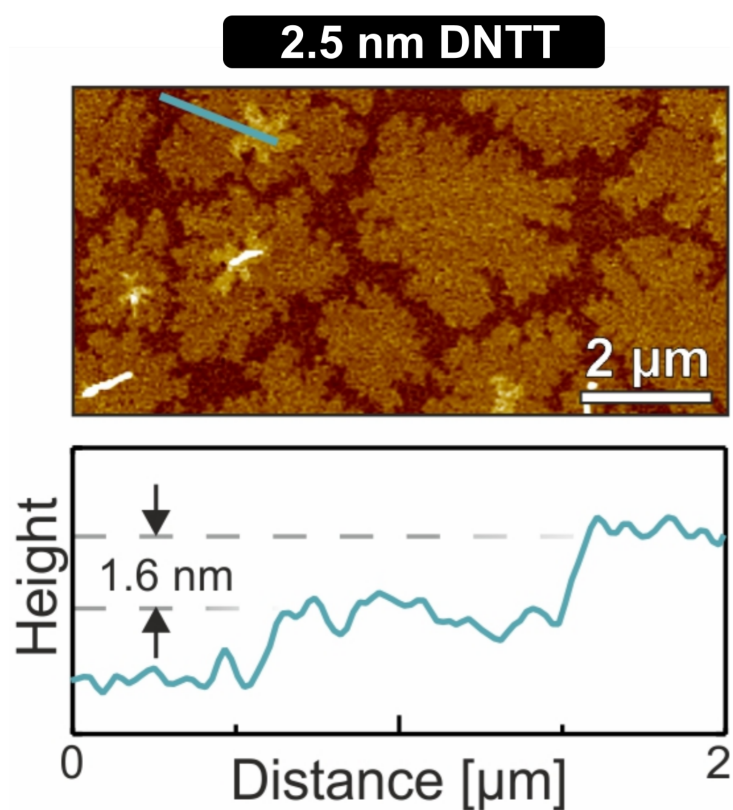


Figure A.1: AFM image depicting the morphology of a nominally 2.5-nm-thick DNTT film deposited onto a hybrid $AlO_x/HC_{14}PA$ SAM gate dielectric, and the height profile indicating a characteristic step height of 1.6 nm, confirming that the DNTT molecules stand approximately upright on the substrate surface

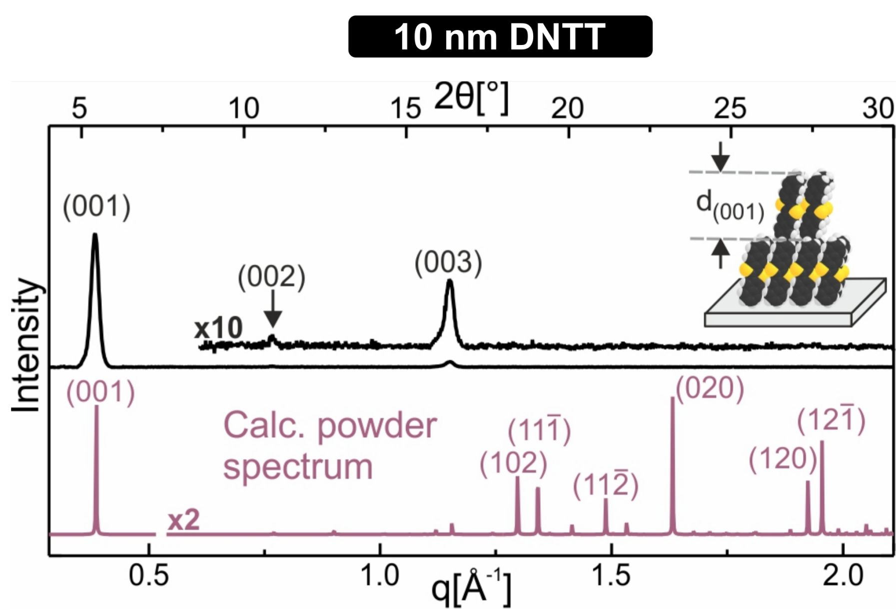


Figure A.2: Specular X-ray diffractogram of a nominally 10-nm-thick DNTT film deposited onto a hybrid $AlO_x/HC_{14}PA$ SAM gate dielectric together with a calculated powder spectrum. The inset schematically depicts the molecular arrangement

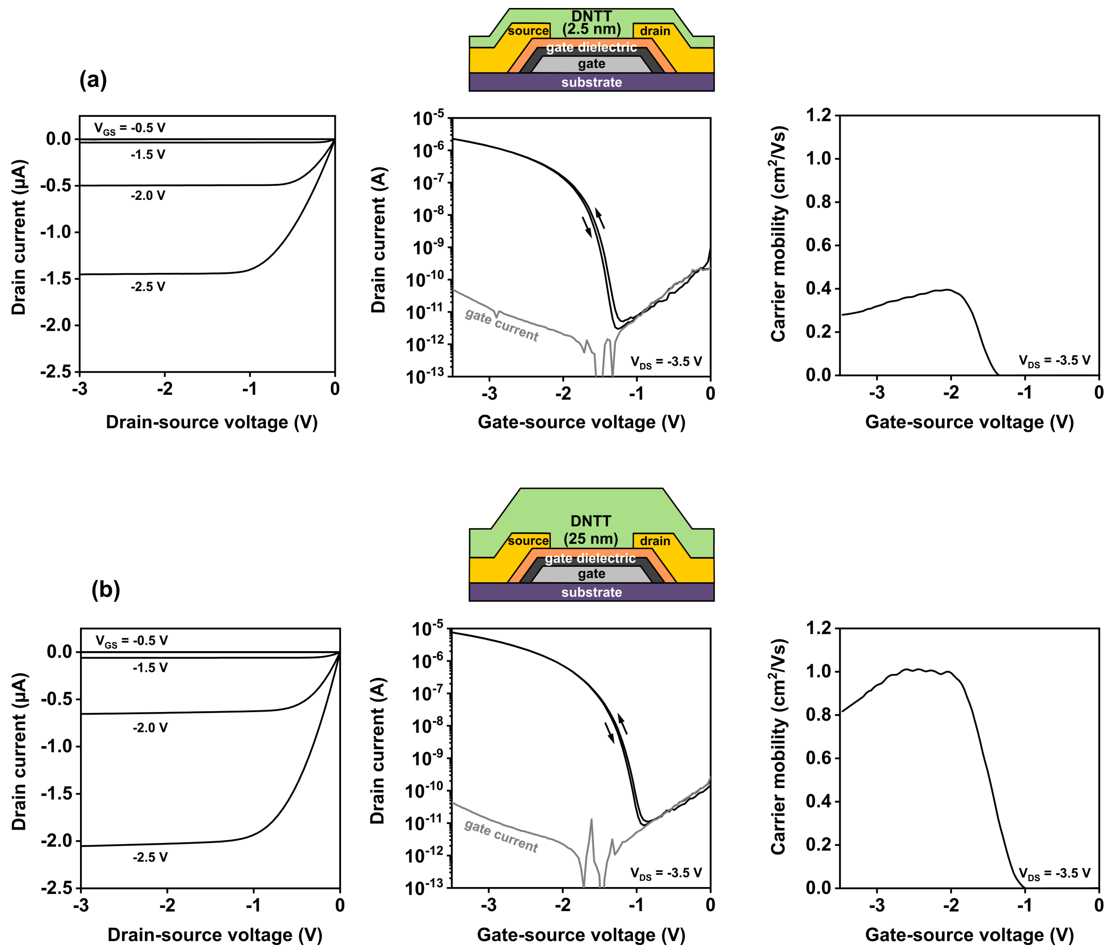


Figure A.3: Output and transfer curves and charge-carrier mobility as a function of gate-source voltage of (a) a TFT with a nominally 2.5-nm thick DNTT film; (b) a TFT with a nominally 25-nm thick DNTT film. The transfer curves were recorded within 15 minutes after the completion of the DNTT deposition

Appendix B

Optimizing plasma oxidation for aluminum oxide films

In Chapter 4, the influence of the plasma power and duration of plasma during the fabrication of AlO_x films on the electrical performance of organic TFTs was observed. The transfer characteristics, semiconductor morphology and other properties were showcased for certain combinations of the plasma-process parameters. In this Appendix, the transfer characteristics, output characteristics and the morphology of DNTT films for all 15 combinations tested are given.

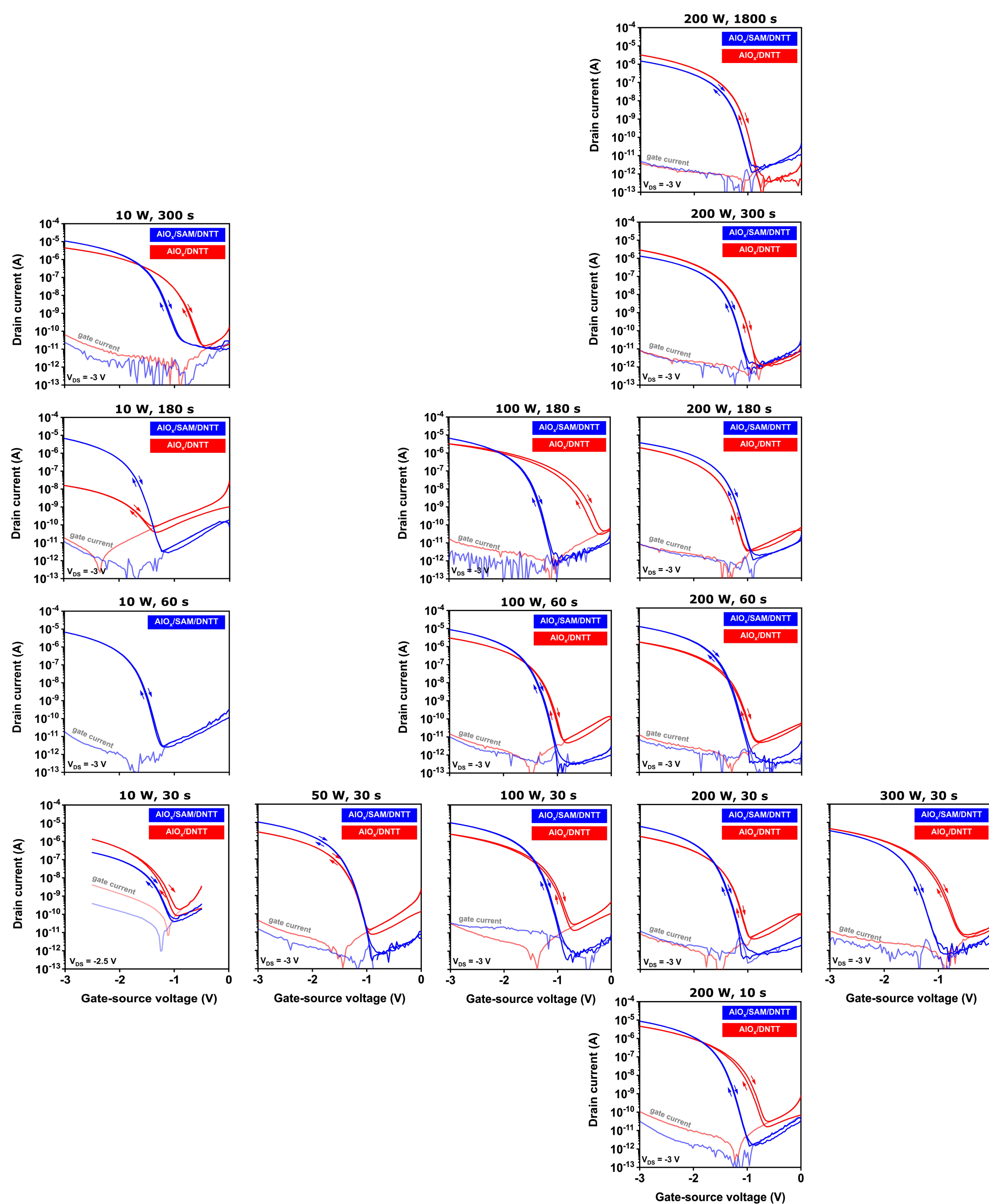


Figure B.1: Transfer characteristics and gate currents of DNTT TFTs fabricated using either a bare-AlO_x gate dielectric (red curves) or a hybrid AlO_x/$HC_{14}PA$ SAM gate dielectric (blue curves) for all fifteen combinations of the plasma power and plasma duration

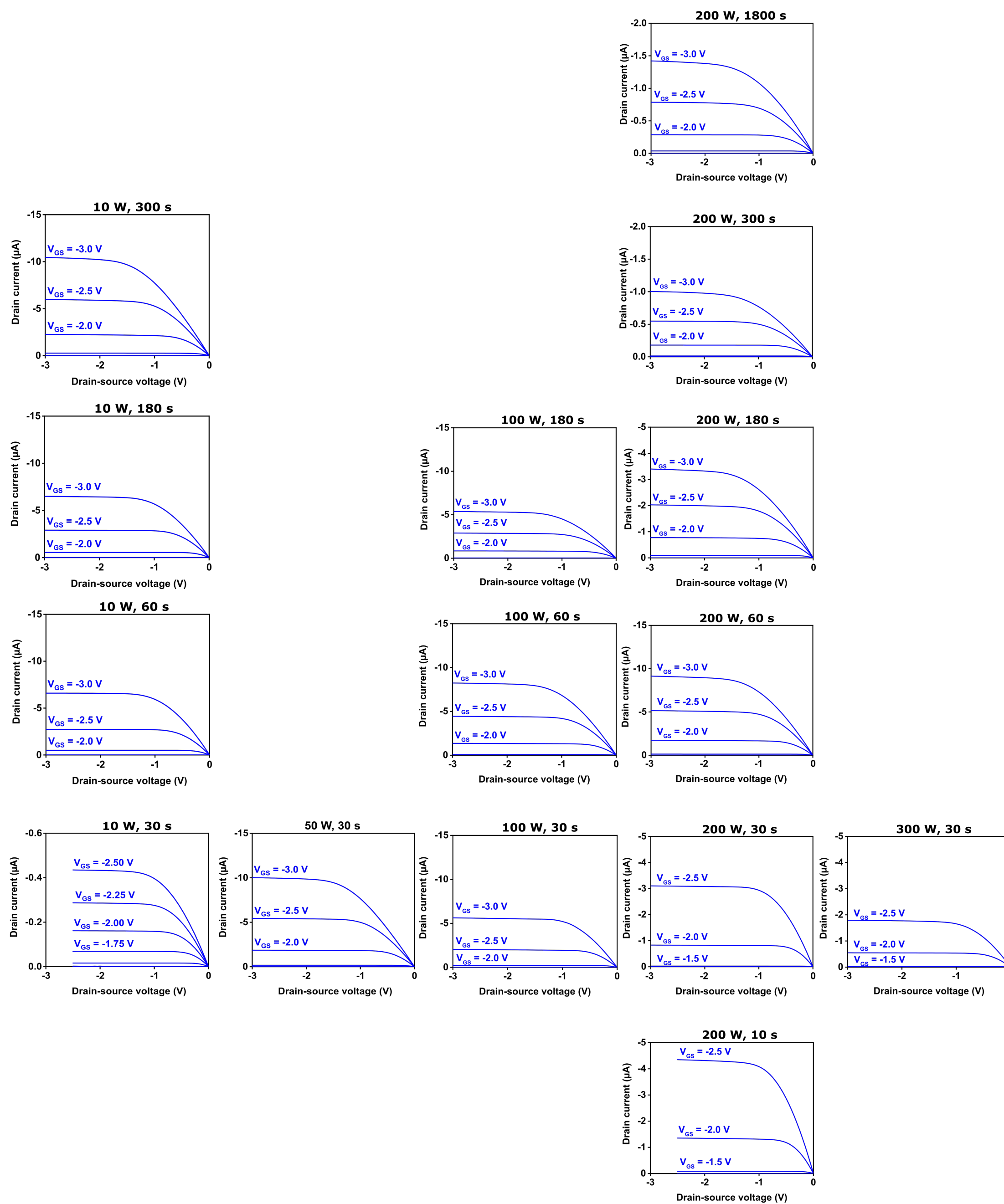


Figure B.2: Output characteristics of DNTT TFTs fabricated using a hybrid AlO_x/$HC_{14}PA$ SAM gate dielectric for all fifteen combinations of plasma power and plasma duration

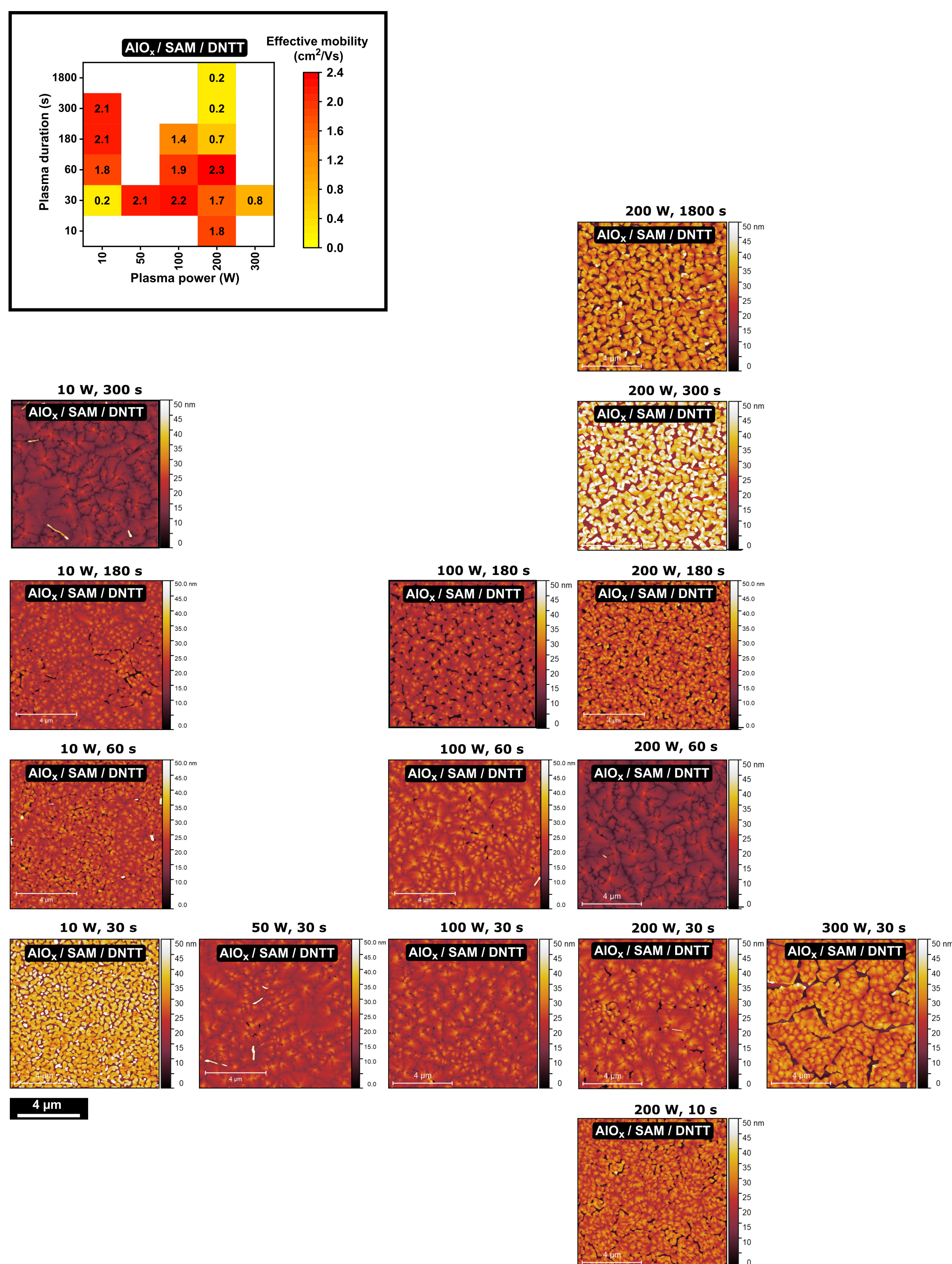


Figure B.3: AFM images of DNTT films deposited onto a hybrid AlO_x/$HC_{14}PA$ SAM gate dielectric for all fifteen combinations of plasma power and plasma duration and effective charge-carrier mobilities extracted from the measured transfer characteristics of DNTT TFTs fabricated using a hybrid AlO_x/$HC_{14}PA$ SAM gate dielectric as a function of plasma power and plasma duration. The high charge-carrier mobilities can be correlated with an optimum semiconductor morphology, i.e. a closed, connected film with a distinct dendritic structure

Appendix C

Optimizing the substrate temperature during semiconductor deposition for different substrates

The organic semiconductor DPh-BTBT was deposited by thermal sublimation in vacuum with the provision of heating the substrate during the semiconductor deposition process. Conventionally, substrates are heated to an optimum temperature to facilitate the diffusion of semiconductor molecules on the surface and form polycrystalline thin films for maximum carrier mobility and an enhanced electrical performance. However, increasing the substrate temperature (T_{sub}) beyond the optimum may result in island-mode growth or desorption of semiconductor molecules from the surface. A striking difference is observed between DPh-BTBT TFTs fabricated on silicon and on PEN substrates in the way the morphology of the DPh-BTBT layer and the TFT performance are affected by the substrate temperature during the semiconductor deposition. As seen in Fig.C.1(a-c), the TFTs fabricated on silicon have carrier mobilities of 0.56 cm^2/Vs when the substrate is held at a temperature of 25 °C during the DPh-BTBT deposition and 1.1 cm^2/Vs when the DPh-BTBT is deposited at a substrate temperature of 100 °C. This is the expected behavior for organic semiconductors deposited by thermal sublimation where a higher substrate temperature promotes larger grain size and enhanced

crystallinity in the thin film. In contrast, for DPh-BTBT TFTs fabricated on PEN, Fig.C.1(d-f) shows that heating the substrate during the DPh-BTBT deposition to a temperature of 100 °C yields a carrier mobility that is 3 orders of magnitude lower than that obtained without substrate heating.

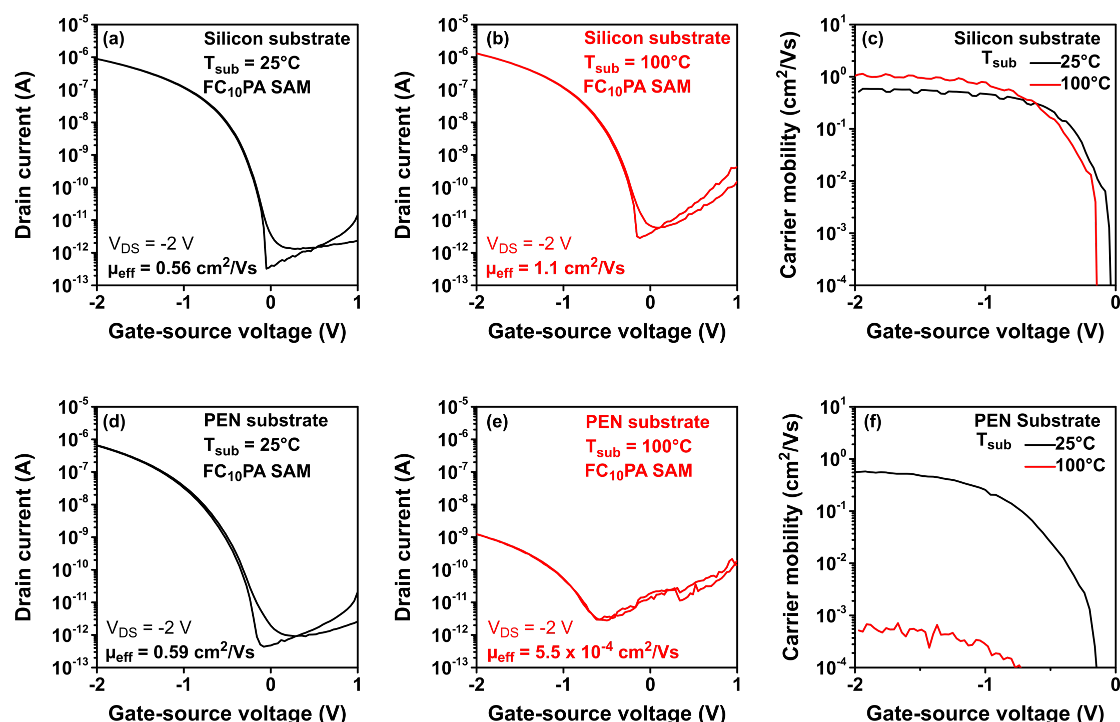


Figure C.1: Transfer curves of DPh-BTBT TFTs fabricated on silicon substrates with the substrate held at temperatures of (a) 25°C and (b) 100°C during the semiconductor deposition and (c) carrier mobilities extracted from the transfer curves. Transfer curves of DPh-BTBT TFTs fabricated on flexible PEN substrates with the substrate held at temperatures (d) 25°C and (e) 100°C during the semiconductor deposition and (f) carrier mobilities extracted from the transfer curves

The thin-film morphologies as seen in the scanning electron microscopy (SEM) images show that when the PEN substrate is heated during the semiconductor deposition, the DPh-BTBT molecules form isolated islands (Fig.C.2(c), inset) instead of a continuous film formed when the PEN substrate is held at 25 °C(Fig.C.2(d), inset). Since a percolation path for the molecules is harder to form through isolated islands, the carrier mobility is significantly lower. For silicon substrates held at 100 °C(Fig.C.2(a), inset) and 25 °C(Fig.C.2(b), inset), the thin-film morphologies indicate thin films with almost complete coverage in both cases, thereby establishing that the substrate temperature has little influence on the thin-film morphology of DPh-BTBT films on silicon substrates. Out-of-plane XRD measurements (Fig.C.2) performed on the DPh-BTBT films on PEN and silicon substrates indicate the possible orientation of the DPh-BTBT molecules,

establishing the influence of the substrate temperature on the thin-film morphology for the two different substrates. On the PEN substrate for the films deposited at a substrate temperature of 25°C, the DPh-BTBT molecules are mostly in an upright-standing orientation, with a dominant diffraction peak at $2\theta = 4.65°$ that corresponds to a (001) interlayer spacing of 19 Å. The appearance of the peaks corresponding to (002) and (003) further indicates a good layer-by-layer structure of the film. On the other hand, the DPh-BTBT films deposited on PEN at a substrate temperature of 100°C are characterized by a mix of upright-standing and lying-down orientation of the molecules, with peaks appearing at $2\theta = 4.65°$, 23.8°, and 27.1° that correspond to the (001), (020), and (120) orientations, respectively. The intensity of the (001) signal is much smaller than that measured on the film deposited at a substrate temperature of 100°C. Only the semiconductor molecules that are standing upright contribute to the lateral carrier transport, which explains why the carrier mobility is significantly larger when the semiconductor deposition is carried out at a substrate temperature of 25°C, rather than 100°C. In contrast, it is observed that the XRD spectra of the DPh-BTBT films on the silicon substrates are very similar for the two substrate temperatures, with a single dominant peak at $2\theta = 4.65°$, corresponding to molecules in an upright-standing configuration. Since this orientation is favorable to lateral carrier transport, this also explains the carrier mobilities of 0.56 and 1.1 cm^2/Vs for DPh-BTBT TFTs on silicon substrates for substrate temperatures of 25°C and 100°C, respectively, and the fact that the transistor characteristics depend only weakly on the substrate temperature during the semiconductor deposition.

A similar trend in the DPh-BTBT morphology can be seen in Fig.C.3, in which the underlying surface was a bare-AlO_x gate dielectric. On the silicon substrate, at a substrate temperature of 100°C, DPh-BTBT molecules exhibit a closed, connected thin-film morphology with XRD data indicating molecules in a favorable upright-standing configuration. On the PEN substrate, at an elevated temperature of 100 °C, the DPh-BTBT thin-film morphology is suboptimal with many holes and cracks seen in the SEM image. However, the XRD data indicates that the molecules are in a favorable orientation at both substrate temperatures.

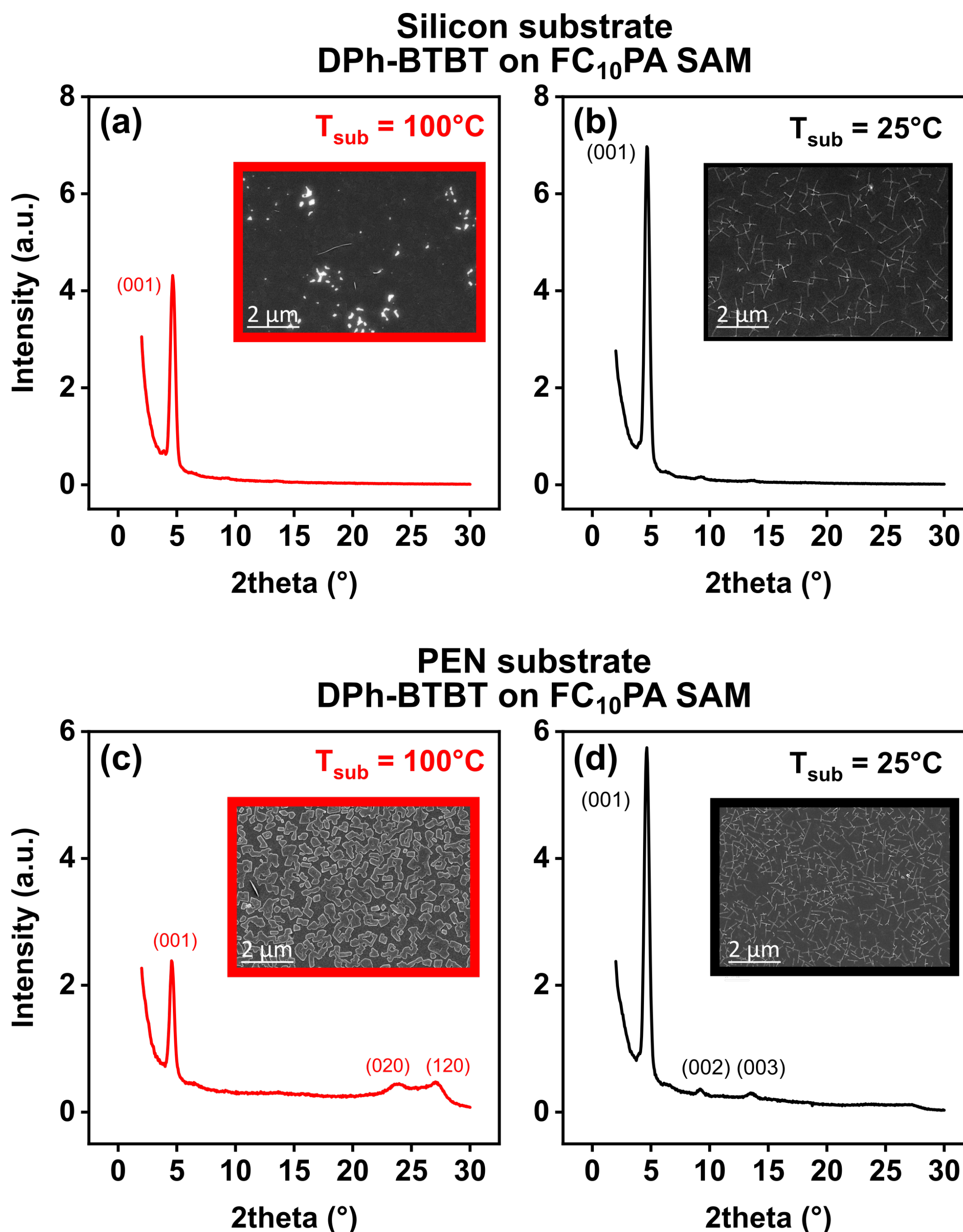


Figure C.2: Out-of-plane XRD spectra and corresponding scanning electron microscopy images of DPh-BTBT thin films deposited onto hybrid $AlO_x/FC_{10}PA$ SAM dielectrics on silicon substrates held at temperatures of (a) 100°C (red line) and (b) 25°C (black line) and on PEN substrates held at temperatures of (c) 100°C (red line) and (d) 25°C (black line) during the semiconductor deposition

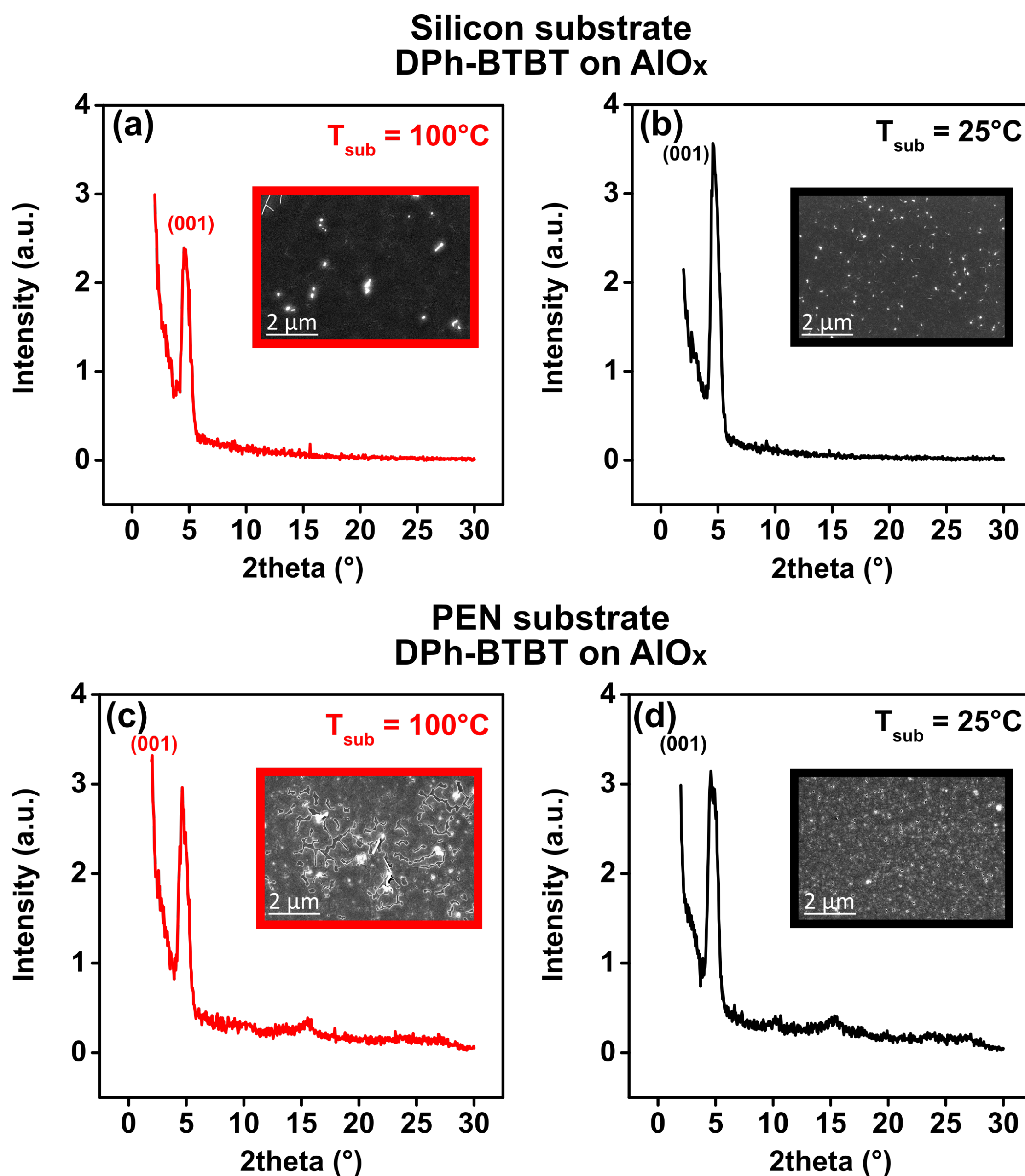


Figure C.3: Out-of-plane XRD spectra and corresponding scanning electron microscopy images (insets) of DPh-BTBT thin-films deposited onto bare AlO_x dielectrics on silicon substrates held at temperatures of 100˚C (red line, (a)) and 25˚C (black line, (b)) and on PEN substrates held at a temperature of 100˚C (red line, (c)) and 25˚C (black line, (d)) during the semiconductor deposition.

Appendix D

Optimizing combinations of the organic semiconductor/phosphonic acid SAM

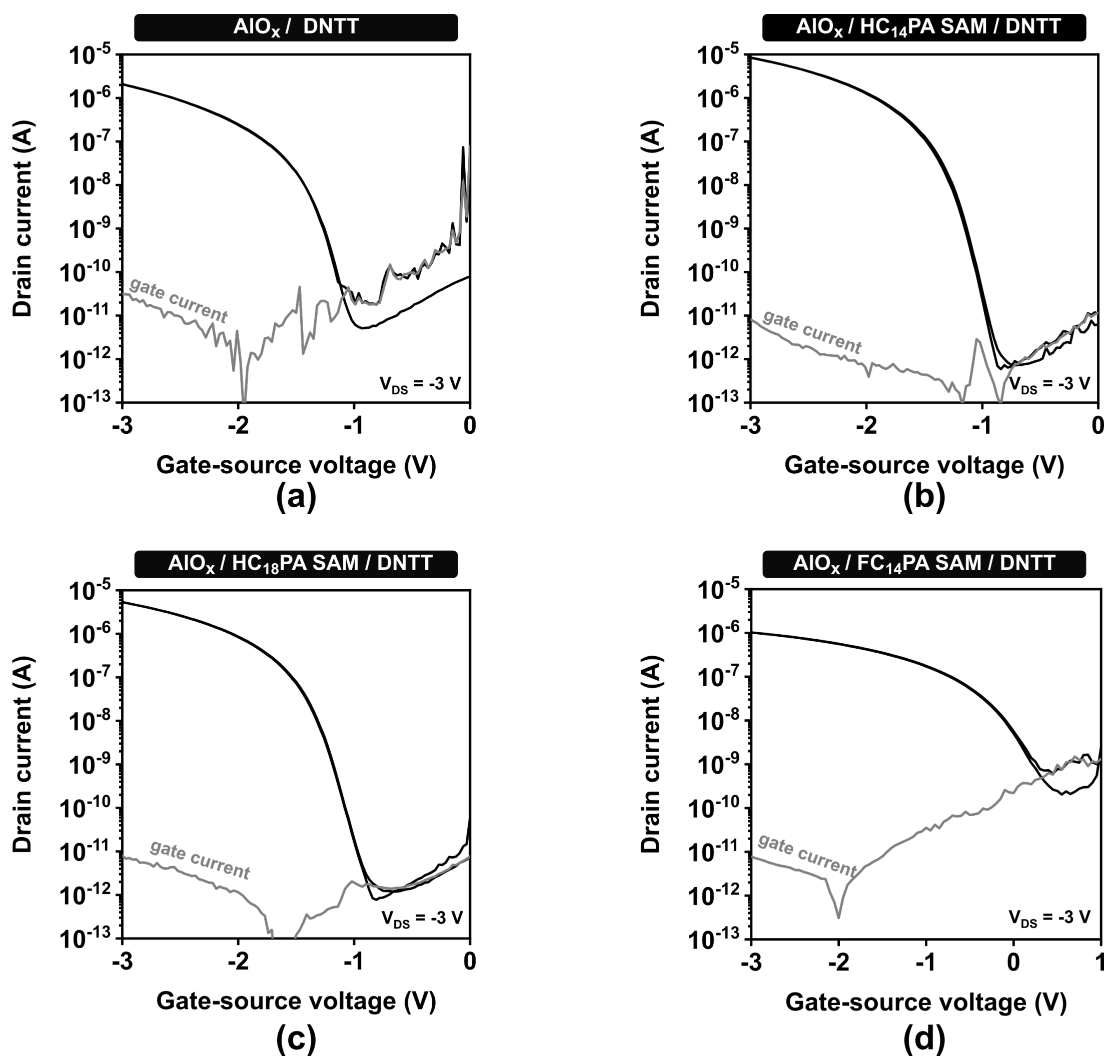


Figure D.1: Transfer characteristics of DNTT TFTs with different gate dielectrics (a) bare-AlO_x (b) AlO_x/HC_{14}PA SAM (c) AlO_x/HC_{18}PA SAM and (d) AlO_x/FC_{14}PA SAM

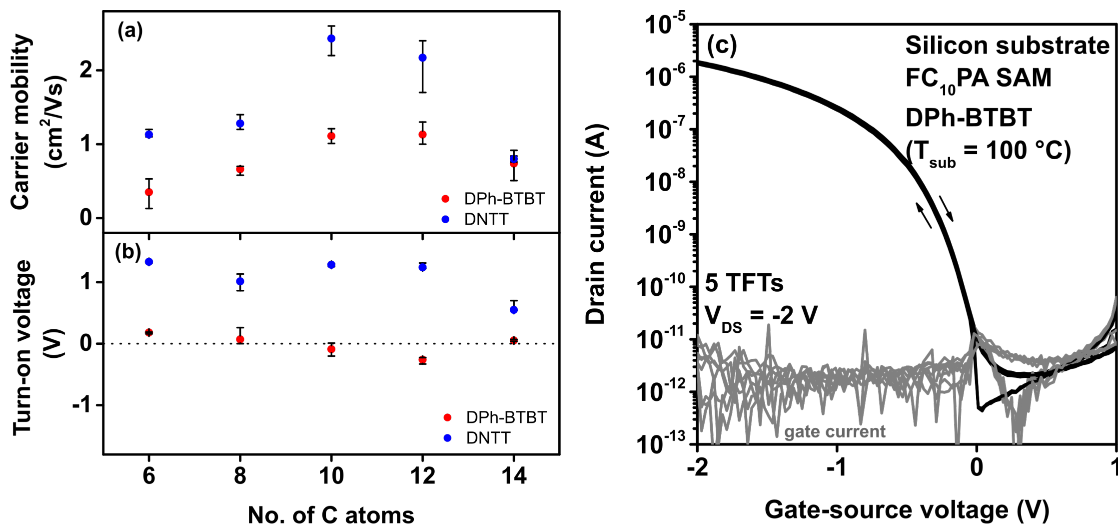


Figure D.2: (a) Carrier mobilities and (b) turn-on voltages of DPh-BTBT and DNTT TFTs with hybrid AlO_x/SAM gate dielectrics based on fluoroalkylphosphonic acids with chain lengths of 6, 8, 10, 12, and 14 carbon atoms fabricated on silicon substrates. (c) Transfer curves of five DPh-BTBT TFTs with a hybrid $AlO_x/FC_{10}PA$ SAM gate dielectric fabricated on a silicon substrate, showing a turn-on voltage of exactly 0 V. The substrate was held at a temperature of 100°C during the DPh-BTBT deposition and at a temperature of 60°C for the DNTT deposition

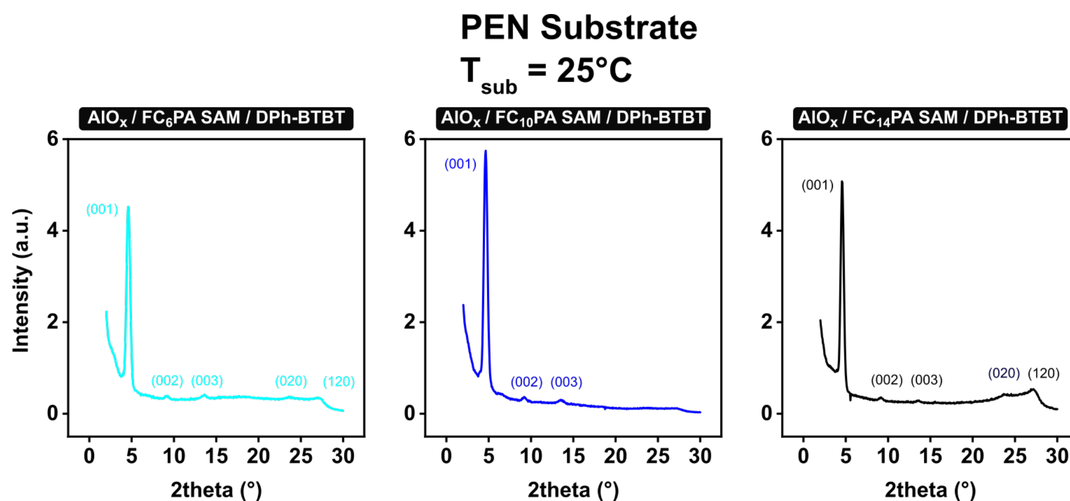


Figure D.3: Out-of-plane XRD spectra measured on DPh-BTBT thin films deposited onto three different hybrid AlO_x/SAM dielectrics on PEN substrates

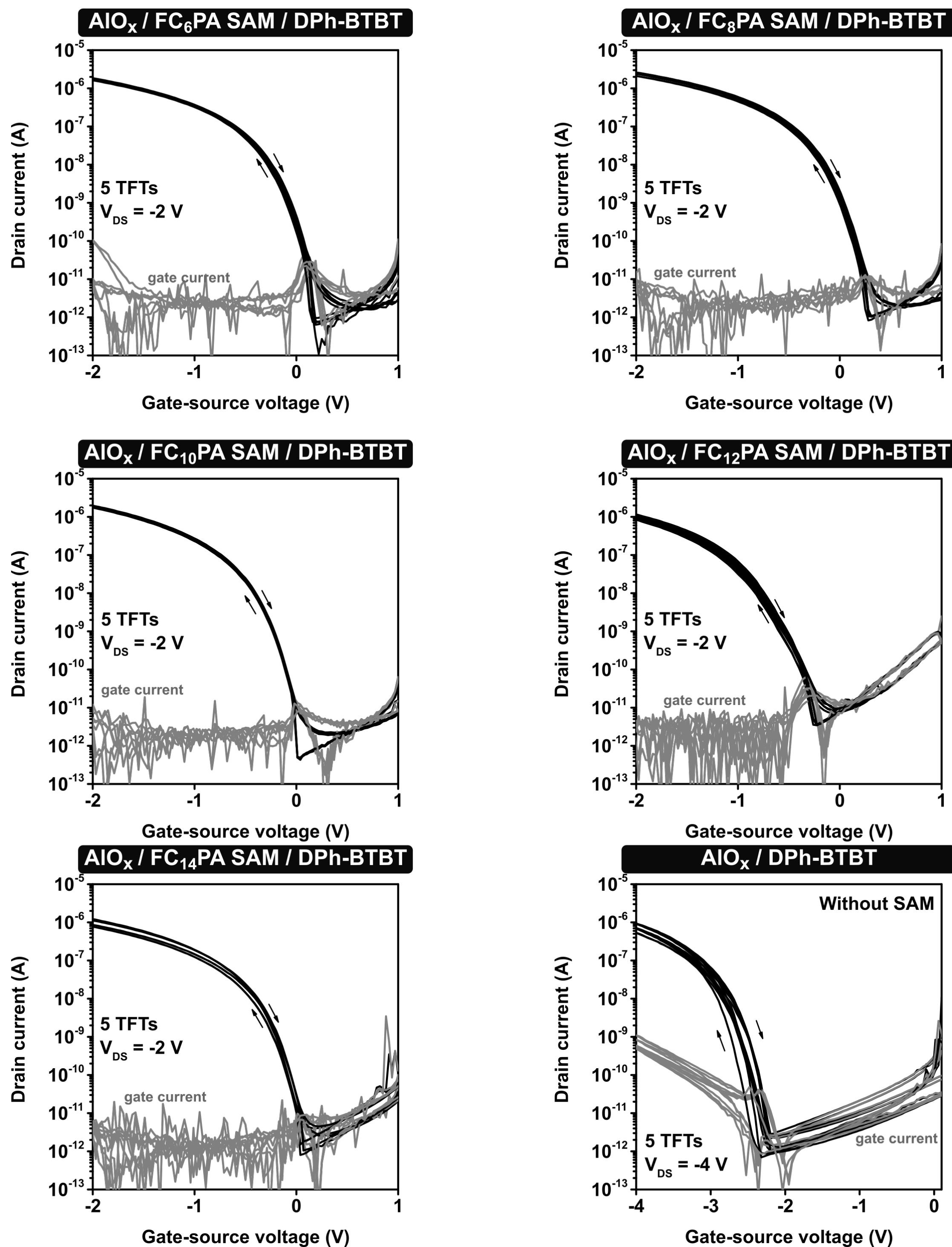


Figure D.4: Transfer curves of five DPh-BTBT TFTs each with a hybrid AlO_x/SAM gate dielectric based on fluoroalkyl phosphonic acids with five different chain lengths, along with a bare AlO_x gate dielectric (without SAM) fabricated on silicon substrates with substrate temperature at 100°C during semiconductor deposition

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