20 Gbit/s 2:1 Multiplexer Using 0.3 μm Gate Length Double Pulse Doped Quantum Well GaAs/AlGaAs Transistors

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ABSTRACT

A high speed 2:1 multiplexer circuit in source coupled FET logic has been developed and fabricated using a recessed gate process for enhancement and depletion transistors with 0.3μm gate length. First results show a data rate of over 20 Gbit/s at 5 V supply voltage and 250 mW power consumption. The output voltage swing is adjustable between 0.3 V and 0.8 V for a 50 Ohm load. The output level can be varied between +1 V and -1 V. Comparison between simulation and measurement shows very good agreement.

1. INTRODUCTION

High speed multiplexers are key components in many electronic systems e.g. in fast optoelectronic communications systems, instrumentation or test equipment. Recently a lot of work has been done to improve those circuits using different technologies [1-4]. In this paper we report on a 2:1 multiplexer for high speed non return to zero (NRZ) data generation for test equipment purposes. The circuit fabrication is based on an advanced E/D recessed gate process [5] with 0.3 μm gate length transistors.

2. CIRCUIT DESIGN AND SIMULATION

Fig. 1 shows a schematic of the 2:1 multiplexer. It consists of a logic part with a high speed switch, two data inputs, amplitude and level adjustment, and a 50 Ohm output driver stage. The design using source-coupled-FET-logic (SCFL) with 0.3 μm en-
hancement transistors for the active elements and 2 μm depletion transistors as level shifting diodes give the circuit highest performance. The active and passive elements have been optimized using an ‘in house’ adapted SPICE model. Fig. 2 shows a full logic test pattern simulation. The chip size is 1 x 1 mm² and contains two identical circuits.

3. MEASUREMENTS

On-wafer full logic high speed tests have been performed on the multiplexer. The measurement setup can be seen in fig. 3. The typical power supply voltages are $V_{dd} = 2.0$ V and $V_{ss} = -3.0$ V. The power consumption is about 250 mW. The input voltages are 0.7 V for data and switch against ground. The output level (zero state) is adjustable from -1.0 V to +1.0 V. The output voltage swing can be varied from 0.3 V to 0.8 V at a 50 Ohm load. Fig. 4 shows results of a complete functional test at 16.4 Gbit/s. At present this is the upper limit of our measurement equipment. Simpler switching tests function also at 20 Gbit/s (fig. 5). This circuit setup enables us to extend the maximum testing speed of our measurement equipment by a factor of two.

4. ACKNOWLEDGEMENT

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5. REFERENCES

Fig. 1 Circuit diagram of the 2:1 multiplexer.

Fig. 2 SPICE full logic simulation.

Fig. 3 Testing scheme for the multiplexer. Two different data patterns are generated from one data source by programming both data input streams in series and delaying the data for input B.
Fig. 4 Complete functional test at 16.4 Gbit/s

Fig. 5 Switching test at 20 Gbit/s. Input A is held at logic high and input B at low.