## TA 6.6: 19GHz Monolithic Integrated Clock Recovery Using PLL and 0.3μm Gate-Length Quantum-Well HEMTs*

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ICs for optical data links have been developed for bit rates between 10 and 20Gb/s [1]. The only exception was the clock recovery (CR) IC at these high bit rates. In fact, the IC realization of CR is generally accepted as the weak point of high-speed system integration [2]. While the bit rates of some ICs reach up to 40Gb/s , monolithic ICs for a full CR function are limited to 2.5 Gb/s [3, 4]. The monolithic IC described here, for CR with a PLL including a full-balanced VCO, is based on the IC reported in Reference 5. Clock frequencies up to 19GHz are recovered with the IC reported here.

The block diagram of the CR IC is shown in Figure 1. No off-chip components are required. A modified XOR-circuit introduced in Reference 5 is used here for three reasons: 1) it can be integrated monolithically, 2) it has a fully-balanced structure, and 3) it has a filtering function on the output side. A double-balanced multiplier with a capacitively-coupled current amplifier in the lower level (as in the modified XOR) is adopted for phase detector (PD) in the PLL. This circuit completely eliminates the influence of the dc components of both input signals. For the loop filter, the typical lead-lag active low-pass was utilized. To adjust loop performance, the circuit shown in Figure 2 is used for on-chip adjustable resistances. In the circuit the drain-to-source channel of the depletion HEMT (DF) is used as an adjustable resistor. The gate-to-source control voltage is provided by resistor RGS and the current ICR, controlled by the external voltage VCR. The opamp is composed of three stages of differential amplifiers, for which depletion HEMTs are used as active loads to increase gain.

As the key part of the PLL, a VCO circuit based on the circuit described in Reference 6 is used. An important feature of the VCO circuit is its fully-balanced structure. Thus, an ultra-high working frequency at lower noise level is obtained. It can be directly connected back to the PD.

The micrograph of the IC, including about 150 HEMTs, 20 resistors, 4 inductors, and 8 capacitors, is shown in Figure 3. The process used for the ICs in Reference 1 is used for IC fabrication. A detailed description of the process can be found in Reference 7. The gate length of the HEMTs is 0.3μm. The transit frequency $f_T$ of the enhancement HEMT is typically 50GHz. For capacitors, both the interdigital and the MIM-structure can be used. Air bridges and high-Q inductors are constructed through the second interconnect metal.

About 30 chips distributed over two 2-inch wafers were measured on wafer using 50Ω coplanar test probes. The measured results and other chip data are summarized in the Table 1.

Figure 4 shows a spectrum of a free-running VCO at the center frequency of about 19 GHz. The spectral line width here is less than 1MHz. The ratio of the center frequency to the spectral line width is about 19k, and the phase noise estimated from the spectrum is about -85dBc/Hz at an offset of 1MHz. Figure 5 shows the spectrum of the output signal of a locked VCO. In this case the -3dB spectral line width is reduced to about 50kHz, the level of the input signal. Figure 6 shows the measured eye diagrams of the input data and the recovered clock signal. Due to the pattern generator used, the 9.3Gb/s bit rate of the input data is at one half the desired data rate. In this case the LC loop on the drain side of the XOR is tuned to the second harmonic of the detected clock signal. Even under such unfavorable conditions, the clock signal is still well recovered. Running at full bit rate, the quality of the clock signal is expected to improve. This is the first reported monolithic CR IC with working frequency greater than 10GHz. With minor parameter modifications, the CR circuit can be implemented in the future SDH/SONET systems at bit rates about 20Gb/s (8xSTM-16).

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|---|---|
| VCO max. oscillating frequency | 19GHz |
| Mean center frequency, $f_o$ (30 chips, Vcm=0) | 18.35GHz |
| $\sigma f_o$ (standard deviation of $f_o$) of 30 chips | 0.35GHz |
| $\Delta f$ at $f_o$ by control of Vcm (0 to -2V | 1.5GHz |
| $\Delta f$ at $f_o$ by control of Vco (-1 to -2V) | 0.65GHz |
| $\Delta f$ at $f_o$ by supply voltage change of ±0.1V | 12MHz |
| Spectral line widths of free-running VCO | <3MHz |
| Measured hold-in range of one PLL | 180MHz |
| Measured lock-in range of same PLL | 150MHz |
| Supply voltage | -5V |
| Supply current | <70mA |
| Chip area | 1.5x1mm² |

**Table 1: Parameters**



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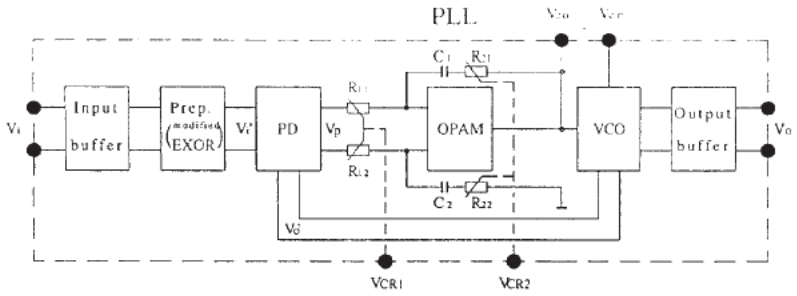


**Figure 1: Block diagram of IC for high-speed clock-recovery with PLL.**

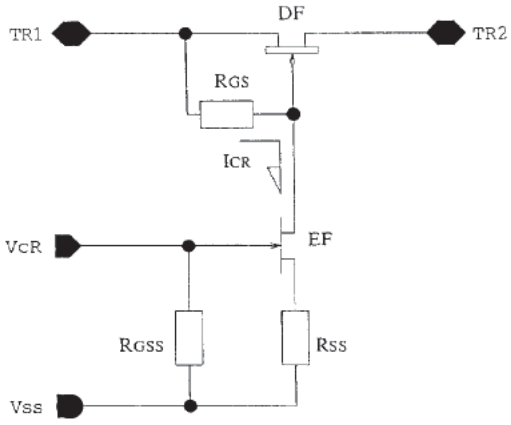


**Figure 2: On-chip variable-resistance circuit.**
**Figure 3: See page 320.**

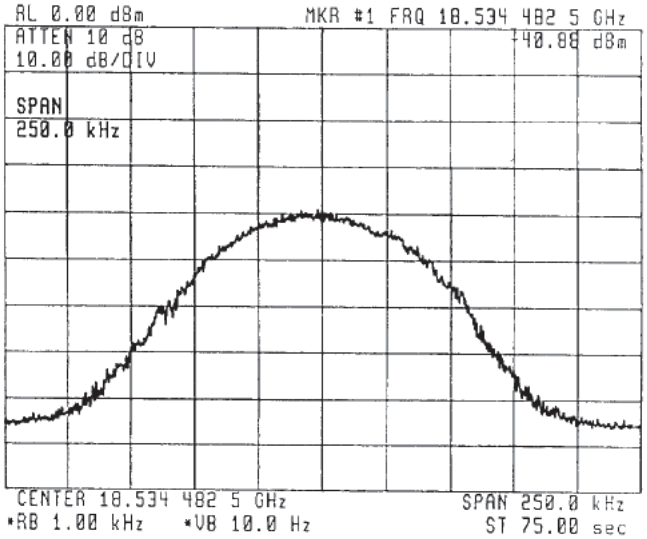


**Figure 5: Near-carrier spectrum of locked VCO.**

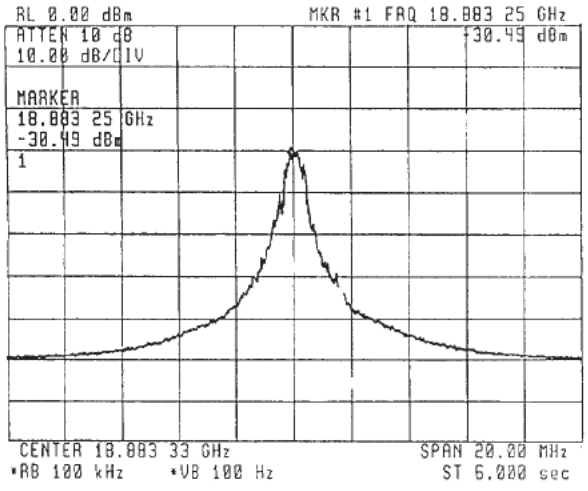


**Figure 4: Near-carrier spectrum of free-running VCO.**

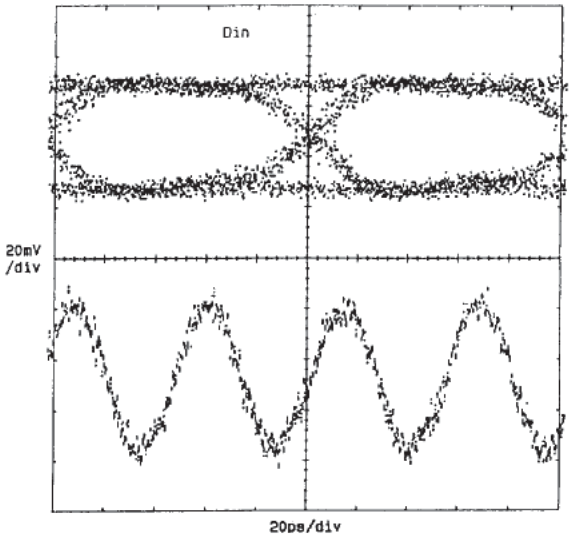


**Figure 6: Eye diagram of a 19 GHz clock-recovery IC; input data (top), recovered clock (bottom).**