been increased with the application of transistor structures based on GaAs or related compounds. Using 0.2-mm GaAs MESFETs [1] and 0.25-mm inverted AlGaAs HEMT [2], operating frequencies of 26-5 GHz have been presented for dynamic frequency dividers. Static dividers based on AlGaAs-GaAs-HBTs [3] and AlGaAs-GaAs-HBTs [4] achieved frequency limits of 34.8 and 39.5 GHz, respectively.

The design and performance of a dynamic frequency divider operating in the 18-34 GHz range based on AlGaAs-GaAs/AlGaAs quantum well transistors was presented in Reference 5. As far as we know this was the best result ever reported for HEMT circuits and similar to the frequency limit achieved by use of AlGaAs-GaAs/HBTs.

A further performance enhancement up to 51 GHz operation by the use of pseudomorphic AlGaAs/InGaAs MODFETs will be presented here.

AlGaAs/GaAs/InGaAs MODFET process: We have developed a mix and match technology combining e-beam with optical lithography whereby the e-beam is used for writing the gates only. Mushroom-shaped gates were used to reduce the resistance of 0.15-μm gates. The layer structure including n+ - and p-type GaAs supply layers, AlGaAs spacers, and pseudomorphic InGaAs channel was grown by MBE [6]. Precise control of the threshold voltage was guaranteed by an AlGaAs etch stop using a dry etch process. In our process sequence we have E-type MODFETs, NiCr thin film resistors, MIM capacitors, and two layers for interconnections. The top layer can be fabricated as air bridges thus reducing the capacitance.

Circuit design: Fig. 1 schematically depicts the dynamic frequency divider. Two ring oscillators each consisting of one push-pull inverter and three source followers were fed back by transfer gates. A memory type flip-flop was used for data storage during the period when the transfer gates show high resistance due to the low voltage applied to the clock input. The inverter stages were built up in DCL with passive resistor loads, and push-pull and source follower buffers were realised by enhancement type MODFETs. The circuit design was optimised by SPICE simulation based on an 'in house' developed FET network model [7].

The operating frequency range of the divider is given by

\[
\frac{2(1 \text{NWS} + 6 \text{SF})^{-1}}{1} \leq f \leq \left(1 + \frac{3 \text{SF}}{1 \text{NWS}}\right)^{-1}
\]

where \(1\text{NWS}\) and \(1\text{SF}\) are the propagation delays of the inverter and the source follower, respectively.

Results: Measurements carried out on the dynamic frequency divider gave a lower limit for stable operation of 28 GHz and a value of 51 GHz for the maximum input frequency. Fig. 2 shows the pulse diagram of the 51 GHz input and the 25.5 GHz output. To the best of our knowledge this is the highest input frequency ever reported for frequency divider circuits in any technology.

The divider can operate with single phase input. Both single phase and differential outputs are available. The circuit runs at a power supply of \(V_{\text{DS}} = +3.5\) V and \(V_{\text{DD}} = -0.5\) V. The required input voltage swing is less than 600 mV at 28 GHz and decreases as the frequency increases. A power consumption of 440 mW was measured for the divider including the output buffers. The chip size was \(200 \times 220 \mu\text{m}^2\).
Summary: The design and performance of a dynamic frequency divider were presented. This digital IC demonstrates the ability of our pseudomorphic Al0.3Ga0.7As/In0.53Ga0.47As MODFETs with 0.15 µm mushroom-shaped gates. Stable operation was achieved in the frequency range 28-51 GHz with a power consumption of 440 mW.

Acknowledgments: This work was a group effort and the authors are grateful to the entire staff of the laboratory. We especially want to thank H. S. Rupprecht for his directing and continuous encouragement, and T. Jakobus for his expert technology management. The German Federal Ministry of Research and Technology is acknowledged for the financial support through the DFE-project TK357 / 9.

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ERRATA

Authors' corrections
The third and fourth subcaptions to Fig. 1 should read:
- rectangular
- trapezoidal

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