Monolithic Opto-Electronic Co-Integration on the Example of a Photonic-Assisted, High-End Sampler

Von der Fakultät Informatik, Elektrotechnik und Informationstechnik der Universität Stuttgart zur Erlangung der Würde eines Doktor-Ingenieurs (Dr.-Ing.) genehmigte Abhandlung

Vorgelegt von

Benjamin Krüger

aus Böblingen

Hauptberichter:	Prof. Dr. habil. Jörg Schulze
Mitberichter:	Prof. Dr. Boris Murmann
Tag der mündlichen Prüfung:	05.09.2018

Institut für Halbleitertechnik

der Universität Stuttgart

2018

Declaration of Authorship / Erklärung

I declare that this thesis and the work presented in it has been unassistedly generated by myself. The literature in use and any other resources are indicated completely.

Hiermit versichere ich, die vorliegende Arbeit selbstständig und ohne fremde Hilfe angefertigt zu haben. Die verwendete Literatur und sonstige Hilfsmittel sind vollständig angegeben.

Munich, January 03, 2018

Contents

Declaration of Authorship / Erklärung I

Contents V

List of Figures XI

List of Tables XIII

Glossary XV

Acronyms XVII

Physical Constants XXI

Zusammenfassung XXIII

Abstract XXV

Acknowledgements XXVII

1 Introduction 1

1.1 Motivation . . . 1

1.2 Thesis Overview . . . 5

2 ADC Fundamentals 7

2.1 Sampling Basics . . . 7

2.2 Static Performance of ADCs . . . 11

2.3 Dynamic Performance of ADCs . . . 12

2.3.1 Noise in Analog Signal Path . . . 12

2.3.2 Harmonic Distortions in Analog Signal Path . . . 13

2.3.3 Non-Harmonic Distortions due to Gain and Offset Mismatch . . . 13

2.3.4 Non-Harmonic Distortions due to Timing Skew . . . 15

2.3.5 Clock Jitter . . . 15

2.3.6 Overall Dynamic Performance in Terms Of ENOB . . . 19

3 System Considerations for High-Speed and High-Resolution Sampling Performance 21

4 Architecture Considerations for the Implementation of the System Components 25
4.1 Photonic SiGe-BiCMOS Technology Platform . . . 25
4.2 Fiber-to-Chip Interface . . . 26
4.3 Optical Clock Distribution Network . . . 28
4.3.1 Integrated Silicon Waveguides . . . 28
4.3.2 Multimode Interference Coupler as Optical Power Divider . . . 31
4.3.3 Clock Distribution Network for the Proposed 80 GS/s TI ADC . . . 32
4.4 High-Performance Photodiode . . . 34
4.5 Mode-Locked Laser as High-Performance Clocking Source . . . 36
4.6 High-Speed Sampler Architectures . . . 38
4.6.1 Track-And-Hold Architecture . . . 38
4.6.2 Pulse-Sampling Architecture . . . 43

5 Opto-Electronic Clock Converter 51
5.1 Circuit Design . . . 51
5.2 Experimental Results . . . 57
5.2.1 Measurement Setup . . . 57
5.2.2 Measurement Results . . . 59

6 Optically Clocked Sampler Core Unit 67
6.1 Circuit Design . . . 67
6.2 Experimental Results . . . 73
6.2.1 Measurement Setup . . . 73
6.2.2 Measurement Results . . . 75

7 Development of a Reliable Method for the Characterization of Ultra-Low Sampler Jitter 83
7.1 State of the Art in Jitter Measurement . . . 83
7.2 Cyclostationary, Stochastic Approach . . . 85
7.3 Measurement Accuracy and Error Sources . . . 86
7.3.1 Stationary Noise . . . 87
7.3.2 Cyclostationary Noise . . . 88
7.3.3 Generator Jitter . . . 89
7.3.4 Distortion Robustness . . . 91
7.3.5 Data Acquisition with a Waveform Recorder . . . 92
7.4 Implemented Post-Processing Algorithm . . . 93

7.5 Experimental Results Using an Electrical High-End Sampler 95
7.5.1 Measurement Setup 95
7.5.2 Measurement Results 96
7.6 Experimental Results Using the Photonic-Assisted Sampler 100
7.6.1 Measurement Setup 100
7.6.2 Measurement Results 101

8 Conclusions **105**

Appendices **107**

A Jitter Induced by Noise in the Electrical Domain for the Edge-Triggered Sampling Architecture **109**

B Timing Errors due to a Pulse Shape Deviation for the Edge-Triggered Sampling Architecture **111**

C Influence of Timing Skew on the Efficiency of Generator Jitter Cancellation **113**

References **115**

Curriculum Vitae **127**

List of Figures

1.1 ENOB as a function of the analog signal frequency for state-of-the-art ADCs published in [3] and theoretical limits due to jitter σ_t. . . . 2
1.2 A block diagram of a TI architecture. . . . 2
1.3 A CDN on the example of a symmetrical H-tree topology. . . . 3

2.1 A block diagram of an ADC. . . . 7
2.2 a) Variation in time of an ideal S/H output (solid line) for the given input signal v(t) (dashed line). In this example, the width ΔT of the rectangular function is equal to the sample period T_s. b) Spectrum at the S/H output (solid line) and spectrum of the input signal (dashed line). . . . 9
2.3 A quantization diagram of a linear mid-tread quantizer with N = 4 bits. . . . 10
2.4 Simple model of a sampler a) in the hold mode and b) in the sample mode. . . . 12
2.5 Errors induced by a) offset mismatch, respectively b) gain mismatch on the example of a sinusoidal signal sampled with a 4x TI ADC. . . . 14
2.6 Error induced by timing skew on the example of sampling a sinusoidal signal with a 4x TI ADC. . . . 15
2.7 Transfer from timing jitter to voltage error. . . . 16
2.8 Relationship between the input signal (top), the normalized magnitude-squared of its derivative (middle), and the normalized jitter-induced noise (bottom). . . . 18

3.1 A block diagram of the proposed photonic-assisted TI sampler architecture, as well as the contributions of the individual project partners. . . . 22
3.2 Composition of ENOB on block level. . . . 23

4.1 Photonic BiCMOS cross-section, perpendicular to the direction of light propagation, of the monolithically integrated receiver components: Ge-PIN-PD and Si-WG on a local SOI and a SiGe HBT fabricated in an adjacent bulk region (Source: [39]). . . . 26
4.2 a) Basic configuration of fiber-to-chip coupling by a 1D grating. b) A photograph of a fiber placed above the grating coupler on the chip (Source: [47]). . . . 27
4.3 Measured losses of two 1D grating couplers (Source: [22]). . . . 27
4.4 Cross section of rib WG. . . . 28

4.5 a) Measured output power of the Si-WG as a function of the input power for various pulse train characteristics. b) Calculated output pulse energy of the Si-WG as a function of the input pulse energy (Source: [47]). 30
4.6 Layout of a 1x2 MMI coupler. 31
4.7 Optical CDN proposed for the implementation in the 80 GS/s TI ADC (Source: [47]). 32
4.8 Schematic of the test structure, implemented for the characterization of the skew of the proposed CDN (Source: [47]). 33
4.9 Measured skews relative to the first pulse position as a function of temperature (Source: [47]). 34
4.10 a) Frequency response of first generation PD for different reverse bias voltage values, measured at a wavelength of $\lambda = 1550$ nm and and average photocurrent of $I_{photo} = 100\,\mu$A. b) Frequency response of second generation PD for different reverse bias voltage values, measured at a wavelength of $\lambda = 1550$ nm and and average photocurrent of $I_{photo} = 140\,\mu$A (Source: [41]). 35
4.11 TEM cross sections of the Ge lateral pin PD, perpendicular to the direction of light propagation: a) Layout of the first generation PD with a bandwidth $f_{3dB} = 30$ GHz and a quantum efficiency of $\eta_{PD} = 52\,\%$. b) Layout of the second generation PD with a bandwidth $f_{3dB} > 50$ GHz and a quantum efficiency of $\eta_{PD} = 84\,\%$. 36
4.12 A block diagram of passive MLL. 37
4.13 A block diagram of the optical 1x8 interleaver used for the pulse repetition rate multiplication. 38
4.14 Block diagram of a photonic-assisted 10 GS/s Track-And-Hold Amplifier (THA) architecture. 39
4.15 Jitter $\sigma_{t,edge}$ as a function of the PD bandwidth for an optical pulse width of $\tau_o = 300$ fs and a optical pulse energy of $E_P = 200$ fJ at the input of the PD with an efficiency of $\eta_{PD} = 40\,\%$. The influence when using an EDFA with a gain of $G_{EDFA} = 100$ and noise figure of $10 \cdot \log_{10}(NF_{EDFA}) = 6$ dB to compensate the losses $\eta_{eff} = 0.01$ in the CDN is also shown. 42
4.16 a) Skew induced by a mismatch of the pulse energy for different center bandwidth values. b) Skew induced by a mismatch of the PD bandwidth. 43
4.17 A block diagram of the photonic-assisted pulse-sampling architecture. 44
4.18 Contribution of the amplitude and phase noise to the overall shot noise as a function of the optical pulse duty cycle. 47
4.19 a) SNR_{p2p} due to optical pulse-to-pulse energy fluctuations as a function of the optical pulse energy E_p for $\tau_o = 300$ fs, and an EDFA with a gain of $G_{EDFA} = 100$ respectively a noise figure of $10\log_{10}(NF_{EDFA}) = 6$ dB. b) Jitter σ_t of the proposed pulse sampling architecture for the same parameters. 48

5.1 Simplified schematic of the O/E clock converter circuit. 52
5.2 a) Schematic of the O/E clock converter core at the switching instant. b) Simplified schematic of the same circuit including noise sources. 54
5.3 a) Jitter induced by the electronic circuit devices of the O/E clock converter as a function of the optical design parameters, the 3 dB-bandwidth of the PD and the optical pulse energy ($R_L = 400\,\Omega$ and $C_L = 100\,\text{fF}$). b) Jitter induced by the electronic circuit devices of the O/E clock converter as a function of the electrical design parameters R_L and C_L ($f_{3dB} = 30\,\text{GHz}$ and $E_p = 200\,\text{fJ}$). 56
5.4 a) Overall jitter of the O/E clock converter as a function of the optical design parameters ($R_L = 400\,\Omega$ and $C_L = 100\,\text{fF}$). b) Overall jitter of the O/E clock converter as a function of the electrical design parameters ($f_{3dB} = 30\,\text{GHz}$ and $E_p = 200\,\text{fJ}$). A constant voltage drop of $I_{bias,RS} \cdot R_E = 300\,\text{mV}$ across R_E is assumed. 56
5.5 A block diagram of the processed test chip. 57
5.6 A block diagram of the measurement setup used for the characterization of the O/E clock converter circuit. 58
5.7 Measured optical power $p_{opt,out}$ at the output grating of the CDN as a function of the optical input power $p_{opt,in}$. 59
5.8 a) Normalized variation in time of the PD output voltage for 10 subsequent pulses as response to a $f_{rep} = 10\,\text{GHz}$ optical pulse train with an optical input power $p_{opt,in} = 20\,\text{dBm}$, and a PD bias voltage of $V_{bias,PD} = -3\,\text{V}$. b) Normalized spectrum at the output of the PD for the same operating point. 60
5.9 Normalized variation in time of the PD output voltage for different optical input power values. 61
5.10 Measured variation in time of the O/E clock converter output voltage for different optical input power values. 62
5.11 Measured self-oscillation frequency f_{res} of OE clock converter as a function of the average optical power of the continuous-wave laser. 63
5.12 Measured phase noise of the OE clock converter for different optical input power values. 64

6.1 A block diagram of the implemented 10 GS/s pulse-sampling architecture. 67
6.2 A simplified schematic of the implemented 10 GS/s sampler core, consisting of the input buffer, the multiplier, the DEMUX and the integrators. 69
6.3 A simplified schematic of the implemented TIA. 70
6.4 A simplified schematic of the active reset circuit. 71
6.5 A simplified schematic of the implemented buffer amplifiers, MUX and output driver. 71
6.6 A chip photograph of the processed die, containing two identical 10 GS/s sampler units. 72

6.7 A simplified block diagram of the setup used for the characterization of the implemented 10 GS/s sampler. 73

6.8 A photograph of the measurement setup used for the characterization of the implemented 10 GS/s sampler. 75

6.9 a) Measured variation in time of the voltage at the two single-ended outputs of the 10.08 GS/s sampler as response to a sinusoidal input signal with a frequency of f_{in} = 10.08126 GHz, digitized with a RTO with $f_{s,RTO}$ = 40 GS/s. b) The difference of these single-ended signals, which represents the actually wanted differential signal. 76

6.10 Corresponding spectrum calculated from the signal shown in Fig. 6.9 b). 77

6.11 Harmonic distortions THD, HD2 and HD3 as a function of the input frequency for an optical pulse energy of E_p = 175 fJ. 78

6.12 Measured gain as function of the input frequency of the implemented 10 GS/s sampler core for an optical pulse energy of E_p = 175 fJ. Additional data points are obtained operating the sampler with a reduced sampling rate f_s = 1.26 GS/s. 79

6.13 Calculated 3 dB-bandwidth (solid line) and gain (dashed line) of the sampler as a function of the optical pulse energy. 81

7.1 A simple measurement setup for the characterization of the intrinsic sampler jitter in the time-domain. 84

7.2 Noisy jitter-related cyclostationary variance $\widehat{\sigma_v^2}(\phi)$ obtained from a measurement (solid line), the jitter-sensitive fit function (dashed line), and the corresponding amplitude $\widehat{\sigma_{v,fit}^2}$ to calculate the estimated jitter $\hat{\sigma}_t$. 86

7.3 Noise contribution to the overall $\sigma_v^2(\phi)$ (solid line) on the example of a noisy stationary variance σ_{Ns}^2 (dash-dot line), a triangular-shaped cyclostationary variance $\sigma_{Nc}^2(\phi)$ (dotted line), and the jitter-related noise $\sigma_{Nj,tot}^2(\phi)$ (dashed line). 87

7.4 Cancellation of signal source jitter in a dual-channel measurement setup as a function of the channel skew. Respective sampler bandwidths f_c = 13 GHz and f_c = 30 GHz are considered, whereby an ideal low-pass filter transfer characteristic is assumed. 91

7.5 A flowchart of the implemented digital post-processing algorithm. 93

7.6 A flowchart of the calibration algorithm used for adjusting the post-sampling phase of the waveform recorder. 94

7.7 A block diagram of the setup used for the verification of the proposed jitter measurement method on the example of an electrical high-end 10 GS/s sampler chip. 96

7.8 Results from the post-sampling phase calibration of the waveform recorder: a) The variance $\sigma^2_{v,rms}$ of channel 1 as function of the hardware-controlled time delay (skew) on the example of the first, third and fifth iteration. b) The variance $\Delta\sigma^2_{v,rms}$ calculated from the difference signal of the two channels as a function of the skew on the example of the first, third and fifth iteration. 97

7.9 a) The cyclostationary variances $\sigma^2_{v,hi,S1}$ (solid line) and $\sigma^2_{v,hi,S2}$ (dashed line) calculated from the recorded data of the two sampler outputs as response to a high input signal frequency of $f_{hi} = 11.7\,GHz$. b) The cyclostationary variance $\sigma^2_{v,hi}$ (solid line) obtained from the difference signal of the two channels and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation. 98

7.10 a) The cyclostationary variance $\sigma^2_{v,lo}$ (solid line) obtained from the difference signal of the two channels as response to the low input signal frequency of $f_{lo} = 1.7\,GHz$. In addition, $\sigma^2_{v,hi}$ (dashed line) is shown for comparison. b) The cyclostationary variance $\Delta\sigma^2_v$ (solid line) and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation. 99

7.11 Standard deviation σ_{σ_t} of the estimated jitter $\hat{\sigma}_t$, measured with the electronic 10 GS/s sampler, as a function of the number of acquired samples N_{smp} (solid line). In addition, the maximum allowable standard deviation predicted by the theoretical model is provided for comparative purposes (dashed line). 99

7.12 A block diagram of the setup used for the verification of the proposed jitter measurement method with the photonic-assisted sampler. 100

7.13 a) The cyclostationary variances $\sigma^2_{v,hi,S1}$ and $\sigma^2_{v,hi,S2}$ calculated from the recorded data of the two sampler outputs as response to a high input signal frequency of $f_{hi} = 25.2\,GHz$. b) The cyclostationary variance $\sigma^2_{v,hi}$ (solid line) obtained from the difference signal of the two channels and the corresponding jitter-sensitive fit used for the jitter estimation. 101

7.14 a) The cyclostationary variance $\sigma^2_{v,lo}$ (solid line) obtained from the difference signal of the two channels as response to the low input signal frequency of $f_{lo} = 5.04\,GHz$. In addition, $\sigma^2_{v,hi}$ (dashed line) is shown for comparison. b) The cyclostationary variance $\Delta\sigma^2_v$ (solid line) and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation. 102

7.15 Standard deviation $\sigma_{\hat{\sigma}_t}$ of the estimated jitter $\hat{\sigma}_t$, measured with the photonic-assisted 10 GS/s sampler as a function of the number of the acquired samples N_{smp} (solid line). The maximum allowable standard deviation predicted by the theoretical model is also shown for comparative purposes (dashed line). 103

C.1 A simple model to investigate the effect of timing skew in a two-channel measurement on the efficiency of the noise cancellation. 113

List of Tables

3.1 Summary of the derived top-level specifications. 24

5.1 Performance summary of the implemented O/E clock converter. 65

6.1 Performance summary of the implemented 10 GS/s sampler core. 81

7.1 Performance summary of the RTO and the sampling oscilloscope used in this work. . 92

Glossary

A	Area [m^2]
C	Capacitance [F]
ENOB	Effective Number of Bits
E_g	Band Gap [eV]
G	Gain
HD2	Second Harmonic Distortion [dB]
HD3	Third Harmonic Distortion [dB]
J	Random Process
L_{SSB}	Single-Sideband Phase Noise [dBc/Hz]
NF	Noise Factor
P	Power [W]
R_{PD}	Photodiode Responsivity [A/W]
R	Resistance [Ω]
SINAD	Signal-to-Noise-and-Distortion Ratio [dB]
SNR	Signal-to-Noise Ratio [dB]
$S(f)$	Power Spectral Density [V/Hz]
THD	Total Harmonic Distortion Ratio [dB]
TNHD	Total Non-Harmonic Distortion Ratio [dB]
T_s	Sample Period [s]
T	Temperature [K]
V_t	Thermal Voltage [V]
Z_L	Characteristic Impedance [Ω]
α	Attenuation [dB]
η_{PD}	Quantum Efficiency
λ	Wavelength [m]
ω	Angular Frequency [rad/s]
f_T	Maximum Unity Current Gain Cut-Off Frequency [Hz]

f_s	Sampling Rate [Hz]
f_{3dB}	3 dB-Bandwidth [Hz]
f_{in}	Signal Frequency [Hz]
f_{max}	Maximum Oscillation Frequency [Hz]
f_{rep}	Pulse Repetition Frequency [Hz]
f	Frequency [Hz]
g_m	Transconductance [A/V]
$i(t)$	Current Signal [A]
p	Power [dBm]
t	Time [s]
$v(t)$	Voltage Signal [V]
ν	Frequency of Light [Hz]
ϕ	Phase [rad]
σ_t	Jitter [s]
τ_{FWHM}	Full-Width-at-Half Maximum Pulse Width [s]

Acronyms

SiO_2	Silicon Dioxide
ADC	Analog-to-Digital Converter
BMBF	German Federal Ministry of Education and Research
CB	Common-Base
CDN	Clock Distribution Network
CML	Current-Mode Logic
CoSi	Cobalt Silicide
DC	Direct Current
DEMUX	Demultiplexer
DMM	Digital Multimeter
DNL	Differential Nonlinearity
EDFA	Erbium-Doped Fiber Amplifier
ENOB	Effective Number of Bits
Er:Yb	Erbium-Ytterbium
FSV	Full-Scale Value
FWHM	Full-Width-at-Half-Maximum
Ge	Germanium
HBT	Heterojunction Bipolar Transistor

IHP	Innovations for High Performance Microelectronics
IHT	Institute for Semiconductor Engineering
INL	Integral Nonlinearity
LSB	Least Significant Bit
MIM	Metal-Insulator-Metal
MLL	Mode-Locked Laser
MMI	Multi-Mode Interference Coupler
MOSAIC	Monolithic Integrated Optically-Clocked Sampler Integrated Circuit
MUX	Multiplexer
O/E	Opto-Electronic
OPM	Optical Power Meter
P	Phosphor
PD	Photodiode
PLL	Phase-Locked Loop
PPM	Parts Per Million
R&S	Rohde & Schwarz GmbH & Co. KG
RF	Radiofrequency
RIN	Relative Intensity Noise
RMS	Root-Mean Square
RS	Reset-Set
RTO	Real-Time Oscilloscope
S/H	Sample-and-Hold Circuit
SESAM	Semiconductor Saturable Absorber Mirror
Si	Silicon
SiGe BiCMOS	Silicon Germanium Bipolar Complementary Metal-Oxide Semiconductor

SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon-On-Insulator
SSB	Single Sideband
TEM	Transmission Electron Microscopy
THA	Track-And-Hold Amplifier
THD	Total Harmonic Distortion Ratio
TI	Time-Interleaved
TIA	Transimpedance Amplifier
TNHD	Total Non-Harmonic Distortion Ratio
VOA	Variable Optical Attenuator
WG	Waveguide

Physical Constants

Symbol	Description	Value [1]
c_0	Speed of Light in Vacuum	$299792458\,\mathrm{m/s}$
q	Elementary Charge	$1.602176620898 \cdot 10^{-19}\,\mathrm{C}$
h	Planck Constant	$6.62607004081 \cdot 10^{-34}\,\mathrm{Js}$
k_B	Boltzmann Constant	$1.3806485279 \cdot 10^{-23}\,\mathrm{J/K}$

[1] The values of the physical constants are taken from [1].

Zusammenfassung

Die ständig wachsende Nachfrage an höheren Datenraten fürt zu immer anspruchsvolleren Anforderungen an die Geschwindigkeit und Auflösung von Analog-Digital-Wandlern, welche die zentrale Schnittstelle zwischen der analogen und digitalen Welt darstellen. Die Performance von Hochgeschwindigkeits-Wandlern wird hierbei hauptsächlich beschränkt durch Jitter, welcher die Ungenauigkeit des Abtast-Zeitpunkts beschreibt. Dieser Parameter konnte trotz großer Bemühungen und technologischem Fortschritt in den letzen Jahrzehnten nicht signifikant verbessert werden.
Die hier vorliegenden Arbeit präsentiert einen neuen, photonischen Ansatz zur Überwindung des jitterbezogenen Performance-Limitierung. Hierbei wird ein Mode-Locked Laser als Taktquelle verwendet, welcher einen Puls mit kurzen optischen Impulsen und einer fixen Pulswiederholrate emittiert. Die Jitter-Performance dieser Laser übertrifft die von rein elektrischen Oszillatoren um Größenordnungen, und das selbst bei Gigahertz-Wiederholraten. Verteilt man das optische Taktsignal mit monolithisch integrierten Silizium-Wellenleitern im Chip, so lässt sich eine zeitlich verschachtelte Architektur zur Erhöhung der Abtastrate realisieren, ohne zusätzlichen Jitter hinzuzufügen.
Mit Blick auf die Anforderungen der Messtechnik von Morgen zielt das Systemdesign auf einen Wandler ab mit einer Abtastrate von $f_s = 80\,\mathrm{GS/s}$, einer Bandbreite $f_{3dB} > 30\,\mathrm{GHz}$ und einer effektiven Auflösung von 8 Bits ab. Hierfür werden zunächst die Spezifikationen für die einzelnen System-Kompenenten gemäß dem Top-Down-Ansatz hergeleitet. Die Vorteile des photonischen Ansatzes werden anschließend mit zwei Demonstrator-Chips nachgewiesen. Als Erstes wird ein opto-elektrischer Taktkonverter als Schlüsselkomponente für viele unterschiedliche jitter-arme Anwendungen präsentiert, welcher das optische Signal des Lasers in ein elektrisches Rechtecksignal wandelt. Mit einer Rausch-Analyse der Schaltung werden die Vorteile dieses Ansatzes in der Theorie gezeigt, während die Messergebnisse das Potential der Schaltung praktisch darlegen. Anschließend wird ein 10 GS/s Sampler als Kern-Kompenente für den angestrebten 80 GS/s Wandler präsentiert. Hierbei wurde eine Puls-Sampling-Architektur hierbei gewählt, da von dieser eine deutlich bessere Jitter-Performance zu erwarten ist als von einer klassischen Track-And-Hold-Architektur. Messungen an den hergestellten Testchips zeigen eine Bandbreite $f_{in} > 30\,\mathrm{GHz}$, ein $\mathrm{THD} < -33\,\mathrm{dB}$ über das gesamte Frequenzband, und ein $\mathrm{SNR} = 35\,\mathrm{dB}$. Für die Charakterisierung der Jitter-Performance des Samplers wurde ein neues Verfahren entwickelt, mit welchem sich Jitter-Werte im erwarteten Femtosekunden-Bereich messen lassen. Die Beständigkeit und Genauigkeit des entwickleten Verfahrens werden messtechnisch, unter anderem mit dem entwickelten 10 GS/s Sampler, gezeigt.

Abstract

The continuously increasing demand for higher data rates lead to higher requirements on the speed and resolution of analog-to-digital converters as key interface between the analog and digital domain. Herein, the performance of high-speed analog-to-digital converters is mainly limited by the accuracy of the sampling instant. Its uncertainty is known as clock jitter, and it has not been significantly improved over the last decades and the technology improvements.

In this thesis, a novel photonic approach is presented to overcome the jitter-related performance limitations. Herein, a mode-locked laser is used as clocking source. It provides an optical train consisting of ultra-short pulses with a fixed pulse repetition rate and with orders of magnitude lower jitter compared to electronic oscillators. In addition, distributing the optical clock by a network of integrated silicon waveguides does not involve a significant jitter penalty, which allows to implement a time-interleaved architecture to further increase the sample rate.

Targeting the requirements of the next-generation test and measurement instrumentation, the system design of an 8x time-interleaved Analog-to-Digital Converter with a sampling rate of $f_s = 80\,\mathrm{GS/s}$, a bandwidth in the millimeter wave range ($f_{in} > 30\,\mathrm{GHz}$), and an effective resolution of 8 bits is presented. A detailed system analysis according to the top-down approach is used to derive the specifications for the individual system components. The advantage of the photonic approach is then demonstrated with two test chips. At first, an opto-electronic clock converter, as key enabling block for various low-jitter applications, was developed. It turns the optical pulse train coming from the laser into a low-jitter electrical square-wave signal. A noise analysis of the circuit is given to demonstrate the advantages of the photonic approach in theory, while the measurement results of the implemented test chips verify its potential in practice. Hereby, a wideband phase noise floor of $L_{SSB} < -166\,\mathrm{dBc/Hz}$ was measured, which corresponds to a jitter of only $\sigma_t < 11.2\,\mathrm{fs}$.

Furthermore, a 10 GS/s sampler core unit suitable for the implementation in the proposed 80 GS/s time-interleaved ADC was designed. Therefore, a pulse-sampling architecture was used due to its superior jitter performance compared to a classical track-and-hold architecture. Measurements on the fabricated test chips have shown a bandwidth $f_{in} > 30\,\mathrm{GHz}$, a $\mathrm{THD} < -33\,\mathrm{dB}$ over the entire band, and a $\mathrm{SNR} = 35\,\mathrm{dB}$. Regarding the measurement of the samplers jitter performance, a novel method was developed to measure the intrinsic sampler jitter in the expected femtosecond range. The consistency and accuracy of the developed approach are experimentally demonstrated, amongst others on the developed 10 GS/s sampler, revealing an outstanding jitter of $\sigma_t < 30\,\mathrm{fs}$.

Acknowledgements

I want to take the chance to acknowledge and thank the people, who provided technical guidance and moral support during this thesis:

First of all, I want to thank my supervisors and colleagues for their continuously support and the endless in-depth technical discussions: Prof. Dr. habil. Jörg Schulze, Dr. Robert Elvis Makon, Dr. Oliver Landolt, Kai Ulbricht, Kirill Gorelik, Harald Wickenhäuser, Edgar Krune, Simon Pippers, Philipp Steingruber, Carlo van Driesten, Dr. Alexandru Negut, Dr. Dieter Knoll, Ols Hidri, Matthieu Fernandez, Dieter Schiggas, Dr. Lukas Krainer, Dr. Lars Zimmermann, Dr. Thomas Huber, Peter Regner, Ilan Melczarsky, Dr. Alexander Schild, Dr. Ingo Dettmann, Dr. Gerhard Kahmen, Thomas Schweiger, and Thomas Rabenstein.
In addition, I owe my thanks to the group of Dr. Gerd Hechtfischer, in particular Joseph Bachmair, Anna Bridier and Dr. Michael Aigle, for sharing their expert knowledge in optical and on-wafer measurements.
Furthermore, I want to thank Rohde & Schwarz GmbH & Co. KG and the German Federal Ministry of Education and Research (BMBF) for providing the financial support for such an interesting and topical field.
Besides the technical support, this thesis would not have been possible without the moral support of my family and friends during my whole lifetime.

And finally, the greatest thanks go to my beloved wife. My research and this thesis would not have been possible without her continuous support and interest. She has always been my constant source of inspiration and encouragement, and I am infinitely grateful to share the rest of my life with my soulmate!

1 Introduction

1.1 Motivation

Since the beginning of the digital age, a major amount of the analog operations was transferred into the digital domain, coming along with the commonly-known advantages of being more flexible, controllable, more cost-effective, and less time-consuming. Herein, the Analog-to-Digital Converter (ADC) as the interface between the analog physical and the digital domain of signal processing has become a key enabling block. Regarding wideband applications such as high-end instrumentation, wireless communications, or radar applications, the performance of the ADC often limits the overall system performance, and a lot of effort was spent to improve the speed and the accuracy of the converters. On the way towards higher resolution of high-frequency signals, clock jitter has become the major bottleneck [2] of the ADC performance. In general, jitter is a stochastic timing uncertainty, and with respect to the sampler application, it describes a deviation from the ideal sampling instant. As a consequence, an error is introduced during the sampling process and the overall ADC performance is degraded. Although a lot of innovation has been driven to improve the jitter performance of electronic ADCs, it has not been decreased significantly for the last two decades.

Fig. 1.1 shows the dynamic performance of electronic ADCs, which is defined by their Effective Number of Bits (ENOB), as a function of the maximum input frequency for ADCs published in [3]. For later discussion, ADCs using a Time-Interleaved (TI) architecture are highlighted by a blue circle. In addition, the solid and dashed lines representing limits due to the jitter are also shown in the plot. The performance is significantly decreased for high frequency signals, and the best ADCs deliver a jitter in the range of $\sigma_t = 100\,\text{fs}$. The lowest jitter value found in the literature was $\sigma_t = 60\,\text{fs}$ for a 32x TI, 36 GS/s ADC [4], respectively a 64x TI, 90 GS/s ADC [5]. In addition, it has recently been shown that technology scaling shows no significant improvement on the jitter performance of the converters [6]. With respect to next-generation instrumentation and measurement systems, a target resolution of ENOB > 8 bits for input frequencies in the millimeter wave range ($f_{in} > 30\,\text{GHz}$) at a sampling rate of $f_s > 80\,\text{GS/s}$ is pursued. This requires a jitter in the range of $\sigma_t < 20\,\text{fs}$, which is an extremely challenging task. The major goal of this work is to demonstrate that jitter-limited ADC performance can be significantly improved using a photonic approach.

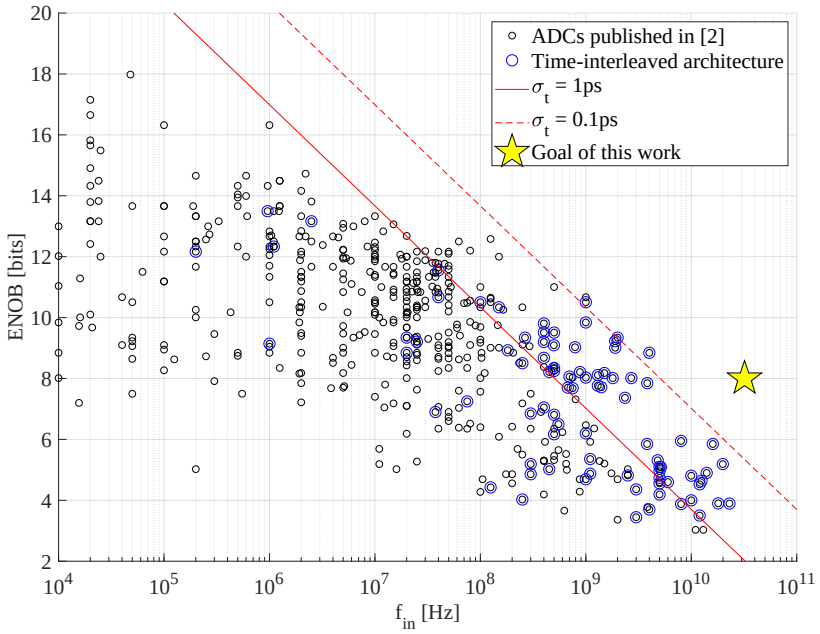


Figure 1.1: ENOB as a function of the analog signal frequency for state-of-the-art ADCs published in [3] and theoretical limits due to jitter σ_t.

Concentrating on the GHz regime in Fig. 1.1, one may notice that the TI architecture is the one most commonly used. A block diagram of the TI architecture is shown in Fig. 1.2. It consists of N sub-ADCs, each providing the full acquisition bandwidth and operating at a sample rate reduced by the factor of N. The phases ϕ_i of the clock signals are distributed equally across the full sample

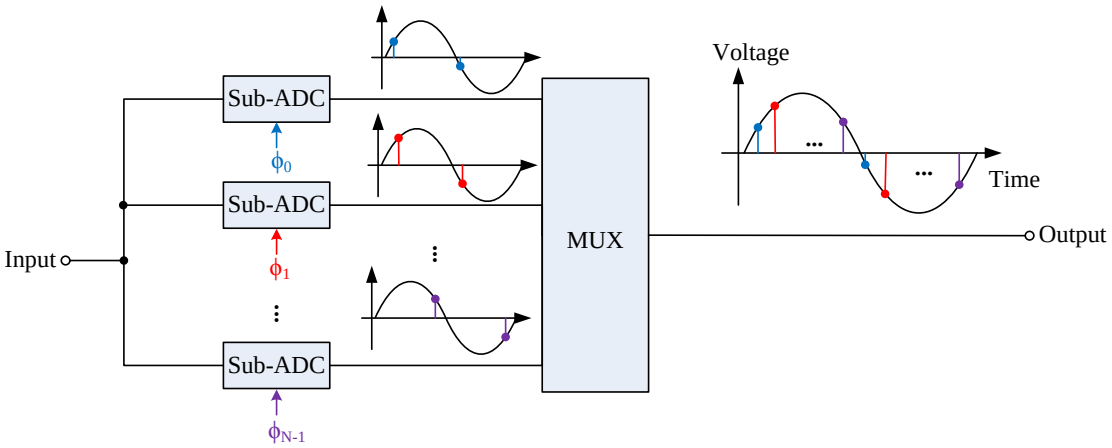


Figure 1.2: A block diagram of a TI architecture.

period. A Multiplexer (MUX) at the output merges the data streams to form the full-rate sample stream. Designing each sub-ADC for the highest sampling rate in a given process, the TI architecture can be used to overcome this physical limitation. Alternatively, the TI architecture can be used in a energy-efficient design. Having a reduced sampling rate of the sub-ADCs, more time is available to perform the sample-and-hold and the comparison operations, which can be very power consuming for small conversion times.

Regarding the jitter performance, the electrical clock distribution is the major bottleneck in such an architecture. A Clock Distribution Network (CDN) is typically designed as a tree, spine, grid, or a hybrid of those topologies [7]. Fig. 1.3 illustrates a CDN on the example of a symmetrical H-tree, which distributes the clock signal generated by an oscillator to eight ADCs. Since the driving capability of the clock source is commonly limited, buffer amplifiers are required to drive the total capacitive load, consisting of the input capacitance of the subsequent stage and the capacitive load of the transmission line. Each buffer adds noise to the clock signal, therefore the jitter at the output of the chain is the quadratic sum of the jitter values of each stage.

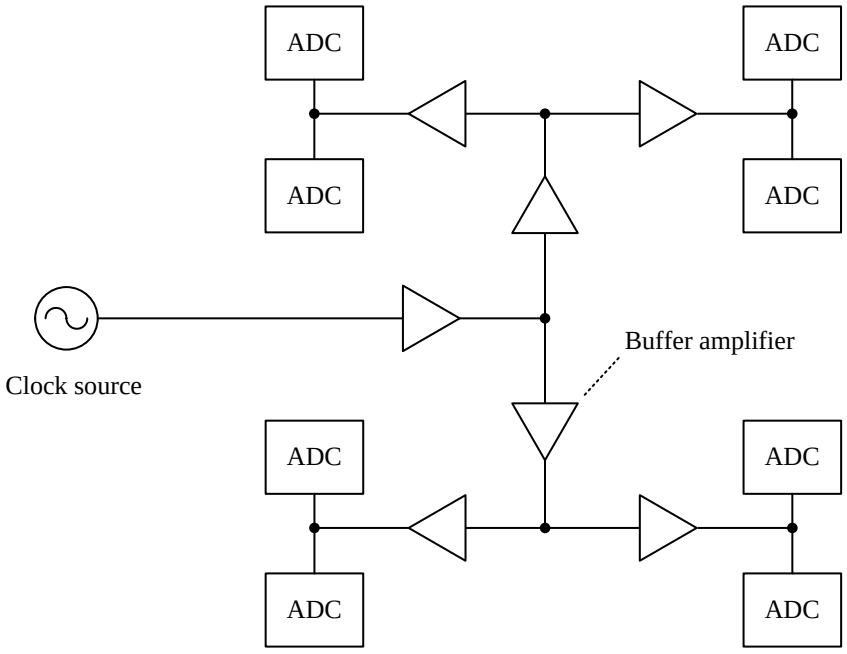


Figure 1.3: A CDN on the example of a symmetrical H-tree topology.

A promising approach to significantly push forward the jitter-related performance limitations of ADCs is photonic-assisted sampling. Herein, an optical pulse train provided by a Mode-Locked Laser (MLL) is used as frequency source for clocking an electronic ADC. The main motivation arises from

the superior jitter performance of the MLL, showing jitter levels many orders of magnitude lower than their electronic counterparts [2]. For example, MLLs with a subfemtosecond jitter performance [8] even for gigahertz repetition rates [9], [10] have been reported. Furthermore, distributing the optical clock through a network of optical Waveguides (WGs) does neither involve a significant jitter or distortion penalty, nor suffer from additional commonly-known problems (power consumption, mismatch, crosstalk, etc.) of the electronic distribution of multi-gigahertz clock signals [11].
The potential of photonic-assisted architectures to improve the performance of an electronic ADC leads back to the 1970s [12]. Although the purpose of the first "photonic ADC" was used to determine the pulsewidth of picosecond lasers [13], the potential for generating and measuring electrical signals with a high time resolution has been well acknowledged by various authors [14], [15], [16], [17], [18], [19]. Optoelectronic switches have shown much faster rise times and lower pulse-to-pulse jitter than their electronic counterparts, thus allowing the processing of high-frequency signals with much higher accuracy.
In [20], an optically clocked diode-bridge, triggered by a MLL, was proposed to sample an electronic signal. In addition to the jitter improvement, this approach provides an improved nonlinear response of the bridge due to the reduced aperture time. Using this approach, an ENOB of 9.6 bits was demonstrated for an input frequency of $f_{in} = 1.0073\,\text{GHz}$ and a sampling rate of $f_s = 1.003\,\text{GS/s}$ [21], which corresponds to a jitter of $\sigma_t = 170\,\text{fs}$.
In [2], a discrete-component photonic ADC was built to demonstrate the low-jitter sampling of high-frequency signals. Using a 2x TI sampler with a sample rate of $f_s = 2.1\,\text{GS/s}$, an ENOB of 7 bits for an input frequency of $f_{in} = 41\,\text{GHz}$ was measured, which corresponds to a jitter as low as 25 femtoseconds.
But all of the recent works have in common that they are either hybrid solutions, where electronics-only chips are combined with separate-fabricated photonic-only chips, or the optical components are implemented off-chip. However, to be able to compete with electronic ADCs, the electronic and photonic devices must be integrated into a single chip. Monolithic integration enables robustness, miniaturization, low-cost mass production, and the potential to improve the power efficiency. In addition, a seamless signal integrity, by eliminating interconnects between separate chips, minimizes the integration-related parasitics and enables highest possible speed [22].
Embedded in the "Monolithic Integrated Optically-Clocked Sampler Integrated Circuit (MOSAIC)" project funded by the German Ministry of Education and Research (13N12435), the scope of this work will focus on the system design of an 80 GS/s TI ADC, and the circuit design of a 10 GS/s sampler providing an analog bandwidth $f_{3dB} > 30\,\text{GHz}$ as the corresponding key component. Applying the so-called top-down approach, the specifications for the individual system components are derived to provide the design goals for the project partners. In addition, an optically-clocked clock converter circuit and a 10 GS/s sampler core unit are implemented as demonstrators for the feasibility of the photonic-assisted approach and its advantages compared to purely electronic solutions are demonstrated.

1.2 Thesis Overview

The structure of this thesis is organized as follows:

- Chapter 2 introduces some ADC fundamentals, which are required for the basic understanding of this work. Furthermore, the influence of error sources on the static and dynamic ADC performance is presented. Herein, the main focus is laid on the jitter as major bottleneck of high-speed ADCs.
- In Chapter 3, the specifications for the individual components in the 80 GS/s TI ADC are derived from the requirements on the overall ADC performance. Based on these specifications, the development and optimization of the components are coordinated to meet the design goals.
- Chapter 4 provides an overview of the implementation of the system components and a comparison of the reached performance with the specifications. At first, a review of the photonic Silicon Germanium Bipolar Complementary Metal-Oxide Semiconductor (SiGe BiCMOS) technology is presented, followed by an overview of the individual system components. Two sampling architectures suitable for a high-performance and high-resolution sampling operation are presented and fundamental performance limitations are derived.
- Chapter 5 presents the design and the characterization of a low-jitter Opto-Electronic (O/E) clock converter, which turns the optical pulse train of the MLL into a low-jitter electrical square-wave signal. A detailed jitter analysis of the circuit demonstrates the superiority of the proposed photonic approach for clock distribution compared to a pure electronic solution. Measurement results of the implemented test chip substantiate the theoretical results and conclude this chapter.
- Chapter 6 presents the design of the proposed 10 GS/s sampler core unit suitable for the integration in the 80 GS/s TI ADC, followed by the measurement results of the implemented test chip.
- In Chapter 7, a novel method for measuring ultra-low sampler jitter is presented. Based on the fundamental properties of jitter-induced noise, a cyclostationary stochastic approach is used to extract jitter-induced noise from other error sources in the measurement setup. The consistency and accuracy of the developed approach are experimentally demonstrated, amongst others on the developed 10 GS/s sampler.
- Chapter 8 concludes this thesis and provides an outlook for the future work.

2 ADC Fundamentals

In this chapter the fundamentals of the analog-to-digital conversion are introduced. Based on the ideal sampling operation, the quantization noise is identified as a fundamental performance limitation. In addition, the influence of other error sources on the ADC performance are discussed. Thereby, the main focus is on jitter as major bottleneck of wideband ADCs.

2.1 Sampling Basics

Fig. 2.1 illustrates a simple block diagram of an ADC. Its fundamental task - converting an analog signal at equidistant time instants $\Delta t = T_s$ into a digital representation - can be split into two basic functions:

1. A Sample-and-Hold Circuit (S/H) upfront samples the analog signal v(t) and holds it for a specified time ΔT, which is required for

2. the quantization of the held value by a digitizer.

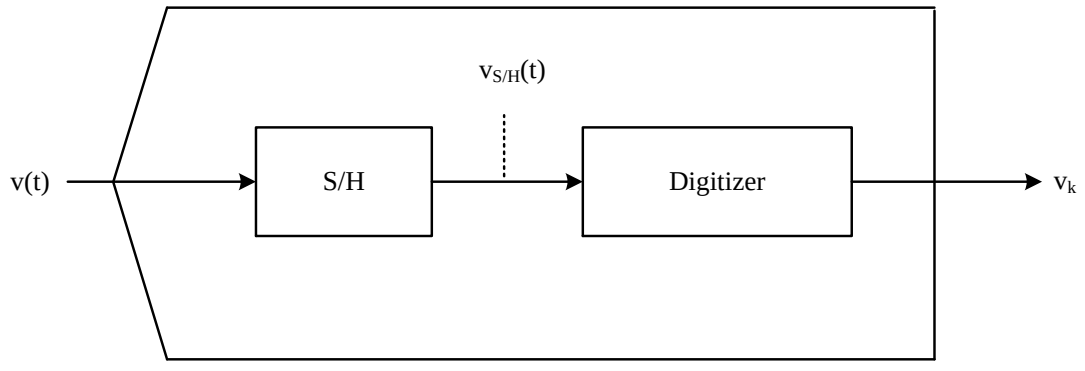


Figure 2.1: A block diagram of an ADC.

The ideal sample and hold operation is mathematically described by [23]:

$$v_{S/H}(t) = \left[v(t) \cdot \sum_{k=-\infty}^{\infty} \delta_0(t - k \cdot T_s) \right] * \text{rect}\left(\frac{t}{\Delta T}\right), \tag{2.1}$$

where $\delta_0(t)$ is a Dirac impulse, T_s the sample period, and "$*$" the convolution. In Eq. 2.1, the ideal sampling operation is represented by the multiplication with the Dirac pulse, while the hold operation corresponds to the convolution with a rectangular function

$$\text{rect}\left(\frac{t}{\Delta T}\right) = \begin{cases} 1, & \text{if } \frac{|t|}{\Delta T} < \frac{1}{2} \\ \frac{1}{2}, & \text{if } \frac{|t|}{\Delta T} = \frac{1}{2} \\ 0, & \text{otherwise} \end{cases} \tag{2.2}$$

In the frequency domain, the spectrum of the continuous time sampled-and-held signal is given by [23]:

$$V_{S/H}(j \cdot \omega) = \mathcal{F}\left\{v_{S/H}(t)\right\} \tag{2.3}$$

$$= \frac{\Delta T}{T} \cdot \text{sinc}\left(\omega \cdot \frac{\Delta T}{2}\right) \cdot \sum_{\nu=-\infty}^{\infty} V\left(j \cdot \left(\omega - \nu \cdot \frac{2 \cdot \pi}{T}\right)\right), \tag{2.4}$$

where $\mathcal{F}\{\cdot\}$ is the Fourier transform

$$\mathcal{F}\{x(t)\} = \int_{-\infty}^{\infty} x(t) \cdot e^{-j \cdot \omega \cdot t} dt, \tag{2.5}$$

sinc(x) is the sinus cardinalis

$$\text{sinc}(x) = \frac{\sin(x)}{x}, \tag{2.6}$$

and $V(j \cdot \omega) = \mathcal{F}\{v(t)\}$ is the spectrum of the input signal.

According to Eq. 2.4, the spectrum at the output of the S/H consists of copies of the input signal spectrum, which repeat periodically with the angular sampling frequency $\omega_s = 2 \cdot \pi / T_s$, and which are scaled by the sinc function given in Eq. 2.6. It should be noted that the hold time ΔT serves merely to provide enough processing time for the digitizer, but it does not affect the signal value to be digitized. Therefore, the corresponding sinc distortion is indeed present at the analog output of the S/H, but it does not affect the discrete time frequency response of the sampler.

Fig. 2.2 illustrates these fundamental relations. Fig. 2.2 a) shows the variation in time of an ideal S/H output $v_{S/H}(t)$ for the given input signal v(t) (dashed blue line). In the example, the width ΔT is equal to the sample period T_s.
Fig. 2.2 b) shows the corresponding spectrum as well as the spectrum of the band-limited input signal. Herein the bandwidth BW of the input signal is limited to fulfill the Nyquist criterion

$$BW < \frac{f_s}{2}, \tag{2.7}$$

which is required to guarantee a perfect reconstruction of the input signal [23].

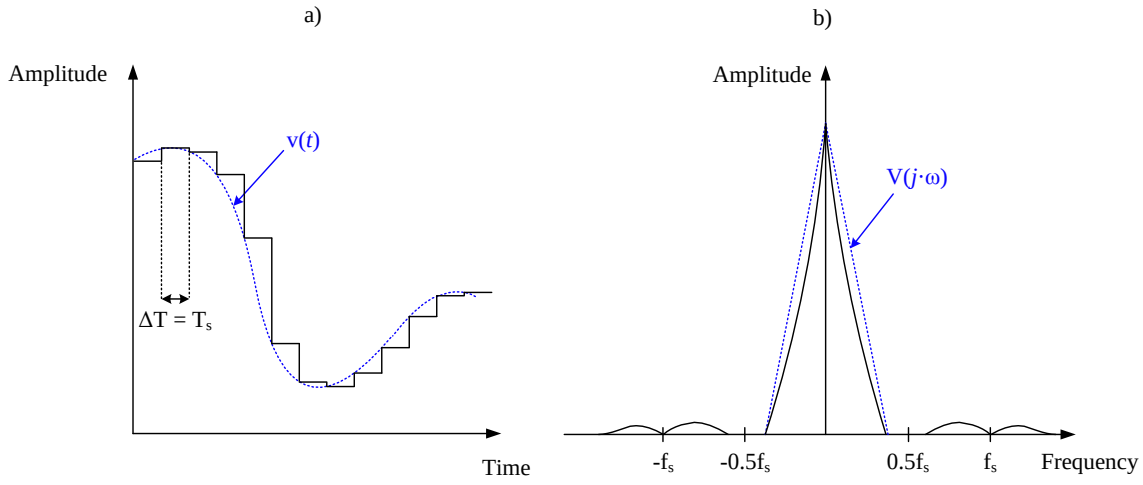


Figure 2.2: a) Variation in time of an ideal S/H output (solid line) for the given input signal v(t) (dashed line). In this example, the width ΔT of the rectangular function is equal to the sample period T_s. b) Spectrum at the S/H output (solid line) and spectrum of the input signal (dashed line).

The digitizer maps the continuous amplitude values from a given input range $v_{range} = v_{max} - v_{min}$ to discrete values v_Q, which are finally allocated to a digital representation:

$$v_Q(k \cdot T_s) = Q\left\{v_{S/H}(k \cdot T_s)\right\}. \tag{2.8}$$

Herein, Q represents the quantization operator. As an example, the quantization diagram of a linear quantizer with N = 4 bits is illustrated in Fig. 2.3. The quantization interval Δv - which is also known

as Least Significant Bit (LSB) - is given by

$$\Delta v = \frac{v_{range}}{2^N}. \tag{2.9}$$

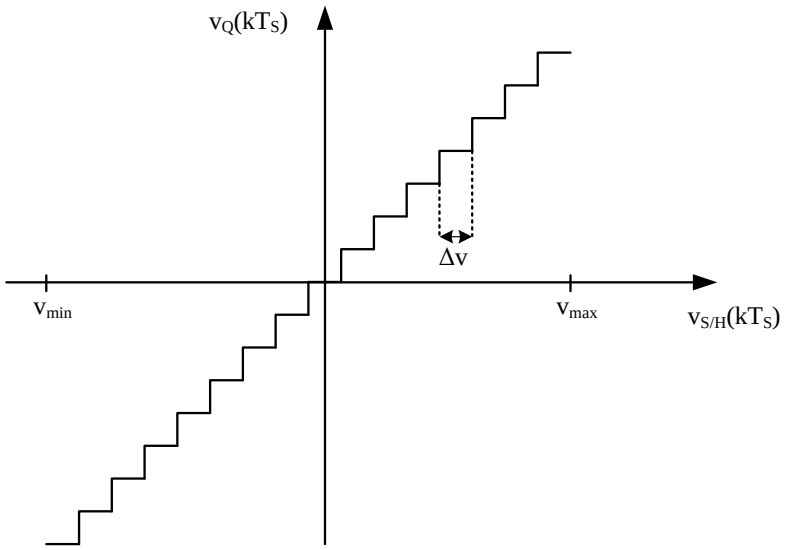


Figure 2.3: A quantization diagram of a linear mid-tread quantizer with N = 4 bits.

This so-called mid-tread characteristic provides a true representation of the zero value, but it introduces an asymmetry for an even number of codes. This can be avoided by shifting the curve to the left by half of the quantization interval, but with the disadvantage of not providing a true representation of the value zero.

Quantization inherently introduces an error due to the truncation. Assuming an equal probability distribution of the quantization error within every amplitude interval and assuming that the quantization error is not correlated with the input signal, the variance σ_Q^2 of the quantization noise is given by [23]:

$$\sigma_Q^2 = \frac{\Delta v^2}{12}. \tag{2.10}$$

As a consequence, the noise due to the quantization represents one fundamental limitation of the performance of an ADC. Usually, the performance of an ADC is described by the Signal-to-Noise Ratio

(SNR) in dB, which is defined as the ratio of the Root-Mean Square (RMS) of the input signal power P_s and the RMS of the noise power P_n:

$$SNR = 10 \cdot \log_{10}\left(\frac{P_s}{P_n}\right). \tag{2.11}$$

Assuming an ideal N-bit ADC with quantization noise as a single noise source and a sinusoidal input signal covering the full-scale input range of the quantization diagram, the SNR is then given by [23]:

$$SNR_{Quant} = 6.02 \cdot N + 1.76. \tag{2.12}$$

In the practical implementation, there are other error sources which degrade the overall ADC performance. They can be basically separated into two groups: the first group represents the influence on the Direct Current (DC) accuracy and the static performance, while the second group affects the dynamic performance of an ADC.

2.2 Static Performance of ADCs

The DC accuracy is important when measuring relatively static signals, such as data from sensors or transducers. Since this work focuses on the dynamic performance of the ADC, only a short summary of the static specifications is given for the sake of completeness:

1. The **offset error** describes the deviation of quantization diagram from its ideal behavior. It is usually specified in Volts, LSB, % Full-Scale Value (FSV), or Parts Per Million (PPM).

2. The **full-scale or gain error** describes the difference between the ideal voltage which provides full-scale output code and the actual voltage for which the converter provides a full-scale output. It is usually specified in Volts, LSBs or % FSV.

3. The **Differential Nonlinearity (DNL)** describes the deviation of the actual step size observed for each ADC code from the ideal step size Δv. It is usually specified in LSBs or % FSV.

4. The **Integral Nonlinearity (INL)** describes the deviation of the actual transfer function with respect to the ideal transfer function. It is usually specified in LSBs or % FSV.

A detailed overview is given in [24].

2.3 Dynamic Performance of ADCs

2.3.1 Noise in Analog Signal Path

In the analog signal path, a fundamental noise limit is given by Johnson-Nyquist-noise - also known as thermal noise - which results from the thermal carrier movement in the electronic circuit. It is considered to be white, which means that it has a flat spectrum within the considered bandwidth. Its power spectral density $S_{n,th}(f)$ is given by:

$$S_{n,th}(f) = 4 \cdot k_B \cdot T \cdot R_L, \tag{2.13}$$

where k_B is the Boltzmann constant, T the temperature, and R_L the effective thermal noise resistance. The variance $\sigma^2_{v,th}$ of the voltage noise over the bandwidth interval Δf is then given by:

$$\sigma^2_{v,th} = \int_0^{\Delta f} S_{n,th}(f) df = 4 \cdot k_B \cdot T \cdot R_L \cdot \Delta f \tag{2.14}$$

Regarding the sampler application, the sampled signal value is usually represented as the voltage of the hold capacitor. A simple model to illustrate a fundamental noise limit of a sampler is shown in Fig. 2.4. In the hold mode, the ideal switch is opened and the voltage at the output is equal to the voltage at the capacitor. In the sample mode, the closed switch is represented by its on-state resistance R_{on}.
The power transfer function from the input to the output is then given by:

$$|H_{RC}(f)|^2 = \frac{1}{1 + (2 \cdot \pi \cdot R_{on} \cdot C_H \cdot f)^2}. \tag{2.15}$$

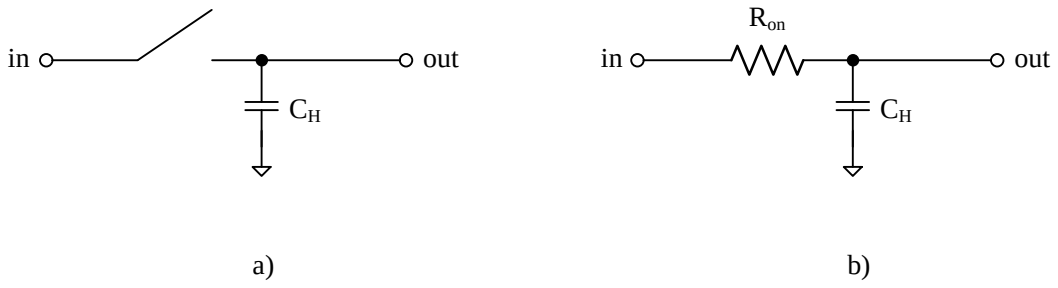


Figure 2.4: Simple model of a sampler a) in the hold mode and b) in the sample mode.

The variance of the voltage noise $\sigma^2_{\mathrm{RC,tot}}$ at the output of the sampler is then obtained by integrating the power spectral density, formed by the power transfer function:

$$\sigma^2_{\mathrm{RC,tot}} = \int_0^\infty \mathrm{S_{n,th}}(f) \cdot |\mathrm{H_{RC}}(f)|^2 \, \mathrm{d}f = \frac{\mathrm{k_B \cdot T}}{\mathrm{C_H}}. \tag{2.16}$$

Eq. 2.16 is a quite interesting result, since it states that the output noise generated by the resistor is a function of the temperature and the capacitance only, but independent of the value of the resistance. This results from the fact that the value of $\mathrm{R_{on}}$ affects the spectral noise density (Eq. 2.14) and the bandwidth of the RC-circuit, and both effects compensate each other.
As shown in [25], Eq. 2.16 remains valid when the switch is periodically turned on, and the output is sampled at the same period $\frac{1}{\mathrm{f_s}}$. Therefore, the $\frac{\mathrm{k_B \cdot T}}{\mathrm{C_H}}$ noise is another fundamental limit next to the quantization noise.
It should be noted that there are a lot of other noise sources in the actual sampler circuit, such as shot noise of the transistors, noise of the biasing circuits, etc., which contribute to the overall SNR.

2.3.2 Harmonic Distortions in Analog Signal Path

In addition to the noise, the ADC performance in the signal path is affected by harmonic distortions, which originate from the non-linear behavior of the amplifier circuits within the ADC. They are described by the Total Harmonic Distortion Ratio (THD), which is defined as the ratio of the power of the first $\mathrm{N_{harm}}$ harmonics to the fundamental signal power $\mathrm{P_{sig}}$:

$$\mathrm{THD} = 10 \cdot \log_{10} \left(\frac{\sum_{\mathrm{n=2}}^{\mathrm{N_{harm}}} \mathrm{P_i}}{\mathrm{P_{sig}}} \right). \tag{2.17}$$

2.3.3 Non-Harmonic Distortions due to Gain and Offset Mismatch

Dealing with a TI architecture as presented in Chapter 1, non-harmonic distortions originate from offset and gain mismatch between the individual ADCs. Fig. 2.5 a) illustrates the error, induced by the offset mismatch, on the example of an ideal sinusoidal signal, sampled with a 4x TI ADC. The error depends on the absolute value of the offset mismatch and is independent of the signal waveform. In the frequency domain, the offset mismatch of an $\mathrm{N_{int}}$-times interleaved ADC manifests through discrete tones at $\mathrm{f_{spur}} = \mathrm{k} \cdot \frac{\mathrm{f_s}}{\mathrm{N_{int}}}$, $\mathrm{k} \in \mathbb{N}$.
Considering a sinusoidal input signal, the Total Non-Harmonic Distortion Ratio (TNHD) is given by

[26]

$$\mathrm{TNHD}_{\delta \mathrm{O}} = 10 \cdot \log_{10}\left(\frac{\mathrm{N_{int}}}{\mathrm{N_{int}} - 1} \cdot \frac{\mathrm{P_{sig}}}{\sigma_{\mathrm{o}}^2}\right), \tag{2.18}$$

where σ_{o}^2 is the variance of a normally-distributed, zero-mean offset and TNHD is the ratio of the fundamental signal power $\mathrm{P_{sig}}$ to the power of all non-harmonic tones $\mathrm{P_{nh,i}}$:

$$\mathrm{TNHD} = 10 \cdot \log_{10}\left(\frac{\mathrm{P_{sig}}}{\sum_{\mathrm{i}} \mathrm{P_{nh,i}}}\right). \tag{2.19}$$

Fig. 2.5 b) illustrates the error induced by the gain mismatch for the same configuration. This time, the error depends on the amplitude of the signal at the sampling instant, and it can be considered as an amplitude-modulation of the input signal. Regarding a sinusoidal input signal with a frequency $\mathrm{f_{in}}$, a gain mismatch results in discrete tones occuring at the frequencies $\mathrm{f_{spur}} = \frac{\mathrm{k} \cdot \mathrm{f_s}}{\mathrm{N_{int}}} \pm \mathrm{f_{in}}$ ($\mathrm{k} \in \mathbb{N}$). The corresponding $\mathrm{TNHD}_{\delta \mathrm{G}}$ is given by [26]:

$$\mathrm{TNHD}_{\delta \mathrm{G}} = 10 \cdot \log_{10}\left(\frac{\mathrm{N_{int}}}{\mathrm{N_{int}} - 1} \cdot \frac{1}{\sigma_{\mathrm{G}}^2}\right), \tag{2.20}$$

where σ_{G}^2 is the variance of a normally-distributed, zero-mean gain.

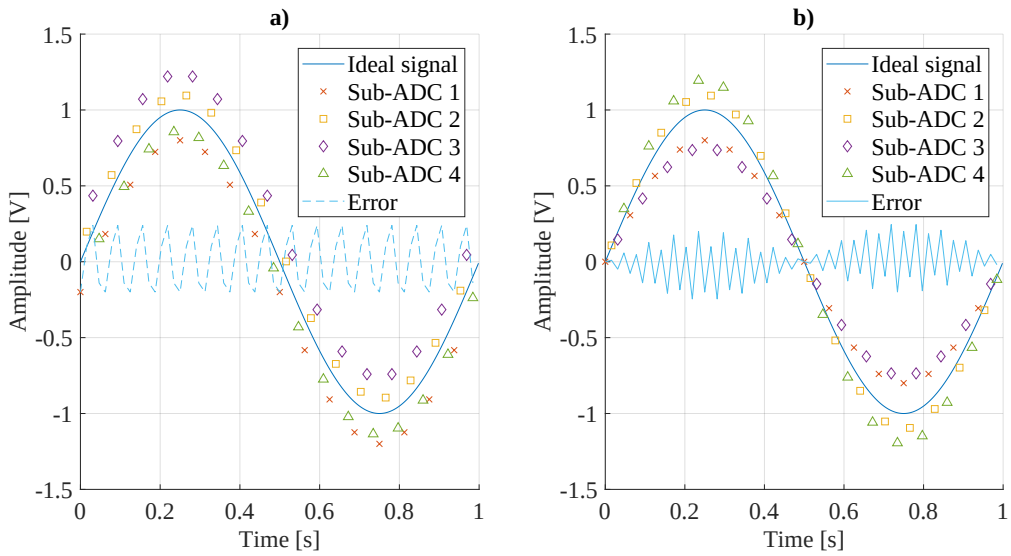


Figure 2.5: Errors induced by a) offset mismatch, respectively b) gain mismatch on the example of a sinusoidal signal sampled with a 4x TI ADC.

2.3.4 Non-Harmonic Distortions due to Timing Skew

A timing skew is a static timing error between the sub-ADCs of a TI-ADC architecture. Its effect on the sampling operation is shown in Fig. 2.6 on the example of sampling a sinusoidal signal with a 4x TI ADC. In the presence of skew, an error proportional to the slope of the input signal is introduced. Thus, the input signal is effectively phase-modulated by the sampling operation, resulting in discrete tones at the frequencies $f_{spur} = \frac{k \cdot f_s}{N_{int}} \pm f_{in}$ ($k \in \mathbb{N}$) in the spectrum. Assuming that the skew is a normally-distributed, zero-mean random variable with a variance σ^2_{skew}, the TNHD is given by: [26]

$$TNHD_{skew} = 10 \cdot \log_{10}\left(\frac{N_{int}}{N_{int}-1} \cdot \frac{1}{(2 \cdot \pi \cdot f_{in} \cdot \sigma_{skew})^2}\right). \tag{2.21}$$

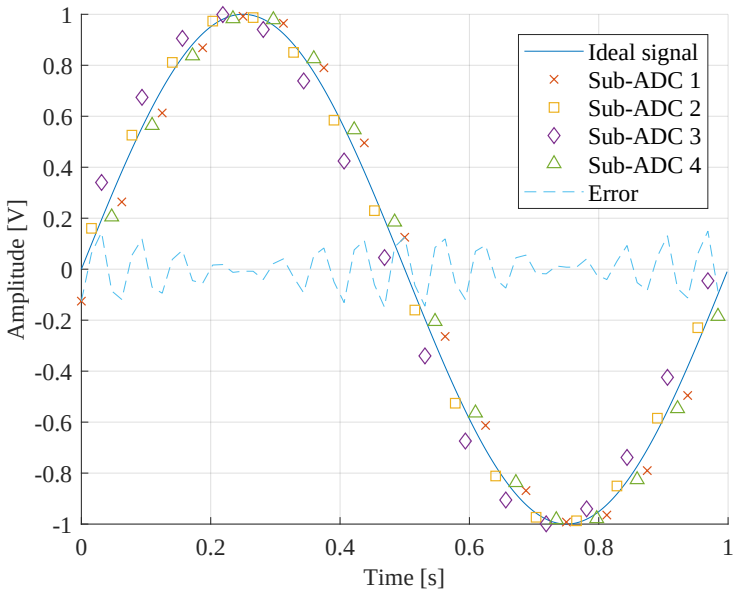


Figure 2.6: Error induced by timing skew on the example of sampling a sinusoidal signal with a 4x TI ADC.

2.3.5 Clock Jitter

In general, jitter describes a stochastic timing uncertainty. In the literature, a number of different jitter definitions (cycle, cycle-to-cycle, period, accumulated, absolute, long-term, and for each of those the RMS, 3-sigma, peak, peak-to-peak value can be provided) can be found, and the choice of the “correct”

specification depends on the considered system and measurement [27]. In the following, the jitter σ_t is defined as the standard deviation of a normally distributed random process J_t with zero mean μ_t:

$$\mathrm{J_t} \sim \mathcal{N}(\mu_\mathrm{t} = 0, \sigma_\mathrm{t}^2). \tag{2.22}$$

In order to understand the impact of the jitter on the sampling operation, the signal $\mathrm{v}(t)$ to be sampled is linearized around the ideal sampling instant $\mathrm{t_0}$. This is a justifiable assumption, as long as the signal value does not vary significantly within $\Delta\mathrm{t}$:

$$\mathrm{v}(\mathrm{t_0} + \Delta t) = \mathrm{V_t}\Big|_{t=\mathrm{t_0}} + \left.\frac{\mathrm{dv}(t)}{\mathrm{d}t}\right|_{t=\mathrm{t_0}} \cdot \Delta t. \tag{2.23}$$

Fig. 2.7 visualizes the influence of the jitter on the sampling operation for such a linearized signal. The deviation of the ideal sampling instant results in a voltage error, which follows a normally distributed process

$$\mathrm{J_v} \sim \mathcal{N}\left(\mu_\mathrm{v}, \sigma_\mathrm{v}^2\right), \tag{2.24}$$

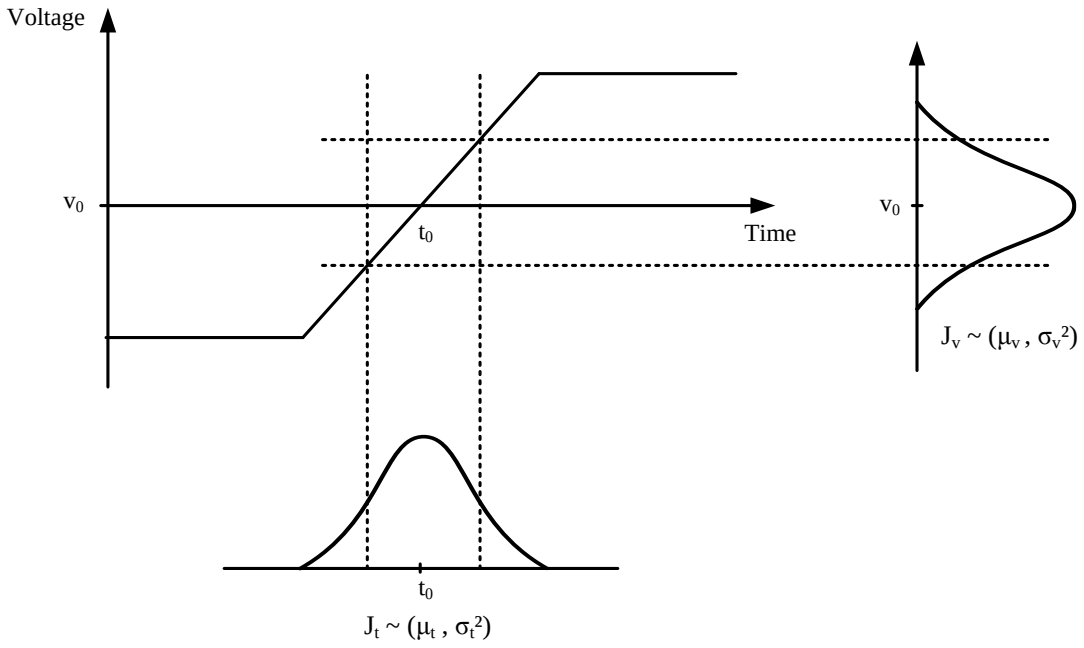


Figure 2.7: Transfer from timing jitter to voltage error.

where the mean μ_v is determined by the signal value at the sampling instant

$$\mu_\mathrm{v} = \mathrm{v}(t)\big|_{t=\mathrm{t}_0}, \tag{2.25}$$

and the variance σ_v^2:

$$\sigma_\mathrm{v}^2 = \sigma_\mathrm{t}^2 \cdot \left|\frac{\mathrm{dv}(t)}{\mathrm{d}t}\right|^2\Bigg|_{t=\mathrm{t}_0}. \tag{2.26}$$

According to Eq. 2.26, the variance of the jitter-induced noise depends on the jitter σ_t of the clock signal and the magnitude-squared slope of the sampled signal at the sampling time instant $t = \mathrm{t}_0$. Considering the practical implementation of the measurement, a sinusoidal signal with an amplitude $\hat{\mathrm{v}}$ and a frequency $\mathrm{f_{in}}$ is used as input signal:

$$\mathrm{v}(t) = \hat{\mathrm{v}} \cdot \cos\left(2 \cdot \pi \cdot \mathrm{f_{in}} \cdot t\right). \tag{2.27}$$

Dealing with a periodic signal, $\mathrm{J_v}$ turns into a cyclostationary random process. In the following, the variable t is substituted by the signal-related phase $\phi \in [0, 2 \cdot \pi]$:

$$\phi = 2 \cdot \pi \cdot \mathrm{f_{in}} \cdot t \mod (2 \cdot \pi). \tag{2.28}$$

Combining Eq. 2.26, Eq. 2.27, and using Eq. 2.28, the phase-dependent, cyclostationary variance $\sigma_\mathrm{v}^2(\phi)$ can be expressed as:

$$\begin{aligned}\sigma_\mathrm{v}^2(\phi) &= \sigma_\mathrm{Nj}^2 \cdot \sin^2(\phi) \\ &= \frac{\sigma_\mathrm{Nj}^2}{2} \cdot \left(1 - \cos\left(2 \cdot \phi\right)\right).\end{aligned} \tag{2.29}$$

Herein, the following substitution has been used:

$$\sigma_\mathrm{Nj} = 2 \cdot \pi \cdot \sigma_\mathrm{t} \cdot \hat{\mathrm{v}} \cdot \mathrm{f_{in}}. \tag{2.30}$$

According to Eq. 2.29, the variance $\sigma_\mathrm{v}^2(\phi)$ of the jitter-induced noise has a cosine shape. The two maximums correspond to the zero crossings of the signal with maximum slope, while the two minimums correspond to the turning points of the signal with zero slope. These basic relations are illustrated in Fig. 2.8, which shows one period of the sinusoidal signal (top), the normalized magnitude-squared of its derivative (middle), and the corresponding normalized jitter-induced noise as a function of the signal phase ϕ (bottom).

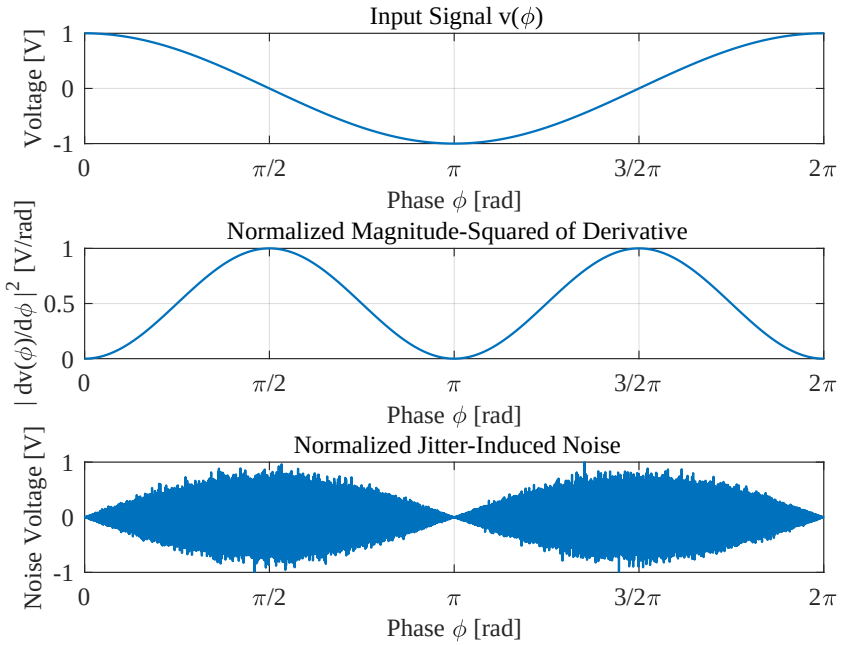


Figure 2.8: Relationship between the input signal (top), the normalized magnitude-squared of its derivative (middle), and the normalized jitter-induced noise (bottom).

The root-mean-square $\sigma^2_{\mathrm{v,rms}}$ of $\sigma^2_{\mathrm{v}}(\phi)$ is then given by:

$$\begin{aligned}\sigma^2_{\mathrm{v,rms}} &= \frac{1}{2\cdot\pi}\int_0^{2\cdot\pi}\sigma^2_{\mathrm{v}}(\phi)\mathrm{d}\phi \\ &= \left(\frac{2\cdot\pi\cdot\sigma_t\cdot\hat{\mathrm{v}}\cdot\mathrm{f_{in}}}{\sqrt{2}}\right)^2,\end{aligned} \tag{2.31}$$

which leads to the commonly known SNR [28], [29]:

$$\begin{aligned}\mathrm{SNR_{jitter}} &= 10\cdot\log_{10}\left(\frac{\left(\frac{\hat{\mathrm{v}}}{\sqrt{2}}\right)^2}{\sigma^2_{\mathrm{v,rms}}}\right) \\ &= 20\cdot\log_{10}\left(\frac{1}{2\cdot\pi\cdot\mathrm{f_{in}}\cdot\sigma_{\mathrm{t}}}\right).\end{aligned} \tag{2.32}$$

Unless otherwise stated, it is assumed that the input frequency used for the jitter calculation is equal to the Nyquist frequency $\frac{\mathrm{f_s}}{2}$.

2.3.6 Overall Dynamic Performance in Terms Of ENOB

The ENOB describes the overall dynamic performance of an ADC in terms of the effective number of bits of an ideal, quantization noise-limited ADC according to Eq. 2.12:

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02}. \tag{2.33}$$

Herein, the Signal-to-Noise and Distortion Ratio (SINAD) is defined as the ratio of the input signal power P_{sig} to the sum of the power of the noise P_n and all undesired spectral components P_{dist}:

$$\mathrm{SINAD} = 10 \cdot \log_{10}\left(\frac{P_{sig}}{P_n + P_{dist}}\right). \tag{2.34}$$

3 System Considerations for High-Speed and High-Resolution Sampling Performance

In this chapter, the specifications for the individual system components are derived from the requirements on the overall ADC performance. Recalling from the Chapter 1.1, the target goal of this work is the system design of an 80 GS/s TI ADC with an analog bandwidth $f_{3dB} > 30$ GHz, and providing an ENOB of 8 bits. Fig. 3.1 illustrates a block diagram of the proposed ADC architecture including the contributions of the corresponding project partners.

A MLL, which is developed by Advanced Laser Diode Systems A.L.S. GmbH, is used as high-performance optical clock source. It provides a clock train, consisting of ultra-short optical pulses, with a fixed pulse repetition rate of $f_{rep} = 10$ GHz.

The optical signal is coupled into the chip with a grating coupler and then distributed to the receiving circuits through a network of optical WGs and Multi-Mode Interference Coupler (MMI), which used as optical power splitters. The delays between the outputs of the CDN required in the TI architecture are implemented using WGs of different lengths. The design and analysis of the optical CDN was done at the Technical University of Berlin. A finite-element-based simulation tool, developed at JCMWave GmbH, is used for the layout optimization of the optical components.

At each output of the CDN, a high-speed Germanium (Ge) Photodiode (PD) convert the optical signal into an proportional current. As shown later, the overall sampler performance is mainly determined by the large-signal characteristic of the PD, so a lot effort was spend to improve the bandwidth and the quantum efficiency of the PD. This was done in a close collaboration between the Innovations for High Performance Microelectronics (IHP), which provides the used photonic SiGe BiCMOS technology, and the Institute for Semiconductor Engineering (IHT) of the University of Stuttgart with its expert knowledge of the design, processing and characterization of high-performance PDs.

The system design and the design of the actual sampler circuit, which is the focus of this work, was under the guidance of Rohde & Schwarz GmbH & Co. KG (R&S). In order to enable a deeper analysis of the ADC performance and to derive the specifications for the individual system components,

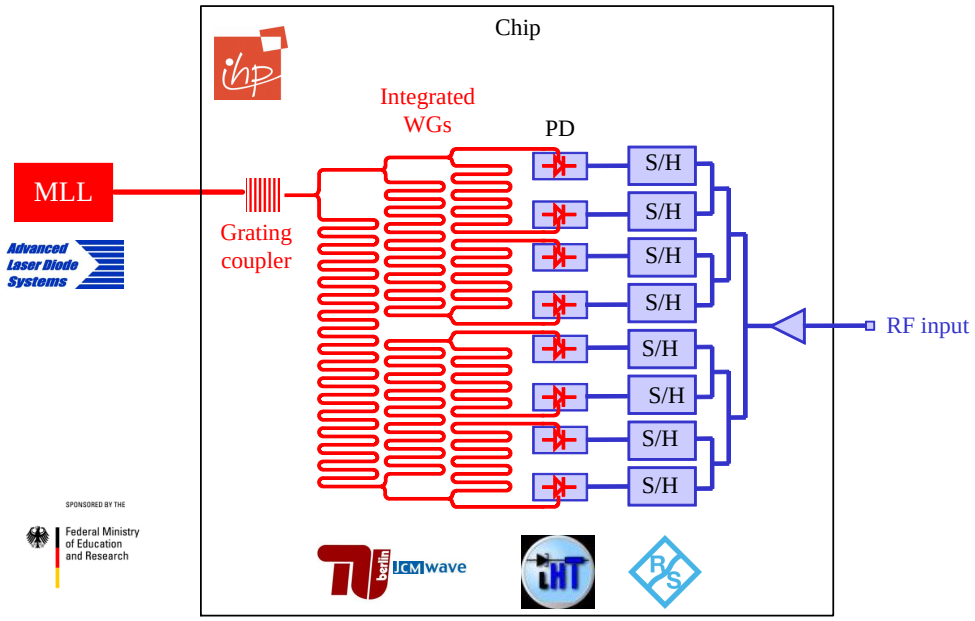


Figure 3.1: A block diagram of the proposed photonic-assisted TI sampler architecture, as well as the contributions of the individual project partners.

it is desirable to separate the different contributors from each other. Fig. 3.2 illustrates the most critical error sources contributing to the the overall SINAD, which were introduced in the last chapter. A target ENOB of 8 bits corresponds to a SINAD of 50 dB according to Eq. 2.34. It can be distinguished between errors originating from the signal path, which are represented by $\mathrm{SINAD}_{\mathrm{signal}}$, and those coming from the clock path of the sampler, which are considered by $\mathrm{SINAD}_{\mathrm{clk}}$. The overall SINAD is then given by:

$$\mathrm{SINAD} = 10 \cdot \log_{10}\left(\frac{1}{10^{\frac{\mathrm{SINAD}_{\mathrm{signal}}}{10}} + 10^{\frac{\mathrm{SINAD}_{\mathrm{clk}}}{10}}}\right). \tag{3.1}$$

As the system components were still under development during the project runtime, an equal error distribution was aimed in the system design phase. Therefore, a maximum tolerable $\mathrm{SINAD}_{\mathrm{signal}} = \mathrm{SINAD}_{\mathrm{clk}} = 53\,\mathrm{dB}$ is assigned to each contributor.

In the signal path, the noise arising from the analog signal path ($\mathrm{SNR}_{\mathrm{analog}}$) and the harmonic distortions (THD) are considered in the calculation of $\mathrm{SINAD}_{\mathrm{signal}}$. Offset and gain mismatches can be calibrated, either in hardware using trimming digital-to-analog converters or variable gain amplifiers, or with appropriate filters in the digital domain [26], [30], [31], [32], [33], [34], [35].

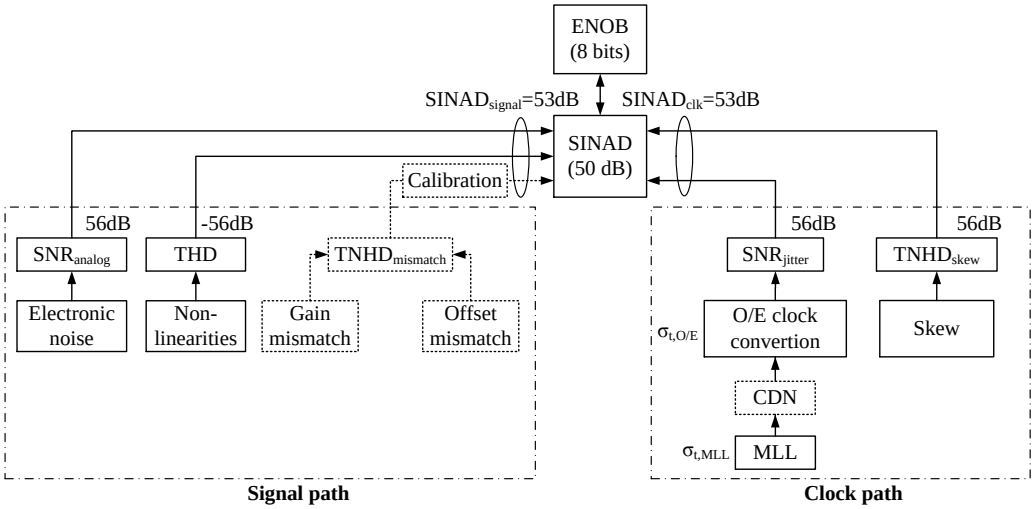


Figure 3.2: Composition of ENOB on block level.

Using the relationship

$$\mathrm{SINAD}_{\mathrm{signal}} = 10 \cdot \log_{10}\left(\frac{1}{10^{\frac{\mathrm{SNR}_{\mathrm{analog}}}{10}} + 10^{\frac{-\mathrm{THD}}{10}}}\right), \tag{3.2}$$

and targeting an equal error contribution $\mathrm{SNR}_{\mathrm{analog}} = -\mathrm{THD}$, this yields to a maximum allowed $\mathrm{SNR}_{\mathrm{analog}} = 56\,\mathrm{dB}$, respectively $\mathrm{THD} = -56\,\mathrm{dB}$, as shown in Fig. 3.2.
In the clock path, timing skew and and clock jitter are considered in the calculation:

$$\mathrm{SINAD}_{\mathrm{clk}} = 10 \cdot \log_{10}\left(\frac{1}{10^{\frac{\mathrm{SNR}_{\mathrm{jitter}}}{10}} + 10^{\frac{\mathrm{TNHD}_{\mathrm{skew}}}{10}}}\right). \tag{3.3}$$

Again, an equal error contribution yields to $\mathrm{SNR}_{\mathrm{jitter}} = \mathrm{TNHD}_{\mathrm{skew}} = 56\,\mathrm{dB}$, which corresponds to a total maximum tolerable jitter $\sigma_{\mathrm{t,tot}} = 7.8\,\mathrm{fs}$ according to Eq. 2.32, respectively a maximum tolerable skew of $\sigma_{\mathrm{skew}} = 7.8\,\mathrm{fs}$ for an 8x TI architecture according to Eq. 2.21.

Regarding the jitter, it compounds of $\sigma_{\mathrm{t,MLL}}$ originating from the MLL and jitter $\sigma_{\mathrm{t,O/E}}$ due to the O/E clock conversion. The optical CDN is considered to be noiseless and its influence on the overall jitter can be reduced to its losses [36]. Using the assumption that the noise contributors are independent, the total jitter is given by:

$$\sigma_{\mathrm{t,tot}} = \sqrt{\sigma_{\mathrm{t,MLL}}^2 + \sigma_{\mathrm{t,O/E}}^2}. \tag{3.4}$$

An equal jitter contribution yields to a maximum tolerable jitter of $\sigma_{t,MLL} = \sigma_{t,O/E} = \frac{\sigma_{t,tot}}{\sqrt{2}} = 5.5\,fs$.

The derived top-level specifications for the individual block components are summarized in Table 3.1.

Contributor	Parameter	Specification
Sampler	SINAD	**50 dB**
	f_{3dB}	**30 GHz**
	f_s	**80 GS/s**
Signal path	$SINAD_{signal}$	**53 dB**
	SNR_{analog}	56 dB
	THD	56 dB
Clock path	SNR_{clk}	**53 dB**
	$\sigma_{t,MLL}$	5.5 fs
	$\sigma_{t,O/E}$	5.5 fs
	σ_{skew}	7.8 fs

Table 3.1: Summary of the derived top-level specifications.

It is worth noting that the specifications are derived using a sinusoidal input signal. The requirements on jitter and timing skew are relaxed for wideband signals, i.e. by a factor of 3, respectively 4.7 dB, when considering a wide-sense stationary signal [26].

4 Architecture Considerations for the Implementation of the System Components

This chapter focuses on architecture considerations for the implementation of the system components, which are required for the proposed 80 GS/s TI ADC. At first, a review of the photonic SiGe BiCMOS technology platform and the challenges of the monolithic co-integration are presented. With regard to the system specifications derived in the last chapter, a review of the implementation of the components in the optical path is presented. The analysis of two architectures suitable for wideband and low-jitter sampling concludes this chapter.

4.1 Photonic SiGe-BiCMOS Technology Platform

A 0.25 μm SiGe BiCMOS process of the IHP product line - SG25H1 - forms the basis for the photonic co-integration [37]. The key component of this basic technology to enable the high-frequency performance is the high-speed Heterojunction Bipolar Transistor (HBT) with f_T = 180 GHz, respectively f_{max} = 200 GHz. The electrical module also features p-MOS and n-MOS devices, Metal-Insulator-Metal (MIM) capacitors, and polysilicon resistors, while the backend-of-line comprises 5 metal layers with different widths, respectively current density capacities.
The major goal was the integration of high-performance photonic components to the baseline technology without compromising the already demonstrated performance of the electrical devices, thereby maintaining a comparable high level of device yield with respect to the basic technology. The fulfillment of this requirement is bound to several technological problems. For example, high-performance BiCMOS is typically implemented on a bulk substrate, which enables the fabrication of low-impedance HBT collectors to ensure their high-speed potential and a proper heat dissipation. Silicon (Si)-based photonics requires a Silicon-On-Insulator (SOI) substrate for the fabrication of low-loss optical components. This incompatibility was solved using a local-SOI approach, which allows to fabricate SOI-based photonic structures in a bulk BiCMOS environment [38].
In Fig. 4.1, a Transmission Electron Microscopy (TEM) cross section of the photonic BiCMOS technology is shown to illustrate the Ge-PIN-PD integration with BiCMOS. The Ge-PIN-PD and the Si-WG below is located on the left-hand side, grown on a local SOI. The direction of the light propagation is perpendicular to the cross-section. On the right-hand side, a SiGe HBT fabricated in an adjacent bulk

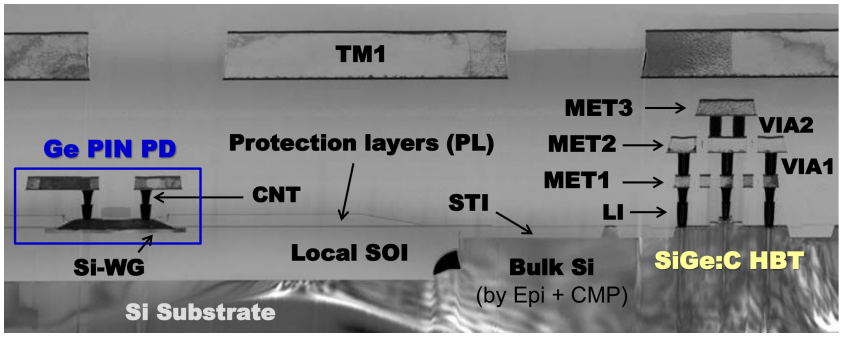


Figure 4.1: Photonic BiCMOS cross-section, perpendicular to the direction of light propagation, of the monolithically integrated receiver components: Ge-PIN-PD and Si-WG on a local SOI and a SiGe HBT fabricated in an adjacent bulk region (Source: [39]).

region and some of the metal layers (MET) are shown.
In addition, the integration of the high-performance Ge-PDs with bandwidths in the order of tens of GHz, a good responsivity, and a low dark current at the same time is another challenging task due to conflicting requirements of the thermal budget [40], [41]. A solution to this problem is presented in Chapter 4.4.

4.2 Fiber-to-Chip Interface

The light coming from the MLL is guided into a fiber with an effective mode area of $A_{\text{fiber}} = 80\,\mu\text{m}^2$, while the typical effective mode area of an integrated Si-WG is in the range of $A_{\text{WG}} = 0.1\,\mu\text{m}^2$. In order to achieve an efficient light coupling from the fiber into the chip, an interface is required, which focuses the light into the WG. For this purpose, a one-dimensional (1D) grating coupler, as shown in Fig. 4.2 a), is used. The area of grating is $A_{\text{fiber}} = 10\,\mu\text{m}$ x $10\,\mu\text{m}$, and a subsequent adiabatic taper of about $L_{\text{taper}} = 200\,\mu\text{m}$ length is required to narrow down to the WG width. Fig. 4.2 b) shows a photograph of a fiber placed above the grating coupler. Due to Bragg diffraction at the periodic structure, the diffracted light interferes constructively in the direction parallel to the chip surface, thus focusing the light directly into the WG. The efficiency of the coupling is given by the Bragg condition, which is a function of the optimum angle of incidence Θ, the wavelength, and the periodic refractive index variation due to the grating geometry.

The optimum layout was found by numerical simulations using the finite-element-based software JCMwave. The simulations are very time-consuming due to the large ratio of the simulated area and the wavelength, and a lot of effort was spent to improve the simulation time and accuracy [42], [43],[44],[45],[46]. As a result, the losses of the grating couplers were significantly reduced.

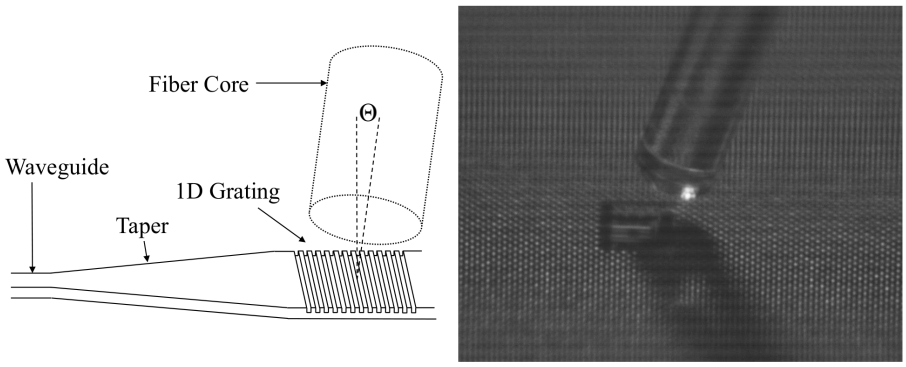


Figure 4.2: a) Basic configuration of fiber-to-chip coupling by a 1D grating. b) A photograph of a fiber placed above the grating coupler on the chip (Source: [47]).

In Fig. 4.3, the optical transmission spectra of two 1D grating couplers for different incidence angles are shown. The WG propagation loss of the WG and the optical input power have already been subtracted, therefore the illustrated attenuation corresponds to the losses of two gratings, each with a typical loss of $\alpha_{\mathrm{gr}} = 3\,\mathrm{dB}$, an optimum incidence angle of $\Theta \approx 12°$ for the used wavelength of $\lambda = 1550\,\mathrm{nm}$, and a 3 dB-bandwidth of $\lambda_{3\mathrm{dB}} = 40\,\mathrm{nm}$ - $60\,\mathrm{nm}$.

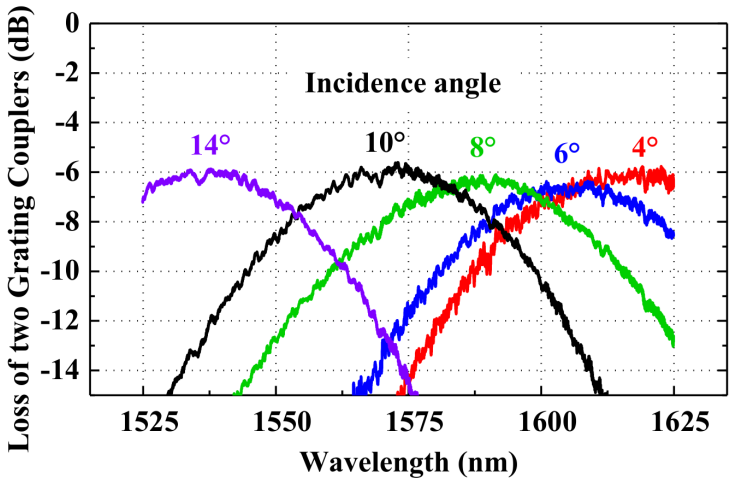


Figure 4.3: Measured losses of two 1D grating couplers (Source: [22]).

4.3 Optical Clock Distribution Network

4.3.1 Integrated Silicon Waveguides

Si is nearly transparent for λ = 1550 nm and therefore an ideal candidate for the integrated WGs. A high refractive index contrast towards the used cladding material Silicon Dioxide (SiO_2) results in a high confinement, thus enabling small bend radii and device miniaturization.
A major design goal was to minimize the linear losses of the WG, which benefits high pulse energy at the input of the PD for maximizing jitter performance of the sampler, as shown in Chapter 4.6. In addition, lower losses in the WG also reduce the power mismatch at the outputs of the CDN, which results from different WG lengths used to introduce the time delay required for the time-interleaving.

A cross section of a rib WG is shown in Fig. 4.4. This geometry shows much lower losses compared to that of a strip WG (h = H), since the electric field is mainly concentrated in the WG core. A lower limit for the linear losses is given by the effect of scattering on the non-ideal surface of the WG. The roughness of the WG surface depends on the manufacturing tolerances and limits the overall attenuation in the optical path.
Again, JCMwave was used to optimize the layout of WG structure for minimum losses. As a result, WG losses as low as α_{WG}/L =0.7 dB/cm for H = 220 nm, h = 70 nm, and W = 700 nm were reached [22].

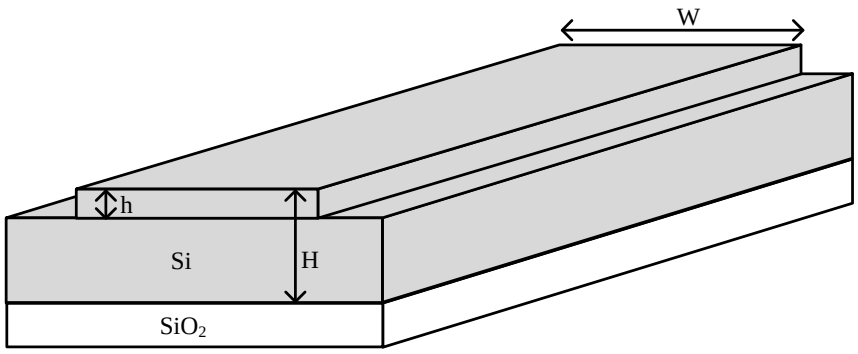


Figure 4.4: Cross section of rib WG.

In general, a CDN contains bends, and it should be considered that bend losses dramatically increase when the bend radius falls below a critical value. This value depends on the WG geometry and the guided mode and shrinks for smaller WGs [48]. For example, a bend radius r_{bend} as low as five microns for a strip WG with W = 400 nm and H = 200 nm does not involve any additional bend losses [49]. For the test chips developed in this work, a generous radius r_{bend} = 100 μm was used to ensure that no

additional bend losses are introduced.

In addition to the linear losses, non-linear effects become relevant when dealing with high optical peak energy values associated with the ultra-short pulses provided by the MLL. Usually the energy of a photon at a wavelength $\lambda = 1550\,\text{nm}$ is not sufficient to excite bound electrons from the valence band to the conduction band. But high optical intensity values increase the probability of the absorption of two photons simultaneously, whereby the sum of their energy values is sufficient to overcome the Si band gap of $E_{g,Si} = 1.12\,\text{eV}$. The induced free charge carriers assist the photon absorption process, resulting in an intensity-dependent loss [50], [51]. This effect is amplified when the pulse repetition rate of the optical pulse train is shorter than the effective carrier lifetime, since these free charge carriers accumulate over multiple pulses [52].

The non-linear losses were investigated on a simple test chip, consisting of an input and output grating couplers connected by a straight rib WG of $L = 2.1\,\text{mm}$ length [47]. As optical source, a MLL with a fundamental pulse repetition rate of $f_{rep} = 1.25\,\text{GHz}$ provides a train of ultra-short optical pulses of $\tau_{FWHM} = 200\,\text{fs}$ width, which can be broaden to $\tau_{FWHM} = 3.5\,\text{ps}$ by an optical bandpass filter. The pulse repetition rate can be optionally increased to $f_{rep} = 10\,\text{GHz}$ using an optical 1x8 interleaver, as described in Chapter 4.5. In addition, a MLL with $f_{rep} = 100\,\text{MHz}$ and a pulse width of $\tau_{FWHM} = 100\,\text{fs}$ was available.
Fig. 4.5 a) illustrates the measured average output power as a function of the average input power for the various configurations. Lower repetition rates are stronger attenuated for the same input power. This can be well explained by the two-photon absorption due to a higher pulse energy value compared to the pulse energy at higher repetition rate for the same input power. A surprising result was that the ultra-short pulses, which correspond to a higher peak intensity values, are attenuated less than broader pulses for the repetition rates of $f_{rep} = 1.25\,\text{GHz}$ and $f_{rep} = 10\,\text{GHz}$. This behavior can not be explained by the widely used model [53], a hint that it is not applicable to ultra-short pulses.
Fig. 4.5 b) shows the calculated pulse energy values for the plot in Fig. 4.5 a). It can be seen that the $f_{rep} = 10\,\text{GHz}$ pulse train is stronger attenuated than the $f_{rep} = 100\,\text{MHz}$ and the $f_{rep} = 1.25\,\text{GHz}$ pulse train. This can be well explained by the free-carrier absorption model, since the free carriers accumulate over multiple pulses to higher concentrations. When the effective carrier life time is relative short compared to the pulse repetition rate, this effect is negligible, which explains why the $f_{rep} = 100\,\text{MHz}$ and the $f_{rep} = 1.25\,\text{GHz}$ pulse train are attenuated in a similar way.

The design of an optical CDN for TI applications requires a specified delay between the outputs, which is implemented by WGs of different lengths. For this purpose, the group velocity must be known. It is determined by simulating the guided fundamental mode and its effective refractive index n_{eff}.

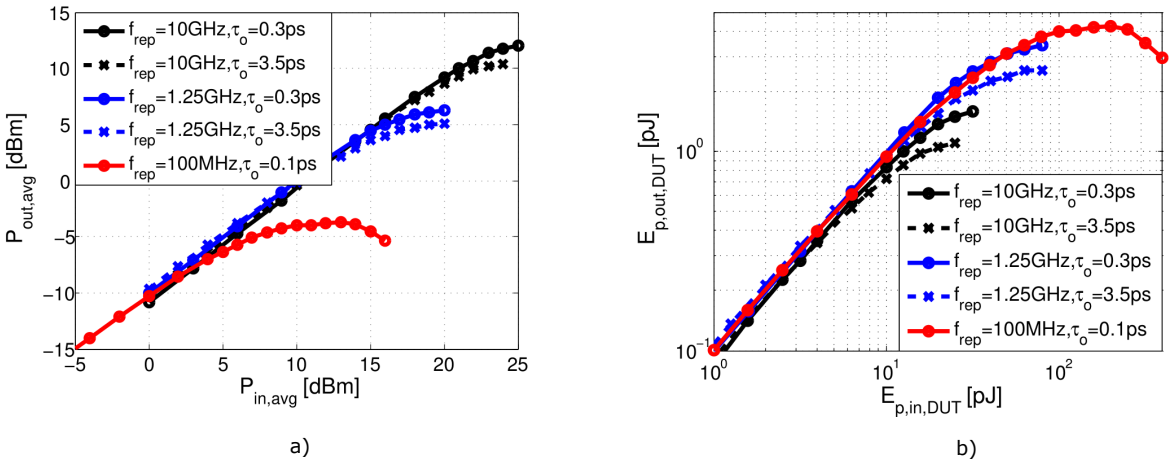


Figure 4.5: a) Measured output power of the Si-WG as a function of the input power for various pulse train characteristics. b) Calculated output pulse energy of the Si-WG as a function of the input pulse energy (Source: [47]).

This allows to calculate the group index

$$n_{grp} = n_{eff}(\lambda) - \lambda \cdot \frac{dn_{eff}(\lambda)}{d\lambda}. \tag{4.1}$$

Using the the commonly-known relationship

$$v_{grp} = \frac{c_0}{n_{grp}}, \tag{4.2}$$

the group velocity v_{grp} can be calculated. Herein, c_0 is the speed of light in vacuum. Once the group velocity is known, the length difference ΔL, which is required for a specified delay Δt, can be calculated:

$$\Delta L = v_{grp} \cdot \Delta t \tag{4.3}$$

The high thermo-optic coefficient of Si, which is more than one order of magnitude larger than that of SiO_2, causes a temperature dependency of the group index of the Si-WG [54],[55]. As a consequence, a deviation from the nominal design temperature leads to a temperatur-dependent skew.
From simulations, a group index of $n_{grp,291K} = 3.7743$ at room temperature and $n_{grp,352K} = 3.7879$ at the nominal chip temperature $T = 352\,K$ was determined [47]. Assuming a given delay $t_{d,nom}$ at the nominal temperature, the temperature-dependent skew can given by

$$\frac{t_{skew}}{dT} = \frac{t_{d,nom}}{\Delta T} \cdot \frac{n_{grp,opt}}{n_{grp,\delta T}}, \tag{4.4}$$

which results in $\frac{t_{skew}}{dT} = t_{d,nom} \cdot 6.1 \cdot 10^{-5}$ s/K with the simulated values given above. Regarding the 8x 10 GS/s TI architecture, the maximum nominal delay between the shortest and the longest path is $t_{d,nom} = 87.5$ ps, and a temperature-dependent skew of $\frac{t_{skew}}{dT} = 5.3$ fs/K is expected. Recalling to the skew requirements from Table 3.1, a maximum temperature difference of $\Delta T = 1.5$ K is tolerable to meet the specifications.
It is worth mentioning that one drawback of the passive clock distribution is its design for a fixed clock frequency. A change of that frequency requires additional measures to adjust the delays in the individual paths.

4.3.2 Multimode Interference Coupler as Optical Power Divider

Optical power dividers are necessary in a TI architecture to split the optical clock signal to the individual sampler units. For this purpose, MMI couplers are used, since they offer an excellence performance - compared to alternative implementations - with an excess loss $\alpha_e < 0.5$ dB, a crosstalk as low as $\alpha_{xtalk} < -30$ dB, and a power imbalance $\Delta p < 0.5$ dB [56], [57].
In general, N x M MMI couplers can be designed for a specified number of N input and M output ports. Due to a superior imbalance characteristic and the relaxed fabrication requirements [49], it will be focused on a 1x2 MMI configuration as shown in Fig. 4.6. It consists of a multimode center region, designed to support a large number (≥ 3) of modes, to which the input and output WGs are connected. Its operation is based on the self-imaging principle, which can be described as follows. When light is applied to the input WG, it excites multiple higher order modes in the center region. These higher order modes have different propagation constants, and they interfere when propagating along the multimode region. By properly placing the output WGs, an image of the input field profile is coupled into them.[57].

Figure 4.6: Layout of a 1x2 MMI coupler.

4.3.3 Clock Distribution Network for the Proposed 80 GS/s TI ADC

Fig. 4.7 illustrates the optical CDN proposed for the implementation in the 80 GS/s TI ADC [47]. A relative time delay between two CDN outputs of $d\tau_0 = 12.5\,\text{ps}$ is required, which results in a length difference of $\Delta L = 0.99\,\text{mm}$ between each path according to Eq. 4.3. Herein, a group index of $n_{grp,353K} = 3.7879$ at the expected chip temperature of $T = 353\,\text{K}$ was simulated.
Considering a WG loss of 0.7 dB/cm [22], a maximum length difference between the shortest and longest path of $\Delta L = 7\,\text{mm}$ corresponds to a power mismatch of $\Delta p = 0.5\,\text{dB}$, respectively
$\Delta p = \pm 0.25\,\text{dB}$ relative to the mean. The consequences of a power mismatch and its influence on the ADC performance depends on the sampler architecture and is investigated in Chapter 4.6.
The precision of the delay is limited by fabrication tolerances. Since the group index of the WG depends on the geometry, the influences of height, etch depth, and width variations on the delay were investigated by simulations [47]. Assuming given process-specific tolerances, a maximum skew of $t_{skew} = 700\,\text{fs}$ is expected between the shortest and the longest path due to simulations. Comparing this value with the system specifications from Table 3.1, it becomes obvious that the skew due to fabrication tolerances must be compensated.

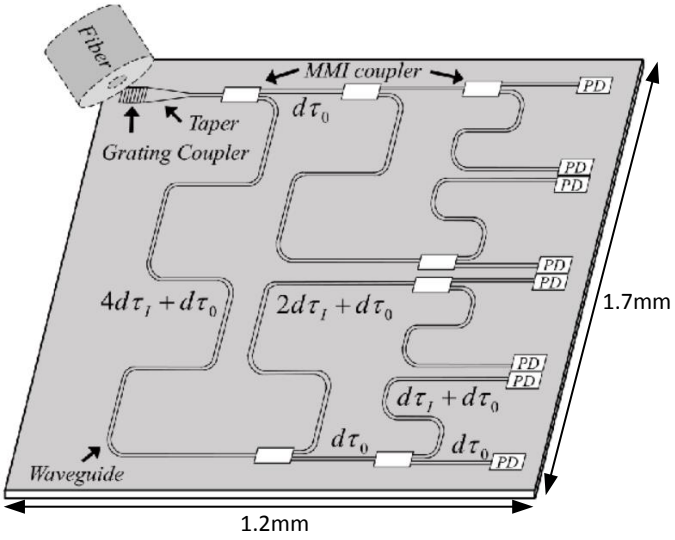


Figure 4.7: Optical CDN proposed for the implementation in the 80 GS/s TI ADC (Source: [47]).

Fig. 4.8 illustrates the schematic of the test structure, which is implemented for the characterization of the skew. It consists of an 1D input grating to couple the the optical pulse train into the chip. The CDN consists of one half of the proposed CDN from Fig. 4.7, which is connected to its mirrored copy. As a result, four TI pulses with a nominal delay of $t_d = k \cdot 25\,\text{ps}$ (k = 1,2,3) at a temperature $T = 353\,\text{K}$ are coupled out of the 1D output grating as a response to each input pulse. The output fiber is connected

to a high-speed PD, and a sampling oscilloscope acquires the received pulse train. The deviations from the nominal delays between four adjacent pulses are the determined by detecting and comparing the peak positions of the pulses. Since only one output grating is used to detect the multiplexed pulse train, the influence of the fiber position at the output grating is minimized. In addition, the measurement accuracy is significantly improved compared to the acquisition of the individual CDN outputs in Fig. 4.7.

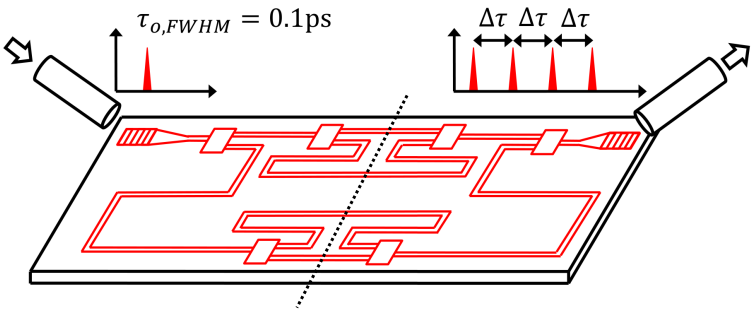


Figure 4.8: Schematic of the test structure, implemented for the characterization of the skew of the proposed CDN (Source: [47]).

Fig. 4.9 illustrates the measured skews relative to the first pulse as a function of temperature. For each temperature value, five measurements were performed to reduce the impact of noise. At the design temperature of T = 353 K, a timing skew $t_{skew} < 100$ fs was measured. A linear fit applied on the temperature drift leads to the following values:

t_d	25 ps	50 ps	75 ps
$\frac{dt_{skew}}{dT}$ (measured)	<1 fs/K	3 fs/K	6 fs/K
$\frac{dt_{skew}}{dT}$ (ideal)	1 fs/K	3 fs/K	4.6 fs/K

Comparing them with the expected values due to the thermo-optic coefficient of Si under ideal fabrication process conditions, it becomes obvious that there are other temperature-dependent effects, which affect the effective refractive index. A possible candidate might be strain between the WG and the cladding material SiO_2, which induces an effective refractive index change due to the stress-induced photo-elastic effect [58], [59].

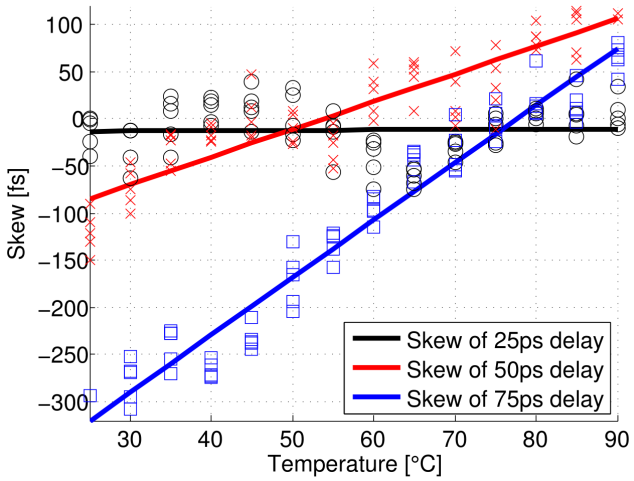


Figure 4.9: Measured skews relative to the first pulse position as a function of temperature (Source: [47]).

4.4 High-Performance Photodiode

The PD, as interface between the optical and electrical domain, is the key element of photonic-assisted low-jitter applications, since it has to transfer the superior jitter performance of the MLL into the electrical domain without adding a significant amount of noise. In Chapter 4.6.1 and Chapter 4.6.2, the influence of the PD bandwidth on the performance of the corresponding sampler architecture is presented, and it can already be said that a high PD bandwidth and a high quantum efficiency are essential to meet the target specifications.

Ge has become the material of choice for integrated high-speed PDs in the telecommunication wavelengths for several reasons. A high electron mobility enables the implementation of high-speed devices, and bandwidths exceeding 100 GHz have been demonstrated [60]. A direct bandgap of $E_{g,Ge} = 0.8\,eV$ results in a strong absorption coefficient and therefore a large responsivity at the telecommunication wavelengths [49]. The responsivity at the used wavelength $\lambda = 1550\,nm$ is $R_{PD} = 1.25\,A/W$ [49]. In addition, the intrinsic Ge layer of the PD can be directly grown on the Si-WG. Due to the high refractive index of Ge compared to Si, the light in the WG is refracted towards the intrinsic region, and subsequently absorbed. As a consequence, a lateral pin PD structure can be integrated, which does not suffer from the trade-off between the bandwidth and the quantum efficiency, which is typically known for vertical PDs [61].

At the beginning of this thesis, PDs with a quantum efficiency of $\eta_{PD} = 40\,\%$ and a zero-bias bandwidth in the range of $f_{3dB,0V} \approx 10\,GHz$ were available in the used technology, and several innovative approaches have been implemented to improve their performance. For example, the Ge epitaxy is carried

out before baseline BiCMOS Cobalt Silicide (CoSi) formation, which is required to get low-ohmic $CoSi_2$ layers. This process step includes a final anneal with a temperature of 700 °C or higher [62], which leads to a smearing of the implanted Phosphor (P) profiles of the PD by diffusion [63]. A significant bandwidth degradation of the PD results from minority-carrier diffusion in non-depleted, weakly doped regions. Reducing the temperature of the CoSi anneal is limited due to the increase of the external base resistance, and therefore the decrease of f_{max} of the HBT [22]. This influence was significantly reduced by the additional implantation of non-doping elements to reduce the minority-carrier lifetime, and therefore the bandwidth-limiting diffusion component in the PD [41].

Fig. 4.10 a) illustrates the normalized small-signal frequency responses of the first generation PD for different biasing voltages. It has a zero-bias bandwidth of $f_{3dB,0V} = 12\,GHz$, which increases to $f_{3dB,-2V} = 30\,GHz$ when a bias voltage $V_{bias,PD} = -2\,V$ is applied.
In Fig. 4.10 b) illustrates the normalized small-signal frequency responses of the second generation PD for the same bias voltages. The zero-bias bandwidth could be increased by ≈ 66 % to $f_{3dB,0V} = 30\,GHz$, while an outstanding bandwidth of $f_{3dB,-2V} > 70\,GHz$ is achieved for a bias voltage $V_{bias,PD} = -2\,V$.

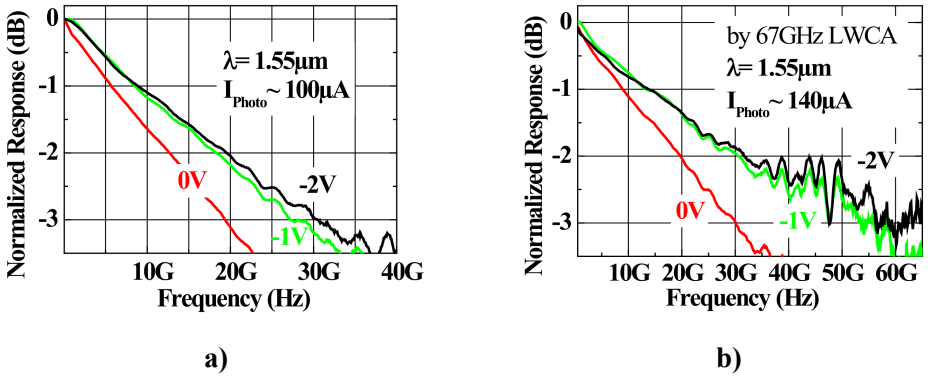
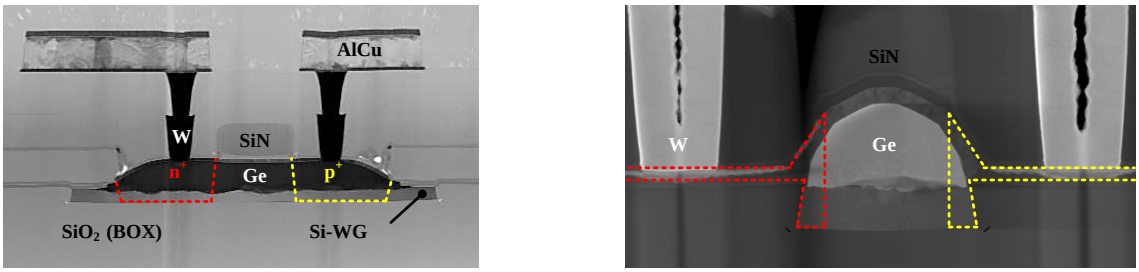


Figure 4.10: a) Frequency response of first generation PD for different reverse bias voltage values, measured at a wavelength of $\lambda = 1550\,nm$ and and average photocurrent of $I_{photo} = 100\,\mu A$. b) Frequency response of second generation PD for different reverse bias voltage values, measured at a wavelength of $\lambda = 1550\,nm$ and and average photocurrent of $I_{photo} = 140\,\mu A$ (Source: [41]).

In addition, the quantum efficiency was significantly improved by an optimization of the PD layout. Fig. 4.11 a) illustrates a TEM cross section of the first generation PD with a bias-independent quantum efficiency of $\eta_{PD} = 50\,\%$ [41]. The optimized layout of the second generation PD with an improved quantum efficiency of $\eta_{PD} = 65\,\%$ for zero-bias, respectively $\eta_{PD} = 84\,\%$ for a bias voltage $V_{bias,PD} = -2\,V$ is shown in Fig. 4.11 b). The improvement of the quantum efficiency results from a reduced metal absorption due to the separation of the absorption layer (Ge) from the contact regions (Si) [39]. While the window for Ge epitaxy is inside the Si-WG contour for the old PD, it overlaps the underlying WG in the new layout. It should be noted that the given values for the bandwidth and



a) b)

Figure 4.11: TEM cross sections of the Ge lateral pin PD, perpendicular to the direction of light propagation: a) Layout of the first generation PD with a bandwidth $f_{3dB} = 30\,\text{GHz}$ and a quantum efficiency of $\eta_{PD} = 52\,\%$. b) Layout of the second generation PD with a bandwidth $f_{3dB} > 50\,\text{GHz}$ and a quantum efficiency of $\eta_{PD} = 84\,\%$.

the quantum efficiency are measured under small-signal conditions. Applying an optical pulse with a short pulse duration and high peak intensity power values, such as provided by the MLL, does not fulfill these conditions, so the further analysis of the actual large-signal behavior was also part of this work.

4.5 Mode-Locked Laser as High-Performance Clocking Source

A MLL emits a periodic train of ultra-short and ultra-stable pulses with a technique called mode-locking. The term mode locking originates from the description in the frequency domain, where the formation of the short pulses corresponds to a fixed phase relationship between the longitudinal modes in the laser resonator. The more of the longitudinal modes fulfill the phase condition, the shorter pulses can be generated. A mathematical description of the mode-locking mechanism is given by the Haus-master equation [64].

Basically, the laser resonator consists of a gain medium and a non-linear element, which causes the formation of an ultra-short pulse circulating in the resonator. Active MLLs perform the mode-locking with an active element, for example an optical modulator, which modulates the phase or losses. But since the timing jitter of active MLLs is determined by the aperture uncertainty of the RF signal reference, the following analysis will focus on passive MLLs with their outstanding jitter performance.

A simple block diagram of a passive MLL is illustrated in Fig. 4.12. The light from the pump diode passes a dichroic mirror and enters the actual cavity, consisting of the gain medium (Erbium-Ytterbium (Er:Yb) glass), and a Semiconductor Saturable Absorber Mirror (SESAM). Due to the intensity-dependent transfer characteristic of the SESAM, high intensities are less attenuated than low intensities, resulting in a pulse formation inside the cavity. The output coupler mirror directs a small amount of power to

the output each time the pulse arrive, thus providing an optical pulse train with a pulse repetition rate proportional to the round-trip time.

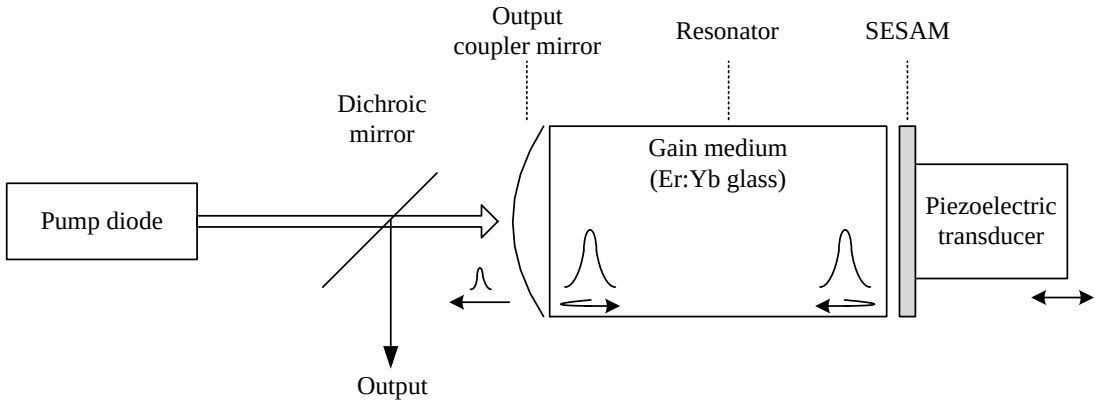


Figure 4.12: A block diagram of passive MLL.

Concentrating on the photonic ADC application, the most relevant characteristics of the pulse train are the pulse-to-pulse-energy fluctuations, which are usually described by the Relative Intensity Noise (RIN), and the timing jitter. The noise properties of a MLL were successfully described the first time by means of the soliton perturbation theory [65], and the results were more generalized to non-soliton-effects in [66], [67]. Basically, the noise of a MLL can be classified into quantum noise and technical noise.

Quantum noise is associated with spontaneous emissions, and its strength is influenced by the pulse parameters such as pulse energy, pulse duration and repetition rate [8]. It defines the fundamental noise limit for high offset frequency fluctuations and can only be reduced by a higher optical power, a longer cavity length, or a shorter pulse width.

Technical noise results from other noise sources in the laser setup, such as resonator vibrations, pump excess noise, temperature fluctuations or drift due to the lack of a reference [68], [69], [66], [67]. Although the technical noise is mainly concentrated in a small bandwidth - typically a few tens of kilohertz - around the fundamental frequency, it usually determines the overall timing jitter. It can be significantly reduced by using a piezoelectric transducer, as shown in Fig. 4.12, to control the cavity length and integrating the MLL in a Phase-Locked Loop (PLL) feedback control [70].

MLLs providing optically pulse trains with repetition rates of tens of gigahertz, respectively extreme short cavity lengths, usually show insufficient timing stability regarding the photonic ADC

application. In addition, high power at high repetition rates at the same time can lead to thermal destruction of the saturable absorber. Such problems can be overcome by using a pulse repetition rate multiplication to increase the repetition rate of a slower MLL with an excellent jitter performance [71]. Doubling the repetition rate is achieved by splitting the pulse train, and combining again with a delay corresponding half the pulse period. Higher multiplication factors can be realized by cascading multiple stages.

In the framework of this project, a MLL with a repetition rate of $f_{rep} = 1.25\,\text{GHz}$ was developed, and a cascaded Mach-Zehnder interferometer scheme by fibers and couplers is used to achieve the target repetition rate of $f_{rep} = 10\,\text{GHz}$, as shown in Fig. 4.13. The characterization of its jitter performance was part of the measurement campaign of the first developed demonstrator chip, and the results are presented in Chapter 5.2.

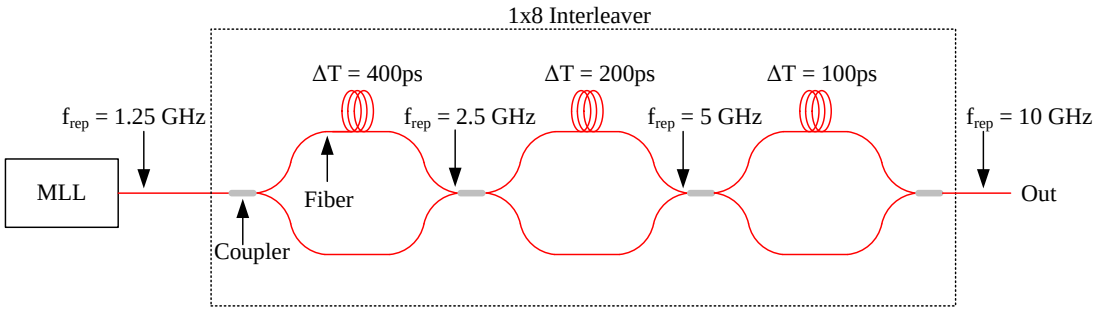


Figure 4.13: A block diagram of the optical 1x8 interleaver used for the pulse repetition rate multiplication.

4.6 High-Speed Sampler Architectures

4.6.1 Track-And-Hold Architecture

Functional Description

A differential open-loop track-and-hold architecture is chosen as a starting point for the design of the high-speed sampling circuit because of its well-known benefits. The structure consists of an input buffer, a THA, and an output buffer. It is fast and provides an analog bandwidth exceeding the multi-ten-GHz range with a high linearity [72], [73], [74], [75], [76], [77], [78], [79], [80], [81]. In addition, it has a low sensitivity to common-mode errors, and is unconditionally stable, if the input and output buffers are stable. Fig. 4.14 illustrates a block diagram of a photonic-assisted 10 GS/s track-and-hold architecture, which basically consists of two TI 5 GS/s-THA. The basic operation of one

THA core can be divided into two phases. In the track mode, the corresponding switch of a sampler is closed and the output of the samplers is tracking the input signal. In the hold mode, the signal value at the instant of the track-to-hold transition is held for the transmission through the MUX to provide a stable output to the digitizing ADC.

Aiming at highly-stable time-aligned clocking of THAs and MUX, the optical pulse train provided by the MLL is converted into a low-jitter square-wave clock signal by the O/E clock converter. The converter circuit basically consists of a toggle-flipflop, which is triggered by an optical pulse to switch its state. As a result, the circuit delivers an electrical square-wave signal with a frequency equal to half of the pulse repetition rate as response to the optical pulse train. A MUX at the output, selects the corresponding signal in the hold phase, and provides the desired full-rate sample stream to the subsequent ADC.

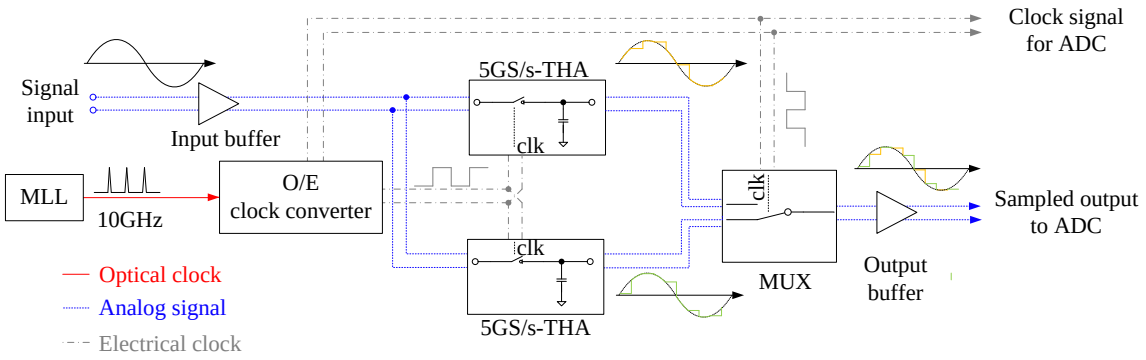


Figure 4.14: Block diagram of a photonic-assisted 10 GS/s THA architecture.

The analog performance in the signal path of the sampler is mainly determined by that of the input buffer and the THA.
The jitter performance of the sampler is determined by the jitter at the output of the PD, and the additional jitter contributed by the O/E clock converter.

Jitter

A fundamental jitter performance limitation of such a sampling architecture was derived in [52]. Herein, it is assumed that the sampling operation is directly triggered by the rising edge of the photocurrent exceeding a given threshold value I_{thres}. In this case, the jitter $\sigma_{t,PD}$ can be approximated by

$$\sigma_{t,PD}^2 = \frac{\sigma_{i,noise}^2}{\left(\frac{di_{PD}(t)}{dt}\Big|_{t=t_{thres}} \right)^2}, \tag{4.5}$$

where the deterministic photocurrent $i_{PD}(t)$ is superposed by a current noise with a variance $\sigma^2_{i,noise}$. Applying an optical Gaussian-shaped pulse with an energy E_{PD} to the input of the PD with a Gaussian-shaped impulse response, the jitter $\sigma_{t,PD}$ is given by [52]:

$$\sigma^2_{t,PD} = \frac{h \cdot \nu}{16 \cdot \ln(2) \cdot \eta_{PD} \cdot E_P} \left[1 + \eta_{eff} \cdot (G_{EDFA} \cdot NF_{EDFA} - 1)\right] \cdot \frac{(\tau_e^2 + \tau_o^2)^3}{\tau_e^3 \cdot \sqrt{\tau_e^2 + 2 \cdot \tau_o^2}} \cdot e^{\left(\frac{2 \cdot \ln(2) \cdot \tau_e^2}{\tau_e^2 + \tau_o^2} - \frac{2 \cdot \ln(2) \cdot \tau_e^2}{\tau_e^2 + 2 \cdot \tau_o^2}\right)}, \tag{4.6}$$

where h is the Planck constant, $\nu = \frac{c_0}{\lambda}$ the light frequency, c_0 the speed of light in vacuum, λ the wavelength, τ_o the optical Full-Width-at-Half-Maximum (FWHM) pulse width, and τ_e the electrical FWHM pulse width. In Eq. 4.6, an Erbium-Doped Fiber Amplifier (EDFA) with a gain G_{EDFA} and a noise factor NF_{EDFA} is considered, and the losses η_{eff} in the optical path are given by:

$$\eta_{eff} = \alpha_{gr} \cdot \alpha_{mmi} \cdot \alpha_{WG} \cdot \eta_{PD}. \tag{4.7}$$

Herein, α_{gr} represents the losses of the grating coupler, α_{MMI} the "losses" of the MMIs due to the power splitting, α_{WG} the attenuation in the WG coupler, and η_{PD} the quantum efficiency of the PD.

From Eq. 4.6, it becomes obvious that a high pulse energy, a short optical pulse width, and a short PD impulse response are required to reduce the jitter. Increasing the optical pulse energy is limited since it corresponds to higher peak intensity values and therefore higher non-linear losses in the CDN. Usually the optical pulse width is in the range of a few hundred femtoseconds and therefore much smaller compared to the electrical one. Thus, the most efficient way to improve the jitter is to reduce the PD impulse response by increasing its bandwidth.

In addition, stochastic pulse-to-pulse energy fluctuations will affect the instant of the threshold crossing and result in an additive jitter component. These fluctuations are described by the RIN power spectral density S_{RIN}, which is given for a shot-noise-limited MLL by [82]:

$$S_{RIN} = \frac{2 \cdot h \cdot \nu}{P_{avg}}. \tag{4.8}$$

Herein $P_{avg} = E_p \cdot f_{rep}$ represents the average power for the given pulse repetition rate f_{rep}.
Considering the EDFA mentioned above, the variance of the pulse-to-pulse energy fluctuations is calculated to

$$\sigma_{p2p} = 1 + \sqrt{\int_0^{\frac{f_{rep}}{2}} S_{RIN} \cdot NF_{tot} \, df}, \tag{4.9}$$

where the total noise factor F_{tot} is given by [83]:

$$NF_{tot} = NF_{EDFA} + \frac{1 - \eta_{eff}}{\eta_{eff} \cdot G_{EDFA}}. \tag{4.10}$$

As shown in Appendix B, the jitter $\sigma_{t,p2p}$, induced by pulse-to-pulse energy fluctuations for a Gaussian-shaped impulse response of the PD, is given by Eq. B.8:

$$\sigma_{t,p2p} = \frac{\delta_E}{2 \cdot \sqrt{2} \cdot \pi \cdot f_{3dB}}, \tag{4.11}$$

where the 3 dB-bandwidth f_{3dB} of the PD is related to the electrical pulse width τ_e by:

$$f_{3dB} = \frac{\sqrt{2} \cdot \ln(2)}{\pi \cdot \tau_e}. \tag{4.12}$$

Since the two jitter sources are uncorrelated, the total jitter $\sigma_{t,edge}$ is given by

$$\sigma_{t,edge}^2 = \sigma_{t,opt}^2 + \sigma_{t,p2p}^2. \tag{4.13}$$

Fig. 4.15 illustrates the jitter induced by quantum fluctuations and pulse-to-pulse energy fluctuations as a function of the PD bandwidth for an optical pulse width of $\tau_o = 300\,fs$, and the nominal optical pulse energy $E_P = 200\,fJ$ at the input of the PD. It can be seen that a bandwidth $f_{3dB} > 60\,GHz$ is required to meet the target jitter specification of $\sigma_t = 5.5\,fs$ for the practical case where an EDFA required. It should be noted, that the PD bandwidth must still exceed 50 GHz when an MLL with sufficient power is available and no EDFA is required ($G_{edfa} = 1$ and $NF_{edfa} = 1$).

Influence of Mismatch

A power mismatch at the outputs of the CDN affects the crossing instant of the photocurrent and results in a constant timing error. A detailed analysis is given in Appendix B, and a skew resulting from power mismatch for a PD with a Gaussian-shaped impulse response is given by:

$$t_{skew,\delta_E} = \frac{\sqrt{\ln(2)}}{2 \cdot \pi \cdot f_{3dB}} \cdot \left[\sqrt{2 \cdot \ln(2)} - \sqrt{2 \cdot \ln\left(2 \cdot (1 + \delta_E)\right)}\right]. \tag{4.14}$$

Herein, the power mismatch δ_E is defined by

$$\delta_E = \frac{\Delta E_p}{E_{p,nom}}, \tag{4.15}$$

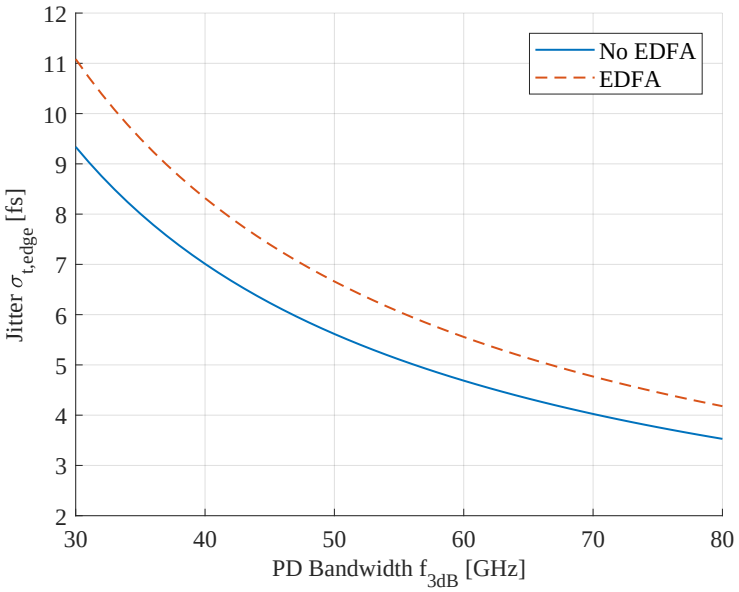


Figure 4.15: Jitter $\sigma_{t,edge}$ as a function of the PD bandwidth for an optical pulse width of $\tau_o = 300\,fs$ and a optical pulse energy of $E_P = 200\,fJ$ at the input of the PD with an efficiency of $\eta_{PD} = 40\,\%$. The influence when using an EDFA with a gain of $G_{EDFA} = 100$ and noise figure of $10 \cdot \log_{10}(NF_{EDFA}) = 6\,dB$ to compensate the losses $\eta_{eff} = 0.01$ in the CDN is also shown.

where ΔE_p is the deviation from the nominal pulse energy $E_{p,nom}$.

In a similar way, the influence of a mismatch of the PD bandwidth also affects the crossing instant of the photocurrent. From the analysis given in Appendix B and the resulting skew is given by

$$t_{skew,\delta_f} = \frac{\sqrt{\ln(2)}}{2 \cdot \pi \cdot f_{3dB}} \cdot \left[\sqrt{2 \cdot \ln(2)} - \frac{\sqrt{2 \cdot \ln(2 \cdot \delta_f)}}{\delta_f} \right], \tag{4.16}$$

where the bandwidth mismatch is defined as

$$\delta_f = \frac{f_{3dB,\delta}}{f_{3dB,nom}}. \tag{4.17}$$

Fig. 4.16 a) illustrates the skew induced by a mismatch of the pulse energy, while Fig. 4.16 b) shows the skew induced by a PD bandwidth mismatch for different center bandwidth values. It becomes obvious that a pulse energy mismatch is more critical than a bandwidth mismatch, with a skew almost four times larger for the same relative deviation.
Recalling from Chapter 4.3.3, a relative power mismatch of $10 \cdot \log_{10}(\delta_E) = \pm 0.25\,dB$ is expected due to the WGs of different lengths. This results in a skew $t_{skew} > 75\,fs$ for the investigated PD bandwidths, which corresponds to $TNHD_{skew} < 37.6\,dB$.

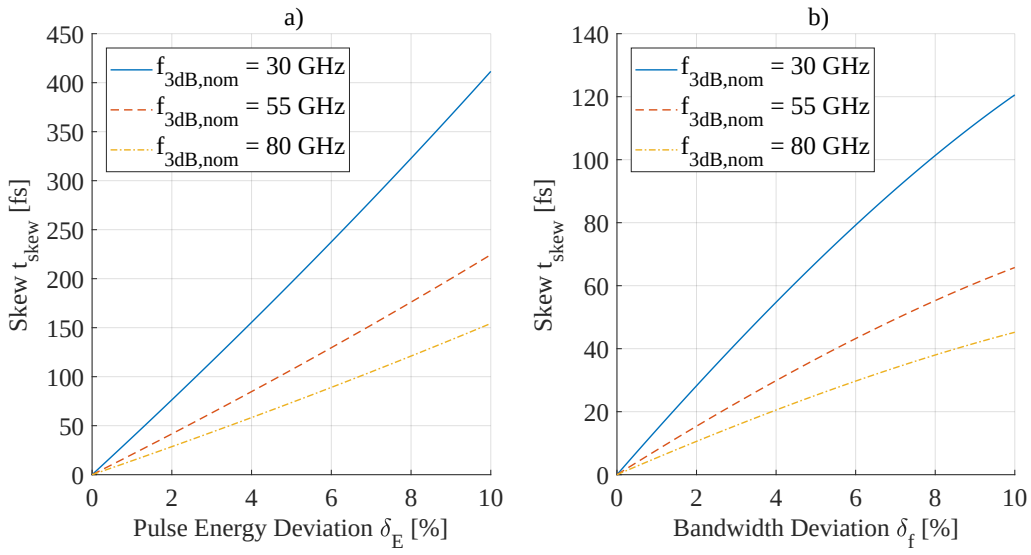


Figure 4.16: a) Skew induced by a mismatch of the pulse energy for different center bandwidth values. b) Skew induced by a mismatch of the PD bandwidth.

Although a significant statistical analysis of the process variations is not yet available, some first measurements of the bandwidth mismatch of the processed PDs were performed [39]. A relative bandwidth mismatch of $\delta_f = 5\,\%$, measured at a mean bandwidth of $f_{3dB,nom} = 46.5\,GHz$, results in a skew of $t_{skew} > 25\,fs$, respectively $TNHD_{skew} < 47.1\,dB$. Comparing these results with the specifications according to Table 3.1, it becomes obvious that additional measures must be taken to meet the overall system specifications. Various skew calibration techniques have been proposed by the circuits community and the signal processing community, an excellent overview is given in [84].

4.6.2 Pulse-Sampling Architecture

Functional Description

A sampling architecture, which uses an electrical train of short pulses as clock signal to perform the sampling operation, was proposed in [85]. The capability of achieving analog bandwidths in the millimeter wave range was successfully demonstrated recently [86]. Such an architecture becomes interesting for the photonic-assisted approach for two reasons.

On the one hand, the circuit to convert the optical pulses into an electrical pulse train is much less complex, compared to the pulse-to-square-wave conversion used in the track-and-hold architecture. Since less complexity usually involves less noise-contributing components, a lower jitter is expected. On the other hand, it was recently shown that the accuracy of the pulse center position of a photocurrent pulse train, in terms of jitter, can be orders of magnitude lower compared to that of the

traditional edge-triggered architecture [36]. Since the sampling instant in the proposed pulse-sampling architecture is directly coupled to the pulse center position, this advantage can be directly exploited.

Fig. 4.17 illustrates a block diagram of the architecture. The basic sampling operation is performed by multiplying an electronic clock pulse train with the input signal, and subsequently integrating the weighted pulses. Intersymbol interference is avoided by resetting the integrators before the next pulse arrives. In the clock path, a PD followed by a Transimpedance Amplifier (TIA) suffices to convert the current pulses of the PD into a proportional voltage to drive the multiplier.
Since a sinusoidal or square-wave signal is usually required to drive the subsequent ADC, the O/E clock converter circuit already mentioned in Chapter 4.6.1 can be used. As the jitter of the synchronization signal is much less critical, an asymmetric MMI [87] can be used as coupler to apply the major amount of the optical power to the jitter-critical PD, while a minimum optical power is applied to the O/E clock converter.

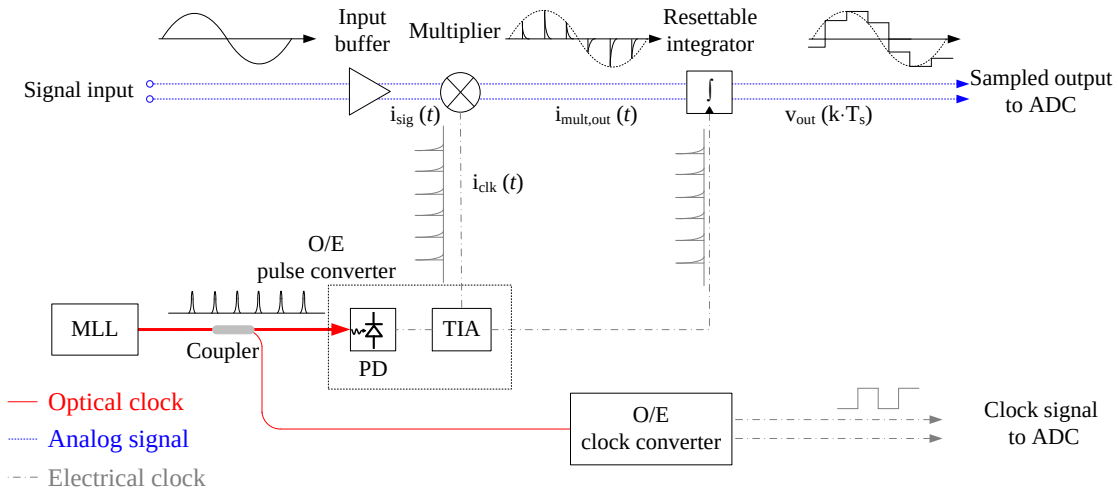


Figure 4.17: A block diagram of the photonic-assisted pulse-sampling architecture.

Assuming an input signal current $i_{sig}(t)$ and a clock signal $i_{clk}(t)$, the output current of the multiplier is given by

$$\begin{aligned} i_{mult,out}(t) &= i_{sig}(t) \cdot i_{clk}(t) \\ &= i_{sig}(t) \cdot \sum_{k=-\infty}^{\infty} g_{clk}(t - k \cdot T_s), \end{aligned} \tag{4.18}$$

where $g_{clk}(t)$ is the waveform of a single clock pulse. At next, the weighted current pulses are integrated over one clock period T_s. Regarding the practical implementation of using a capacitor as integrator,

the voltage at its output is given by

$$v_{out}(k \cdot T_s) = \frac{1}{C_H} \cdot \int_{t=k\cdot T_s-\frac{T_s}{2}}^{k\cdot T_s+\frac{T_s}{2}} i_{sig}(t) \cdot \sum_{k=-\infty}^{\infty} g_{clk}(t - k \cdot T_s)dt, \tag{4.19}$$

As the integrator is reset to a specific initial voltage before the next pulse arrives, the effect of intersymbol interference can be neglected, and Eq. 4.19 simplifies to:

$$v_{out}(k \cdot T_s) = \frac{1}{C_H} \cdot \int_{t=k\cdot T_s-\frac{T_s}{2}}^{k\cdot T_s+\frac{T_s}{2}} i_{sig}(t) \cdot g_{clk}(t - k \cdot T_s)dt. \tag{4.20}$$

For the calculation of the low-frequency gain, the frequency of the input signal is assumed to be much slower compared to the bandwidth of the pulse. Therefore, the integral in Eq. 4.20 can be approximated by

$$\begin{aligned} v_{out}(k \cdot T_s) &= \frac{i_{sig}(k \cdot T_s)}{C_H} \cdot \int_{t=-\frac{T_s}{2}}^{t=\frac{T_s}{2}} g_{clk}(t)dt \\ &= \frac{E_{clk}}{C_H} \cdot i_{sig}(k \cdot T_s). \end{aligned} \tag{4.21}$$

According to Eq. 4.21, the output voltage v_{kT_s} and therefore the sampler gain is proportional to the ratio of the pulse energy E_{clk} and the capacitance C_H.

Taking a closer look at Eq. 4.20, the integral almost looks like a convolution of the input signal $i_{sig}(t)$ and the clock pulse $g_{clk}(t)$. The integration limits can be expended to the range from $-\infty$ to $+\infty$, as long as the amplitude of the clock pulse is negligibly small enough outside the old integration limits. Assuming a symmetrical pulse $g_{clk}(t) = g_{clk}(-t)$, Eq. 4.20 can be rewritten to:

$$v_{out}(\tilde{t}) = \frac{1}{C_H} \cdot \int_{\tau=-\infty}^{\infty} i_{sig}(\tau) \cdot g_{clk}(\tilde{t} - \tau)d\tau, \tag{4.22}$$

where $\tilde{t} = k \cdot T_s$.
Eq. 4.22 can be interpreted as the convolution of the input signal with the clock pulse, evaluated at the sampling instants $k \cdot T_s$ and scaled by $1/C_H$. As a result, the frequency response of the pulse-sampling

architecture is equal to the Fourier transform of the clock pulse:

$$\mathrm{H_{sampler}}(\mathrm{j}\cdot\omega) = \mathcal{F}\{\mathrm{g_{clk}}(t)\}\,(j\cdot\omega) \tag{4.23}$$

Therefore, the large-signal impulse response of the PD directly affects the frequency response of the sampler. Or vice versa, the sampler can be used to measure the large-signal behavior of the PD indirectly by observing the frequency response of the sampler.

Jitter

A recent study on the shot noise in the detection of ultra-short optical pulse trains has demonstrated, that the amplitude and phase noise of a photocurrent pulse train are not equally distributed for ultra-short optical pulse widths [88]. Assuming a MLL provides an optical pulse train with a repetition frequency $\mathrm{f_{rep}}$ and a pulse energy $\mathrm{E_P}$ at the input of the PD with a quantum efficiency η_{PD}. It has been shown that the Single Sideband (SSB) amplitude noise $\mathrm{L_{AM}}$ of the photocurrent pulse train relative to the signal power of the n-th harmonic is then given by

$$\mathrm{L_{AM}} = \frac{\mathrm{h}\cdot\nu}{2\cdot\eta_{PD}\cdot\mathrm{E_P}\cdot\mathrm{f_{rep}}}\left[1+\mathrm{e}^{-(2\cdot\pi\cdot\mathrm{n}\cdot\mathrm{f_{rep}}\cdot\tau_\mathrm{o})^2}\right], \tag{4.24}$$

while the SSB phase noise $\mathrm{L_{SSB}}$ is calculated as:

$$\mathrm{L_{SSB}} = \frac{\mathrm{h}\cdot\nu}{2\cdot\eta_{PD}\cdot\mathrm{E_P}\cdot\mathrm{f_{rep}}}\left[1-\mathrm{e}^{-(2\cdot\pi\cdot\mathrm{n}\cdot\mathrm{f_{rep}}\cdot\tau_\mathrm{o})^2}\right]. \tag{4.25}$$

Herein, $\nu = \mathrm{c_0}/\lambda$ is the light frequency. An interesting fact is that the phase noise respectively jitter does not depend on the PD bandwidth at all, but rather on the optical pulse characteristics.

Fig. 4.18 illustrates the amplitude and phase noise contribution to the overall shot noise $\sigma^2_{\mathrm{shot}} = \frac{\mathrm{h}\cdot\nu}{\eta_{PD}\cdot\mathrm{E_p}}$ as a function of the optical pulse duty cycle $\mathrm{D_{opt}} = \tau_\mathrm{o}\cdot\mathrm{f_{rep}}$. It can be observed that for long optical pulse widths ($\tau_o \rightarrow \infty$), amplitude and phase noise equally contributes to the shot noise. For the ultrashort pulse limit ($\tau_o \rightarrow 0$), a significant imbalance between amplitude and phase noise up to several orders-of-magnitude can be observed, whereby the most part of the shot noise is concentrated in the amplitude noise. This imbalance results from spectral correlations in the shot noise, and the strength of the correlations is determined by the optical pulse width.
Regarding the pulse-sampling architecture, there are two consequences. On the one hand, a significant improvement of the clock jitter can be achieved using short optical pulses. The shot noise-limited pulse-to-pulse timing jitter $\sigma_{\mathrm{t,opt}}$ for the ultrashort pulse limit can be calculated from the SSB phase noise $\mathrm{L_{SSB}}$:

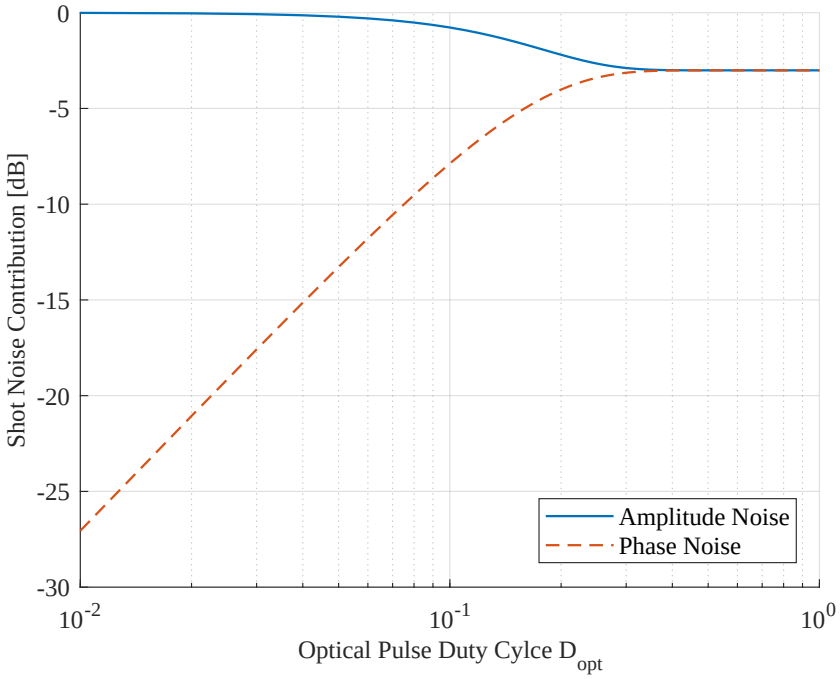


Figure 4.18: Contribution of the amplitude and phase noise to the overall shot noise as a function of the optical pulse duty cycle.

$$\begin{aligned}\sigma_{\mathrm{t}}^2 &= \frac{1}{(2\cdot\pi\cdot \mathrm{n}\cdot \mathrm{f_{rep}})^2}\cdot\int_0^{\frac{\mathrm{f_{rep}}}{2}} 2\cdot \mathrm{L_{SSB}}\mathrm{d}f \\ &\overset{\tau_o\to 0}{=} \frac{\mathrm{h}\cdot\nu}{2\cdot\eta_{PD}\cdot \mathrm{E_P}}\cdot\tau_{\mathrm{o}}^2.\end{aligned} \tag{4.26}$$

On the other hand, the amplitude noise corresponds to pulse-to-pulse energy fluctuations, which affect the sampler gain according to Eq. 4.21. Regarding the ultrashort pulse limit, results in a white noise with the variance:

$$\begin{aligned}\sigma_{\mathrm{p2p}}^2 &= \int_0^{\frac{\mathrm{f_{rep}}}{2}} 2\cdot \mathrm{L_{AM}}\mathrm{d}f \\ &\overset{\tau_o\to 0}{=} \frac{\mathrm{h}\cdot\nu}{\eta_{PD}\cdot \mathrm{E_p}},\end{aligned} \tag{4.27}$$

and the corresponding SNR of the sampler is given by:

$$\mathrm{SNR_{p2p}} = -20\cdot\log_{10}(\sigma_{\mathrm{p2p}}). \tag{4.28}$$

In [36], identical results were derived with a different approach. Herein the jitter of the position of the pulses center-of-mass was determined. In addition, the usage of an EDFA was considered in the calculations and leads to slightly different terms:

$$\sigma_t^2 = \frac{h \cdot \nu}{\eta_{PD} \cdot E_p} \cdot \frac{\tau_o^2}{2} \cdot [1 + \eta_{eff} \cdot (G_{EDFA} \cdot NF_{EDFA} - 1)], \tag{4.29}$$

respectively

$$\sigma_{p2p}^2 = \frac{h \cdot \nu}{\eta_{PD} \cdot E_p} \cdot NF_{EDFA}. \tag{4.30}$$

It is worth noting that the analysis for pulse shapes differing from the used Gaussian profile results in slightly different factors than $\frac{1}{2}$ in Eq. 4.29, but with the same dependency on the optical pulse width [89], [90].

Fig. 4.19 a) illustrates SNR_{p2p} due to optical pulse-to-pulse energy fluctuations as a function of the optical pulse energy E_p for $\tau_o = 300\,fs$, and an EDFA with a gain of $G_{EDFA} = 100$ and a noise figure of $10 \cdot \log_{10}(NF_{EDFA}) = 6\,dB$. At the nominal pulse energy of $E_p = 180\,fJ$, a SNR of $SNR_{p2p} \approx 55.7\,dB$ meets well the specification.
Fig. 4.19 b) shows the jitter of the photocurrent pulse train for the same parameters, and an outstanding jitter performance of $\sigma_t < 1\,fs$ outperforms that of a track-and-hold architecture significantly.

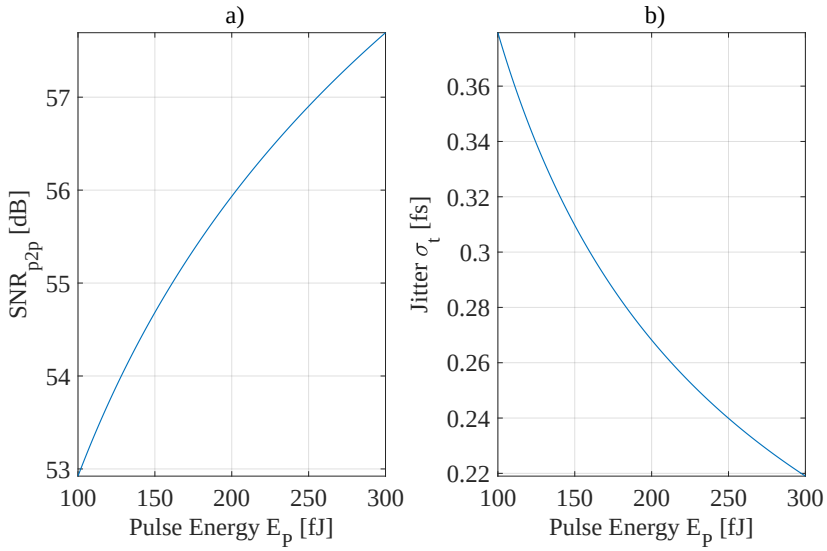


Figure 4.19: a) SNR_{p2p} due to optical pulse-to-pulse energy fluctuations as a function of the optical pulse energy E_p for $\tau_o = 300\,fs$, and an EDFA with a gain of $G_{EDFA} = 100$ respectively a noise figure of $10\log_{10}(NF_{EDFA}) = 6\,dB$. b) Jitter σ_t of the proposed pulse sampling architecture for the same parameters.

Influence of Mismatch

Regarding the pulse-sampling architecture, a power mismatch between the outputs of the CDN is translated into an equal gain mismatch. Recalling from Chapter 4.3.3, a relative power mismatch of $10 \cdot \log_{10}(\delta_E) = \pm 0.25\,\text{dB}$ is expected due to the WGs of different lengths. This results in $\text{TNHD}_{\delta G} = 26\,\text{dB}$ according to Eq. 2.20, and additional measures must be taken to meet the overall system specifications.
In addition, a bandwidth mismatch of the PDs will directly affect the transfer functions of the individual sub-samplers. Such a mismatch can hardly be calibrated in hardware, but compensation techniques in the digital domain have been reported by various authors [91], [92], [93], [94], [95], [96], [97].

5 Opto-Electronic Clock Converter

In Section 4.6, two architectures were investigated in detail with the focus on their potential for the low-jitter sampler application. It turned out, that both architectures require an O/E clock converter circuit, which converts the optical pulse train from the MLL into an electrical square wave signal with a duty cycle of 50 %. Regarding the track-and-hold architecture proposed in Chapter 4.6.1, this circuit is directly used to trigger the sampler, thus its jitter performance directly affects the overall sampler performance. In the pulse-sampling architecture proposed in Chapter 4.6.2, it is not involved in the sampler clock generation, but in the generation of a synchronous Demultiplexer (DEMUX) and MUX clock signals. In that case, the requirement on the jitter performance is not a primary design goal. In addition, the O/E clock converter circuit can be considered as a key enabling block for various low-jitter applications, which are driven by a square-wave signal.
This chapter discusses the design of the O/E clock converter circuit with the focus on its jitter performance. A detailed noise analysis is presented, which is used to estimate the inherent jitter of the proposed circuit. In addition, the measurement results of the implemented test chip are presented to validate the O/E co-integration and to verify the potential of the O/E clock converter circuit with respect to low-jitter applications.

5.1 Circuit Design

Fig. 5.1 illustrates a simplified schematic of the O/E pulse-to-clock converter [98], which converts the optical pulse train from the MLL into a low-jitter electrical square wave signal with a duty cycle of 50 %. The core of the circuit consists of a Current-Mode Logic (CML) differential Reset-Set (RS) latch, Q_3 and Q_4. The PD receiving the optical pulses is connected as the tail current source of a differential pair of transistors Q_1 and Q_2. Depending on the state at its electrical data input at the base connection of Q_1-Q_2, the differential pair Q_1-Q_2 directs the photocurrent pulse to either set or reset the RS-latch. Thus, this part of the circuit operates as an optically clocked D-flip-flop.
The present state of the RS-latch is inverted by Q_5-Q_6 and fed back to the data input, such that the next photocurrent pulse will toggle the state. As a result, in response to an optical pulse train, the O/E clock converter delivers an electrical square wave with a duty cycle of 50 %.
For reliable operation, the optical pulse energy must be large enough, such that the resulting current at the data input of the latch exceed the bias current of the latch $I_{bias,RS}$. In addition, the signal propagation

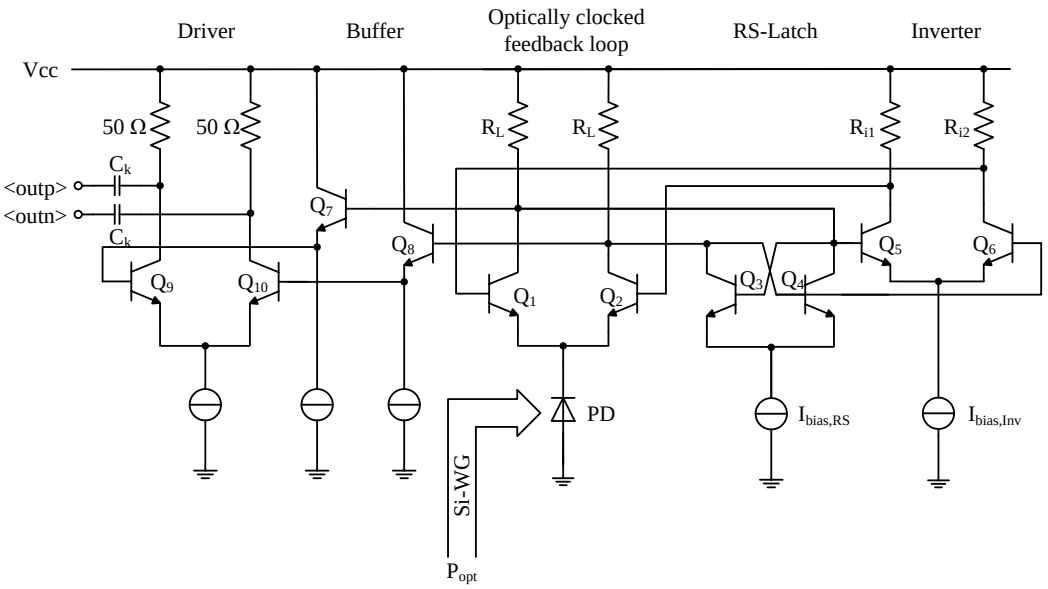


Figure 5.1: Simplified schematic of the O/E clock converter circuit.

delay $t_{d,latch}$ from the latch input to the differential pair input should be greater than the pulse width of the signal at the PD output. Otherwise, one single pulse will trigger multiple toggle events, and a stable state can not be achieved. Given an actual PD bandwidth of $f_{3dB} = 30\,\text{GHz}$ (first generation), a single buffer stage in the feedback loop - the inverter - suffices to provide enough hold time. Furthermore, the signal propagation delay $t_{d,latch}$ determines the maximum pulse repetition rate $f_{rep,max}$, since the latch must fully toggle its state to provide a stable input at the differential pair Q_1-Q_2:

$$f_{rep,max} \leq \frac{1}{t_{d,latch}}. \tag{5.1}$$

The emitter follower Q_7-Q_8 is used as high-speed buffer stage, while a driver Q_9-Q_{10} provides an AC-coupled differential 100 Ω interface to the measurement setup. The individual current sources are implemented by an emitter-degenerated current mirror.

Simulations have shown that an additional current source in parallel with the PD was not required to speed up the turn-on time of the optically clocked differential pair. The dark current of the PD for a bias voltage of $V_{bias,PD} > 2\,\text{V}$ is in the range of several hundred nano-ampères [41], and therefore sufficient to pre-bias the transistors.

In order to determine the jitter performance of the O/E clock converter, a well-established strategy proposed for the analysis of jitter in electronic frequency dividers is adapted from [99]. Herein,

the jitter σ_t of the voltage clock signal $v_{clk}(t)$ is calculated using the relationship:

$$\sigma_t^2 = \frac{\sigma_{v,noise}^2}{\left(\frac{dv_{clk}(t)}{dt}\Big|_{t=t_{thres}}\right)^2}, \tag{5.2}$$

where $\sigma_{v,noise}^2$ is the variance of the output noise voltage. It consists of the individual noise sources contributing to the overall noise.

Fig. 5.2 a) illustrates a schematic of the O/E clock converter core at the switching instant. It is assumed that the signal at the output of the latch has completely switched before the optical pulse arrives. Therefore, one of the differential pair transistors Q_1-Q_2 is conducting and directs the photocurrent $i_{PD}(t)$ to the load, while the other transistor is considered to be off. This simplification can also be applied to the latch transistors Q_3 and Q_4.
Neglecting the on-resistance of the conducting transistors, the circuit can be further simplified as shown in Fig. 5.2 b). Herein the capacitance C_L represents the total output capacitance, given by the input capacitance of the transistors connected to the output nodes and the interconnect capacitance. In addition, the noise sources affecting the zero-crossing of the clock signal are also shown. Regarding the clock switching instant, only one of the transistors pairs Q_1-Q_2 respectively Q_3-Q_4 is on, and the inherent transistor noise does not contribute. Therefore, the noise sources considered for the jitter calculation are the thermal noise of the load resistors $I_{n,RL}^2$, the noise of the PD $I_{n,PD}^2(t)$, and the noise of the emitter-degenerated current mirror providing the tail current $I_{bias,latch}$ of the latch.
The thermal noise of a load resistor in parallel to a capacitor was already derived in Chapter 3, Eq. 2.16. Since the noise voltages of the two load resistors are independent, the total noise $\sigma_{v,R_L,tot}^2$ at the differential output is given by

$$\begin{aligned}\sigma_{v,R_L,tot}^2 &= 2 \cdot \sigma_{RC,tot}^2 \\ &= \frac{2 \cdot k_B \cdot T}{C_L}.\end{aligned} \tag{5.3}$$

The power spectral density $S_{v,CM}$ of the noise voltage, originating from the emitter-degenerated current mirror, is given by

$$S_{v,CM}(f) = |Z_L|^2 \cdot S_{i,CM}, \tag{5.4}$$

where $Z_L = \frac{R_L}{1+\omega \cdot R_L \cdot C_L}$ is the load impedance and $S_{i,CM}$ the power spectral density of the noise current at the output of a emitter-degenerated current mirror [100]

$$S_{i,CM}(f) = 2k_B \cdot T \cdot g_m \cdot \frac{1 + 2 \cdot g_m \cdot R_E}{(1 + g_m \cdot R_E)^2}, \tag{5.5}$$

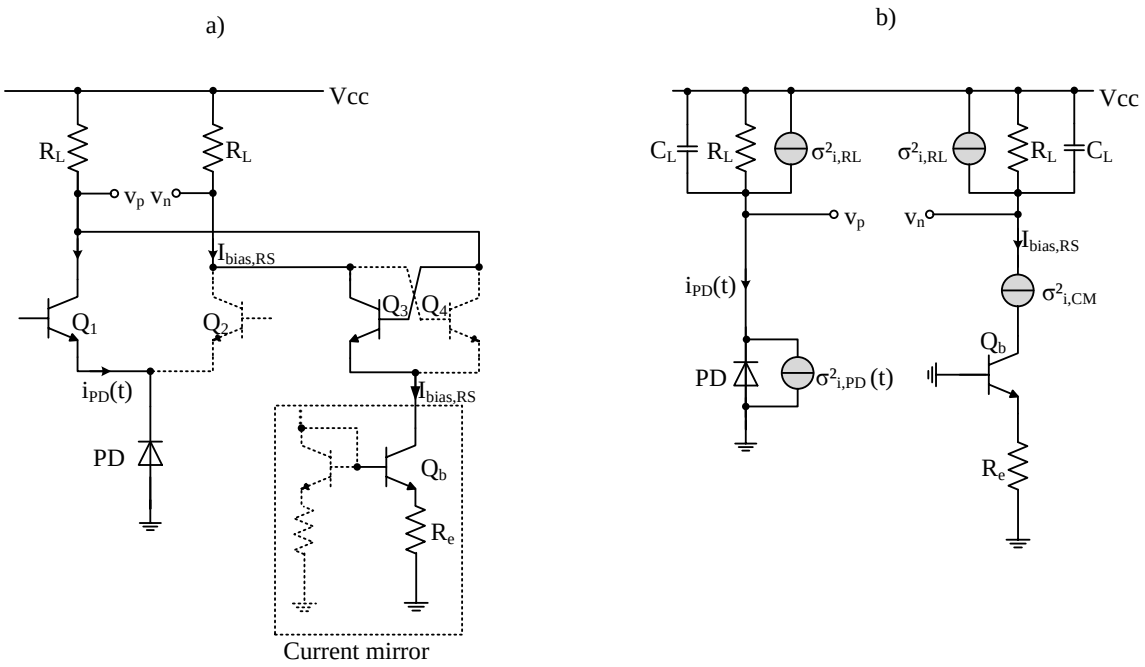


Figure 5.2: a) Schematic of the O/E clock converter core at the switching instant. b) Simplified schematic of the same circuit including noise sources.

where $g_m = \frac{I_{bias,RS}}{V_t}$. The total noise at the output voltage node is then given by integrating $\sigma^2_{v,CM}$:

$$\begin{aligned}\sigma^2_{v,CM,tot} &= \int_{f=0}^{\infty} S_{v,CM}(f)\mathrm{d}f \\ &= \frac{k_B \cdot T \cdot g_m \cdot R_L \cdot (1 + 2 \cdot g_m \cdot R_E)}{2 \cdot C_L \cdot (1 + g_m \cdot R_E)^2}.\end{aligned} \tag{5.6}$$

According to Eq. 5.6, the emitter degeneration lowers the output noise voltage contributed by the bias current source. This measure for improvement is limited by the voltage drop across R_E due to the total voltage headroom.

In order to calculate the jitter induced by the electronic devices, the slew rate of the clock signal at the switching instant must be determined. Assuming a constant node v_n during the zero-crossing, the slope of the differential clock signal is determined by the voltage drop across the photocurrent-driven load at node v_p:

$$v_p(t) = i_{PD}(t) * h_{RC}(t). \tag{5.7}$$

The impulse response $h_{RC}(t)$ of the RC network is given by

$$h_{RC}(t) = \frac{e^{-\frac{t}{\tau_{R_L} \cdot C_L}}}{C_L} \cdot u(t), \tag{5.8}$$

where $u(t)$ is the Heavyside step function:

$$u(t) = \begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}. \tag{5.9}$$

Assuming a photocurrent pulse response with a Gaussian shape, there is no closed-form solution of Eq. 5.7. Therefore, the slope of the clock signal is solved numerically in the following analysis.

Fig. 5.3 a) illustrates the jitter induced by the thermal noise and bias current source as a function of the optical design parameters, namely the bandwidth of the PD f_{3dB}, and the optical pulse energy E_p at the input of the PD. Herein, a resistance $R_L = 400\,\Omega$, a capacitance $C_L = 100\,\text{fF}$ and a constant voltage drop of $I_{bias,RS} \cdot R_E = 300\,\text{mV}$ are assumed. A high PD bandwidth and a high optical pulse energy value is required for a low jitter. Since the optical parameters do not affect the noise voltages (Eq. 5.3 and Eq. 5.6), the dependency of the jitter arises only from the slope of the photocurrent-induced voltage.
Fig. 5.3 b) illustrates the jitter induced by the thermal noise and bias current source as a function of the electrical design parameters, namely R_L and C_L, for a constant PD bandwidth of $f_{3dB} = 30\,\text{GHz}$ and an optical pulse energy of $E_p = 200\,\text{fJ}$. A small jitter is achieved by minimizing the load capacitance at the output nodes, while the load resistors should be maximized. It should be noted that increasing the resistance also affects the time constant of the RC network and therefore the total gate delay. As a consequence, there is a trade-off between the maximum operation speed and the jitter of the O/E clock converter.

The overall jitter of the clock converter is the superposition of the jitter induced by the electronic circuit devices and the jitter induced by the PD. Fig. 5.4 a) and b) illustrates the total jitter of the O/E clock converter as a function of the optical design parameters, respectively the electrical design parameters. It can be seen that the most effective method to improve the jitter performance is to maximize the PD bandwidth and the optical power, while the electrical design parameters show only a little influence on the overall jitter.

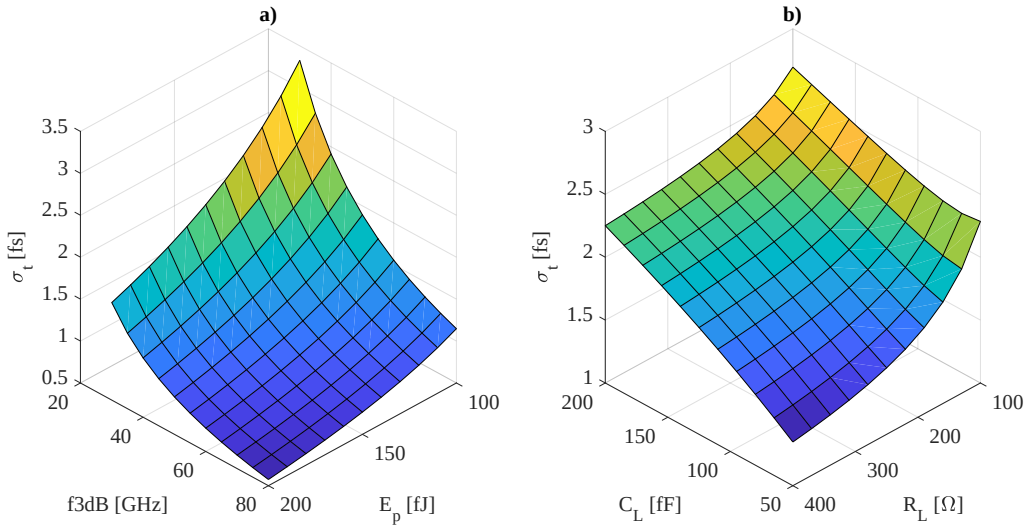


Figure 5.3: a) Jitter induced by the electronic circuit devices of the O/E clock converter as a function of the optical design parameters, the 3 dB-bandwidth of the PD and the optical pulse energy ($R_L = 400\,\Omega$ and $C_L = 100\,fF$). b) Jitter induced by the electronic circuit devices of the O/E clock converter as a function of the electrical design parameters R_L and C_L ($f_{3dB} = 30\,GHz$ and $E_p = 200\,fJ$).

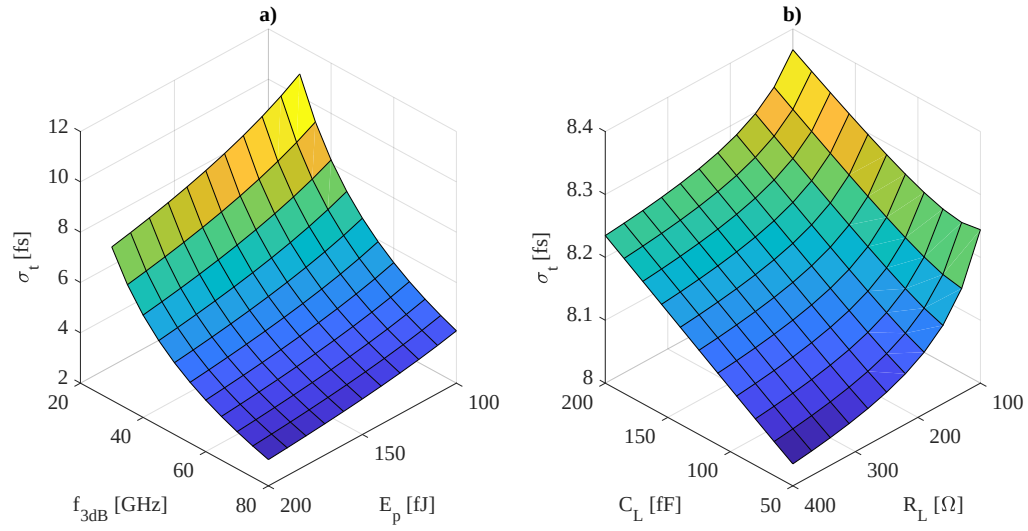


Figure 5.4: a) Overall jitter of the O/E clock converter as a function of the optical design parameters ($R_L = 400\,\Omega$ and $C_L = 100\,fF$). b) Overall jitter of the O/E clock converter as a function of the electrical design parameters ($f_{3dB} = 30\,GHz$ and $E_p = 200\,fJ$). A constant voltage drop of $I_{bias,RS} \cdot R_E = 300\,mV$ across R_E is assumed.

5.2 Experimental Results

5.2.1 Measurement Setup

A block diagram of the photonic test chip including the O/E clock converter (OECC) is shown in Fig. 5.5. The optical pulse train from the MLL is coupled out of the fiber into the WG by the input grating. The optical signal is split into 8 branches using 1x2 MMI couplers and distributed across the chip. At one branch, an output grating coupler enables the measurement of the optical power at the end of the CDN for the purpose of optimum fiber positioning, polarization adjustment, and the characterization of non-linear losses in the CDN. At the output of the other branches, either a PD for the purpose of large-signal characterization or an O/E clock converter circuit is placed. Placing the electronic circuits as close as possible to the pads ensures proper matching of the $Z_L = 100\,\Omega$ differential microstrip lines with the on-wafer probe as measurement interface. The total chip area including pads is $A_{chip} = 3.1$ mm x 2.7 mm.
In the inlet in Fig. 5.5, a chip photograph of the O/E clock converter after finalization of the first metal layer is shown. The PD is placed as close as possible to the switching transistors and connected to the electronic domain over thick metal layers (not shown in the figure) to minimize parasitic inductances. The O/E clock converter unit occupies an area of $A_{OECC} = 490\,\mu$m x 250 μm and consumes an overall power of $P_{tot} = 230$ mW from a Vcc = 4.5 V power supply, but it should be noted that about 40 % of this power is needed by the output buffer for proper driving of the external load as a part of the measurement setup.

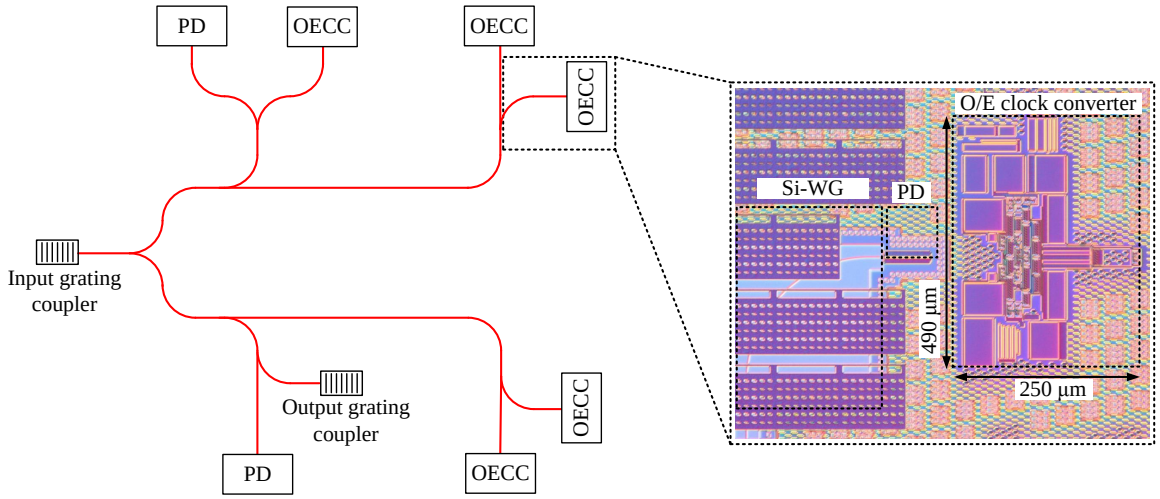


Figure 5.5: A block diagram of the processed test chip.

Fig. 5.6 illustrates a block diagram of the measurement setup used for the characterization of the test chip. An optical pulse train with a pulse repetition rate of $f_{rep} = 10\,\text{GHz}$ and a pulse duration $\tau_{FWHM} = 200\,\text{fs}$ is generated on the basis of a MLL with a fundamental repetition rate $f_{rep} = 1.25\,\text{GHz}$ through 1x8 time-interleaving using a fiber-based MUX.
A Variable Optical Attenuator (VOA) reduces the optical power to protect the subsequent EDFA [101], which boosts the optical signal to the desired maximum power level of $p_{opt,in} = 20\,\text{dBm}$ at the input of the chip. The optical pulse width is hereby increased to $\tau_{FWHM} = 300\,\text{fs}$.

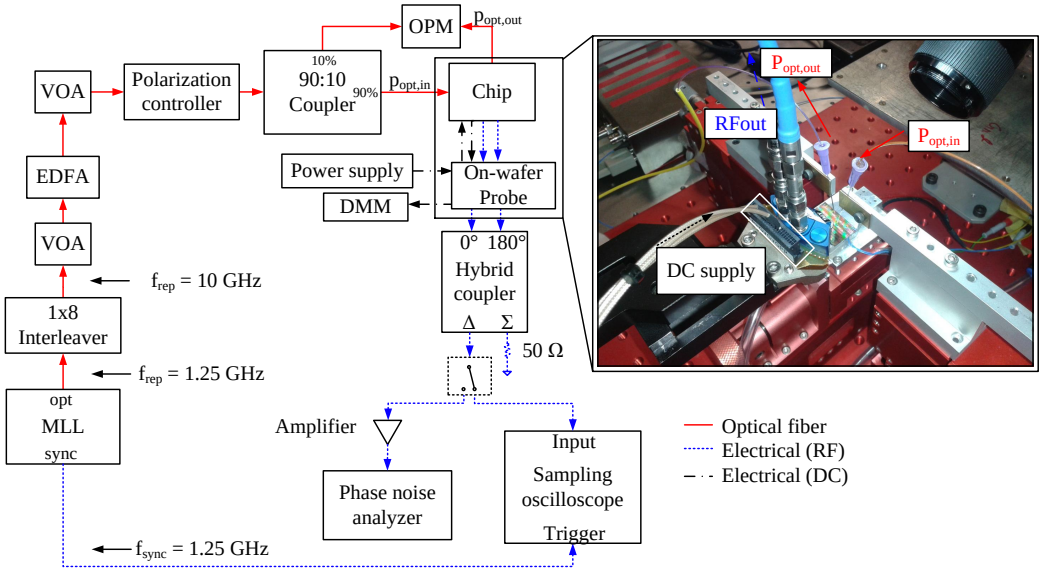


Figure 5.6: A block diagram of the measurement setup used for the characterization of the O/E clock converter circuit.

A VOA at the output of the EDFA adjusts the optical power at the input of the chip, while the optimum polarization for the grating coupler is set by a 3-paddle polarization controller.
A 90:10 coupler is placed in front of the optical input of the chip, which enables to monitor the optical power. The 90 % output provides the input signal for the chip with a power $p_{opt,in}$, while an Optical Power Meter (OPM) is connected to the 10 % output port of the coupler. An optimum coupling of the optical signal into the chip requires a certain positioning of the fiber above the input grating. This is achieved by accurately position the fiber using a micromanipulator as shown in the camera picture inset in Fig. 5.6. The second fiber, positioned above the output grating coupler, is connected to an OPM, thus providing a measure of the optical power coupled into the chip. More precisely, $P_{opt,out}$ is equal to

the optical power at the input of the PDs minus the losses of the grating coupler $\alpha_{\mathrm{gr}} = 10 \cdot \log_{10}(\eta_{gr})$ and losses of the fiber facet $\alpha_{\mathrm{facet}} \approx 0.5\,\mathrm{dB}$:

$$p_{\mathrm{opt,out}} = p_{\mathrm{opt,PD}} - \alpha_{\mathrm{gr}} - \alpha_{\mathrm{facet}}. \tag{5.10}$$

A customized on-wafer probe head [102] is placed at the contact pads. It provides the DC probe tips for the supply voltage, and differential Radiofrequency (RF) tips in a GSGSG configuration for the acquisition of the high-frequency signals. Measurements have shown significant voltage drop across the ohmic contacts, which is compensated by measuring the internal supply voltage with a high-impedance Digital Multimeter (DMM) and thereby adjusting the externally applied voltage properly. The differential output of the O/E clock converter is converted into a single-ended signal using a broadband 180° hybrid coupler [103]. A wideband sampling oscilloscope with a bandwidth of $f_{3\mathrm{dB}} = 67\,\mathrm{GHz}$ [104] is used for time-domain visualization. The trigger signal for the oscilloscope is derived from an auxiliary electrical output of the MLL, thus providing a synchronous electrical pulse comb. The jitter of the O/E clock converter is determined in the frequency domain by measuring the phase noise with a signal source analyzer [105]. An additional amplifier [106] at the output of the chip is used to increase the signal power level, which is required for a sufficiently high sensitivity of the phase noise analyzer.

5.2.2 Measurement Results

At first, the non-linear losses in the CDN were determined by measuring the optical power $p_{\mathrm{opt,out}}$ at the output grating as a function of the input power $p_{\mathrm{opt,in}}$ as shown in Fig. 5.7. Considering the facet

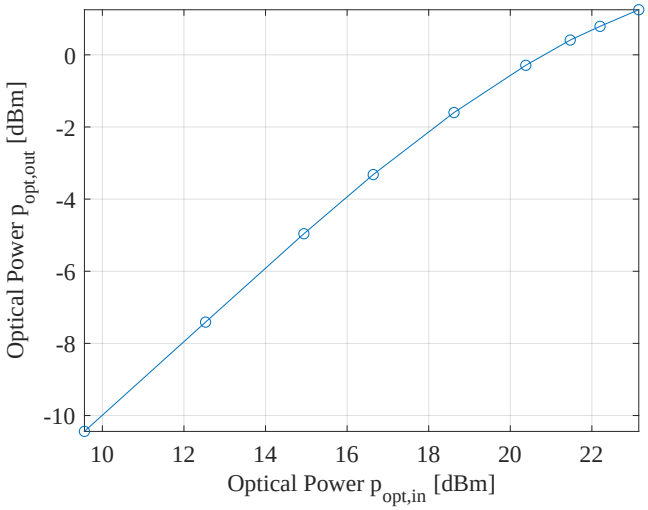


Figure 5.7: Measured optical power $p_{\mathrm{opt,out}}$ at the output grating of the CDN as a function of the optical input power $p_{\mathrm{opt,in}}$.

losses from the two fibers of $2 \cdot \alpha_{\text{facet}} = 1\,\text{dB}$ and a separately measured grating coupler insertion loss of $\alpha_{\text{gr}} = 4\,\text{dB}$, the total attenuation from input grating to the PD is $\alpha_{\text{tot}} < 16\,\text{dB}$ for an input power values up to $p_{\text{opt,in}} = 20\,\text{dBm}$, including the power split to the eight outputs. For higher input power values, non-linear losses as introduced in Chapter 4.3 become more significant, thus increasing the overall attenuation and leading to distortion of the optical pulse.

At next, the PD response to the $f_{\text{rep}} = 10\,\text{GHz}$ optical pulse train from the MLL is investigated at one of the CDN branches. The bias voltage $V_{\text{bias,PD}}$ for the PD is applied using a wideband bias-T, while the single-ended RF output is fed either to the sampling oscilloscope or to a spectrum analyzer. Fig. 5.8 a) illustrates the normalized variation in time of the PD output voltage for 10 subsequent pulses as response to the optical pulse train from the MLL with an optical input power $p_{\text{opt,in}} = 20\,\text{dBm}$, and a PD bias voltage of $V_{\text{bias,PD}} = -3\,\text{V}$. An amplitude variation, which repeats after eight pulses, results from the non-ideal optical interleaving used for the repetition rate multiplication mentioned in Chapter 4.5.

Fig. 5.8 b) illustrates the normalized spectrum of the PD output for the same operating point. At first, one may notice that the frequency of the carrier is not exactly $f_{\text{rep}} = 10\,\text{GHz}$, but rather $f_{\text{rep}} = 10.08\,\text{GHz}$. Measuring the MLL fundamental frequency confirm that the used MLL is operating at a frequency of $f_{\text{rep}} = 1.26\,\text{GHz}$. In addition, spurs with a frequency spacing of $\Delta f = 1.26\,\text{GHz}$ can be observed in the spectrum. These spurs are also the result of an amplitude and phase mismatch of the non-ideal interleaver used for the repetition rate multiplication.

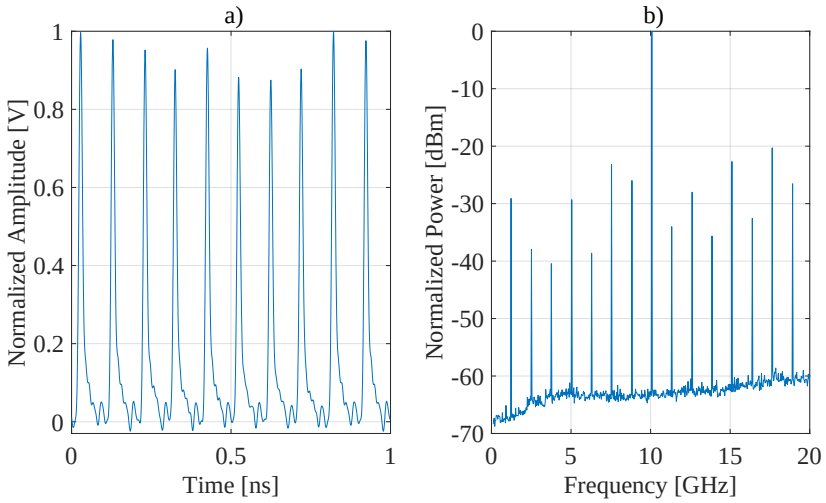


Figure 5.8: a) Normalized variation in time of the PD output voltage for 10 subsequent pulses as response to a $f_{\text{rep}} = 10\,\text{GHz}$ optical pulse train with an optical input power $p_{\text{opt,in}} = 20\,\text{dBm}$, and a PD bias voltage of $V_{\text{bias,PD}} = -3\,\text{V}$. b) Normalized spectrum at the output of the PD for the same operating point.

The large-signal behaviour of the PD was investigated for different optical input power values, aiming at determining the onset of saturation of the PD. Fig. 5.9 illustrates the normalized variation in time of the PD output voltage for different optical input power values $p_{opt,in}$. While the relevant rising edge is not affected by the higher pulse energy values, a slightly pulse widening from $\tau_{FWHM} = 12\,ps$ to $14\,ps$ can be observed for increasing the optical input power from $p_{opt,in} = 18\,dBm$ to $23\,dBm$.

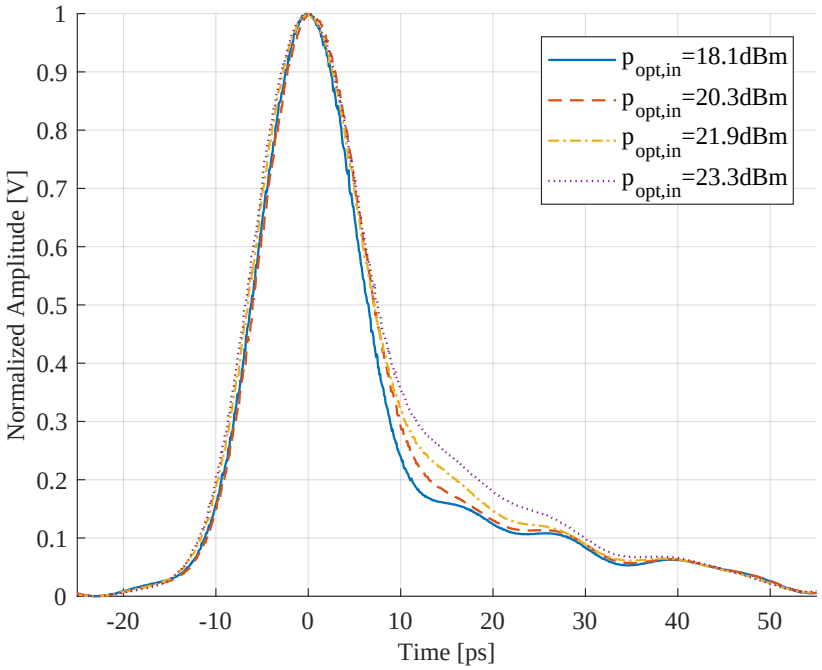


Figure 5.9: Normalized variation in time of the PD output voltage for different optical input power values.

Finally, the measurement results of the actual O/E clock converter circuit are presented. Fig. 5.10 illustrates the measured variation in time of the output voltage as a function of the optical input power. A rectangular waveform with a period of $t_p = 200\,ps$ can be observed, which corresponds to the expected frequency of $f_{OECC,out} = 5\,GHz$. A minimum power of $p_{opt,in} = 14\,dBm$ is required for a stable operation, which corresponds to a pulse energy at the input of the PD of $E_{p,PD} = 63\,fJ$.
Further increasing of the optical power results only in a small change of the output amplitude, which is expected since the output amplitude of the O/E clock converter is basically determined by the current of the output driver and its load. On the other hand, higher optical input power values should increase the maximum slew rate of the signal, which could not be observed from the measurements, since it is determined by the limited bandwidth of the measurement setup at the output of the chip. In addition, measurements on the single-ended output signals have shown that the differential-to-single-ended conversion, performed by the hybrid coupler, does not work accurately. A proper phase matching

between the two single-ended output signals could not be assured due to the lack of phase-matched cables in this setup. As a consequence, one major advantage of the differential topology - the suppression of supply noise - may not be exploited entirely, as it will be shown soon in the phase-noise measurement.

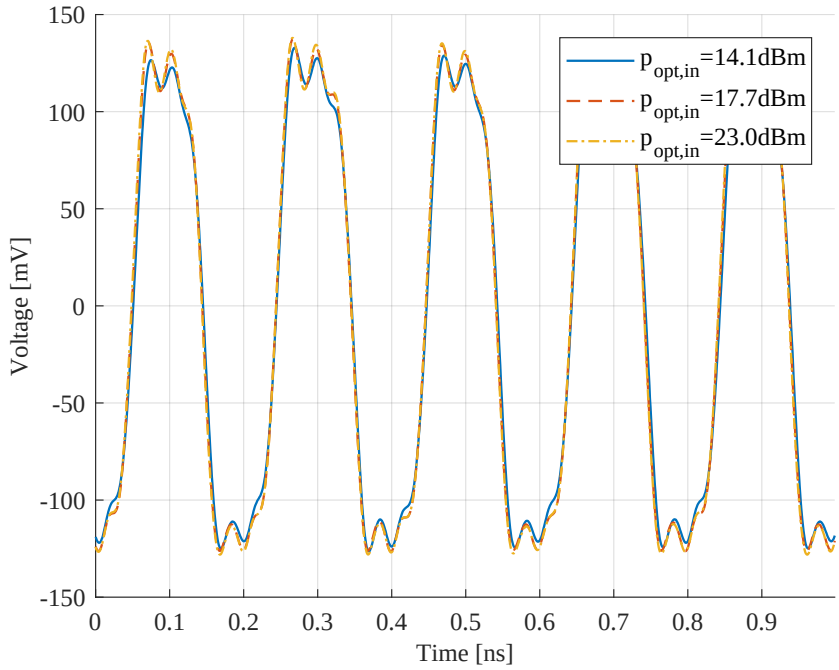


Figure 5.10: Measured variation in time of the O/E clock converter output voltage for different optical input power values.

The maximum operation speed of the O/E clock converter is estimated by measuring its self-oscillation frequency f_{res}. For this purpose, a continuous-wave laser source is used to bias the frequency divider circuit near its threshold. As a result, the flip-flop oscillates at a frequency reciprocal to the corresponding gate delay $t_{d,latch}$ [107]:

$$f_{res} = \frac{1}{2 \cdot t_{d,latch}}. \tag{5.11}$$

Since the the circuit is able to toggle its state two times within a period $t_p = \frac{1}{f_{res}}$, the maximum operating pulse repetition rate is twice of the self-oscillating frequency. The gate delay depends on the operating point of the differential pair Q_1-Q_2, hence f_{res} depends on the average optical power at the input of the PD. Fig. 5.11 illustrates the measured self-oscillation frequency as a function of the optical input power. It ranges between $6.5\,\text{GHz} \leq f_{res} \leq 11.8\,\text{GHz}$, which is sufficient for optical pulse repetition rates between $13\,\text{GHz} \leq f_{rep} \leq 23.6\,\text{GHz}$.

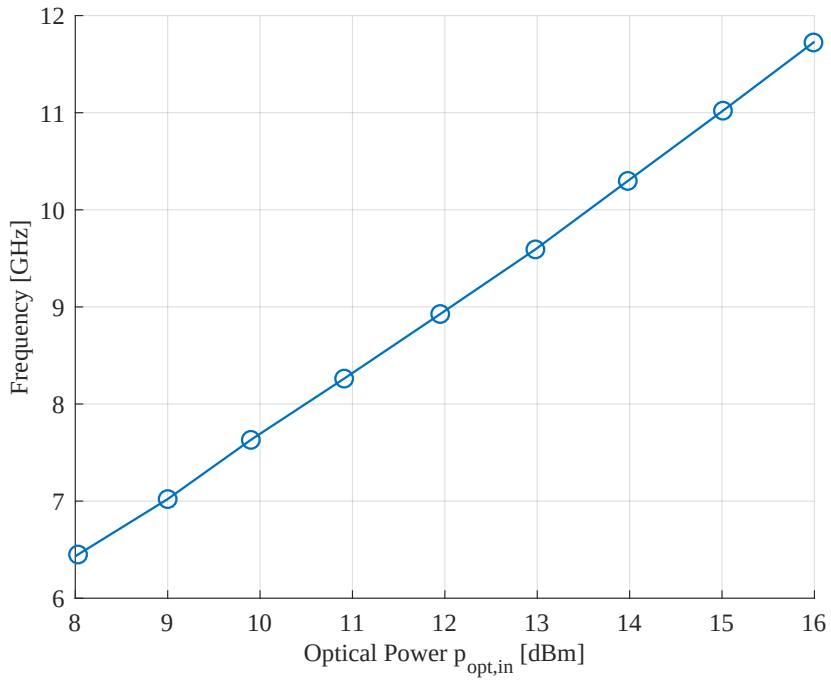


Figure 5.11: Measured self-oscillation frequency f_{res} of OE clock converter as a function of the average optical power of the continuous-wave laser.

At last, the jitter performance of the O/E clock converter is characterized. Usually, the jitter of a clock signal is determined by measuring its phase noise in the frequency domain, since the jitter sensitivity of modern phase noise test systems outperforms that of an oscilloscope by orders-of-magnitude. Jitter and phase noise describe the same phenomenon from different points of view. Jitter as the aperture uncertainty in the time domain corresponds to an instability of the frequency, and is described by phase noise in the frequency domain. Regarding a clock signal with a frequency f_{clk}, the jitter σ_t is related to the measured SSB phase noise $L_{SSB}(f)$ by [108]:

$$\sigma_t = \frac{1}{2 \cdot \pi \cdot f_{clk}} \cdot \sqrt{2 \cdot \int_0^\infty 10^{\frac{L_{SSB}(f)}{10}} df}. \tag{5.12}$$

In order to obtain the in-band noise that will affect the actual SNR of the sampler, the integration limits in Eq. 5.12 are substituted by a finite intervall $[f_{low}, f_{hi}]$. The lower limit f_{low} depends on the observation period of interest, which is usually determined by the memory depth of the subsequent ADC. With respect to the target application, the lower integration limit is set to $f_{low} = 1\,\text{kHz}$. The

upper limit f_{hi} depends on the bandwidth of the clock input of the actual sampler [109].
Fig. 5.12 illustrates the measured phase noise for different optical input power values. In addition, the phase noise of the signal at the output of the PD is represented, which is a good indication for the MLL phase noise. It has been shifted down by 6 dB compared to the phase noise of the OECC due to the difference by a factor of two in the considered signal frequencies.
For offset frequency values in the range $1\,\text{kHz} \leq f_{offset} < 40\,\text{kHz}$, the phase noise is mainly determined by the MLL. For offset frequencies in the range $40\,\text{kHz} \leq f_{offset} < 3\,\text{MHz}$, an unusual bulge is observed. In this region, the phase noise of the single-ended output of the O/E clock converter shows up to 3 decibel more noise compared to the differential output, which is suppressed by the differential configuration. The bulge indicates that the noise canceling of the differential-to-single-ended operation by the hybrid coupler does not work properly, as already observed in the time-domain measurement. For offset frequency values $f_{offset} \geq 3\,\text{MHz}$, the wideband phase noise floor is reached. Increasing the optical input power up to $p_{opt,in} = 17.7\,\text{dBm}$ significantly lowers the phase noise floor down to $L_{SSB} = -160\,\text{dBc/Hz}$, where the measurement limit of the used setup is achieved [105].
In terms of jitter, three regions can be identified: the main contribution lies within an offset frequency range of $1\,\text{kHz} \leq f_{offset} < 2\,\text{kHz}$ with a corresponding jitter $\sigma_t = 24\,\text{fs}$ originating solely from the MLL. The result was expected, since no PLL feedback control was available for the used MLL to suppress inherent noise, as mentioned in Chapter 4.5.The phase noise for offset frequencies

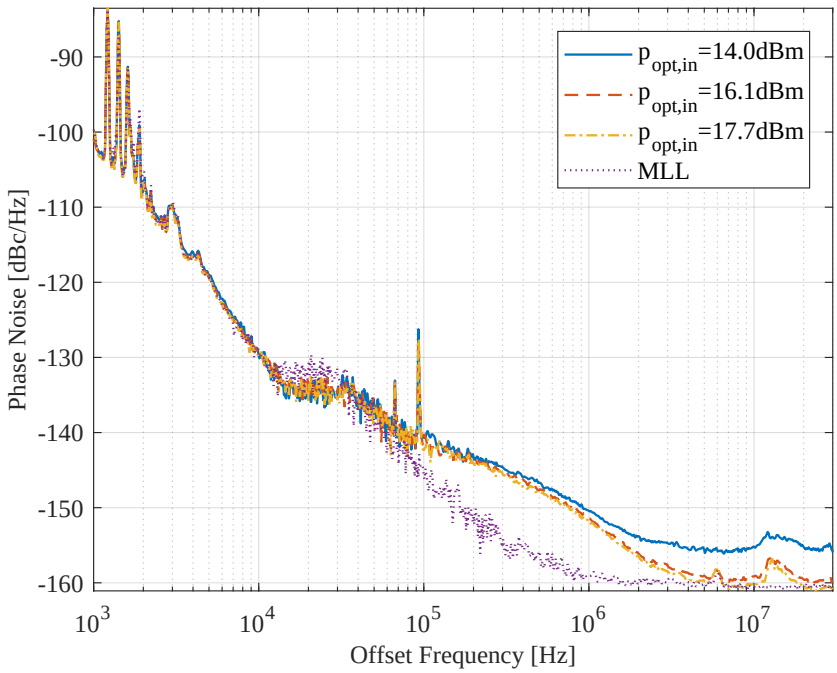


Figure 5.12: Measured phase noise of the OE clock converter for different optical input power values.

$2\,\text{kHz} \leq f_{\text{offset}} < 30\,\text{MHz}$ corresponds to a jitter $\sigma_t < 1\,\text{fs}$. Regarding offset frequencies $f_{\text{offset}} \geq 30\,\text{MHz}$ and sufficient high input power, an upper limit for the jitter can be estimated from the minimum noise level of $L_{\text{SSB}} = -160\,\text{dBc/Hz}$. Including the noise figure of $10 \cdot \log_{10}(\text{NF}_{\text{edfa}}) = 6\,\text{dB}$ of the used amplifier in the calculation [110], and integrating the resulting phase noise $L_{\text{SSB}} = -166\,\text{dBc/Hz}$ up to the Nyquist frequency of 2.5 GHz as used in the model [36], a jitter $\sigma_t = 11.2\,\text{fs}$ is obtained. Regarding a separately measured PD bandwidth $f_{3\text{dB}} = 30\,\text{GHz}$ and $\eta_{\text{PD}} = 40\%$, the measurement results matches very well with the theoretical model according to Fig. 4.15.

Table 5.1 summarizes the performance of the implemented O/E clock converter circuit.

Minimum optical power at the chip input	$p_{\text{opt,in}} = 14\,\text{dBm}$	
Minimum pulse energy at the PD input	$E_{\text{P,min}} = 63\,\text{fJ}$	
Nominal pulse repetition rate	$f_{\text{rep}} = 10\,\text{GHz}$	
Nominal output frequency	$f_{\text{OECC,out}} = 5\,\text{GHz}$	
Wideband phase noise floor ($f_{\text{rep}} = 10\,\text{GHz}$, $E_P = 100\,\text{fJ}$)	$L_{\text{SSB}} < -166\,\text{dBc/Hz}$	
Jitter ($f_{\text{rep}} = 10\,\text{GHz}$, $E_P = 100\,\text{fJ}$)	$\sigma_t = 23.1\,\text{fs}$	for $1\,\text{kHz} \leq f_{\text{offset}} < 2\,\text{kHz}$
	$\sigma_t < 1\,\text{fs}$	for $2\,\text{kHz} \leq f_{\text{offset}} < 30\,\text{MHz}$
	$\sigma_t = 11.2\,\text{fs}$	for $30\,\text{MHz} \leq f_{\text{offset}} < 2.5\,\text{GHz}$
Differential output voltage	$v_{\text{out}} = 250\,\text{mV}$	
Differential output impedance	$Z_{\text{out}} = 100\,\Omega$	
Maximum pulse repetition rate	$f_{\text{rep,max}} = 24\,\text{GHz}$	
Core area	$A_{\text{OECC}} = 490\,\mu\text{m} \times 250\,\mu\text{m}$	
Power consumption	$P_{\text{tot}} = 230\,\text{mW}$	

Table 5.1: Performance summary of the implemented O/E clock converter.

6 Optically Clocked Sampler Core Unit

This chapter focuses on the design of the 10 GS/s sampler core suitable for the implementation in the 80 GS/s TI ADC. The sampler is based on the pulse-sampling architecture proposed in Chapter 4.6.2 due to its superior jitter performance. The key building blocks and their influence on the sampler performance are investigated, and design guidelines are provided. In the end, the measurement results of the implemented test chip are presented.

6.1 Circuit Design

Fig. 6.1 illustrates the block diagram of the implemented 10 GS/s sampler core. Regarding the clock path, a PD followed by a TIA is used to convert the optical pulse train <clk_{opt}> from the MLL into an electrical voltage pulse train <clk_{el}> to drive the multiplier. In the signal path, an input buffer provides a differential impedance $Z_L = 100\,\Omega$ interface to the measurement setup and decouples the sampler from the signal source.

The integration-and-reset operation is implemented using a TI topology. Therefore, the weighted pulse train from the output of the multiplier is alternately directed by a DEMUX into two parallel paths, each operating at half of the MLL repetition rate. The reset operation is simply performed by connecting the output of the inactive integrator to a constant potential.

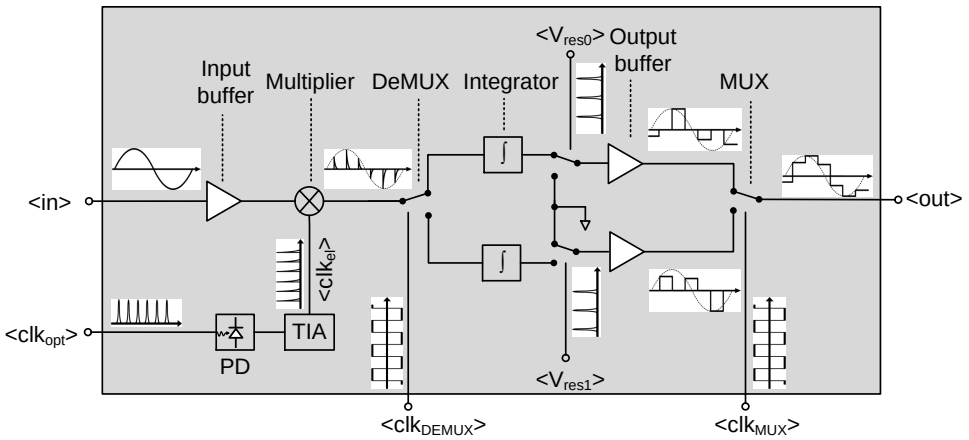


Figure 6.1: A block diagram of the implemented 10 GS/s pulse-sampling architecture.

Using such a configuration, the trigger signals for the reset operation, <V_{res0}> and <V_{res1}>, can be directly derived from an auxiliary output of the multiplier, as it will be shown later. In addition, the interleaving increases the hold time for the subsequent stages by a factor of two, which can be beneficial especially at highest sampling rates.
At the output, a MUX merges both data streams to form the full-rate sample stream, while buffer amplifers in between reduce its impact on the integration operation.
In the particular design, the clock signals <clk_{DEMUX}> and <clk_{MUX}> are generated off-chip.

Fig. 6.2 illustrates a simplified schematic of the implemented sampler core. It consists of the input buffer as interface to the measurement setup, the multiplier, the DEMUX, and the two banks of capacitors as integrators. A fully differential topology is chosen, which benefits from the high-level suppression of common-mode noise. As a matter of fact, thanks to the symmetrical configuration of the circuit, noise affects both signal paths equally. As the actual signal is obtained from the difference of both paths, any common-mode disturbance, such as noise from the power supply, is rejected.
A Common-Base (CB) circuit, consisting of Q_1-Q_2, is used as input buffer stage. The transistors are biased for maximum f_T, thus contributing to the achievement of a high sampler bandwidth. The input stage is designed for a full-scale signal amplitude $\hat{v}_{in} = 500\,mV$. This corresponds to a signal current of $\hat{i}_{in} = 5\,mA$ at a differential impedance $Z_L = 100\,\Omega$, so a bias current of $I_{bias,core} = 10\,mA$ is selected. The input impedance of the CB configuration is given by [111]

$$r_{in} = \frac{1}{g_m + \frac{1}{r_\pi}} = \frac{\beta_0}{\beta_0 + 1} \cdot \frac{1}{g_m}, \tag{6.1}$$

where $g_m = \frac{I_{bias,core}}{V_t}$ is the transconductance, r_π the small-signal input resistance, and β_0 is the forward current gain. For the given bias current, two resistors $R_{in} = 47\,\Omega$ are set in series to the emitter input to provide a differential $100\,\Omega$ interface at the sampler input.
The multiplication is performed by two pairs of switching transistors, Q_3-Q_4 and Q_5-Q_6, which are driven by the opto-electronic-converted voltage pulse train, $(v_{clk,p} - v_{clk,n})$. Herein, the outputs of Q_3 and Q_6 correspond to the actual multiplier output as illustrated in Fig. 6.2. Q_4 and Q_5 provide an auxiliary output to generate the voltage strobes required for the active reset of the integrators.
The current densities of the HBTs are set to achieve a minimum pulse width, which results in a maximum sampler bandwidth.
The DEMUX in the signal path, consisting of Q_7-Q_8 and Q_{15}-Q_{16}, switches the signal alternately to two pairs of hold capacitors, which perform the integration operation of the current pulses.
The voltage strobes to trigger the reset of the hold capacitors, <$V_{res,0}$> and <$V_{res,1}$>, are generated by alternately superposing a constant bias current I_{comp} to the corresponding auxiliary outputs of the multiplier.

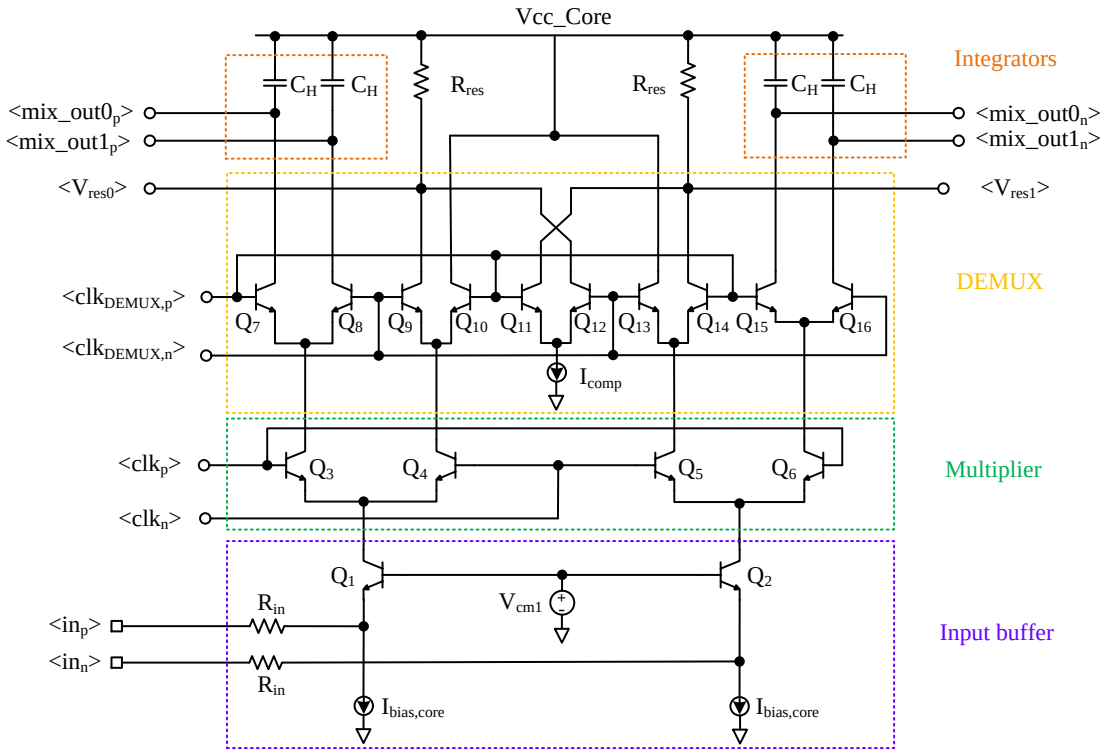


Figure 6.2: A simplified schematic of the implemented 10 GS/s sampler core, consisting of the input buffer, the multiplier, the DEMUX and the integrators.

Fig. 6.3 illustrates a simplified schematic of the implemented TIA, which converts the current pulses generated by the PD into a differential voltage signal to drive the multiplier. A CB topology is selected, which provides a high bandwidth respectively a short pulse width of the output voltage, and therefore a large sampler bandwidth.

In addition, it provides a constant reverse PD bias voltage $V_{bias,PD} = -(I_{bias,TIA,n} \cdot R_n + V_{be})$, which benefits proper operation of the PD irrespective of the large-signal voltage signals generated at the output of the TIA. Large inductors in series to the bias current sources fulfill two purposes. On the one hand, they directly filter high-frequency noise components originating from the current source. On the other hand, they increase the high-frequency output impedance of the current source from the view of the emitter of Q_1. As a consequence, the shot noise from Q_1 will flow into the low-impedance emitter input of Q_1 and does not contribute to the output node <clk_p>.

Neglecting the base current of Q_1, the non-inverting, pseudo-differential voltage (<clk_p>-<clk_n>) is

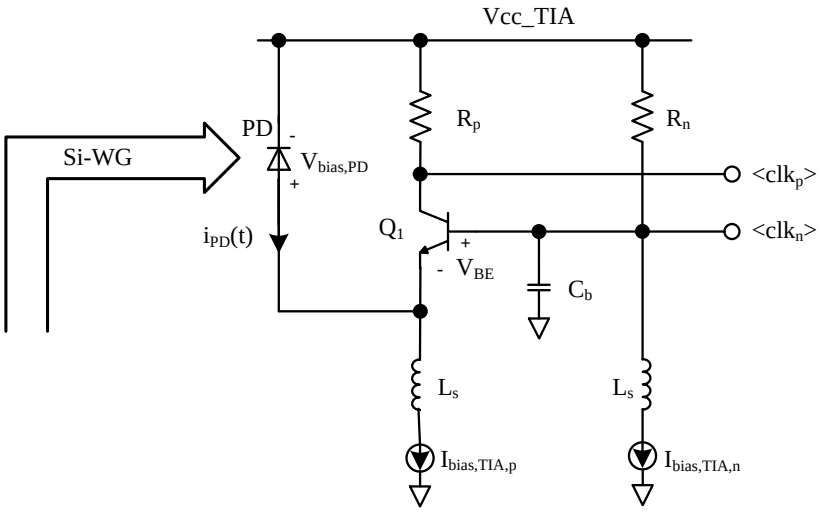


Figure 6.3: A simplified schematic of the implemented TIA.

given by:

$$v_{clk,diff} = i_{PD}(t) \cdot R_p + I_{bias,TIA,n} \cdot R_n - I_{bias,TIA,p} \cdot R_p. \tag{6.2}$$

To minimize the pulse width of the TIA output voltage, the bandwidth of the CB must be maximized. The transfer function is given by [100]

$$\frac{V_{clk,p}(j \cdot \omega)}{I_{PD}(j \cdot \omega)} = \frac{R_p}{\left(1 + j \cdot \omega \cdot \frac{C_{in}+C_{\pi}}{g_m}\right) \cdot \left(1 + j \cdot \omega \cdot R_p \cdot C_{out}\right)}. \tag{6.3}$$

According to Eq. 6.3, the two poles $p_1 = -\frac{1}{R_p \cdot C_{out}}$ and $p_2 = -\frac{g_m}{C_{in}+C_{\pi}}$ must be maximized. A higher collector bias current gives a higher input pole for a given C_{in}, but it requires a greater voltage headroom due to the voltage drop across R_p.

An active circuit is required to reset the integrator capacitors to a specific initial voltage. A simplified schematic of the implemented circuit is shown in Fig. 6.4. The voltage strobes $V_{res,X}$ ($X \in \{0;1\}$) generated in the sampler core (Fig. 6.2) are compared with an internally-generated constant potential $V_{cm,reset}$ to decide whether or not the nodes <mix_outXp> and <mix_outXp> are pulled to the potential $V_b - V_{be}$.

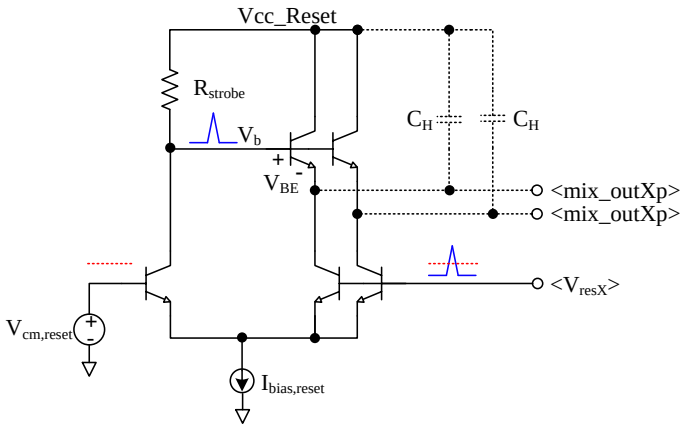


Figure 6.4: A simplified schematic of the active reset circuit.

Fig. 6.5 illustrates a simplified schematic of the output stage of the 10 GS/s sampler core, consisting of the buffer amplifiers and the MUX to merge the data streams. Emitter-followers $Q_1 - Q_4$ are used as buffer amplifiers to decouple the MUX from the hold capacitors. Two emitter-degenerated differential pairs, consisting of $Q_5 - Q_8$, are designed to provide sufficient bandwidth and linearity. The MUX, consisting of $Q_{13} - Q_{16}$, directs the desired signal in the hold mode to the $R_L = 50\,\Omega$ load resistors, while the undesired signal is dumped in the auxiliary outputs, terminated by the diodes $D_1 - D_4$.

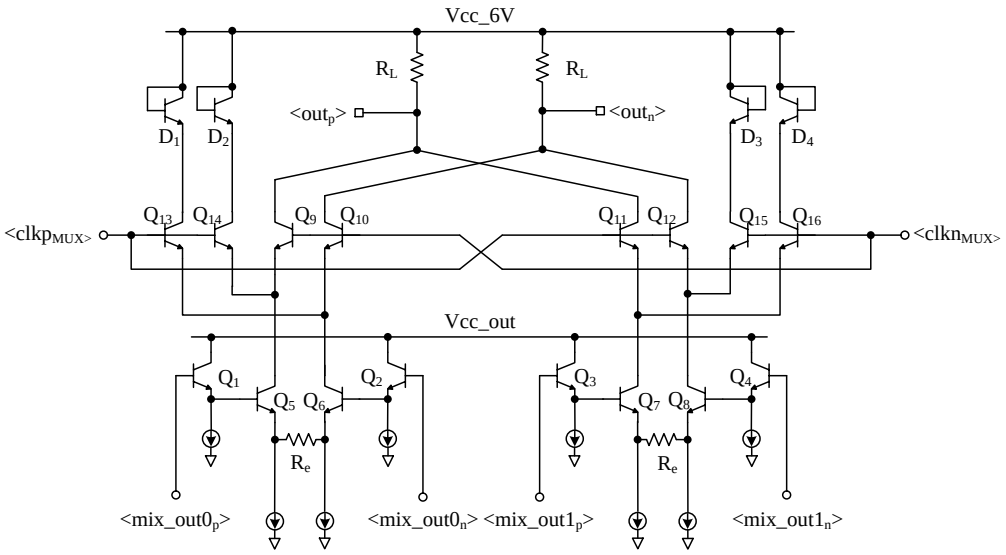


Figure 6.5: A simplified schematic of the implemented buffer amplifiers, MUX and output driver.

A chip photograph of the processed die is shown in Fig. 6.6. The optical CDN is located below the visible metal layers and therefore not visible, thus the location of the integrated Si-WGs is highlighted in the figure. The chip contains two identical 10 GS/s sampler units for the purpose of measuring jitter on the basis of time-domain correlation, as described in Chapter 7. The light from the fiber is coupled into the chip at the grating coupler and distributed by a 1x3 optical CDN to the samplers and to an additional PD for the purpose of optical path monitoring.
At the input, microstrip lines with a characteristic impedance $Z_L = 100\,\Omega$ are used to route the differential input signal from the contact pads symmetrically to the input buffer. The latter is placed close to the pads to minimize signal distortion due to transmission line effects.
The PD and the TIA are placed as close as possible to the switching transistors of the multiplier in the sampler core, thus eliminating any disposition to ringing along the electrical clock signal path.
The off-chip-generated clock signals clk_{DEMUX} and clk_{MUX} are routed symmetrically with differential microstrip lines ($Z_L = 100\,\Omega$).
Providing a maximum control of the operating conditions of the chip, the inputs of the current mirrors, which generate the bias currents of the circuits, are fed individually for the individual block components. The reference currents $I_{ref,input}$, $I_{ref,TIAX}$, $I_{ref,coreX}$, $I_{ref,resetX}$, and $I_{ref,outputX}$ ($X \in [0;1]$) corresponding to the input buffer, the TIAs, the sampler cores, the active reset circuits, and the output buffers are illustrated in Fig. 6.6.
The chip occupies an area of $A_{chip} = 2.2\,\text{mm} \times 2.2\,\text{mm}$, while each sampler dissipates an overall power of $P_{sampler} = 1.25\,\text{W}$ from a $Vcc = 6\,\text{V}$ power supply.

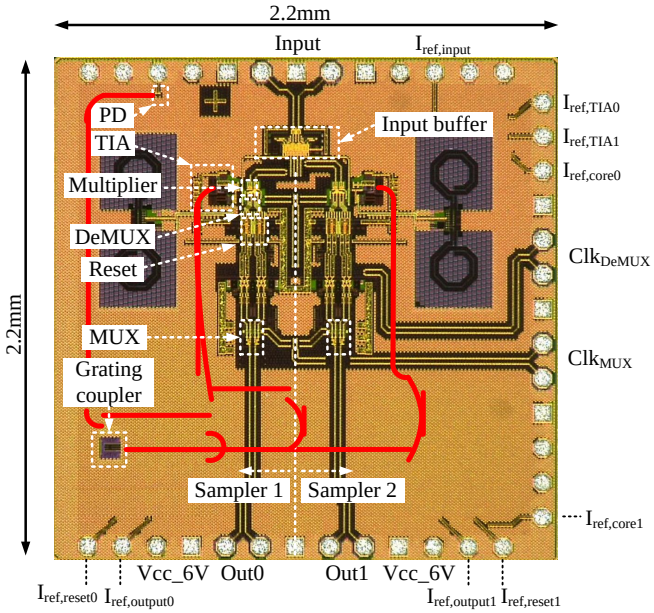


Figure 6.6: A chip photograph of the processed die, containing two identical 10 GS/s sampler units.

6.2 Experimental Results

6.2.1 Measurement Setup

The functionality of the implemented 10 GS/s sampler has been successfully verified by on-wafer measurements. A simplified block diagram of the test setup used for the characterization is shown in Fig. 6.7. For the sake of clarity, the power supply and the current mirror reference current sources are not shown in the figure. The optical signal path is the same as for the characterization of the O/E clock converter circuit (Fig. 5.6). Details can be found in Chapter 5.2.
The performance of the sampler is measured by applying a sinusoidal signal to the sampler input, digitizing the analog outputs of the sampler, and calculating the relevant parameters from the digital data stream.
A high-performance signal generator is used as signal source, which provides sinusoidal signals with a high spectral purity and frequency values up to $f_{in} = 40$ GHz [112].
For the digitizing the analog output signals of the samplers, a four-channel Real-Time Oscilloscope (RTO) with a sampling rate $f_{s,RTO} = 40$ GS/s for each channel, and an analog bandwidth

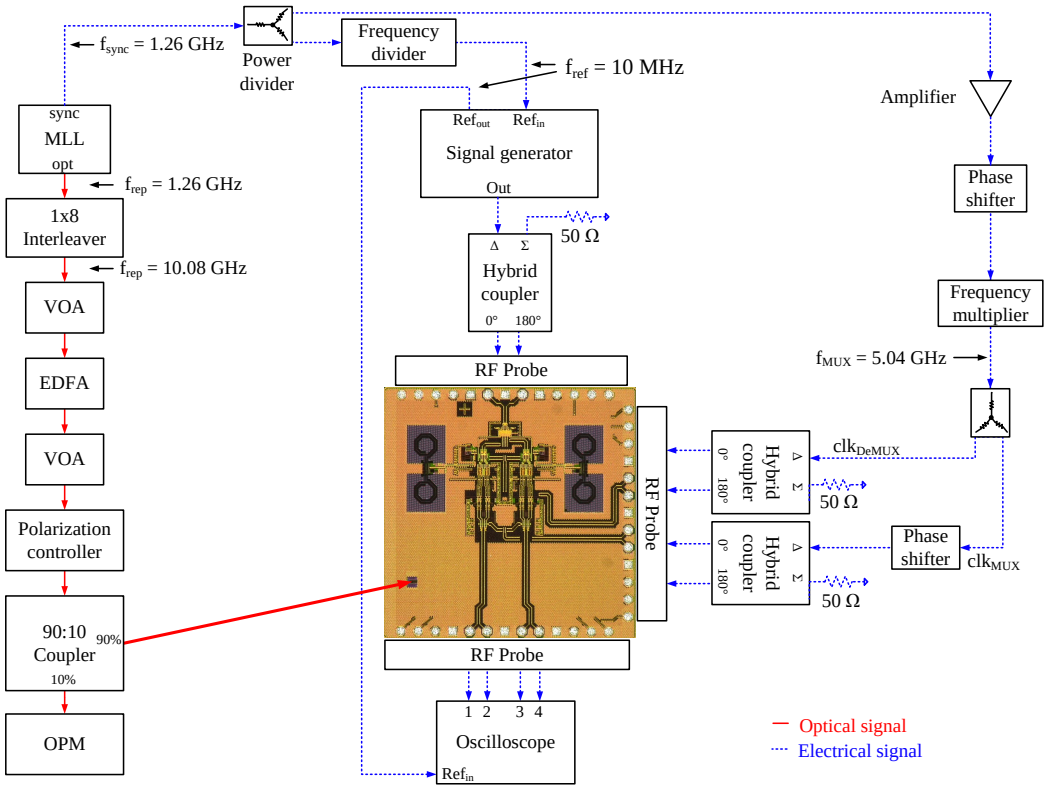


Figure 6.7: A simplified block diagram of the setup used for the characterization of the implemented 10 GS/s sampler.

of $f_{3dB} = 20\,\text{GHz}$ is used to acquire the single-ended analog outputs of the sampler [113]. Hybrid couplers used to perform the differential-to-single-ended-conversion were deliberately left out due to the phase matching problems mentioned in Chapter 5.2. Alternately, the two single-ended output signals are digitized individually, and the difference is calculated in the digital domain. This enables the possibility of a digital drift and mismatch correction, which improves the signal quality significantly.
For a proper sampler operation, it must be guaranteed that the clock signals driving the DEMUX and MUX must be perfectly synchronous to the optical clock. For this purpose, the electrical synchronization output of the MLL is used. It provides an electrical pulse train with a frequency $f_{sync} = 1.26\,\text{GHz}$, which is converted into a sinusoidal signal with $f_{MUX} = \frac{f_s}{2} = 5.04\,\text{GHz}$ using a frequency multiplier. Additional phase shifters are used to adjust the timing between the clock signals, while wideband 180° hybrid couplers [114] provide the differential signals.
A proper synchronization of the MLL, the signal generator, and the oscilloscope is mandatory to get correct measurement results. In other words, the drift between the individual clock signals must be small enough during the measurement time, such that it does not influence the measured performance. For this purpose, the clock signals are synchronized using the electrical reference output of the MLL. It is divided by a factor of 125 to ensure the compatibility with the available $f_{ref} = 10\,\text{MHz}$ reference inputs of the signal generator and the oscilloscope.

Fig. 6.8 illustrates a photograph of the measurement setup used for the characterization of the implemented 10 GS/s sampler. Except for the power supplies providing the supply voltages and reference currents, the measurement components are installed on an optical table with an active pneumatic isolation to minimize the impact of vibrations.
The test chip is attached on a probing station, which features a high-resolution microscope for a proper adjustment of the fiber and the electrical probe heads using micromanipulators.
Due to the complexity of the setup, the measurement is automatized as much as possible. Therefore, a Matlab-based plug-in developed by R&S is used to control the measurement devices, and acquire the digital data as well as additional information, such as internal node voltages and currents, average photocurrent at the output of the monitoring path, to ensure that the chip is working properly during the measurement.

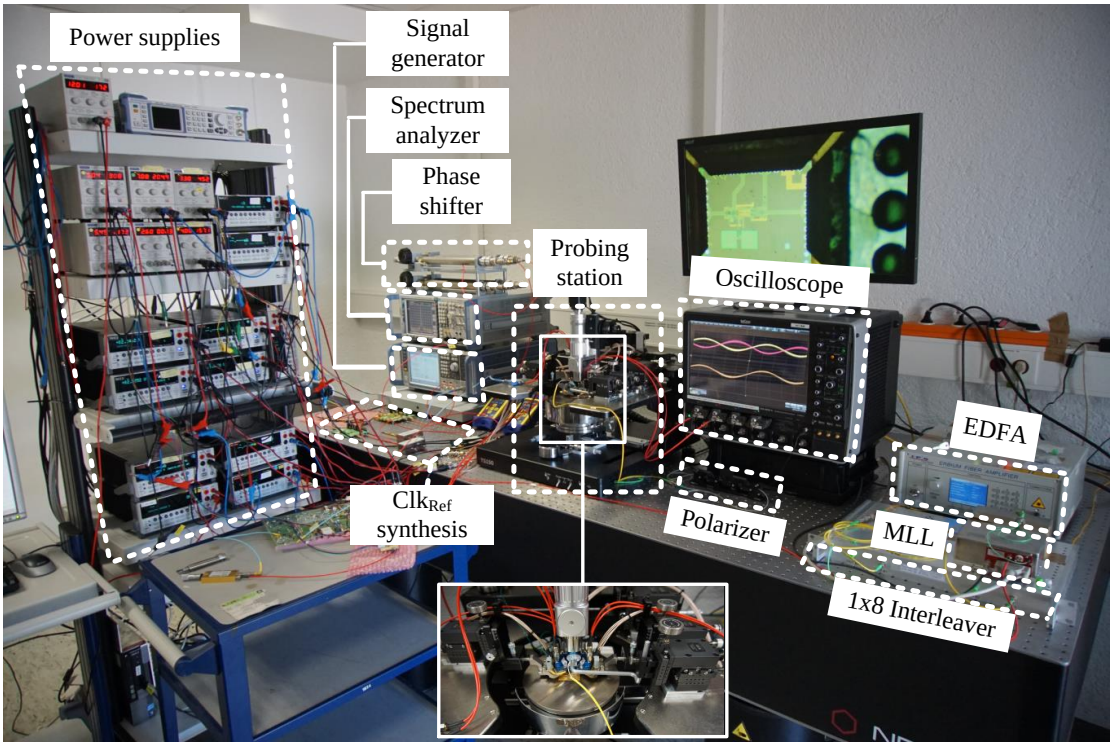


Figure 6.8: A photograph of the measurement setup used for the characterization of the implemented 10 GS/s sampler.

6.2.2 Measurement Results

At first the functionality of the sampler is verified by applying a sinusoidal signal with a frequency

$$f_{in} = \frac{k}{l} \cdot f_s, \tag{6.4}$$

where k,l$\in \mathbb{N}$, to the input of the sampler. As a consequence of the sampling operation, a periodic signal with a period of l samples is obtained at the output of the sampler.
Fig. 6.9 a) illustrates the raw 40 GS/s digital data stream from the RTO obtained from the two single-ended outputs of the sampler as response to a sinusoidal input signal with a frequency $f_{in} = \frac{8001}{8000} \cdot 10.08\,\text{GHz} = 10.08126\,\text{GHz}$. As the input signal frequency is above the Nyquist frequency $\frac{f_s}{2} = 5.04\,\text{GHz}$, it is folded into the first Nyquist zone, and the alias frequency f_{alias} at the output of the sampler is given by

$$f_{alias} = \left| f_{in} - k \cdot \frac{f_s}{2} \right|, \tag{6.5}$$

where $k \in \mathbb{N}$ is chosen such that $f_{alias} < \frac{f_s}{2}$. With the values given above, an alias frequency of $f_{alias} = 1.26\,\text{MHz}$ with a corresponding period of $t_p = 0.8\,\mu\text{s}$ is expected at the sampler output. This matches good with the measurement results from Fig. 6.9.
The differential output, which is used for the further investigation of the sampler performance, is shown in Fig. 6.9 b). It is calculated from the single-ended outputs by subtracting the two single-ended signals in the digital domain.

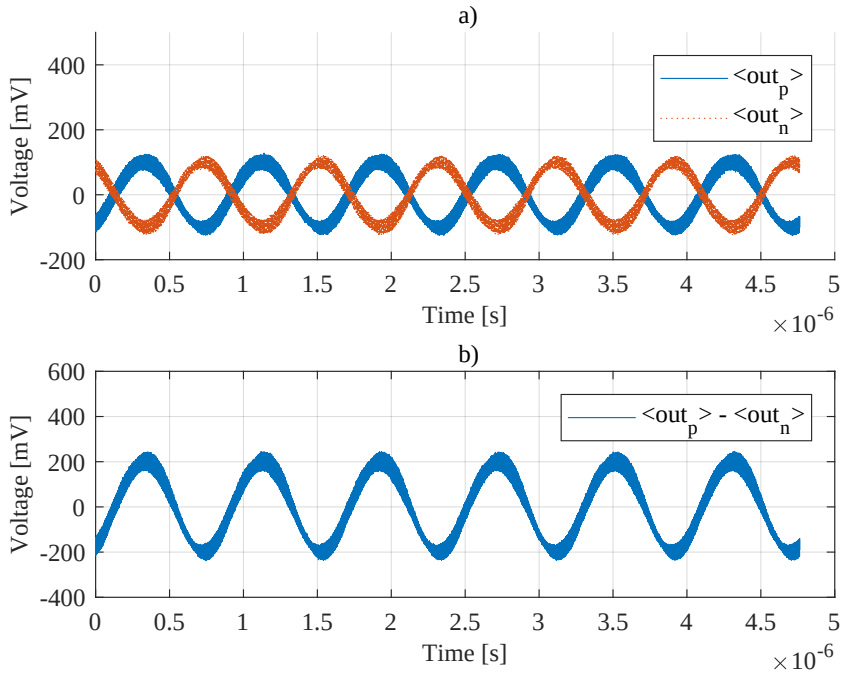


Figure 6.9: a) Measured variation in time of the voltage at the two single-ended outputs of the 10.08 GS/s sampler as response to a sinusoidal input signal with a frequency of $f_{in} = 10.08126\,\text{GHz}$, digitized with a RTO with $f_{s,RTO} = 40\,\text{GS/s}$. b) The difference of these single-ended signals, which represents the actually wanted differential signal.

The spectrum calculated from the differential output is shown in Fig. 6.10. It consists of the fundamental at a frequency $f_{alias} = 1.26\,\text{MHz}$, and spurs at integer multiples of the MLL fundamental frequency $f_{rep} = 1.26\,\text{GHz}$. As mentioned in Chapter 3, these spurs originate from a timing skew and an amplitude mismatch of the optical 1x8 interleaver. An amplitude mismatch of the optical pulses in the range of ±5 %, as shown in Fig. 5.8 a), corresponds to a sampler gain mismatch in the same order. According to Eq. 2.20, this yields to TNHD = 26.6 dB, which matches very well with the results from the measurement. With respect to the target 80 GS/s TI ADC application, it is worth noting that each 10 GS/s sampler unit is receiving all of the subsequent pulses. Therefore, it is not possible to calibrate these spurs in the analog domain.

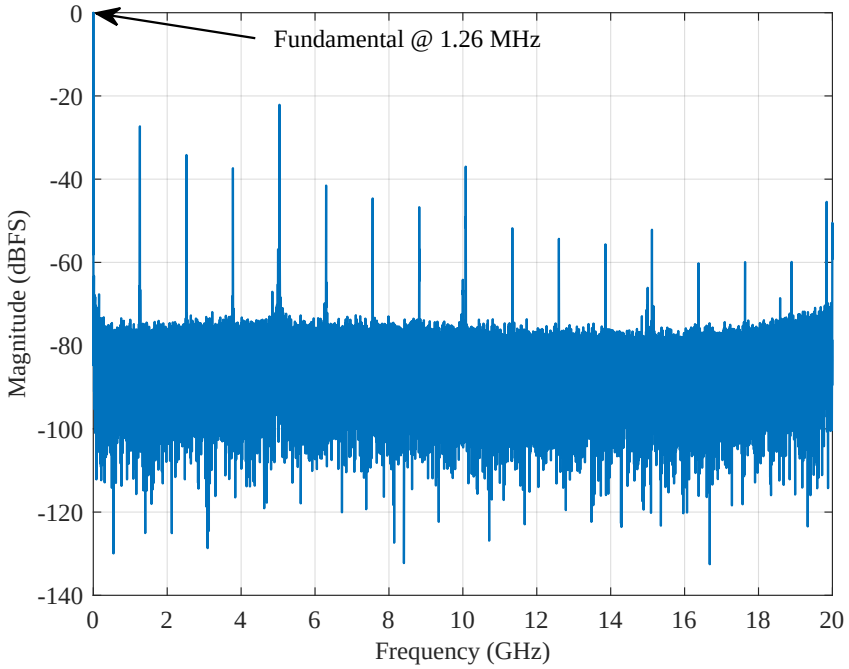


Figure 6.10: Corresponding spectrum calculated from the signal shown in Fig. 6.9 b).

Regarding the quality of the signal, it turned out that operating the sampler at its full sample rate $f_s = 10.08\,\text{GHz}$ results in a significant degradation of the SNR of the reconstructed signal. Even for low input frequency values, a poor value of only $\text{SNR}_{\text{meas}} = 25\,\text{dB}$ was measured, which does not match to a simulated value of $\text{SNR}_{\text{sim}} = 40\,\text{dB}$. The excess of noise arises from coprime sampling rates of the MLL and the RTO, which results in a drift of the sampling instant in the digitizing process. Assuming that the held output signals of the sampler would be perfectly flat in the hold phase, this drift would not affect the performance of the digital signal. But since the analog output signals of the sampler also include the transition between adjacent samples and therefore intersymbol interference, a drift of the sampling instant corresponds to a non-uniform sampling, which results in an additional noise component.

Reliable tests of sampler performance are indeed achieved by operating it a reduced sampling rate equal to the MLL fundamental frequency $f_{\text{rep}} = 1.26\,\text{GHz}$. Maintaining the optical pulse energy applied to the PD constant, the performance of the sampler is not affected. Increasing the sampler hold time enables a partial correction of the aforementioned drift in the digital domain. As a result, the SNR was significantly increased to $\text{SNR} = 34.1\,\text{dB}$, respectively $\text{SNR} = 35.3\,\text{dB}$ when the specified noise contribution of the RTO is taken into account.

Another possible noise source is the imperfect stability of the optical coupling. Although the measurement setup was optimized to provide a maximum mechanical stability, it turned out that the

efficiency of the optical coupling is not constant over the time. Since the gain of the sampler is directly proportional to the optical power applied to the PD, it can be considered as a gain modulation, which results in an additional noise component, and further investigations are necessary to clarify this influence.

From the calculated spectrum, the harmonic distortions can be determined. Fig. 6.11 shows the harmonic distortions THD, HD2 and HD3 as a function of the input frequency f_{in} using an optical pulse energy of $E_p = 175\,fJ$. Hereby, HD2 and HD3 is defined as the ratio of the power of the second, respectively third harmonic to the fundamental signal power according to Eq. 2.17. A THD $< -33\,dB$[1] over the entire bandwidth can be observed. It is dominated by the HD2, which is unusual for a fully differential topology. Presumably, imperfections in the measurement setup are the reason for that, and this phenomenon needs to be further investigated. Regarding the third harmonic, a HD3 $< -41\,dB$ over the entire bandwidth does not meet the specification, but it is a good starting point for a future optimization.

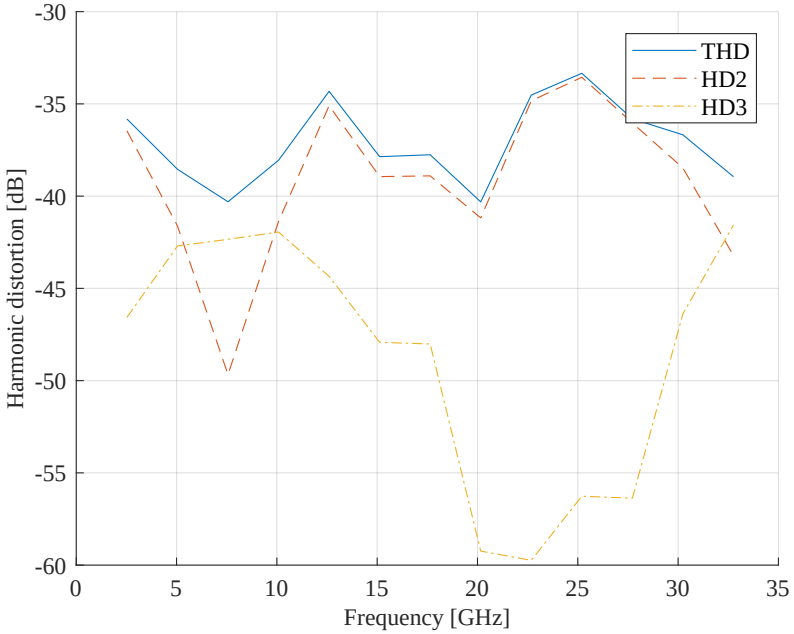


Figure 6.11: Harmonic distortions THD, HD2 and HD3 as a function of the input frequency for an optical pulse energy of $E_p = 175\,fJ$.

At next, the frequency response of the sampler is determined by estimating the amplitude of the sampled signals for different input signal frequency values. Before the actual measurement was performed, a calibration of the input and the output is necessary to minimize the influence of the measurement setup on the results.

[1] $N_{harm} = 9$

Regarding the analog input, the frequency response from the single-ended output of the signal generator to the differential probe tips connected to the contact pads is measured separately using an Open-Short-Load calibration [115]. In order to apply the same power to the sampler input for all frequencies, the signal power provided by the signal generator is adjusted reciprocal to the measured frequency response of the setup.
At the sampler output, an alternative calibration is proposed. According to Eq. 6.5, input signals with a frequency above the Nyquist frequency are aliased into the first Nyquist zone. As the frequency range of interest from DC to 40 GHz spans 8 Nyquist zones, the input frequency values are chosen such that they are folded back to the same alias frequency. As a consequence, the influence of the signal path at the output of the sampler affects all measurements in the same way. Tolerating a constant gain error due to the attenuation of the output signal path, a calibration of the output is not necessary.

Fig. 6.12 illustrates the measured frequency response of the sampler for an optical pulse energy of $E_p = 175\,\mathrm{fJ}$. It has a bandwidth $f_{3dB} = 31\,\mathrm{GHz}$ and a low-frequency gain of $g_{sampler} = -8.5\,\mathrm{dB}$.

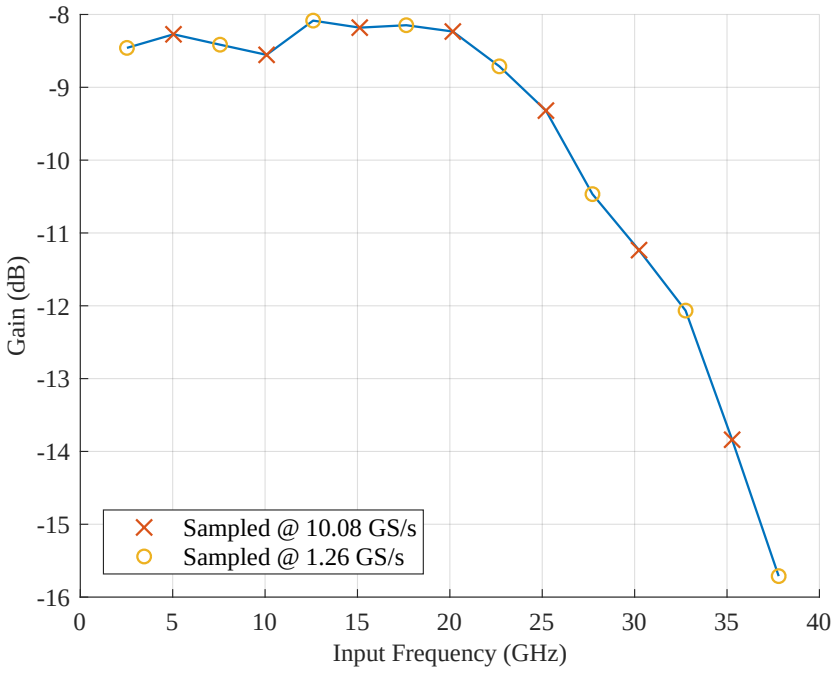


Figure 6.12: Measured gain as function of the input frequency of the implemented 10 GS/s sampler core for an optical pulse energy of $E_p = 175\,\mathrm{fJ}$. Additional data points are obtained operating the sampler with a reduced sampling rate $f_s = 1.26\,\mathrm{GS/s}$.

Herein, the gain is defined as the logarithmic power ratio of the sampler output voltage $\hat{v}_{out}$ and the specified input signal amplitude $\hat{v}_{in} = 500\,\mathrm{mV}$ applied to the input of the sampler:

$$g_{sampler} = 20 \cdot \log_{10}\left(\frac{\hat{v}_{out}}{\hat{v}_{in}}\right) \tag{6.6}$$

Since the frequency of the input signal is known, the amplitude $\hat{v}_{out}$ can be calculated by calculating the magnitude of the Fourier coefficient corresponding to the alias frequency f_{alias}:

$$\hat{v}_{out} = \left| \frac{2}{N_{snmp}} \cdot \sum_{k=1}^{N_{snmp}} e^{-j\cdot 2\cdot \pi \cdot f_{alias} \cdot t} \cdot v_{out}(k \cdot T_s) \right| \tag{6.7}$$

Since the number of alias frequencies in a certain bandwidth depends on the sampling rate, a finer resolution is obtained by taking additional measurements at a sample rate equal to the MLL fundamental $f_s = 1.26\,\mathrm{GS/s}$. Regarding the measurement setup, the output signal of the MLL is directly used without the optical 1x8 interleaver, and a frequency-divider-by-two is used in the generation of the DEMUX respectively MUX clock signals instead of the frequency multiplier shown in Fig. 6.7.

In Fig. 6.13, the measured 3 dB-bandwidth (solid line) and the sampler gain (dashed line) are shown as a function of the optical pulse energy. Increasing the optical pulse energy from $E_p = 140\,\mathrm{fJ}$ to 210 fJ increases the sampler gain from $g_{sampler} = -11.5\,\mathrm{dB}$ to $-8\,\mathrm{dB}$. For pulse energy values $E_p < 195\,\mathrm{fJ}$, the expected quadratic dependency of the sampler gain and the pulse energy can be observed. For higher pulse energy values, a lower gain indicates a saturation of the PD.
Regarding the 3 dB-bandwidth, a decrease from $f_{3dB} = 35.8\,\mathrm{GHz}$ to 23.5 GHz can be observed. For pulse energy values $E_p < 180\,\mathrm{fJ}$, the shape of the electrical clock signal is mainly determined by the waveform of the photocurrent. Therefore, the results obtained in Fig. 6.13 can be used to qualitatively appreciate the large-signal behavior of the PD. It seems that the photocurrent pulse width is increasing for higher pulse energy values, which was also observed for the first generation of PDs as shown in Fig. 5.9.
For pulse energy values $E_p > 180\,\mathrm{fJ}$, an additional pulse widening arise from inappropriate biasing of Q_1 in the clock generator circuit in Fig. 6.3 and the observed saturation of the PD.

Table 5.1 summarizes the performance of the implemented 10 GS/s sampler core unit.

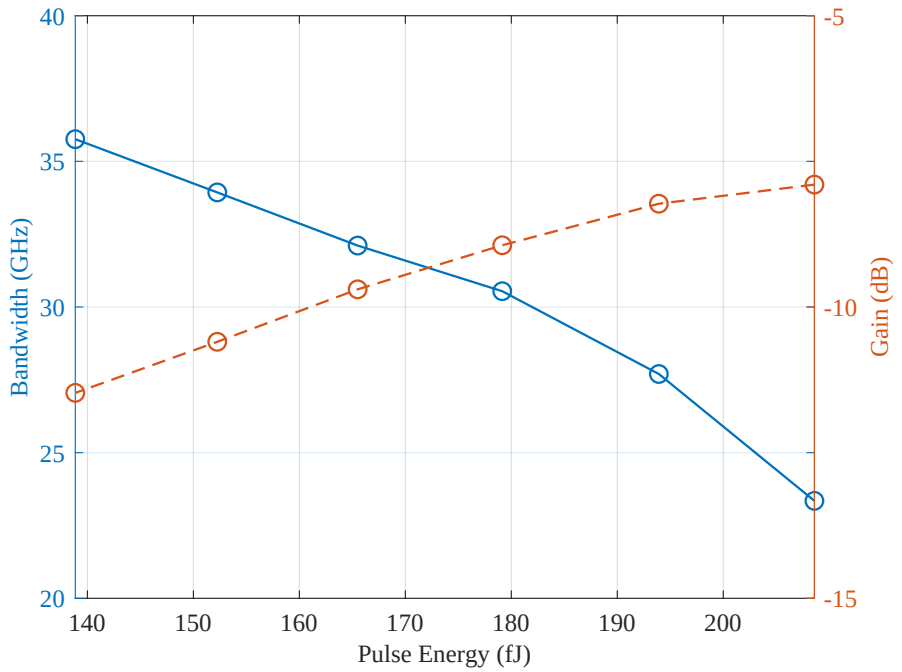


Figure 6.13: Calculated 3 dB-bandwidth (solid line) and gain (dashed line) of the sampler as a function of the optical pulse energy.

Sampling rate	$f_s = 10\,\mathrm{GS/s}$
Optical pulse energy at the PD input	$140\,\mathrm{fJ} \leq E_P \leq 210\,\mathrm{fJ}$
Gain	$-11.5\,\mathrm{dB} \leq g_{sampler} \leq -8\,\mathrm{dB}$
Bandwidth	$35.8\,\mathrm{GHz} \geq f_{3dB} \geq 23.5\,\mathrm{GHz}$
Noise ($E_P = 175\,\mathrm{fJ}$, f_{in}=10.08 GHz)	SNR = 35.3 dB
In-band harmonic distortions ($E_P = 175\,\mathrm{fJ}$)	THD < -33 dB HD3 < -41 dB
Jitter ($E_P = 175\,\mathrm{fJ}$)	$\sigma_t \leq 28$ fs (see Chapter 7.6)
Sampler core area	$A_{sampler} = 1.1$ mm x 1.75 mm
Power consumption per sampler	$P_{sampler} = 1.25$ W

Table 6.1: Performance summary of the implemented 10 GS/s sampler core.

7 Development of a Reliable Method for the Characterization of Ultra-Low Sampler Jitter

The measurement of sampler jitter in the expected range of a few femtoseconds turned out to be extremely challenging. An intensive literature research showed that the proposed techniques were not suitable for this ambitious task, so a novel method for the characterization of ultra-low sampler jitter was developed. In Chapter 2.3.5, the fundamental properties of jitter-induced noise were presented. Based on these properties, a cyclostationary stochastic approach is derived to extract the jitter-induced noise from other noise sources in the measurement setup. A further investigation of these error sources provides effective techniques for their compensation when possible, or at least an estimation of their influence on the accuracy of the measurement.
The consistency of the developed approach is experimentally demonstrated by measuring jitter of an electrical high-end 10 GS/s sampler in the range of $\sigma_t = 20$ fs. This packaged, product-ready chip developed by R&S in combination with a qualified testboard enables a long-term stable measurement setup with the best conditions for the challenging measurement.
Finally the measurement results of the implemented photonic-assisted 10 GS/s sampler are presented.

7.1 State of the Art in Jitter Measurement

In Chapter 5.2, the jitter of the O/E clock converter output signal - as clock signal for a sampler - is determined in the frequency domain by integrating the measured phase noise for the frequency range of interest. Although this method allows to determine very low jitter values of a clock signal precisely, it is not suitable for measuring the intrinsic jitter of the sampler.
For this purpose, the sampler must be a part of the measurement setup, and various methods for measuring the jitter in the time domain were developed [116], [117], [118], [119], [120], [121], [122], [123]. The basic idea of all these methods is to sample and to digitize a signal with a well-defined shape, and extract the noise induced by the jitter amongst other noise sources.
Fig. 7.1 illustrates a simple measurement setup for the characterization of the intrinsic sampler jitter in the time-domain. A sinusoidal input signal with the frequency f_{in} according to Eq. 6.4 is applied to the input of the sampler. Its analog output is converted to the digital domain with a waveform recorder, for example a high-resolution sampling oscilloscope or a RTO. From the digital data stream,

the jitter-related noise needs to be separated from other noise sources in the measurement setup.

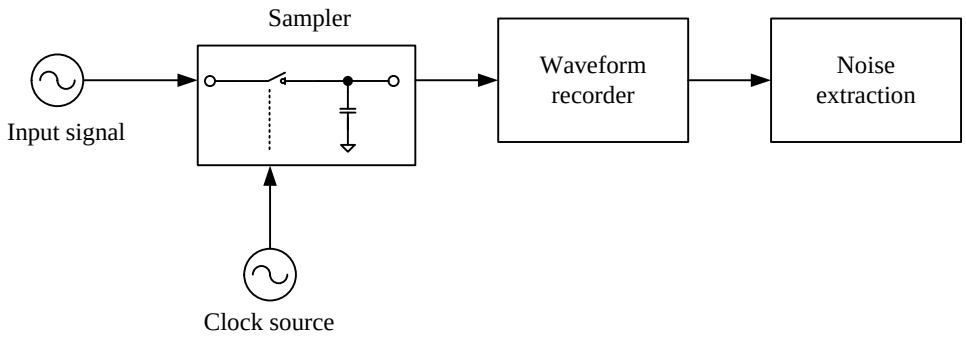


Figure 7.1: A simple measurement setup for the characterization of the intrinsic sampler jitter in the time-domain.

Simple methods exploit the dependency of the jitter-induced noise $\sigma^2_{\mathrm{v,rms}}$ on the amplitude or frequency in Eq. 2.31 by measuring the noise floor observed by spectral averaging [116]. Since $\sigma^2_{\mathrm{v,rms}}$ does not only contain jitter-induced noise, but also non-jitter-related noise components, this method is very sensitive to errors induced by the measurement setup.

More advanced techniques exploit the unique characteristic of jitter-induced noise according to Eq. 2.29, instead of dealing with the averaged $\sigma^2_{\mathrm{v,rms}}$. In [117], a double-beat and subtraction technique is proposed, whereby the noise is evaluated at different phases, respectively different slopes of the sinusoidal signal. Further improvement of the sensitivity was achieved by reducing the impact of the measurement setup. In effect, jitter from signal generators in the measurement setup has been eliminated by a time-domain correlation using a two-channel measurement [117], [118]. Furthermore, statistical methods were proposed to remove limitations introduced by quantization noise and ADC nonlinearities [119], [120].

Despite all these efforts, the lowest reported jitter values are in the range of 100 femtoseconds [121], [122], while the highest reported measurement accuracy is 50 femtoseconds for a jitter value $\sigma_{\mathrm{t}} = 300\,\mathrm{fs}$ [120]. In addition, the statistical properties of the results are either unclear or difficult to investigate. Since the jitter of the photonic-assisted sampler is expected in the range of a few femtoseconds, a novel measurement method was developed with the goal to improve the sensitivity and the accuracy significantly.

7.2 Cyclostationary, Stochastic Approach

Recalling from Chapter 2.3.5, the stationary random process J_t is mapped onto the cyclostationary random process J_v by sampling a periodic input signal $v(t)$. Assuming that all parameters of this mapping are known, it is possible to calculate the properties of the process J_t from those observed in the process J_v.
Dealing with a cyclostationary random process, all samples obtained from the output of the sampler are sorted by their corresponding phase ϕ upfront. This is possible because the frequency f_{in} of the signal is known, so a phase ϕ can be assigned to each sample. If the signal acquisition is done properly, a number of samples N_{smp} is uniquely allocated to a number of phases N_{ph}, respectively. At next, the cyclostationary variances $\sigma_v^2(\phi)$ are estimated by

$$\widehat{\sigma_v^2}(\phi) = \frac{1}{N_{smp} - 1} \sum_{i=1}^{N_{smp}} \left(x_{i,\phi} - \widehat{\mu_v}(\phi) \right)^2 , \tag{7.1}$$

where $x_{i,\phi}$ denotes the samples corresponding to a certain phase ϕ and $\hat{\mu_v}(\phi)$ denotes the estimated mean:

$$\widehat{\mu_v}(\phi) = \frac{1}{N_{smp}} \sum_{i=1}^{N_{smp}} x_{i,\phi}. \tag{7.2}$$

Recalling from Eq. 2.3.5, the ideal jitter-induced cyclostationary variance $\sigma_v^2(\phi)$ of a sinusoidal input signal has a specific $\cos(2 \cdot \phi)$-shape, so it is sufficient to calculate the Fourier coefficient $\widehat{\sigma_{v,fit}^2}$ for $\cos(2 \cdot \phi)$ of $\widehat{\sigma_v^2}(\phi)$:

$$\widehat{\sigma_{v,fit}^2} = \frac{1}{\pi} \int_0^{2 \cdot \pi} \widehat{\sigma_v^2}(\phi) \cdot \cos(2 \cdot \phi) \mathrm{d}\phi. \tag{7.3}$$

The estimated jitter $\widehat{\sigma_t}$ can now be deduced from Eq. 2.29 and is given by

$$\widehat{\sigma_t} = \frac{1}{2 \cdot \pi \cdot f_{in} \cdot \hat{v}} \cdot \sqrt{2 \cdot \widehat{\sigma_{v,fit}^2}}. \tag{7.4}$$

Fig. 7.2 illustrates these basic relationships on the example of a noisy jitter-related variance $\widehat{\sigma_v^2}(\phi)$, the jitter-sensitive fit function, and the corresponding amplitude $\widehat{\sigma_{v,fit}^2}$, from which $\hat{\sigma}_t$ is obtained.

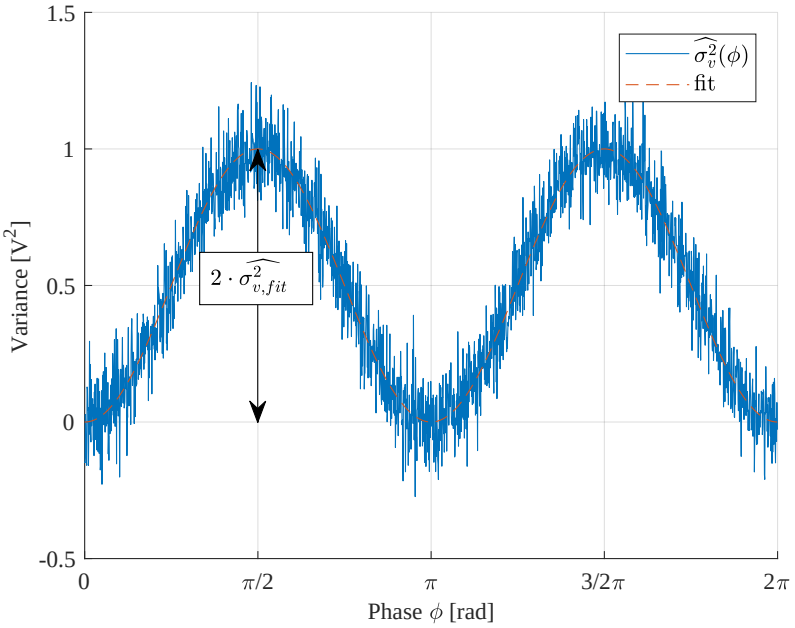


Figure 7.2: Noisy jitter-related cyclostationary variance $\widehat{\sigma_{\mathrm{v}}^2}(\phi)$ obtained from a measurement (solid line), the jitter-sensitive fit function (dashed line), and the corresponding amplitude $\widehat{\sigma_{\mathrm{v,fit}}^2}$ to calculate the estimated jitter $\hat{\sigma}_{\mathrm{t}}$.

7.3 Measurement Accuracy and Error Sources

In a practical measurement, the cyclostationary variance $\sigma_v^2(\phi)$ is composed of additional noise components originating from the measurement setup. Therefore, $\sigma_v^2(\phi)$ can be rewritten as:

$$\sigma_{\mathrm{v}}^2(\phi) = \underbrace{(\sigma_{\mathrm{Nj}}^2 + \sigma_{\mathrm{Nj,ext}}^2) \cdot \cos^2(\phi)}_{\sigma_{\mathrm{Nj,tot}}^2(\phi)} + \sigma_{\mathrm{Nc}}^2(\phi) + \sigma_{\mathrm{Ns}}^2. \tag{7.5}$$

In Eq. 7.5, non-sampler-related jitter $\sigma_{\mathrm{t,ext}}$, is represented by the corresponding $\sigma_{\mathrm{N,j,ext}}$ according to Eq. 2.30. Non-jitter-related components can be split into a stationary part σ_{Ns}^2, and a cyclostationary part $\sigma_{\mathrm{Nc}}^2(\phi)$. One possible example of noise composition is shown in Fig. 7.3. Herein, the stationary variance σ_{Ns}^2 is modeled as a random variable to illustrate its noisy character of the measurement, while the other variances are modeled ideally.
In the following, the influence of the individual contributors on the accuracy and the sensitivity of the jitter measurement are investigated in detail.

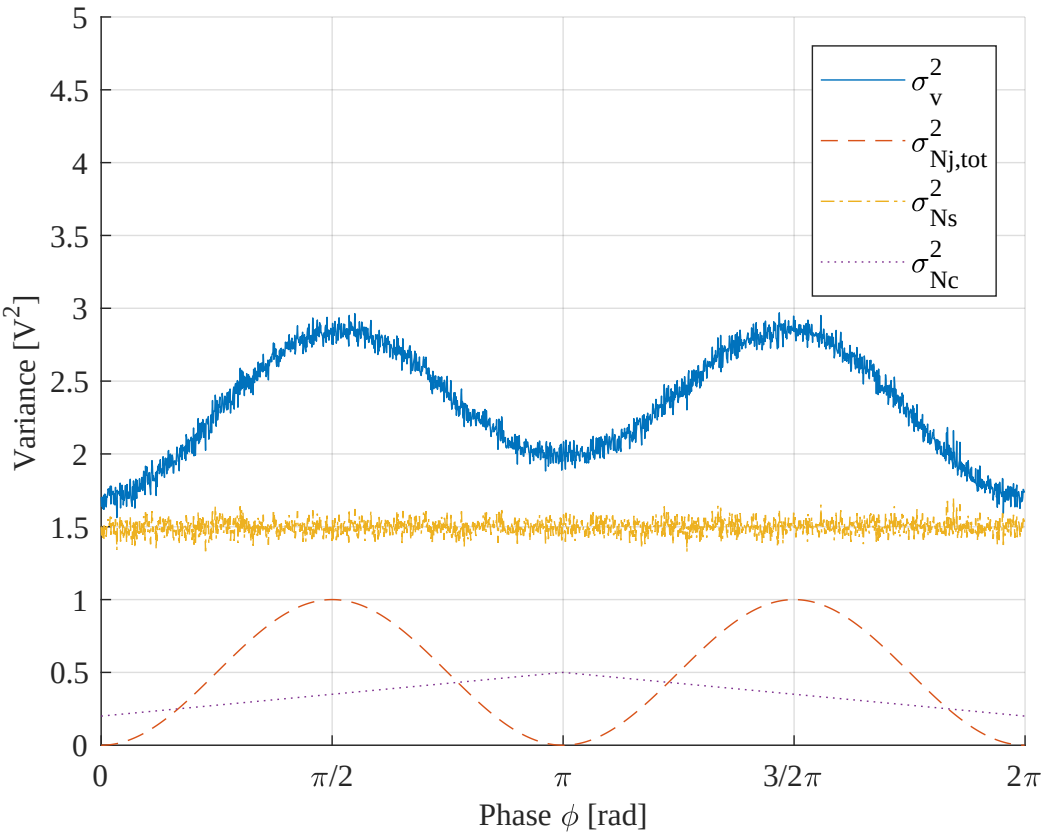


Figure 7.3: Noise contribution to the overall $\sigma_v^2(\phi)$ (solid line) on the example of a noisy stationary variance σ_{Ns}^2 (dash-dot line), a triangular-shaped cyclostationary variance $\sigma_{Nc}^2(\phi)$ (dotted line), and the jitter-related noise $\sigma_{Nj,tot}^2(\phi)$ (dashed line).

7.3.1 Stationary Noise

The presence of stationary noise σ_{Ns}^2 limits the accuracy of the jitter measurement. Considering the major time effort for completing a measurement, it is desirable to a priori determine the number of samples required, such that a certain accuracy is met with a given probability. A detailed stochastic analysis of the accuracy is given in [124], and a formula to calculate the minimum number of samples N_{min} is derived.

Assuming a jitter in the expected range $[\sigma_{tmin}, \sigma_{tmax}]$ with a sinusoidal signal with an amplitude A and a frequency f_{in}, the minimum number of samples N_{min} is calculated as [124]:

$$N_{min} = \frac{\frac{7}{16} \cdot \sigma_{Njmax}^4 + \sigma_{Njmax}^2 \cdot \sigma_{Ns}^2 + \sigma_{Ns}^4}{\left(\frac{\sigma_{\dot{\sigma}_{tmax}}}{2} \cdot (2 \cdot \pi \cdot f_{in} \cdot \hat{v})^2 \cdot \sigma_{tmin}\right)^2}, \tag{7.6}$$

where $\sigma_{\hat{\sigma}_{\mathrm{tmax}}}$ is the maximum allowed standard deviation of the calculated jitter.
Assuming a well-known jitter of the device-under-test ($\sigma_{\mathrm{tmin}} = \sigma_{\mathrm{tmax}} = \sigma_{\mathrm{t}}$), Eq. 7.6 can be simplified to

$$N_{\mathrm{min}} = \frac{4 \cdot \left(\frac{7}{16} + \frac{\sigma_{\mathrm{Ns}}^2}{\sigma_{\mathrm{Nj}}^2} + \frac{\sigma_{\mathrm{Ns}}^4}{\sigma_{\mathrm{Nj}}^4} \right)}{\epsilon^2}, \tag{7.7}$$

with

$$\epsilon = \frac{\sigma_{\sigma_{\mathrm{tmax}}}}{\sigma_{\mathrm{t}}}. \tag{7.8}$$

From Eq. 7.7, it can be seen that the required minimum number of samples strongly depends on the ratio $\frac{\sigma_{\mathrm{Ns}}^2}{\sigma_{\mathrm{Nj}}^2}$. On the one hand, it can be lowered using a high signal frequency $\mathrm{f_{in}}$, which corresponds to a large σ_{Nj}^2. But this measure is limited by the sampler bandwidth, since an attenuation of the signal amplitude for input frequency values near and above $\mathrm{f_{3dB}}$ will result in an reduced slope and therefore a decrease of σ_{Nj}^2. On the other hand, the stationary noise, represented by σ_{Ns}^2, needs to be reduced as much as possible.

7.3.2 Cyclostationary Noise

Experiments have shown that jitter originating in the clock path of the waveform recorder induces an additional frequency-invariant, cyclostationary noise component, which lowers the overall sensitivity of the proposed method. This can be easily understood when the analog output signal of the sampler is not regarded as an ideal staircase signal with zero-slope in the hold phase, but as a true analog signal, including transient effects, voltage droop, etc. As a consequence, an aperture uncertainty of the waveform recorder clock signal will induce an error, whose phase-dependent characteristic strongly depends on the actual waveform of the signal.
This kind of noise is represented by $\sigma_{\mathrm{Ncfi}}^2(\phi)$, whereas the frequency-variant, non-stationary noise is represented by $\sigma_{\mathrm{Ncfv}}^2(\phi)$ such that

$$\sigma_{\mathrm{Nc}}^2(\phi) = \sigma_{\mathrm{Ncfi}}^2(\phi) + \sigma_{\mathrm{Ncfv}}^2(\phi). \tag{7.9}$$

The frequency-differential method is an extension to the method already outlined so far. Two measurements at different frequencies, $\mathrm{f_1}$ and $\mathrm{f_2}$, are conducted and processed as outlined before. Hence two corresponding cyclostationary variances $\sigma_{\mathrm{v},1}^2(\phi)$ and $\sigma_{\mathrm{v},2}^2(\phi)$ according to Eq. 7.5 are obtained. Cyclostationary, non- jitter-related, frequency-invariant noise $\sigma_{\mathrm{Ncfi}}^2(\phi)$ can now be eliminated by taking

the difference of these variances to obtain $\Delta\sigma_{\mathrm{v}}^2(\phi)$:

$$\begin{aligned}\Delta\sigma_{v}^2(\phi) &= \sigma_{\mathrm{v},1}^2(\phi) - \sigma_{\mathrm{v},2}^2(\phi) \\ &= \sigma_t^2 \cdot (2\cdot\pi)^2 \left(\mathrm{f}_1^2 - \mathrm{f}_2^2\right) \left(\frac{\mathrm{dv}(\phi)}{\mathrm{d}\phi}\right)^2 + \sigma_{\mathrm{Ncfv1}}^2(\phi) - \sigma_{\mathrm{Ncfv2}}^2(\phi) + \sigma_{\mathrm{Ns1}}^2 - \sigma_{\mathrm{Ns2}}^2.\end{aligned} \tag{7.10}$$

The amplitude of the signal must be the same in both measurements, such that $\left(\frac{\mathrm{dv}(\phi)}{\mathrm{d}\phi}\right)^2$ is the same for both. This is achieved by proper calibration and eliminates $\sigma_{\mathrm{Ncfi}}^2(\phi)$, as it is the same for both measurements. If σ_{Ns1}^2 and σ_{Ns2}^2 have similar values, they may cancel out as well, but this is not a requirement since it does not affect the jitter-sensitive fit (Eq. 7.3).
Regarding $\sigma_{\mathrm{Ncfv1}}^2(\phi)$ and $\sigma_{\mathrm{Ncfv2}}^2(\phi)$, it must either be ensured that these components are the same, or have a phase dependency different from $\cos(2\cdot\phi)$. This is achieved by choosing f_1 as image frequency of f_2 according to the sampling frequency f_s:

$$\mathrm{f}_1 = |\pm \mathrm{f}_2 \pm \mathrm{k}\cdot \mathrm{f}_\mathrm{s}|, \tag{7.11}$$

with $k \in \mathbb{N}$. In this case, the signal at the sampler output is the same for both input frequencies, and therefore the noise induced by jitter of the waveform recorder.
The calculated variance $\Delta\sigma_{\mathrm{v}}^2(\phi)$ is henceforth processed as outlined before. Once the jitter-sensitive fit parameter $\widehat{\Delta\sigma_{\mathrm{v,fit}}^2}$ is determined, the estimated jitter $\widehat{\sigma_\mathrm{t}}$ is calculated in a similar way as in Eq. 7.4:

$$\widehat{\sigma_\mathrm{t}} = \frac{1}{2\cdot\pi\cdot A}\sqrt{\frac{2\cdot\widehat{\Delta\sigma_{v,\mathrm{fit}}^2}}{(\mathrm{f}_1^2 - \mathrm{f}_2^2)}}. \tag{7.12}$$

Using the frequency-differential approach does also affect $\mathrm{N}_{\mathrm{min}}$ [124]. Measuring at two frequencies f_1 and f_2 with a common amplitude A, the minimum number of samples for the frequency-differential approach N_{FD} is given by [124]

$$N_{\mathrm{FD}} = \frac{\frac{7}{32}\cdot\frac{\left(\sigma_{\mathrm{Nj1max}}^4+\sigma_{\mathrm{Nj2max}}^4\right)}{\sigma_{\mathrm{Ns}}^4} + \frac{\left(\sigma_{\mathrm{Nj1max}}^2+\sigma_{\mathrm{Nj2max}}^2\right)}{2\cdot\sigma_{\mathrm{Ns}}^2} + 1}{\left(\frac{\sigma_{\hat{\sigma}_{\mathrm{tmax}}}}{2}\cdot(2\cdot\pi\cdot A)^2\left(f_1^2 - f_2^2\right)\cdot\sigma_{t\mathrm{min}}\right)^2}, \tag{7.13}$$

where σ_{Nj1max}, σ_{Nj2max} are calculated according to Eq. (2.30).

7.3.3 Generator Jitter

Jitter induced by clock and input signal generator, $\sigma_{\mathrm{Nj,clk}}$ respectively $\sigma_{\mathrm{Nj,gen}}$, is usually much larger than the intrinsic sampler jitter. This jitter can be eliminated with a dual-channel measurement as proposed in [117], [119]. Herein, the input signal and the clock signal are passively split and fed

into two identical samplers, S1 and S2. The errors arising from input and clock signal propagate through both samplers. Therefore, they can be eliminated by subtracting the samples $x_{k,S1}(k \cdot T_s)$ and $x_{k,S2}(k \cdot T_s)$, recorded from S1 respectively S2 simultaneously at the sampling instant $k \cdot T_s$:

$$\Delta x(k \cdot T_s) = x_{S1}(k \cdot T_s) - x_{S2}(k \cdot T_s), \tag{7.14}$$

where T_s is the sampling rate and $k \in \mathbb{N}$. The subsequent post-processing steps are then performed in the same way as described in Chapter 7.2. It should be noted that both samplers contribute to the calculated jitter. Assuming two identical samplers, the calculated jitter in a dual-channel setup, $\sigma_{t,\mathrm{dual}}$, is increased by a factor of $\sqrt{2}$:

$$\sigma_{t,\mathrm{dual}} = \sqrt{2} \cdot \sigma_t. \tag{7.15}$$

The efficiency of this noise cancellation technique is limited by the amplitude and phase mismatch of the two samplers. The amplitude mismatch can be compensated by normalizing the signals properly. The impact of phase mismatch is investigated in Appendix C. Assuming that both samplers have an ideal lowpass filter characteristic with a cutoff frequency f_c and a skew in the clock path of ΔT, the generator jitter $\sigma_{t,\mathrm{Gen}}$ is reduced by the correlation to an effective jitter $\sigma_{t,\mathrm{Gen,eff}}$:

$$\sigma_{t,\mathrm{Gen,eff}} = \sqrt{2 - 2 \cdot \mathrm{sinc}\,(2 \cdot \pi \cdot f_c \cdot \Delta T)} \cdot \sigma_{t,\mathrm{Gen}}. \tag{7.16}$$

According to Eq. 7.16, the efficiency of this cancellation technique does not solely depend on the absolute skew ΔT, but rather on the product $\Delta T \cdot f_c$. Concentrating on samplers with a bandwidth in the multi-GHz range and low intrinsic jitter values, an extreme low skew is tolerable to achieve sufficient generator noise suppression η_{xcorr}:

$$\begin{aligned} \eta_{\mathrm{xcorr}} &= 1 - \frac{\sigma_{t,\mathrm{Gen,eff}}}{\sigma_{t,\mathrm{Gen}}} \\ &= 1 - \sqrt{2 - 2 \cdot \mathrm{sinc}\,(2 \cdot \pi \cdot f_c \cdot \Delta T)}. \end{aligned} \tag{7.17}$$

It must be ensured that the channel phase mismatch between the two samplers is small enough to reduce the generator jitter sufficiently. Fig. 7.4 illustrates η_{xcorr} as a function of the skew ΔT on the example of two different sampler bandwidths, whereby an ideal low-pass filter transfer characteristic of the sampler is assumed. Thinking of a realistic scenario, where the generator jitter is ten times larger than the intrinsic sampler jitter, η_{xcorr} should be at least 99 % to suppress the generator jitter sufficiently. Therefore, a maximum skew of $\Delta T = 68\,\mathrm{fs}$ for $f_c = 13\,\mathrm{GHz}$, respectively $\Delta T = 29\,\mathrm{fs}$ for $f_c = 30\,\mathrm{GHz}$ is tolerable.

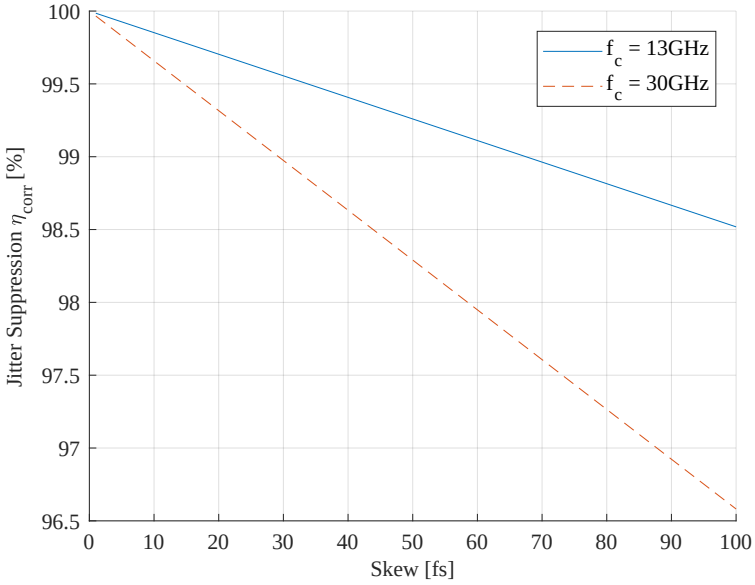


Figure 7.4: Cancellation of signal source jitter in a dual-channel measurement setup as a function of the channel skew. Respective sampler bandwidths $f_c = 13\,\text{GHz}$ and $f_c = 30\,\text{GHz}$ are considered, whereby an ideal low-pass filter transfer characteristic is assumed.

7.3.4 Distortion Robustness

The influence of distortion on the accuracy of the proposed method depends on the type of distortion. At first, the influence of harmonic distortion is investigated. Considering an input signal $v(t) = A \cdot \sin(2 \cdot \pi \cdot f_{in} \cdot t) + B \cdot \sin(4 \cdot \pi \cdot f_{in} \cdot t)$, which consists of the fundamental with amplitude A and the second harmonic with amplitude B, leads to the cyclostationary variance

$$\begin{aligned}\sigma_v^2(\phi) = \sigma_t^2 \cdot (2 \cdot \pi \cdot f)^2 \cdot \Big[&\frac{A^2}{2} + \frac{A^2}{2} \cdot \cos(2 \cdot \phi) + 2 \cdot A \cdot B \cos(\phi) \\ &+ 2 \cdot A \cdot B \cos(3 \cdot \phi) + 2 \cdot B^2 \cdot \cos(4 \cdot \phi) + 2 \cdot B^2\Big] \\ &+ \sigma_{Nc}^2(\phi) + \sigma_{Ns}^2.\end{aligned} \tag{7.18}$$

According to Eq. 7.18, the cyclostationary variance has grown quite a bit depending on the amplitude B. But the jitter-sensitive function parameter fit in Eq. 7.3 is only sensitive to the term proportional to $\cos(2 \cdot \phi)$ due to the orthogonality of the basis functions of the Fourier series. Therefore, the presence of a second harmonic has no effect on the calculated jitter. Extending the analysis to higher-order harmonics leads to slightly differing terms in Eq. 7.18, but again without affecting the jitter-sensitive fit.

At next, the influence of non-harmonic distortions is investigated. Since non-harmonic distortions have a frequency coprime to the signal frequency, the sorting-by-phase operation converts them into

a phase-independent noise component. As a consequence, the stationary noise σ_{Ns}^2 increases and more samples must be acquired to get the same accuracy as without the presence of non-harmonic distortion according to Eq. 7.6 and Eq. 7.13.

7.3.5 Data Acquisition with a Waveform Recorder

The choice of the device used for digitizing the analog output of the sampler has also a strong influence on the achievable accuracy. Thus, it is worth to compare the two available time-domain sampling methods, RTO and sampling oscilloscope, with respect to the requirements of the proposed jitter measurement method.

A RTO captures consecutive samples around the trigger event at the full-sample rate and stores the samples in the memory. Modern oscilloscopes provide highest sampling rates up to $f_s = 240\,\text{GS/s}$ at adequate high bandwidths up to $f_{3dB} = 100\,\text{GHz}$, but with a dynamic range limited typically to 8 bits [125], [126], [127].

A sampling oscilloscope acquires periodic signals at comparable bandwidths with a high dynamic range, typically 14 bits. It has a lower noise compared to RTOs, and an extreme fine time resolution. This is realized by an alternative trigger concept. On the first trigger event, the scope captures a set of non-contiguous samples. Before the next trigger event arrives, a hardware-controlled delay is applied on the trigger signal, hence the next set of samples is captured time-delayed. The time-base resolution is determined by the accuracy of the delay, which is in the range of 100 femtoseconds for modern sampling oscilloscopes.

The improved dynamic range and time resolution comes at the expense of an increased measurement time. Considering a periodic signal with a period t_p and the acquisition of one sample per trigger event, the acquisition of N_{smp} samples will take a duration of

$$t_{meas,SO} = N_{smp} \cdot t_p, \tag{7.19}$$

which is increased by a factor of N_{smp} compared to the measurement duration using a RTO.

A performance summary of the instruments available for this work is shown in Table 7.1.

	RTO [125]	Sampling oscilloscope [128]
Bandwidth f_{3dB}	20 GHz	50 GHz
Sampling frequency f_s	40 GS/s	200 kHz
Deskew resolution Δt	25 ps	100 fs
Jitter σ_t	100 fs	800 fs
Resolution	8 bits	14 bits
Noise floor (rms)	1.44 mV	600 μV

Table 7.1: Performance summary of the RTO and the sampling oscilloscope used in this work.

Since the accuracy of the measurement strongly depends on the stationary noise floor σ_{Ns}, a sampling oscilloscope is the preferable choice for the jitter measurement due to its high dynamic range and low noise floor. Additionally, its higher bandwidth allows an accurate acquisition of the signals, and an extreme fine de-skew availability allows a very accurate adjusting of the sampling instant, which turned out to be very helpful for maximizing the efficiency of the noise-canceling.

7.4 Implemented Post-Processing Algorithm

A flowchart of the implemented digital post-processing algorithm is shown in Fig. 7.5. As proposed in Chapter 7.3.2, two individual measurements are performed. The jitter-induced noise is measured with a high input signal frequency $f_{in} = f_{hi}$, while the cyclostationary noise originating from the digitizing operation is measured with a low signal frequency $f_{in} = f_{lo}$ according to Eq. 7.11.

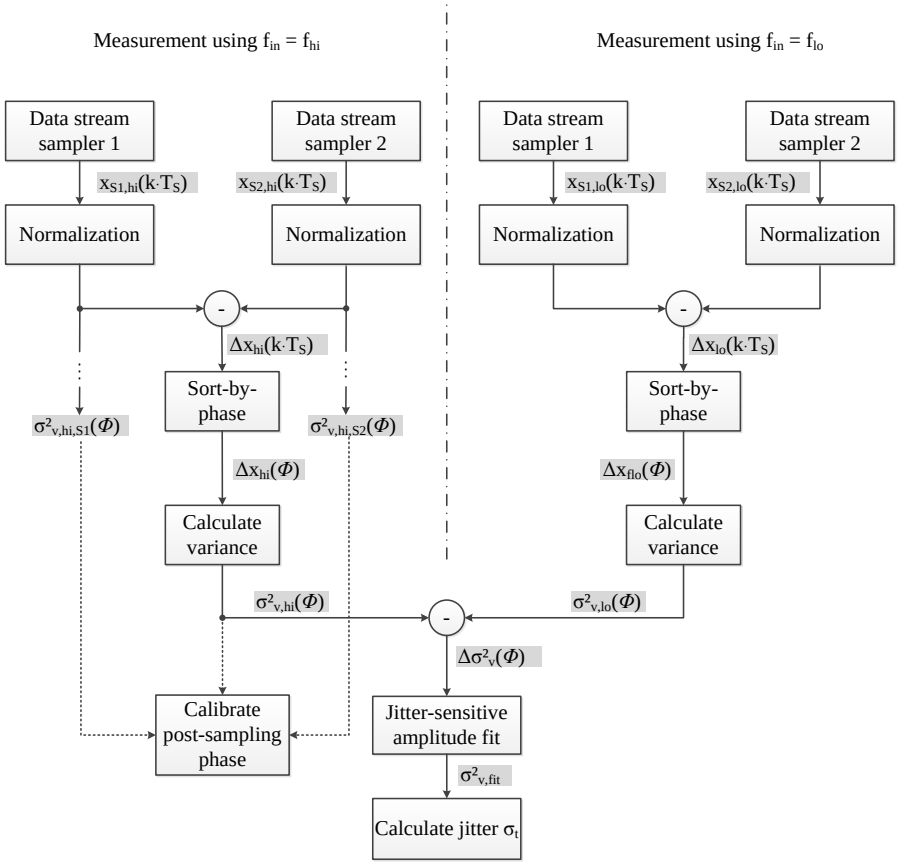


Figure 7.5: A flowchart of the implemented digital post-processing algorithm.

Each data stream is normalized to compensate a possible gain mismatch between the devices. In case the sampler is implemented in a TI architecture, the data stream is de-interleaved at first, and the normalization is performed individually for each sub-stream.
Then, the samples of the corresponding data streams are subtracted (Eq. 7.14), resulting in the signals $\Delta x_{hi}(k \cdot T_s)$ respectively $\Delta x_{lo}(k \cdot T_s)$. The samples are sorted by phase and the corresponding cyclostationary variances $\sigma^2_{v,hi}$ and $\sigma^2_{v,lo}$ are calculated (Eq. 7.1). The jitter-sensitive parameter fit (Eq. 7.3) is applied on the difference $\Delta\sigma_v(\phi)$ and the jitter σ_t is calculated (Eq. 7.12).

Experiments have shown a strong influence of the waveform recorders sampling instant, namely its precision, on the noise cancellation efficiency of this method. Only the development of a sophisticated calibration algorithm for adjusting the post-sampling phase enables the full potential of the proposed method. Regarding the sampler output of a single channel, it is obvious that the relevant information is contained in the hold phase of the analog output signal. Digitizing the analog output in the transition between two samples would significantly increase the noise of the resulting digital data stream. For this purpose, the post-sampling phase is adjusted such that the RMS noise is minimized.
A flowchart of the implemented calibration algorithm is shown in Fig. 7.6. The basic idea is to:

1. Sweep the post-sampling phase in between a certain range of phase offset values with a given step-size (phase loop).
2. Find the optimum post-sampling phase with the minimum RMS noise $\sigma_{v,RMS}$, which is defined by $\sigma_{v,RMS} = \sqrt{\frac{1}{N_{ph}} \cdot \sum_{n=1}^{N_{ph}} \sigma_v^2(\phi_n)}$.
3. Enclosure the found optimum in the subsequent iterations by centering a decreased range of interest with an reduced step size around it (zoom loop).

At first glance, this may appear pretty straight-forward, but as only a finite number of samples are taken into account for the calculation of $\sigma^2_{v,rms}$, the measured value becomes a random variable itself.

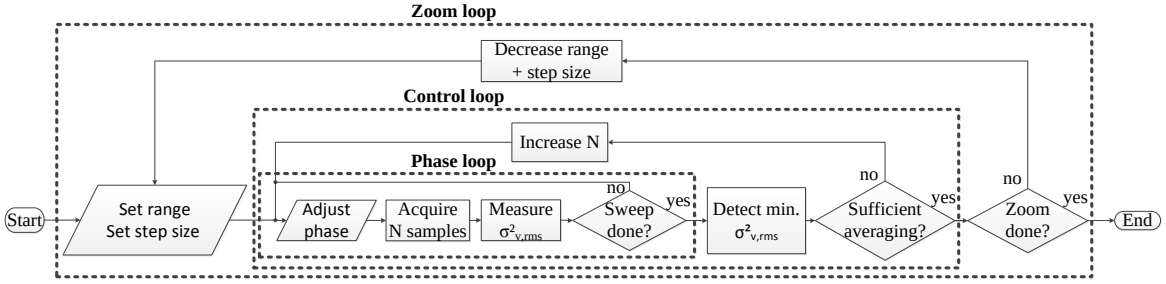


Figure 7.6: A flowchart of the calibration algorithm used for adjusting the post-sampling phase of the waveform recorder.

It must be ensured that the detection of the minimum is not affected by the noisy character of the random variable. Especially when the step size is sufficient small and therefore also the difference between the measured RMS values, is becomes quite hard to determine the exact minimum accurately. Therefore, an additional check is implemented (control loop), which verifies that sufficient samples are acquired to find the minimum.
As the success of the calibration cannot be seen before the time-consuming measurement is performed and evaluated - which can take easily multiple hours - it is preferable that the stop criteria in the control loop is robust against any errors and fast enough to realize a short calibration time. For this purpose, multiple measurements are performed for each post-sampling phase value and a moving-average filter is applied on this data. At next, the number of samples is increased and the relative positions of the averaged $\sigma^2_{\mathrm{v,rms}}$ values are compared with the positions of their neighbors. As stop criterion, the relative positions must not change for a certain number of subsequent iterations of the control loop.
From the previous discussion, it becomes obvious that the precision of the phase adjusting control strongly influences the efficiency of the proposed method. According to the discussion in Chapter 7.3.5, a sampling oscilloscope having a hardware-controlled de-skew capability with an extreme fine resolution is the preferable device for the jitter measurement.

7.5 Experimental Results Using an Electrical High-End Sampler

7.5.1 Measurement Setup

The functionality of the proposed method was verified at first on an electrical high-end sampler chip developed by R&S. This packaged, product-ready chip in combination with an available evaluation board enables a long-term stable measurement setup and therefore best conditions for the challenging measurement. The chip contains two 10 GS/s samplers, each providing an analog bandwidth of $f_{3dB} = 13\,\mathrm{GHz}$ and a simulated jitter of $\sigma_t = 20\,\mathrm{fs}$.
In Fig. 7.7, a block diagram of the used measurement setup is shown. The input and clock signals are provided by two identical low phase noise signal generators [129], which are synchronized with the available $f_{ref} = 10\,\mathrm{MHz}$ reference. The input signal is split by a passive 3 dB-splitter and fed to the sampler inputs, while the clock signal is distributed on-chip to the samplers.
A sampling oscilloscope [128] acquires the analog signals at the sampler outputs. The required trigger signal is provided by a buffered clock signal provided by the chip, which is scaled down by a low-jitter frequency divider.
Experiments have shown that even small changes in the temperature, which are usually unavoidable in a laboratory, have a noticeable influence on the efficiency of the overall noise cancellation. Further investigations revealed a dependency of the relative phase of the digitized data streams on the temperature and explain well the degradation. The analysis of the source of this effect, the chip itself or the

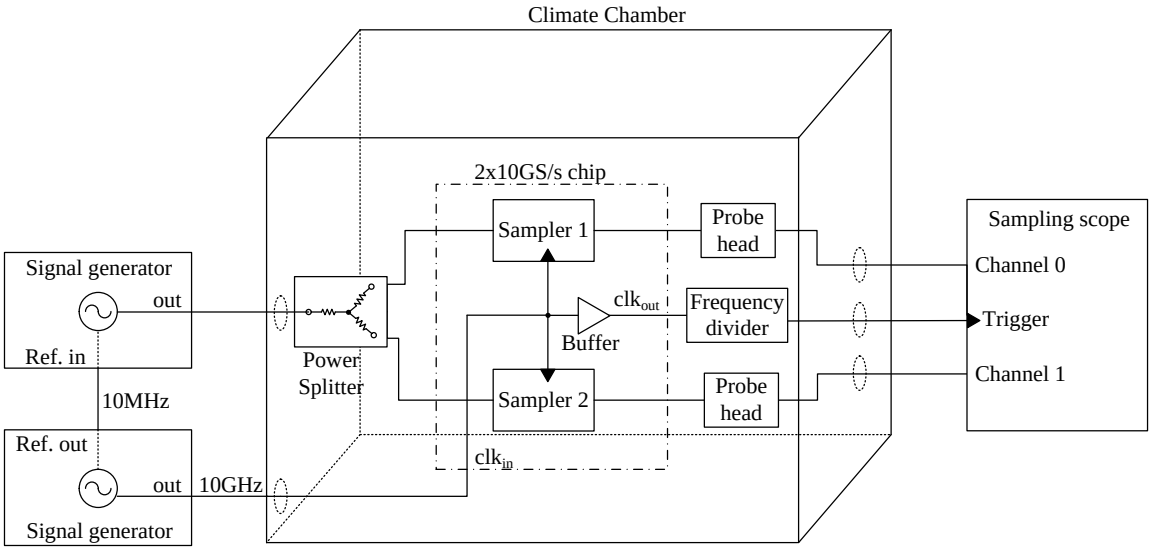


Figure 7.7: A block diagram of the setup used for the verification of the proposed jitter measurement method on the example of an electrical high-end 10 GS/s sampler chip.

digitizing process, might be subject of further investigations. As a consequence, the temperature of the critical measurement components (chip and evaluation board, frequency divider, probes of the sampling oscilloscope) were stabilized using a climate chamber.

7.5.2 Measurement Results

Before the actual measurement is performed, the optimum post-sampling phase of the sampling oscilloscope is adjusted de-skewing the individual channels according to the algorithm proposed in Chapter 7.4. At first, the calibration is performed on one of the two channels. In the given example, channel 1 is used.

Fig. 7.8 a) illustrates $\sigma^2_{\mathrm{v,rms}}$, the RMS of $\sigma^2_{\mathrm{v,hi,S1}}$, as a function of the adjusted time delay on the example of the first, third, and fifth iteration of the zoom loop. Regarding the first iteration, the time delay is swept over the total sample period $\mathrm{T_s} = 100\,\mathrm{ps}$ and two minima of equal value can be identified. They correspond to the optimum post-sampling phase of two adjacent samples. As expected, the noise significantly increases in between the two optimum sampling instants. In the following iterations, the range of interest continuously enclosures the one of the minima, while the step size is further reduced until the minimum step size of the sampling oscilloscope is reached.

Once the first channel is calibrated properly, the phase of the second channel is adjusted. Therefore, the minimum of the variance $\Delta\sigma^2_{\mathrm{v,rms}}$ as RMS of the variance $\Delta\sigma^2_{\mathrm{v,hi}}$, obtained from the difference of the two channels, is located by the same calibration algorithm. The results from this calibration are shown in Fig. 7.8 b). Taking a look at the first iteration, a local and a global minimum can be identified

and their absolute values obviously differ from each other. The global minimum corresponds to the desired optimum post-sampling phases with the best noise cancellation efficiency. The local minimum corresponds to an optimum adjusting of the two individual channel phases, but the difference is obtained from two non-contiguous samples. As a consequence, the noise cancellation of the generator jitter does not work properly at this point.

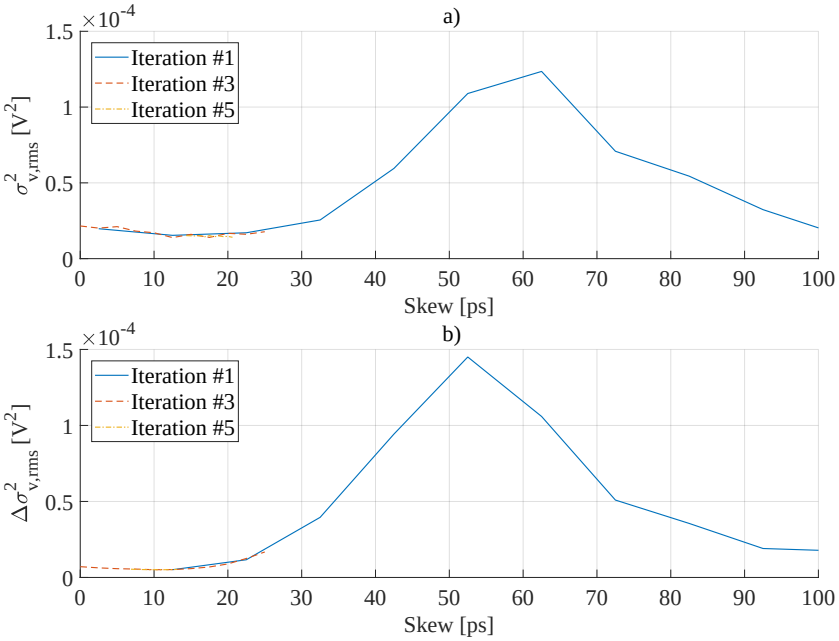


Figure 7.8: Results from the post-sampling phase calibration of the waveform recorder: a) The variance $\sigma^2_{\mathrm{v,rms}}$ of channel 1 as function of the hardware-controlled time delay (skew) on the example of the first, third and fifth iteration. b) The variance $\Delta\sigma^2_{\mathrm{v,rms}}$ calculated from the difference signal of the two channels as a function of the skew on the example of the first, third and fifth iteration.

Once the calibration is done, the actual measurement is performed. Fig. 7.9 a) illustrates the cyclostationary variances $\sigma^2_{\mathrm{v,hi,S1}}(\phi)$ and $\sigma^2_{\mathrm{v,hi,S2}}(\phi)$, obtained from the measured output signals of the two samplers, as response to an input signal with a frequency of $\mathrm{f_{hi}} = 11.7\,\mathrm{GHz}$. An estimated amplitude $2 \cdot \widehat{\sigma^2_{\mathrm{v,fit}}} = 320\,(\mathrm{mV})^2$ corresponds to a jitter $\hat{\sigma}_{\mathrm{t}} = 240\,\mathrm{fs}$ according to Eq. 7.4, which is much higher than expected intrinsic sampler jitter due to the additional jitter contributed by the signal and clock generator.

Fig.7.9 b) illustrates the cyclostationary variance $\sigma^2_{\mathrm{v,hi}}(\phi)$, which is calculated from the difference of the sampler output signals. As expected, $\sigma^2_{\mathrm{v,hi}}(\phi)$ is much smaller compared to $\sigma^2_{\mathrm{v,hi,S1}}(\phi)$ and $\sigma^2_{\mathrm{v,hi,S2}}(\phi)$, which demonstrates that the generator jitter cancellation works well. The amplitude of the jitter-sensitive fit has a value of $2 \cdot \widehat{\sigma^2_{\mathrm{v,fit}}} = 7.6\,(\mathrm{mV})^2$, which corresponds to a total jitter $\hat{\sigma}_{\mathrm{t,dual}} = 37.3\,\mathrm{fs}$, respectively $\hat{\sigma}_{\mathrm{t}} = 26.4\,\mathrm{fs}$ for each sampler according to Eq. 7.15.

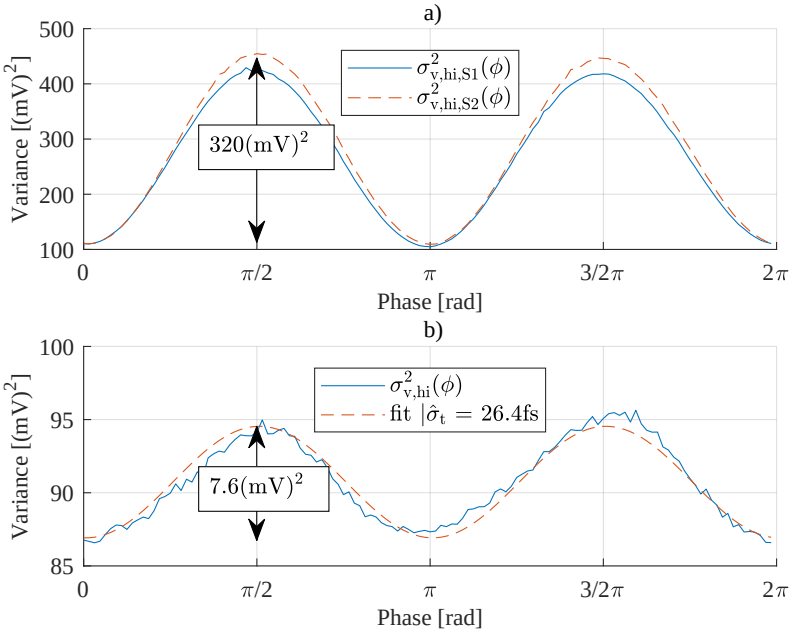


Figure 7.9: a) The cyclostationary variances $\sigma^2_{v,hi,S1}$ (solid line) and $\sigma^2_{v,hi,S2}$ (dashed line) calculated from the recorded data of the two sampler outputs as response to a high input signal frequency of $f_{hi} = 11.7\,GHz$. b) The cyclostationary variance $\sigma^2_{v,hi}$ (solid line) obtained from the difference signal of the two channels and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation.

At next, the measurement with a low input signal frequency of $f_{lo} = 1.7\,GHz$ is performed. Fig. 7.10 a) illustrates the obtained cyclostationary variance $\sigma^2_{v,lo}(\phi)$ (solid line). One can clearly recognize a jitter-characterstic shape of the curve, but due to the low input frequency it must originate from the post-sampling effects described in Chapter 7.3.2. Since the magnitude of this undesired noise component is in the same order of $\sigma^2_{v,hi}(\phi)$ (dashed line), it increases the estimated jitter appropriately. The post-sampling effects are then eliminated by taking the difference of these variances, and the resulting variance $\Delta\sigma^2_v$ is shown in Fig. 7.10 b) (solid line). The function fit (dashed line) has an amplitude $2 \cdot \widehat{\sigma^2_{v,fit}} = 4.2\,(mV)^2$, which corresponds to a total jitter $\hat{\sigma}_{t,dual} = 28.0\,fs$, respectively $\hat{\sigma}_t = 19.8\,fs$ for each sampler.

At last, the accuracy of the proposed method is compared to the theoretical value expected from Eq. 7.13. Therefore, multiple measurements are performed with a given number of samples used for calculating the jitter. From these measurements the standard deviation $\sigma_{\hat{\sigma}_t}$ of the measured jitter values is calculated and compared to $\sigma_{\sigma_{tmax}}$ of the model. A stationary noise floor of $\sigma^2_{Ns} = 84\,(mV)^2$ is extracted from Fig. 7.10 a).

As shown in Fig. 7.11, the statistic model fits to the measurement results very well, which demonstrates the consistency of the model. It should be noted that an unprecedented accuracy of $\sigma_{\hat{\sigma}_t} = 324\,as$ is

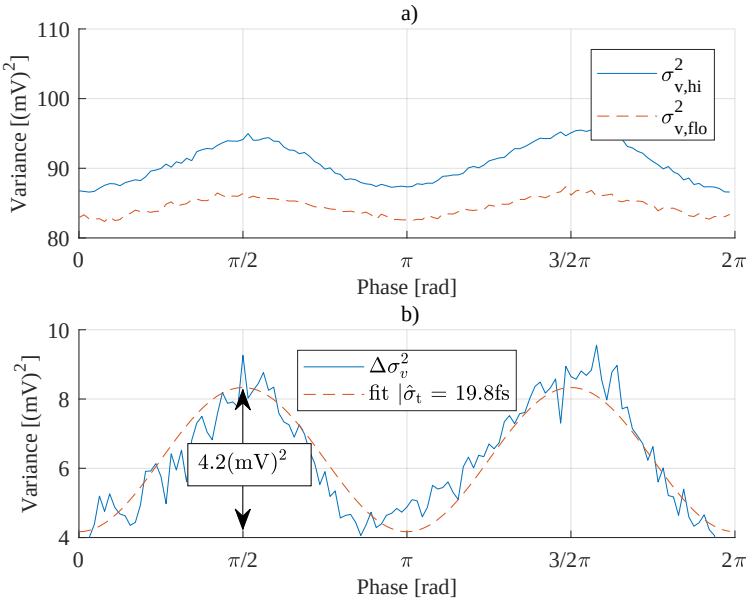


Figure 7.10: a) The cyclostationary variance $\sigma^2_{\mathrm{v,lo}}$ (solid line) obtained from the difference signal of the two channels as response to the low input signal frequency of $\mathrm{f_{lo}} = 1.7\,\mathrm{GHz}$. In addition, $\sigma^2_{\mathrm{v,hi}}$ (dashed line) is shown for comparison. b) The cyclostationary variance $\Delta\sigma^2_{\mathrm{v}}$ (solid line) and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation.

demonstrated using a total number of about 31 million samples.

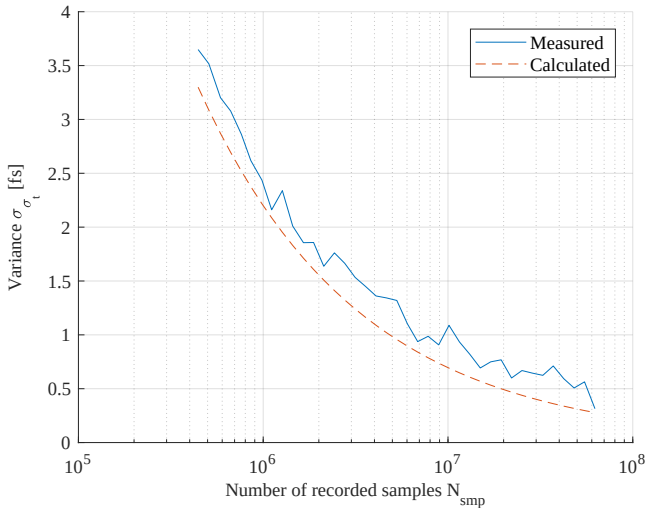


Figure 7.11: Standard deviation $\sigma_{\sigma_{\mathrm{t}}}$ of the estimated jitter $\hat{\sigma}_{\mathrm{t}}$, measured with the electronic 10 GS/s sampler, as a function of the number of acquired samples $\mathrm{N_{smp}}$ (solid line). In addition, the maximum allowable standard deviation predicted by the theoretical model is provided for comparative purposes (dashed line).

7.6 Experimental Results Using the Photonic-Assisted Sampler

7.6.1 Measurement Setup

A block diagram of the setup used for the verification of the proposed jitter measurement method with the photonic-assisted sampler is shown in Fig. 7.12. Experiments have shown that the long-term stability of the setup was not sufficient to use the preferable sampling oscilloscope as waveform recorder, thus a RTO [125] was used to digitize the analog outputs of the samplers.
As shown in Chapter 6.2.2, synchronization problems between the MLL and the RTO lead to a significant increase of the noise floor. As a consequence, the number of samples to be acquired for a given accuracy would increase dramatically, and due to this also the duration of the measurement. Since the jitter performance of the sampler is not determined by its sample rate, but by the optical pulse energy at the input of the PD (Eq. 4.29), the sampler operates at a reduced sample rate of $f_s = 1.26\,\mathrm{GS/s}$. Therefore, the optical interleaver is not used to increase the pulse repetition rate of the MLL, and the frequency divider used in the DEMUX/MUX clock generation is replaced by a frequency divider to provide the clock signal $f_{MUX} = 630\,\mathrm{MHz}$ for the MUX and DEMUX.

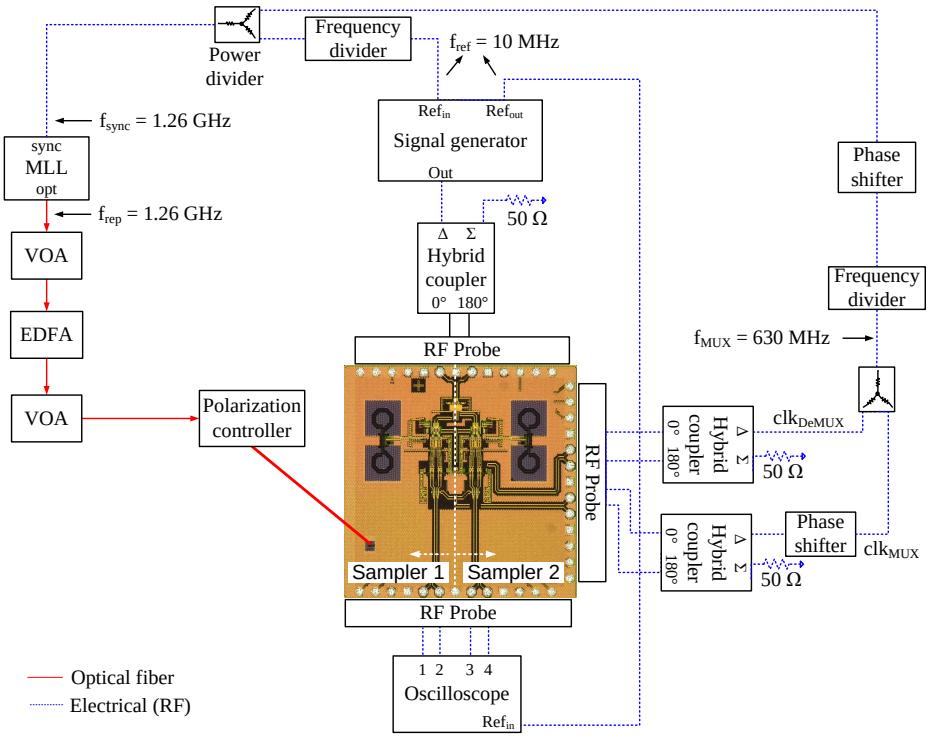


Figure 7.12: A block diagram of the setup used for the verification of the proposed jitter measurement method with the photonic-assisted sampler.

7.6.2 Measurement Results

Fig. 7.13 illustrates the cyclostationary variances $\sigma^2_{\mathrm{v,hi,S1}}$ and $\sigma^2_{\mathrm{v,hi,S2}}$, obtained from the two sampler outputs as response to a high-frequency input signal with $f_{\mathrm{hi}} = 25.2\,\mathrm{GHz}$. A jitter-characteristic shape with an amplitude $2 \cdot \widehat{\sigma^2_{\mathrm{v,fit}}} = 200\,(\mathrm{mV})^2$ corresponds to a jitter of $\hat{\sigma}_{\mathrm{t}} = 90\,\mathrm{fs}$, which is in the range of the jitter expected from the signal generator [112]. But since the calculated variances differ from the ideal cosine shape of jitter-induced noise, a significant amount of non-jitter-related noise is still contained in the cyclostationary variances.
Fig. 7.13 b) illustrates the cyclostationary variance $\sigma^2_{\mathrm{v,hi}}$ (solid line), calculated from the difference of the sampler outputs. A jitter-characteristic shape can be observed and the amplitude of the jitter-sensitive fit (dashed line) of $2 \cdot \widehat{\sigma^2_{\mathrm{v,fit}}} = 42\,(\mathrm{mV})^2$ corresponds to a total jitter of $\hat{\sigma}_{\mathrm{t,dual}} = 41\,\mathrm{fs}$, respectively $\hat{\sigma}_{\mathrm{t}} = 29\,\mathrm{fs}$ for each sampler.

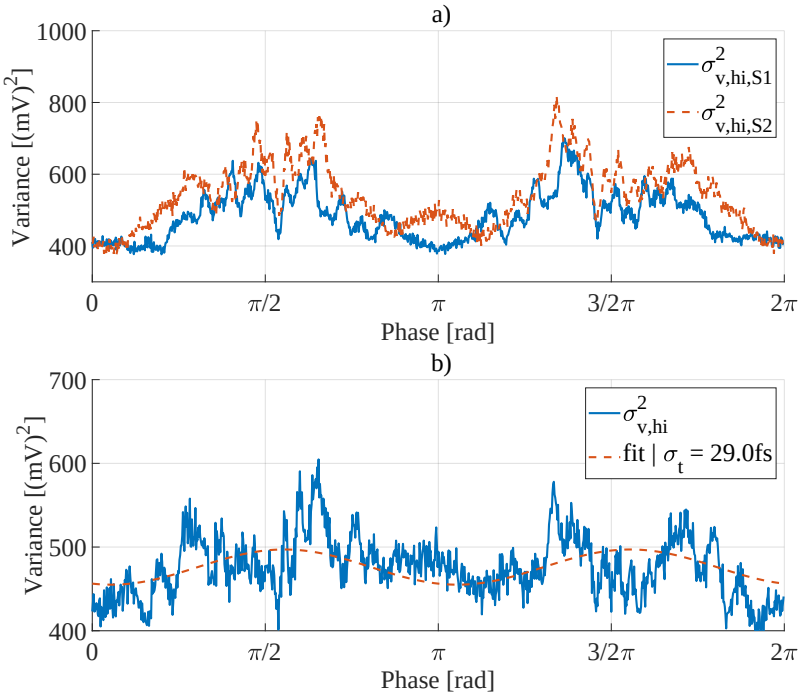


Figure 7.13: a) The cyclostationary variances $\sigma^2_{\mathrm{v,hi,S1}}$ and $\sigma^2_{\mathrm{v,hi,S2}}$ calculated from the recorded data of the two sampler outputs as response to a high input signal frequency of $f_{\mathrm{hi}} = 25.2\,\mathrm{GHz}$. b) The cyclostationary variance $\sigma^2_{\mathrm{v,hi}}$ (solid line) obtained from the difference signal of the two channels and the corresponding jitter-sensitive fit used for the jitter estimation.

Fig. 7.14 a) illustrates the cyclostationary variance $\sigma^2_{\mathrm{v,lo}}$ (solid line), obtained from the dual-channel measurement with the low-input frequency $f_{\mathrm{lo}} = 5.04\,\mathrm{GHz}$. Again, a phase-dependent characteristic can be observed. Comparing the shape with that of $\sigma^2_{\mathrm{v,hi}}$ (dashed line), it becomes obvious that only a small amount of non-jitter-related noise will cancel out by the frequency-differential approach.

The cyclostationary variance $\Delta\sigma_v^2$ and the corresponding jitter-sensitive fit are shown in Fig. 7.14 b). The fit shows an amplitude of $2 \cdot \sigma_{v,fit}^2 = 38\,(\mathrm{mV})^2$, which corresponds to an total jitter of $\sigma_{j,dual} = 40\,\mathrm{fs}$, respectively $\sigma_t = 28.2\,\mathrm{fs}$. But taking a look at the phase-dependent characteristic of $\Delta\sigma_v^2$, it becomes obvious that not all non-jitter-related error sources could be eliminated properly. Therefore, the stated jitter value represents a pessimistic estimation of the actual sampler jitter.

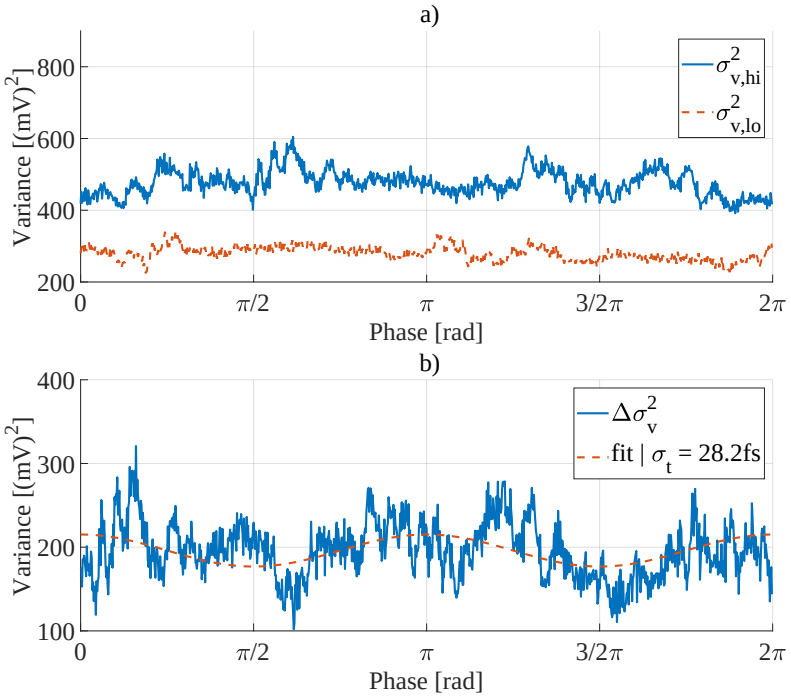


Figure 7.14: a) The cyclostationary variance $\sigma_{v,lo}^2$ (solid line) obtained from the difference signal of the two channels as response to the low input signal frequency of $f_{lo} = 5.04\,\mathrm{GHz}$. In addition, $\sigma_{v,hi}^2$ (dashed line) is shown for comparison. b) The cyclostationary variance $\Delta\sigma_v^2$ (solid line) and the corresponding jitter-sensitive fit (dashed line) used for the jitter estimation.

At last, the accuracy of the jitter measurement using the photonic-assisted sampler is investigated by performing multiple measurements and observing the statistic of the results. Fig. 7.15 illustrates the standard deviation $\sigma_{\hat{\sigma}_t}$ of the measured jitter values as a function of the number of the acquired samples N_{smp}. Using a maximum number of 2.5 million samples, a measurement accuracy of $\sigma_{\hat{\sigma}_t} = 1.2\,\mathrm{fs}$ is demonstrated. Comparing it with the maximum allowable standard deviation predicted by the theoretical model, a significant deviation in the shape of the curves can be observed for a lower number of samples. Obviously, the synchronization and stability problems from the measurement setup affect the accuracy of the method significantly.

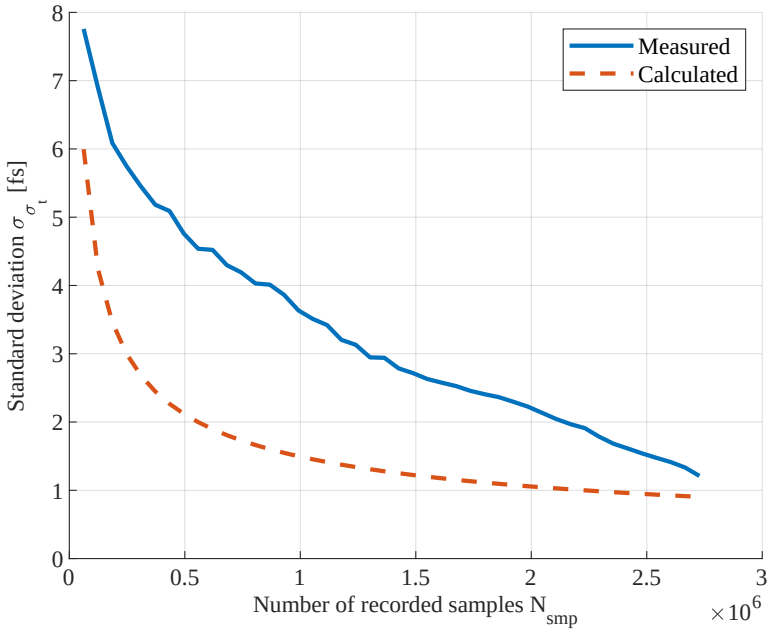


Figure 7.15: Standard deviation $\sigma_{\hat{\sigma}_t}$ of the estimated jitter $\hat{\sigma}_t$, measured with the photonic-assisted 10 GS/s sampler as a function of the number of the acquired samples N_{smp} (solid line). The maximum allowable standard deviation predicted by the theoretical model is also shown for comparative purposes (dashed line).

8 Conclusions

In this thesis, the advantages of photonic-assisted sampling to push forward the jitter-related performance limitation of high-speed ADCs were successfully demonstrated. Within the frame of this demonstration, a monolithically integrated, optically clocked wideband sampler has been developed in a photonic 0.25 μm SiGe BiCMOS technology.

Starting with the ADC basics, the static and dynamic effects influencing the ADC performance were investigated. Hereby, the main focus is laid on clock jitter as the major bottleneck of high-speed ADCs. According to a top-down approach, the system specifications for an 80 GS/s, TI-ADC architecture providing an analog bandwidth $f_{3dB} > 30$ GHz and an ENOB of 8 bits were derived to specify the requirements for the individual system components.

The derived specifications were used for the development of the individual system components - namely the photonics BiCMOS platform, the fiber-to-chip interface, the optical CDN, the PD as key components of the O/E integration and the MLL.

As first demonstrator, an O/E clock converter circuit as key enabling block for various low-jitter applications was developed. It converts the optical pulse train coming from the MLL into an low-jitter square wave signal. A noise analysis of the circuit including the most critical noise sources was performed to assess the jitter of its electrical output. The fabricated test chip includes the optical CDN proposed for the 8x TI ADC, PDs for their large-signal characterization, and O/E clock converter circuits. Measurements have shown a total jitter of $\sigma_t = 24$ fs, whereby the main contribution originates from the used MLL. Regarding the wideband phase noise floor of the clock converter of $L_{SSB} < -166$ dBc, a jitter $\sigma_t = 11.2$ fs is obtained, which matches very well the expectations from the theoretical model.

Finally, a 10 GS/s sampler core unit suitable for the integration in a 80 GS/s TI-ADC was developed. Herein, a pulse-sampling architecture is selected, whereby the to-be-sampled signal is multiplied with a sequence of short electrical pulses derived from the optical pulse train und subsequently integrated. Due to an extraordinary performance of the PD, this architecture provides an extremely low intrinsic jitter and the required bandwidth. Measurements on the fabricated test chips have shown a bandwidth $f_{3dB} > 30$ GHz, a THD < -33 dB over the entire band, and a SNR = 35.3 dB for low-frequency input signals.

To determine the intrinsic sampler jitter in the expected femtosecond range, a novel method was developed. Based on a detailed analysis of the error sources in the measurement setup, techniques

for their compensation as well as equations allowing to quantify the the accuracy are presented. The method was successfully verified with an electrical high-end sampler, and an outstanding accuracy of $\sigma_{\sigma_t} = 320\,\text{as}$ was demonstrated by measuring jitter in the range of $\sigma_\text{t} = 20\,\text{fs}$. This method was finally used to measure the jitter of the developed optically-clocked 10 GS/s sampler core unit, revealing an outstanding jitter of $\sigma_\text{t} < 30\,\text{fs}$.

In conclusion, photonic-assisted ADCs are able to achieve a significant improvement of the jitter performance compared to their electronic counterparts. The used Si photonics platform allows a monolithic integration of all required optical components - except of the optical clock source - in a high-performance BiCMOS process. In addition, high-performance PDs with bandwidths $f_{3\text{dB}} > 50\,\text{GHz}$ enable the implementation of wideband samplers circuits with extreme low intrinsic jitter values. But there are still some open issues, which need to be solved to be suitable for the practical application:

- A fundamental 10 GHz MLL laser source with a comparable jitter performance and output power is required to avoid an intrinsic skew of the optical clock, which is coupled into the chip.
- As the measurements with the test chips have shown, a stable optical coupling is required, resulting in the necessity of new optical packages. This is already topic of actual research and further progress can be expected in the near future [130].
- The temperature-dependent skew originating from the optical CDN is a problem, and compensation techniques needs to be investigated.
- The development of the PDs has not been finished yet, and it is expected that the performance is further improved until the final qualification of the technology.
- The extension from a 10 GS/s sampler core to a fully 80 GS/s TI ADC involve more challenges, such as the wideband signal distribution, which needs to be further investigated.
- The design of the developed 10 GS/s sampler has focused on the jitter and bandwidth performance, and a further optimization of the noise and linearity of the sampler is required to meet the overall system specifications.

Although these working packages involve a lot of future work and presumably more open issues, this work has demonstrated the advantages of the photonic approach to finally overcome the jitter- related performance limitation and its capability of pushing the performance of next-generation ADCs to new levels.

Appendices

A Jitter Induced by Noise in the Electrical Domain for the Edge-Triggered Sampling Architecture

In the electrical domain, thermal noise and shot noise contribute .... Thermal current noise is described by a normally-distributed random process with zero-mean and a power spectral density S_{th} of

$$S_{th}(f) = \frac{4 \cdot k_B \cdot T}{R_L}. \tag{A.1}$$

The variance of the thermal noise in the equivalent noise bandwidth $f_{n,eq}$ is then given by

$$\begin{aligned} \sigma_{th}^2 &= \int_0^{f_{n,eq}} S_{th}(f) \mathrm{d}f \\ &= \frac{4 \cdot k_B \cdot T \cdot f_{n,eq}}{R_L}. \end{aligned} \tag{A.2}$$

The equivalent noise bandwidth of a Gaussian transfer can be found by solving the equation

$$\int_{-\infty}^{\infty} |I(j \cdot \omega)|^2 \mathrm{d}\omega = \int_{-\infty}^{\infty} |H_{rect}(j \cdot \omega)|^2 \mathrm{d}\omega, \tag{A.3}$$

where $I(j \cdot \omega)$ is the frequency response and ${H_{rect}}^2(j \cdot \omega)$ is an ideal rectangular function with a cutoff frequency of $2\pi f_{eq}$. For a Gaussian frequency response with a 3 dB-bandwidth f_{3dB}, the equivalent noise bandwidth is given by

$$f_{n,eq} = \frac{\sqrt{\pi}}{2 \cdot \sqrt{\ln(2)}} \cdot f_{3dB}. \tag{A.4}$$

Combining Eq. 4.5, Eq. A.2, and Eq. A.4 yields to a thermal noise-induced jitter of

$$\sigma_{t,th}^2 = \frac{k_B \cdot T \cdot \sqrt{\pi \cdot \ln(2)}}{2 \cdot R_L} \cdot \frac{1}{E_p^2 \cdot {R_{PD}}^2 \cdot \pi^3 \cdot {f_{3dB}}^3}. \tag{A.5}$$

The power spectral density of shot noise is given by

$$S_{shot}(f) = 2 \cdot q \cdot I, \tag{A.6}$$

where q is the electrical charge q and I the corresponding threshold current. Using the same calculation steps as outlined before, the shot noise-induced jitter is given by:

$$\sigma^2_{t,shot} = \frac{q}{4 \cdot \sqrt{2}} \cdot \frac{1}{E_p \cdot R_{PD} \cdot \pi^2 \cdot {f_{3dB}}^2}. \tag{A.7}$$

B Timing Errors due to a Pulse Shape Deviation for the Edge-Triggered Sampling Architecture

When the sampling instant is determined by a certain threshold current generated by a PD, a deviation from the nominal impulse response will result in a timing error. For the following analysis, a Gaussian current impulse response $i_{PD}(t)$ of the PD is considered:

$$i_{PD}(t) = i_0 \cdot e^{-\frac{t^2}{2 \cdot c^2}}. \tag{B.1}$$

The parameter c is related to the FWHM pulse width τ_{FWHM} respectively the (electrical) 3 dB-bandwidth of the PD f_{3dB} by the relationship:

$$c = \frac{\tau_{FWHM}}{2 \cdot \sqrt{2 \cdot \ln(2)}} = \frac{\sqrt{\ln(2)}}{\pi} \cdot \frac{1}{f_{3dB}}. \tag{B.2}$$

According to the conservation of energy, the peak current I_{peak} for an optical pulse energy E_p at the input of a PD with a responsivity R_{PD} is given by

$$i_0 = \frac{2 \cdot \pi}{\ln(2)} \cdot E_p \cdot R_{PD} \cdot f_{3dB}. \tag{B.3}$$

The sampling operation is initiated when the PD current crosses a certain threshold value I_{thres} at a nominal sampling time $t = t_{s,nom}$. When $i_\delta(t)$ is the deviant current crossing the threshold at the time instant $t = t_{s,\delta}$

$$i_\delta(t)\big|_{t=t_{s,\delta}} = i_{PD}(t)\big|_{t=t_{s,\delta}}, \tag{B.4}$$

the timing error Δt is then given by

$$t_{error} = t_{s,nom} - t_{s,\delta}. \tag{B.5}$$

Lets consider at first the influence of a deterministic mismatch of η_{eff}. It can be caused by a power mismatch of the outputs of the CDN, or by a mismatch of the responsivities of the PDs and affect the pulse energy $\mathrm{E_p}$, and causes a constant timing deviation. Defining the mismatch δ_{E} by

$$\delta_{\mathrm{E}} = \frac{\Delta \mathrm{E_p}}{\mathrm{E_p}}, \tag{B.6}$$

the resulting skew $\mathrm{t_{skew,\delta_E}}$ at a nominal sampling instant at $\mathrm{t_{s,nom}} = \mathrm{c} \cdot \sqrt{2 \cdot \ln(2)}$ is given by:

$$\mathrm{t_{skew,\delta_E}} = \frac{\sqrt{\ln(2)}}{2 \cdot \pi \cdot \mathrm{f_{3dB}}} \cdot \left[\sqrt{2\ln(2)} - \sqrt{2 \cdot \ln\left(2 \cdot (1 + \delta_{\mathrm{E}})\right)} \right]. \tag{B.7}$$

Besides the deterministic case, stochastic pulse-to-pulse fluctuations of the MLL also affect the instant of the threshold crossing and result in a jitter $\sigma_{\mathrm{t,p2p}}$. For a usually given small deviation, the root can be linearized around $\delta_{\mathrm{E}} = 0$, and the jitter can be approximated by

$$\sigma_{\mathrm{t,p2p}} = \frac{\delta_{\mathrm{E}}}{2 \cdot \sqrt{2} \cdot \pi \cdot \mathrm{f_{3dB}}}. \tag{B.8}$$

The influence of a bandwidth mismatch of two PDs can be calculated in the same manner. Defining the bandwidth mismatch by:

$$\delta_{\mathrm{f}} = \frac{\mathrm{f_{3dB,\delta}}}{\mathrm{f_{3dB,nom}}}, \tag{B.9}$$

the resultung skew is given by:

$$\mathrm{t_{skew,\delta_f}} = \frac{\sqrt{\ln(2)}}{2 \cdot \pi \cdot \mathrm{f_{3dB}}} \cdot \left[\sqrt{2 \cdot \ln(2)} - \frac{\sqrt{2 \cdot \ln(2 \cdot \delta_{\mathrm{f}})}}{\delta_{\mathrm{f}}} \right]. \tag{B.10}$$

C Influence of Timing Skew on the Efficiency of Generator Jitter Cancellation

Timing mismatch in the clock distribution limits the efficiency of the generator noise cancellation. For the analysis, the signal of a band-limited white noise source is subtracted from a time-shifted copy of itself as shown in Fig. C.1. The variance after the subtraction operation is given by

$$\sigma_{\mathrm{diff}} = 2 \cdot \sigma_{\mathrm{nf}} - \mathrm{Cov}\{\sigma_{\mathrm{nf}}, \sigma_{\mathrm{nfd}}\}, \tag{C.1}$$

where Cov(·) is the covariance. Considering a zero-mean signal, Cov(·) is given by the cross-correlation $R_{x,x'}$, which can be calculated by Fourier-transform the cross-spectral density $S_{x,x'}(j \cdot \omega)$:

$$\begin{aligned} \mathrm{Cov}\{x, x'\} &= R_{nf,nfd} \\ &= \frac{1}{2\pi} \cdot \int_{\mathbb{R}} \mathrm{S}_{\mathrm{nf,nfd}}(j \cdot \omega) d\omega \\ &= \mathcal{F}^{-1}\left\{|H(j \cdot \omega)|^2\right\}. \end{aligned} \tag{C.2}$$

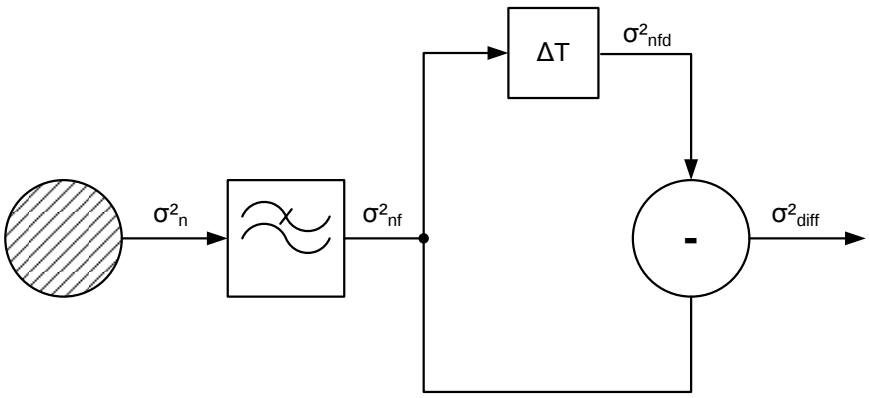


Figure C.1: A simple model to investigate the effect of timing skew in a two-channel measurement on the efficiency of the noise cancellation.

Having an ideal low-pass filter with a cut-off frequency f_c, the variance $\sigma_{x,nc}$ after the subtraction is given by:

$$\sigma_{diff} = (2 - 2 \cdot \mathrm{sinc}\,(2 \cdot \pi \cdot f_c \cdot \Delta T)) \cdot \sigma_{nf}. \tag{C.3}$$

Bibliography

[1] P. J. Mohr, D. B. Newell, and B. N. Taylor, "CODATA recommended values of the fundamental physical constants: 2014," Journal of Physical and Chemical Reference Data, vol. 45, no. 4, p. 043102, 2016. [Online]. Available: https://arxiv.org/pdf/1507.07956.pdf

[2] A. Khilo, S. J. Spector, M. E. Grein, A. H. Nejadmalayeri, C. W. Holzwarth, M. Y. Sander, M. S. Dahlem, M. Y. Peng, M. W. Geis, N. A. DiLello et al., "Photonic ADC: overcoming the bottleneck of electronic jitter," Optics Express, vol. 20, no. 4, pp. 4454–4469, 2012.

[3] B. Murmann, "ADC performance survey 1997-2017," 2017. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[4] L. Kull, J. Pliva, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 110 mw 6 bit 36 GS/s interleaved SAR ADC for 100 gbe occupying 0.048 mm2 in 32 nm SOI CMOS," in 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov 2014, pp. 89–92.

[5] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 90GS/s 8b 667mW 64x interleaved SAR ADC in 32nm digital SOI CMOS," in 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb 2014, pp. 378–379.

[6] A. Bahai, "1.2 dynamics of exponentials in circuits and systems," in 2017 IEEE International Solid-State Circuits Conference (ISSCC), Feb 2017, pp. 14–20.

[7] T. Xanthopoulos, Clocking in modern VLSI systems. Springer Science & Business Media, 2009.

[8] R. Paschotta, "Timing jitter and phase noise of mode-locked fiber lasers," Optics express, vol. 18, no. 5, pp. 5041–5054, 2010.

[9] H. Yang, H. Kim, J. Shin, C. Kim, S. Y. Choi, G.-H. Kim, F. Rotermund, and J. Kim, "Gigahertz repetition rate, sub-femtosecond timing jitter optical pulse train directly generated from a mode-locked Yb:KYW laser," Optics letters, vol. 39, no. 1, pp. 56–59, 2014.

[10] D. Li, "Attosecond timing jitter modelocked lasers and ultralow phase noise photonic microwave oscillators," dissertation, Massachusetts Institute of Technology, 2014.

[11] C. Thangaraj, R. Pownall, P. Nikkel, G. Yuan, K. L. Lear, and T. Chen, "Fully CMOS-compatible on-chip optical clock distribution and recovery," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 10, pp. 1385–1398, Oct 2010.

[12] G. C. Valley, "Photonic analog-to-digital converters," Optics Express, vol. 15, no. 5, pp. 1955–1982, 2007.

[13] A. Siegman and D. Kuizenga, "Proposed method for measuring picosecond pulsewidths and pulse shapes in CW mode-locked lasers," IEEE Journal of Quantum Electronics, vol. 6, no. 4, pp. 212–215, 1970.

[14] D. H. Auston, "Picosecond optoelectronic switching and gating in silicon," Applied Physics Letters, vol. 26, no. 3, pp. 101–103, 1975.

[15] R. A. Lawton and J. R. Andrews, "Optically strobed sampling oscilloscope," IEEE Transactions on Instrumentation and Measurement, vol. IM-25, no. 1, pp. 56–60, March 1976.

[16] A. J. Low and J. E. Carroll, "10ps optoelectronic sampling system," Solid-State and Electron Devices, IEE Journal on, vol. 2, no. 6, pp. 185–190, November 1978.

[17] F. Leonberger and V. Diadiuk, "High-speed InP-based photodetectors," in Electron Devices Meeting, 1983 International. IEEE, 1983, pp. 460–463.

[18] C. Cox III, V. Diadiuk, I. Yao, F. Leonberger, and R. Williamson, "InP optoelectronic switches and their high-speed signal-processiny applications," in 27th Annual Techincal Symposium. International Society for Optics and Photonics, 1983, pp. 164–168.

[19] F. Leonberger and P. Moulton, "High-speed InP optoelectronic switch," Applied Physics Letters, vol. 35, no. 9, pp. 712–714, 1979.

[20] C.-K. Sun, C.-C. Wu, C. T. Chang, P. Yu, and W. H. McKnight, "A bridge type optoelectronic sample and hold circuit," Journal of lightwave technology, vol. 9, no. 3, pp. 341–346, 1991.

[21] E. W. Jacobs, J. B. Sobti, V. F. Vella, R. Nguyen, D. J. Albares, R. B. Olsen, C. T. Chang, S. K. Sun, M. J. Choe, S. Beccue, R. Yu, and J. P. A. van der Wagt, "Optically clocked track-and-hold for high-speed high-resolution analog-to-digital conversion," in 2004 IEEE International Topical Meeting on Microwave Photonics (IEEE Cat. No.04EX859), Oct 2004, pp. 190–192.

[22] D. Knoll, S. Lischke, A. Awny, M. Kroh, E. Krune, C. Mai, A. Peczek, D. Petousi, S. Simon, K. Voigt, G. Winzer, R. Barth, and L. Zimmermann, "High-performance BiCMOS Si photonics platform," in 2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM, Oct 2015, pp. 88–96.

[23] K.-D. Kammeyer, Nachrichtenübertragung. Vieweg + Teubner, 2011.

[24] M. J. Pelgrom, Analog-to-digital conversion. Springer, 2010.

[25] K. Kundert, "Simulating switched-capacitor filters with SpectreRF," The Designers Guide Community, pp. 1–25, 2006.

[26] M. El-Chammas and B. Murmann, Background calibration of time-interleaved data converters. Springer Science & Business Media, 2011.

[27] N. D. Dalt, M. Harteneck, C. Sandner, and A. Wiesbauer, "On the jitter requirements of the sampling clock for analog-to-digital converters," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 49, no. 9, pp. 1354–1360, Sep 2002.

[28] Rohde & Schwarz, "Selecting a Signal Generator for Testing AD Converters," December 2010. [Online]. Available: https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_application/application_notes/1gp66/1GP66_1E.pdf

[29] Linear Technology, "Understanding the Effect of Clock Jitter on High Speed ADCs." [Online]. Available: http://cds.linear.com/docs/en/design-note/dn1013f.pdf

[30] D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 1904–1911, 1998.

[31] J. Elbornsson and J.-E. Eklund, "Blind estimation of timing errors in interleaved AD converters," in Acoustics, Speech, and Signal Processing, 2001. Proceedings.(ICASSP'01). 2001 IEEE International Conference on, vol. 6. IEEE, 2001, pp. 3913–3916.

[32] S. M. Jamal, D. Fu, N. C. J. Chang, P. J. Hurst, and S. H. Lewis, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," IEEE Journal of Solid-State Circuits, vol. 37, no. 12, pp. 1618–1627, Dec 2002.

[33] V. Ferragina, A. Fornasari, U. Gatti, P. Malcovati, and F. Maloberti, "Gain and offset mismatch calibration in time-interleaved multipath A/D sigma-delta modulators," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 12, pp. 2365–2373, Dec 2004.

[34] J. M. D. Pereira, P. S. Girão, and A. C. Serra, "An FFT-based method to evaluate and compensate gain and offset errors of interleaved ADC systems," IEEE Transactions on Instrumentation and Measurement, vol. 53, no. 2, pp. 423–430, 2004.

[35] M. Jridi, G. Monnerie, L. Bossuet, and D. Dallet, "An offset and gain calibration method for time-interleaved analog to digital converters," in Electronics, Circuits and Systems, 2006. ICECS'06. 13th IEEE International Conference on. IEEE, 2006, pp. 1097–1100.

[36] E. Krune, B. Krueger, L. Zimmermann, K. Voigt, and K. Petermann, "Comparison of the jitter performance of different photonic sampling techniques," Journal of Lightwave Technology, vol. 34, no. 4, pp. 1360–1367, Feb 2016.

[37] D. Knoll, S. Lischke, L. Zimmermann, A. Awny, M. Kroh, Peczek, K. Voigt, and K. Petermann, "Fabrication of high bit rate, monolith ically integrated receivers in photonic BiCMOS technology," in 2015 IEEE 12th International Conference on Group IV Photonics (GFP), Aug 2015, pp. 181–182.

[38] D. Knoll, H. H. Richter, B. Heinemann, S. Lischke, Y. Yamamoto, L. Zimmermann, and B. Tillack, "Substrate design and thermal budget tuning for integration of photonic components in a high-performance SiGe:C BiCMOS process," ECS Transactions, vol. 50, no. 9, pp. 297–303, 2013. [Online]. Available: http://ecst.ecsdl.org/content/50/9/297.abstract

[39] D. Knoll, S. Lischke, A. Awny, and L. Zimmermann, "SiGe BiCMOS for optoelectronics," ECS Transactions, vol. 75, no. 8, pp. 121–139, 2016.

[40] S. Lischke, D. Knoll, L. Zimmermann, Y. Yamamoto, M. Fraschke, A. Trusch, A. Krüger, M. Kroh, and B. Tillack, "Low dark current Ge PIN photodiode for a high-performance, photonic BiCMOS process for radio-over-fiber applications," in IEEE Photonics Conference 2012, Sept 2012, pp. 628–629.

[41] S. Lischke, D. Knoll, L. Zimmermann, A. Scheit, C. Mai, A. Trusch, K. Voigt, M. Kroh, R. Kurps, P. Ostrovskyy, Y. Yamamoto, F. Korndörfer, A. Peczek, G. Winzer, and B. Tillack, "High-speed, waveguide Ge PIN photodiodes for a photonic BiCMOS process," in 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Sept 2014, pp. 29–32.

[42] S. Burger, L. Zschiedrich, J. Pomplun, M. Blome, and F. Schmidt, "Advanced finite-element methods for design and analysis of nanooptical structures: Applications," in SPIE OPTO. International Society for Optics and Photonics, 2013, pp. 864 205–864 205.

[43] B. Wohlfeil, S. Burger, C. Stamatiadis, J. Pomplun, F. Schmidt, L. Zimmermann, and K. Petermann, "Numerical simulation of grating couplers for mode multiplexed systems," in SPIE OPTO. International Society for Optics and Photonics, 2014, pp. 89 880K–89 880K.

[44] B. Wohlfeil, C. Stamatiadis, M. Jäger, L. Zimmermann, S. Burger, and K. Petermann, "Integrated optical fiber grating coupler on SOI for the excitation of several higher order fiber modes," in 2014 The European Conference on Optical Communication (ECOC), Sept 2014, pp. 1–3.

[45] S. Burger, P. Gutsche, M. Hammerschmidt, S. Herrmann, J. Pomplun, F. Schmidt, B. Wohlfeil, and L. Zschiedrich, "Hp-finite-elements for simulating electromagnetic fields in optical devices

with rough textures," in SPIE Optical Systems Design. International Society for Optics and Photonics, 2015, pp. 96 300S–96 300S.

[46] J. Pomplun, S. Burger, L. Zschiedrich, P. Gutsche, and F. Schmidt, "Method for fast computation of angular light scattering spectra from 2D periodic arrays," in SPIE Advanced Lithography. International Society for Optics and Photonics, 2016, pp. 977 839–977 839.

[47] E. Krune, "Performance analysis of low jitter high-speed photonic analog-to-digital converters in silicon photonics," dissertation, Technische Universitaet Berlin, 2017.

[48] G. T. Reed and A. P. Knights, Silicon photonics: an introduction. John Wiley & Sons, 2004.

[49] K. Yamada, "Silicon photonics ii: Components and integration," 2011.

[50] R. Soref and B. Bennett, "Electrooptical effects in silicon," IEEE Journal of Quantum Electronics, vol. 23, no. 1, pp. 123–129, Jan 1987.

[51] M. Nedeljkovic, R. Soref, and G. Z. Mashanovich, "Free-carrier electrorefraction and electroabsorption modulation predictions for silicon over the 1-14-μm infrared wavelength range," IEEE Photonics Journal, vol. 3, no. 6, pp. 1171–1180, Dec 2011.

[52] E. Krune, K. Jamshidi, K. Voigt, L. Zimmermann, and K. Petermann, "Jitter analysis of optical clock distribution networks in silicon photonics," Journal of Lightwave Technology, vol. 32, no. 22, pp. 4378–4385, Nov 2014.

[53] Q. Lin, O. J. Painter, and G. P. Agrawal, "Nonlinear optical phenomena in silicon waveguides: Modeling and applications," Opt. Express, vol. 15, no. 25, pp. 16 604–16 644, Dec 2007. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-15-25-16604

[54] J. Komma, C. Schwarz, G. Hofmann, D. Heinert, and R. Nawrodt, "Thermo-optic coefficient of silicon at 1550 nm and cryogenic temperatures," Applied Physics Letters, vol. 101, no. 4, p. 041905, 2012. [Online]. Available: http://dx.doi.org/10.1063/1.4738989

[55] G. Cocorullo, F. Della Corte, and I. Rendina, "Temperature dependence of the thermo-optic coefficient in crystalline silicon between room temperature and 550 K at the wavelength of 1523 nm," Applied physics letters, vol. 74, no. 22, pp. 3338–3340, 1999.

[56] K. Voigt, L. Zimmermann, G. Winzer, H. Tian, B. Tillack, and K. Petermann, "C -band optical 90° hybrids in silicon nanowaveguide technology," IEEE Photonics Technology Letters, vol. 23, no. 23, pp. 1769–1771, Dec 2011.

[57] L. B. Soldano and E. C. M. Pennings, "Optical multi-mode interference devices based on self-imaging: principles and applications," Journal of Lightwave Technology, vol. 13, no. 4, pp. 615–627, Apr 1995.

[58] D.-X. Xu, P. Cheben, D. Dalacu, A. Delâge, S. Janz, B. Lamontagne, M.-J. Picard, and W. N. Ye, "Eliminating the birefringence in silicon-on-insulator ridge waveguides by use of cladding stress," Optics letters, vol. 29, no. 20, pp. 2384–2386, 2004.

[59] M. Huang and X. Yan, "Thermal-stress effects on the temperature sensitivity of optical waveguides," JOSA B, vol. 20, no. 6, pp. 1326–1333, 2003.

[60] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, and J. M. Fédéli, "Zero-bias 40Gbit/s germanium waveguide photodetector on silicon," Optics express, vol. 20, no. 2, pp. 1096–1101, 2012.

[61] K. Kato, "Ultrawide-band/high-frequency photodetectors," IEEE transactions on Microwave Theory and Techniques, vol. 47, no. 7, pp. 1265–1281, 1999.

[62] A. Berti and S. Baranowski, "Self-aligned cobalt silicide on MOS integrated circuits," Apr. 7 1998, uS Patent 5,736,461. [Online]. Available: http://www.google.com/patents/US5736461

[63] T. Canneaux, D. Mathiot, J.-P. Ponpon, and Y. Leroy, "Modeling of phosphorus diffusion in Ge accounting for a cubic dependence of the diffusivity with the electron concentration," Thin Solid Films, vol. 518, no. 9, pp. 2394 – 2397, 2010, proceedings of the {EMRS} 2009 Spring Meeting Symposium I: Silicon and germanium issues for future {CMOS} devices. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0040609009016435

[64] H. A. Haus, J. G. Fujimoto, and E. P. Ippen, "Structures for additive pulse mode locking," JOSA B, vol. 8, no. 10, pp. 2068–2076, 1991.

[65] H. A. Haus and A. Mecozzi, "Noise of mode-locked lasers," IEEE Journal of Quantum Electronics, vol. 29, no. 3, pp. 983–996, Mar 1993.

[66] R. Paschotta, "Noise of mode-locked lasers (part i): numerical model," Applied Physics B: Lasers and Optics, vol. 79, no. 2, pp. 153–162, 2004.

[67] ——, "Noise of mode-locked lasers (part ii): timing jitter and other fluctuations," Applied Physics B: Lasers and Optics, vol. 79, no. 2, pp. 163–173, 2004.

[68] D. Li, U. Demirbas, A. Benedick, A. Sennaroglu, J. G. Fujimoto, and F. X. Kärtner, "Attosecond timing jitter pulse trains from semiconductor saturable absorber mode-locked Cr: LiSAF lasers," Optics express, vol. 20, no. 21, pp. 23 422–23 435, 2012.

[69] A. Schlatter, B. Rudin, S. Zeller, R. Paschotta, G. Spühler, L. Krainer, N. Haverkamp, H. Telle, and U. Keller, "Nearly quantum-noise-limited timing jitter from miniature Er: Yb: glass lasers," Optics letters, vol. 30, no. 12, pp. 1536–1538, 2005.

[70] L. Banchi, F. Rossi, M. Ferianis, A. Bogoni, L. Potì, and P. Ghelfi, "Synchronization of 3 GHz repetition rate harmonically mode-locked fiber laser for optical timing applications," Proc. DIPAC 2007, 2007.

[71] A. Haboucha, W. Zhang, T. Li, M. Lours, A. N. Luiten, Y. L. Coq, and G. Santarelli, "Optical-fiber pulse rate multiplier for ultralow phase-noise signal generation," Opt. Lett., vol. 36, no. 18, pp. 3654–3656, Sep 2011. [Online]. Available: http://ol.osa.org/abstract.cfm?URI=ol-36-18-3654

[72] M. J. Hoskins and D. R. Williams, "High-speed SiGe HBT track-and-hold," in Proceedings of the 20th IEEE Instrumentation Technology Conference (Cat. No.03CH37412), vol. 2, May 2003, pp. 1448–1453 vol.2.

[73] Y. Lu, W.-M. L. Kuo, X. Li, R. Krithivasan, J. D. Cressler, Y. Borokhovych, H. Gustat, B. Tillack, and B. Heinemann, "An 8-bit, 12 GSample/sec SiGe track-and-hold amplifier," in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2005., Oct 2005, pp. 148–151.

[74] S. Shahramian, A. C. Carusone, and S. P. Voinigescu, "Design methodology for a 40-GSamples/s track and hold amplifier in 0.18- μm SiGe BiCMOS technology," IEEE Journal of Solid-State Circuits, vol. 41, no. 10, pp. 2233–2240, Oct 2006.

[75] P. Zammit, I. Grech, J. Micallef, and E. Gatt, "A 10 Gsamples/s SiGe track-and-hold amplifier with 8-bit resolution," in 2007 14th IEEE International Conference on Electronics, Circuits and Systems, Dec 2007, pp. 1232–1235.

[76] X. Li, W. M. L. Kuo, and J. D. Cressler, "A 40 GS/s SiGe track-and-hold amplifier," in 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Oct 2008, pp. 1–4.

[77] F. Cannone, D. Cascella, G. Avitabile, and G. Coviello, "A high bandwidth 11-bit 1.5GS/s track and hold amplifier in 0.25 μm SiGe BiCMOS," in 2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Sept 2012, pp. 49–52.

[78] F. Cannone, G. Avitabile, and G. Coviello, "A 11-bit track and hold amplifier in 0.25 μm SiGe BiCMOS for RF sampling receivers," in 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Aug 2013, pp. 792–795.

[79] D. Lal, M. Abbasi, and D. S. Ricketts, "A compact, high linearity 40GS/s track-and-hold amplifier in 90nm SiGe technology," in 2015 IEEE Custom Integrated Circuits Conference (CICC), Sept 2015, pp. 1–4.

[80] A. Meyer, P. Desgreys, H. Petit, B. Louis, and R. CorbiÃ©re, "Single-ended/differential 2.5-GS/s double switching track-and-hold amplifier with 26ghz bandwidth in SiGe BiCMOS technology," in 2016 IEEE MTT-S International Microwave Symposium (IMS), May 2016, pp. 1–3.

[81] J. Li, H. Wu, N. Ning, S. Wu, and R. Guo, "An improved switched-emitter-follower for high-resolution GS/s-rate track-and-hold amplifiers," in 2016 IEEE International Nanoelectronics Conference (INEC), May 2016, pp. 1–2.

[82] R. Paschotta, Encyclopedia of Laser Physics and Technology. Wiley-VCH, Dec. 2008. [Online]. Available: https://www.rp-photonics.com/encyclopedia.html

[83] M. Teich and B. Saleh, "Fundamentals of photonics 2nd edn," Canada, Wiley Interscience, 2007.

[84] B. Razavi, "Problem of timing mismatch in interleaved ADCs." in CICC. Citeseer, 2012, pp. 1–8.

[85] C. Schiller and P. Byrne, "A 4-GHz 8-b ADC system," IEEE Journal of Solid-State Circuits, vol. 26, no. 12, pp. 1781–1789, Dec 1991.

[86] R. Shimon, B. Asay, D. Dascher, K. Griggs, C. Rehorn, M. Adamski, E. Ehlers, C. Hutchinson, and B. Doerr, "InP IC technology powers Agilent's Infiniium 90000 X-Series real time oscilloscope," in 2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Oct 2010, pp. 1–4.

[87] Q. Deng, L. Liu, X. Li, and Z. Zhou, "Arbitrary-ratio 1× 2 power splitter based on asymmetric multimode interference," Optics letters, vol. 39, no. 19, pp. 5590–5593, 2014.

[88] F. Quinlan, T. M. Fortier, H. Jiang, and S. A. Diddams, "Analysis of shot noise in the detection of ultrashort optical pulse trains," JOSA B, vol. 30, no. 6, pp. 1775–1785, 2013.

[89] F. Quinlan, T. M. Fortier, H. Jiang, A. Hati, C. Nelson, Y. Fu, J. Campbell, and S. Diddams, "Exploiting shot noise correlations in the photodetection of ultrashort optical pulse trains," Nature Photonics, vol. 7, no. 4, pp. 290–293, 2013.

[90] J.-D. Descênes, "Non-stationary photodetection shot noise in frequency combs: a signal processing perspective," Ph.D. dissertation, Laval University, 2014.

[91] S. Mendel and C. Vogel, "A compensation method for magnitude response mismatches in two-channel time-interleaved analog-to-digital converters," in 2006 13th IEEE International Conference on Electronics, Circuits and Systems, Dec 2006, pp. 712–715.

[92] ——, "On the compensation of magnitude response mismatches in M-channel time-interleaved ADCs," in 2007 IEEE International Symposium on Circuits and Systems, May 2007, pp. 3375–3378.

[93] P. Satarzadeh, B. C. Levy, and P. J. Hurst, "Bandwidth mismatch correction for a two-channel time-interleaved A/D converter," in 2007 IEEE International Symposium on Circuits and Systems, May 2007, pp. 1705–1708.

[94] M. Seo, M. Rodwell, and U. Madhow, "Generalized blind mismatch correction for two-channel time-interleaved A-to-D converters," in 2007 IEEE International Conference on Acoustics, Speech and Signal Processing - ICASSP '07, vol. 3, April 2007, pp. III–1505–III–1508.

[95] M. Seo and M. Rodwell, "Generalized blind mismatch correction for a two-channel time-interleaved ADC: Analytic approach," in 2007 IEEE International Symposium on Circuits and Systems, May 2007, pp. 109–112.

[96] H. Johansson, "A polynomial-based time-varying filter structure for the compensation of frequency-response mismatch errors in time-interleaved ADCs," IEEE Journal of Selected Topics in Signal Processing, vol. 3, no. 3, pp. 384–396, June 2009.

[97] M. Agrawal and R. Nema, "Compensating frequency response mismatches in time interleaved analog to digital converters," International Journal of Emerging Technology and Advanced Engineering, vol. 2, pp. 78–82, 2012.

[98] O. Landolt, "Electronic circuit for optical control of a flip-flop," Aug. 25 2015, uS Patent 9,118,328.

[99] S. Levantino, L. Romano, S. Pellerano, C. Samori, and A. L. Lacaita, "Phase noise in digital frequency dividers," IEEE Journal of Solid-State Circuits, vol. 39, no. 5, pp. 775–784, May 2004.

[100] B. Razavi, Design of integrated circuits for optical communications. John Wiley & Sons, 2012.

[101] Erbium Fiber Amplifiers EAR-10K-C Datasheet, IPG Photonics, 05 2012.

[102] InfinityQuad Datasheet, Cascade Microtech, 2015. [Online]. Available: https://www.cascademicrotech.com/files/InfinityQuad-DS.pdf

[103] Double Arrow 180 degree Hybrid Model 4010124 Datasheet, Krytar. [Online]. Available: https://krytar.com/pdf/4010124.pdf

[104] Infiniium DCA-X 86100D Wide-Bandwidth Oscilloscope Mainframe and Modules Datasheet, Keysight Technologies. [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/5990-5824EN.pdf

[105] R&S FSUP Signal Source Analyzer Specifications, Rohde & Schwarz GmbH & Co. KG, 5 2011, version 06.03. [Online]. Available: https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/FSUP_dat-sw_en.pdf

[106] SHF810 Broadband Amplifier Datasheet, SHF Communication Technologies AG, 2007. [Online]. Available: https://www.shf.de/wp-content/uploads/datasheets/datasheet_shf_810.pdf

[107] J. A. McNeill and D. Ricketts, The designer's guide to jitter in ring oscillators. Springer Science & Business Media, 2009.

[108] C. Azeredo-Leme, "Clock jitter effects on sampling: A tutorial," IEEE Circuits and Systems Magazine, vol. 11, no. 3, pp. 26–37, 2011.

[109] B. Brannon, Application Note AN-756: Sampled Systems and the Effect of Clock Phase Noise and Jitter, Analog Devices, 12 2004, rev. 0. [Online]. Available: http://www.analog.com/media/en/technical-documentation/application-notes/AN-756.pdf

[110] J. Breitbarth and J. Koebel, "Additive (residual) phase noise measurement of amplifiers, frequency dividers and frequency multipliers," Microwave Journal, vol. 51, no. 6, p. 66, 2008.

[111] P. R. Gray, Analysis and Design of Analog Integrated Circuits, 5th ed. Wiley Publishing, 2009.

[112] R&S SMW200A Vector Signal Generator Specifications, Rohde & Schwarz GmbH & Co. KG, 12 2016, version 04.04. [Online]. Available: https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/SMW200A_dat-sw_en_3606-8037-22_v0404.pdf

[113] WaveMaster 8 Zi-B Oscilloscopes Datasheet, Teledyne LeCroy, 1 2016. [Online]. Available: http://cdn.teledynelecroy.com/files/pdf/wavemaster-8zi-b-datasheet.pdf

[114] 180 degree Hybrid JSO-50-471/6S Datasheet, Pulsar Microwave Corporation. [Online]. Available: https://www.pulsarmicrowave.com/spec_sheets/JSO-50-471-6S.pdf

[115] S. A. Wartenberg, RF measurements of die and packages. Artech house, 2002.

[116] Y. C. Jenq, "Digital spectra of nonuniformly sampled signals: theories and applications-measuring clock/aperture jitter of an A/D system," IEEE Transactions on Instrumentation and Measurement, vol. 39, no. 6, pp. 969–971, Dec 1990.

[117] Y. Langard, J. L. Balat, and J. Durand, "An improved method of ADC jitter measurement," in Test Conference, 1994. Proceedings., International, Oct 1994, pp. 763–770.

[118] G. Chiorboli and M. Fontanili, "Cross-correlation noise measurements in A/D converters," IEEE Transactions on Instrumentation and Measurement, vol. 48, no. 6, pp. 1282–1286, Dec 1999.

[119] G. Chiorboli, M. Fontanili, and C. Morandi, "A new method for estimating the aperture uncertainty of A/D converters," in Instrumentation and Measurement Technology Conference, 1997.

IMTC/97. Proceedings. Sensing, Processing, Networking., IEEE, vol. 1, May 1997, pp. 632–635 vol.1.

[120] G. Chiorboli, "Sub-picosecond aperture-uncertainty measurements [ADCs]," IEEE Transactions on Instrumentation and Measurement, vol. 51, no. 5, pp. 1039–1044, Oct 2002.

[121] E. Cetin and T. Kuyel, "Hundred femtosecond jitter measurement using dual-channel ADC with imprecise clock stimulus," Electronics Letters, vol. 48, no. 24, pp. 1525–1526, November 2012.

[122] M. Wu, Z. Liu, L. Xu, and D. Chen, "Accurate and cost-effective technique for jitter and noise separation based on single-frequency measurement," Electronics Letters, vol. 52, no. 2, pp. 106–107, 2016.

[123] D. M. Hummels, W. Ahmed, and F. H. Irons, "Measurement of random sample time jitter for ADCs," in Proceedings of ISCAS'95 - International Symposium on Circuits and Systems, vol. 1, April 1995, pp. 708–711 vol.1.

[124] T. Schweiger, B. Krueger, and F. Wiedmann, "Cyclostationary stochastic jitter measurement method with uncertainty prediction," IEEE Transactions on Instrumentation and Measurement, vol. 66, no. 9, pp. 2371–2379, Sept 2017.

[125] LabMaster 10 Zi-A High Bandwidth Modular Oscilloscopes Datasheet, Teledyne LeCroy, 1 2016. [Online]. Available: http://cdn.teledynelecroy.com/files/pdf/labmaster-10zi-a-datasheet.pdf

[126] Infiniium Z-Series Oscilloscopes Datasheet, Keysight Technologies. [Online]. Available: https://literature.cdn.keysight.com/litweb/pdf/5991-3868EN.pdf

[127] MSO/DPO70000 Series Datasheet, Tektronix. [Online]. Available: https://www.tek.com/link-click-count?url=http%3A//download.tek.com/datasheet/DPO70000SX-Digital-Oscilloscope-Datasheet-55W3066218.pdf&nid=75816

[128] Digital Serial Analyzer Sampling Oscilloscope - DSA8200 Datasheet, Tektronix, 8 2011. [Online]. Available: http://www.tek.com/sites/tek.com/files/media/media/resources/85W_17654_20.pdf

[129] R&S SMB100A RF and Microwave Signal Generator Specifications, Rohde & Schwarz GmbH & Co. KG, 7 2016, version 09.00. [Online]. Available: https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/service_support_30/SMB100A_dat-sw_en_5213-8396-22_v0900.pdf

[130] C. Kopp, S. Bernabá, B. B. Bakir, J. M. Fedeli, R. Orobtchouk, F. Schrank, H. Porte, L. Zimmermann, and T. Tekin, "Silicon photonic circuits: On-CMOS integration, fiber optical coupling, and packaging," IEEE Journal of Selected Topics in Quantum Electronics, vol. 17, no. 3, pp. 498–509, May 2011.

Curriculum Vitae

Personal Information

Name:	Benjamin Krüger
Born:	June 20, 1986 in Böblingen
Nationality:	German

Education

2017 - now:	Postdoctoral Researcher at the University of Stuttgart and the University of Stanford (Prof. Dr. habil. Jörg Schulze, Prof. Dr. Boris Murmann)
2013 - 2016:	PhD research at Rohde & Schwarz GmbH & Co. KG in Munich and the University of Stuttgart (Prof. Dr. habil. Jörg Schulze)
2013:	Diploma thesis: “Implementation of a NOAA weather satellite receiver algorithm with a zero-IF architecture” (Prof. Dr.-Ing. Bin Yang)
2007 - 2013:	Academic studies of Electrical Engineering and Information Technology at the University of Stuttgart Diploma
1997 - 2006:	Gymnasium in den Pfarrwiesen in Sindelfingen German Abitur