Hybrid System-in-Foil Integration and Interconnection Technology based on Adaptive Layout Technique

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to Baba,
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ABSTRACT

The Hybrid System-in-Foil (HySiF) including ultra-thin embedded silicon chips in polymer foil in combination with large area electronics, such as organic thin-film transistors (OTFTs), capacitive sensors, antennas, and strain gauges is a promising technological solution for the next generation of consumers in the field of flexible electronics. This work mainly contributes to developing the CMOS-compatible process flow to embed and interconnect ultra-thin silicon chips inside polymer foil in combination with other devices. The fine-pitch (10 µm) chip to foil interconnectivity is pursued by relocating the active pads on a silicon chip to the foil periphery, therefore, saving silicon area and costs and providing a far larger I/O count is possible.

The Chip-Film Patch (CFP) concept is suitable for HySiF technology. However, limitations often exist due to restriction in processing methods and incompatibility of the material with an IC processing fabrication line. These issues and corresponding solutions are treated in this thesis. Besides optimization of the already published concept of two-polymer CFP and bringing that to fabrication level, key aspects of this dissertation are:

– The process flow development of face-up low-stress CFP technology to avoid the coefficient of thermal expansion (CTE) mismatch between embedded silicon chips, deposited polymer layers, and silicon substrate carrier.

– The fabrication process of the face-down CFP technology to minimize topography on top of the embedded chip, thus, reaching finer pitch and pad size. Embedding devices with different thickness and chip backside processing are other advantages of the face-down CFP technology.

– The challenge of unwanted rotation and positioning offset after chip embedding on foil using an adaptive layout technique based on laser direct writer lithography. Using the adaptive layout technique, wafer level embedding and interconnecting of multiple silicon chips as a HySiF become possible. The overlay accuracy below 1 µm in x-axis and y-axis for any arbitrary position of the embedded chip is achieved.

– The thermal behavior of power chips embedding in polymer foil and self-heating phenomenon and corresponding cooling methods, such as heat spreader on the chip's backside.

– The CMOS-compatible process flow to fabricate a rigid mm-wave patch antenna and flexible dipole antenna in polymer foil with antennas that are fabricated, measured, and high-frequency properties of the polymer packages are extracted.

Keywords: Chip-Film Patch, HySiF, Adaptive layout technique, CTE mismatch

KURZFASSUNG

Das Hybride System in Folie (HySiF) mit ultradünnen eingebetteten Siliziumchips in Polymerfolie in Kombination mit großflächiger Elektronik, wie zum Beispiel organische Dünnschichttransistoren (OTFTs), kapazitive Sensoren auf Folien, Antennen und Dehnungsmessstreifen sind vielversprechende technologische Lösungen für die nächste Generation von Anwendungen im Bereich der flexiblen Elektronik. Der Fine-Pitch-Chip (10 µm Pitch) zur Untersuchung der Verbindungsfähigkeit wird durch Verlagerung der aktiven Pads vom Siliziumchip zur Folienperipherie realisiert. Somit ist es möglich, Siliziumfläche und Kosten einzusparen und eine viel größere Anzahl I/O bereitzustellen. Die Chip-Film-Patch (CFP) Technologie ist für die Realisierung von HySiF geeignet. Häufig bestehen jedoch Einschränkungen aufgrund der Verarbeitungsverfahren und der Kompatibilität des Materials mit der IC Fertigungslinie. Diese Fragen und entsprechende Lösungen werden in dieser Arbeit diskutiert. Neben der Optimierung des bereits publizierten Konzepts des Zwei-Polymer-CFP und der damit verbundenen Herstellung werden die nachfolgenden wesentlichen Aspekte dieser Dissertation genannt:

– Die Prozessflussentwicklung der "Face-up low-CTE CFP-Technologie" zur Vermeidung von temperaturbedingter Verspannung zwischen den eingebetteten Siliziumchips, den abgeschiedenen Polymerschichten und dem Silizium-Substratträger.

– Der Grundlagenprozess für "Face-down CFP-Technologie" zur Minimierung der Topografie auf dem eingebetteten Chip und zur möglichen Erzielung einer feineren Metallisierung und Padgröße. Einbettungsvorrichtungen mit unterschiedlicher Dicke und Chiprückseiten-Verarbeitung sind weitere Anwendungen dieser Face-down CFP-Technologie.

– Der Umgang mit unerwünschtem Verdrehen und Positionierungsoffsets nach der Chipeinbettung auf Folie durch eine adaptive Layout-Technik unter Verwendung eines Laserdirektschreibers. Somit können in einer Wafer-Ebene mehrere Siliziumchips als HySiF eingebettet und miteinander verbunden werden. Eine Plaziergenauigkeit unter 1 µm in x-Achse und y-Achse für jede beliebige Position auf dem eingebetteten Chip wird erreicht.

– Untersuchung des thermischen Verhaltens von in Polymerfolie eingebetteten und sich selbst erhitzenden Leistungschips und entsprechende passive Kühlverfahren, wie die Wärmeverteilung über eine Rückseitenmetallisierung.

–Der CMOS-kompatible Prozessablauf zur Herstellung einer Millimeterwellen Patch Antenne und einer flexiblen Dipolantenne in Polymerfolie. Die Antennen werden hergestellt, gemessen und die Hochfrequenzeigenschaften des CFPs werden extrahiert.

Schlagwörter: Chip-Film Patch, HySiF, Adaptive Layout Technik, CTE-Mismatch

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NOMENCLATURE

ACA	Anisotropic Conductive Adhesive
AlSiCu	Aluminum-Silicon-Copper
Au	Gold
BCB	Benzocyclobutene
BGA	Ball Grid Array
BG	Back Grinding
BOX	Buried Oxide
CF_4	Tetrafluoromethane
CFP	Chip-Film Patch
CMOS	Complementary Metal-Oxide Semiconductor
CMP	Chemical-Mechanical-Polishing
CoO	Cost-of-Ownership
CPS	Cyber-Physical System
CSP	Chip-Scale Package
CTE	Coefficient of Thermal Expansion
DAF	Die Attach Film
DBG	Dicing-before-Grinding

DbyT	Dicing-by-Thinning
DIP	Dual-in-line Package
DI	Deionized
DLR	Dynamic Release Layer
DOP	Degree Of Planarization
DPA	Differential Power Amplifier
DUT	Device Under Test
EBR	Edge Bead Removal
ECT	Embedded Component Technology
EC	European Commission
FEM	Finite Element Method
FPC	Flexible Printed Circuit
HBT	Heterojunction Bipolar Transistor
HDI	High-Density Interconnect
HMDS	Hexamethyldisilazane
HySiF	Hybrid System-in-Foil
I/O	Input/Output
IC-CAP	Integrated Circuit Characterization and Analysis Program
ICP	Inductively Coupled Plasma
ICT	Information and Communication Technology
IMS	Institute for Microelectronic Stuttgart
IoT	Internet of Things
IPA	Isopropyl Alcohol
IPD	In-Plane Distortion
ITRS	International Semiconductor Roadmap for Semiconductors

KGD	Known Good Die
LAE	Large Area Electronic
LCP	Liquid Crystal Polymer
MCM	Multi-Chip Modules
MCP	Multi-Chip Package
MEMS	Micro-Electro-Mechanical Systems
MPI-SSR	Max Planck Institute for Solid-State Research
MtM	More than Moore
N_2	Nitrogen
NCA	Non-Conductive Adhesive
NFC	Near-Field Communication
Ni	Nickel
O_2	Oxygen
OTFT	Organic Thin-Film Transistor
OT	Operational Technology
PA	Power Amplifier
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEN	Polyethylene-naphthalate
PET	Polyethyleneterephthalate
PGA	Pin Grid Array
PGMEA	1-Methoxy-2-propanol Acetate
PiP	Package-in-Package
PI	Polyimide
PoP	Package-on-Package

PVD	Physical Vapor Deposition
QFP	Quad-Flat Package
R2R	Reel-to-Reel
RCC	Resin-Coated-Copper
RFID	Radio Frequency Identification Device
RF	Radio Frequency
RH	Relative Humidity
RIE	Reactive Ion Etching
SCP	Single-Chip Packaging
SEM	Scanning Electron Microscope
SiF	System-in-Foil
SiP	System-in-Package
Si	Silicon
SMT	Surface Mount Technology
SoC	System-on-Chip
SOI	Silicon-On-Insulator
TCT	Thermal Cycling Test
TGP	Thermal Ground Plate
THST	Thermal and Humidity Storage Test
TLM	Transmission Line Method
TLR	Technology Readiness Levels
TLR	Thru-Line-Reflect
TSV	Through Silicon Via
UTCOF	Ultra-Thin Chip on Flex
UTCP	Ultra-Thin Chip Package

UTFP Ultra-Thin Film Package

VNA Vector Network Analyzer

WLP Wafer Level Packaging

CHAPTER 1

MOTIVATION

> "We can know only that we know nothing. And that is the highest degree of human wisdom."
>
> — Leo Tolstoy, War and Peace

The world of semiconductor technology is evolving rapidly towards miniaturization and , at the same time, increasing I/O count in the chip. However, the crystalline structure of silicon may limit the device downscaling at some point in progress [1]. Consequently, following Moore's prediction with available technologies is difficult [2]. Therefore, the International Semiconductor Roadmap for Semiconductors (ITRS) considers applications of silicon technology named "More than Moore (MtM)" which follows the basic silicon progress but requires less downsizing of the minimum feature size ("More Moore") [3]. The MtM follows recent demands, such as radio frequency (RF), power, sensor/actuator, and micro-electro-mechanical systems (MEMS) [4]. It developes the possibility to incorporate digital and analog functionality into one compact system [3]. In this case, the electronic packaging world is progressing in the direction of smaller size, less weight, lower costs, and higher functionality while accelerating the speed of the MtM progress.

By increasing demand for portable, wearable, and implantable electronics and sensor systems, the conventional mechanical rigid packages have to be replaced by flexible and bendable equivalent packages. Flexible electronics are large area electronics, including the flexible substrate, integrating components, and an encapsulation with a great potential towards bendability and flexibility [1], [5], [6].

The organic or thin-film technologies with low-cost per unit area are great for large area electronics applications, such as displays, electronic papers, and foldable solar panels. Moreover, these large-area technologies have an inherent mechanical flexibil-

ity, making them suitable for flexible electronics. They, however, lack the integration and performance capabilities of silicon technology. On the other side, silicon technology has a high integration density, high circuit performance and, at the same time, high production cost per unit [7]. A logical trend in the technology development for flexible electronics is, therefore, to combine the merits of large-area electronics and microelectronics. This is possible by embedding and integrating ultra-thin, flexible silicon chips in flexible foil carriers which also include large-area components and structures, thus, arriving at a hybrid system-in-foil (HySiF) [8], [9]. For this purpose, silicon chips need to be thinned down ($\leq$ 20 µm) with high thickness uniformity and excellent mechanical stability in order to be integrated in the flexible substrate. Otherwise, the flexibility of the integrated system in polymeric foils would not be achieved.

The hybrid system-in-foil is an advanced generation of flexible electronics which mainly focuses on the integration and interconnection of the advanced CMOS chips in combination with sensors, MEMS, antennas, and organic thin-film transistors (OTFTs) which are fabricated on the chip or on polymer foil. The HySiF technology is still in the development phase and the challenges, such as the bendability of the final system and integration of the flexible system as an interposer in the other systems are under development. HySiF is ideal for the internet of things (IoT) and industry 4.0 for autonomous and intelligent flexible system fabrication.

This thesis presents the process development and characterization of the Chip-Film Patch (CFP) technology towards embedding and adaptively interconnecting multiple ultra-thin chips in combination with antennas, OTFTs, and sensors as a HySiF. It is organized into seven chapters, including this motivation. Chapter 2 gives a historical perspective and the general view of the conventional packaging and available flexible packaging techniques. Chapter 3 focuses on the Chip-Film Patch concept based on the various developed techniques. Materials, applications, processing methods, limitations, and corresponding solutions are discussed in this chapter. Chapter 4 presents the new method for multiple chip interconnection, named the adaptive layout technique, which employs the laser direct writer lithography tool for patterning, via opening, and metal interconnecting multiple chips inside polymer foil despite unwanted chip's offset and rotation. The organic thin-film transistors and ring oscillators fabrication on CFP in combination with embedded ultra-thin chips towards Hybrid Systems-in-Foil are also discussed. Chapter 5 is devoted to electrical, mechanical, thermal, and RF characterization of the system-in-foil (SiF). Chapter 6 introduces the various applications and corresponding demonstration which are proposed using CFP technology and the adaptive layout technique. Finally, in Chapter 7, a general conclusion and an outlook to future work is presented.

CHAPTER 2

OVERVIEW OF ELECTRONIC PACKAGING

> "A people without the knowledge of their past history, origin and culture is like a tree without roots."
>
> — Marcus Garvey

System-in-foil is an emerging technology in the field of flexible electronics in which complete systems including ultra-thin silicon chips, the arrays of sensors, antennas, and displays are integrated into polymer foil. An initial overview of the packaging history is given. Then, the system-in-foil (SiF) concept in the field of flexible electronics, basic material choices, different available technologies, corresponding restrictions, and challenges will be described. Additionally, the complex or hybrid systems-in-foil (HySiF) as the next generation of flexible electronics is discussed. Finally, the available technologies to fabricate ultra-thin silicon chips as a key element in flexible electronic technology are explained.

2.1 History of Conventional Packaging

Moore's law [10] has shown great success over the past 40 years in forecasting the progress in CMOS technology and reduction of device dimensions to microns and nanometers. But slowly, following Moore's prediction with available technologies will be difficult [2]. While microelectronic scientists work hard to pursue Moore's law, there is increasing progress and demand for the improvement of "More than Moore" (MtM) items that follow silicon advancements but do not necessarily follow Moore's law. RF, power, sensor/actuator, and micro-electro-mechanical systems (MEMS) as a system-in-package(SiP) are the group of examples for MtM world. The increasing need for

complex and heterogeneous system integration motivate the microelectronic communities to develop new technologies like advanced systems-on-chip (SoC). There is hope that MtM will expand rapidly and promote the possibilities to reach higher, faster and cheaper technologies to make people's life easier [4]. Therefore, the electronic packaging world is progressing fast to fulfill the requirements and meet the demands of end-use system applications. Packaging is defined as the last step to connect, seal, and interface ICs with each other and, at last, to the physical world. In the present electronics world, packaging's main focus is on portability, smaller size, low weight, low cost, ease of use, and functionality [11]. Such hardware products and their associated system-level developments have forced significant paradigm shifts in electronic packaging. This evolutionary steps and revolution are schematically illustrated in Fig 2.1. There, revolutionary shifts, like surface mount technology (SMT) as a package (to board) connectors or evolutionary progress, like Dual-in-line package (DIP) for single-chip packaging [11] are shown. One package, in general, should accomplish four important tasks: sealing and protecting the die from environmental effects such as moisture, transporting heat from the die to ambient in high power systems, transporting electrical power to die, and transporting signals between die and the outside world [12]. When considering these four tasks, the packaging technology is mainly categorized into two groups: single-chip and multi-chip packages. A brief description for each of them is following.

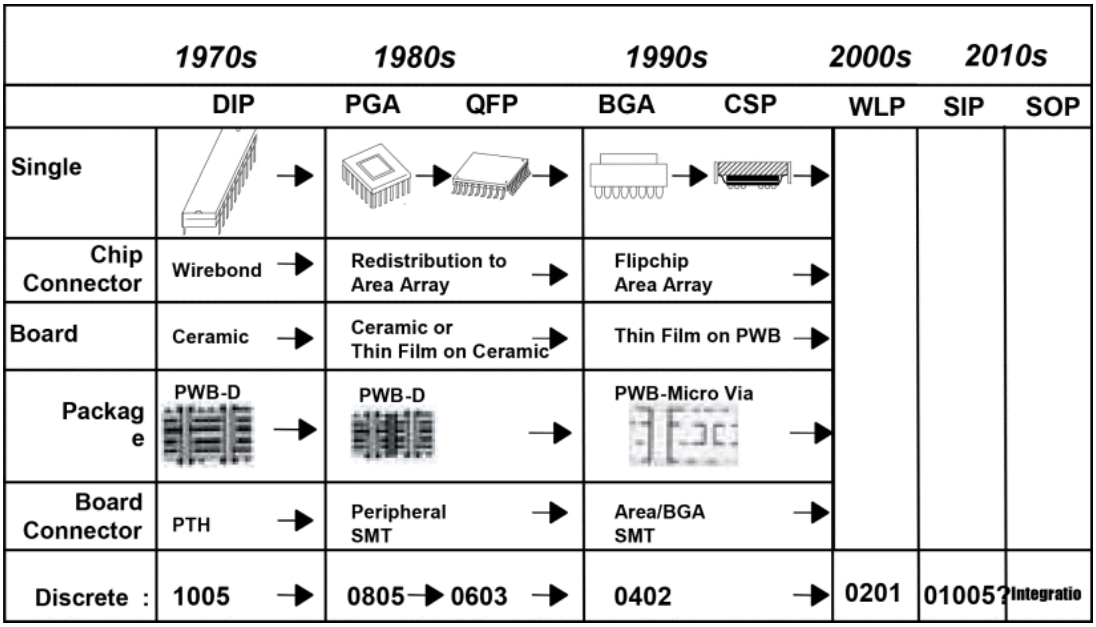


Figure 2.1: Package Evolution Trend [13].

2.1.1 Single-chip packaging (SCP)

There are various types of available technologies for single-chip packaging similar to ball grid array package (BGA), dual-in-line package (DIP), quad-flat package (QFP), pin grid arrays (PGA). However, they can be categorized into three groups: dual in-line packages, chip carriers, and grid arrays.

Dual-In-line Packages – DIP, a rectangular package style with two leads on two sides of the chip, which can be performed through a hole or surface mount technology (SMT).

Chip carrier – a rectangular or square package style with perimeter leads on all four sides, QFP is an example of this technology and can be performed by SMT.

Grid array – leads to an area array. In grid array technique, chips are being mounted directly to the below circuit board ("direct-chip attach"). In this technique, the chips with the higher density of I/O can be packed as well. In case of the through hole it is called pin grid array (PGA) and for SMT it is called ball grid array (BGA).

Each of them can be divided into the smaller groups based on the lead pitch, the number of I/O, thickness, size of packages, and application [12], [11]. The illustrations of three packages of single-chip packaging (SCP) families are shown in Fig 2.2. Chip-scale packages (CSP) are categorized in the grid array group and precisely as a micro-BGA which has a high-density area of interconnection and belongs to miniaturized series [14]. CSPs usually have the footprint areas with the size slightly bigger than the size of the chip ($\leq$ 1.5 times) [15]. Among CSP types, wafer level packaging (WLP) or in the other words, wafer level chip single packaging (WLCSP) receives lots of attention especially in the field of advanced mobile products [16]. The WLCSP offers the smallest footprint in IC packaging. Additionally, it shows high electrical and thermal performance after the direct solder interconnection [17].

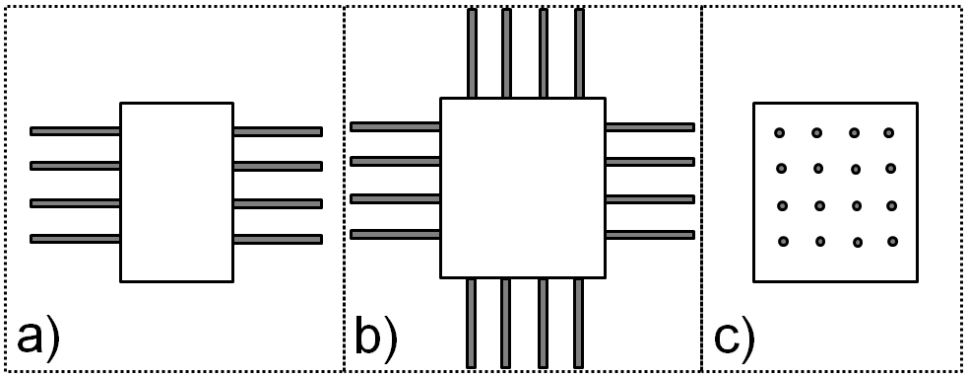


Figure 2.2: Illustration of three package families of single-chip packaging, a) dual-in-line packages (DIP), b) chip carrier, c) grid array.

2.1.2 Multi-chip packaging

The system-on-chip (SOC) refers to IC chips which include transistors, active and passive components in one individual chip. The SoC can also be called 2D integration. However, design complexities and a high cost of fabrication are some of the restrictions with SOC [13]. Therefore, the need for a higher level of integration has forced researchers to find better solutions for miniaturization, efficiency, integration, and low costs. One of the early solutions (1980's and 1990's) are multi-chip modules (MCM). MCM packages include multiple semiconductors and discrete components which are integrated and packed side by side onto a single substrate [17]. MCMs are classified into three primary categories, i.e, MCM-L, MCM-D, and MCM-C, for laminated, deposited, or ceramic substrates, respectively. Chips are mounted to these substrates either by wire bonding or by flip chipping [14], [17]. One of the continued extension of MCMs is "System-in-Package (SiP)" [18]. SiP consists of active devices, passive components and discrete devices which are integrated into a custom package. SiP can include another form of packages same as a package-in-package (PiP), package-on-package (PoP) and multi-chip package (MCP) [19]. In SiP, the active devices can be assembled using wire bonding or flip chipping [18]. PiP and PoP are two examples of 3D stacked packages [20] which are shown in Fig 2.3. One of the important benefits of PiP and PoP are known as "known good die (KGD)". PoP and PiP packages allow testing each individual prepacked semiconductor prior to the final 3D packaging [17]. One of the key technologies for 3D integration and WLP is through silicon via (TSV). TSV is a great candidate to be used instead of the wire bonding technology [21]. The fabrication of TSVs includes three significant steps: silicon via etching, via insulation and via metallization. The TSVs with reducing the size, cost, and shorter electrical connections are suitable for the recent demanding products like mobile phones, and cameras [22]. System-on-package (SOP) goes one step further than all the described technologies (SOC, SIP, and MCM). The SOP concepts rely on integrating various systems in one compact, thin, high performance, and low-cost package [13]. The improvement in SOP is because of using CMOS-silicon to integrate transistors, and the package mainly for RF, optical and digital integration in combination with integrated ICs in package [23]. The comparison of SOC, MCM, SIP, and SOP is given in Fig 2.4.

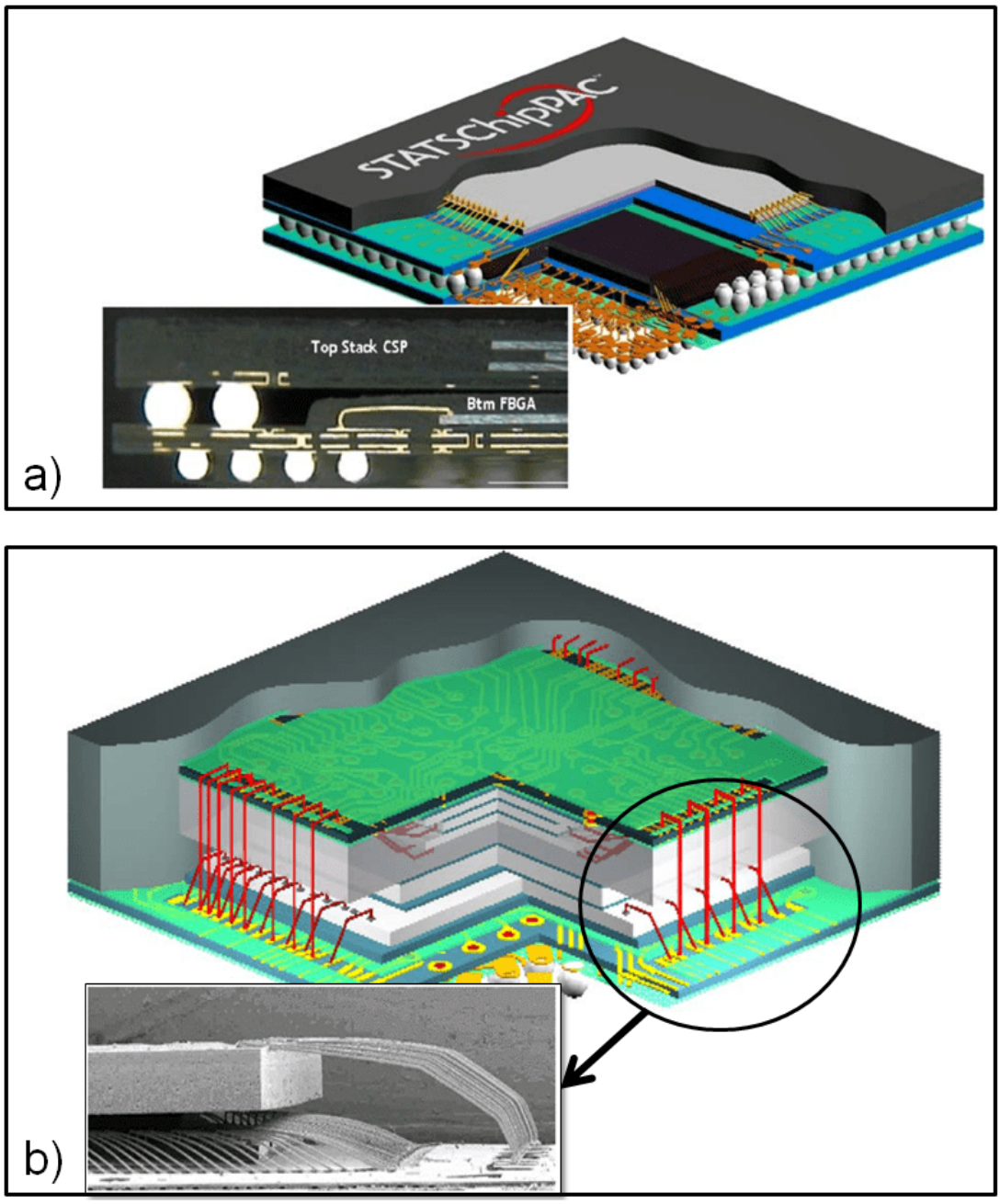


Figure 2.3: Illustration of PoP and PiP packages, a) stacked PoP structure. The bottom package which includes the logic devices is wire bonded, b) stacked PiP structure. The top package is stacked and wire bonded within the base package [20].

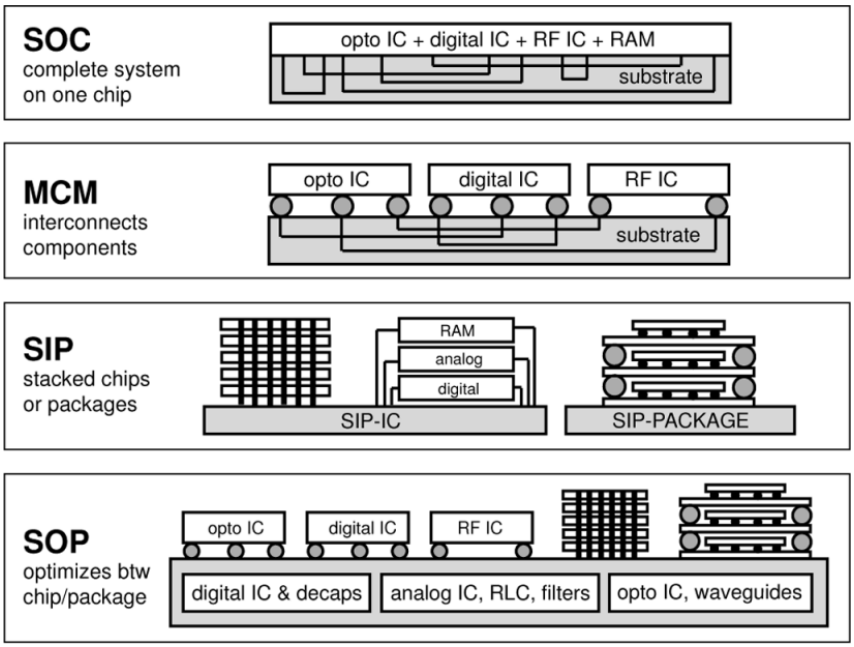


Figure 2.4: Comparison of SOC, MCM, SIP, and SOP [23].

2.2 Flexible Packaging

Flexible electronics have a great potential for bendable, stretchable, and rollable integrated systems. The smart patches, foldable displays, wearable devices, and disposable sensor devices are some of the applications for foil-based or flexible electronics [1], [5]. Furthermore, the flexibility of chip design, the bendable compact product and, low-cost assembly, bio-compatibility, and diversity of embedded modules are remarkable advantages of the recent developing technology [24]. In general, large area electronics (LAE) are made of (1) a substrate, (2) integrating components and (3) an encapsulation. To reach a flexible system, all the components should have some degree of flexibility. When fabricating flexible electronics, either the completed circuit is embedded in flexible electronic or the circuit is directly fabricated on the flexible substrate [25], [6]. Flexible substrates are one of the important factors in the final product costs and reliability of the integrated system. In general, three types of substrate materials are available for flexible packaging applications: metals, plastic (organic) polymers, and flexible glass [25].

Glass plates – with the thickness down to several 100 µm while having a smooth surface, low coefficient of thermal expansion (CTE), and resistance to chemical attacks. But, flexible glass is rigid and, therefore, handling them is difficult.

Plastic polymers – are cheap substrates. However, most of them have a high CTE mis-

match compared to silicon and are not robust to the moisture. Polyethylene terephthalate (PET) and polyethylene naphthalate are two examples of organic polymers (PEN) at low costs. Their process temperature is, however, limited to 150 - 200 °C. In contrast, Polyimide (PI) has a high glass transition temperature of 350 °C, but it absorbs moisture.

Metal Foils – with a thickness less than 125 µm are flexible substrates. Stainless steel is one of the metal foils which is commonly used in research. This substrate can tolerate the process temperature up to 1000 °C. However, stainless steel's surface roughness is high ($\sim$ 100 nm) and can cause failure in devices [1], [25].

In summary, each substrate can be chosen based on the application and requirements. However, to reduce cost, reel-to-reel (R2R) manufacturing in combination with the low-cost base material is a solution for the cost-effective production of flexible electronics [1]. Examples of flexible electronic systems are shown in Fig 2.5. The current trend in flexible electronics is polymer electronic systems. Polymer electronics is a low-cost process with high-density interconnects (HDI) which enable embedding ultra-thin complex silicon chips in combination with micro-electro-mechanical systems (MEMS), sensors, and passive devices in the same polymer substrate [26]. The silicon chips should be thin ($\leq$ 50 µm) to keep the system flexible and bendable. In following, the existing concepts for polymer + flexible electronics are discussed.

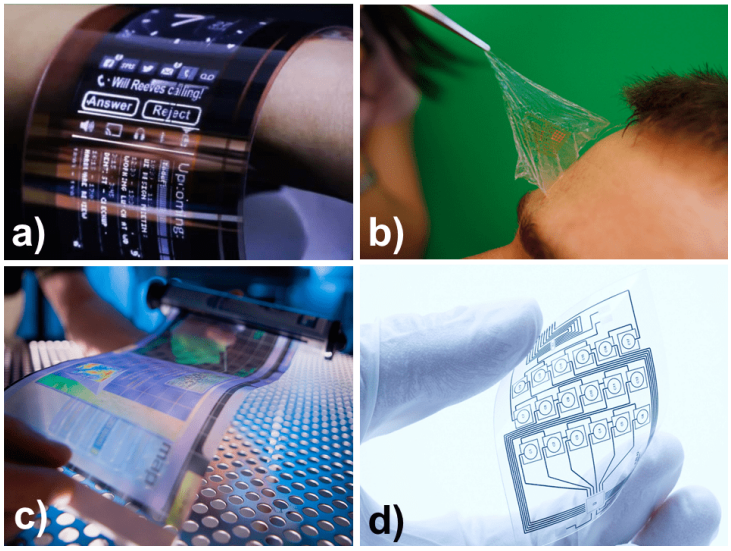


Figure 2.5: Examples of recent high functionality flexible electronic products and prototypes including, a) a wearable demonstrator [27], b) subtle sensors are like temporary tattoos. The radio frequency communication circuit on the foil can send data from a sensor on the skin to the user [28], c) HP's flexible display [29], d) printed electronics to sense applications, RFID tags, and monitoring [30].

2.2.1 Embedded Component Technology (ECT)

Embedded Chip-in-Flex with µ-via-contacts is a technology for direct chip embedding into a foil substrate technology, also known as Embedded Component Technology (ECT) [31]. The ECT technology mainly uses the printed circuit board (PCB) process. The ECT relies on using large substrates for the packaging and, therefore, saves cost [32].

Researchers at Fraunhofer IZM and TU Berlin are the innovators of ECT packaging. The schematic process flow of embedding thin chips using ECT is shown in Fig 2.6. As shown in the process flow depicted in Fig 2.6, in the beginning, the core substrate (either organic or non-organic) is prepared. The thin chips are bonded face-up or face-down on the substrate. The chip is attached to the substrate by using die attach films (DAF) or printable pastes [32]. The precise thickness of DAF plays an important role

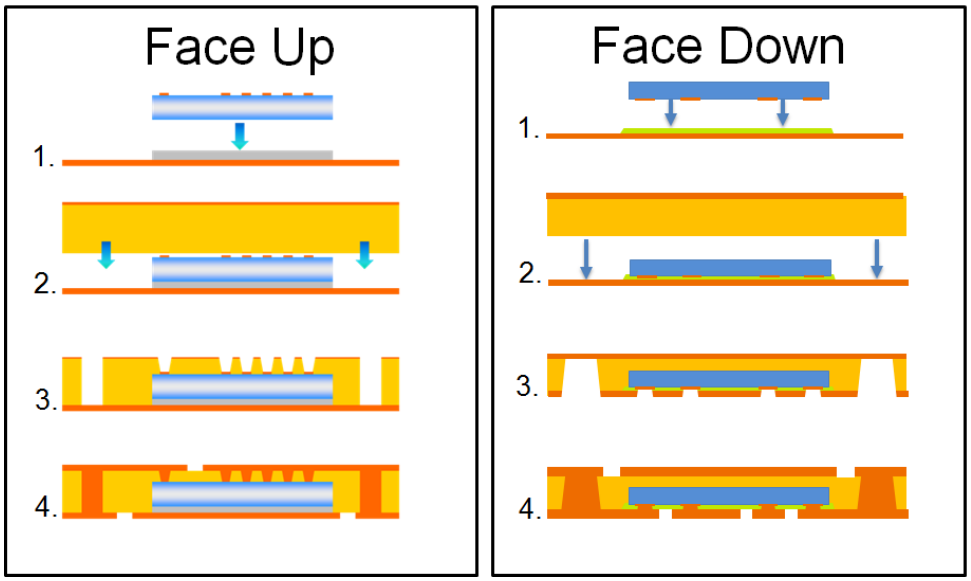


Figure 2.6: Schematic process flow of ECT, a) face-up chip embedding, b) face-down chip embedding [33]. The process flow for both, the face-up and face-down chip embedding includes (1) die bonding to substrate, (2) vacuum lamination, (3) laser drilling of micro via, and (4) copper metallization and patterning.

at avoiding chip damage during the lamination step. Following this, the embedded chip on the substrate is vacuum laminated with Resin-Coated-Copper (RCC) polymer films [34]. Subsequently, via opening on the active pads of the embedded chip is done by laser drilling. Finally, metallization of the vias is performed by electroless copper plating and photolithographic patterning. The face-down chip embedding is a better candidate for a fine-pitch interconnection. However, the face-up ECT provides better

electrical and thermal backside contact [33].

Würth electronic is developing a Chip-in-Flex embedding technique for industrial applications. This company uses a non-conductive adhesive (NCA) for the die attachment and copper-clad liquid crystal polymer (LCP) as a substrate. In Würth's technique, the other multilayer copper-clad LCP is pressed on top of the embedded chip with a thickness close to the bottom foil to minimize the unwanted stress on the chip [9], [35]. The ECT is under development to reach the ultra-fine pitch ($\sim$ 50 µm) interconnection, called via-less embedding technique. Besides that, dual chip packaging or PiP is another application of ECT [36]. The size of micro via formation is limited by laser drilling equipment. The via diameter can go down to 30 µm diameter and a 100 µm pitch [33], [32].

2.2.2 Ultra-Thin Film Package (UTFP)

The ultra-thin film package (UTFP) is composed of several parts including, ultra-thin chips ($\sim$ 18 µm), solder bump (3 µm copper) with underfill, embedding material on bottom and top, and metal traces [37]. The UTFP process flow is illustrated in Fig 2.7. As shown in Fig 2.7, 3 µm Cu layer is printed as a solder paste on top of the 18 µm foil

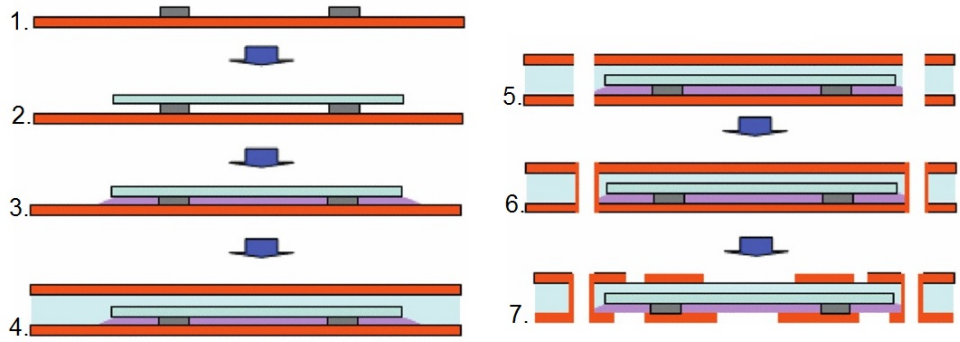


Figure 2.7: Schematic process flow of UTFP, 1) solder ball printing and reflow on Cu foil, 2) flip chip bonding, 3) underfill dispensing, 4) lamination, 5) via formation, 6) metallization, and 7) patterning [37], [38].

substrate. The height of the solder ball is around 16 µm. Then, the fabricated ultra-thin chips are embedded in the "flip-chip method" on top of the solder bump by thermal compressing. The gap between the Cu solder bump and embedded silicon chip is filled by underfill dispensing and a corresponding curing step. The top surface of the embedded chip is covered with Ajinomoto build-up film (ABF) during lamination process. The 18 µm carrier foil with 3 µm Cu is laminated above the ABF. The Cu carrier film has a symmetrical thickness on top and bottom of the embedded chip. Following

this, the electrical interconnections are formed using laser drilling and metallization. The total thickness of the UFTP package is up to 100 µm and can be bent to a 10 mm radius of curvature. The UFTP system has gone through several reliability tests, such as the thermal cycling test (TCT), the thermal and humidity storage test (THST), static bending, and dynamic bending [37] [39].

2.2.3 Ultra-Thin Chip Package (UTCP)

The ultra-thin chip packaging (UTCP) technique is a technology of direct embedding ultra-thin chips in flexible spin-on polyimide (PI) substrates. The UTCP technology was invented at IMEC [40] and Gent University [41]. The first publication about UTCP technology was in 2006 by Jan Vanfleteren and Wim Christiaens [42]. The UTCP process flow is depicted in Fig 2.8. As illustrated in Fig 2.8, the surface of the rigid glass

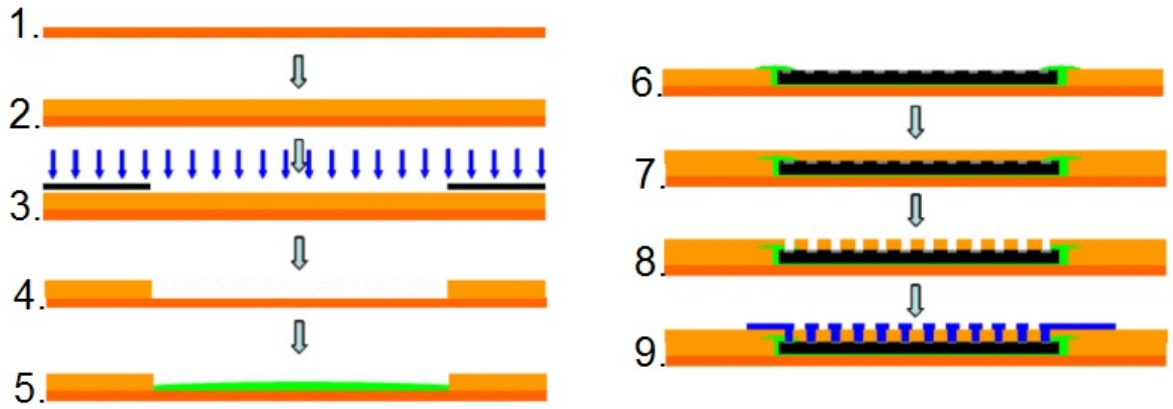


Figure 2.8: Schematic process flow of UTCP, 1) release layer deposition and base PI coating on top of glass carrier, 2) spin coating photodefinable PI, 3) illuminating photodefinable PI, 4) cavity opening, 5) BCB dispensing as a permanent adhesive layer, 6) face-up chip embedding, 7) coating top PI, 8) via opening, 9) metallization and patterning [43], [42].

substrate is treated either with a thin layer of KCl as an adhesion lowering layer [44] or VM652 as an adhesion promoter [45]. A surface treatment step is necessary to release the final UTCP from the substrate carrier. Next, low CTE PI2611 is spin coated on top of a glass substrate. HD-4110 photodefinable PI is used for cavity opening using a lithography process [42]. During the chip placement step, a well-controlled amount of benzocyclobutene (BCB) is dispensed into the cavity which acts as a permanent glue. BCB is an excellent adhesive material for void-free and strong bonding which needs a minimum bonding temperature of 180 °C [46]. The ultra-thin chips are placed in the

pre-defined cavity and will be cured in the vacuum oven to achieve void-free chip embedding. The top PI is coated on top of the embedded chip with a thickness similar to the bottom PI. Then, the vias on-chip are opened by laser drilling. The size of the via can go down to 40 µm. The further via minimization ($\sim$ 15 µm) can be achieved by using metal as a hard mask [1]. Once the vias to the contact pads of the embedded chip are opened, a thin layer of TiW/Cu (500 nm/1 µm) is sputtered [40], [43] as a seed layer and 5 µm Cu is electroplated on top of them. Finally, the metal layer is structured and the thin chip in the UTCP package can be released through a laser cut. The tested UTCP (KGD) can be embedded as a package in standard multilayer flex board or PCB and the embedded chip is interconnected through via drilling and the metallization process [47], [48]. The UTCP test samples have gone through various reliability tests (ex: TCT, THST) and survived each of them. In recent years, the UTCP has evolved from single-chip placement (Mono-UTCP) to multi-chip placement (Multi-UTCP) and interconnection [49]. In addition, the stretchable circuit, including functional chips and stretchable interconnects is another technology which is achieved at IMEC and in combination with UTCP [50]. The summary of the UTCP technology is shown in Fig 2.9.

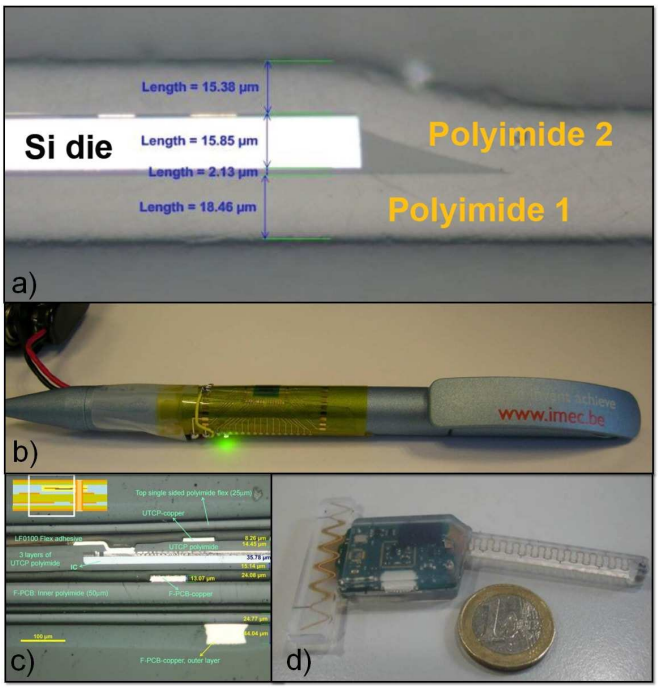


Figure 2.9: Summary of the UTCP technology, a) cross section of the UTCP stack, b) highly bendable UTCP [51], c) UTCP in FCB for a wireless sensor node application [42], d) the stretchable ECG sensor device [50].

2.2.4 Chip-Film Patch (CFP)

The Chip-Film Patch (CFP) technology is an already published process to embed and interconnect ultra-thin chips in polymer foil. The CFP was developed at Institute for Microelectronic Stuttgart (IMS Chips) in 2011 [52]. The CFP process flow, optimization, and the related performance evaluation are mainly the topics of this thesis. The main advantage of CFP is, its compatibility with the IC processing line which allows for a fine-pitch interconnection ($\sim$ 10 µm) [53] and high numbers of I/O. The process flow of the CFP is shown in Fig 2.10. As shown in Fig 2.10, after substrate preparation,

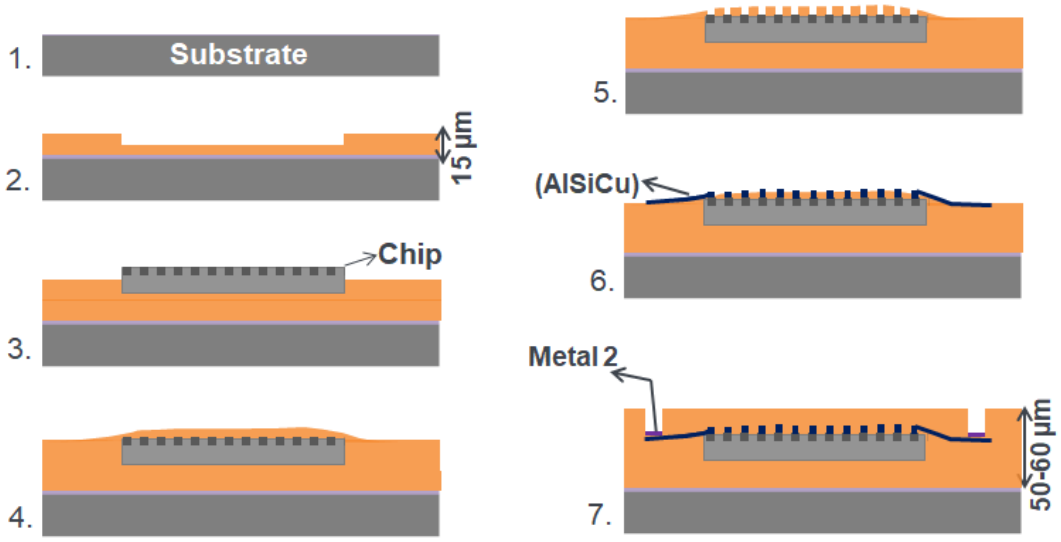


Figure 2.10: Schematic process flow of the CFP, 1) depositing adhesion lowering layer on silicon carrier, 2) polymer coating and cavity opening, 3) face-up chip embedding in cavity, 4) top polymer coating and surface planarization, 5) via opening, 6) metallization and metal patterning, 7) polymer coating, outer pad opening, further metallization, and releasing CFP from temporary carrier.

15 µm polymer is deposited on top of the substrate. Then, cavities are defined using a lithographic process and RIE. The small size ultra-thin chips (down to 10 µm) are embedded face-up in the cavities by using BCB as a permanent glue. The surface of the embedded chips is covered with a polymer symmetrically to the polymer underneath. During the via opening step, the metal pads on the embedded chips are opened by a lithography process using a hard or soft mask. After the via opening, the 1 µm metal (AlSiCu) is sputtered and patterned. The surface of the metal is covered with polymer and the outer pads are opened on foil. To avoid moisture absorption and native oxide generation, the outer metal pads on foil can be covered with noble metal. In the end, the ultra-thin chip embedded in foil can be released from the temporary silicon sub-

strate. The final CFP product can be used either as an interposer layer in other packages or as a standalone system. The functionality of the chips can be tested (KGD) before embedding them in other packages (PoP). Additionally, CFP can be extended to Multi-CFP which includes multiple chips-in-foil embedding and interconnection. The CFP can be advanced to the complex system-in-foil by integrating multiple chips in combination with OTFTs, antennas, and sensors. The CFP test samples are gone through various reliability tests, such as bending, TCT, and THST and successfully survived all of them. The details of the variety of CFP, process flow, challenges, materials, and characterization of CFP are coming in Chapter 3 and Chapter 5, respectively.

There are several technologies in addition to describing techniques which follow approximately similar concepts. Ultra-thin chip on flex (UTCOF) ([54], [55]), Thin Chip Foil Package [56], flip chip-in-flex, and "Chip in FlexRS^{TM} with printed contacts" [31] are other available approaches.

Criteria and specifications – the available technologies can be categorized based on 1) assembly (face-up or face-down), 2) interconnection (solder bump, ACA, or metal sputtering), and 3) substrate (on foil/FPC or inside polymer foil). Bendability of the fabricated system-in-foil, the minimum size of the pitch, number of I/O, and integrating with other packages depend directly on the categories which are chosen [57]. A summary of specifications for described flexible electronic technologies is shown in table 2.1.

Table 2.1: Criteria and specifications of the available flexible electronic technologies [32], [58], [37], [40], [43]. In this table, **FD** and **FU** stand for **face-down** and **face-up**, respectively.

Criteria	ECT	UTFP	UTCP	CFP
Chip thickness	50 µm	18 µm	15-25 µm	10-45 µm
Package thickness	100 µm	98 µm	50-60 µm	60-100 µm
Chip embedding direction	FD/FU	FD	FU	FD/FU
Via opening method	laser drilling	laser drilling	laser drilling/ lithography	lithography
Metal interconnection	Cu	Cu	TiW/Cu	AlSiCu/Ti/Au
Chip pad pitch	100 µm	200 µm	40 µm	**10 µm**
Chip pad size	30 µm	40 µm	15 µm	**5 µm**
Known good die	Yes	Yes	Yes	Yes
Bendability (radius of curvature)	10 mm	10 mm	10 mm	**4 mm**
IC process line compatibility	No	No	No	**Yes**
Thermal reliability test	Yes	Yes	Yes	Yes
Package on package (PoP)	Yes	Yes	Yes	Yes

2.2.5 Complex System-in-Foil

Large area electronics (LAE) can be chosen for various applications from wearable medical purposes to military application. However, a successful flexible electronic system should be the combination of large-area thin-film technology, the array of sensors, and advanced CMOS technology. Temperature, pressure, and humidity sensor besides thin-film batteries in combination with OTFTs, RF transceiver [59], oscillators, capacitors, inductors, and CMOS integrated circuits are a number of components required for hybrid or complex system-in-foil (HySiF).

However, the HySiF technology is still in the development phase and researchers in different groups are working to resolve the restrictions and develop a robust technique. The HySiF technology can be categorized into three groups; a) "monotonic integration" of all the components on a single package, b) interconnecting rigid islands which include different components, and c) 3-D interconnections of multiple sublayers with various integrated components in flexible substrates [60], [61]. In all cases, each component is either patterned directly or assembled on the flexible substrate.

The alignment of components corresponding to each other and the bendability of the final system, especially in case of 3D multiple sublayers, are challenges which must be solved. Also, the optimal placing of the components based on their functionalities are another interesting topic to be investigated [62]. The thermal source isolation or integrating strain sensor far from the neutral line are examples of an optimal placement. The monolithic integration of components toward the complex system-in-foil has already been proposed and developed in this thesis and the challenges and corresponding solutions are detailed in Chapter 4 and Chapter 5. In Fig 2.11, three demonstrations of HySiF are shown. These demonstrations cover three categories of monotonic integration, rigid island integration in the field of stretchable electronics, and 3D integration.

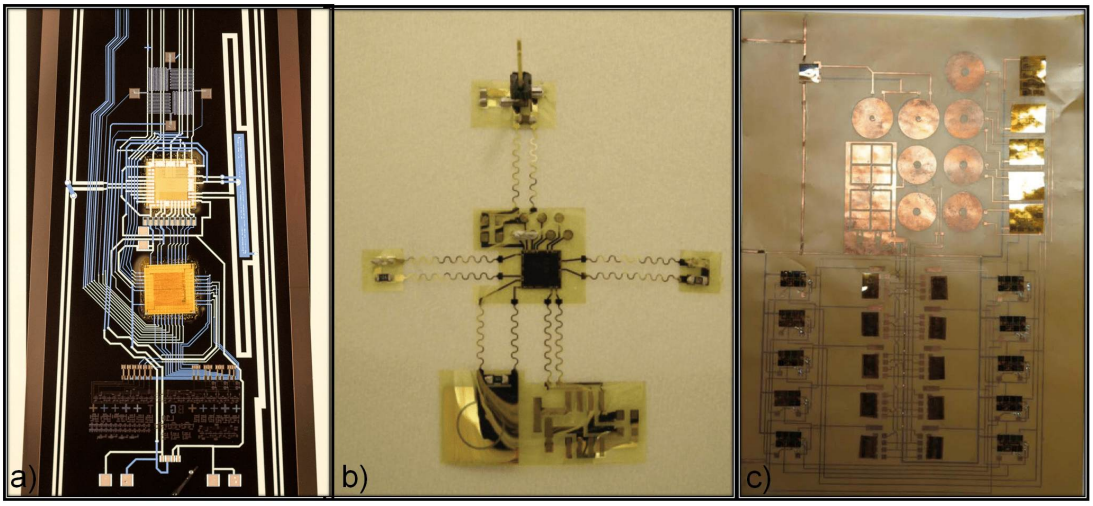


Figure 2.11: Illustrative examples of integrated systems on flexible substrates. a) monotonic integration of ultra-thin chips, strain gauges, and OTFTs in a single polymer foil. This system is developed as a part of this thesis. b) integration of isolated fabricated components on foil as a UTCP stretchable demonstration [51]. c) active thin-film circuits on passive copper backplane as multiple sublayers on top of each other [61].

2.3 Fabrication of Ultra-thin Chips

Silicon substrates have a thickness in the range of 500-1000 µm for reliability and mechanical stability of the wafer in microelectronic manufacturing steps [1]. However, the silicon chips need to be thinned down to be utilized in flexible electronic or 3D integration technologies. Driven by flexible electronic evolution, wafer thinning technology and ultra-thin chip fabrication is promoted down to $\leq$ 20 µm. This chip thickness is suited to be integrated into bendable or flexible electronic system [24].

In general, ultra-thin chip manufacturing can be categorized into two main groups; the subtractive approaches and the additive approach [63]. Each approach offers a new application for silicon technology and at the same time has special constraints. These ultra-thin chip manufacturing techniques are described in the following.

2.3.1 Subtractive Approaches

Silicon wafer back grinding is the conventional method to reduce the thickness of silicon wafers to the required thickness down to 50-100 µm [64]. However, as the wafers become thinner, micro-crack generations become a serious problem for the functionality of the ICs [1]. Besides that, the non-uniformity of wafer thickness restricts the repro-

ducibility of the wafer back grinding technology [63], [65]. Therefore, additional process steps, such as chemical-mechanical-polishing (CMP), wet etching, or dry plasma etching [64] are needed to remove grinding damages. Besides that, the main purpose of the wafer back-thinning is the thin chip fabrication. So, new techniques, such as "dicing-by-thinning (DbyT)", and "Dicing-before-Grinding (DBG)" were developed to manufacture and handle ultra-thin chips with a thickness below 50 and down to 20 µm [1]. In this work, the DBG manufacturing technique among other subtractive approaches is described and used.

Dicing-Before-Grinding (DBG) Process

In a conventional back grinding process, dicing is applied after back grinding. However, further problems arise from this, like edge chipping, the creation of micro-cracks, and wafer handling. Therefore, the DBG technique is developed to minimize the challenges during the conventional process. The DBG process reverses the existing process by dicing the wafer before back grinding [1]. The DBG process flow is shown in Fig 2.12. As shown in Fig 2.12, as a first step, the silicon wafer is laminated on top of

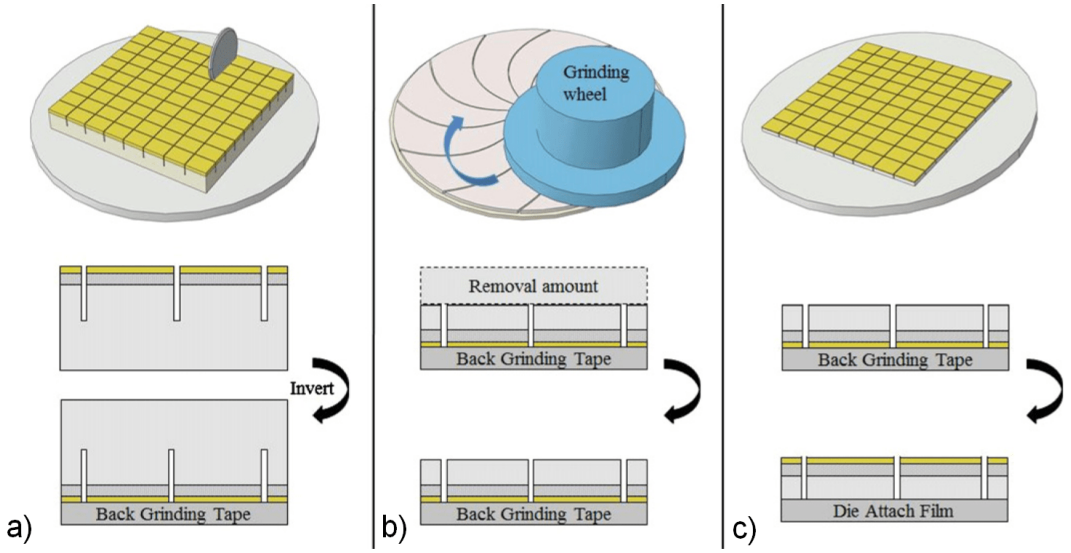


Figure 2.12: Fabrication of an ultra-thin device by using the DBG (dicing before grinding) process. a) dicing and front side laminating on BG tape, b) back grinding, c) laminating backside to attach film and releasing the front side from BG tape [66].

the foil. The dicing saw cuts a wafer into the die with the depth slightly bigger than the required final thickness of the thinned chip [67]. Then, the circuit side of the wafer is laminated on top of the back grinding tape. The back grinding is performed with a grinding wheel using "diamond abrasive grains" in two steps [1]. In the first step, the wafer is back grinded with a coarse grain size. After that, the fine grain size is used to remove damage which is caused by the coarse grinding wheel. After reaching

the grooves formed by the dicing process, the "stress-relief etching step" is performed. The stress-relief is performed to minimize damage and related stress on fabricated thin chips using wet etching, dry polishing, CMP, or plasma etching [68]. In the end, the back grinded wafer is mounted on top of the standard dicing frame and the back grinding (BG) tape is removed from the circuit side. The ultra-thin chips with the thickness in the range of 35-20 µm can be fabricated using the DBG manufacturing process.

In order to conduct this cost-efficiently, IMS CHIPS has developed a method to grind back single chips rather than on a wafer level. The functionality of these chips is tested and these ultra-thin chips were integrated into polymer foil as part of this research.

Silicon-on-insulator (SOI) is another subtractive approach which has far better results and thickness uniformity in comparison to the back grinding method [63]. However, the high cost-of-ownership (CoO) of SOI wafers besides technical challenges are two important drawbacks of this technology [1]. In contrast to high costs, SOI technology reduces the capacitance between junctions, passive current, and eliminates latch-up. A basic SOI structure includes a thin silicon film above an insulating layer (silicon dioxide) on top of the bulk silicon substrate. The top silicon layer, silicon dioxide, and bottom silicon substrate act as an active device, dielectric material, and mechanical support, respectively [69]. After circuit integration, the active device region is separated from the below silicon substrate using BOX and help of various other methods such as "IMplantation of OXygen (SIMOX), Bonded and Etch-back SOI (BESOI) and the SmartCut process" [1]. With this technique, the ultra-thin chips can be manufactured with a thickness down to 10 µm.

2.3.2 Additive Approach

ChipFilm™ technology is an additive technique allowing for precise control of a small chip thickness below 20 µm. The thickness of chips is identical to the thickness of the epitaxial layer which is prepared in the first step of ChipFilm™ technology. The schematic illustration of the ChipFilm™ technology is shown in Fig 2.13. As shown in Fig 2.13, the ChipFilm™ fabrication process can be categorized into four modules; pre-process, CMOS integration, trenching, and chip singulation. The thickness of the chip is defined in pre-processing [71] by fabricating buried cavities which separate the "chip-to-be" in a CMOS integration step from the substrate. At the same time, the "chip-to-be" is kept safely attached to the membrane till the end of the process by the anchor array which is fabricated in the pre-processing step. In post process module and after the CMOS fabrication, trenches are etched using RIE at the chip edges down into buried cavities while the group of anchors remain below the chip and on the chip's corners. The number of anchors below and on the edge of the chip are arranged in the way that the chips can be detached easily using conventional picking equip-

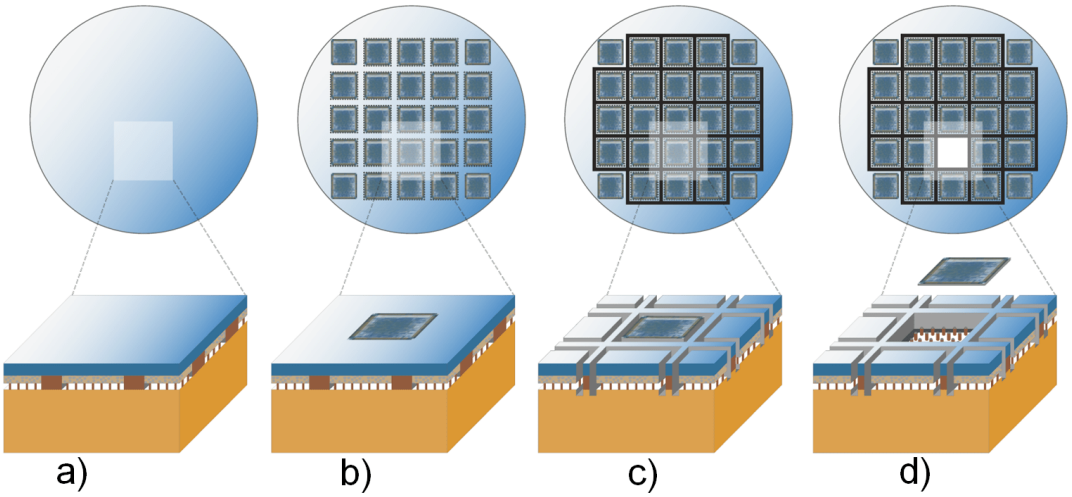


Figure 2.13: Illustration of ChipFilm™ process flow: a) the fabrication of pre-processed wafer substrates include buried cavities underneath the intended chip areas, b) CMOS process and device integration, c) trench and test, d) chip singulation, pick, crack and place™ (post process) [65] , [70].

ment [1], [72]. The excellent thickness control of the ChipFilm™ technology plays an important role in the Chip-Film Patch for face-up integration and interconnection of ultra-thin chips in polymer foil. Therefore, in this work, internal chips are manufactured using ChipFilm™ technology and external chips are back grinded down to the required thickness.

2.4 Summary

The world of CMOS technologies is evolving at a high pace while reducing feature sizes, and increasing I/O count on the chip at the same time. Beside the progress in CMOS technology, demands for the complex and heterogeneous system motivate microelectronic researchers to develop electronic packaging towards miniaturization and complexity. Electronic packaging is mainly categorized into two groups: single chip and multiple chip packages. In both cases, four basic elements define the package structure; a) the interconnection of the chip to package, b) the encapsulation of the chip, c) the structure and material of the package, and d) the connection of the package to the PCB or other packages [73].

On the other side, a flexible electronic world is driven by the need to add more functionality, more features, and bendability all at the same time and at a lower cost. Flexible electronics are generally based on a thin polymer structure or flex. Flexible electron-

ics are also known as a system-in-foil (SiF). The flexible and bendable SiF technology can provide interconnection and integration of thinned inorganic or organic semiconductors in combination with RF, sensors, and MEMS in one single substrate. However, the size of the pitch, I/O counts, flexibility, and stretchability of final system-in-foil is in direct relation to the substrate material, chip embedding, interconnection, and encapsulation. The recent focus has mainly been on integration and interconnection of the hybrid system in the flexible foil (HySiF) including advanced CMOS technology, the array of sensors, and high-frequency antennas.

On the other side, silicon chips need to be thinned down in order to be integrated into a flexible substrate. Otherwise, the flexibility of system cannot be guaranteed. Therefore, various manufacturing technologies are in progress to fabricate ultra-thin chips. These technologies can be categorized into two groups; subtractive approaches and additive approaches. This classification is based on whether the primary silicon is added to the substrate (additive) or removed (subtractive) from the substrate. Each of the technologies can be chosen based on the costs, desired final thickness of the chip, thickness uniformity, and reproducibility.

CHAPTER 3

CHIP-FILM PATCH CONCEPT AND TECHNOLOGIES

"Paths are made by walking."

— Franz Kafka

The Chip-Film Patch technology (CFP) is providing a method to embed and integrate of ultra-thin chips into a flexible, bendable, low-cost, and large area polymer foil substrate. CFP can be applied either as a foil interposer embedded in a laminated printed circuit board (PCB) or as a standalone foil system in combination with sensors, battery, organic thin-film transistors (OTFTs), and antennas as an autonomous system [74]. The CFP technology is a great candidate towards hybrid system-in-foil (HySiF) technology, but often limitations exist due to a restriction in processing methods and incompatibility of the material with the IC processing fabrication line. These issues are discussed herein, together with the various concepts of technologies and a comparison between them.

3.1 CFP Face-Up Concept

Embedding ultra-thin chip in flexible substrates can be differentiated depending on the die attach technique used: face-down assemblies (flip chip mounting) on preprocessed wiring layers or face-up assemblies followed by subsequent interconnection and wiring. The via opening can further be performed either by laser drilling [58] or photolithographic patterning [56]. In CFP face-up concept, the chips are embedded face-up in the pre-defined cavities in the polymer foil substrate using benzocyclobutene (BCB) as a permanent glue. The primary purpose of this process is to bring the device side and polymer foil to the same level in order to perform further via

opening, metallization, and metal patterning. However, the embedded chip surface planarization is still a significant challenge, especially in the via opening step. The planarization is achieved with several coating steps and additional inspections. This way, it is also possible to build a smooth ramp transition from the chip top surface to the foil level to realize the subsequent metallization step [57]. This smooth ramp transition from the edge of the chip to the polymer foil plays an important role in long time reliability of the system in bent condition. The face-up chip embedding is a suitable approach when embedding and integrating multiple chips with the same thickness in the polymer foil. The schematic process flow of the two polymer embedding technique using the face-up concept is depicted in Fig 3.1. The CFP technology with face-up chip

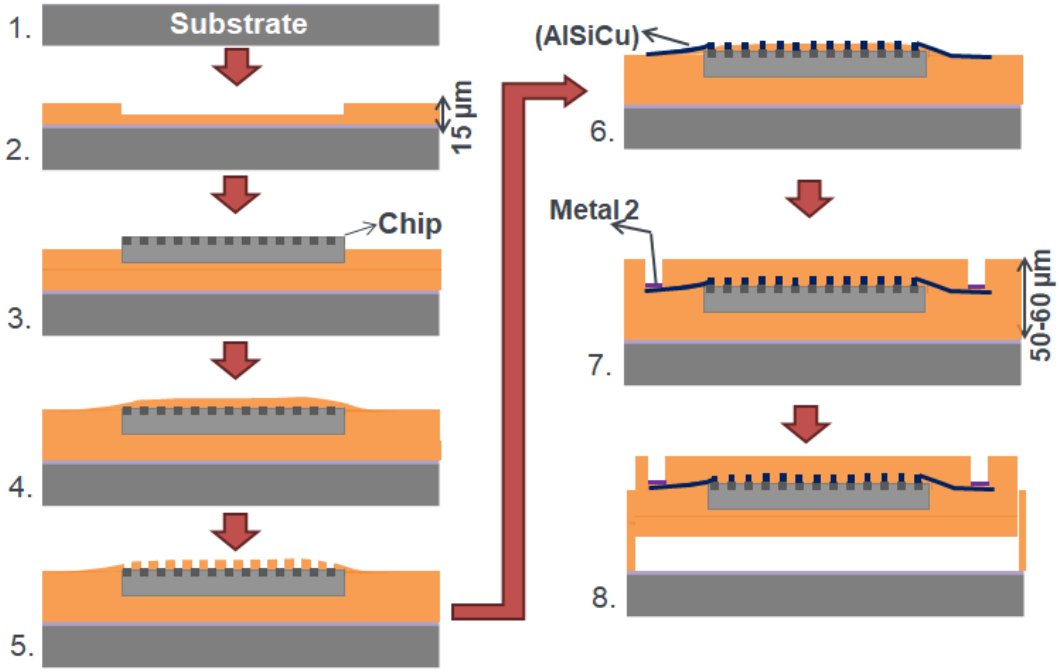


Figure 3.1: Process flow overview of the CFP Face-Up concept: 1) wafer pre-surface treatment, 2) spin coating the base polymer and cavity opening, 3) face-up chip embedding, 4) top polymer coating and surface planarization, 5) via opening, 6) first metallization, and metal patterning, 7) polymer coating, second via opening, and outer pad metallization, and finally 8) releasing system in polymer foil from the temporary substrate.

assembly can be categorized into two categories: two-polymer CFP technology and low-stress CFP technology. In both cases, a silicon wafer acts as a temporary carrier while embedding and integrating ultra-thin chips into polymer foil. First, the specific wafer pre-surface treatment is performed in accordance with the applied technology. After pre-processing, the base polymer layer is spin coated on top of the temporary

carrier. A cavity slightly bigger than the chip size ($\sim$ 500 µm from each side) is patterned and opened for the next step, the chip placement. The ultra-thin silicon chip is then embedded face-up inside the cavity with the help of a thin layer of BCB acting as the adhesive layer. The surface of the silicon chip is covered with a top polymer layer. The top polymer coating steps are performed to reach a reasonable planarization level between the chip surface and the foil at the chip edges. Micro-vias are then etched directly on the chip contact pads using photolithography and dry etching process. Conventional AlSiCu metallization is performed to create the metal interconnection from the pads on chip towards foil surface. Finally, the final polymer is spin coated on top of the chip stack to reach the top polymer thickness in symmetry with the bottom layer. The outer metal pads are opened using a dry etching process, and a second metallization step (noble metal) is performed before releasing the final system from the temporary carrier.

3.1.1 Two-Polymer CFP Technology

Two-polymer CFP Technology is an already published process [53] which is relying on embedding ultra-thin face-up chips inside two sandwich polymer layers. With this technology, a combination of benzocyclobutene (BCB) and durimide is applied. BCB, used as an embedding polymer, is a negative photoresist with high planarization capability. Durimide provides the mechanical flexibility of the system-in-foil (SiF), reinforces the layer stack, and shifts the brittle BCB near the neutral line of stress. The key advantage of this technology is its compatibility with CMOS technology, which enables a fine-pitch interconnectivity as well as an adoption to mainstream IC production facilities [7]. The major disadvantage for the two-polymer CFP technology comes from the high coefficient of thermal expansion (CTE) [75], [76] in comparison with silicon. Therefore, thermo-mechanical stress and strain arise from the deposition of these polymers during the embedding process due to a high CTE mismatch. In addition, durimide has a high moisture absorption compared to BCB and other polymers. Therefore, durimide is not a proper choice for standalone sealing or encapsulation. The schematic cross section of the two polymer ultra-thin chip embedding in CFP technology is illustrated in Fig 3.2. As shown in Fig 3.2, the two-polymer CFP technology is a face-up chip technology in which the via opening on the active pads of the embedded chips is done by lithography. The chip embedding is performed by using a thin layer of BCB (3.5 µm) as a permanent adhesive.

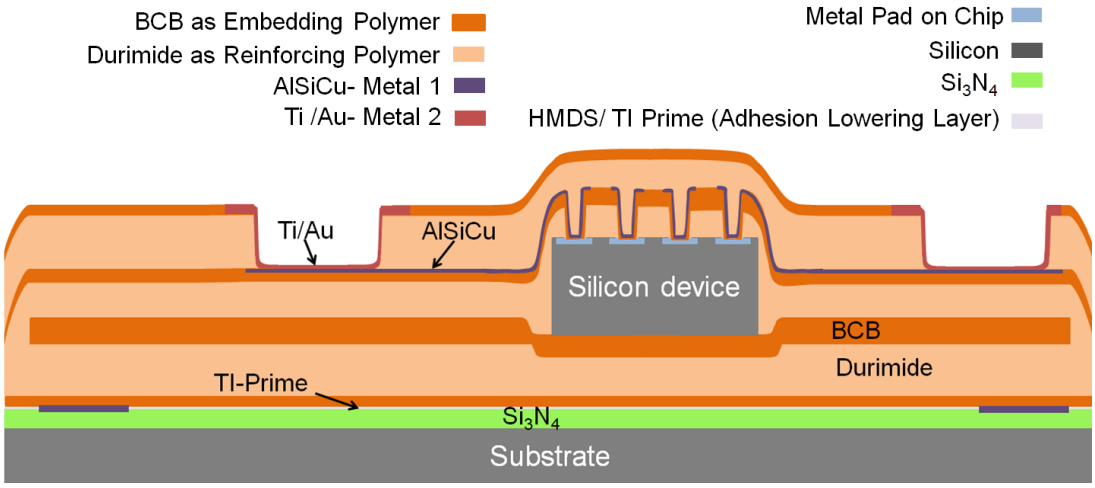


Figure 3.2: Schematic cross section of two-polymer CFP technology.

3.1.2 Low-Stress CFP Technology

Low-stress CFP is a novel technology which presents a polyimide (PI)-based embedding technology for very thin chips in flexible and thin polymer packages. In this technology, the PI2611 polymer is a low CTE polymer from HD Microsystems, provides both flexibility and planarization of the complete system-in-foil [77]. This type of polyimide is particularly useful because its CTE is approximately similar to that of silicon, thus, mitigating in-plane stress from potential CTE mismatches. This CTE match is very important in order to prevent introducing high thermal stress in the very thin silicon devices; in curing step (up to 350 °C) during the CFP processing [45]. The major disadvantage of PI2611 polyimide is that it has a higher level of water absorption compared to the BCB. In humid environments ($>$ 80% RH), PI2611 polymer experiences high-frequency losses, as well as dimensional instability [78]. Therefore, in a majority of high-frequency applications BCB is used instead.

The schematic cross section of the low-stress CFP technology is illustrated in Fig 3.3. In Fig 3.3, the ultra-thin chip is embedded face-up in the pre-defined cavity. The chip embedding is performed by using a thin layer of BCB (1 µm) as a permanent adhesive. The PI2611 polymer is coated symmetrically on top and bottom. The via opening on the pads of the embedded chip is done using lithography process. In addition, the low-stress CFP can be performed for face-down chip embedding as well. The face-down chip embedding is more suitable for the fine-pitch interconnection.

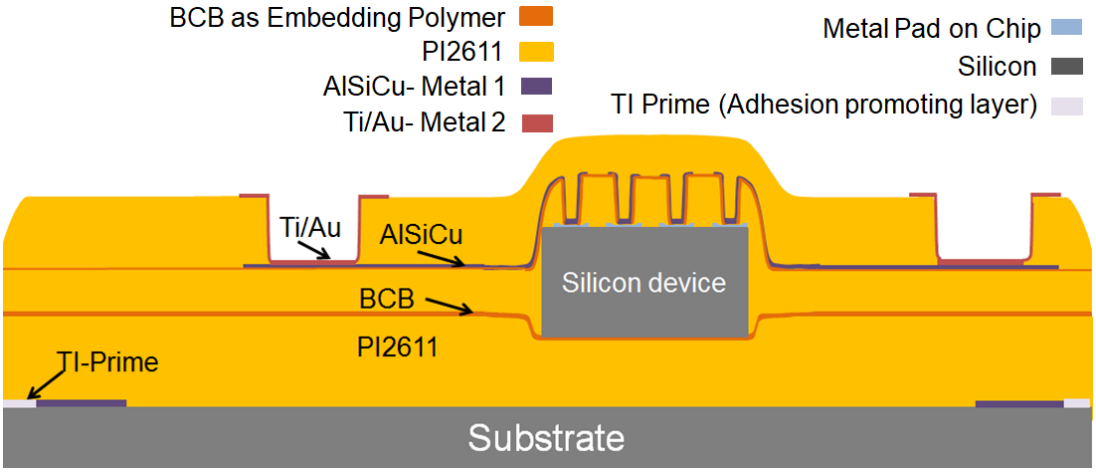


Figure 3.3: Schematic cross section of low-stress CFP technology for ultra-thin chips embedding in polymer foil.

3.1.3 Comparison of Two Face-Up CFP Technologies

In order to compare the two proposed face-up CFP technologies, we need to know their mechanical and electrical properties which are shown in table 3.1. Based on the low dielectric constant k (relative permittivity ε_r) characteristic of BCB, the material is very attractive as an interlayer dielectric for RF-components. The non-polar chemical structure of BCB leads to low dielectric constant (ε_r= 2.65) and a high breakdown voltage (530 V/µm) in combination with a low water uptake (less than 0.2 %). The good planarization properties also make BCB suitable for 3-D and adhesive bonding [79]. In contrast, PI2611 experiences high-frequency loss especially in humid environments (> 80 % RH).

When it comes to thermo-mechanical properties, BCB and durimide with high CTE mismatch with silicon induce a huge amount of thermomechanical stress on the chip and temporary carrier. This unwanted stress forces us to perform extra pre-surface treatment on a temporary carrier which is time consuming and costly. In addition, the embedded chip inside the foil is going to be under constant mechanical stress due to the CTE mismatch which can affect the reliability of the system. However, using low-stress PI2611, this problem is easily solved.

In flexible electronics, BCB with low elongation after curing becomes rigid and can-not be used alone. It, therefore, needs to be combined with another polymer with high elongation after curing such as durimide. However, PI2611 polymer remains flexible after curing and can be handled alone.

Overall, depending on the requirements and the type of application, each of the above

processes can be chosen. As an example, in case of the non-flexible high-frequency mm-antenna wave, BCB with a low dissipation factor and dielectric loss is suitable. On the other side, for fabricating humidity sensors, durimide with high moisture uptake can be chosen. PI2611 is a good option for high-temperature robustness applications or stress sensitive chips and modules.

Table 3.1: Mechanical and electrical properties table of Cyclotene 4000 (BCB), Durimide and PI2611 [76], [75], [77].

Parameters	BCB	Durimide	PI2611
Modulus of elasticity	2.9 ± 0.2 GPa	2.8 GPa	8.5 GPa
Tensile strength	87 ± 9 MPa	122 MPa	350 MPa
CTE	42 ppm/°C	52 ppm/°C	3 ppm/°C
Dielectric constant	2.65-2.5 (1 MHz-10 GHz)	3.5-3.8 (1 MHz, 4 %-50 % RH)	2.9 (1 kHz, 50 % RH)
Dissipation factor	0.0008-0.002 (1 MHz-10 GHz)	0.013-0.024 (1 MHz, 4 %-50 % RH)	0.002 (1 kHz, 50 % RH)
Moisture uptake	< 0.2 %	~ 1.08 % (50 % RH)	0.5 %
Elongation at break	8 ± 2.5 %	85 %	100 %
Glass transition temp.	> 350 °C	277 °C	360 °C
Poisson' ratio	0.34	0.34	0.34

3.2 CFP Face-Down Concept and Process Flows

In the past decade, different embedding technologies have been developed due to different requirements with respect to the electrical performance, chip dimensions, I/O counts, size of pitch, and required interconnection [32].

The primary purpose of the face-down CFP process is to bring the foil and the chip top surface to the same level for ease of processing and fine pitch interconnections from chip to the foil level [57]. Additionally, embedding chips with different chip's thicknesses inside foil can benefit from this process. With this technique, after face-down chip embedding, the active side of all the embedded chips comes to the same foil level, thus enabling ease of interconnectivity between them. This characteristic can be extended to embedding ultra-thin silicon chips in combination with other modules same as GaN with different thicknesses as a hybrid system-in-foil (HySiF).

Apart from same level chip embedding in foil, backside processing of silicon chip is another application which can be pursued with the help of the chip face-down tech-

nology. For example, we can think of fabricating a heat spreader in the chip's backside as a cooling method for the embedded high power ultra-thin silicon chips in polymer foil.

The process flow of the chip face-down for CFP is illustrated graphically in Fig 3.4. As shown in Fig 3.4, the ultra-thin chips are embedded face-down inside the cavity by

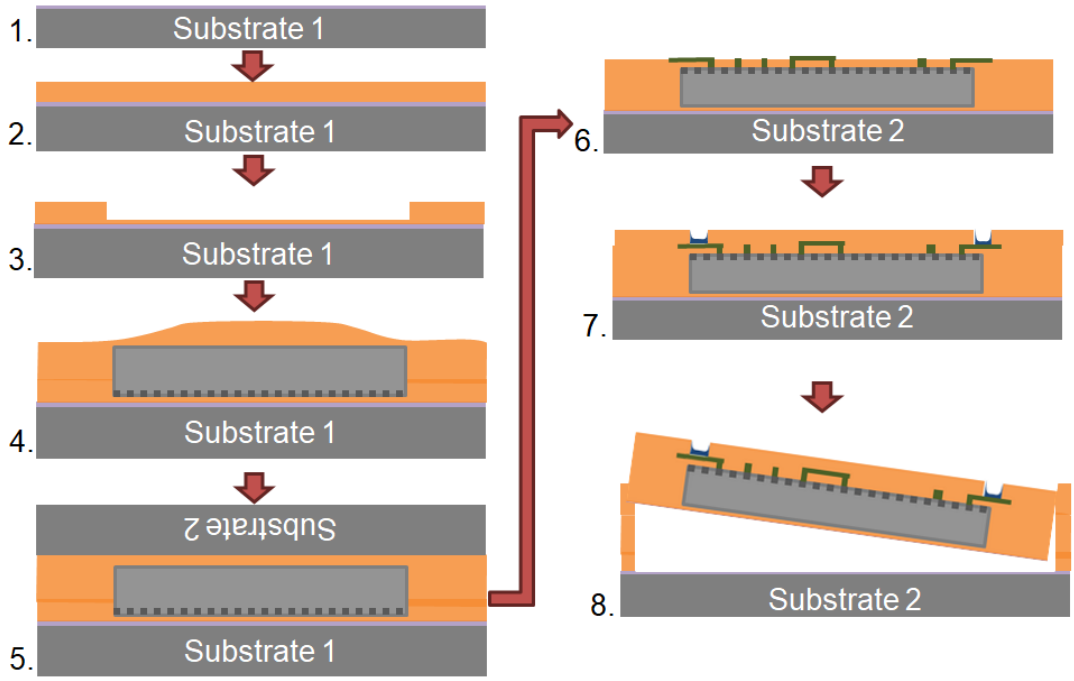


Figure 3.4: Graphical illustration of the chip face-down process flow: 1) wafer pre-surface treatment, 2) spin coating the base polymer and cavity opening, 3) face-down chip embedding, 4) top polymer coating, 5) coating bonding material and introducing substrate 2, 6) transferring from substrate 1 to substrate 2 , via opening, first metallization, and patterning, 7) polymer coating, second via opening, and outer pad metallization, and finally 8) releasing system in polymer foil from substrate 2.

using BCB as an adhesive layer. The bottom and top polymer are coated symmetrically. The face-down process follows similar process steps to face-up CFP up to via opening. Then, the embedded chip inside the polymer foil is transferred to the second substrate as a face-up chip. Afterwards, the via opening is done through lithography. In this case, one of the key challenges is to release the face-down chip into the foil from the first temporary carrier and attach the foil as a face-up chip, to the second carrier for further processing steps (step 5 and 6 in Fig 3.4).

The foil transfer from one carrier to the second carrier can be categorized mainly as: thermomechanical debonding, chemical debonding, laser assisted debonding, and

lamination. The next subsections mainly focus on different technologies to debond polymer foil from the first carrier and transferring that to the second carrier.

3.2.1 Thermo Mechanical Debonding

The mechanical release system offers separation suitable for both low- and mid-volume production environments [80]. The primary challenge in the transfer technology originates from the stress that is developed during high-temperature processing predominately through thermal-mechanical CTE mismatches between the first carrier, deposited polymers, and the second substrate [81]. A series of polymers with a different coefficient of thermal expansion (CTE), elasticity modulus, and thickness are coated on the temporary silicon carrier to investigate and correlate the thermo-mechanical properties of polymer foils with ease of bonding and debonding from the substrate. In this process, a thin layer of BCB acts as a temporary bonding material between the first and the second carrier.

As a summary, for the two-polymer CFP technology (3.1.1), due to the high CTE mismatch between the polymers and the silicon wafer, debonding the foil from the first carrier generates micro-cracks on the chip and, therefore, damages the ultra-thin silicon chip which is embedded in foil.

3.2.2 Chemical Debonding

Chemical debonding is ideal for low-volume R&D production environments. One of the conventional chemical debonding methods is depositing and processing the materials on a perforated carrier for further processing. After processing is completed, the bonded pair is placed in a suitable solvent bath for separation [80]. In our case, the perforated carrier could not be effectively employed for fabrication of Chip-Film Patch technology due to several difficulties. The primary difficulties involved in the process include wafer backside contamination during the spin coating process, and foil surface roughness because of the perforation pattern transfer. The wafer backside contamination makes further wafer handling process difficult for other tools [57].

Instead of the perforated carrier, coating an adhesion lowering layer as a first layer on top of silicon handling carrier is one of the steps in the pre-surface treatment of the face-up CFP technology. On this term, a strong adhesion lowering layer is applied on top of the first carrier as an initial step. It is important the adhesion should be reduced to the extent that the entire embedding process can be carried out without any difficulties or undesired delamination until transferring step. In this case, several wafers are processed with an anti-stick layer called BGL-GZ-83. The BGL-GZ-83 acts as

an anti-stick layer especially in the process of separating stamp and substrate following the resist coating [82].

Although the transfer process was successful (Fig 3.5), it could not effectively be applied for the fabrication of the face-down CFP technology due to a number of difficulties. The primary challenge being the non-repeatability step of the process due to the non-homogeneity of first coated polymer on top of the anti-stick layer. Additionally, transferring the foil from one carrier to the smaller carrier reduces the so-called yield of production.

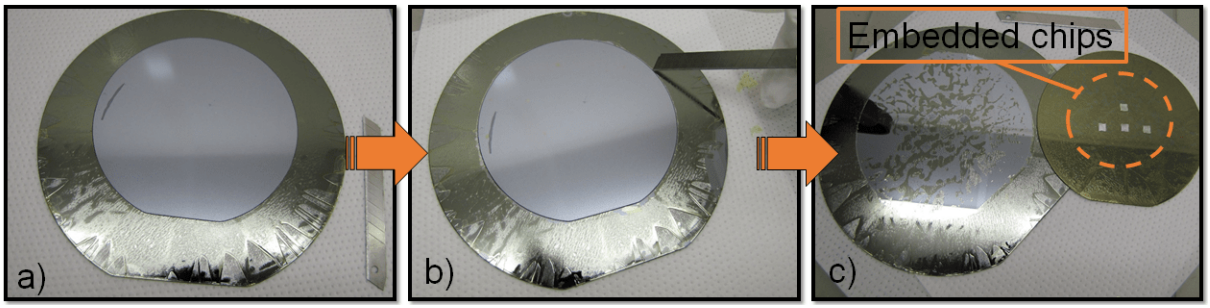


Figure 3.5: Transferring the face-down embedded chips on foil from the first carrier to the second carrier using pre-surface treatment: a) temporary bonding of the 100 mm second silicon carrier on top of the 150 mm first silicon carrier using BCB on the round of smaller carrier, b) cutting the polymer foil from edges, and c) releasing the face-down chip embedded in polymer foil from the first carrier and transferring that as a face-up chips to the second one.

3.2.3 Excimer Laser Assisted Debonding

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments. The schematic process flow of face-down CFP using the excimer laser is depicted in Fig 3.6. In this process flow, BCB acts as a bonding material and HD3007 polymer serves as a release material. The HD3007 polymer is spin coated on top of the glass substrate and is subsequently cured in the nitrogen atmosphere to obtain a thermoplastic layer with a defined thickness between 3 and 40 µm. The cured films have a high absorption in the UV range with a very low penetration depth of only approx. 200 nm at the wavelength of 248 nm [83], [84], [85]. After embedding the silicon chip inside polymer, the system-in-foil needs to be transformed to the second carrier. The

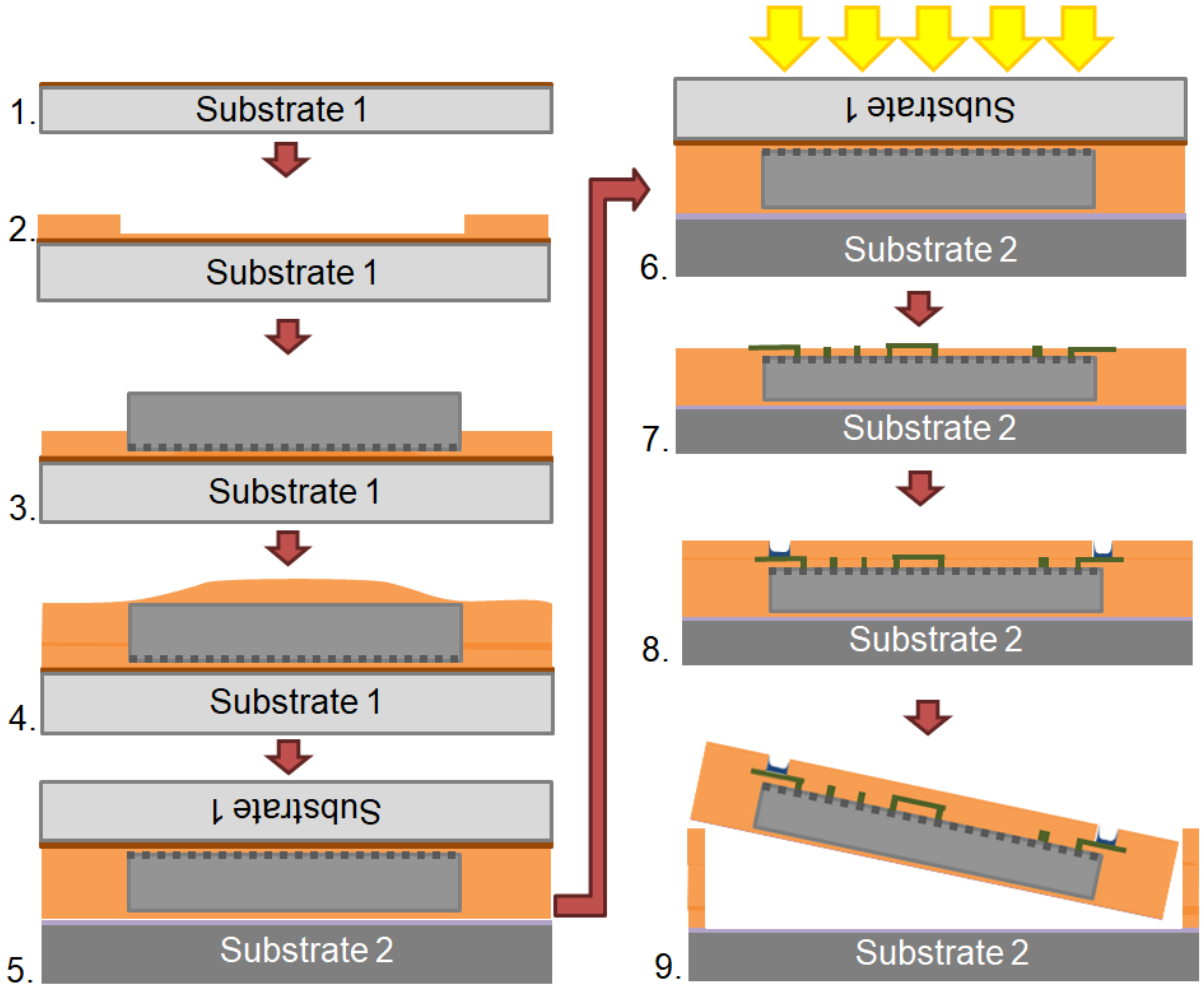


Figure 3.6: Schematic process flow of face-down CFP using the excimer laser; (1) pre-surface treatment includes: removing contamination, priming glass wafer with HD3007 polymer, (2) spin coating of polymer as a composite foil, cavity opening for chip placement,(3) chips face-down assembly inside the cavities using BCB as a glue layer, (4) covering the surface of the chips with polymer planarizing chip-in-foil, (5) temporarily bonding the first glass substrate to second silicon carrier. The glass carrier with polymer on top, is bonded to second silicon carrier using BCB as a glue on round of silicon wafer, (6) exposing the backside of the glass carrier using excimer laser and debonding the foil from the first carrier while attached to second silicon carrier, (7) micro via opening, AlSiCu metal sputtering and structuring, (8) spin coating of polymer symmetrically to the polymer foils below the chip, outer pad opening and noble metal deposition, (9) cutting from side and releasing CFP foil from silicon carrier.

principle workflow to detach the glass carrier wafer is: (1) the side with the temporarily bonded components or wafer has to be attached to the next support medium which in, our case, is a 150 mm silicon carrier. (2) With the glass wafer facing up the laser radiation can transmit through the glass and expose the adhesive at the bond interface.(3) The laser exposure is done using an excimer laser ablation system which allows for a beam focus at the adhesive bond interface as well as the whole wafer area. (4) Due to the high absorption of HD3007 polymer in a very low penetration depth, the whole radiation energy is absorbed within a 200 nm zone of the adhesive [86]. After the entire wafer area is exposed, the glass carrier wafer can be detached from the components or wafer (Fig 3.7). The surface of bonded foil to the second carrier is further cleaned and the adhesive residues are removed.

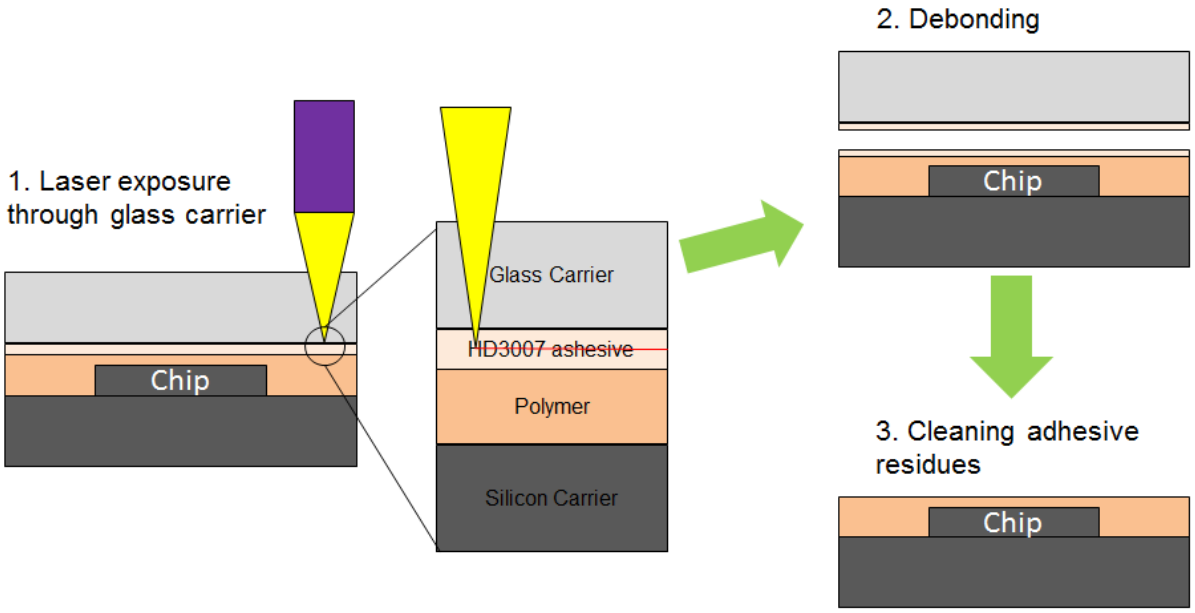


Figure 3.7: Schematic workflow of laser-assisted de-bonding.

Although significant progress has been made with the implementation of the process flow, due to the lack of facilities and required tool (excimer laser), the excimer laser debonding for face-down CFP is considered work to come in the future.

3.2.4 Lamination Foil

One of the common challenges in polymer bonding-debonding is the danger of chip damage and micro-crack generation due to the mechanical stress between two wafers during the detachment. Besides that, wrinkle generation on top of BCB as a bonding

material, due to sliding two carriers on top of each other can cause further problems and add extra unwanted topographies on top of foil. Besides technical limitations, to solve the above challenges, a face-down concept is proposed in which, the embedded ultra-thin chips inside polymer foil are released from the first carrier and fixed as a face-up chip to the second carrier to do further via opening and metallization steps.

A new technique was developed in order to minimize any trapped air or avoid wrinkles generation below the foil in during the transferring step. This technique combines the face-down CFP technology with the lamination foil and laminating system. The CFP polymer foil acts as a substrate in which the TMMF foil as dry film resist is laminated onto it in a vacuum circumstance. Dry film resists are particularly interesting because they can be lithographically structured and, thus, allow for patterns within a low- and submicron scale [87]. The schematic process flow of the face-down CFP by the assistance of the laminating tool and the lamination foil is shown in Fig 3.8. The process flow of the face-down CFP by using lamination foil is detailed in subsection 3.4.12. In this work, the face-down CFP mainly refers to a low-stress CFP in combination with lamination foil and the laminating tool.

The technology readiness levels (TLR) of the CFP technology based on European Commission (EC) definition is summarized in table 3.2. TLR in the definition of the European Commission is numbered from 1 to 9. However, in the scale of research field, the TLR 1 - TLR 6 are more relevant [88]. In table 3.2, there are technologies which are still in optimization and reliability test. Therefore, they are defined as "No" in front of the corresponding TLR number.

Table 3.2: Technology readiness levels of the CFP technology based on various techniques [88]. In this table **FU** and **FD** stand for **Face-up** and **Face-down**, respectively.

TLR	Description	FU two-polymer CFP	FU low-stress CFP	FD two-polymer CFP	FD low-stress CFP
TLR 1	"basic principles observed"	Yes	Yes	Yes	Yes
TLR 2	"technology concept formulated"	Yes	Yes	Yes	Yes
TLR 3	"experimental proof of concept"	Yes	Yes	Yes	Yes
TLR 4	"technology validated in lab"	Yes	Yes	No	Yes
TLR 5	"technology validated in relevant environment"	Yes	Yes	No	No
TLR 6	"technology demonstrated in relevant environment"	Yes	No	No	No

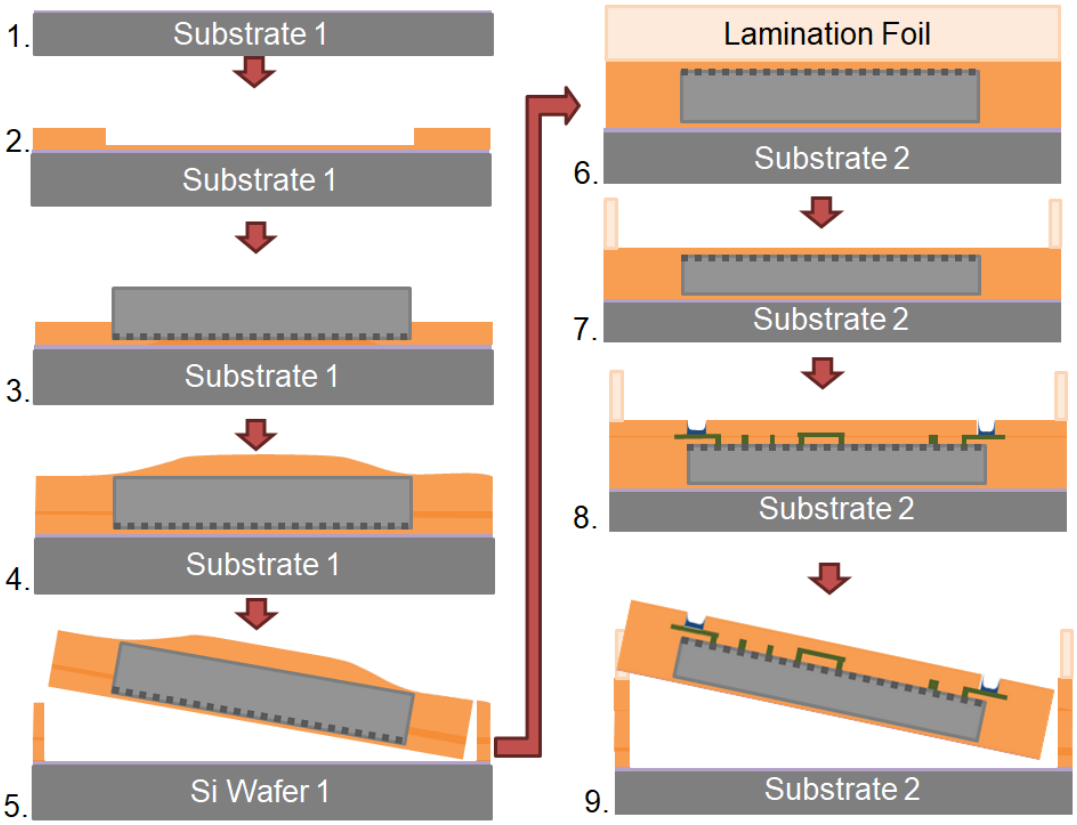


Figure 3.8: Schematic process flow of the face-down CFP using the laminating tool and lamination foil; (1) pre-surface treatment, (2) spin coating of the polymer as a composite foil, cavity opening for chip placement, (3) chips face-down assembly inside cavities with using BCB as a glue layer, (4) covering surface of chips with polymer, planarizing chip-in-foil, (5) releasing the chip embedded in polymer foil from first silicon carrier, (6) laminating the chip embedded in foil as a face-up chip on the second carrier, (7) laminating the dry film resist across the whole area and structuring using photolithography to open the inner area in contact with the chip, (8) micro via opening, AlSiCu metal sputtering and structuring, (9) spin coating of polymer symmetrically to the polymer foils below the chip, outer pad opening and noble metal deposition, and releasing CFP foil from silicon carrier.

3.3 Substrate Materials

The materials used in the CFP process are classified in this section as follows: (i) embedding polymer, (ii) reinforcement polymer, (iii) low CTE polymer, and (iv) surface treatment chemicals. Each material in every class has its advantages and limitations, while often the process conditions as well as the interaction of the materials with other layers, have quite an influence on the performance of the complete system. Therefore, the selection of the materials has to be carefully done to meet application and technology parameters, such as thermal, mechanical, and electrical properties.

High-frequency application – The performance as an operation frequency of the system depends on the dielectric behavior of the polymers.

Environmental stability – For the sustainability and proper lifetime of the complete system-in-foil, the sensitivity of the materials to oxygen and moisture has to be well considered. Besides that, depending on the application, the biocompatibility of the polymers should be taken into the account.

Mechanical properties – The mechanical properties include flexibility, bending radius, conformability, and internal stress. Accordingly, the material, design, and process flow have to be carefully chosen.

Process parameters – The process parameters include throughput, temperature, and ambient conditions. For a reliable production, it is important to adjust the process parameters for the different employed materials.

Cost and yield – High volume production is only possible when the processes allow fabrication at an acceptable yield. This includes adjusted materials, reel-to-reel (R2R) as well as in-line quality control for low-cost and high-performance products.

3.3.1 Benzocyclobutene (BCB) as an Embedding Polymer

The benzocyclobutene (BCB)[1] is a well-known material for thin-film applications. The fully cured BCB comes at a temperature robustness above 350 °C [79]. BCB is quite suitable for packaging because of; a) its excellent adhesion characteristic for void-free and strong bonding at low-temperature [46], b) low curing temperature and low curing shrinkage (less than 5 %) [57], c) high planarization capability [89]. For the Chip-Film Patch process, two liquid varieties of photosensitive Cyclotene 4000 and non-photosensitive 3000 series advanced electronic resins (denoted as BCB in this work) are used. The varieties Cyclotene 4024-40 and Cyclotene 3022-35 have a final cured thickness of 3.5-7.5 µm and 1.01-2.26 µm, respectively. They are well-known in the semiconductor industry for use as interlayer dielectrics because of their high perfor-

[1] BCB is from the Dow Chemical Company.

mance cured film properties. An overview of the material properties of the cured BCB film is provided in table 3.1.

BCB deposition

The Cyclotene 4024-40 and Cyclotene 3022-35 both are highly viscous solutions and are deposited on the wafer substrate by either static or dynamic spin coating. The thicknesses of BCB will differ depending on the spin time, spin speed (table 3.3), and open or closed cover coater. The thickness of BCB film in open bowl is usually higher than closed coater [75]. Right after BCB coating, the substrate speed is decreased down

Table 3.3: Layer thickness resulting from different spin speeds for Cyclotene resins [90], [75].

4024-40 thickness (µm)			3022-35 thickness (µm)
Spin speed (rpm)	After soft bake	Final thickness	Final thickness after curing
1500	10.2	7.2	1.84
2000	8.4	5.9	1.59
2500	7.4	5.2	1.43
3000	6.7	4.8	1.3
3500	6.2	4.4	1.21
4000	5.8	4.1	1.13
5000	5.2	3.7	1.01

to 600-1000 rpm and the backside solvent (T1100 Rinse Solvent) is dispensed as an edge bead removal (EBR) to remove any contamination from the back side of the substrate and remove the bead that has formed on the front side edge. After spin coating, the BCB films should be heated a short period of time (80 °C, 90 s) to drive out residual solvent and to stabilize the film. Then, wafers can either go for photolithography or for curing depending on the process requirements.

BCB cure

In the curing step, the BCB film must be under an inert atmosphere at a high temperature (recommended: < 100 ppm of O_2 at > 150 °C) to avoid any surface oxidation [90]. Therefore, the nitrogen purge oven Despatch LCC1-16N-3 is used. Two different cure profiles are commonly used:

soft curing – or partial curing (approximately 75- 80 % conversion) when multiple BCB layers are used in a structure; it provides improved adhesion between the polymer layers.

hard curing – or full curing ($>$ 95 % conversion) as a single layer or the last layer in a multilayer build [91]. The percentage of BCB cure as a function of temperature and time and BCB cure profile are shown in table 3.4. The optimum planarization is achieved with a relatively slow ramp during the curing step.

Table 3.4: BCB cure profiles for convection oven curing [75].

Step	Soft cure	Hard cure
1	15 min ramp to 150 °C	15 min ramp to 150 °C
2	15 min soak to 150 °C	15 min soak to 150 °C
3	ramp to 210 °C	ramp to 250 °C
4	40 min soak at 210 °C	60 min soak at 250 °C
5	cool to $<$ 150 °C	cool to $<$ 150 °C

BCB dry-etch

The cured BCB film is then descummed by a brief exposure to plasma (30 sec). Descumming is necessary to remove a thin film of polymer residue (1000-2000 Å) left behind in the develop process of BCB 4000 series or increase the adhesion on BCB 3000 or 4000 series to the top materials.

Due to the presence of silicon molecules in the BCB monomer, the etching gas mixture needs some fluorine in combination with oxygen to etch silicon molecules. Oxygen plasma without a fluorine component can create an undesirable amorphous silicon oxide on the surface, thus, the etching process becomes self-passivating, and the etch rate slows down and after some point stops. The resulting surface SiO_2 layer is rigid and can lead to micro-crack generation on BCB's surface. In addition, materials which are deposited on top of this oxide (e.g., metals, CYCLOTENE resins) typically show poor adhesion [90], [92].

Recommended etching at a gas mixture of O_2/CF_4 with a ratio of 80 %: 20 % provides a good balance of organic etching by O_2 and silicon etching by CF_4. The BCB plasma etching using a soft or hard mask is done with the same gas mixtures in a parallel plate etching tool Oxford plasma lab system 100. The optimized parameter of BCB plasma etching in the Oxford plasma lab is shown in table 3.5. In addition to descumming, to enhance adhesion of BCB to silicon or patterned metallization, an adhesion promoter, such as AP3000 should be used. In this case, baking the adhesion promoter AP3000 ($\geq$ 80 °C, 60 sec) can help improve the adhesion level.

Table 3.5: Plasma etching parameters used for BCB film [57].

O_2	CF_4	Pressure	ICP	RIE
80 sccm	20 sccm	6 mT	1500 W	50 W

3.3.2 Durimide as a Reinforcement Polymer

In the two-polymer CFP technology (subsection 3.1.1), durimide provides the mechanical flexibility of the system and reinforces the layer stacks. For this work, it was important to choose a polymer with low-curing temperature (250 °C) and high flexibility. In this matter, durimide 32A[2] is suitable. The letter "A" in the name stands for the formulation which has an adhesion promoter in it [76]. An overview of the material properties of the cured film is given in table 3.1.

Durimide deposition

The durimide 32A is dispensed on top of wafer either using a static or dynamic dispensing method. Based on the required final thickness, the speed of the rotation and time are determined. One of the challenges of processing durimide polymer is its high humidity absorption. In this case, after durimide coating, soft bake will be applied in two steps of 75°C, 300 seconds and 110 °C, 200 seconds, respectively.

Durimide cure

The curing needs to be performed with a nitrogen purge so that the residual solvent evaporated from the film can escape the oven as shown in table 3.6. The durimide film is hard cured at a low temperature up to 250 °C.

Table 3.6: Durimide cure profiles for convection oven curing.

Step	Hard cure
1	15 min ramp to 150 °C
2	15 min soak to 150 °C
3	ramp to 250 °C
4	120 min soak at 250 °C
5	cool to $<$ 150 °C

[2]Durimide is made by Fujifilm Electronic Materials.

Durimide dry-etch

After the curing step, as the durimide 32A has a built-in adhesion promoter, no additional processing step is necessary to enhance the adhesion of the deposited film on another polyimide layer. However, to increase the adhesion of another polymer to the durimide's surface, the short descumm (30 sec) by O_2 or O_2/CF_4 plasma is performed [57]. The durimide dry etching using a soft mask and hard mask can be performed either by O_2 or O_2/CF_4 plasma. The optimized etching parameters by using O_2 and O_2/CF_4 are shown in table 3.7 and table 3.5, respectively.

Table 3.7: O_2 plasma etching parameters used for Durimide film.

O_2	Pressure	ICP	RIE
80 sccm	6 mT	1500 W	50 W

3.3.3 PI2611 as a Low CTE Polymer

PI-2600 series polyimide solutions are highly viscous due to their high molecular weight. The cured PI-2600 products have low stress, low CTE, low moisture uptake, high modulus of elasticity, and good ductility for microelectronic applications [77].

PI2611 deposition

PI2611 can be deposited on the wafer surface either using the static or dynamic dispensing method. In either case, it is important to assure that the polyimide is dispensed in the exact center of the wafer. For best results, the coating should be done after polyimide is fully warmed up to room temperature and in humidity level less than 50 %. Besides that, prior to coating, the wafer should be baked on a hot plate (130 °C, 180 sec) to remove all the moisture from the surface of the wafer. Acceleration to final speed should be as slow as possible to allow the polyimide to flow across the substrate.

PI2611 cure

In case of the PI-2600 series, curing temperature up to 350 °C is required to "completely dissociate the carrier solvent, fully imidize the polymer film, complete polymer orientation, and thereby optimizing electrical and mechanical properties" [77]. During the cure of the PIs, a small N_2 flow rate is added to ensure a better removal of water and solvents evaporating from the spin-on PI. Curing of the PI is done in a programmable

vacuum oven, despatch Oven Model LCD1-16-N5, using the cure profile shown in table 3.8 [45].

Table 3.8: PI2611 cure profiles for convection oven curing.

Step	Hard cure
1	45 min ramp to 200 °C
2	30 min soak to 200 °C
3	50 min ramp to 350 °C
4	60 min soak at 350 °C
5	cool to $<$ 150 °C

PI2611 dry-etch

The patterning of the PI2600 series is mainly performed by O_2 or O_2/CF_4 plasma with the same parameters mentioned in table 3.7 and table 3.5. After dry etching, it may be necessary to clean patterned vias of residuals. Short descumm (30 sec) will slightly roughen the surface of the film, which is desirable to enhance the adhesion of metals or the re-coating of subsequent polyimide layers. Adhesion promoters, such as diluted VM-651 or VM-652 are used in the application of polyimide dielectric layers over patterned metallization [77].

3.3.4 Surface Treatment Materials

The hexamethyldisilazane (HMDS) made by MicroChemicals, is used to promote photoresist adhesion on silicon and other substrates. The HMDS promotes adhesion of photoresist on a silicon and SiO_2 surfaces [93]. However, in the CFP technology, opposite to lithography technology, HMDS is applied as a first adhesion lowering layer before coating BCB on silicon carrier, to release the foil easily from the carrier in the final step. On the other hand, as analog to HMDS, the TI Prime from MicroChemicals adhesion promoter improves resist adhesion on substrates, such as Silicon or glass. The TI Prime is applied via spin coating, where a sub mono-layer is adsorbed onto the surface [94]. Similar to HMDS, the TI Prime is acting as a **lowering adhesion layer** between the silicon and coated BCB layer in the **two-polymer CFP technology**. However, the TI Prime act as **an adhesion promoting layer** between the silicon and coated PI2611 on top of the silicon in **low-stress CFP technology**.

HMDS processing procedures

In HMDS process, the silicon substrate is backed from the bottom and top with the temperature 100 °C and 130 °C, respectively. Then, the substrate wafers are primed with HMDS to create the adhesion reducing layer on the wafer. The standard vapor priming process is used during the photoresist coating and in this case is repeated 2-3 times to ensure better surface coverage and achieving thick (= more than a monolayer) HMDS.

TI Prime processing procedures

After cleaning the substrate with acetone and subsequent IPA, the substrate is baked on the hotplate at a minimum temperature of 120 °C for 10 minutes to remove absorbed water from the surface of the substrate. The TI Prime is spin coated on a spin speed at 1800 rpm. The soft bake at 120 °C for 2 minutes is performed afterward. To increase the adhesion lowering feature and avoid any humidity absorption, the BCB polymer should be coated immediately and proceed as usual [94]. The TI Prime in comparison with HMDS is a better option in case of a number of steps and ease of handling.

3.4 CFP Fabrication Process and Optimizations

This section addresses the fabrication process of CFP in details for both face-up and face-down technologies. In this section, we try to avoid any repetition of already published technologies and focus more on the optimization and strategies towards yield enhancement and avoiding any defects in the final complete system-in-foil.

3.4.1 Carrier Substrate Preparation

Pre-surface treatment in CFP technology depends directly on the techniques and corresponding polymers which are used in the next steps. The pre-surface treatment steps for both, the two-polymer CFP technology (subsection 3.1.1) and low-stress CFP technology (subsection 3.1.2), are shown in table 3.9. For both of them, the 150 mm silicon carrier acts as a temporary carrier.

Compensation of stress-induced warpage for CFP

As described before, in the two-polymer CFP technology, stress and strain arise from the deposition of thin films during the embedding process. BCB and durimide which

Table 3.9: Pre-surface treatment steps for the two-polymer CFP technology in comparison to the low-stress CFP.

Step	Two-polymer CFP technology
1	Removing contamination
2	Deposition of 1.5 µm Si_3N_4 for unwanted warpage compensation
3	500 nm structured AlSiCu as alignment marks on four edges of wafer
4	Priming surface of silicon wafer with TI Prime as an adhesion lowering layer
Step	Low-stress CFP technology
1	Removing contamination
2	500 nm structured AlSiCu as alignment marks on four edges of wafer
3	Priming the edge of the silicon wafer with TI Prime as an adhesion promoting layer

are thermosetting materials are fully cured at 250 °C, leading to tensile stress when cooled down to room temperature. The most common technique to measure the total film stress is by measuring the deflection (bow) of a thin substrate on which the film has been deposited. The substrate deflection is measured with the profilometer, and measurement results are shown in Fig 3.9 [95]. Silicon wafer warpage causes several process difficulties while handling the wafer on vacuum chucks during the automated processing steps, such as photolithography and metallization. To avoid such problems, the process induced warpage on wafers needs to be compensated. Identification of the source of the inherent warpage of the process carrier wafer and calculation of the film stress is detailed in Section 5.2.2.

PECVD SiO_2 and Si_3N_4 are ideal for concave warpage cancellation, because both materials have a CTE that is smaller than that of silicon. Therefore, they can be used to produce a compressive stress on the surface of bare silicon before any device processing step [96]. Generated stress due to chemical vapor deposition (CVD) of Si_3N_4 and SiO_2 depends on many factors, such as SiH_4 pressure flow, the ratio of SiH_4 to NH_3 in the process chamber, process temperature, and pressure. Several experiments are performed based on different thicknesses and recipes for Si_3N_4 and SiO_2. Fig 3.10 shows the generated convex bow of the bare silicon wafer by vapor deposition of Si_3N_4 and SiO_2, with different deposition recipe and thicknesses. Based on our requirement for compensating around 150 µm concave warpage, 1.5 µm Si_3N_4 is chosen. The opted CVD recipe of Si_3N_4 with a film thickness of 1.5 µm is shown in table 3.10. Reducing the pressure flow of SiH_4 in case of similar NH_3 flow, can change the substrate

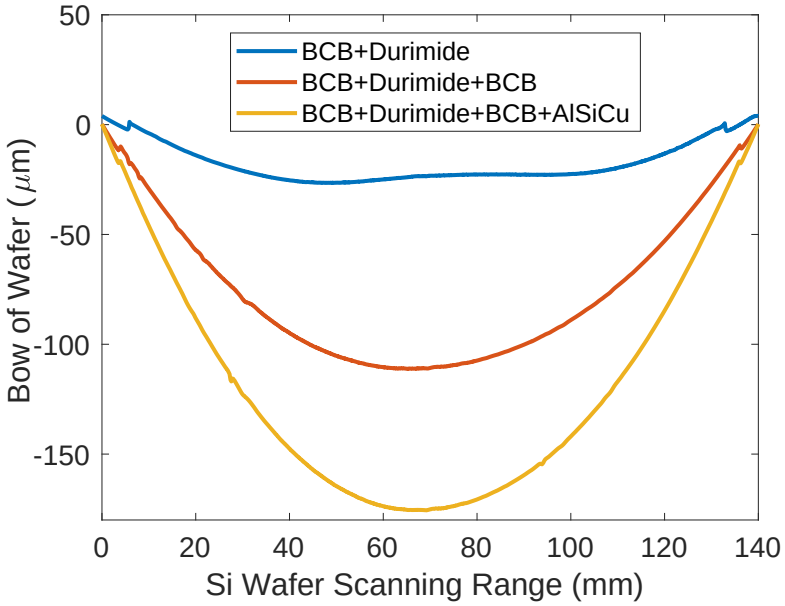


Figure 3.9: 2D bowing plot of a 150 mm silicon wafer with deposited 3.5 µm BCB, 5 µm polyimide, 3.5 µm BCB, and 1 µm AlSiCu in the respective order. The apparent bow was measured after each deposition step, as indicated [95].

conductivity which should be taken into account, depending on the particular device processing and application [95].

Table 3.10: Best achieved PECVD Si_3N_4 deposition recipe for unwanted warpage cancellation of the two-polymer CFP technology.

Si_3N_4 thickness (µm)	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Pressure (Torr)	RF (W)	Temperature (°C)
1.5	150	120	4000	4.7	915	400

With compressive stress induced by Si_3N_4 deposition, in each process step, the amount of stress on the surface is equal to the sum of the stresses from each layer. The initial convex bow of 117 µm on the silicon carrier is reduced to below 90 µm after coating first BCB layer, as illustrated in Fig 3.11. Based on this figure, the primary convex warpage due to the deposition of Si_3N_4 on the silicon wafer will be reduced by thermo-mechanical induced stress of each coated polymer layer on the silicon carrier. Therefore, in the key step of using the processing tool which is AlSiCu metallization and structuring, wafer is in approximately flat state.

During the last step, after releasing the fabricated device in foil, the carrier will re-

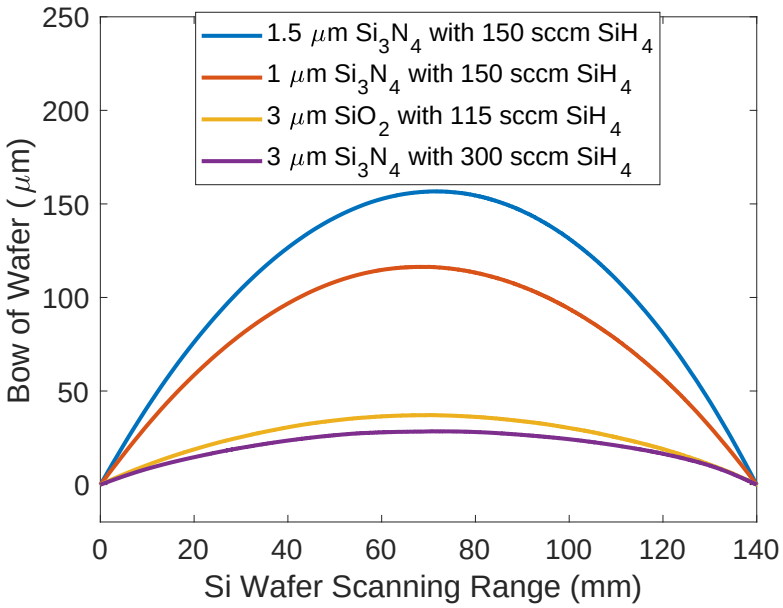


Figure 3.10: Convex warpage on the surface of a 150 mm silicon wafer with vapor deposition of Si_3N_4 and SiO_2 with different deposition recipe and thicknesses [95].

turn to the initial state (convex warpage). Therefore, the silicon carrier can conveniently be reused as a process carrier, which makes the proposed fabrication process cost-effective.

A warpage history plot of the substrate carrier with and without stressor layer during the device fabrication is shown in Fig 3.11. As illustrated in Fig 3.11, without stressor layer, approximately 120 µm concave warpage induces on the silicon substrate carrier up to the AlSiCu metallization step, which makes any handling and further processing impossible.

In the low-stress CFP technology, as the name implies, the technology, the PI2611 with low CTE, induces the little amount of stress to the temporary silicon carrier and the ultra-thin chips embedded inside. Therefore, there is no need to compensate the warpage as is performed in the two-polymer CFP technology. To prove this claim, the silicon substrate warpage is measured after each step of PI2611 coating and is shown in Fig 3.12. The overall warpage of silicon wafer before metallization, can reach up to 20 µm bow. This amount of deformation can be handled with any processing tool without any further difficulties.

The warpage of the substrate is measured at different angles and the overall wafer and is shown in Fig 3.13. As shown in Fig 3.13, the shape of the silicon substrate after coating 15 µm PI2611 is not pure concave and is saddle shape.

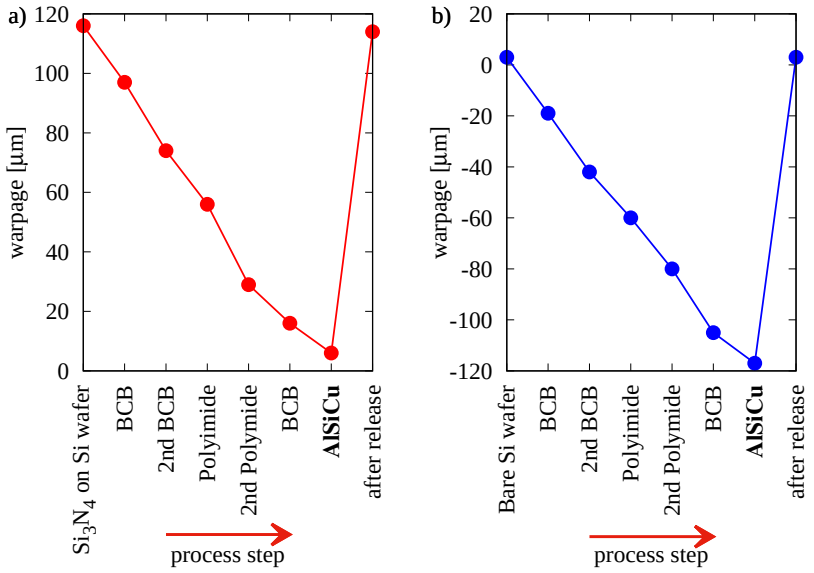


Figure 3.11: Warpage history plot of the substrate carrier with stressor layer (left plot), and without stressor layer (right plot) are shown during device fabrication until release form the carrier [95].

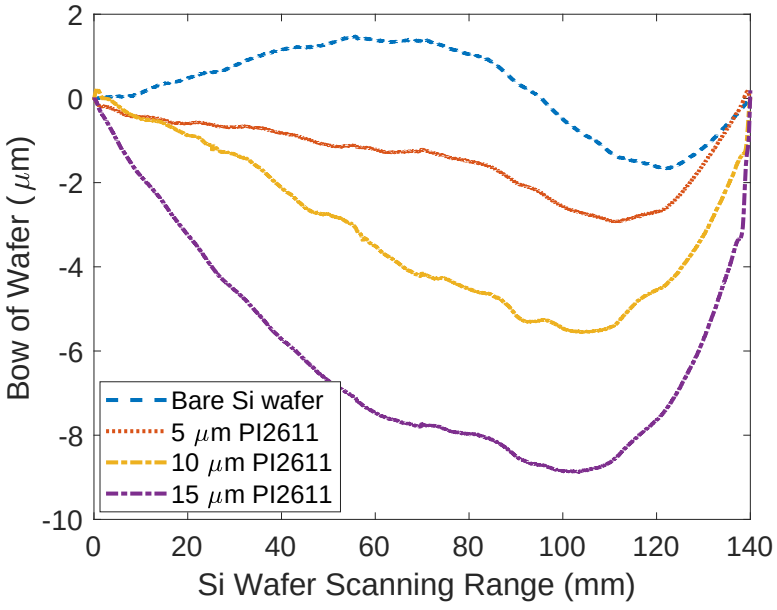


Figure 3.12: 2D bowing plot of a 150 mm silicon wafer with deposited 5 µm, 10 µm, and 15 µm PI2611 in the respective sequence. The apparent bow was measured after each deposition step, as indicated.

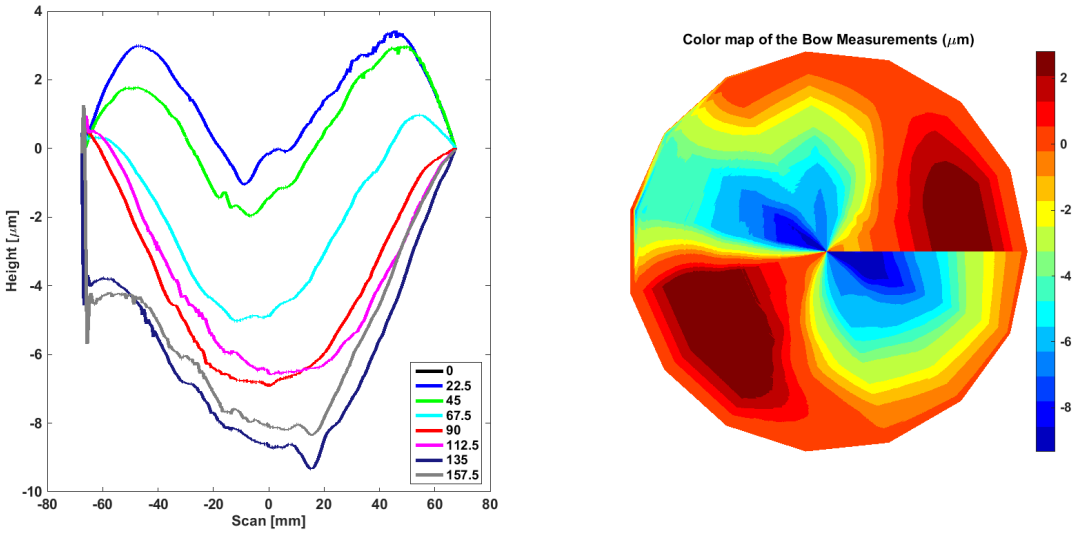


Figure 3.13: 2D bowing plot of a 150 mm silicon wafer, including 15 µm PI2611 all over the wafer. The 2D plot of the silicon wafer based on eight different degrees of rotation (left side), and the interpolated wafer's bow based on profile measurement over the silicon wafer diagonal (right side).

Based on similar experiments with other research groups, two possible explanations are given as, either the regular orientation of molecules caused by the spin-on process or that the biaxial confinement of the spin-on layer during the solvent evaporation resulted in biaxial tensile stress, which leads to anisotropic material properties [97].

Alignment marks on four edges of wafer

Alignment marks are needed to do multi-layer lithography. By providing the location of the alignment mark, it is easy for the operator to locate the correct feature in a short time and so the probability of a misalignment is reduced. Alignment marks should be located on the wafer in the way that the equipment which is used to perform the alignment be able to travel and to align features located within the regions on the wafer. Typically, two numbers of alignment marks are used to align the wafer, preferably spaced far apart, to correct the rotational offsets [98]. The alignment mark in our case is a "+", located on four edges of the silicon carrier ($\pm$4500, $\pm$4500). For this purpose, a thin layer of AlSiCu (500 nm) is sputtered and patterned on top of the carrier wafer. The polymer layers are transparent and, therefore, alignment marks are visible even after the polymer coating. The mentioned alignment marks play an important role in increasing the accuracy of the adaptive layout technique which is going to be described in Section 4.

Adhesion treatment of wafer surface

After generating alignment marks on top of the wafer and before the first step of the polymer coating, depending on the process (refers to table 3.9), the wafer surface is primed with TI Prime. In case of the two-polymer CFP technology, a thin layer of TI Prime or HMDS acts as the weak bond between the polymer layer and the substrate wafer. This bonding force is good enough to keep the foil attached to the carrier wafer, until the end of the process. However, at the same time, the bonding force is weak enough to release the foil from the temporary carrier at the end of process [57].

In the low-stress CFP technology, the bonding between the PI and the silicon carrier is enough to hold the foil intact on the wafer during the process and is released easily at the end of the process. However, the process is optimized further by creating a high adhesion region of about 1 cm along the edge of the wafer by coating TI Prime on the edges of the wafer. In this technology, TI Prime acts as an adhesion promoter instead of the adhesion lowering layer. The TI Prime on the edges of silicon wafer stops the undesired delamination of the foil along the edge during metal sputtering and metal etching steps.

3.4.2 Base Polymer Preparation

In the two-polymer CFP technology, once the adhesion lowering layer is applied, the BCB 4024-40 with the thickness of 3.5 µm is coated and soft cured on top of the silicon wafer. The first BCB layer acts as a protective layer for the top durimide against any moisture absorption or chemical attack. The next layers of durimide 32A with a thickness of 10 µm (2 times coating) is coated as a reinforcement polymer and in order to provide the flexibility of stack. The thickness of the durimide is directly related to the thickness of embedded silicon chip. In our case, we assumed to work with 20 µm thin chips. However, while increasing the chip thickness, the durimide should be coated in additional steps. As the last layer before the chip embedding, again, the thin layer of BCB ($\simeq$ 3.5 µm) is coated on top of the durimide layer to protect the embedded chips from humidity absorption and trapping air.

In the low-stress CFP technology, PI with the thickness of around 5 µm is coated on top of the silicon wafer and completely cured. This work is repeated three times to reach a thickness of around 15 µm before chip embedding.

3.4.3 Void Free Chip Assembly

The CFP technology integrates very thin silicon chips down to 8 µm inside the polymer foils. The ultra-thin chips will be placed face-up or face-down (depending on the

technology) in pre-defined cavities. The cavities are defined using lithography and plasma etching. To find the best size and height for cavities, the group of experiments is performed and the summary of that is as follows;

– The size of cavity = size of the chip $\pm$ 500 µm from each side. This design rule is made based on the limitation of the manual die bonder tool and can change depending on the accuracy of other embedding devices.

– The cavity with the depth of 25 % more than chip's thickness, could break the chip when touching the edge of a cavity by mistake. Besides that, low depth ($\leq$ 2 µm) is not recognized by the microscope during chip embedding step. The best height to avoid damaging chips and any unwanted topographies is around 3.5 µm.

The thin layer of BCB is used as an adhesive glue to embed the chips in the cavities on the foil. The advantage of BCB is its low outgassing characteristic during the curing step which minimizes the chance of air being trapped below and on the edges of chips. In this work, the Tresky T4909 manual die bonder tool is used during chip embedding step.

One of the biggest challenges during the chip assembly step is the warpage of chips which make the handling and embedding difficult. For secure assembly of ultra-thin chips and avoiding micro-cracks on the chips and air traps below chips, many parameters should be taken into account. It is very important to have a void-free bond interface after placement of the chips. These voids can be caused by evaporated water and solvents during the curing, but also by small air bubbles, trapped at the bonding surface during the placement of the chip. Voids on the edge of the chips, especially close to the contact pads on the chip, are one of the important factors for losing metal contact from a metal pad on the chip towards outside on the foil.

The flow-chart illustration of a void and crack free ultra-thin chip embedding in the polymer is shown in Fig 3.14. As shown in Fig 3.14, to avoid CTE mismatch, a thinner BCB is chosen for the low-stress CFP technology. In addition, the size of the wafer piece is at least two times bigger than the chip's size to distribute the applied force from the top weight and to avoid micro-crack generation on the below chips. Besides that, BCB loses its adhesion characteristic shortly after coating (15 min) and , therefore, chip assembly is time-dependent. To increase the number of chips per wafer, a heatable head with a thermal shock up to 100 °C can be recommended.

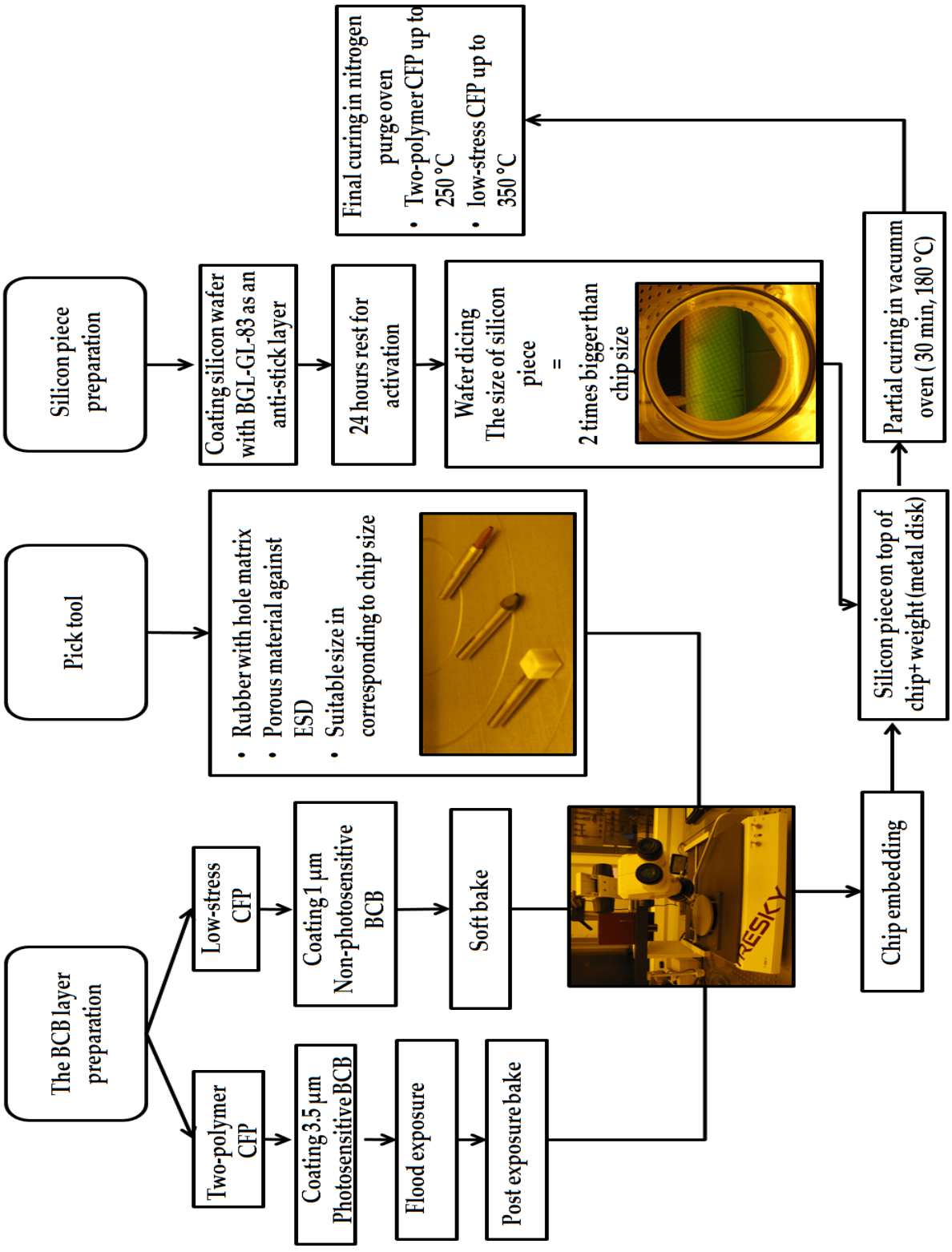


Figure 3.14: Flow-chart illustration of void-free chip embedding.

3.4.4 Polymer Thickness Optimization

After ultra-thin chip embedding in the pre-defined cavity on foil, the surface of the chip is covered with polymer. The top polymer makes a smooth transition from the embedded chip to the bottom polymer foil. However, the CTE mismatch between different polymers as well as the embedding polymers and embedded silicon chips cause internal residual stress inside the film and on the chips. This unwanted stress results in the deformation of the foil as well as the chip. This deformation is more obvious with ultra-thin chips having a thickness comparable to the overall polymer foil thickness. To solve this problem, a group of experiments is performed based on the various thicknesses of the polymer stacks. The summery is as follows;

– The thickness of the top polymer depends on the thickness of the embedded chip in foil.

– The symmetrical polymer stack below the chip and on top of the chip reduce the CTE mismatch effect.

– With the non-symmetrical embedding, the embedded chip warps toward the lower thickness polymer side [57].

– With the low-CTE polymer, the thickness of any polymer except the low-stress PI series causes a huge CTE mismatch and should be minimized to below 1 µm. So, with symmetrical embedding, the embedded chip will be close to the stress-free condition (shown in Fig 3.15).

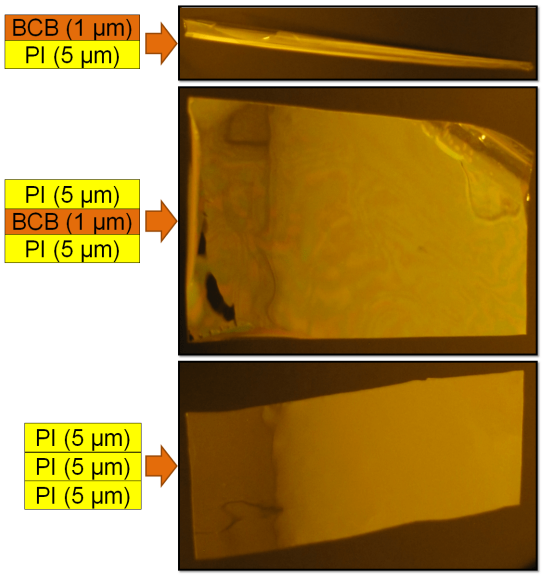


Figure 3.15: Curling effects of a free-standing PI foil as a function of different polymer layers, thicknesses, and the corresponding CTE mismatch.

3.4.5 Sub-Structuring the Embedded Chip

After the chip embedding and planarization step and before the micro-via formation on the pads of the chip, depending on the application, an additional novel technology called sub-structuring chip inside the polymer foil can be performed on the processing wafer. This technology can be applied as a thermal barrier to separate and isolate the thermal source on the chip from other functional units on the chip. In addition, structuring an embedded ultra-thin chip on foil can be a solution towards three dimensional bendability of the system over spherical shapes.

The process development of sub-structuring thin chip is performed using a specific test chip. The process flow for sub-structuring the thin chip after embedding in polymer foil is shown in Fig 3.16. As shown in Fig 3.16, the test chip includes four islands of daisy chains. Also, the ultra-thin test chip with the size of 4.6×4.6 mm^2 and thickness of 20 µm has one metallization layer. As described in Fig 3.16, the ultra-thin test chips

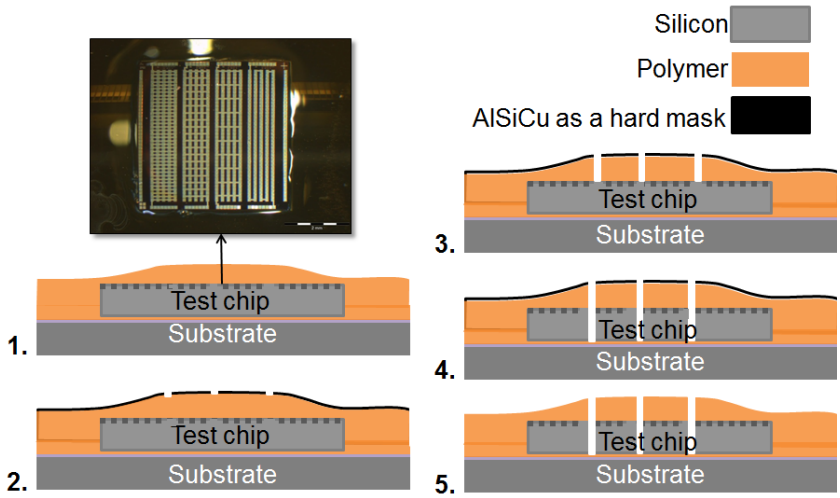


Figure 3.16: Process flow illustration of sub-structuring ultra-thin silicon chip inside foil, 1) embedded ultra-thin test chip inside CFP, 2) metal hard mask deposition and patterning, 3) polymer plasma RIE, 4) Si_3N_4, SiO_2, and Si deep RIE by using Bosch process, 5) removing hard mask and doing further CFP process such as via opening, metallization, metal structuring.

are embedded in the pre-defined cavity using BCB as an adhesive layer. Then, the chip surface is covered with polymer. The alignment marks are defined on the polymer surface using the adaptive layout technique, a laser direct writer lithography tool, and plasma RIE. The reason behind this is that the thin layer of AlSiCu will be sputtered as a hard mask afterward, which covers the surface of the chips and primary alignment marks on the wafer. Therefore, the generated alignment marks before metal sputtering

will increase the overlay accuracy in further lithography steps. After metal sputtering and patterning, the polymer is etched using plasma RIE with the gas mixture CF_4/ O_2. The further plasma etching continues on the silicon surface using Si_3N_4, SiO_2, and Si deep RIE by using Bosch process [99]. After silicon chip structuring, the metal hard mask is removed and the empty area between the silicon chip islands must be filled with polymer. The via opening, metallization, metal structuring, and releasing from the substrate carrier steps follow.

The SEM top view of the structured test chip is shown in Fig 3.17. The concept of sub-structuring the thin chip inside the foil is proven using a simplified scenario including dummy structures and the single metallization layer. However, the process flow will become more complex depending on the chip specifications, such as the number of metallizations, the layout, size, and thickness of the ultra-thin chip.

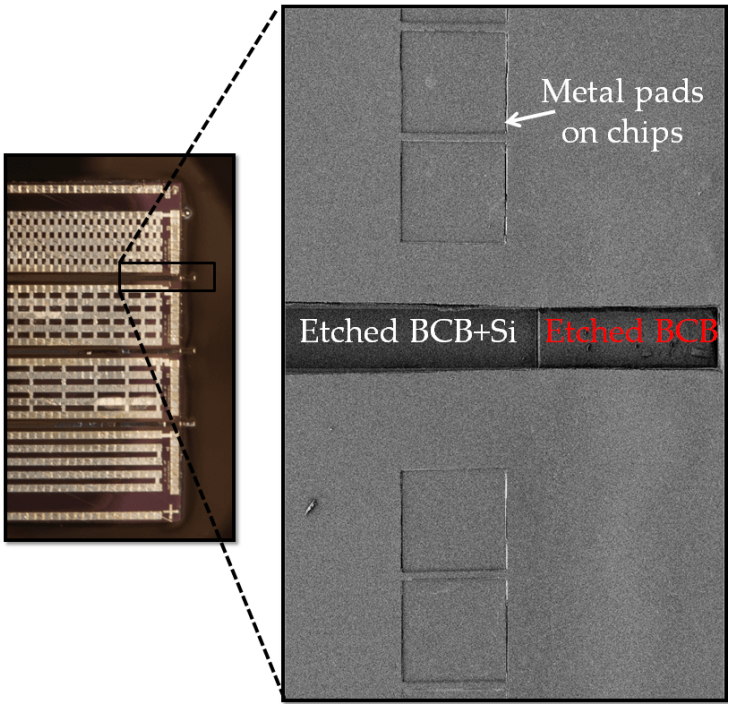


Figure 3.17: Camera image (left side) and SEM top view (right side) of sub-structuring the thin chip in Chip-Film Patch foil using a metal hard.

3.4.6 Micro-Via Formation

After chip embedding and polymer coating, micro-vias should be opened to the contact pads of the chip. The contact pads are opened using dry etching. The micro-via

opening on the polymer film, above embedded chips, can be performed using either a hard mask or a soft mask. The hard mask in CFP technology is developed by two different methods called BCB as a hard mask and conventional metal hard mask. The soft mask refers to the thick layer of the photoresist with approximately same etching selectivity in comparison to the below polymers. The intended purpose of the metal mask is a thin layer ($\simeq$ 600 nm) of AlSiCu. For BCB as a hard mask, oxygen plasma without a fluorine component can create an amorphous silicon oxide on the surface, thus, the etching process becomes self-passivating, and the etch rate of BCB slows down and eventually stops. The resulting surface SiO_2 layer on top of BCB acts as a hard mask for the below polymers and causes the high etching selectivity between BCB and other polymers or photoresists. In Fig 3.18, a short summary of micro-via formation based on using either the hard masks or a soft mask is given. In all cases, plasma RIE is performed using the Plasma lab system 100 manufactured made by Oxford instrument.

One of the biggest challenges in micro via opening on embedded chips is called chip edge exposure. In face-up chip embedding, due to high topography, the thickness of the polymer above the surface of the chip is thicker than the edges of the chip. This phenomenon in this work is called edge bead effect and can cause chip edge exposure during the via opening step. The comparison between three different via opening in CFP technology is shown in table 3.11.In addition, the SEM micrograph of the via profile with AlSiCu and BCB as a hard mask is shown in Fig 3.19. As shown in Fig 3.19, the via profile with metal hard mask is vertical. Despite the sharp sidewalls, the side wall is covered in metallization step and electrical interconnection is achieved. However, in case of BCB hard mask, the via profile follows the shape of patterned BCB. As an example, in Fig 3.19, the top layer BCB is structured using thick resist. Therefore, the resist profile is transferred to BCB and then opened vias.

Table 3.11: Comparison between various via opening technologies.

Mask type	Side wall profile	Minimum via size	Cost	Chip edge exposure	Chip thickness (µm)
AlSiCu hard mask	Vertical side wall	5 µm	++++	No	30-45
BCB hard mask	Over cut	10 µm	+++	Partly	15-30
Resist	Over cut side wall with round shape edges	10 µm	++	Strong	≤ 15

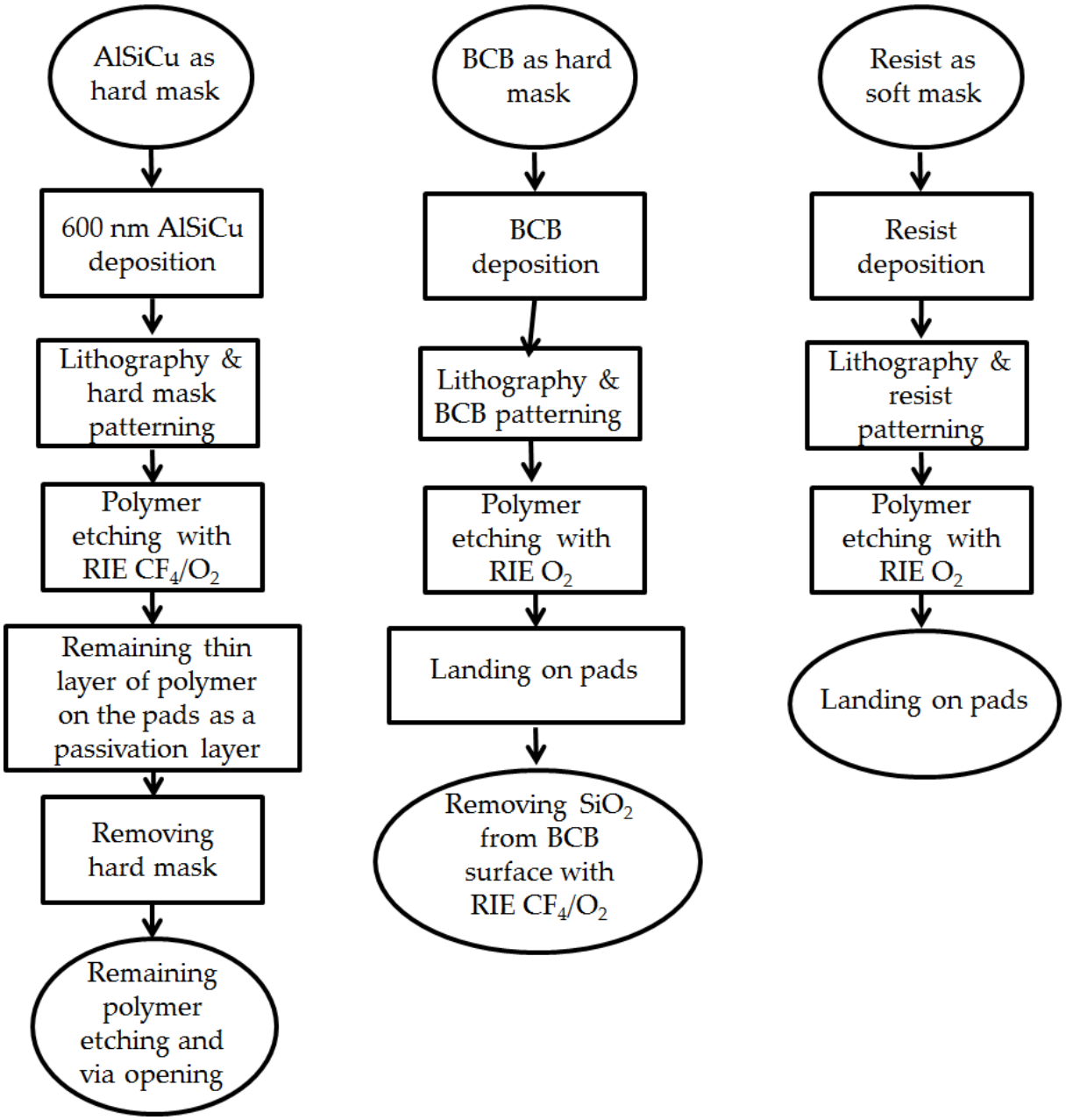


Figure 3.18: Flow-chart illustration of micro-via formation based on various methods.

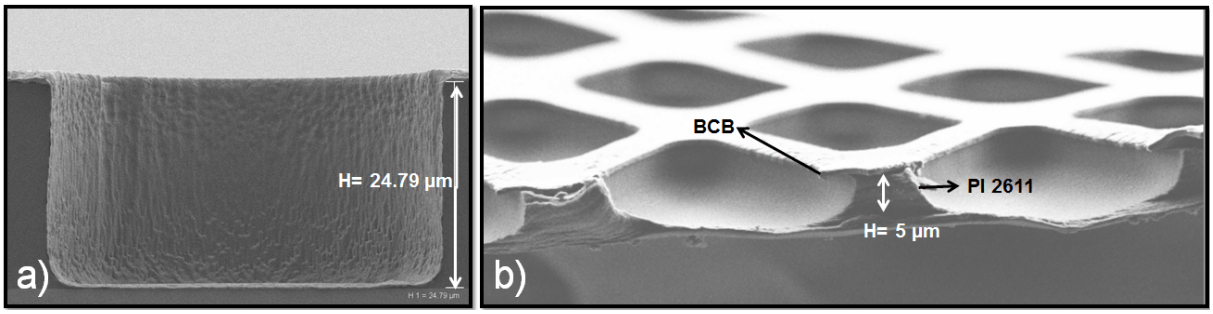


Figure 3.19: SEM micrograph of the side wall profile of via opening by using a hard mask. a) AlSiCu as a hard mask, b) BCB as a hard mask.

3.4.7 Metallization and Metal Interconnection

Once the ultra-thin chips are embedded in the polymer foil and the vias to the contact pads of the chips are opened, the first top metal layer is applied. The metal thickness is around 1 µm and has to provide a good contact from pads on the chips towards interconnection patterns on the polymer foil. Therefore, the adhesion of metal to the below polymer should be ensured. A thin layer of metal can be deposited either by evaporation or sputtering. AlSiCu alloy (98.5 % Al, 1 % Si and 0.5 % Cu [3]) metallization using sputtering and Al using evaporation are employed, respectively. These metals are compatible with the CMOS fabrication technology. The parameters of the sputtering process for the physical vapor deposition (PVD) of AlSiCu , are optimized and given in table 3.12. The AlSiCu is sputtered using an Argon plasma to clean the contact pads on the chips and ensure an adhesion between the polymer and the deposited AlSiCu. With the two-polymer CFP technology, metallization and metal structuring are not possible without a wafer pre-surface treatment and warpage cancellation which is described in subsection 3.4.1.

Table 3.12: PVD parameters for Ar and AlSiCu deposition in Endura tool.

Material	Pressure	DC Power	Temperature	Sputter time
Ar	0.4 mT	125 W	Ambient	30 Sec
AlSiCu	1.9 mT	9 kW	175 °C	70 Sec

[3]The Cu and Si in the alloy reduce the electromigration (EM) speed and spiking, respectively. Therefore, it provides better interconnection results [57].

Moisture absorption

Polyimide materials are known to absorb a certain amount of moisture called swelling. This occurs especially during wet processing (photoresist stripping, etching, etc.) but also when left out in open air and not stored in vacuum conditions. This can affect certain process steps, e. g. evaporating water can cause blistering in sputtered metal layers. To avoid these effects, the substrates are always dried in an oven, after each wet processing step or after longtime storage in open air, and prior to the next processing step. A few minutes (15 min) at 200 °C is usually sufficient to drive off most of the water before metallization [100].

Metal etching and structuring

Metal structuring can be performed either by wet etching or dry etching. One of the drawbacks of wet etching is isotropic etching. Therefore, wet etching is recommended just in case of big and non-critical patterns ($\geq$ 10 µm) or for thin AlSiCu layers ($\leq$ 1 µm). In contrast, dry etching is strongly anisotropic and metal structuring down to 5 µm in the CFP is achievable. With the CFP technology, both technologies are developed and optimized to attain the best metal structuring. Etch parameters for AlSiCu dry etching and resist stripping using the Electrotech Omega 201-2 ICP tool are described in table 3.13 and table 3.14, respectively. Resist stripping is performed right after metal etching in the same chamber without breaking the vacuum to avoid any metal corrosion.

Table 3.13: Etch parameters for 1 µm AlSiCu using the Electrotech Omega 201-2 ICP tool [57].

Cl_2	HBr	ICP	RIE	Pressure	Time
31 sccm	26 sccm	500 W	70 W	8 mT	120 sec

Table 3.14: Optimized process parameter for resist stripping with the Electrotech Omega 201-2 ICP .

O_2	N_2	NH_3	RF	Pressure	Time	Lamp power
300 sccm	15 sccm	30 sccm	300 W	750 mT	120 sec (two times)	50 %

In Fig (3.20), the metallization for a void-free chip embedded in foil is compared to open circuit after metal structuring for the chip with trapped void along the edges. An open circuit occurs due to bad resist lithography which is the consequence of trapped air on the edge of the chip. However, the void free chip embedding is guaranteed

when following the process steps explained in Section (3.4.3). The cross section view of the metal interconnection from active pads on the embedded chip to the surface of the polymer foil is shown in Fig 3.21.

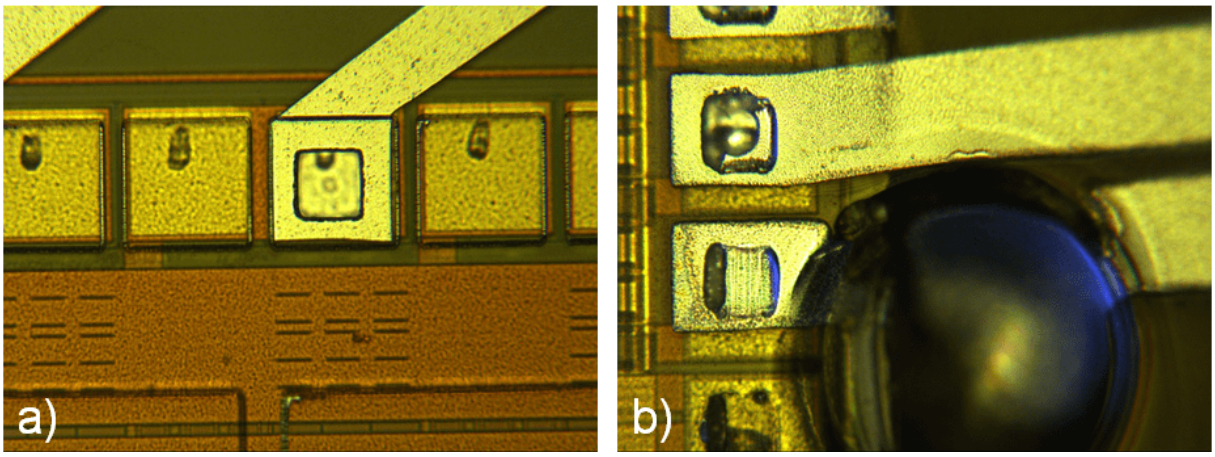


Figure 3.20: Microscopic view after AlSiCu dry etching: a) good metal etching with electrical contact to pads on chip, b) open circuit after metal etching, due to bad lithography because of a big bubble on edge of the chip.

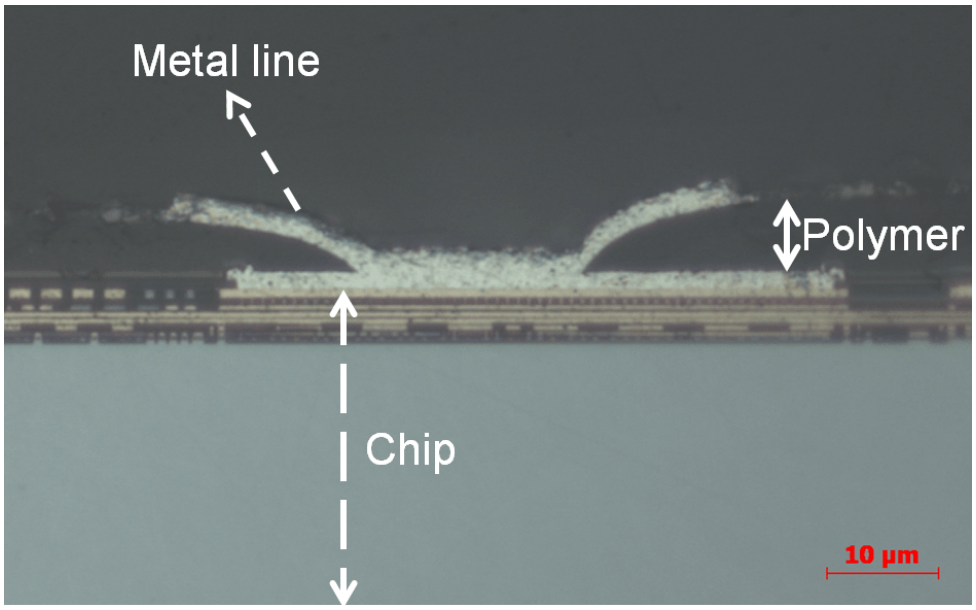


Figure 3.21: Cross section view of the metal interconnection from the active pads on the embedded chip to the surface of the polymer foil.

3.4.8 Top polymer preparation

Once the metal structuring and interconnection is done, the wafer is cured again in the oven to drive off all the moisture which is absorbed during the metallization step. Then, the top polymer is coated to complete the polymer stack and fabricate the symmetrical polymer on the top and bottom of the embedded chip. The adhesion of the polymer on top of the AlSiCu should be improved with the use of adhesion promoter and short descumm prior to the polymer coating.

In the next step, the outer metal pads from the contact pads on the chip towards the foil are opened for second and final metallization. The pads on the foil are usually big ($\geq$ 600 µm) and can be easily opened with either a hard mask or a soft mask (as described in Fig 3.18.

3.4.9 Pad Interface Metallization

The last step prior to the CFP release is the second metallization on the already opened metal pads on the polymer foil. After the release, the CFP is going to either be used as an interposer foil within other foils or be measured as a standalone foil. Therefore, the second metal is deposited as a pad interface metal. In this matter, noble metals, such as Au or Ni/Pd, can be chosen. The electroless nickel/palladium plating is already performed in CFP and the electrical interconnection is partly verified. But, the process is done externally and the deposited nickel layer (thickness of 3 µm) causes stiffness in place of pads which reduces the flexibility of the CFP. Therefore, in this work, an in-house process was developed which is based on Ti/Au evaporation.

Gold is often used in micro-fabricated devices due to its high electrical conductivity and optical reflectivity, combined with a low Young's modulus of 79 GPa [101]. The process flow of the Ti/Au deposition and patterning is illustrated in a flow-chart in Fig 3.22. As shown in Fig 3.22, after resist coating and lithography, short plasma RIE is performed to clean the metal pads from resist residuals and increase the adhesion of top Ti/Au to below AlSiCu pads.

In this case, a negative resist is generally the best choice as a sacrificial layer in the lift-off processes. The negative resists are designed for lift-off to have undercut side walls which prevent the resist sidewalls from being coated and make the subsequent lift-off easier [102]. In addition, the crosslinking of the negative resists maintains the undercut even at very high coating temperatures, which helps to maintain the undercut during metal deposition [103]. The minimum size of patterned Ti/Au depends on: the deposition method, the photoresist side wall, and the percentage of lifted metal in comparison to the remaining one. In our case and with considering all the parameters, we have reached down to 7 µm Ti/Au structuring.

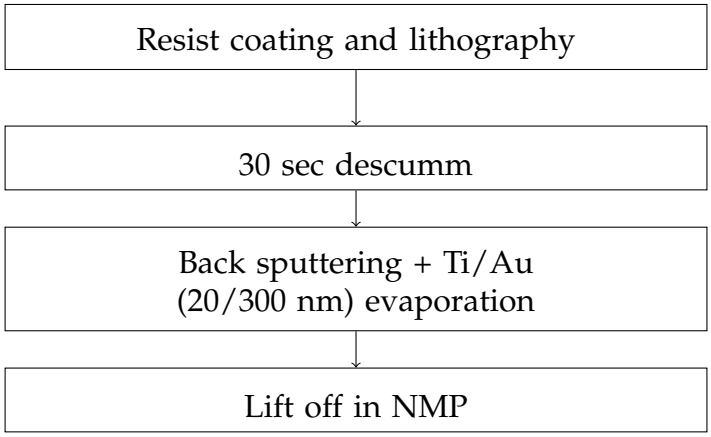


Figure 3.22: Flow-chart illustration of Ti/Au deposition and patterning in the CFP.

3.4.10 CFP Package Release

After the last step of the CFP processing, the CFP foil can easily be cut out from the temporary silicon carrier. This can be done either manually using a sharp blade or, if more precision is needed, by laser cutting or deep RIE etching. Although manual releasing is the easiest and cheapest method to release the CFP from the carrier there is a possibility to generate vertical and horizontal micro-cracks on the edges of foil. These micro-cracks can put the CFP package at the risk of longtime reliability failure. Besides, the size of released foil is limited to the operator's ability. Fig 3.23 shows the manual release of a CFP package from its rigid silicon carrier during the final CFP process step.

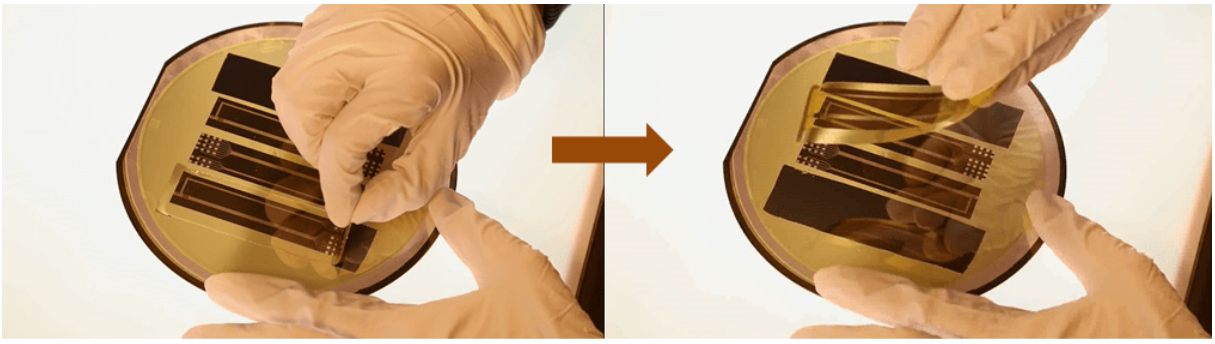


Figure 3.23: Manual release of a CFP package from its temporary carrier.

Laser cutting release

The laser cutting is recommended to avoid any micro-crack generation on edges of polymer foil plus for small size systems which need higher precision. However, in the laser cutting the biggest challenge is to find the correct intensity in order to avoid burning and damaging polymer foil on side walls. Since IMS CHIPS does not yet have a laser cutting capability, this process is carried out in cooperation with NMI in Reutlingen [104] [4].

The purpose is to cut and release the embedded system in the polymer foil with high accuracy down to 100 µm. Therefore, as a demonstration, the embedded silicon needles in the polymer foil are released with the help of an LPKF Proto laser XY. For the laser cutting process, the cutting contour is first created in a CAD program. This CAD layout is also provided with alignment structures, which enable the laser cut to be placed exactly on the corresponding structure. As there are no empirical values for cutting CFP polymer foil on the silicon carrier, preliminary tests are undertaken. The parameters shown in table (3.15) are based on the experience values done at NMI. The

Table 3.15: LPKF Proto laser parameters for cutting and releasing polymer foil from silicon carrier.

Frequency	Current	Speed	Number of exposure
160 kHz	54 A	400 mm/s	6 times

embedded needles in CFP, are placed in the focal plane of the laser. Using an integrated video camera, the set alignment markers are manually approached and transferred to the software. On the basis of this information, the cross section is aligned and lasered into the silicon-polymer substrate. However, in some cases, the edges of the polymer foil are burned and could cause damages (shown in Fig (3.24)), which can make the CFP system mechanically unstable. As a future work, the parameters of the LPKF Proto laser should be further optimized and customized for the CFP.

[4] This work is done in collaboration with Miss Jennifer Erb as her Student project at IMS CHIPS.

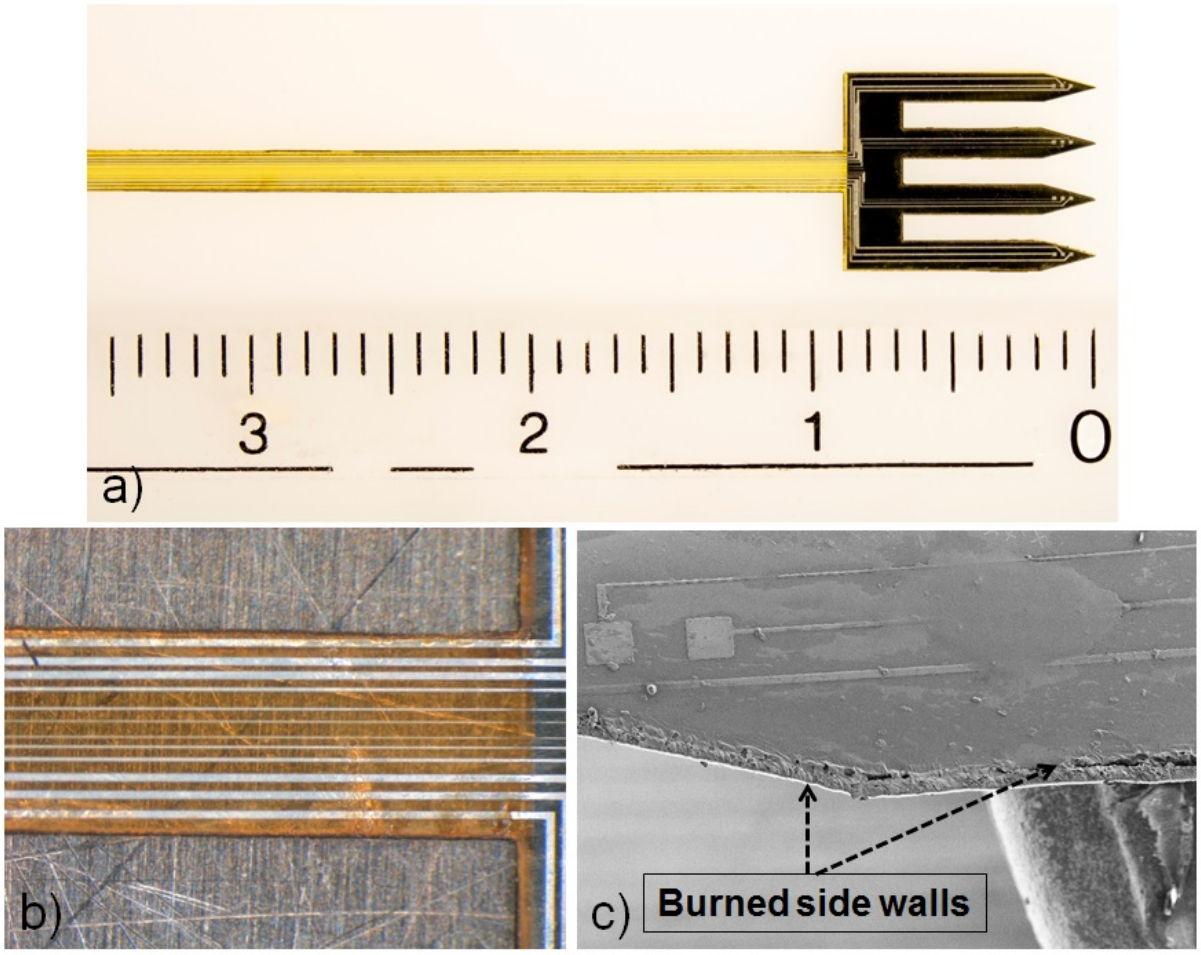


Figure 3.24: Laser cutting of an embedded needle in the CFP package from its temporary carrier. a) Photo of the embedded needle in polymer foil after laser cutting with accuracy down to 50 µm. b) Microscope image of polymer side walls, damaged with a high dose of laser exposure. c) SEM micrograph of polymer sidewall close to the embedded needle after laser cutting.

Deep reactive ion (RIE) etching

The reactive ion etching (RIE) technology is another option in the fabrication of integrated ultra-thin chips in the CFP technology due to the high demand for precise and uniform dry etching either by use of a hard mask or a soft mask. This technology can be extended as a solution for precise polymer foil releasing from silicon carrier in a final processing step. In this case, a hard mask, such as BCB or AlSiCu (depending on the below polymers) is needed and the temporary silicon carrier acts as an etch stop layer. The hard mask should be structured based on the layout which needs to be released from the silicon wafer. The small anchors should be defined on the openings and in the layout in order to prevent the foil to fly after releasing and stay on wafer till the end of the process. In next step, the polymers below the structured hard mask are etched deep down to the silicon carrier.

3.4.11 Wire bonding

A further step after releasing system-in-foil from the temporary silicon carrier is electrical verification. This step can be performed either for CFP as an interposer layer or standalone system. In both cases, wire-bonding from other pads on foil to the outside should be investigated. Therefore, a wafer with daisy chain structures is designed and fabricated to test the possibilities of connecting CFP to outside boards for further electrical measurements without using probe needles. The CFP connection to other boards or wires is an essential feature for the close environment measurement. The longtime reliability test or humidity measurement are examples of measurements which should be performed in a closed environment.

The test wafer is fabricated with the same thickness of polymer stacks as in conventional CFP technology. The two level metallization AlSiCu/Ti/Au with the thickness of 1000/20/300 nm is performed on the wafer. Three interconnection possibilities are tested on top of the dummy wafer (as shown in Fig (3.25)), which can be summarized as follows [5]

– Wire bonding directly on the foil has failed. The foil substrate is too flexible for the wire bonding tool in case of bonding height calibration.

– Copper wire interconnections from metal pads on foil to PCB using conductive silver glue are successfully established. The silver glue added around 5 Ω of resistance.

– Interconnection from the metal pad on foil to the connector with the help of silver glue is achieved. However, to avoid any damage to the foil, the foil is secured on the PCB firmly using adhesives.

[5]The wire bonding interconnection and characterization was done by Mr. Mourad Elsobky.

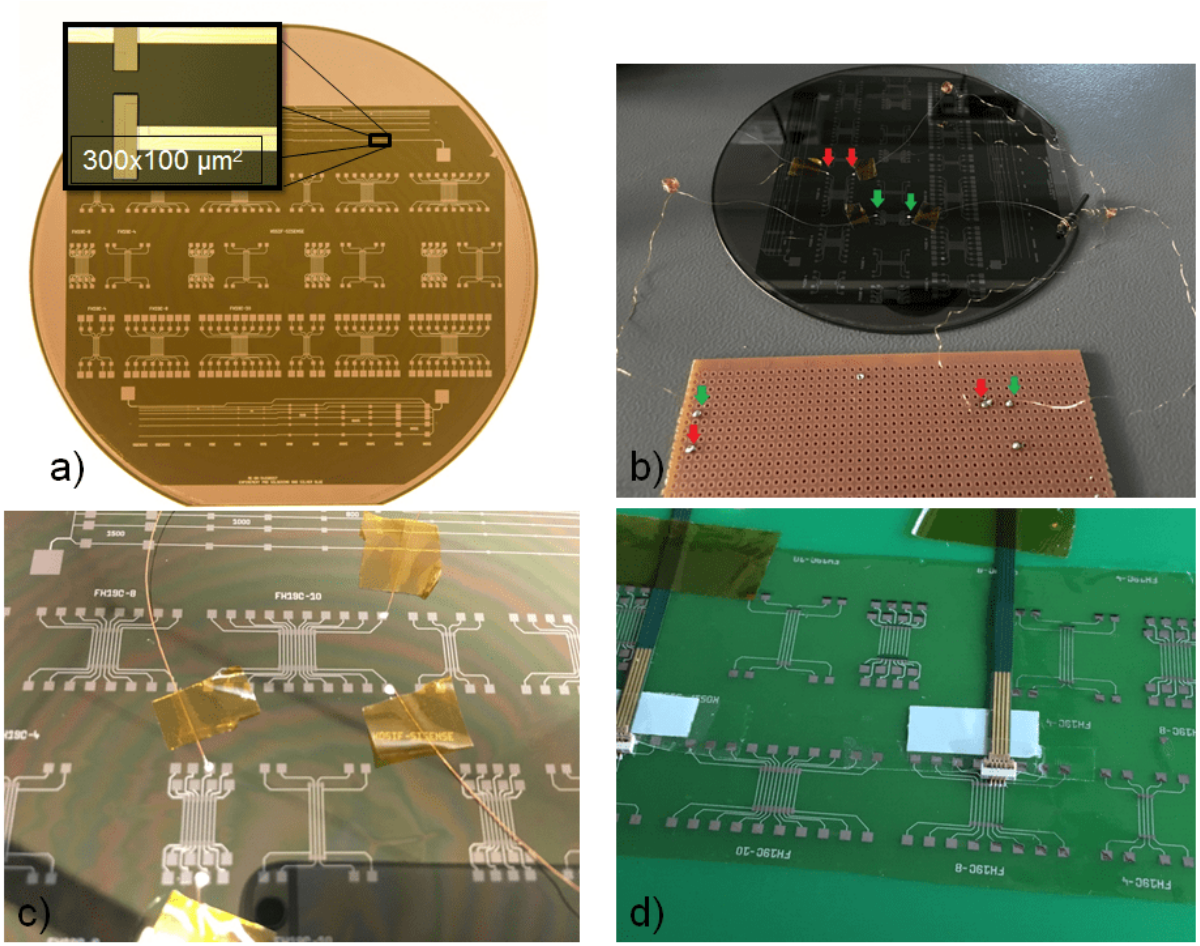


Figure 3.25: Fabricated CFP wafer with daisy chain structures (AlSiCu/Ti/Au) to test the possibilities of connecting the CFP to outside boards. a) Dummy structures with different sizes are fabricated in CFP. The smallest metal pad is 300×100 µm^2.b) An electrical interconnection from the metal pad on the CFP to copper tracks of the PCB is established using silver glue. c) The copper wire was fixed using a Kapton foil tape on top of the wafer for mechanical stability. d) Electrical interconnection from pads on foil to connectors towards the outside is carried out using silver glue. The CFP foil was fixed on top of the PCB board to avoid damaging metal pads on foil.

3.4.12 Foil Transfer to the Second Carrier

The foil transfer is considered as a next step for either the face-down technology and after embedding the chips in foil and before the via opening step or, for the CFP systems with the need of backside processing and as a final step. In both cases, the released CFP foil is transferred to the second carrier with help of the lamination foil, shown in Fig (3.8). The process flow of laminating the CFP foil and the surface opening is as below:

1. The CFP foil is released and placed on top of the surface of the clean silicon carrier. The size of the CFP foil should be smaller than the size of the carrier to make sufficient contact and adhesion between the lamination foil and the below silicon carrier.

2. The TMMF dry film resist from TOK with a thickness of 20 µm is laminated on top of the foil and the carrier. The parameters of the lamination are given in table (3.16). The lamination is repeated based on the thickness of the CFP foil. In this work, the lamination step is repeated up to 3 times (60 µm TMMF foil) to hold the CFP safely until the end of the process.

3. After soft baking the TMMF foil on top of the carrier, at a temperature of 90°C for 5 minutes, the lithography process is performed using the proximity/contact aligner tool EVG 6200NT for 90 seconds to open the inner area in contact with the CFP foil, shown in Fig (3.26). After exposure and during the developing step, the wafer is immersed in 1-Methoxy-2-propanol Acetate (PGMEA) developer for 10 minutes and cleaned at IPA afterwards.

4. In further steps, depending on the application, the laminated CFP is processed. Fabricating the heat spreader on the backside of the chip in foil or via opening for chips with different thicknesses are good examples in this case.

Table 3.16: Parameters of the lamination tool to laminate the TMMF dry film resist on top of foil placed on the carrier.

Temperature of upper roll	Temperature of lower roll	Speed	Pressure	Lamination gap
80 °C	70 °C	16.7 mm/s	4 bar	3.6 mm

After the above processes, the electrical connection of the CFP system-in-foil is verified for further applications. The electrical measurements are described in Section 5.1.

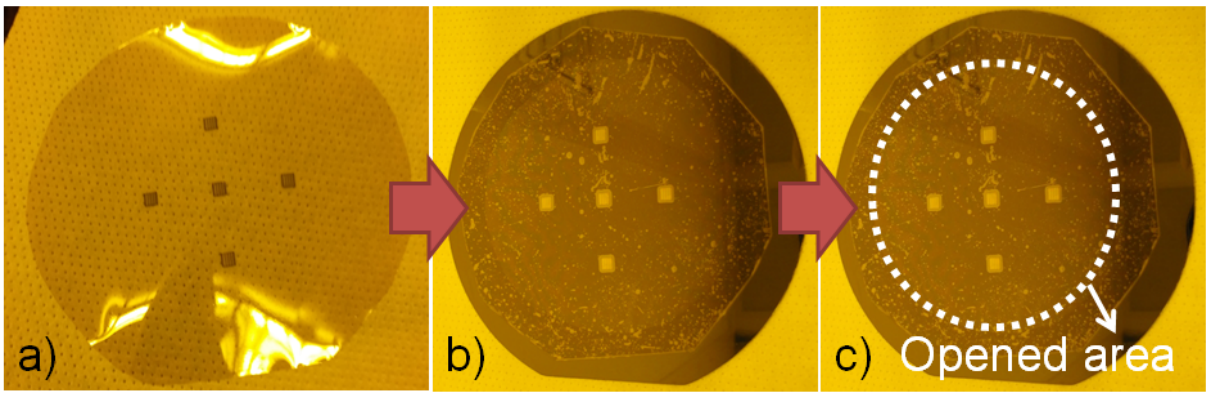


Figure 3.26: Process flow to transfer and laminate the foil to the second carrier. a) The face-down CFP polymer foil is released from the first carrier. b) The CFP foil is laminated to the second carrier. The edges of the foil are fixed on the wafer using a dry film resist (TMMF from TOK). c) The TMMF is removed in the white marked area by photolithography.

3.4.13 Chip-Film Patch Characterization

The Chip-Film Patch technology is an approach to embed and interconnect ultra-thin chips with fine pitches in polymer foil and to enlarge pitches to outer pads on foil. The CFP technology is compatible with IC processing and can be used either as an interposer or standalone foil. The CFP technology can be categorized in two ways, namely face-up and face-down CFP. The SEM image of the face-up CFP cross section with an interconnection from metal pads on the chip to the polymer foil and the bendability of system after the release from the carrier, is shown in Fig (3.27). The summary of the CFP characterization is written in table (3.17). [6]

[6]The Fig (3.27.b) demonstration is developed by Dr. Mahadi UI-Hassan during his PhD in IMS CHIPS.

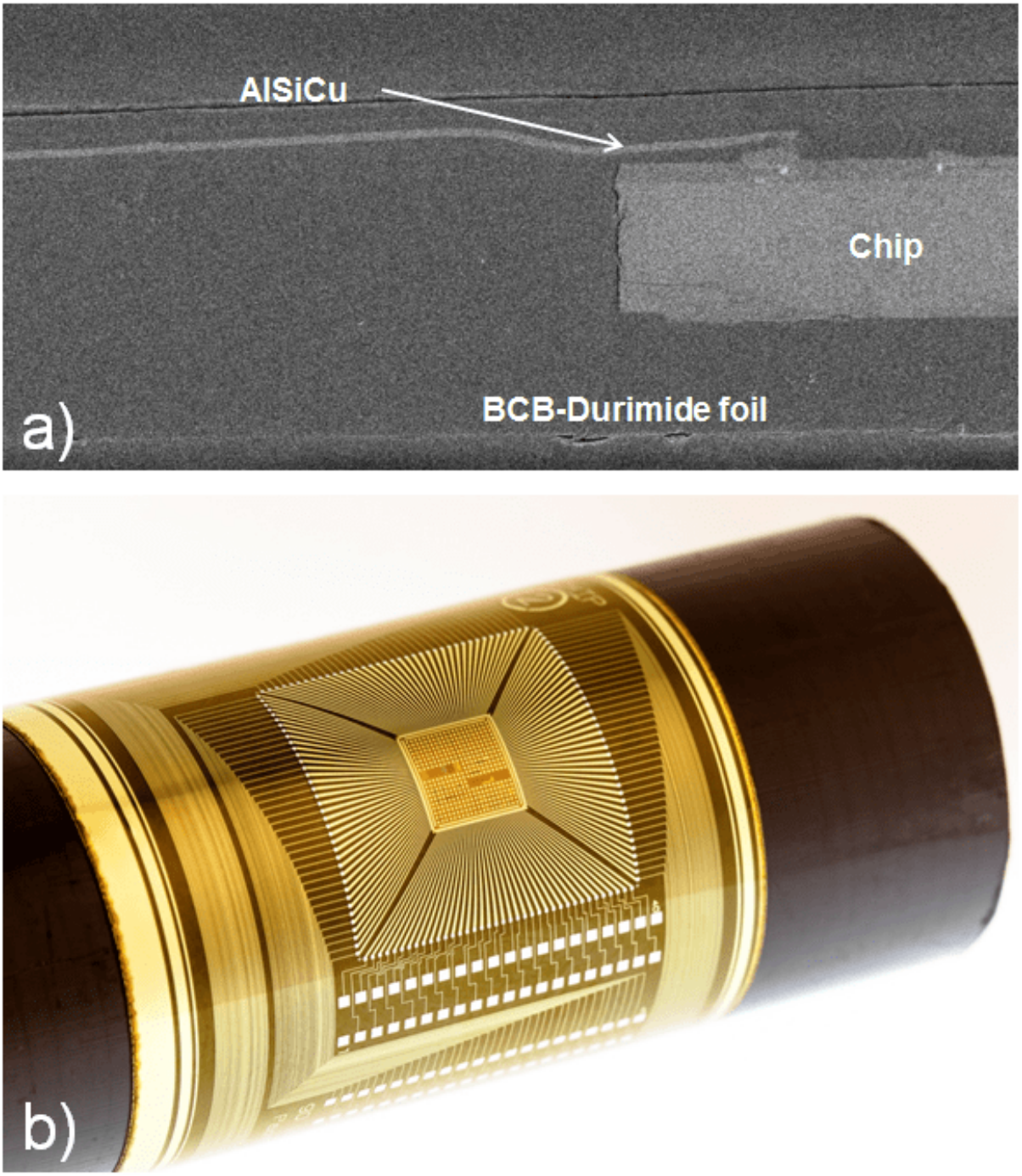


Figure 3.27: SEM cross section of the CFP and its bendability. a) SEM micrograph of its cross section showing the chip along with the metal interconnection through a micro via on chip pad. b) Demonstrating the bendability of CFP.

Table 3.17: Summary of the Chip-Film Patch technology.

Total thickness	depending on the thickness of embedded chip in foil $\Rightarrow$ 20 - 100 µm
Chip thickness	8 - 50 µm
Chip size	≥ 1 mm^2
Embedding materials	PI, Durimide, BCB
Minimum pitch on chip	10 µm
Minimum metal pad on chip	5 µm
Bendability of foil without chip	≤ 100 µm
Bendability of foil with chip	≥ 4 mm radius of curvature

3.5 Summary

The CFP concept and different technologies with the corresponding process flow of embedding ultra-thin chips in CFP are discussed in detail. Ultra-thin chips with the thickness between 10 and 50 µm can be packaged between two polymer layers and the result is a very thin and bendable system-in-foil, with a total thickness of maximum 100 µm and fine pitch interconnections. The issues and corresponding solution are described as well. In summary, CFP technology as a face-up CFP concept is proven and optimized for two technologies namely, two polymer CFP and low-stress CFP. On the other side, the major concept of the CFP technology as a face-down is proven and further optimization needs to be done in the future.

CHAPTER 4

ADAPTIVE LAYOUT TECHNIQUE FOR HYBRID SYSTEM-IN-FOIL

> "Just when you think you know something, you have to look at it in another way. Even though it may seem silly or wrong, you must try!"
>
> — Dead Poets Society Movie

The Hybrid Systems-in-Foil (HySiF) include embedding and interconnecting multiple ultra-thin chips in a polymer film. The integration of different components, such as microcontrollers, sensors, antennas, and near field communication (NFC) into a flexible foil is an interesting topic for a new generation of electronic systems, among others, towards industry 4.0 [105]. In this matter, the CFP process is extended to embed and integrate more than one ultra-thin chip in foil called micro-hybrid Chip-Film Patch process. Therefore, in cooperation with industry, a hybrid combination of microchips with printing techniques and organic electronics (OTFTs) is demonstrated as being intelligent and autonomous systems, which must also be flexible and robust in the long time run. The process flow to embed and interconnect multiple chips in CFP, its restrictions, and accomplished technologies together with CFP are the topics of this chapter.

4.1 Hybrid System-in-Foil Introduction Towards Industry 4.0

The Internet of Things (IoT) is one of the recent movements in the field of information and communication technology (ICT) which will impact every aspect of our future

lives: the small size complex systems interconnected to each other and to the internet. This complex and smart system will communicate with human users to increase the quality of life. One of the relevant topics in this field is "ambient intelligence" which refers to the potential of IoT system to receive data from the surrounding environment, do additional computing, and interact with users [106]. Industry 4.0 is universal automation, production, and data transfer to enhance the available technologies, generate new solutions, and overcome existing barriers. The term Industry 4.0 was revived in Germany (2011 at the Hannover Fair [107]), yet the ideas are in congruity with worldwide activities, including "ambient intelligence, smart factories, Industrial Internet of Things (IoT), and advanced manufacturing". Open source software, open communication, and ease of accessing to data models and data processing makes the implementation of Industry 4.0 attractive. One other term which describes Industry 4.0 is "cyber-physical systems (CPS)". CPS refers to interaction and interconnection between various embedded intelligence systems, such as sensors, actuators, MEMS, functional chips, and antennas [108]. In Fig 4.1, the four industrial revolutions are illustrated and the fourth revolution belongs to Industry 4.0 which includes CPS, IoT, and embedded computing technologies.

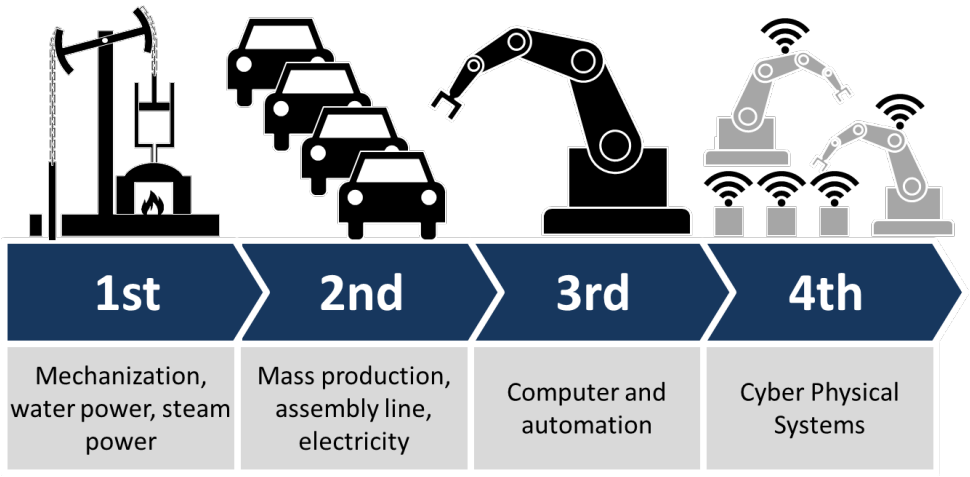


Figure 4.1: Industry 4.0, the four "industrial revolutions" [108].

Flexible and stretchable electronics can cover diverse surfaces, gather various kinds of data, record the related information, and send them to a qualified user. Therefore, these technologies are considered capable of future IoT applications, such as healthcare and wearable technologies towards Industry 4.0 [109].

However, co-integration of silicon-based data processing units and advanced materials based flexible sensors with simultaneous sensing capability calls for heterogeneous integration strategy and system in package instead of single chip and the single-chip package, respectively [110]. In this matter, the CFP technology is extended to a complex

system-in-foil integration, including multiple ultra-thin silicon chips embedding and interconnecting, sensors, organic thin-film transistors (OTFT), wireless antennas, and other available technologies. In all cases, the CFP technology can be used either as an interposer foil or a standalone foil system.

4.2 HySiF CFP Process Flow

The micro-hybrid multiple chips interconnect in CFP technology and integration with other sensors and technologies is developed as a face-up CFP technology for both, the two-polymers CFP and the low-stress CFP. The key element of all the available technologies is the precise control of the thickness uniformity of each individual ultra-thin chip. This property plays a crucial role in the face-up chip interconnection in the polymer foil. Any thickness deviation can cause unwanted topography and further challenges in the micro-via opening step and further metal interconnections. The schematic process flow of embedding and integrating the multiple ultra-thin chips with the help of the micro-hybrid CFP technology is depicted in Fig (4.2). The micro-hybrid CFP technology follows similar process steps as the CFP technology to embed single chips in polymer. The difference lies in the micro-via opening step and the metal interconnection between chips, which are described in the following.

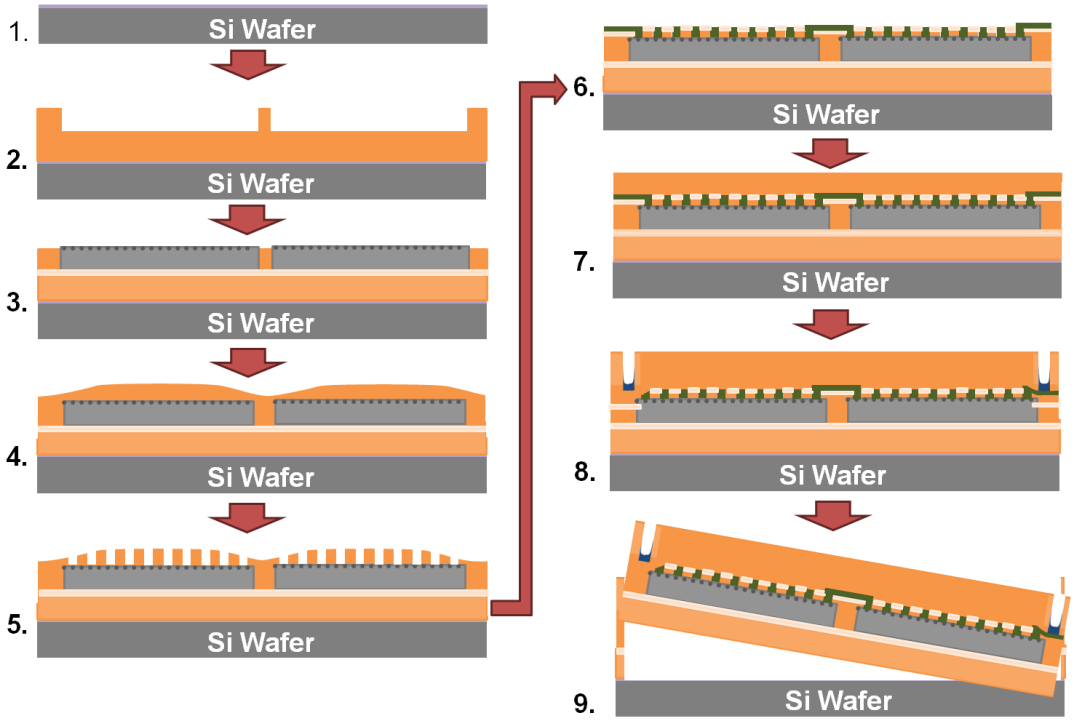


Figure 4.2: Schematic process flow of the micro-hybrid CFP (1) pre-surface treatment includes: removing contamination, deposition of 1.5 µm Si_3N_4 for unwanted warpage compensation, 500 nm structured AlSiCu as alignment marks on four edges of the wafer, priming silicon wafer with adhesion lowering layer, (2) spin coating of polymer, cavity opening for chip placement, (3) chips assembly inside cavities, (4) covering the surface of chips with polymer, (5) chip coordinates measurement and modifying original layout with the adaptive layout technique, micro-via opening, (6) AlSiCu metal sputtering and structuring, (7) spin coating of polymer symmetrically to the polymer foils below the chip, (8) outer pad opening and noble metal deposition, (9) cutting from side and releasing micro-hybrid CFP foil from silicon carrier.

4.3 Challenges of Thin Die Assembly in Polymer Foil

Chip assembly is performed by using a manual die bonder and component placer (Tresky-4909). During the chip placement step in the defined cavities, the limited accuracy of the chip placement and subsequent processes lead to an unwanted rotation and positioning offset for each chip. Beside the accuracy of the chip placement tool, there will always be an amount of offset due to an unwanted movement of the chip on top of the foil during the curing and hardening step, which leads to an undefined offset [74]. This undesirable misalignment and rotation error has detrimental consequences for the metal interconnects, thus, calling for a revised layout with far larger process bias (Fig 4.3).

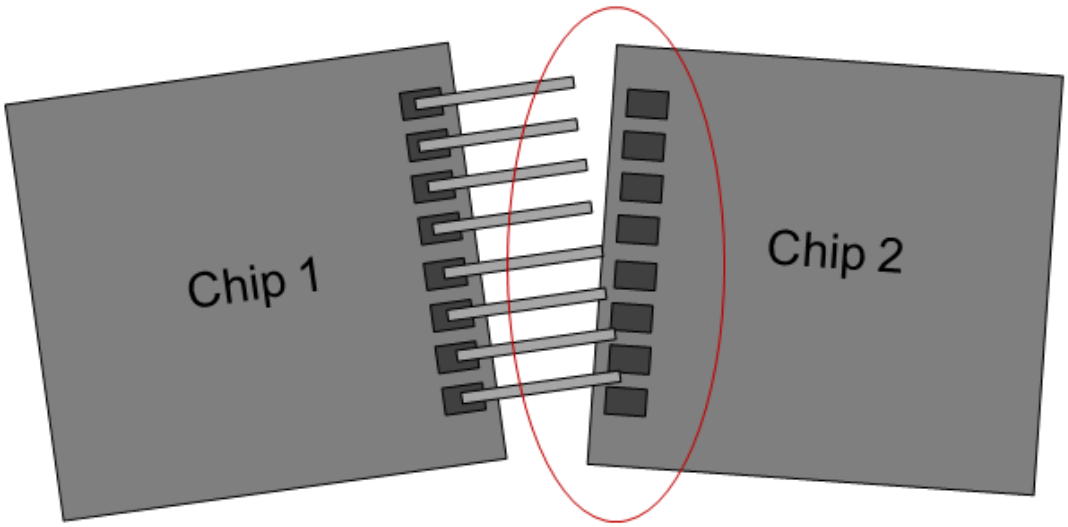


Figure 4.3: Illustration of the consequence of an unwanted chip rotation after the chip assembly. In this illustration, the red rectangular represents the metal pads on chip 2 which should be connected to active pads on chip 1. The interconnection between the two chips can be achieved with the larger interconnection pads.

This, however, contradicts the CFP concept for the fine pitch interconnection. A first potential solution comes with separate layouts for each chip as well as for the interconnects between the chips, which join at rather large pads on the foil to account for the severe process bias. Although this method can technically solve the problem, it is unacceptable from an economic point of view, because it requires three or more lithographic processing steps. Besides process costs, the minimum pad size for the interconnections will substantially be enlarged. To explore the idea of multiple lithographic steps to interconnect the chips, two ultra-thin chips with the thickness of 20 µm and spacing of 200 µm are embedded in the polymer foil, as shown in Fig 4.4. The metal structuring is

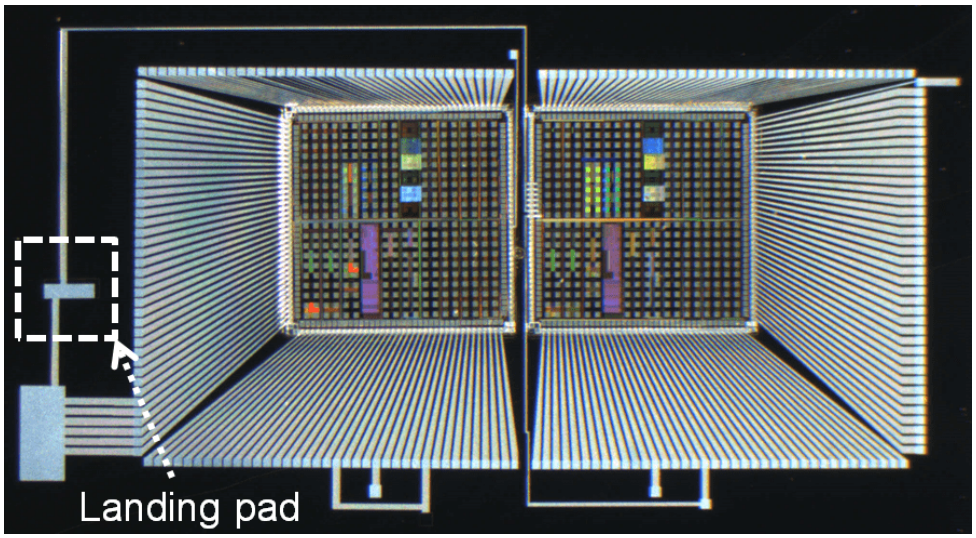


Figure 4.4: A pair of ultra-thin chips embedded and interconnected in foil with extended measurement pads outside. The metal structuring step is done using the individual patterning method, including double exposure. With the individual patterning method, the minimum pad size for the interconnections will substantially be enlarged (landing pad) [7].

done by using the individual patterning method in double exposure. In order to compensate the misalignment, the interconnecting pads between two chips are enlarged. However, a truly practical solution to interconnect those misaligned chips embedded in the CFP results from an adaptive layout with maskless lithography, which is described in the next section.

4.4 Adaptive Layout Concept

As the name suggests, adaptive layout technology is a technique in which the original interconnect layout between the embedded chips in foil will be adopted based on rotation and misalignment of the embedded chips in the polymer foil. The concept of the "adaptive lithography method and system" is well known and was introduced by General Electric (GE) in 1986 [111]. In addition, Deca Technologies already published Fan-Out Wafer-Level Packaging (FO-WLP) with high-throughput by using the process called adaptive patterning [112]. However, in this work, the adaptive layout technique is extended in the embedded chip in flex application including multiple chip integration and interconnection in CFP. Besides that, in the presented technique, the process steps including chip coordinates measurement and patterning are done in the maskless

laser direct writer. In contrast to conventional lithography based on mask preparation prior to wafer processing, a maskless lithography allows adapting of the layout after analyzing the apparent process bias. In the adaptive layout technique, after the chip assembly on foil, the coordinates of each embedded chip are measured. The measurements are done by using the automatic alignment mark detection system of a laser direct write lithography tool (HIMT VPG400 LaserWriter). The offest and rotation of each chip is calculated based on the coordinates of the chip in the original layout and corresponding measured coordinates after embedding. Then, the calculated offset, defined customizable area, and original interconnect layout are imported into the adaptive layout script (written in Perl), which automatically adapts the interconnection design for each individual set of chips. The Perl script to adjust each original layout to the corresponding chip's coordinates after embedding is illustrated in Appendix A. The diagram of the adaptive layout process step is shown Fig 4.5. The lithography can be done directly after the adapting layout, using the same laser writer with submicrometer accuracy and without a physical mask. To increase yield and reduce costs, the adaptive layout is extended to wafer level as well.

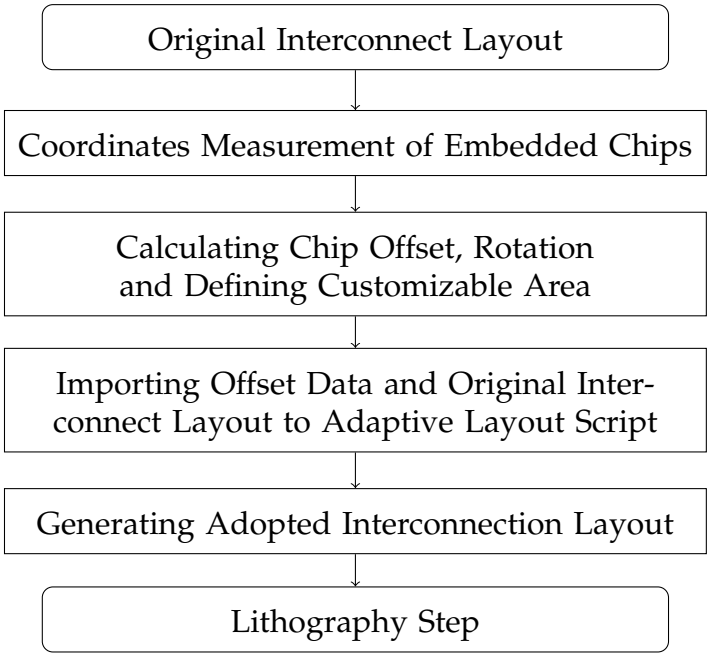


Figure 4.5: Diagram shows the adaptive layout process step. Measurements are done using the automatic alignment mark detection system of a laser direct write lithography tool [7].

4.4.1 Maskless Laser Direct Writer Lithography Tool

The HIMT VPG400 Laser writer by *Heidelberg Instruments Mikrotechnik GmbH* is a maskless lithography tool. The VPG+ small area systems feature a high power pulsed UV laser source with a wavelength of 355 nm, reasonable for i-line resist lithography. The laser writer is capable of accommodating substrates up to 200×200 mm^2 or 400×400 mm^2 in size, respectively. Systems are equipped with an automated alignment capability and an integrated metrology system [113] (Fig 4.6). The advantage of laser writer

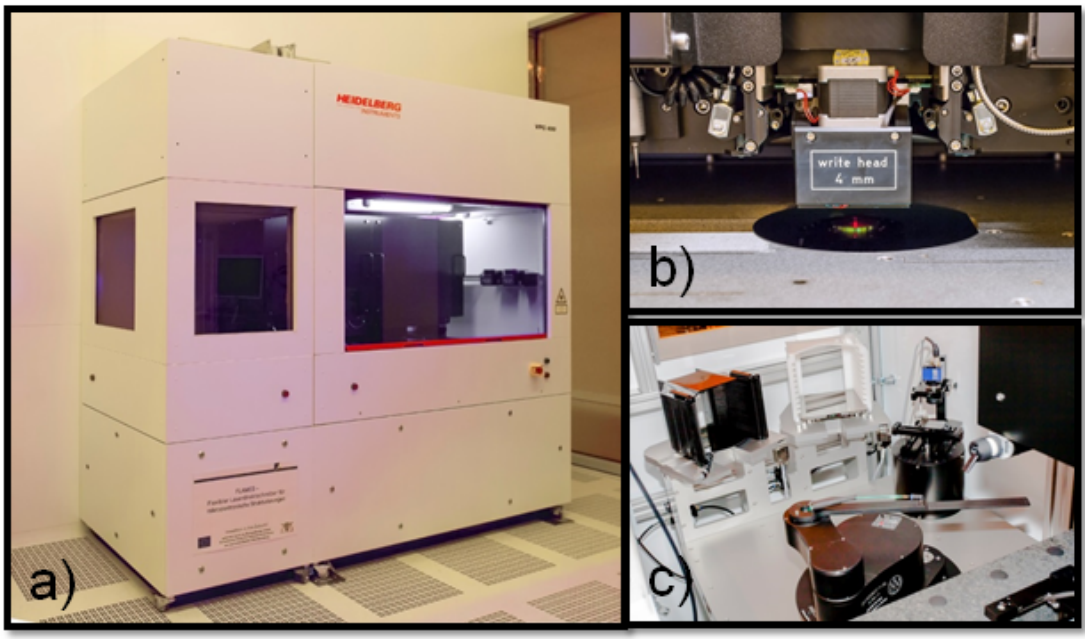


Figure 4.6: The VPG400 Laser writer by *Heidelberg Instruments Mikrotechnik GmbH*. a) The laser writer is a maskless lithography tool, which is capable of large area patterning. b) Three exchangeable write heads (4 mm, 10 mm, and 20 mm) with different resolutions and throughput are available. c) Automatic loading system.

as a lithography tool can be summarized as below;

- A flexible and cost-effective technique to pattern large areas in an acceptable time frame.
- For VPG, the exposure time is independent of the pattern complexity.
- No mask is required. In this case, design changes like adaptive layout can be perused without any delay.
- Mix and match with other lithographic techniques is possible.

- Exposure of high topography substrates with special write head with increased working distance is possible.
- Three interchangeable write heads with different resolution and throughput are available. In case of CFP technology, all the substrates are processed with 10 mm head, which tolerates high topographies (up to 40 µm) as well.
- With the 10 mm head, the minimum feature size and overlay accuracy is 1 µm and 350 nm , respectively.

Besides the general properties of the laser writer, there are key features which make it suitable for the adaptive layout technique. These key features are summarized as follows;

- Multiple data input formats (DXF, CIF, GDSII, Gerber, STL)
- Online data transfer
- Metrology and alignment system, to detect the alignment marks and align the wafer. This property plays an important role in during the multiple lithography steps.
- Edge detector unit, to find the center of the wafer.

4.4.2 Adaptive Layout Process Flow

The process flow of the adaptive layout is shown in Fig (4.5). Based on that, the original interconnect layout between the chips on a wafer level is designed. The original layout includes cavity openings for chips, the layout of silicon chips, via openings on metal pads of the chips and, finally, the metal structuring and metal interconnect between chips. For each layout design, the design rules, such as the size of the cavity in comparison to the size of the chip, size of the via in proportion to the size of the metal pads on the chip must be taken into account.

For offset and rotation calculation, at least two coordinates of each chip in the original layout, (X_1, Y_1) and (X_2, Y_2), must be taken into account (shown in Fig (4.7a)). For this purpose, chip alignment marks or any visible feature with the known position on the chip can be considered. The corresponding two coordinates of each chip after chip assembly, ($X_1^{'}$, $Y_1^{'}$) and ($X_2^{'}$, $Y_2^{'}$), are measured by using an automated laser direct write lithography tool. In this case, the zero point of original layout should be the same as the defined zero point of the wafer in chip position measurement in laser writer.

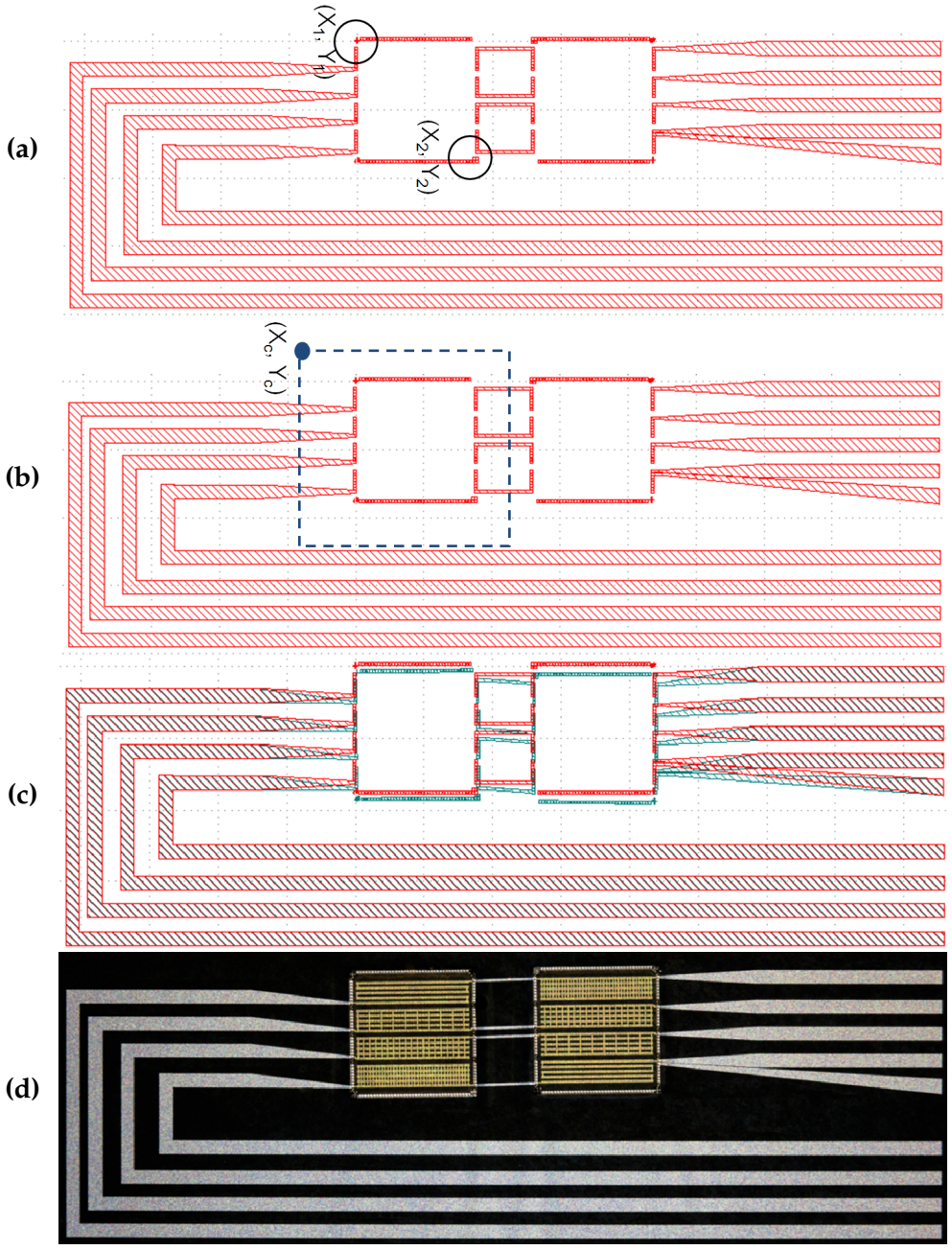


Figure 4.7: Concept of the adaptive layout technique and the final interconnected chips in the CFP. (a) Two coordinates of the chip in the original layout are taken into account to calculate offset and rotation. (b) The customized area is defined with a blue rectangle around two chips. (X_c, Y_c), stands for the center of rotation for the left chip in the adaptive layout script and should be defined for each individual chip. (c) The red color indicates the original layout and the green color stands for the adopted layout of the two chips after assembly. (d) Two chips integration and metal structuring based on the modified layout [114].

The rotation angle (α) can be calculated as follows:

$$\alpha = \arctan(\frac{(Y_1{}' - Y_2{}')}{(X_1{}' - X_2{}')} - \frac{(Y_1 - Y_2)}{(X_1 - X_2)}), \tag{4.1}$$

In the adaptive layout, the customizable area is defined by the user. This way, the interconnect layout is adopted in a defined area and the rest of the layout remains unchanged. In Fig (4.7b), the customized area is defined with the blue rectangle around the two chips. In this figure (X_c, Y_c) stands for the center of the rotation in the adaptive layout script and should be defined for each individual chip.

The scaling factor (K) compensates a possible difference of scaling and can be calculated by use of:

$$K = \sqrt{\frac{(Y_1{}' - Y_2{}')^2 + (X_1{}' - X_2{}')^2}{(Y_1 - Y_2)^2 + (X_1 - X_2)^2}}, \tag{4.2}$$

The chip fabrication tool has a different scaling factor in comparison to the laser direct writer tool. Although the derivation is less than 0.05 %, with considering that effect (K), one can reach a higher degree of resolution in the adaptive layout technique.

The relative offset of each chip after assembly to the original layout, (X_{offset}, Y_{offset}), can be calculated by inserting the defined centering point (X_c, Y_c) and measured coordinates, K, and α in equation 4.3. In the adaptive layout script, in order to adapt each chip to the determined offset and rotation, the zero point of chip shifts to the defined center of rotation. Therefore, the effect of (X_c, Y_c) should be taken into account and cancelled at the end of the adopting process. This work is repeated for all the chips all over the wafer.

$$\begin{bmatrix} X_{offset} \\ Y_{offset} \end{bmatrix} = \begin{bmatrix} X_1{}' \\ Y_1{}' \end{bmatrix} - \begin{bmatrix} K\cos\alpha & -K\sin\alpha \\ K\sin\alpha & K\cos\alpha \end{bmatrix} \begin{bmatrix} X_1 - X_c \\ Y_1 - Y_c \end{bmatrix} - \begin{bmatrix} X_c \\ Y_c \end{bmatrix} + PC \tag{4.3}$$

If the coordination of center of rotation is assumed to be zero, the formula is summarized as below;

$$\begin{bmatrix} X_{offset} \\ Y_{offset} \end{bmatrix} = \begin{bmatrix} X_1{}' \\ Y_1{}' \end{bmatrix} - \begin{bmatrix} K\cos\alpha & -K\sin\alpha \\ K\sin\alpha & K\cos\alpha \end{bmatrix} \begin{bmatrix} X_1 \\ Y_1 \end{bmatrix} + PC \tag{4.4}$$

In equation 4.3, the PC variable stands for process correction for the additional errors caused by the process in laser direct write lithography tool which, occurs in position measuring of chips and lithography step. The reasons for this, are declared in subsection 4.4.3.

The calculated chip offset, rotation, the center of rotation coordinates, and the original layout (gds or cif format) are imported and compiled in adaptive layout script, which is written in Perl (Fig (4.7c)). After generating the adopted layout, the wafer with the embedded chips insides polymer foils goes directly to the lithography step, which is performed by using the laser writer. In all cases, the adaptive layout should be done just one time and afterward, all the lithography steps from first via opening to final metal interconnection are pursued without any further need of adopting.

4.4.3 Overlay Accuracy of Adaptive Layout Technique

Overlay control is an essential part of lithography in semiconductor fabrication. Overlay error in various lithographic levels can cause numerous electrical issues, in this manner affecting yield. An overlay is characterized as the positional precision with which new lithographic pattern prints over a current existing pattern. To measure overlay accuracy, special patterns are designed and used on two different lithographic step one after another such that a metrology instrument can quantify overlay errors at that point on the wafer [115]. In case of CFP, the metal pads on the surface of the embedded chip in the polymer foil considered as a first pattern and new lithographic pattern, such as the via opening on the chip is defined as a second pattern. In this case, a method named "box beside box", is presented where the first box is printed during the first lithographic step on the chip and a neighboring box is printed during the second lithography step using the help of adaptive layout and after embedding the chips in polymer foil. In this work, the presented method is tested for the chips with different thicknesses and warpages.

Test chip design

To optimize the accuracy of the lithography steps using the laser direct write lithographic tool, a chip with a specific overlay layout (box beside box) is designed and fabricated. This test chip is designed to extract the certainty of the adaptive layout technology for the variety of chip warpages, thicknesses, and topographies after the chip embedding in the polymer foil. The overlay chip, shown in Fig 4.8, has four alignment marks on four edges which are detected by the laser direct writer in the position measuring step. In this test chip, the smaller box stands for the metal structuring on the chip and the bigger box stands for the second lithography steps. The distance between them in the x-axis and the y-axis are 20 µm. After embedding the chips on the polymer foil, this distance is measured and the deviation calculated all over the chip and the overlay accuracy for the CFP using the adaptive layout with the help of the laser writer is extracted. To investigate the effect of the warpage versus the accuracy

of the adaptive layout technique in the lithography step, the chips are fabricated and thinned down to 20 µm and 40 µm, respectively.

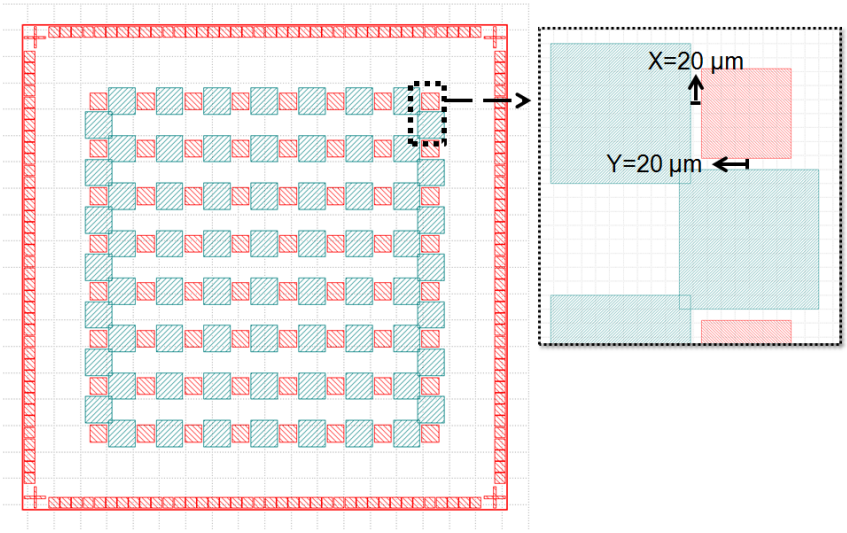


Figure 4.8: Test chip layout to measure the overlay accuracy of the adaptive layout technique using the laser writer [114].

Chip warpage

Ultra-thin chips can show a huge amount of deformation caused by induced residual stress which depends on the number of metallization layers, the layout of the chip, and the desired thickness (Fig 4.9). This deformation is also known as a chip warpage. Any kind of topography can be considered as an important factor to affect the accuracy of the laser direct writer lithography tool [116]. In this case, the surface topography

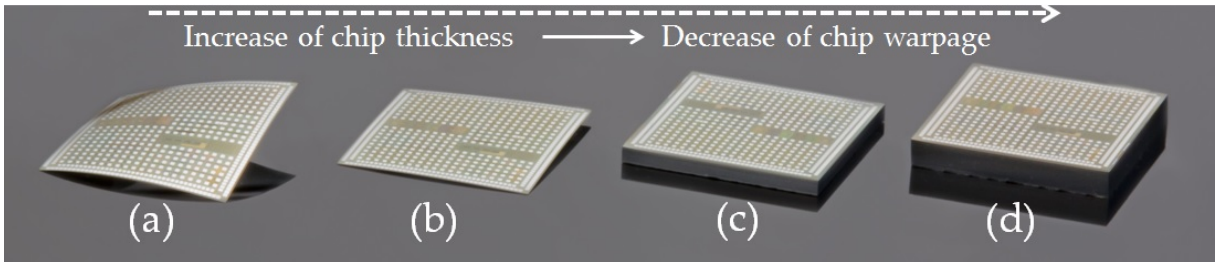


Figure 4.9: ChipFilm™ dies with thickness (a) of 10 µm and (b) 20 µm in comparison to (c) a back-grinded ∼ 400 µm thick chip and (d) a non-thinned die (675 µm) [9].

of each chip was measured after thinning and embedding. The first measurements

revealed that, after embedding the chip, depending on the chip thickness, the warpage induced by the chip internal stress (Fig 4.10) is partially compensated. This warpage reduction is directly correlated to the accuracy of the exposure in the laser writer tool. The warpage comparison of the ultra-thin overlay test chip with the thickness of 20 µm, before and after embedding, is plotted in Fig 4.11. In case of the ultra-thin silicon

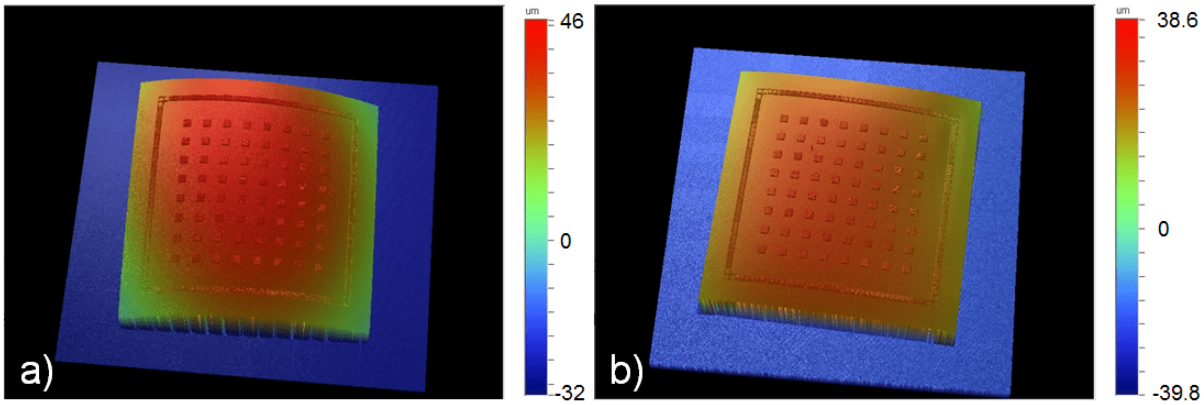


Figure 4.10: Warpage of the ultra-thin silicon chip with the thickness of 20 µm is measured by an optical profiler. a) After back grinding, b) After partial embedding [114].

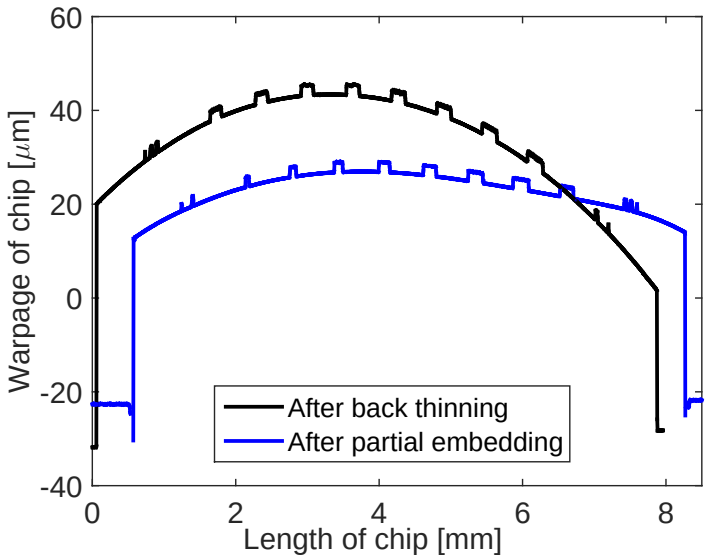


Figure 4.11: Warpage comparison of the ultra-thin silicon chip with a thickness of 20 µm after back-thinning and after partial embedding [114].

chips with a thickness of 40 µm, the initial warpage of the chip after back grinding is

less than with 20 µm chips. The percentage of the warpage reduction after embedding the chip on foil with the 20 µm chip is around double of what it is with the 40 µm chip. A further warpage reduction is achieved by symmetrically embedding chips in foil. The chips with 20 µm become almost flat after complete embedding inside the polymer foil. A comparison of two chips (same layout and metallization layers) using different thicknesses (40 µm and 20 µm) is summarized in table 4.1. In table 4.1, the word "topography" refers to the sum of thickness and warpage for each chip.

Table 4.1: Comparison between overlay test chips with a thickness of 40 µm and 20 µm.

Initial warpage	40 µm chip (22 µm) $<$ 20 µm chip (53 µm)
Warpage reduction after embedding	40 µm chip (15 µm) $<$ 20 µm chip (33 µm)
Topography after embedding	40 µm chip (47 µm) $>$ 20 µm chip (40 µm)
Overlay error	40 µm chip $>$ 20 µm chip

Wafer shape contribution

The wafer is forced to undergo mechanical deformation when it is chucked flat by the laser writer vacuum chuck. This deformation causes the wafer topography to contract or expand radially and this "in-plane distortion (IPD)" may cause a pattern shift [117]. Besides, wafer deformation by chuck, polymer deposition and a corresponding CTE mismatch between wafer and polymer is another important factor for unwanted warpage and misalignment on the wafer (Fig 4.12). In a further step, to investigate the effect of the warpage itself and to remove other factors, like the non-homogeneous thickness of polymers above the embedded chip, a test wafer is fabricated. For this purpose, 1 µm AlSiCu is sputtered and structured as alignment marks (+) all over the wafer. The initial coordinates of the alignment marks are determined and compared with measured corresponding coordinates after each BCB deposition and hard curing. As described before, BCB due to the high CTE mismatch with the silicon carrier wafer induces a warpage on a wafer after coating and curing step. With this method, the alignment coordinate measurement error versus warpage of wafer after each time BCB coating is measured. The overlay error deviation for the wafer with 14 µm BCB in comparison to a bare silicon wafer is increased by 0.06 µm and 0.129 µm in the x-axis and y-axis respectively. In case of wafers with a strong deformation, the overlay error can play an important role and sometimes there is a risk of touching the laser writer head and further damage to the wafer and head of laser writer. Therefore, it is important to control the warpage of wafer before handling it to the laser writer and if is needed, compensate the unwanted warpage.

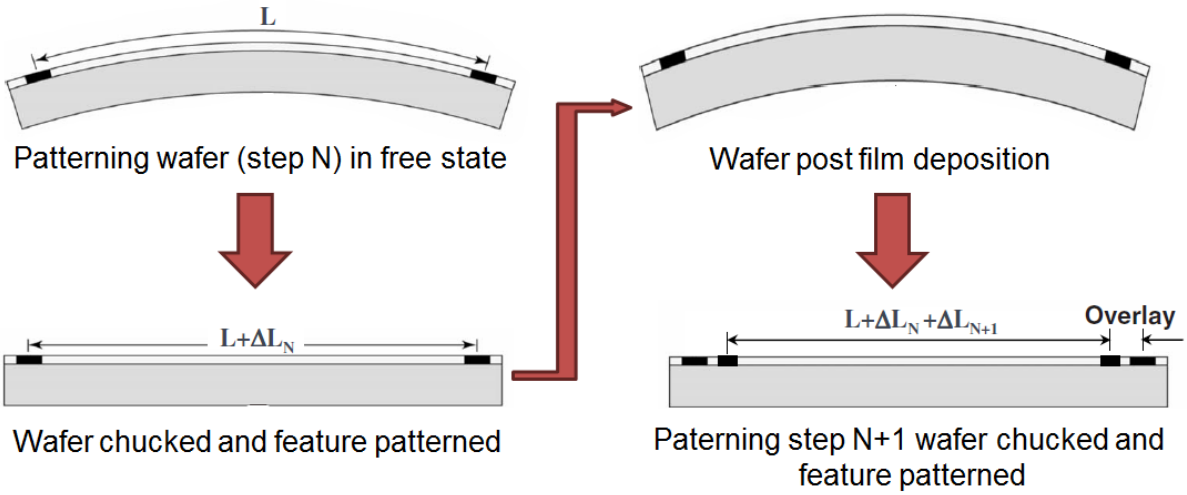


Figure 4.12: Overlay error between patterning steps N and N+1 due to a shape change from the thin-film deposition and chucking-induced distortions [117]. In this illustration, L represents the distance between two features patterned with regard to the induced warpage to the wafer. L+ Δ L stands for the real distance between two features patterned in case of the flat wafer. The difference between them is called an overlay error.

Focusing error

In the adaptive layout technique for the CFP technology, the pneumatic head (10 mm) of the laser direct writer is used for the position measurement and the lithography step. Similar to any other tool, the laser writer has a maximum tolerance for each of the chosen heads. The maximum tolerance of the 10 mm head in the laser writer to achieve best results without any damage to the tool and the processing wafer is investigated here. For this purpose, the overlay chips with two different thicknesses are embedded on top of the wafer and the accuracy measurement for each of them is performed. This way, the maximum tolerance and systemic error of the laser direct writer tool are investigated. In Fig 4.13, alignment mark detection for the chips in polymer foil with different thicknesses is shown. With the 40 µm chip, the misty window of view can cause further measurement and accuracy errors. The reason behind this is that the laser writer usually can tolerate and compensate a topography of up to 40 µm. Therefore, for the topographies above 40 µm, the laser writer goes out of focus. Based on our observations, for large features, the patterning with the additional misalignment is achievable. As a summary, the overall PC (equation 4.3) is mainly the sum of all errors caused by high topography which are the consequences of the thickness of chip and the warpage of each individual chip which leads to a focusing error in the position

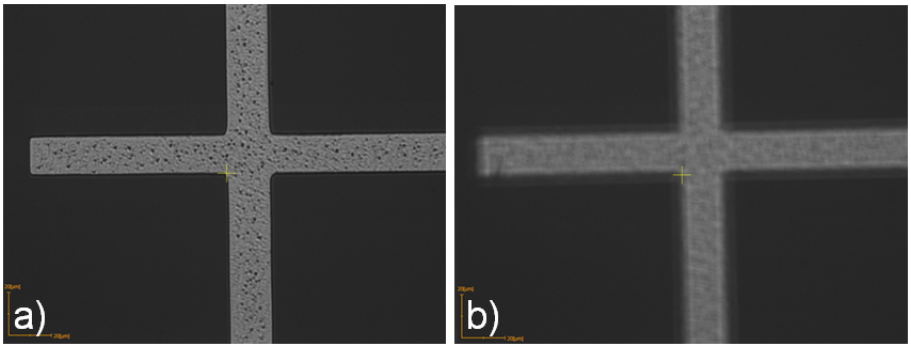


Figure 4.13: The laser writer accuracy in detecting alignment marks on the edge of the chips with different thicknesses. a) The 20 µm overlay chip embedded in foil, b) The 40 µm overlay chip embedded in foil [114].

measurement step. Besides that, the non-homogeneous thickness of the resist and the polymers on top of the embedded chip cause further errors in the lithography step.

Accuracy

With all the possible errors, the overlay accuracy of the wafer level adaptive layout embedding of 6 overlay test chips with different thicknesses and warpages in polymer foils is shown in Fig 4.14. Embedding the chips with a thickness $\simeq$ 20 µm, defined alignment marks on the silicon wafer carrier, and the dynamic focusing system in the laser direct writer will provide the best accuracy. In Fig 4.14, the accuracy error deviation in both axes is less than 5 % of the 20 µm pad size. The amount of accuracy for the chips with a topography below 40 µm is good enough to fulfill our CFP requirements. In case of the thicker chips ($\geq$ 50 µm) with higher topographies, we would need further optimization and error cancellations. As described before, the major goal of the CFP technology is to develop a fine pitch and a high number of I/O for a smaller silicon chip interconnection. Our purpose is to reduce the silicon area consumption while keeping the high performance. In this case, our required pitch and pad size on-chip goes down to 10 µm and 5 µm, respectively. To verify this purpose, a special test chip is designed which has daisy chain structures of various pad sizes from 8×8 µm^2 up to 180×180 µm^2. This test chip is utilized to perform experiments to evaluate the feasibility of the via opening and interconnecting of very small pads with the help of the wafer level adaptive layout technique. The pattern, in this case, is the common "box-in-box" (BiB) target, where an outer box is a metal pad on the chip and is printed during the first lithographic step and the inner box is designed for the via opening, done during the second lithography step, after embedding the chip in polymer foil. These chips with a thickness of 20 µm are embedded in the polymer foil and wafer level via opening with

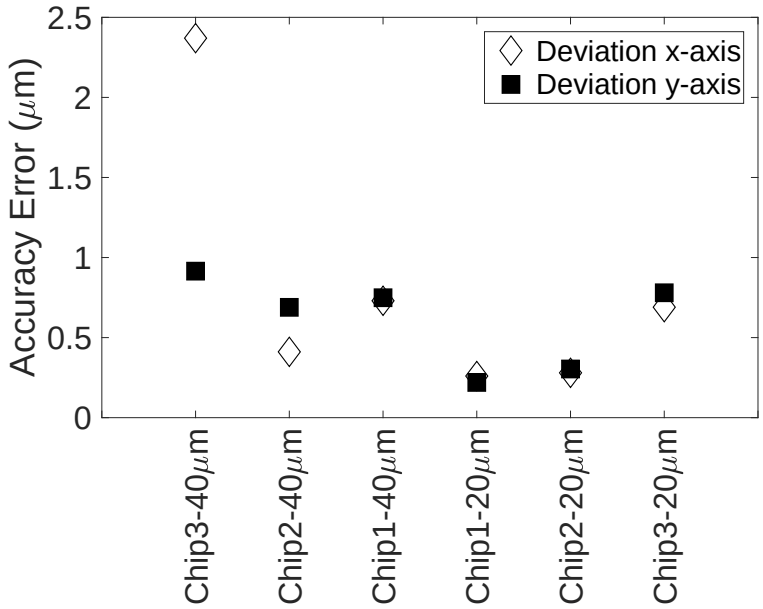


Figure 4.14: Measured accuracy error for the six overlay test chips with different thicknesses in x-axis and y-axis. In the case of chip3-40µm, the higher overlay error in x-axis can be the consequence of trapped air or particle below the chip [114], [74].

the use of the adaptive layout is successfully achieved for all of them and shown in Fig (4.15).

4.4.4 Characterization of the Adaptive Layout Technique

The adaptive layout method has no limitation for rotation and offset. However, adapting the layout might violate design rules, e. g., regarding the pitch of the metal structures. This leads to layout dependent limitations. In Fig 4.16, two chips are intentionally embedded with high rotation relative to each other and, despite that, interconnected and integrated in foil. The adaptive layout can be used for the entire wafer level embedding of chips in foil on a 150 mm silicon carrier (Fig 4.17). Besides that, the system can be extended to the complex system with a large number of I/O and multiple metallization steps, shown in Fig 4.18. In Fig 4.19, the via openings on the active pads of the chip using the laser writer are shown. In this case, the distance between pads is less than 9 µm and a pitch of 109 µm is achieved. However, the opened micro-vias are not exactly in the middle of rectangular AlSiCu structures. There are two reasons: the first micro-via opening on the contact pad was done by using a mask exposed in a contact exposure tool (EVG-6200 NT). The metal structuring, however, is done mask-

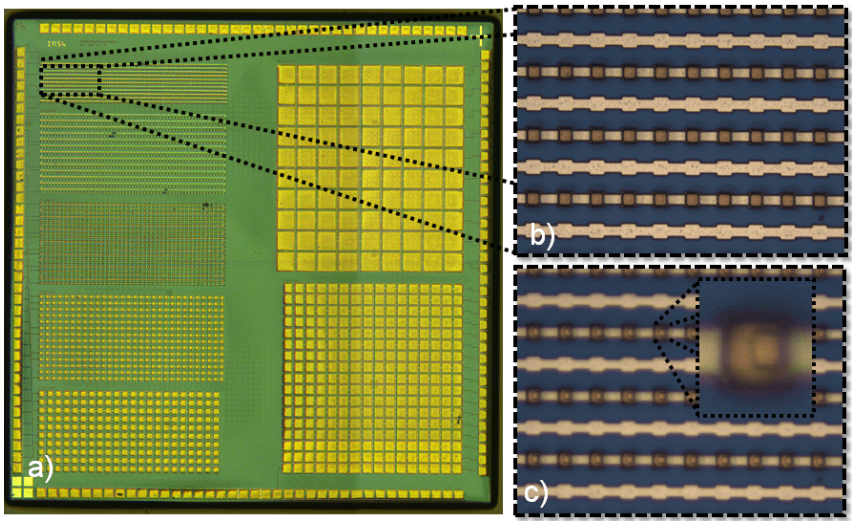


Figure 4.15: Small size pad opening on the embedded test chip in the CFP using the wafer level adaptive layout is shown, a) Microscopic image of the test chip with a thickness of 20 µm embedded in foil, b) Microscopic focus on the metal pads of the chip with a size of 8×8 µm^2, c) Via opening down to 6×6 µm^2. All the vias are opened by wafer level lithography using the adaptive layout and visited below metal pads on the chip [114].

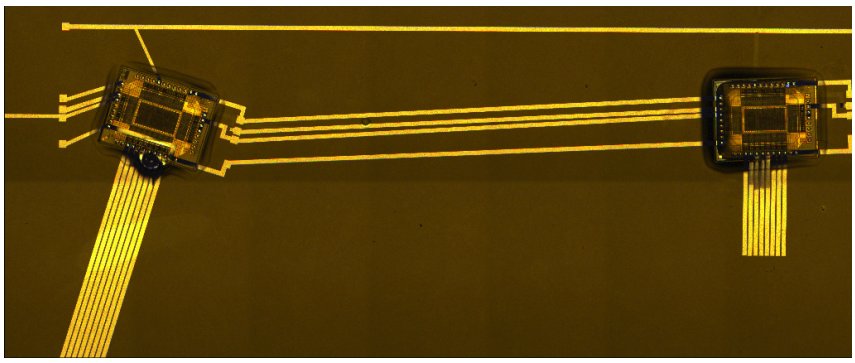
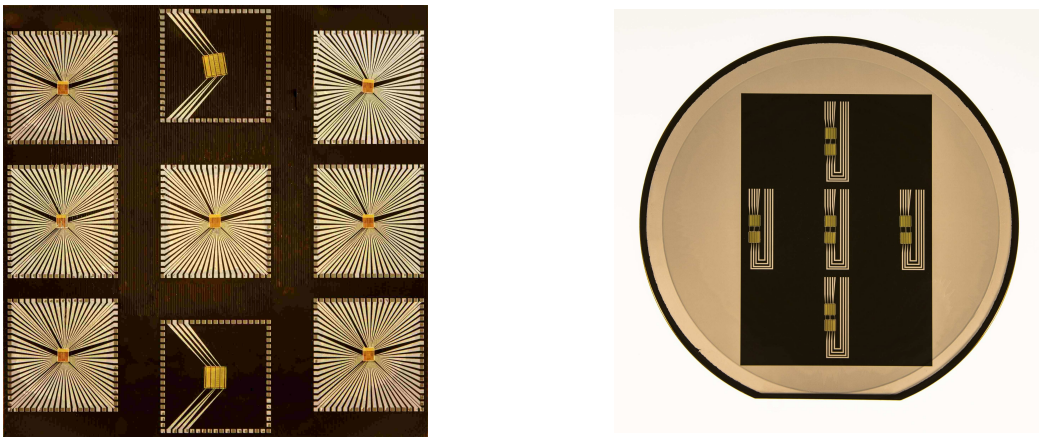


Figure 4.16: Two logic chips are integrated in the CFP based on the adaptive layout. These chips are intentionally placed with high rotation. Despite high rotation, these chips with a thickness of 20 µm and sizes of 1.47×1.82 mm^2 are interconnected to each other [114], [74].



(a) (b)

Figure 4.17: The wafer level adaptive layout technique. The lithography step is done at once at the wafer level using the adaptive layout and the laser direct writer. In this case, the adaptive layout technique is independent of the number of chips per wafer. (a) Nine ultra-thin single chips, (b) Then chips pairwise interconnected [114], [74].

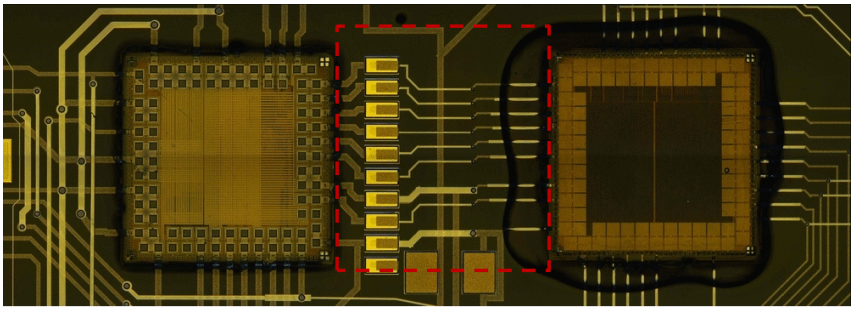


Figure 4.18: Microscopic image of two integrated and interconnected chips in the CFP with a large number of I/O and multiple metallization layers. These functional chips interconnected and integrated in the CFP as a demonstration for the public funded project KoSiF. The red rectangular area defines the interconnection between two chips, which is done by the adaptive layout technique and in two metallization steps [114], [74].

less by using the laser direct writer. These tools have different levels of accuracy. After those lithographic steps, the micro-vias are etched and refilled with metal to reach the contact pads. However, the via etching with a soft mask causes unsymmetrical slopes on the via sidewalls, shifting the center of the opened circle. As a result, the first micro-via opening is not in the center of metal structures [7]. To solve this problem, all the lithographic steps for the micro-via opening as well as for the metal structuring are done by using the laser direct write lithography tool.

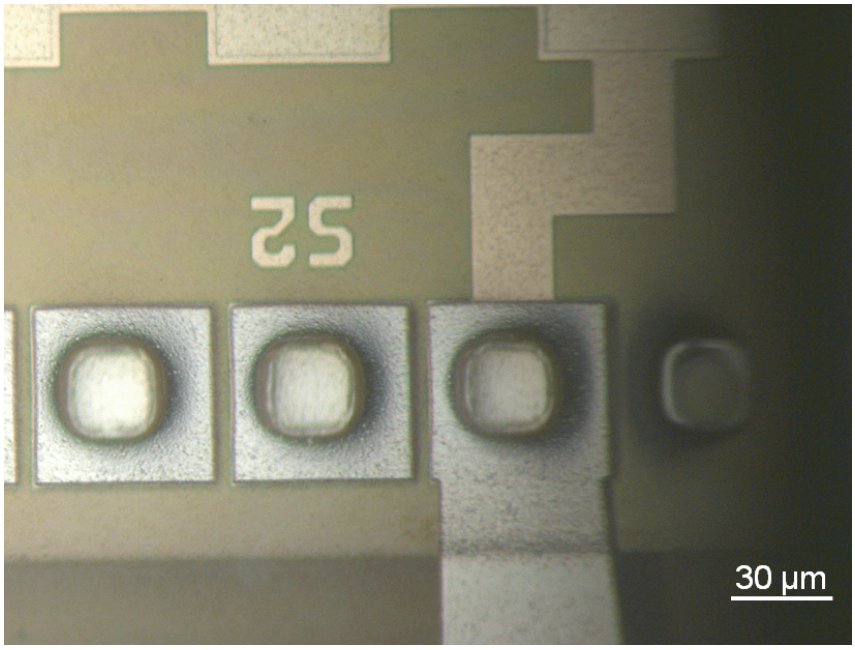


Figure 4.19: Microscopic image of the micro-via opening using the adaptive layout on the embedded chip with a pad distance around 9 µm.

Mix-and-Match

The laser direct writer lithography has the advantage of a high resolution based on requirements, but has the disadvantage of low throughput based on time in comparison with the EVG-6200 NT lithography tool. To increase the throughput in the CFP, with repetitive layouts and interconnections, we can use a strategy called Mix-and-Match lithography. With this method, the customized area which belongs to an opted layout can be processed by the adaptive layout using the laser direct writer. The outer fix layout which usually belongs to the bigger area of the wafer, can be exposed by the EVG-6200 NT or other optical lithography tools. Using the Mix-and-Match technique, there is a common problem, the so-called overlay error between patterns exposed with

the first and second lithography tools. This feature is still in the "proof of concept" phase and further experiments should be performed.

Interconnect yield

To verify the functionality of the chips embedded and interconnected in the polymer foils, the electrical measurements are performed and electrical interconnection is proved. The details of the measurement system are described in section 5.1. A yield of interconnection represents the electrical interconnection from the active pads on the chip to the extended pads on the foil in the CFP technology. For a single chip embedded in foil, with the yield below 100 %, if the disconnect is in non-active pads on the chip, the chip still stays functional. However, this issue plays an important role especially for systems including more than one chip interconnection. The probability of an interconnection ($P_{interconnect}$) between two chips (P_{chip_1} and P_{chip_2}) is defined as

$$P_{interconnect} = P_{chip_1} \times P_{chip_2} \tag{4.5}$$

The above formula can be extended to N number of chips interconnection:

$$P_{interconnect} = P_{chip_1} \times P_{chip_2} \times ... \times P_{chip_{N-1}} \times P_{chip_N} \tag{4.6}$$

Where,

$0 \leq P_{chip_1}, P_{chip_2}, ..., P_{chip_{N-1}}, P_{chip_N} \leq 1$ In equation 5.4, for a yield below 100 % for each single chip, the overall probability of interconnecting between multiple chips reduces considerably. As a result, increasing the interconnection yield for each single chip plays a key factor for the overall yield of micro-hybrid system in the CFP technology. This factor is taken into account and optimized in the micro-hybrid CFP technology and especially in chip embedding and micro-via pad opening on chip. The adaptive layout technique in the CFP technology is summarized in the below table (4.2).

4.5 The Fabricated Devices in System-in-Foil

The integration and interconnection of multiple chips in the CFP with other components, such as various sensor elements, displays, antennas, and OTFTs has excellent potential towards future demands. For this purpose, we have evaluated the visibility of fabricating and combining other devices, including organic thin-film transistors (OTFTs) and strain gauges with ultra-thin chips in the CFP. This idea obviously was not realized without the help of the adaptive layout technique.

Table 4.2: Characterization of the adaptive layout technique in the CFP technology. In this table, "No limitation" refers to the condition that the basic design rules of the original layout are met.

Maximum chip thickness	50 µm
Chip size	≥ 1 mm^2
Minimum pitch on chip	10 µm
Minimum metal pad on chip	5 µm
Wafer level embedding	Yes
Overlay accuracy in x-axis and y-axis	1 µm
Rotation and offset	No limitation
Number of chips per wafer	No limitation
Minimum distance between chips	No limitation
Number of metallizations	2
Face-down and face-up CFP	Both is possible
Electrical interconnection	**Verified**

4.5.1 Organic Thin-Film Transistor Fabrication

The OTFT is an essential building block for a wide range of low-cost and large-area electronic applications. RFID tags, biosensors and flexible displays are examples in which OTFTs play an essential role [118]. Integrating OTFTs with other technologies, such as high-performance silicon technologies are called hybrid systems-in-foil. The advantage of these systems is that the "large-area" and "low-cost" organics and printed electronics are combined with the well-developed silicon technology on a flexible polymer foil [53]. The first step in this case is to evaluate the characteristics of fabricated OTFTs on the surface of the CFP polymer foils. During the OTFT fabrication, two parameters play key roles of process flow;

- The surface smoothness is an important factor when fabricating OTFTs with good performance. The planarization and roughness of the BCB's surface can guarantee an OTFT fabrication with higher performances [119].

- During the OTFT fabrication process the nearly planar handling carrier plays an important role. As a result, a critical process step during silicon chip embedding into the foil is the compensation of the warpage in the handling carrier, which is induced by the thermal mismatch of the polymer-based foils [120].

The OTFTs were fabricated and characterized at Max Planck Institute for Solid-State Research (MPI-SSR) directly on BCB-Durimide foils above the silicon wafer substrate.

The OTFT devices were then fabricated on the surface of the foil using vacuum deposition through high-resolution silicon stencil masks. This technique makes the fabrication of OTFTs with a minimum channel length of about 0.8 µm possible [121]. The OTFTs in this work are based on the inverted-staggered (bottom-gate, top-contact) device structure. The gate dielectric is a combination of an oxygen-plasma-grown AlOx layer and a solution-processed alkyl- or fluoroalkylphosphonic acid self-assembled monolayer (thickness of about 5.3 nm). This combination permits the OTFTs to work with the voltage of around 3 V and makes it feasible to set the threshold voltage to a particular value during the OTFT fabrication [122]. The substrate is a stack of durimide and benzocyclobutene (BCB) with a total thickness of about 40 to 50 µm which is fabricated for a hybrid system-in-foil purpose. The process flow of fabricating OTFTs on BCB is shown in Fig 4.20. Figure 4.21 shows the measured static output and trans-

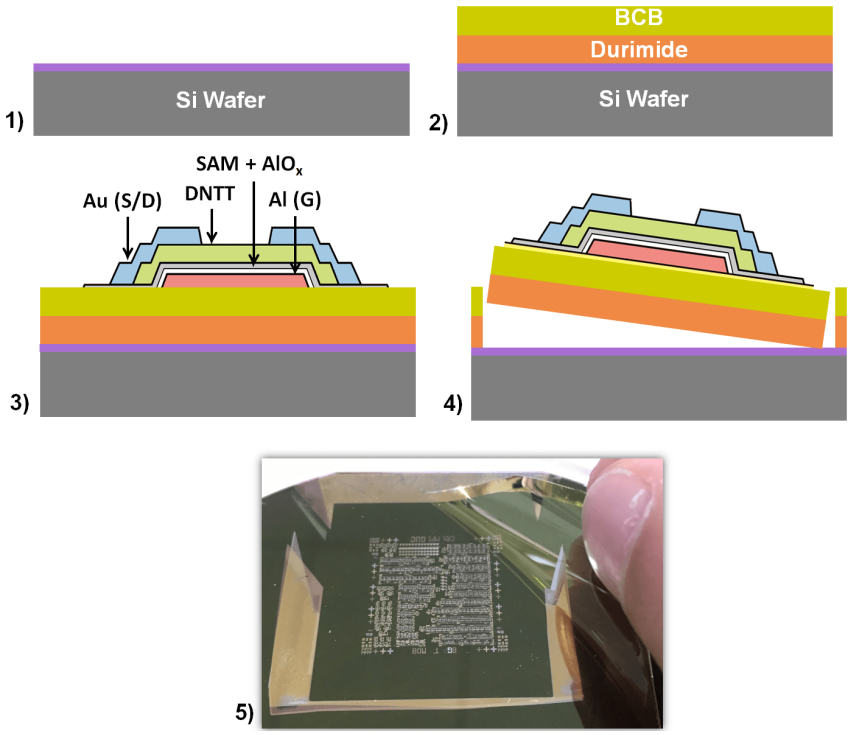


Figure 4.20: OTFT on BCB fabrication process flow: 1) Pre-surface treatment, which includes the deposition of a 1.5 µm Si_3N_4 layer to induce warpage and coat the silicon wafer with an adhesion lowering layer, 2) Spin coating of a Benzocyclobutene (BCB) and Durimide layers as a composite foil, 3) The OTFTs are then fabricated on the surface of the foil using vacuum deposition through high-resolution silicon stencil masks, 4) Cutting from the side and releasing of the polymer foil from the silicon carrier, and finally 5) Optical image of the released OTFT from CFP polymer foil [123], [124].

fer characteristics of the organic TFTs with channel lengths ranging from 100 µm to 4

µm fabricated on the flexible durimide/BCB substrate. The transmission line method (TLM) is used to extract the threshold voltage V_{th}, the intrinsic channel mobility μ_0 and the contact and sheet resistances R_c and R_{sh} [121]; the extracted values are summarized in Table 4.3 [125].

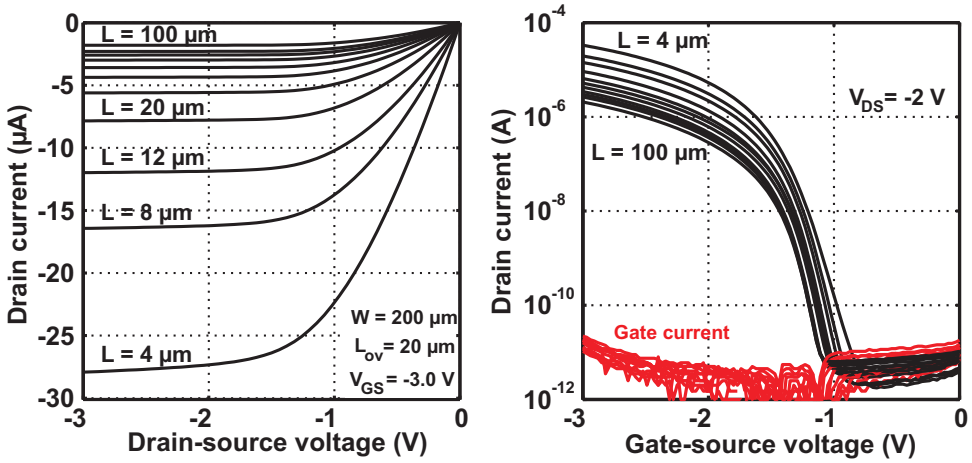


Figure 4.21: Measured static output and transfer characteristics of organic TFTs with channel lengths (L) ranging from 100 µm to 4 µm fabricated on a flexible PI/BCB substrate. All TFTs have a channel width (W) of 200 µm and gate-contact-overlaps (L_{ov}) of 20 µm. [125].

Table 4.3: Extracted transistor parameters [125].

Parameter	Value
Threshold voltage V_{th}	-1 V
Mobility μ_0	1.3 cm^2/Vs
Contact resistance R_c	0.2 kΩ.cm
Sheet resistance R_{sh}	666 kΩ/□
On/off current ratio	10^6

The OTFT devices are fabricated on glass and polyethylene-naphthalate (PEN) as well. The carrier mobility is observed to be 2.1 cm^2/Vs, 1.0 cm^2/Vs and 1.3 cm^2/Vs on glass, PEN and BCB substrates, separately. The OTFTs on BCB as a top layer on the polymer stack have an about 30 % higher carrier mobility compared to the PEN substrate. These measurement results prove the better performance of OTFTs fabricated on substrates with BCB as a top layer and show that BCB with a planarized surface is a good substrate that enables the realization of flexible OTFT devices and circuits [124].

4.5.2 Ring oscillator fabrication

The dynamic performance of the OTFTs are normally characterized by measuring the propagation delays of ring oscillators or by extracting the current gain cutoff frequency from admittance or S-parameter measurements on standalone OTFTs [121]. In this case, 11-stage uni-polar ring oscillator based on p-channel DNTT TFTs on the CFP flexible substrate with BCB and PI2611 as a top layer is investigated. The ring oscillators are fabricated using high-resolution silicon stencil masks. In case of polymer foil with BCB as a top layer, the signal propagation delay for supply voltage down to 0.7 V is measured. The shortest signal delay for the channel length= 4 µm and voltage= 3 V is 11.4 µs. Considering the fact that the substrate was not heated during the deposition of the organic semiconductor, this signal delay is a convincing result. Normally, during the semiconductor deposition the substrate is heated which gives better semiconductor morphology and, thus, slightly larger field-effect mobility. However, at Max Planck Institute, heating the substrate is limited just to 100 mm wafers. Figure 4.22 [1] shows the measured static output and transfer characteristics of the ring oscillator with the channel length of 15 µm fabricated on the flexible durimide/BCB substrate. Signal

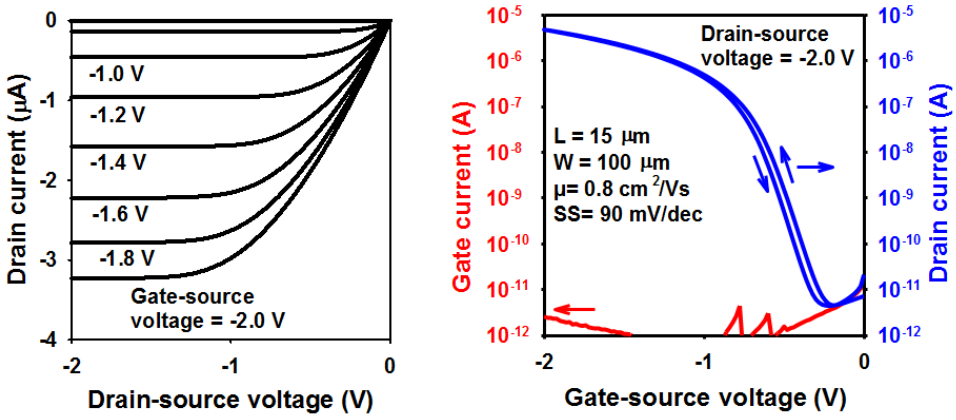


Figure 4.22: Measured static output and transfer characteristics of the ring oscillator with the channel length of 15 µm fabricated on the flexible PI/BCB substrate.

propagation delay per stage as a function of the supply voltage of 11-stage uni-polar organic ring oscillators fabricated using DNTT thin-film transistors on various types of the flexible substrates are compared in Fig 4.23. For this work the use of PI2611 as a top layer of the flexible foil was repeated. Unfortunately, on this wafer, each of the

[1]The ring oscillator fabrication and characterization on polymer foil is done at Max-Planck-Institut for Festkörper-forschung, Stuttgart, Germany.

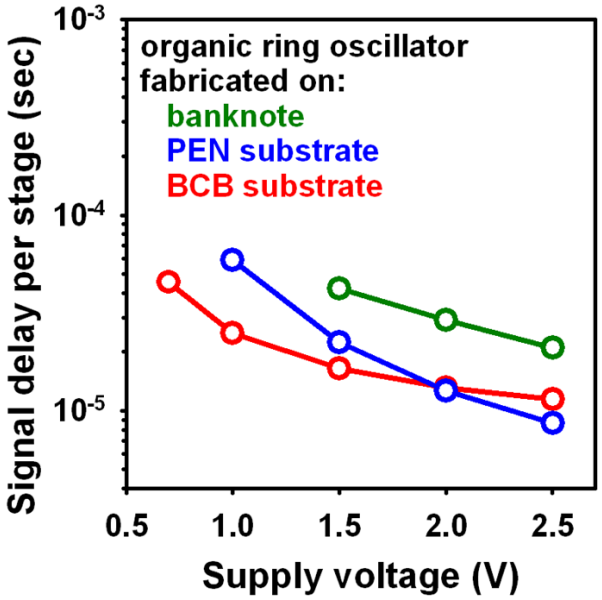


Figure 4.23: Measured signal propagation delay per stage as a function of the supply voltage of 11-stage complementary ring oscillators fabricated using DNTT thin-film transistors on various types of flexible substrate [126], [127].

five stencil masks that were used to pattern the TFTs moved unintentionally by a few microns during the deposition process, so that the alignment between the individual layers turned out badly. As a result, we did not obtain a functional ring oscillator on this substrate. One of the possible solutions can be the surface plasma treatment of polymer before the TFTs fabrication. This will have to be considered in the future.

4.5.3 Final demonstration of the KoSiF project

As a final demonstration for this KoSiF project (This project is described in chapter 6), the complex system-in-foil is fabricated which includes multiple embedded and interconnected ultra-thin silicon chips using the wafer level adaptive layout with multiple metallizations, OTFTs fabrication on the top surface of the foil in a pre-defined area and thin film strain gauges, which are in contact with the OTFTs. [2] This complex micro-hybrid system-in-foil is shown in Fig 4.24. The strain gauges as stress sensor on the foil with BCB as a top polymer layer are fabricated by the Aerosol Jet™ printing

[2]This work has been demonstrated as a part of KoSiF project and in collaboration with Dr. Mahadi UI-Hassan. The OTFT fabrication on polymer foil was done by Max-Planck-Institut for Festkörperforschung, Stuttgart, Germany. The thin film strain gauges are processed at Hahn-Schickard, Stuttgart, Germany.

technique, formerly also known as M3D (Maskless Mesoscale Material Deposition). The process flow of the strain gauges fabrication in the CFP technology and related characterizations have already been published [119].

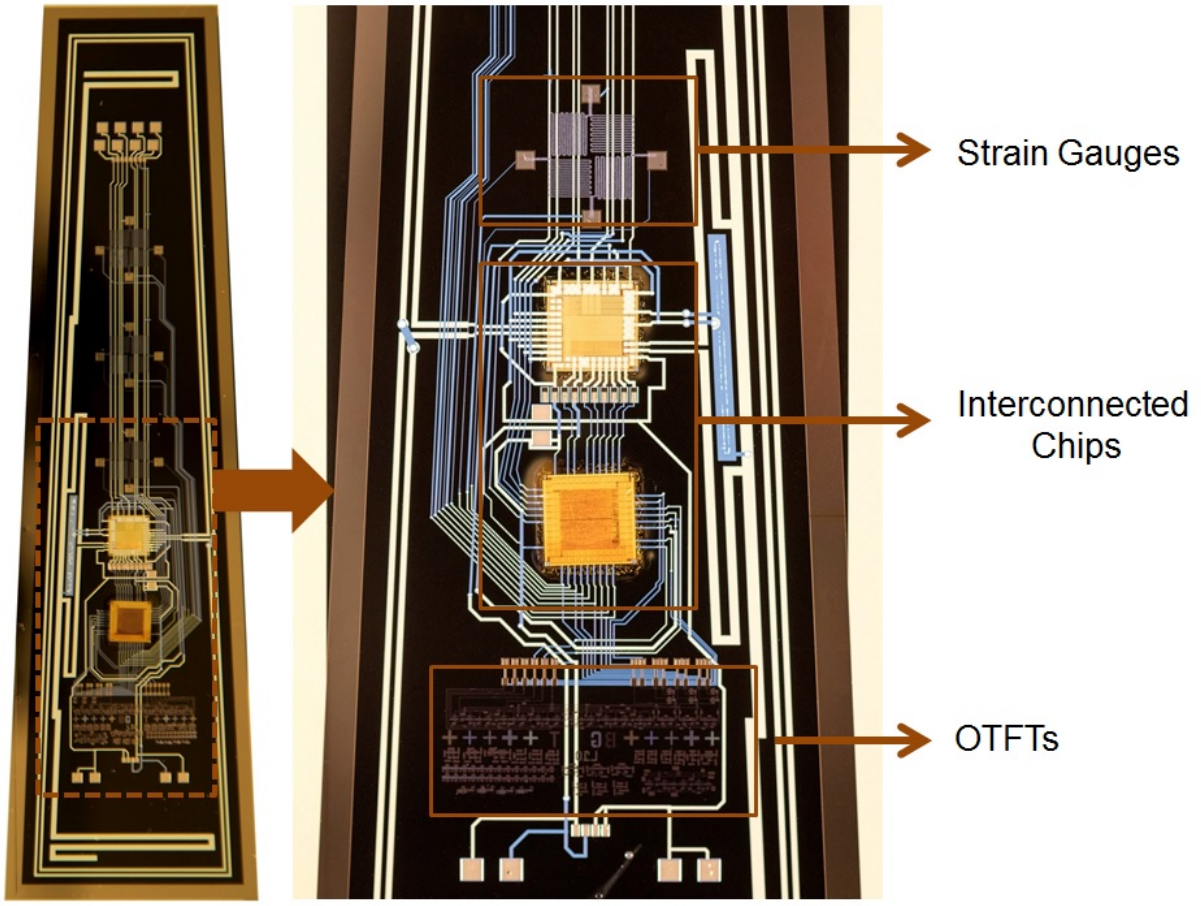


Figure 4.24: Micro-hybrid multiple chips interconnect in the CFP and integration with OTFT and the strain gauge are achieved using the adaptive layout technique [114].

4.6 Summary

In this chapter, the concept of Industry 4.0 and the need to integrate multiple chips with other sensors in the polymer foil was discussed. In this case, the adaptive layout to interconnect chips despite unwanted misalignment is proposed as a solution. Therefore, the wafer level micro-hybrid chip interconnects in the CFP as well as integration with other devices using the adaptive layout technique is pursued. The overlay accuracy

of the method and systematic errors of the laser direct writer tool are investigated and analyzed. The thickness of chips, warpage of chips, and the overall topography play important roles in the overall accuracy of the system. However, the overlay accuracy of the adaptive layout for a wafer level embedding of chips with different thicknesses has successfully been achieved below 1 µm in the x-axis and y-axis for any arbitrary position on the embedded chip. This accuracy fulfills the requirements of the CFP technology to integrate ultra-thin silicon chips with a fine pitch and a high number of I/O in combination with other technologies.

CHAPTER 5

SYSTEM-IN-FOIL CHARACTERIZATION

> "Information is not knowledge. The only source of knowledge is experience. You need experience to gain wisdom."
>
> — Albert Einstein

This chapter gives an overview of the different feasibility test results on the CFP technology. Electrical interconnection tests are performed on CFP integrated interconnection test chips. The single test chips and multiple interconnect chips as daisy chain structures or the functional chips are characterized. The first section describes the interconnection test sample fabrication, including the measurement set up, reliability investigations, the fabricated passive element on foil, and the embedded active elements in the CFP. The next section focuses mainly on the mechanical stress analysis of the CFP technology, measuring and calculating the stress introduced during the processing based on various presented technologies. The third section presents the thermal behavior of the ultra-thin chips on and inside polymer foil. The last section emphasizes the high-frequency aspect of the CFP technology, including the characterization of thin film dielectric material and the on-chip mm-wave resonator fabrication and measurement results.

5.1 Electrical Characterization

This section features the electrical characterization of embedded chips, both daisy chain and functional chips, in the polymer foil. It starts with illustrating the measurement setup which is used to measure chips on the wafer and in a bending position. Then, the electrical characterization of fabricated passive elements, such as capacitors,

inductors and active elements inside CFP polymer foil will be discussed.

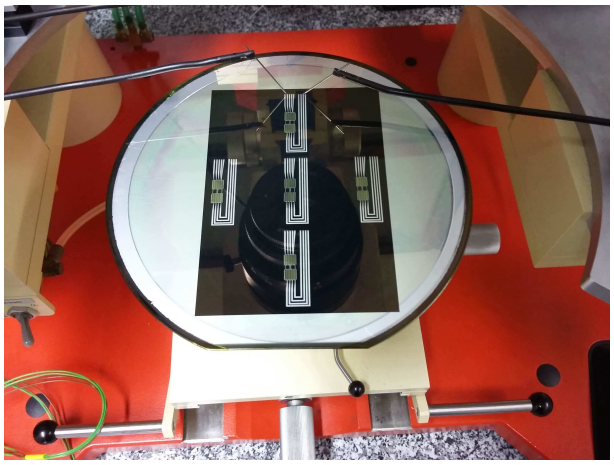
5.1.1 Measurement Setup

The measurement setup should be arranged in a way to do measurement (i) on a wafer level (ii) after releasing and (iii) during bending stress. The wafer level measurements are performed using manual needle type adjustable probes (Fig 5.1a). After releasing the embedded ultra-thin chip in foil from the carrier, the measurements are pursued either with pogo-pin connectors or manual needle probes (Fig 5.1b). The uniaxial bending strategy is a precise technique to assess the impact of mechanical stress on the devices under bending stress. The conventional techniques to apply uniaxial stress are namely "3-point measurement and 4-point measurement". The maximum stress happens under the loading anvil in three-point bending tests. However, in 4-point measurement, the maximum flexural stress is spread between loading points. The stress concentration of a 3-point measurement is small and concentrated in the center of the loading point, whereas the stress concentration of a 4-point measurement spreads across a bigger region, avoiding premature failure [128]. Other popular bending methods are the bending jig method, and the cantilever method, which are proven to be useful for the chips with a thickness > 35 µm. These techniques are hard to apply as sample sizes get thinner and smaller. So, for ultra-thin chips (thickness < 20 µm) these methods cannot be used anymore [1].

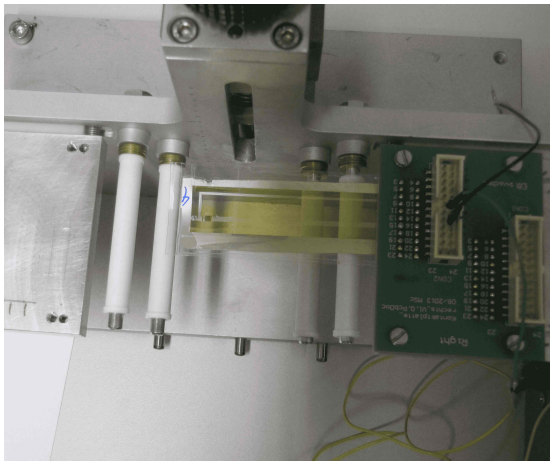
The assessment of embedded ultra-thin silicon chips in the CFP technology under bending stress is accomplished by wrapping them around cylinders with various radii. For this purpose, two sides of the cylinder are flattened so that the CFP foil can reside with its pads on the flat side for ease of interconnection, while the chip can bend over the curved side of the cylinder (Fig 5.1c) [57]. For this purpose, both the single chip in foil and multiple interconnected chips in foil should have all the measurement pads in one direction on the foil and far from the chip (Fig 5.1d). In all the measurements, the ambient temperature is recorded using a platinum temperature sensor Pt-100 placed very close to the chip. A measurement of various devices on chips is performed using the Agilent 5270B Semiconductor Parameter Analyzer (SPA) tool. The entire measurement is controlled and monitored by IC-CAP (Integrated Circuit Characterization and Analysis Program).

4-point Kelvin measurement

One of the simple ways of proving electrical interconnection in CFP technology is to measure embedded chips, including daisy-chain structures, on them. The test chips with different daisy chains, such as corner daisy chains and center daisy chain struc-



(a)



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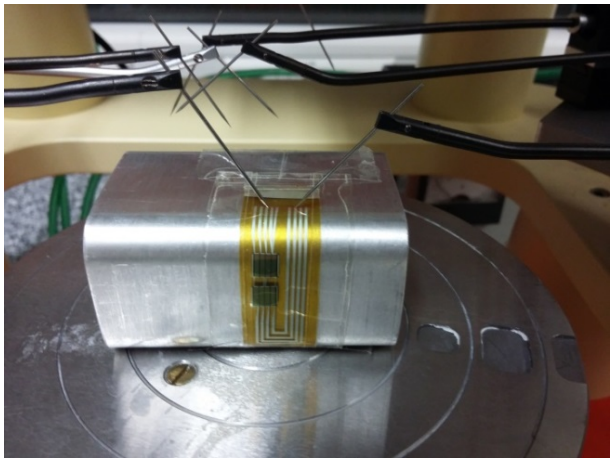

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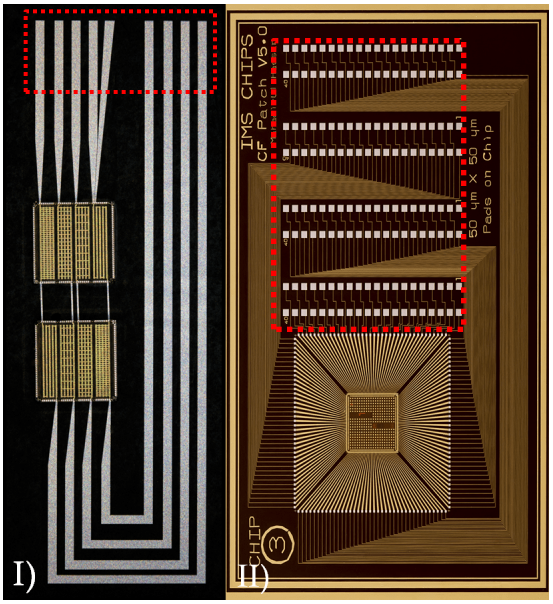


(d)

Figure 5.1: Measurement techniques after embedding and interconnecting test chips in the polymer foil. (a) Measurement with needle-type probes in wafer level condition. (b) The pogo-pin electrical measurement of released CFP foil from temporary carrier. (c) Measurement with needle-type probes after releasing foil and in the bent condition. (d) The fan-out interconnections for ease of subsequent device characterization in bent state are marked with red box. I) the multiple chips, II) the single chip [57], [114].

tures were designed, fabricated, and thinned down to evaluate and verify the existence of contact from metal pads on chip towards bigger metal pads on foil or to the active pads of the neighboring chip. In this case, the daisy chain structures were measured utilizing the 4-point Kelvin measurement technique. The 4-point or known as Kelvin measurement is a resistivity measuring strategy that uses separate pairs of current flow and voltage-sensing electrodes to make more accurate measurements in comparison to the two-terminal (2T) sensing. The advantage of Kelvin measurement is that this method eliminates the lead and contact resistance from the measurement [129].

5.1.2 Reliability Test

The reliability of CFP technology still has to be proven - as, in conventional electronic packaging, the reliability of the fabricated or embedded system-in-foil is governed by the mismatch of thermal, mechanical, and chemical properties of the involved components, substrates, and interconnections. Reliability requirements for each system are defined based on the application. For example, certain tests, such as temperature cycling and temperature/humidity storage are common for consumer and automotive devices [130]. The reliability test is categorized in a bending test, a thermal ageing test, a thermal cycling test (TCT), and thermal and humidity storage (THST). In the two-polymer CFP technology, the bending test and TCT are performed for a single chip inside the polymer foil during the first phase and are already published. In this work mainly the reliability tests, such as the bending test, the thermal ageing test, and THST are performed and verified for multiple test chips embedded and interconnected in the two-polymer CFP technology. The reliability tests are performed on three samples each of them including two embedded and interconnected daisy chain chips in the two-polymer CFP (Fig 5.2). The further reliability tests for low-stress CFP technology and face-down CFP technology are in progress and will be published in the future.

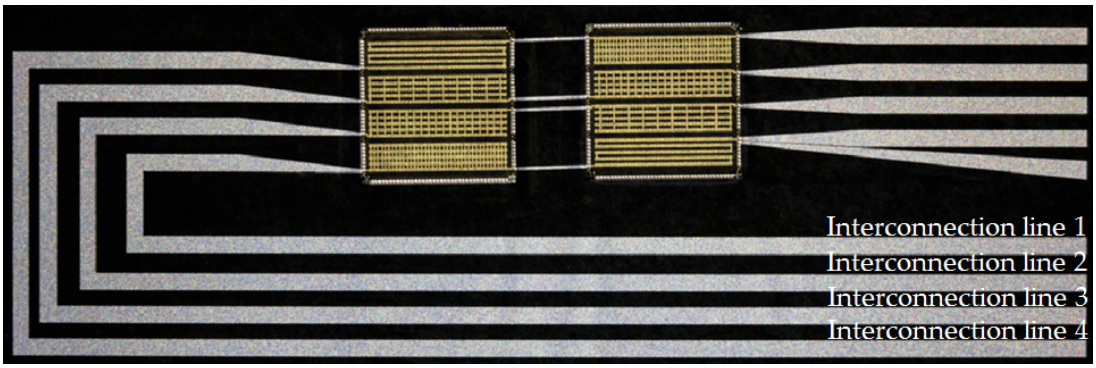


Figure 5.2: Camera image of the integrated and interconnected daisy chain test chips in the CFP during the reliability test.

Bending test

During the bending test, the reliability of metal interconnections between two ultra-thin chips based on bending the released foils to different bending radii is investigated. The resistance value of the daisy chains in several locations of the multiple interconnected chips (2-point measurement) are measured and plotted with respect to the corresponding bending curvature as shown in Fig 5.3. As is obvious from the data, the measurement results exhibit consistent trends versus different bending conditions and no significant change is visible. The small deviation arises from the failure of a manual adjusting and measurement. In this test, the fourth interconnection line was damaged with needle probes during measurements and further measurement was not possible. The measurement implies that metal interconnections remain unharmed under different bending conditions. The bending curvature can extend to the higher value for a single embedded and measured chip compared to the multiple interconnected chips. However, it depends directly on the relative distance of the interconnected chips. As an example, if two chips are placed and interconnected close to each other, the rigid area between them is duplicated, and, therefore, the flexibility of the complete system in the position of the embedded chips may reduce.

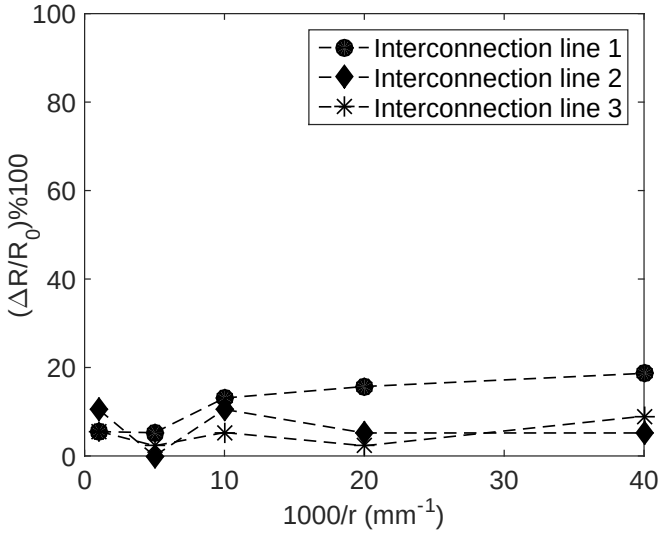


Figure 5.3: Measured resistance of the pair of interconnected daisy chain chips as a function of bending curvature. In this plot, the percentage of resistivity change as a function of the radius of the curvature (r) for three different integration lines is presented. R_0 stands for the resistance of each interconnection line before bending. In this plot, $\triangle R = R_{\text{after bending}} - R_0$ [114].

Thermal ageing test

The other pair of interconnected daisy chain chips in polymer foil with four lines of interconnection is taken for the thermal ageing evaluation of the CFP technology. It also determines the ability of the components in the package to withstand mechanical stresses induced by longtime thermal cycling test. In this case, the temperature alteration starts and ends at room temperature and changes between 120 °C and 22 °C temperature. The CFP sample with two interconnected daisy chain chips is gone through the thermal ageing test where the sample is taken out of the chamber after a certain number of cycles and is electrically characterized. The measurement results are shown in Fig 5.4. The major purpose of this measurement is to check if the interconnection between two chips will survive the thermal ageing. In Fig 5.4, all the interconnection lines survived up to 1000 hours. The trend in this graph shows the resistivity of lines reduce up to 240 h and after 240 h till 1000 h becomes more stable. The approximately similar trend is seen for the longtime ageing experiment from other research groups [100], [44]. Decreasing in the resistance can be interpreted mainly by two reasons; (1) the stress on 1 µm sputtered AlSiCu as an interconnection line inside polymer foil. This stress is caused by the coefficient of thermal expansion (CTE) mismatch between AlSiCu and the polymers which are used in the embedding process. Depending on the compressive or tensile stress, the resistivity of metal interconnection line may decrease or increase, respectively. (2) the annealing process during thermal cycling may cause the better contact in the place of vias on the contact pads of the embedded chips inside foil. Our speculation is that, after 240 hours, the ageing is started and therefore the interconnection's resistance increase gradually up to 600 hours. The native oxide growth on the surface of AlSiCu in contact with air moisture can be another involved parameter. In this case, replacing AlSiCu metallization with noble metals like gold (Au) may optimize the performance of the CFP system. Slight deflections observed in the measurement results are attributed to the contact resistance between the probe needle and aluminum pads due to the formation of a thin native oxide layer plus the resistance of the measurement set up.

Thermal and humidity storage test (THST)

The third pair of interconnected ultra-thin daisy chain chips in CFP was taken for the thermal and humidity storage test. A controlled climate chamber (Vötsch VCL 0010) was used to vary the RH from 40 % to 70 % with temperature alteration between 22°C at 40 % RH and 70 °C at 70 % RH. The CFP sample was taken out of the chamber after a certain number of hours and electrically measured and verified. The measurement results are shown in Fig 5.5.

The measurements indicate that the interconnections are stable under THTS. The small

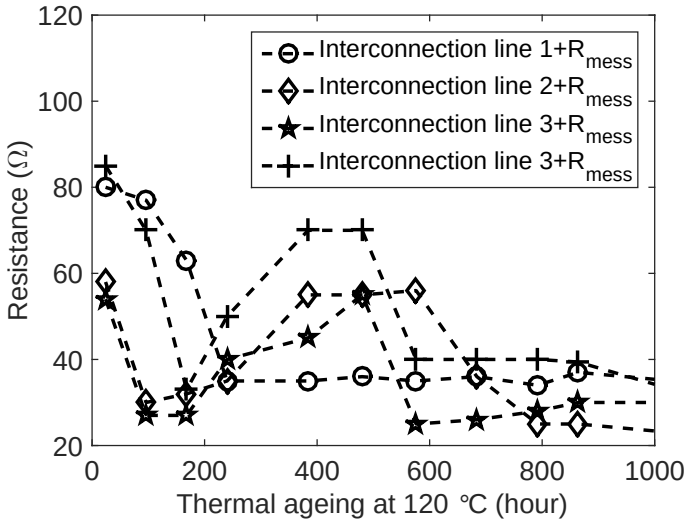


Figure 5.4: The two measured integrated chips include daisy chain structures. In this plot, the resistance as a function of long time temperature exposure for four different interconnection lines is presented. R_{mess} stands for resistance of the measurement set up [114].

degradations are caused due to the formation of native oxide on top of metal pads plus manual measurements.

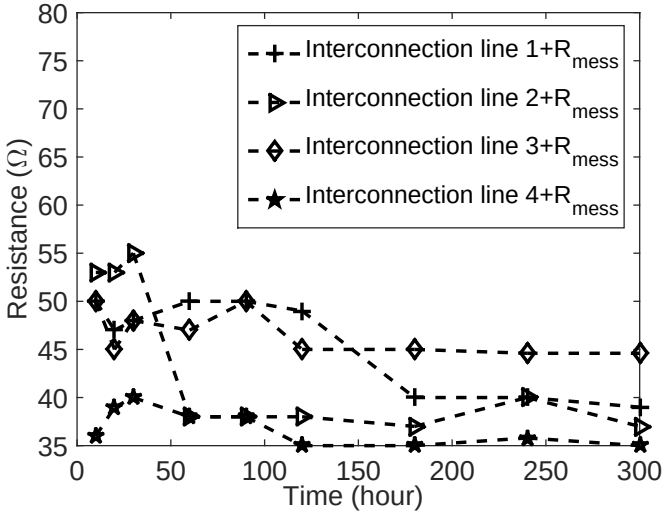


Figure 5.5: Daisy chain resistance under thermal humidity test. In this plot, R_{mess} stands for resistance of the measurement set up.

Failure analysis

In flexible electronics, the mechanical failure in a system is determined by the weakest component. In systems that use inorganic thin-films or ultra-thin silicon chips, these brittle layers are the main source of mechanical failure during bending [131], [132]. When a system-in-foil is bent, the outer surface is under tensile stress and the inner surface experiences compressive stress, while a plane in the middle of the symmetrical sheet experiences no uniaxial stress. Hence, the undesirable cracks can be generated and propagated because of several bending, especially in the place of metal transition from the edge of the chip to the foil. In case of the thermal ageing test, one of the observed failures is generating and expanding of cracks on foil and close to the edge of the embedded chip. This can happen due to the high CTE mismatch between the embedded silicon chip and embedding polymers. In addition, humidity is an important challenge in the systems where polymers are used as e.g. "encapsulants, substrates or adhesives". Polymer can absorb the air moisture which can cause swelling or changes in thermomechanical properties as reducing the glass transition temperature and stiffness or increasing the coefficient of thermal expansion [133]. One of the other failures in this case is metal line delamination due to moisture absorption in the below polymer. In Fig 5.6, the interconnection lines are not sealed and are exposed to air. The test wafers with the different thickness of BCB as a layer below the metal are fabricated. In the case of wafers, in which the thickness of the below BCB (low moisture absorption polymer) is low or close to zero and metal lines are in direct contact with durimide or polyimide (high moisture polymer), after a while (approximately one week), the AlSiCu lines are delaminated from the surface of the polymer. However, the plasma surface treatment, adhesion promoter coating, and covering the surface of metals with low moisture uptake polymers will reduce this phenomenon and increase the overall lifetime of the system-in-foil.

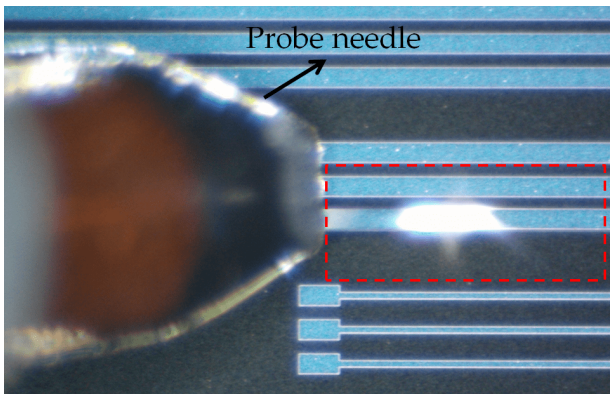


Figure 5.6: The AlSiCu line delamination due to moisture absorption by below polymer. The delaminated line is marked with the red rectangular.

5.1.3 Passive Elements in the CFP

This part describes a low-cost microfabrication of passive devices on the flexible substrate for sensing applications. The planar or discrete capacitors, and inductors are fabricated in CFP technology. In this case, a near-field communication (NFC) antenna and humidity sensor are presented as a demonstration.

Capacitor

The planar capacitor is fabricated using two metallizations (AlSiCu) steps for the bottom ground plate and top power plate. The metal structuring is done by standard lithography. The suitable polymer is deposited as a dielectric in between two plates based on the required application.

In addition, the discrete capacitor is built on the CFP polymer foil. The metal electrodes are fabricated by AlSiCu (1 µm) metal sputtering and structuring using lithography. The top surface of the electrodes is covered with polymer. The via opening using RIE is performed to open measuring pads of the capacitor. The measurement pads are covered by the second Al metallization (2 µm). The schematic cross section of the CFP foil substrate with the planar capacitor and discrete capacitor are shown in Fig 5.7.

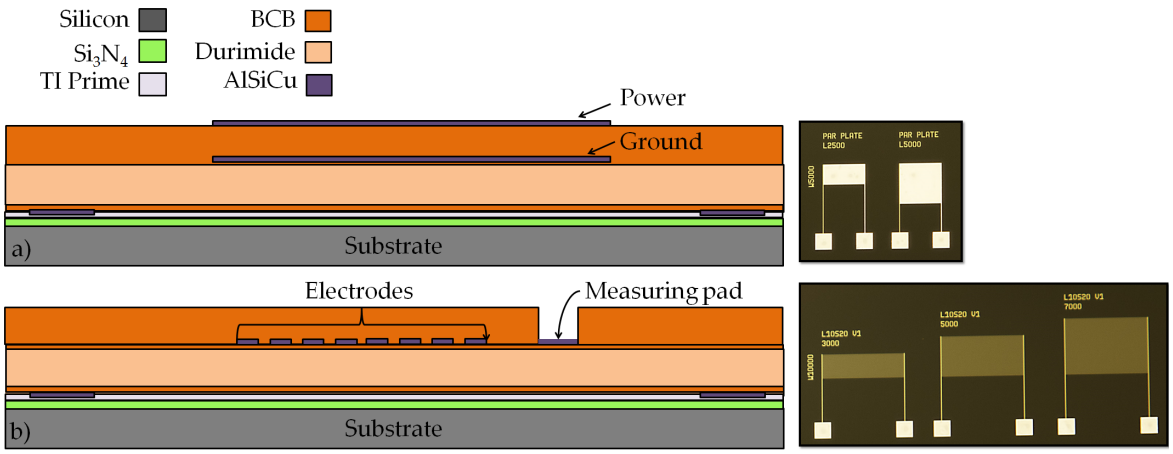


Figure 5.7: Schematic cross section (left) and camera image (right) of the capacitors in the CFP foil, a) Parallel capacitors, b) Discrete capacitors.

As a first demonstration, various parallel capacitors with different plate sizes and discrete capacitors with various number of electrodes are fabricated in CFP foil. BCB with the thickness of 5 µm is deposited as a dielectric and is cured at up to 250 °C. The measurements are performed at the wafer level using manual needle-type probes. The

probes receive the signal from the LCR meter at the frequency range of 10 kHz-5 MHz. The frequency is swept in the LCR meter range at voltage= 1V.

First, the planar capacitor (W×L= 5000×2500) is measured after its release from the substrate carrier (Fig 5.8). The measurement is done on a thick non-conductive plastic carrier to eliminate the effect of a conductive substrate underneath on the measurement. As a next step, the capacitor is bent on top of the cylinders with a different radius of curvature. As shown in Fig 5.8.b, the overall thickness of the released foil ($\sim$ 20µm) is not enough to provide the required sensitivity to detect mechanical strain resulting from bending on the inductor. Therefore, the foil is mounted on top of the thick double sided tape (4 mm) and fixed on top of the cylinder. This way, the distance between the neutral surface of the system and the capacitor on top of the foil increases.

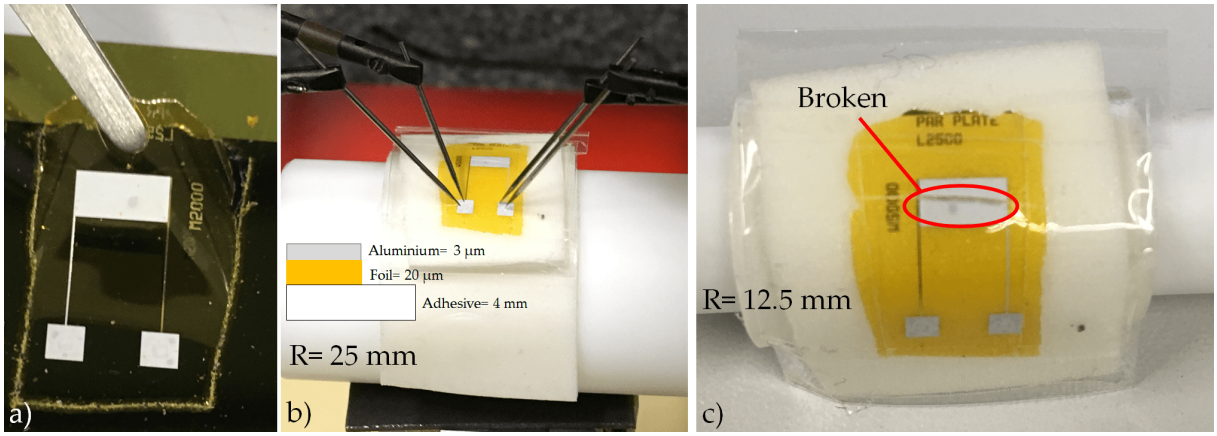


Figure 5.8: The planar capacitor measurement status, a) Releasing from substrate carrier, b) 4-point measurement of the attached capacitor on the tape and above the cylinder, c) Damaged capacitor due to bending. R stands for the radius of curvature.

The 4-point measurements of the planar capacitor at f= 100 kHz is shown in Fig 5.8. As shown in Fig 5.8, in the beginning, and for the R= 30 mm radius of curvature, the capacitance slightly increased which can be due to the polymer thickness reduction between the two plates while bending, shown in equation 5.1. C, A, and d stands for capacitor, area of plates, and distance between two plates, respectively. However, the capacitance is dropped for the higher radius of curvatures. The reason behind this is the micro-cracks generation on both plates. Therefore, the size of the plates are reduced. This damage becomes optically obvious while bending the system on the cylinder with R= 12.5 mm radius of curvature.

$$C \propto \frac{A}{d} \tag{5.1}$$

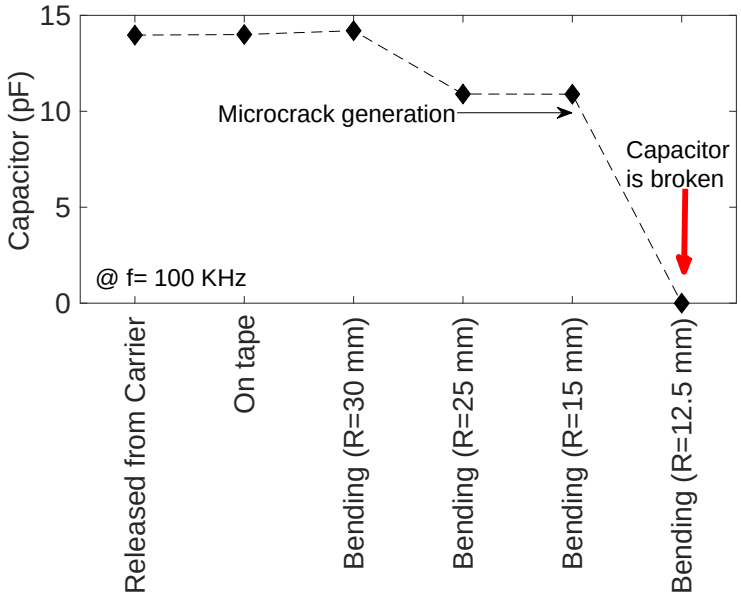


Figure 5.9: The 4-point measurements of the planar capacitor at f= 100 kHz, room temperature, and various conditions is plotted. R stands for the radius of curvature.

A **capacitive sensor** (C) converts a change in properties of dielectric (ϵ_r), area of capacitive plate (A), and distance (d) into an electrical signal [134].

$$C = f(d, A, \epsilon_r) \tag{5.2}$$

The humidity sensing, proximity sensing, and displacement sensing are the group of sensors which are based on capacitive principle. The capacitive humidity sensors are based on the changes in the permittivity of the dielectric between plates of capacitor [134]. One of the already published humidity sensors using CFP technology is shown in Fig 5.10. In Fig 5.10, durimide polymer (thickness about 2.7 µm) is applied as a dielectric. Durimide has a high moisture absorption in comparison with BCB polymer. Therefore, it works well for the humidity sensor application. However, the reference sensor is covered with BCB to be encapsulated against moisture [135]. In the humidity sensor application, the planar capacitor is a better choice in comparison with the parallel capacitor. In addition, in planar capacitors, the distance between the electrodes can change during bending. The fabricated humidity sensors are measured in a humidity chamber up to 80 % RH. The measured sensor sensitivity is around 75 % and a response time of 6 sec [135]. The reference sensor can tolerate moisture of up to 75% RH. The reference sensor may uptake moisture from the BCB surface or sidewalls above this range.

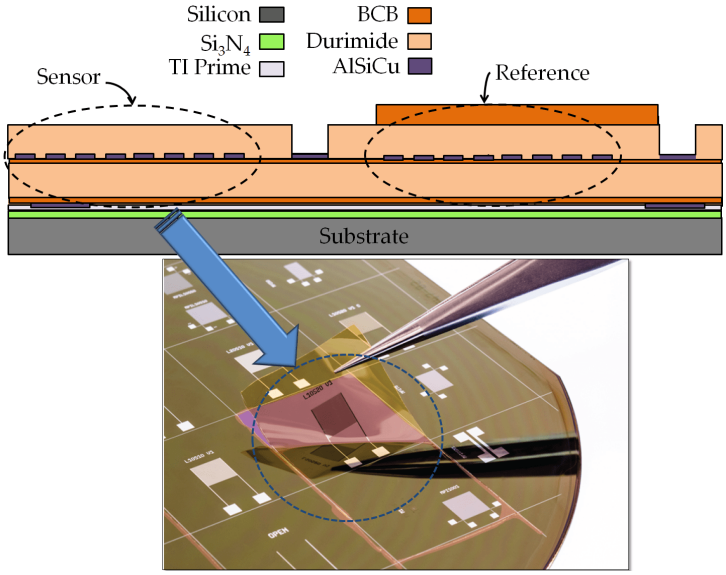


Figure 5.10: Schematic cross section (top figure) and a camera image (below figure) of the humidity sensor in the CFP, respectively [135].

Inductor

For the high-density capacitor fabrication in CFP, a high dielectric constant polymer and smaller thickness are required. However, this requirement is conflicting regarding inductors. A low-dielectric constant (low-k) will cause smaller parasitic capacitance and, therefore, higher operation frequencies for inductors [136]. To solve this challenge, we have chosen BCB with a 5 µm thickness on CFP foil as an intermetal dielectric below spiral inductor. Metal one (AlSiCu) with the thickness of 1 µm is sputtered and patterned on the CFP substrate to form the bottom electrode. Then BCB is spun on the CFP foil surface followed by a photolithography patterning step to open up the via in order to access the bottom and the top electrodes of the capacitors and the center lead metal of the inductors. The BCB on the CFP foil is then cured at up to 250 °C in the convection oven for 2 hours to cross-link. Finally, a 2 µm top interconnect metal (Al) is evaporated to form the spiral metal of the inductors and to make interconnects e.g., ground-signal-ground for both the inductors and the capacitors (see Fig 5.11). The use of thick Al is to reduce the parasitic resistance of the devices, especially for multiple turn inductors in order to realize high-frequency operations [136].

As shown in Fig 5.11, the inductance (L) and the DC resistance of a conductor can be described by the outer length l, turn width W, spacing S, a number of turns N, and thickness of each turn t [137].

The RF characteristics of the fabricated inductors are measured with a LCR meter. The

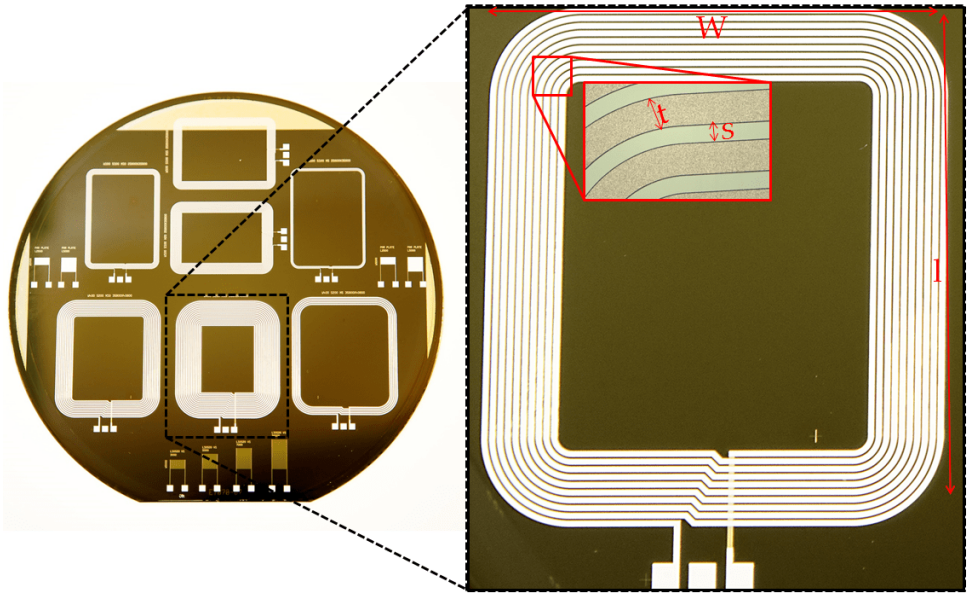


Figure 5.11: Camera image of the wafer level inductor and capacitor fabrication on the CFP. The various inductors and capacitors are fabricated. The inductors are processed based on different W, l, t, N, and S parameters which are shown in the image.

measured L with t=100 µm, S=100 µm, N=10, and W×l=25×35 mm^2 on the silicon wafer, after releasing and bending are plotted in Fig 5.12. First, the inductor is measured on top of the silicon carrier while the silicon wafer is grounded. Next, the fabricated inductor on the foil is released from the substrate carrier (Fig 5.13) and is measured above the thick non-conductive plastic carrier to eliminate the effect of below conductive substrate on the measurement. As a next step, the inductor is bent on top of the cylinders with a different radius of curvature. As shown in Fig 5.13, the overall thickness of the released foil ($\sim$ 20 µm) is not enough to provide the required sensitivity to detect the mechanical strain resulting from bending on the inductor. Therefore, the foil is mounted on top of the thick double sided tape (800 µm) and fixed on top of the cylinder. This way, the distance between the neutral surface of the system and the inductor on top of the foil increases. At different bending radii, the uniaxial tensile strain acting on the loop increases the inductor average diameter, hence the inductance value slightly increases.

According to further measurements, the fabrication of the inductors in the range of 1 µH- 40 µH using CFP technology is achievable. The Near Field Communication (NFC) at 13.56 MHz frequency band is one of the applications of fabricating inductors on the CFP. The NFC technology is a short-range wireless communication technology which transfers information through the electromagnetic induction [139].

From a technology point of view, the functionality of fabricated inductor on polymer

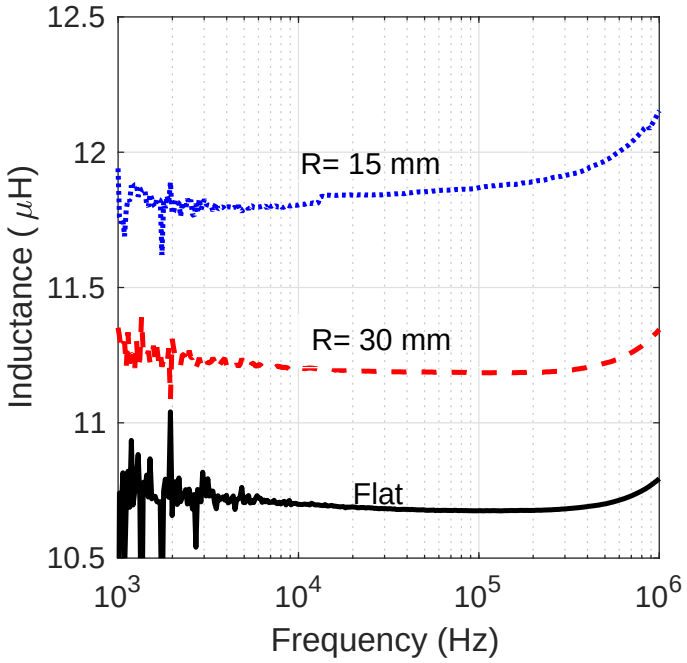


Figure 5.12: Extracted inductance versus frequency on silicon carrier, after releasing, and after bending. All the measurements are performed at the room temperature [138].

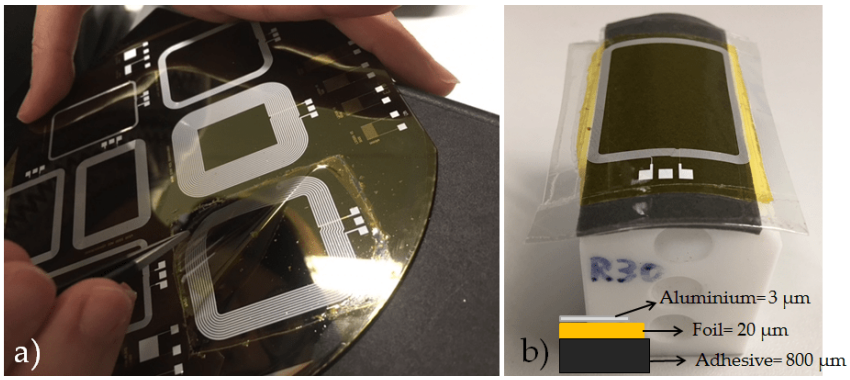


Figure 5.13: a) Camera image of releasing the fabricated inductor on foil from silicon substrate carrier, and b) Camera image of bent inductor on foil along with the epoxy adhesive using cylinder.

foil is proven. The role of parasitic capacitors versus different substrates and corresponding models should be extracted at the circuit design level. A further measurement, verification with simulations, and integration of NFC, humidity sensor, and multiple silicon chips as a hybrid system demonstration will have to be done in the future.

5.1.4 Active Elements in the CFP

In order to validate Chip-Film Patch (CFP) technology from the point of view of the electrical behavior of the circuits, a study is performed to evaluate the impact of the chip back-thinning and embedding process on the electrical characteristics of basic discrete devices, in this case, bipolar and MOS transistors. The DC characteristic of Bipolar and MOS transistors before thinning, after thinning, and after partial embedding in foil are measured and compared. The gate leakage and DC characteristics of MOS transistors in addition to the variation of the collector and the base currents (I_C, I_B) in bipolar transistors are investigated and described in Appendix B. In general, the differences are in an acceptable range of device functionality and are mainly due to induced stress on a silicon chip and the micro-crack generation while transporting or back-thinning or dislocations in the bipolar devices [140].

In addition to the DC measurements, the RF characteristic of SiGe BiCMOS HBT differential power amplifier (DPA) is measured under six conditions: I) thick Si chip on vacuum chuck, II) thick Si chip on printed circuit board (PCB), III) thinned Si chip (45 µm) on vacuum chuck, IV) thinned Si chip (45 µm) on PCB, V) thinned Si chip embedded and interconnected inside CFP polymer foil, and VI) thinned Si chip embedded inside the CFP polymer foil with a heat spreader on the back of the chip. The measurements are compared to the simulation results as well. The measured S-parameters are plotted together with the simulation results in Fig 5.14 [1].

The measured small-signal gain of the DPA is 10.85 dB and 10 dB at 5.5 GHz before and after thinning, respectively, and the center frequency is shifted around 300 MHz towards higher frequencies compared to the measured results with the thick silicon. In the designed PA chip, the inductors on thin Si chip (thickness of 45 µm) have slightly lower inductance due to the ground image currents in the ground plane. The reflected image inductor is located at twice the substrate thickness from the actual one, and a negative mutual inductance occurs because of the current flowing in the opposite direction [142]. Therefore, the center frequency and gain are changing depending on the material below the IC and relate to the image inductance. The small degradation of S-parameter after embedding the chip with/without heat spreader inside the CFP is observed.

[1]The measurements and simulations are done by Mr. Sefa Özbek at Institut für Elektrische und Optische Nachrichtentechnik (INT)

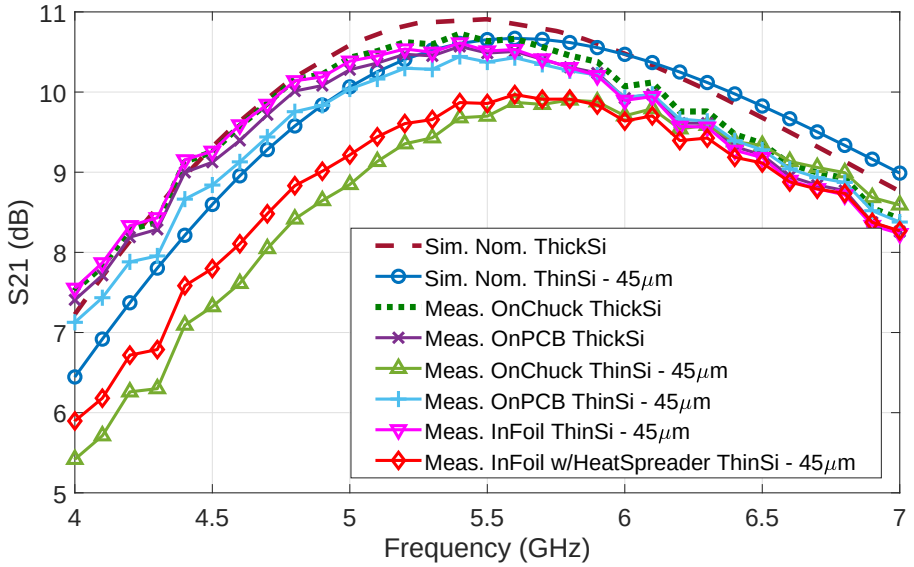


Figure 5.14: Simulated and measured S21 of PA [141].

5.2 Mechanical Stress Analysis

Mechanical stress analysis is one of the important aspects which should be evaluated in microelectronic and flexible electronics. External force for bending the flexible system-in-foil can affect the reliability of materials, such as the embedded silicon chips and the polymers. Besides that, the piezoresistive effect caused by mechanical bending may influence the functionality of the system on the device level. In addition, induced internal stress due to a thermal mismatch between materials and related deformations can lead to an array of problems, such as wafer handling problems, alignment difficulties, and losing interconnections. Therefore, understanding the concepts of stress, strain, and the elastic mismatch can help us to understand, predict, and minimize the related problems.

5.2.1 Physical Basics of Mechanical Stress

Mechanical stress σ is defined by the internal forces response on a cross sectional area A acting within a deformable solid body which is externally loaded. The internal perpendicular forces on the cross section are characterized by the normal force F_N [143] (Fig 5.15.a).

Mathematically, stress is a measure of the average force per unit area of a surface within a body on which the internal forces act. According to the balance of forces, the normal

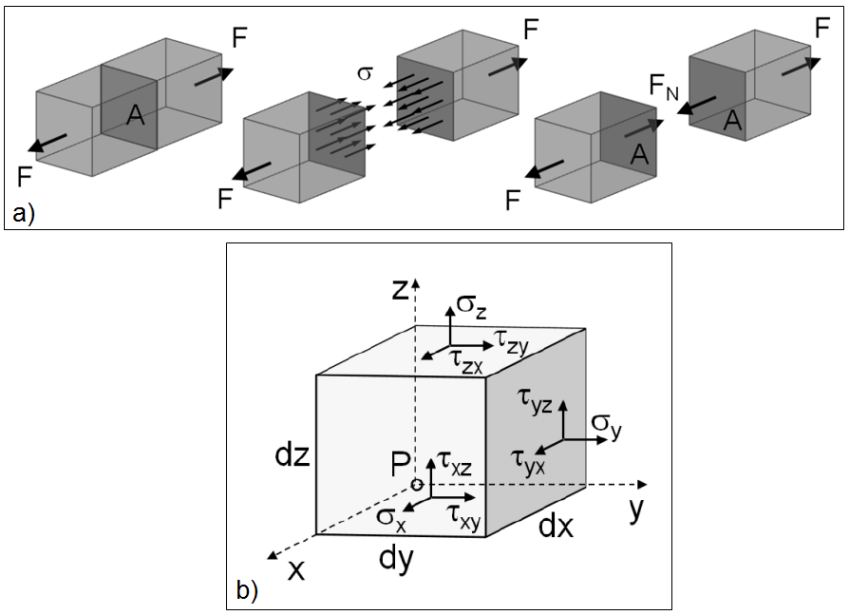


Figure 5.15: Schematic illustration of mechanical stress a) F_N stands for internal force in response to the external loaded force. b) The components of the mechanical stress tensor on an infinitesimal cube [143].

force F_N is equivalent to the external load F and, hence, the mechanical stress can be calculated by:

$$\sigma = \frac{F}{A} \tag{5.3}$$

Three types of stresses are named as: tensile stress ($\sigma > 0$), compressive stress ($\sigma < 0$), and shear stress. In general, external forces on a solid body can act in different directions which may cause variable stress in the cross section. The mechanical stress at an arbitrary point P (Fig 5.15.b) is determined by the nine element stress tensor σ_{ij} (equation 5.4). The σ_x, σ_y and σ_z are three normal stresses and τ_{xy}, τ_{xz}, τ_{yx}, τ_{yz}, τ_{zx}, τ_{zy} are shear stress components.

$$\sigma_{ij} = \begin{bmatrix} \sigma_x & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_y & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_z \end{bmatrix} \tag{5.4}$$

Mechanical strain ϵ is deformation of a physical body caused by the applied forces. The various types of strains are categorized by; positive and negative linear strain produced by the tensile load and compressive load, respectively, shear strain and torsional deformation.

When axially loaded, the normalized length change ΔL/L of a body while assuming that the cross section is unchanged, can be denoted by the mechanical strain and can be described as:

$$\epsilon = \frac{\Delta L}{L} \tag{5.5}$$

The general deformation of the body can be described by the second order strain tensor ϵ_{kl}. In equation 5.8, ϵ stands for the normal strain components and γ for the shearing strain.

$$\epsilon_{kl} = \begin{bmatrix} \epsilon_x & \frac{1}{2}\gamma_{xy} & \frac{1}{2}\gamma_{xz} \\ \frac{1}{2}\gamma_{yx} & \epsilon_y & \frac{1}{2}\gamma_{yz} \\ \frac{1}{2}\gamma_{zx} & \frac{1}{2}\gamma_{zy} & \epsilon_z \end{bmatrix} \tag{5.6}$$

Poisson's ratio ν is a negative ratio of the lateral contraction of the material to the longitudinal extensions (Fig 5.16). The poisson's ratio can be expressed as;

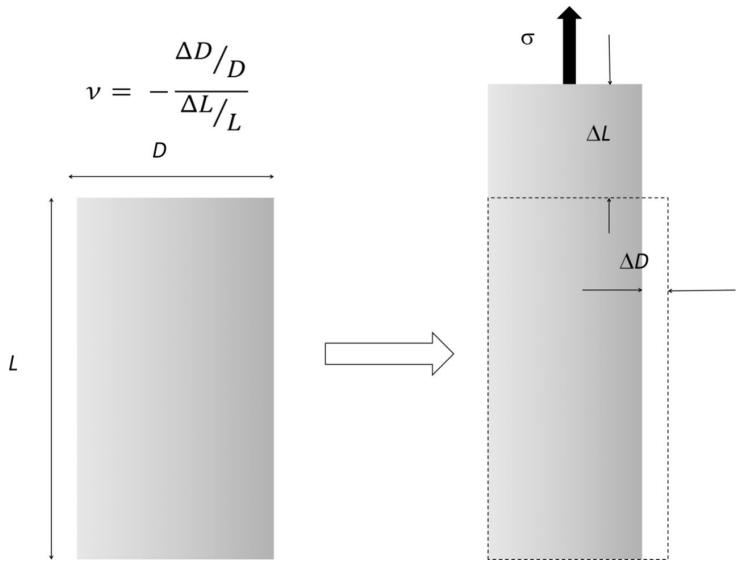


Figure 5.16: Defining Poisson's ratio from the negative ratio of lateral and longitudinal stress [144].

$$\nu = \frac{\text{transverse strain}}{\text{longitudinal strain}} = -\frac{\epsilon_t}{\epsilon_l} = -\frac{\frac{\triangle D}{D}}{\frac{\triangle L}{L}} \tag{5.7}$$

Accordingly, the relation between the three normal strain components and the Poisson coefficient ν is expressed by equation 5.8.

$$\begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \end{bmatrix} = \begin{bmatrix} 1 & -\nu & -\nu \\ -\nu & 1 & -\nu \\ -\nu & -\nu & 1 \end{bmatrix} \cdot \begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \end{bmatrix} \tag{5.8}$$

In silicon with its anisotropic nature, the Poisson coefficient along the crystallographic [100]-direction (ν_{100} = 0.28) is bigger in comparison with the [110]-direction (ν_{110} = 0.06) [143]. Theoretically, Poisson's ratio for isotropic materials should be $1/4$; furthermore, the maximum value for ν is 0.50.

Young's modulus E, also known as the elastic modulus, represents the stiffness property of the material. It defines the relationship between stress σ and strain ϵ of a material. In the linear elastic region (Fig 5.17) the relation between normal stress and strain is demonstrated by Hooke's law (equation 5.9).

$$E = \frac{\sigma}{\epsilon} \Rightarrow \sigma = E \cdot \epsilon \tag{5.9}$$

Stress-strain relationship

The stress-strain diagram shows a relationship between an applied load to a material and the deformation of the corresponding material, caused by the load. The stress-strain diagram is determined by the tensile test. Tensile tests are performed in the tensile test machines, giving controlled uniformly increasing tension force, applied to the testing sample [145]. In Fig 5.17, the **elastic region** is the linear part of the graph with it's slope being used to calculate the Young's modulus. If material is stretched only in this region and then the force is released, then the material goes back to its original form. The **plastic region** is the region of permanent deformation. If material is stretched into this region, then it starts to permanently deform and, thus, the material never returns back to its original shape. **Yield stress** is the minimum stress that causes permanent deformation. **Ultimate tensile stress** is the maximum stress that material can tolerate before the ultimate failure starts. "**Necking** is a localized decrease in the cross sectional area". **Fracture stress** is the point in the curve which is the last stress state for the material before it fails [145].

BCB and polyimide as plastic materials have a broad plastic deformation range compared to the elastic range. However, silicon and glass as rigid materials have fracture points closer to the yield strength [57].

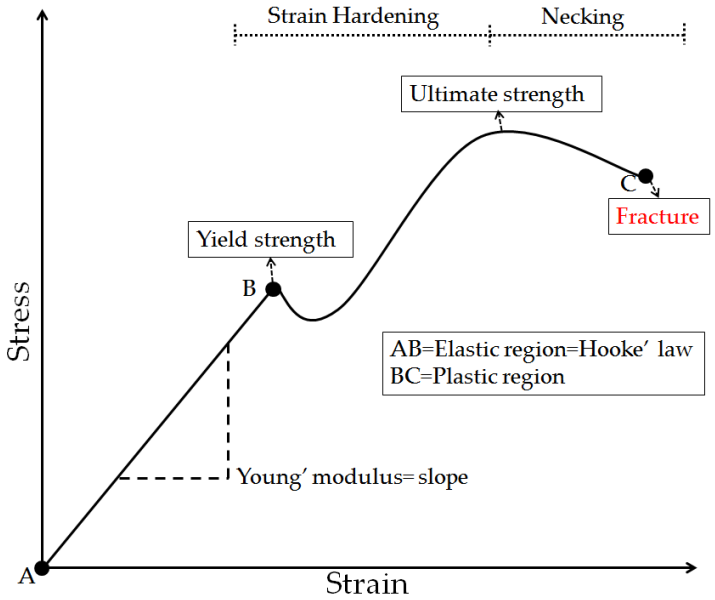


Figure 5.17: The stress-strain diagram.

5.2.2 Stress-Induced Warpage during CFP Processing

In the flexible electronic technology, the organic material is typically deposited at an elevated temperature while the substrate is flat. Upon cooling, a stress field arises due to the difference in thermal contraction between the film and the substrate. This thermal contraction occurs due to the mismatch between coefficient thermal expansion mismatch (CTE) of materials. BCB and other polyimides which are thermosetting materials are fully cured, leading to tensile stress when cooled down to room temperature [120]. The total stress and strain on the surface of the silicon carrier with deposited foil layers can, in principle, be categorized into three parts: (i) extrinsic stress, (ii) intrinsic stress due to layer epitaxial growth and lattice misfit, and (iii) stress from coefficient thermal expansion (CTE) mismatch named as thermomechanical stress,

$$\sigma_t = \sigma_{int} + \sigma_{ext} + \sigma_{th} \tag{5.10}$$

where σ_t stands for the total stress, σ_{int} the internal stress, σ_{ext} the external stress, and σ_{th} is the thermomechanical stress due to a CTE mismatch. Internal stress due to a lattice mismatch can be ignored since no epitaxial growth is involved in the device fabrication. Also, external stress is negligible, as we have avoided any externally applied load. So, we just focus on stress effects due to the CTE mismatch. Therefore, equation 5.10 can be summarized as,

$$\sigma_t = \sigma_{th} \tag{5.11}$$

The coefficient thermal expansion of the used materials in CFP is written in table 5.1. The CTE mismatch causes thermal strain and stress which is either tensile stress (con-

Table 5.1: The coefficient thermal expansion of used materials in the CFP

Material	BCB	Durimide	PI2611	AlSiCu
CTE (ppm/°C)	42	52	3	24

cave bow) or compressive stress (convex bow). In tensile stress, thermal expansion coefficient of deposited material (α_f) is higher than the substrate's coefficient ($\alpha_f > \alpha_s$). However, in compressive stress it is the opposite ($\alpha_f < \alpha_s$).

If thermosetting films with tensile stresses identical to BCB and polyimide are deposited on a silicon substrate carrier, the silicon wafer will bend to relax the film stress until the equilibrium of stress and bow is reached. The resulting induced wafer bow from the thermal mismatch of the polymer film deposition on the substrate is illustrated in Fig 5.18. In Fig 5.18, the subscripts s and f are for the substrate and the film, respectively. Besides that, T_d and T_r are for the deposition and room temperatures, respectively. Figure 5.18 represents a film deposition on a free-standing substrate at an

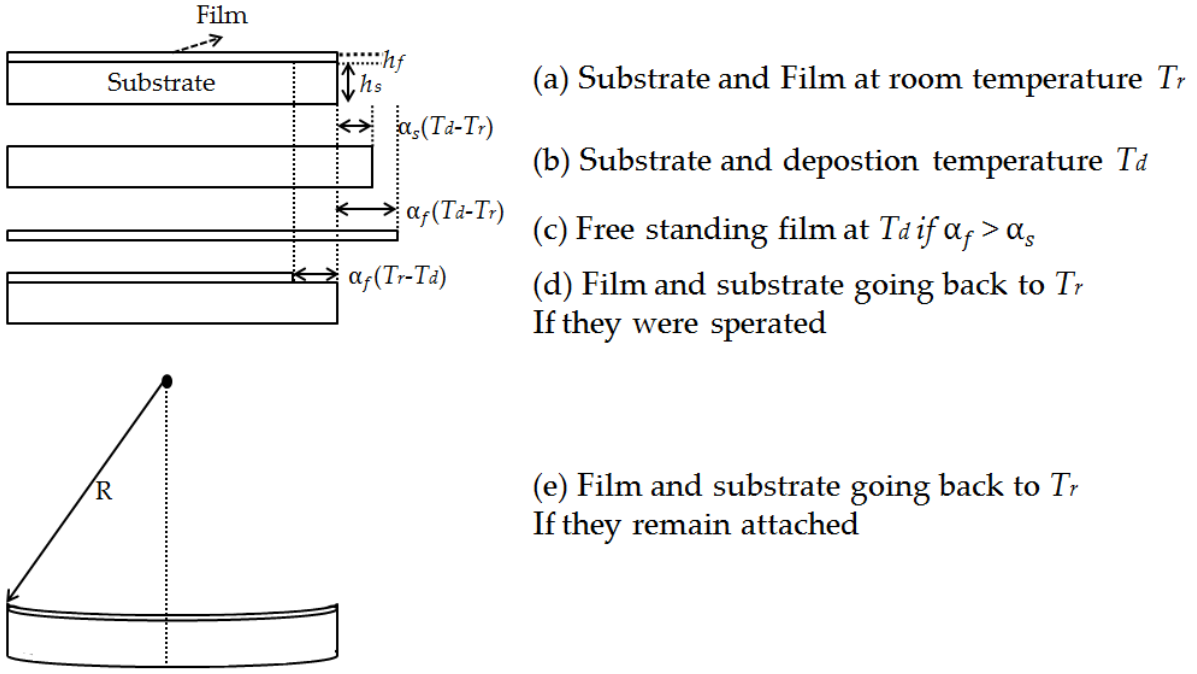


Figure 5.18: Graphical illustration of substrate bending mechanism due to residual stress resulting from the tensile stressed film.

elevated temperature. The substrate is held flat during the film deposition. It expands

when heated to the deposition temperature but remains stress-free. The growing film may develop a built-in strain ϵ_f that causes a built-in stress σ_f. The built-in strain arises from atoms deposited in out-of-equilibrium positions. Next, the unconstrained workpiece is cooled down to room temperature. Since the coefficient of thermal expansion (CTE) of the deposited film, α_f, is higher than that of the substrate, α_s, the film wants to shrink more than the substrate, forcing the workpiece to curves inwards. The generated thermal strain can be calculated as,

$$\epsilon_f = \epsilon_{th} = (\alpha_f - \alpha_s)(T_\mathrm{d} - T_\mathrm{r}) \tag{5.12}$$

where ϵ_f is the total film strain and ϵ_{th} stands for the thermal mismatch foil strain. It is assumed that the strain induced in the film is caused by the CTE mismatch. By assuming an isotropic film and no stress in direction normal to substrate, the biaxial film stress (σ_f) is calculated in equation 5.13 (ϵ_x= ϵ_y= ϵ_f, σ_x= σ_y= σ_f and σ_z= 0).

$$\sigma_f = \frac{E_f}{1-\nu_f} \cdot \epsilon_f \tag{5.13}$$

Here, E_f and ν_f are the modulus of elasticity and Poisson's ratio of the film, respectively. The resulting radius of the curvature on the substrate R after polymer layer deposition (Fig 5.18) can be calculated from Stoney's formula which is written in equation 5.14 [120].

$$R = \frac{E_s}{1-\nu_s} \frac{h_s^2}{6\sigma_f h_f} \tag{5.14}$$

E_s and ν_s are the modulus of elasticity and Poisson's ratio of the substrate, respectively. h_s and h_f stand for the thickness of substrate and film, respectively.

Equation 5.14 can be extended to the curvature estimation with multilayer films deposited foils on substrate ($h_f \ll h_s$). In this case, the total bending curvature is the sum of the curvatures that each of the layers would introduce separately on the substrate. Since the wafer bow is conveniently measured by using a profilometer, we need to convert the results from both, the simulations and the measurements, to either curvature or wafer bow (equation 5.15). R stands for the radius of a curvature of the silicon substrate after the polymer layer deposition. We assume that the silicon wafer is perfectly flat prior to the processing.

$$\text{wafer Bow} = \frac{\text{radius of wafer}^2}{R} \tag{5.15}$$

Fig 5.19 shows the comparison of the analytical calculation based on Stoney's formula to the measurements done by the profilometer. As shown in Fig 5.19, the measured

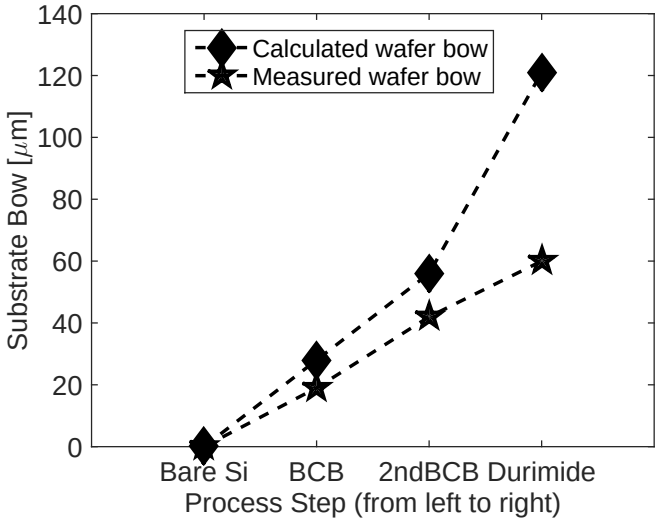


Figure 5.19: Bow comparison between analytical calculation and measurements vs. film deposition steps [95].

wafer bow is less than the calculated one. This divergence is attributed to an overestimation of the thickness of BCB and polyimide, as those films are typically reduced in volume after being cured, which limits the exact stress calculation based on as-deposited thickness. To evaluate the amount of unwanted induced warpage on a silicon wafer due to the polymer deposition, a Finite Element Method (FEM) simulation of the deposited foil on the silicon carrier is performed. In this case, the finite element program ANSYS 15.0 (APDL) is used. With the given ANSYS model, the behavior of BCB thin-film deposited on the silicon carrier was parametrically investigated. This numerical value is in line with previous analytical and measured values for the same thickness of BCB which is deposited on silicon (see in Fig 5.20) [146].

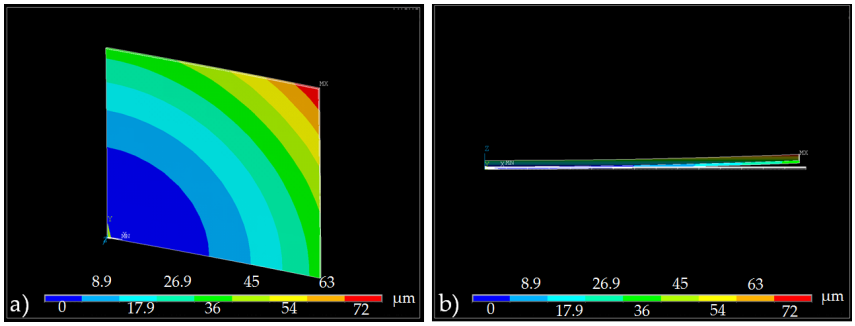


Figure 5.20: Z-displacement simulation of deposited BCB on a silicon carrier. a) Front side view, b) Cross section and concave warpage.

5.2.3 Numerical Estimation of Stress on Chip in CFP

In the case of chip embedded in polymer foil, the chip inside the polymer foil or on top of the polymer foil is under various types of stress which can be categorized as;

- Thermal mismatch between the CFP polymers and embedded silicon chip inside foil
- External stress which occurs in the bending. It is important to investigate the amount of stress on the chip during the bending status. This analysis is also helpful when investigating the fracture point of the embedded thin silicon chip in polymer foil or the metal interconnection transition from the chip to the foil.

In this part, the focus is mainly on the analytical estimation of stress on the chip during bending and under an external force which is done for two different conditions: single chip on foil, a single chip inside foil. To evaluate the amount of resultant stress from cylindrical bending of the system, a Finite Element Method (FEM) simulation [2] of the chip on foil system is performed. In this case, Workbench ANSYS 17.1 is used where the FEM model is constructed with layer dimensions and properties similar to the CFP technology. For the sake of simplicity, all the layer materials used in the model are considered isotropic and linearly elastic. In order to handle the wide variety of materials and conditions easily, the model presented is built using the parameterization features of the FEM software (Ansys). With the parameterized code available any number of variations can be run easily.

The Ansys 17.1 Workbench FEM is used to determine the stress magnitude and distribution in the system at different bending radii R and the chip thicknesses. The uniform bending of the system on the cylinder is achieved by applying an external force F on the right edge of the system. The contact pair between the cylinder surface and the foil is rigid-to-flexible. The mesh sensitivity analysis revealed that the further refinement of the mesh does not change the results significantly. The maximum stress on the ultra-thin silicon chip is limited to a maximum of 300 MPa. Above this degree of stress, an undesired chip fracture may occur. The material properties are shown in table 5.2.

With on-foil chip with R= 10 mm and F= 9 mN, the maximum stress is equal to 241 MPa on the corners of the silicon chip (see Fig 5.21). The applied force and corresponding bending is transferred from the foil to the chip layer via glue layer below the chip. Based on the simulation, the maximum stress for the embedded chips on foil during bending happens along the edges of the chip. The stress parallel to the x-axis is generated by the applied force and corresponding bending which is transferred from the

[2] These simulations were done in a team with Miss Zahra Mardy and were part of her internship at IMS CHIPS.

Table 5.2: Mechanical properties and thickness of the material layers in the ANSYS simulation. In this table, the embedding "Foil" stands for the sum of Foil 1 and Foil 2.

Layer	Thickness	Size	E-modulus	Poisson's ration	CTE	Material
	µm	mm^2	GPa		ppm/°C	
Chip	50	2×1.3	168.9	0.064	2.56	Silicon (<110>)
Foil 1	12.5	20×5	2.9	0.34	42	BCB
Foil 2	45	20×5	2.8	0.34	52	Durimide

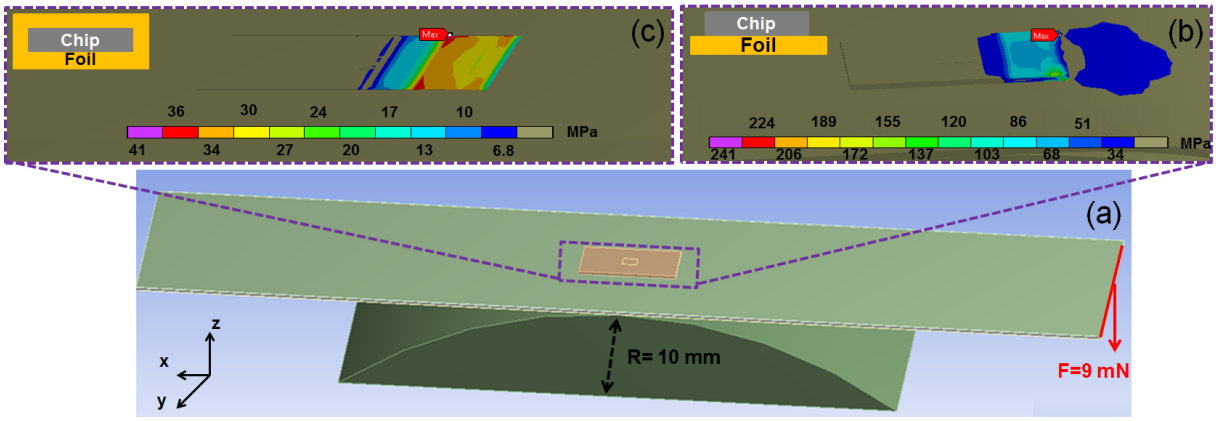


Figure 5.21: FEM Ansys simulation of CFP bent over a cylinder with a 10 mm radius, (a) The cross section image of the built system in Ansys. The uniform bending of the system on top of the cylinder (10 mm) is achieved by applying an external force F on the right edge of the system and the corresponding uniaxial tensile stress on top of the chip is estimated, (b) The chip is attached to the foil from all sides and only the top surface is free, (c) The chip is embedded inside a symmetrical polymer foil.

foil to the chip layer via glue layer below the chip. In addition, the stress parallel to the y-axis is caused due to the peeling effect and tensile stress. Both of them, introduce a non-uniform stress distribution on the surface and along the edges of the chip. In reality, the failures like delamination and cracks usually happen along the edges of the chip bonded to the foil [147].

The FEM simulation is repeated for the chip with the same size and thickness (see table 5.2), which is embedded symmetrically inside the foil. The thickness of foil on top of the chip is equal to the sum of "Foil 1" and "Foil 2" (table 5.2) below the chip. It is observed that for the same bending radius and external force, the amount of stress for the chip attached to the foil is larger than the amount of stress for the chip completely inside the foil. This effect is attributed to the shifting of neutral surface position due to the thickness of the foil. For the embedded chip inside the symmetrical polymer foil, the neutral surface of the system is in the middle. However, for the embedded chip on top of the foil, the neutral surface is shifted slightly depending on the chip thickness, the chip's E-modulus, the foil thickness, and the foil's E-modulus [143]. The position shifting of the neutral surface in a chip on foil system can affect the stress level increase in the system as the foil thickness increases significantly compared to the chip. Besides externally loaded stress on the embedded chip while bending, there is an induced internal stress which is caused by the CTE mismatch between the embedding foil and the embedded thin chip.

5.3 Thermal Management of CFP

The thermal management of ultra-thin silicon chips with a total thickness smaller than 20 µm in comparison with bulk silicon chips with a thickness larger than 400 µm is challenging because of the increased lateral thermal resistance [148]. In addition, the maximum surface temperature of a flexible polyimide substrate is higher because of the poor thermal conductivity of the polyimide substrate. Therefore, thermal characterization of the embedded chip inside the polymer foil is the topic of this section and a prediction of the temperature gradient of such chips inside the Chip-Film Patch is necessary.

5.3.1 Fundamentals

Heat transfer, in general, takes place with three primary mechanisms: conduction, convection, and radiation. Each of these mechanisms has its own mathematical model. As shown in fig 5.22, we refer to different types of heat transfer processes as modes [149].

Conduction – The physical mechanism of conduction is easily described by assuming

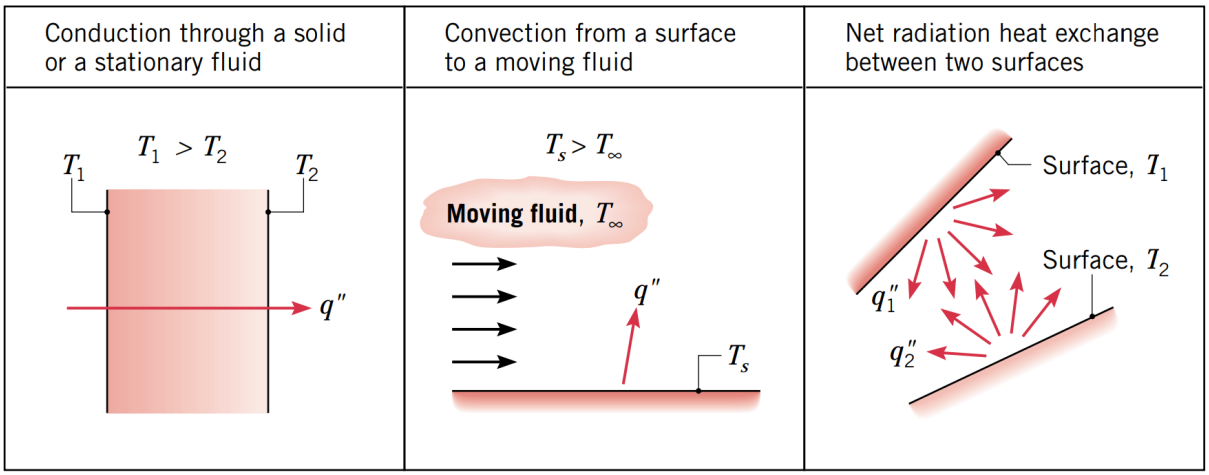


Figure 5.22: Conduction, convection, and radiation heat transfer modes [149].

a gas with a temperature gradient. The gas may fill the space between two surfaces that are kept at different temperatures. The temperature at any point relates to the energy of the gas molecules at that point. This energy is related to the random translational motion, as well as to the internal rotational and vibrational motions, of the molecules. However, in case of solids, conduction attributes in form of lattice waves induced by atomic vibration. In addition to lattice vibration, the random motion of free carriers associate to the conduction heat transfer in conducting materials [150].

For heat conduction, the rate equation is known as Fourier's law. For the one dimensional plane wall, having a temperature distribution $T(x)$, the rate equation is expressed as

$$q_x'' = -k\frac{dT}{dx} \tag{5.16}$$

The heat flux q_x'' (W/m^2) is the "heat transfer rate in the x direction per unit area perpendicular to the direction of the transfer, and it is proportional to the temperature gradient, dT/dx, in this direction". The parameter k stands for the thermal conductivity (W/m.K) of the material and is a characteristic of the wall material. The minus sign presents the fact that heat is transferred in the direction of decreasing temperature. Under the steady-state conditions, where the temperature distribution is linear, the temperature gradient may be expressed as

$$\frac{dT}{dx} = \frac{T_2 - T_1}{L} \tag{5.17}$$

and the heat flux as

$$q_x'' = -k\frac{T_2 - T_1}{L} = -k\frac{\triangle T}{L} \tag{5.18}$$

This equation 5.18 provides a heat flux, that is, the rate of the heat transfer per unit area. The heat rate by conduction, q_x(W), through a plane wall of area A is then illustrated as

$$q_x = q_x^{"} \cdot A \tag{5.19}$$

There is an analogy between the diffusion of heat and electrical charge. A thermal resistance is associated with the conduction of heat, same as an electrical resistance which is associated with the conduction of electricity. Defining resistance as the ratio of a driving potential to the corresponding transfer rate, the thermal resistance for conduction in a plane wall is

$$R_{t,cond} = \frac{T_2 - T_1}{q_x} = \frac{L}{kA} \tag{5.20}$$

Similarly, for electrical conduction in the same system, Ohm's law provides an electrical resistance of the form

$$R_e = \frac{E_2 - E_1}{I} = \frac{L}{\sigma A} \tag{5.21}$$

Convection – The heat transfer through gas or liquid with fluid motion is known as convection heat transfer. The convection heat transfer mode is comprised of two mechanisms: random molecular motion (diffusion) and energy transfer by the motion of the fluid. This fluid motion causes the movement of large numbers of molecules in total. In general, the appropriate rate equation is expressed as

$$q^{"} = h(T_s - T_\infty) \tag{5.22}$$

where $q^{"}$, the convective heat flux (W/m^2), is proportional to the difference between the surface and fluid temperatures, Ts and T_∞, respectively. This expression is known as "Newton's law of cooling", and the parameter h (W/m^2. K) is called the convection heat transfer coefficient. It depends on the boundary layer conditions, which are affected by surface geometry and the nature of the fluid motion [151].

Radiation – The heat transfer may occur through solid surfaces or liquids and gases. Radiation heat transfer is energy transported due to the emission of electromagnetic waves (or photons) from a surface or volume. Unlike conduction and convection, radiation does not need a heat transfer medium and can occur in the vacuum. Radiation heat transfer depends on the surface properties, such as colors, surface orientation and the fourth power of the absolute temperature (T^4) of the surface [149]. The basic equation for radiation heat transfer between two gray surfaces is given as

$$q_{rad}^{"} = \epsilon\sigma(T_h^4 - T_c^4) \tag{5.23}$$

where $q^{"}_{rad}$, is the radiation heat transfer and the constant of proportionality σ is the Stefan Boltzmann's constant (σ= 5.67 $\times$ 10^{-8} W/m^2. K^4), ϵ is emissivity of a body compared to a black body (0 < ϵ < 1), T_h and T_c are hot body absolute temperature (K) and old surroundings absolute temperature (K), respectively. Please note that radiation is not considered in further investigations.

5.3.2 Thermal behavior of Embedded Power Amplifier Chip in Foil

As described before, the embedded silicon chips in the polymer foil need to be thinned down to provide the flexible system-in-foil. However, such ultra-thin chips have the low vertical thermal resistance which is beneficial for power chips in which a considerable amount of heat should be dissipated from the chip area. However, by reducing the chip thickness and cross section area, high lateral thermal resistance is implied on the chip's surface opposed to a bulk thick silicon chip. The huge temperature gradient on the surface of the chip could lead to thermal mismatch and reliability problems [152].

This phenomenon can become a serious challenge especially for embedded power devices in polymer foil. The reason behind this is the poor thermal conductivity of the polyimide substrate which causes further self-heating on the chip. Therefore, a thermal behavior of the chip with three power amplifier (PA) units is investigated. The power chip is implemented in a 0.25 µm SiGe BiCMOS bulk Si technology. The chip size is 2.34$\times$1.6 mm^2 and consists of three differential power amplifiers (DPA) as thermal source with maximum a 72 mW power and four temperature sensing diodes as on-chip temperature sensing elements. The main reason for the high temperature in overall transceiver (TRX) systems is the significant self-heating of the power amplifier (PA) because of the great amount of power dissipation and the low thermal conductivity of the below polymer substrate.

Temperature-Sensing Elements

Here, on-chip thermal sensors are more relevant than the discrete element temperature sensors (ex: Pt100 resistor) since a temperature distribution on the chip's surface is to be evaluated. For this purpose, four sensors based on the bipolar transistor diode are designed and embedded into a chip in order to evaluate the temperature distribution at different locations on the chip's surface and, hence, the temperature distribution. It is to be noted that, with transistors, the absolute temperature can be potentially measured but only after the appropriate calibration of the elements. During the measurement step, the current in the transistor is kept at a minimum value (10 µA) to avoid self-heating of the device caused by the temperature sensor. The mathematical equation covering the temperature dependence of a transistor's junction voltage when used in

a diode connection is approximated as [150]

$$V_B = V_{B0} + \beta T \tag{5.24}$$

Where V_B is the forward voltage of the diode, V_{B0} is the sensor's voltage at 0 K and β is the temperature coefficient of the sensor. In this formula, β is a negative number meaning that with increasing temperature, the diode voltage decreases linearly. Equation 5.24 shows that the dependence of the diode junction voltage is linear as a function of the temperature. This linear relation is only valid in a limited range of temperatures. The equation 5.24 is the fundamental equation governing all the voltage to temperature conversions during the measurements conducted in this work.

Measurement Results

As a first step, temperature sensors on each silicon chip are calibrated on the thermal-chuck. The forward bias of each diode is set to 10 µA to avoid self-heating. The calibration curve for the junction voltage as a function of temperature is approximately defined by the equation 5.25 and equation 5.26 for the silicon chips before and after back-thinning ($\simeq$ 45 µm), respectively.

$$V_B = 0.74936 - 0.00136T \tag{5.25}$$

$$V_B = 0.75354 - 0.00149T \tag{5.26}$$

In all cases, the chips are measured on the thermal chuck for the V-T calibration curve. Prior to the temperature measurements, each device under test (DUT) is isolated from the thermal chuck with low thermal conductive foil, while the thermal chuck acts as a thermal heat spreader for the above DUT. Five different scenarios are investigated as: (I) thick PA chip, (II) thin ($\simeq$ 45 µm) PA chip, (III) thin PA chip embedded partially on top of polymer foil, (IV) thin PA chip embedded inside the two-polymer CFP technology, and (V) thin PA chip embedded inside the two-polymer CFP technology with heat spreader (1.5 µm AlSiCu) below chip. The five various samples are shown in Fig 5.23[3].

In this study, PAs (red block) which are shown in Fig 5.24 act as heating sources while the temperature sensors (green blocks) act as sensing elements. Here, the measurement for four diodes is performed with the differential power amplifier near the second diode (D_2) which is powered up (T_2) and then switched off (T_1) after reaching a stable temperature.

[3]These measurements are done by Mr. Sefa Özbek at Institut für Elektrische und Optische Nachrichtentechnik (INT)

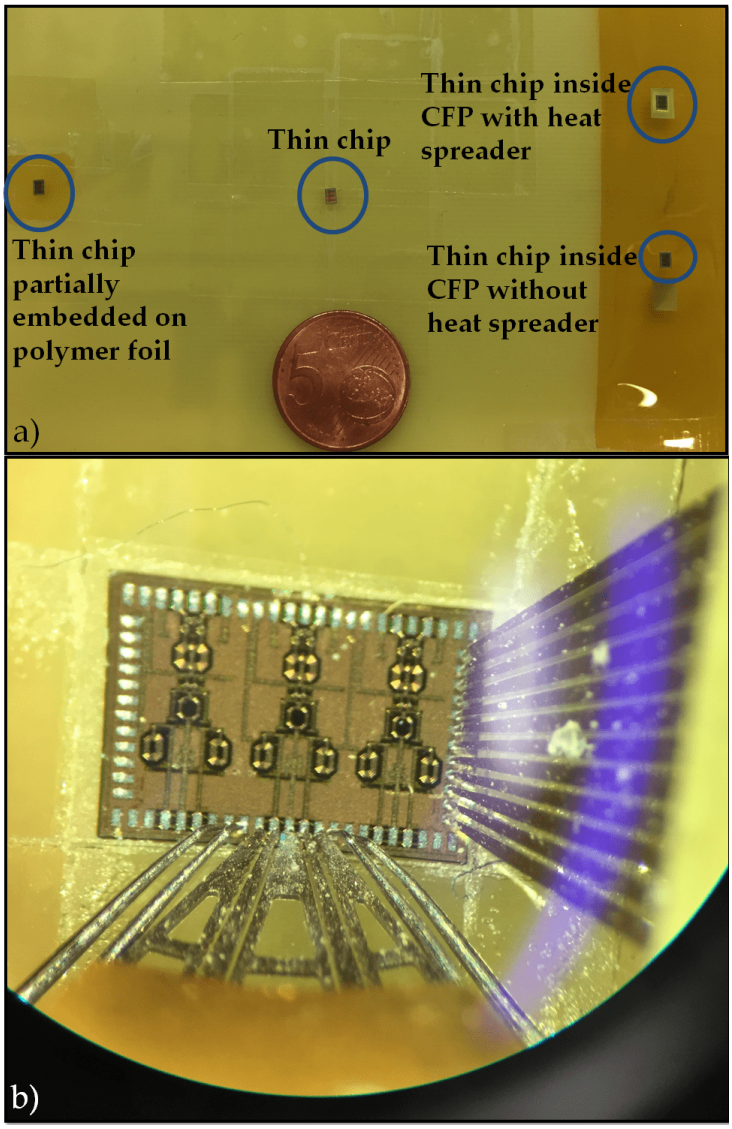


Figure 5.23: Thermal behavior investigation of the PA chip under different conditions, a) Camera image of PA chips thermal investigation under four conditions, b) Camera image of measurement setup and probe cards of the PA chips under test [153].

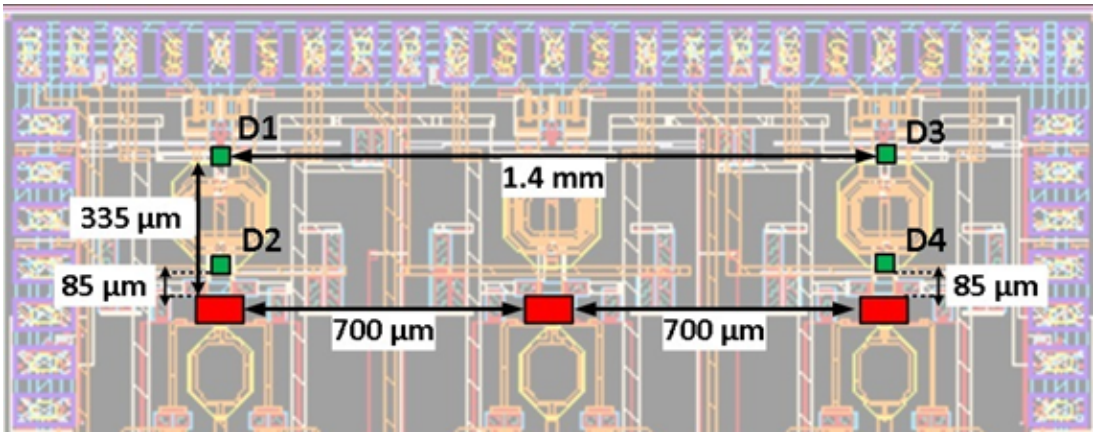


Figure 5.24: Layout of the 3-Path DPA. The red blocks represent the DPA as a heater whereas four green blocks are bipolar based temperature sensing diodes [153].

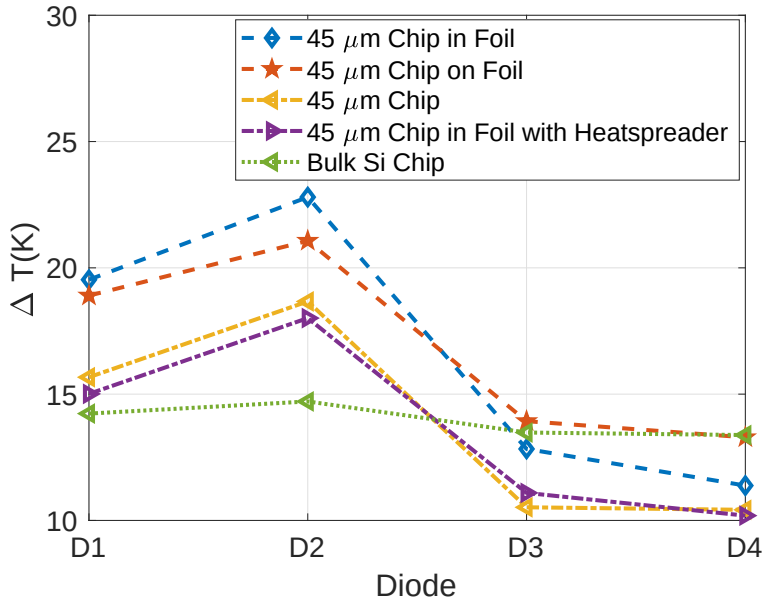


Figure 5.25: Measured surface temperature increase using four different diode locations. The measurement for the four diodes is performed with the differential power amplifier near the second diode (D_2) which is powered up and after reaching a stable temperature is switched off. $\Delta T = T_2 - T_1$, T_2 and T_1 are the measured temperatures with PA switched On and OFF, respectively [153], [154].

Fig 5.25 indicates that the maximum surface temperature of the thin silicon chip is 18 K. However, the maximum temperature of the thick silicon chip only reaches up to 14 K. In addition, the thinned embedded chip inside the CFP foil experiences the maximum temperature due to the low thermal conductivity of the embedding polymer and corresponding self-heating loop. This problem is minimized by fabricating a thin layer of heat spreader below the embedded thin chip inside foil.

In general, after silicon chip back-thinning, D_1 and D_2 temperature diodes near the thermal source experience higher temperature compared to the thick silicon chips due to a larger lateral resistance. In addition, the temperature gradient across the entire surface of the thick chip is lower opposed to the thin chip due to higher vertical thermal resistance. The thermal resistance (K/W) is expressed as

$$R_{\text{th}} = \frac{\Delta T}{P} = \frac{L}{K_{\text{th}} A} \tag{5.27}$$

In equation 5.27, P (W) is the dissipated power, ΔT (K) is the temperature rise above the ambient at the diode location, L is the length of the sample, K_{th} is the isotropic thermal conductivity of silicon (W/mK), and A is the cross section area [148]. The equation 5.27 can be used to calculate both, the vertical and the lateral resistance. The calculated resistances can be helpful when predicting the thermal behavior of the system using a simplified qualitative lumped-element thermal circuit.

5.3.3 Cooling method

As described before, thin chips embedded in foil are prone to self-heating, which causes the device transconductance to drop, the leakage currents to rise, and the overall component reliability to drop. In this context, beside power optimization and thermal management at circuit level, the thermal management at the technology level needs to be taken into consideration. In this work, two technological concepts are proposed; (I) sub-structuring the thin chip to introduce physical thermal barrier (described in subsection 3.4.5) and (II) adding heat spreader structures at the backside of the chip.

Heat spreader

The thermal management solutions to cool hot spots in an electronic system can be done using heat spreaders. The heat pipes (since the 1980s) [155] or, more recently, the vapor chambers, and the thermal ground plates (TGP) are group of examples in this field [156]. Here, the heat spreading mechanism is performed for temperature uniformization below the PA chip. In addition, the heat spreader below the embedded chip inside the polymer minimizes the self-heating effect due to the low thermal

conductivity of the polymer. The fabricated heat spreader is chosen based on, I) the available technology for CMOS compatibility of the process flow, II) the required flexibility of the final system, III) the size and thickness of the embedded chip, IV) the effect of the fabricated heat spreader to the antenna that is interconnected to the chip, and finally V) the overall costs of the process. In addition to all of the above conditions, a simplified FEM Ansys simulation by parameterizing size, shape, and material of the heat spreader is performed to support the experimental concept [4]. Finally, the heat spreader for the thin power amplifier chip with 72 mW power is fabricated using deposition and structuring 1.5 µm AlSiCu. The heat spreader is twice as big as the embedded chip. The final process flow is illustrated in Fig 5.26.

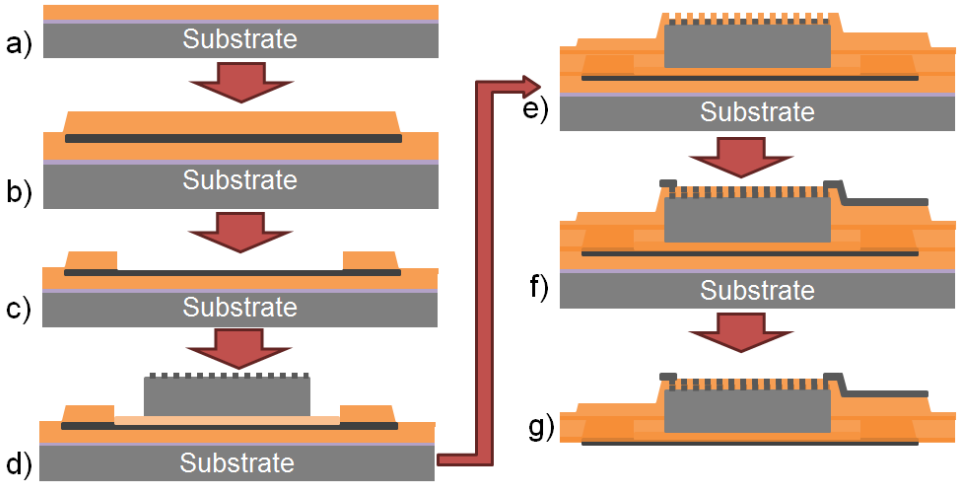


Figure 5.26: Process flow illustration of embedding a PA chip with backside heat spreader inside the CFP, a) applying polyimide, b) fabricating and structuring heat spreader using AlSiCu, and covering it with deposited polymer, c) defining a cavity, d) placing the PA thinned chip in the cavity, e) polymer coating, chip covering, planarization, and via opening, f) the vias metallization and metal structuring, and finally g) release from carrier, transferring flipped foil to the second carrier, back side plasma etching.

Firstly, a 10 µm polymer layer is spin coated followed by sputtering a 1.5 µm AlSiCu layer thickness. The heat spreader is then defined using lithographic and metal etching. Then, a 5 µm polymer is spin coated and a cavity is defined by lithography and polymer plasma RIE. The thinned PA chip is placed and fixed in the cavity using 1 µm BCB as a permanent adhesive layer. After curing the BCB, the chip is covered with polymer and the vias are opened using a mask and plasma etching. Afterwards, the vias are metallized and, simultaneously, an electrical fan-out is provided. After final

[4]The thermal simulations are done by Miss. Zahra Mardy.

metallization, the polymer backside heat spreader can be removed by foil transfer using lamination foil (referring to subsection 3.4.12) and plasma etching. At the end of the process, the embedded chip inside the polymer is released (Fig 5.27) and further electrical measurements are performed.

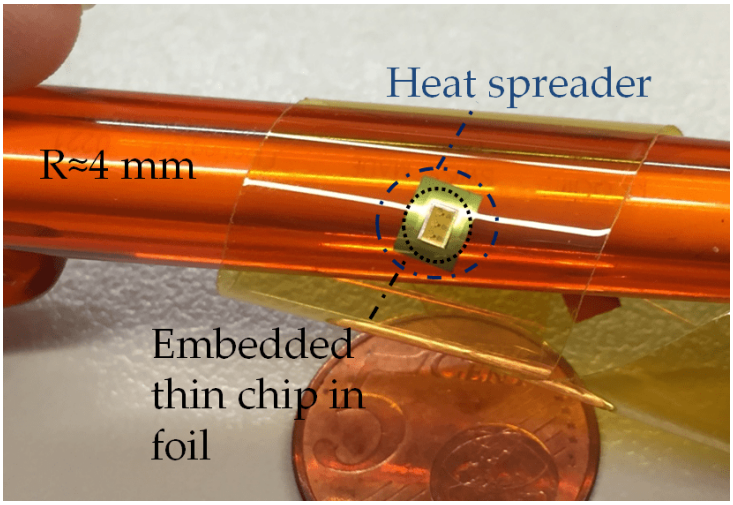


Figure 5.27: Demonstration of the embedded PA chip with the backside heat spreader inside the CFP polymer foil. The integrated system-in-foil is released from the temporary silicon carrier and bendability of the final system is proven [153].

5.4 RF Characterization of CFP

In the last decade the demand for as well as the progress in the field of radiofrequency (RF) has increased. The developing interest for RF identification (RFID) tags onto rigid or plastic (flexible) substrates, and low-cost wireless communications applications are examples for this [157]. The focus in this section is to explain the process flow how to fabricate rigid or flexible antennas in polymer foil, as well as measurement and extracting related high-frequency properties of the polymer package.

5.4.1 Fundamentals

The **dielectric material** has the ability to store energy when an external electric field is applied. By applying DC voltage across a parallel plate capacitor, more energy can be stored with dielectric material being between the plates than without material (a vacuum) between them. It means that the dielectric material increases the storage capacity

of the capacitor by "neutralizing charges at the electrodes" and, therefore, generating an external field [158]. In radio frequency circuit design the characterization of the used dielectric materials is an important step which should be performed before the final design. The dielectric material characterization depends mainly on knowing its relative permittivity with respect to the air (ϵ_r) and its loss tangent (tanδ) [159]. In general, the dielectric constant (ϵ_r) is a complex number given as

$$\epsilon_r = \epsilon_r^{'} - j\epsilon_r^{"} = \epsilon_r^{'}(1 - jtan\delta) \tag{5.28}$$

where, $\epsilon_r^{'}$ is the real part and $\epsilon_r^{"}$ is the imaginary part. The real part $\epsilon_r^{'}$ represents the relative permittivity and the imaginary part $\epsilon_r^{"}$ defines the energy loss in the dielectric medium.

Relative permittivity – is a property which is associated with how much electrical charge a material can store in a given volume. Relative permittivity is defined for materials other than vacuum.

Loss tangent – defines how lossy the material is. For lossless material there is no loss tangent ($tan\delta$=0). The loss tangent is defined as

$$tan\delta = \frac{\epsilon_r^{"}}{\epsilon_r^{'}} = \frac{\text{Energy lost per Cycle}}{\text{Energy stored per cycle}} \tag{5.29}$$

Besides the dielectric material characterization, the **conductivity** (σ) of the conductors is an important factor which should be carried out before the final RF circuit design.

In this work, two groups of antennas, namely, the patch antenna and the dipole antenna are fabricated and measured in the polymer foil. Therefore, the short descriptions for each of them are as follows:

Patch antenna – a microstrip or patch antenna is a low and flat profile antenna with smaller size, lower weight, and less cost in comparison with other antennas [160], [161]. A basic patch antenna is composed of a flat plate and a ground plane. The substrate between the flat plate and the ground plane is usually a dielectric. The distance between the patch and the ground plane or dielectrics' thickness determines the bandwidth (Fig 5.28).

Dipole antenna – a dipole antenna includes two terminals (poles) of wire, rod, or tubing that are one-quarter wavelength long at the desired operating frequency. One of the most common antenna types is the half-wave dipole (doublet) [162]. The dipole antenna is widely used both for radio transmitting and receiving applications (Fig 5.29).

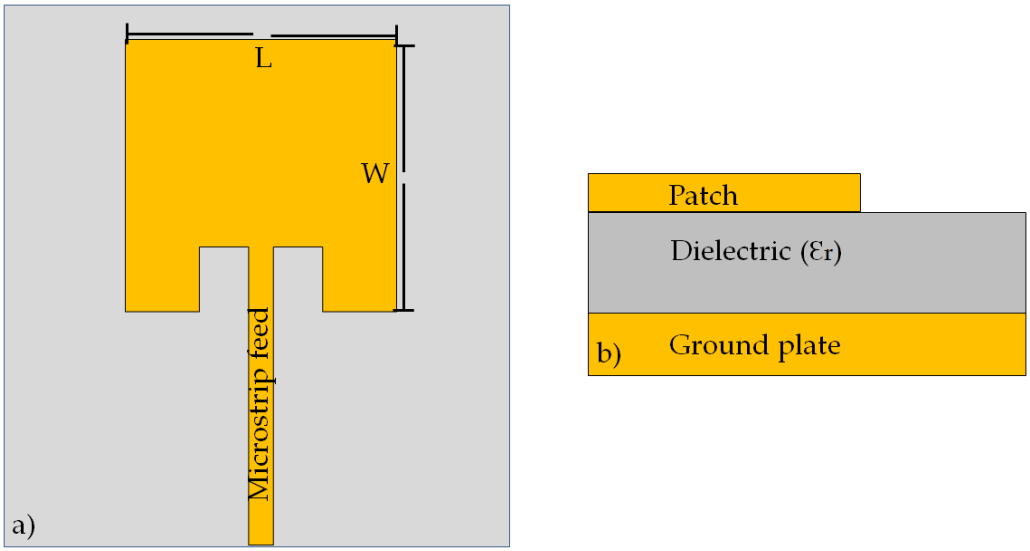


Figure 5.28: The patch antenna graphic illustration, a) Front view illustration, b) Cross section illustration.

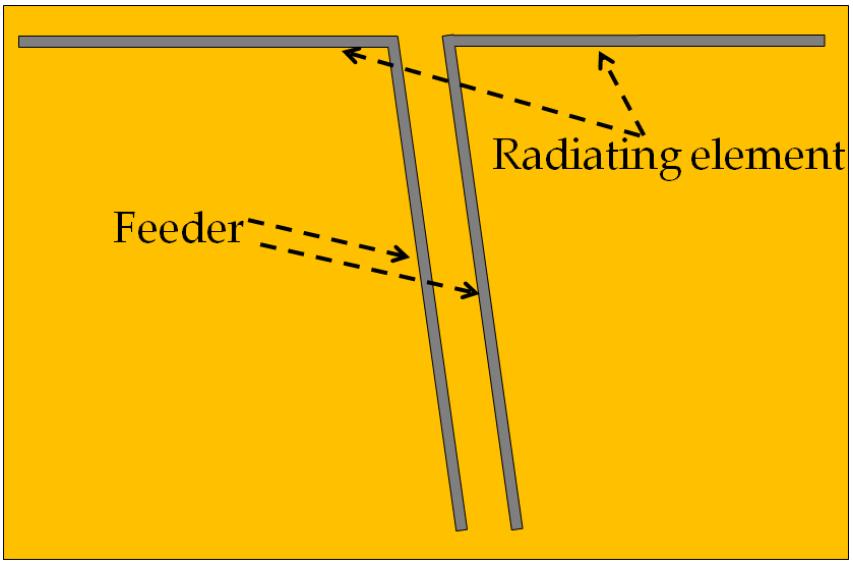


Figure 5.29: Front view dipole antenna graphic illustration.

5.4.2 BCB silicon-based millimeter-wave-on-chip dielectric resonator

The dielectric material to fabricate a millimeter wave antenna using a microstrip antenna array should have a small loss tangent and low dielectric constant to prohibit losses. In addition, the thermal stability of the RF properties for dielectric material should be taken into account. Here [5], BCB with the low relative dielectric constant ϵ_r=2.55, low loss tangent between 0.008 to 0.002 within the frequency interval from 1 MHz to 10 GHz [163], and dielectric stability versus temperature is chosen. In order to keep the technology CMOS line compatible, AlSiCu is chosen as a conductor (σ=3.10^7 S/m). The stacking of layers in the chip is shown in Fig 5.30 [164].

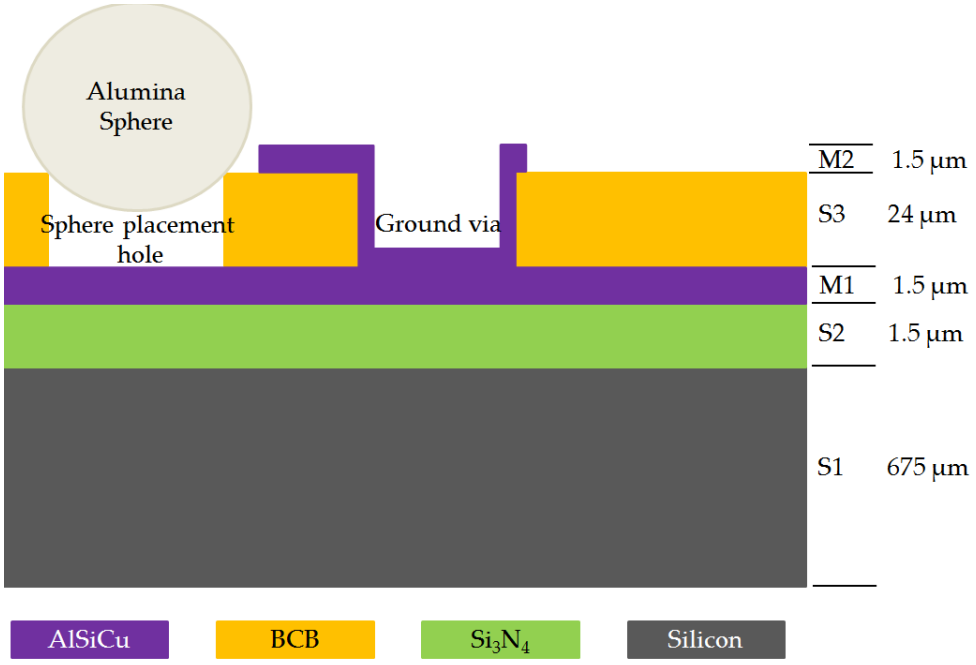


Figure 5.30: Cross section illustration of the on-chip microstrip antenna.

In Fig 5.30, S_1 and S_2 are not relevant in terms of radiofrequency performance as they are shielded from the circuit by the M1 layer, which is required to cover the entire wafer. However, S_1 is a 150 mm silicon carrier and S_2 layer is deposited to compensate unwanted induced warpage caused by depositing top metals and a thick layer of BCB. M_1 layer is intended to cover the entire wafer. In RF terms, it will serve as a ground plane and shield from the high lossy silicon beneath. S_3 or BCB layer acts as the dielectric substrate of the microstrip configuration, the main media in which the wave will be propagated across the chip. The layer will be etched in some regions for the purpose

[5]This work is done in collaboration with Institut für Hochfrequenztechnik (IHF).

of connecting layers M_1 and M_2 (ground vias at the end of the microstrip resonators) or for the purpose of fixing the placement of the dielectric resonator spheres to be coupled on top of the chip. Finally, M_2 will be the top layer of the chip and includes all the different lines and coupling circuits, as well as the pads for the efficient probing of the different structures. In this device, Alumina (Al_2O_3) ceramic dielectric spheres with high permittivity (to limit the size) [164] are used as self-aligned resonator (Fig 5.30). According to the sphere's size, the depth of the cavity should be at least 21 µm with vertical sidewall profile for precise placement of the sphere inside the cavity.

Fabrication process flow

The process flow illustration to fabricate the microstrip antenna is depicted in Fig 5.31. As shown in Fig 5.31, first, a 1.5 µm Si_3N_4 is deposited on top of 150 mm silicon carrier to compensate unwanted warpage. The AlSiCu is sputtered and structured as a ground plane. The AlSiCu structuring is performed to reduce stress which may generate micro-cracks between the AlSiCu and top rigid BCB layer. The adhesion promoter layer is necessary to guarantee enough adhesion between BCB and AlSiCu. After the BCB coating and hard curing, a 600 nm metal is deposited and patterned using lithography. The metal layer acts as a hard mask for RIE thick BCB. The via is etched down to 24 µm and the thin layer of the BCB remains as a passivation layer. After removing the hard mask, the remaining thin layer of the BCB is etched. The second metallization (AlSiCu) is deposited which acts as a hard mask and interconnection. Therefore, the first metal patterning belongs to the second via opening. In the lithography step, a spray coating resist is chosen to cover and passivate the side walls of the already metallized vias (first vias). After the second via opening, the same metallization layer is structured as a final step. The CMOS-compatible mm-wave antenna fabrication is performed based on different designs and in three categories: **A chip to waveguide dielectric resonator-based transition** [165], **the spherical dielectric resonator bandpass flter** [166], and **the spherical dielectric resonator antenna** [164]. From the technological point of view, the fabrication of a CMOS-compatible mm-wave antenna using the BCB and the silicon substrate is proven and despite the thickness non-uniformity of the BCB over the substrate ($\pm$ 2µm), a yield of above 80 % functional devices per substrate is achieved. The graphical summary of the fabricated mm-wave antenna is shown in Fig 5.32.

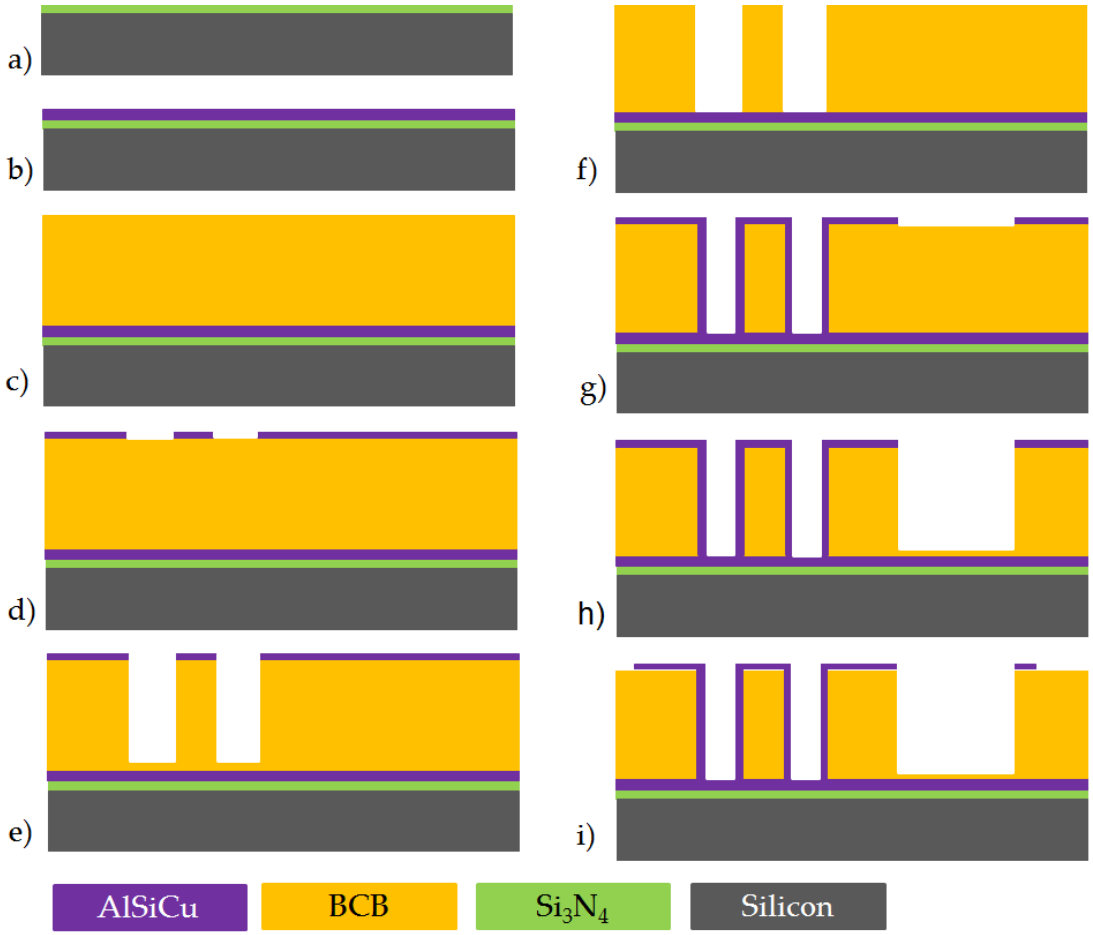


Figure 5.31: Process flow illustration of the millimeter-wave antenna fabrication, a) Pre-surface treatment and Si_3N_4 deposition, b) AlSiCu sputtering and patterning, c) BCB deposition (26 µm) and hard curing, d) Metal hard mask (600 nm) deposition and patterning, e) BCB plasma RIE down to 24 µm, f) Hard mask removing and deep plasma etching, g) Metallization and second via patterning, h) BCB plasma RIE down to 23 µm, and finally i) Metal structuring.

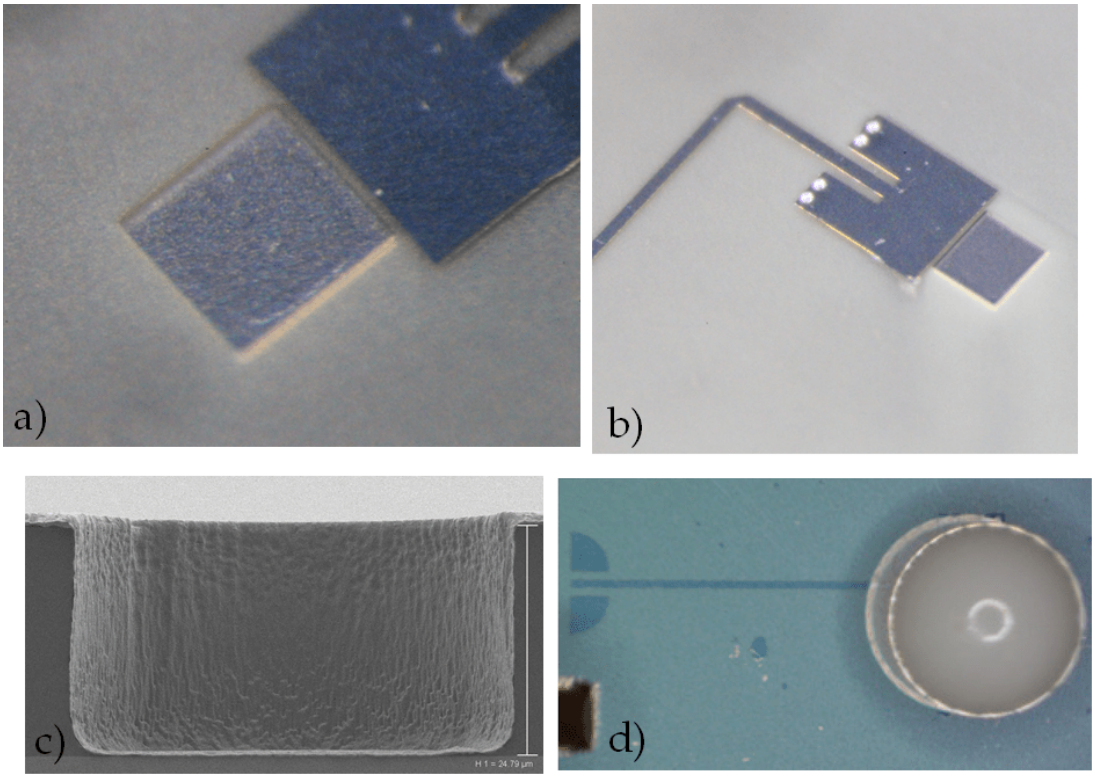


Figure 5.32: Graphical summary of the fabricated mm-wave antenna. a) Photograph of the defined cavity for placement of sphere in the width of 350 µm, b) Photograph of the fabricated microstrip including cavity and smaller vias (40 µm) which are connected to the ground plane, c) SEM cross section of BCB deep etching and metallization. Despite the vertical side wall, the side wall metal coverage is successful, d) Photograph of the spherical dielectric resonator after aligning the sphere inside cavity [164].

Characterization of the dielectric material

The RF measurements are not the focus of this work. However, the RF characteristic of the device from a technologic perspective, such as a dielectric constant, loss tangent, and the conductivity are the topics of this part. The measurements are performed using a vector network analyzer (VNA)[6]. To measure the conductivity of the AlSiCu in the microstrip array, a 30 mm long line at both V and W band is measured on the chip. The TRL calibration kit has a 4 mm length for a V band and 4.26 mm for a W band. Therefore, the measurements have to be compared to the simulations of 26 and 25.76 mm, respectively.

The lines are measured and compared to the simulations. The loss is found to be lower in the measurements, which points to a smaller loss tangent or higher conductivity of the metal. The measurements and simulations are fitted by varying the conductivity of the metal. The conductivity is determined to be about 3.4×10^7 S/m for the V band and 3.8×10^7 S/m for the W band. Due to the measurement inaccuracy, an average of them is taken into the account. Other effects may have some influence as well, like the way the calibration was carried out for both bands, a possible difference of height in the substrate, or a different degree of surface roughness for both lines.

The transmission of the lines and comparison with fitted simulations are shown in Fig 5.33. To determine the dielectric constant based on Fig 5.33, the phase shift along the line is compared between measurements and simulations. A perfect match is found for a permittivity of 2.57. The summary of the comparison between measured properties and simulation values are shown in table 5.3.

Table 5.3: Extracted properties of the fabricated mm-wave antenna.

Parameters	Measured	Simulation value
AlSiCu conductivity (σ)	3.4-3.8 $\times 10^7$ S/m	3×10^7 S/m
BCB loss tangent (tanδ)	0.008	0.008
BCB permittivity (ϵ_r)	2.57	2.55

[6]Measurements and characterizations are done by Mr. Daniel Lopez at Institut für Hochfrequenztechnik (IHF).

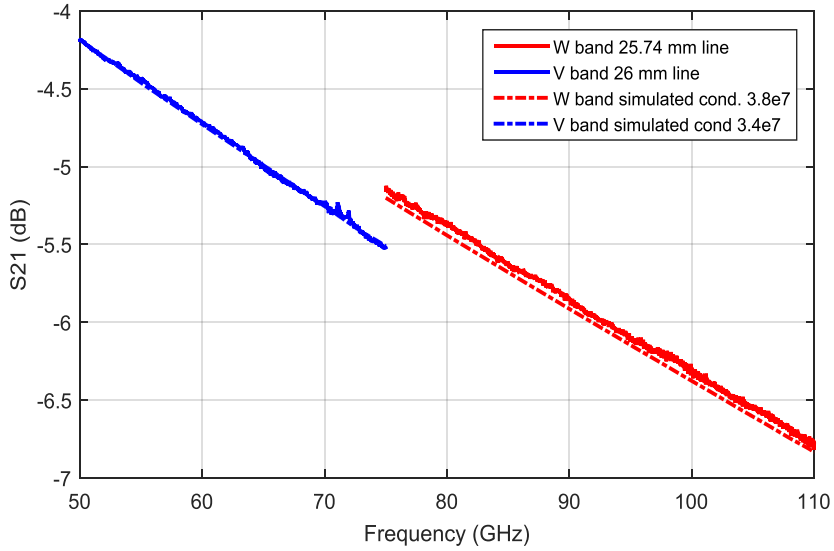


Figure 5.33: Transmission of the lines and comparison with fitted simulations.

5.4.3 Dipole antenna fabrication in CFP

The fabrication of a dipole antenna in combination with the RF thinned chip inside the CMOS-compatible Chip-Film Patch technology is part of the FFLexCom project [7] which is described here. In this work, the required signal transmission is at 5.5 GHz and the integrated antenna on the polymer foil has to adapt to the shape changes during bending to the different radii [167]. As a first step, the best polymer materials, metal, and desired thicknesses are determined. These properties are limited based on the CMOS fabrication compatibility limitations, the flexibility of the overall system, cost, return loss of the antenna, antenna efficiency, and thickness of the thin RF chip. Therefore, the face-up two-polymer CFP layer stack in combination with the thin RF chip is simulated in the *CST MICROWAVE STUDIO* software[8] (Fig 5.34) and all the properties are parameterized to find the best fit from both the design and the technology side of view.

[7] FFLexCom project is a Deutsche Forschungsgemeinschaft (DFG) project with grant-no. BE 2256/25-1.

[8] The simulation is done by Mahsa Rasteh at Institut für Hochfrequenztechnik (IHF).

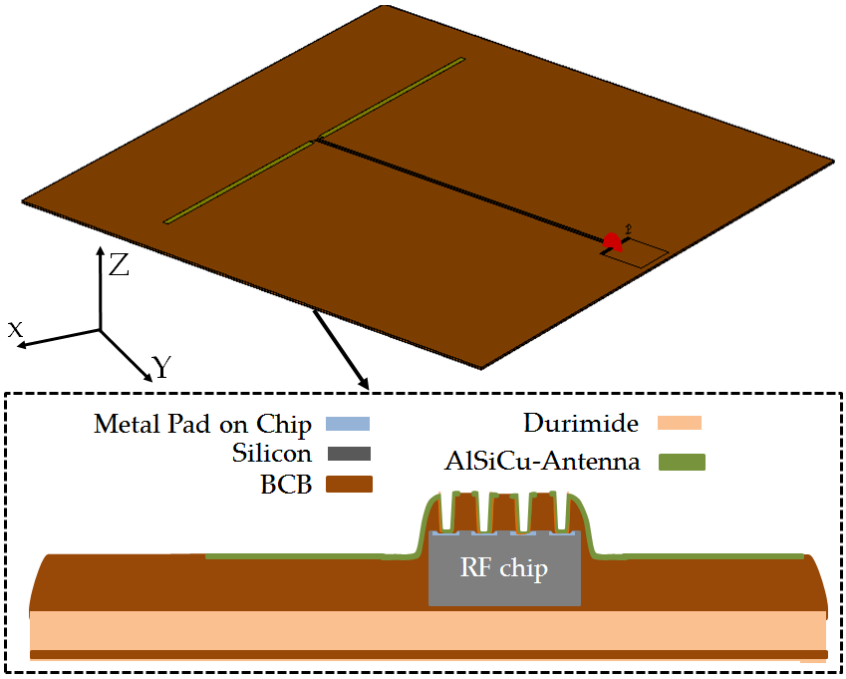


Figure 5.34: Illustration of a dipole antenna including the stack layer of an embedded RF chip in the CFP.

Process flow

BCB polymer with relatively low loss tangent and low dielectric constant is suitable as a substrate for the antenna fabrication. This polymer (BCB) acts as a barrier between the embedded lossy silicon chip and the connected antenna. However, BCB cannot be used as a single polymer in the CFP technology due to the stiff nature of it after curing. Therefore, the combination of the BCB polymer with the durimide as a reinforcing polymer needs to be used. To remain flexible and bendable, the overall thickness of the integrated system should not exceed 100 µm. In addition, the material to fabricate the antenna can affect the efficiency and the directivity of the antenna. In this work, AlSiCu and Al are chosen to keep the technology CMOS fabrication compatible. Considering all the conditions, the final thickness of each layer from the bottom layer to the top antenna layer is summarized in table 5.4.

During the fabrication process, the surface of temporary silicon carrier is treated with TI PRIME as an adhesion lowering layer. Next, Si_3N_4 is deposited as a stress release layer. Afterwards, BCB and durimide are deposited and cured one after another. After defining the cavity, the RF chip is embedded by using BCB as an adhesive layer. Then, the chip's surface is covered by BCB with the thickness similar to the bottom polymers. Then, the vias on-chip are opened by using metal as a hard mask and plasma reactive

Table 5.4: Thickness of each layer from the bottom to the top in the dipole antenna integration and interconnection in the CFP technology.

Layer	Thickness (µm)
Bottom BCB	3.5
Durimide	10
BCB as an adhesive	3.5
Chip thickness	45
Top BCB	10-14
AlSiCu (Interconnection line + Antenna)	2-5

ion etching. Once the vias to the contact pads of the embedded chip are opened, an AlSiCu layer is sputtered and structured. As shown in the Fig 5.35, the RF chip is integrated and interconnected with the antenna with the carrier frequency at 5.5 GHz in the CFP technology.

Measurements

The fabricated antennas with the carrier frequency at 5.5 GHz on top of polymer foil are measured as a standalone system. For this purpose, each antenna is measured: (I) on the wafer, (II) after releasing, and (III) during the bent status with a different radius of curvature (R) (shown in Fig 5.36). The measurements are performed [9] using a vector network analyzer (VNA).

As shown in Fig 5.36, the antenna is measured during the straight and the bent status above the cylinders with the permittivity, such as air (ϵ_r). The reflection coefficient magnitude (S_{11}) is measured at Institut für Hochfrequenztechnik and is shown in Fig 5.37. The measurements are compared with the corresponding simulations. The simulations are done for the antenna on polymer foil without the silicon carrier underneath. Therefore, it is clear that the measurement after releasing from the silicon carrier and during the straight status is showing the better performance in comparing to the wafer level measurements.

The measured input reflection coefficient (S_{11}) is lower than the simulated value. One of the reasons is due to the bend in the transmission line implemented during measurements (see Fig 5.36. b). The 90 ° bend introduces bending loss, which reduced the measured reflection coefficient when compared to the simulated value with a straight transmission line. The shift in measured resonance frequency of the antenna is due to

[9]Measurements and characterizations are done by Miss Mahsa Rasteh at Institut für Hochfrequenztechnik (IHF).

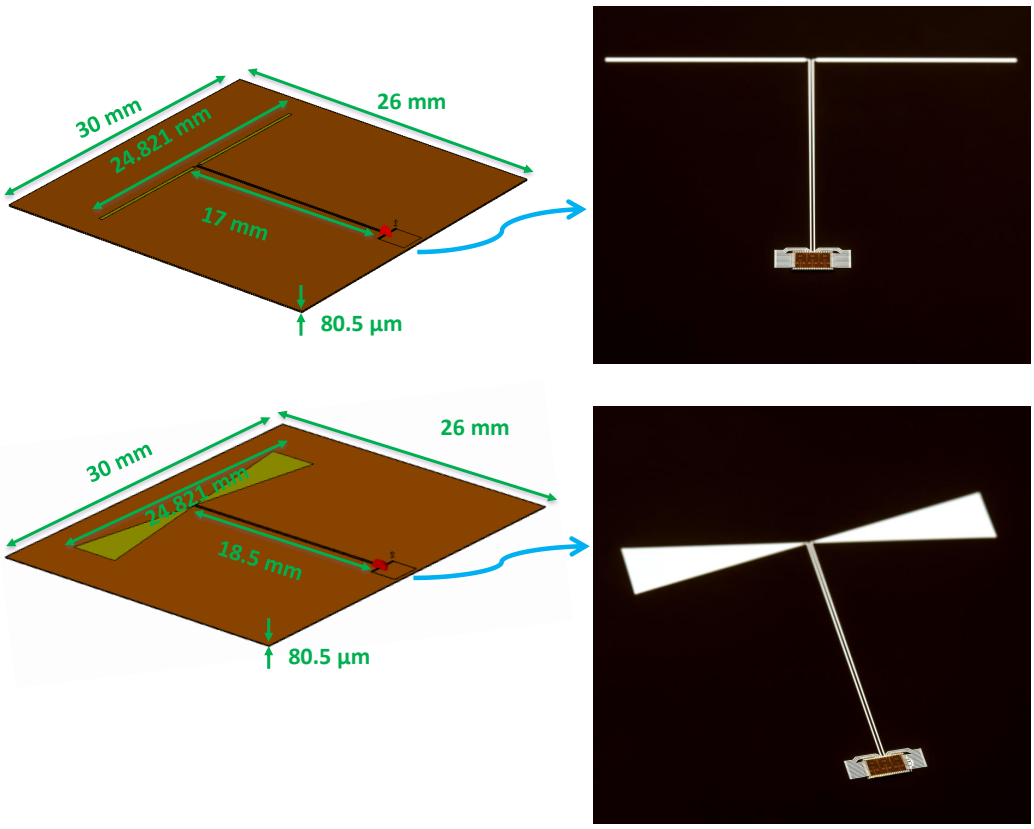


Figure 5.35: Simulation illustration and corresponding graphical view of the dipole antenna (top image) and the bowtie antenna (bottom image) which are fabricated on the CFP polymer foil.

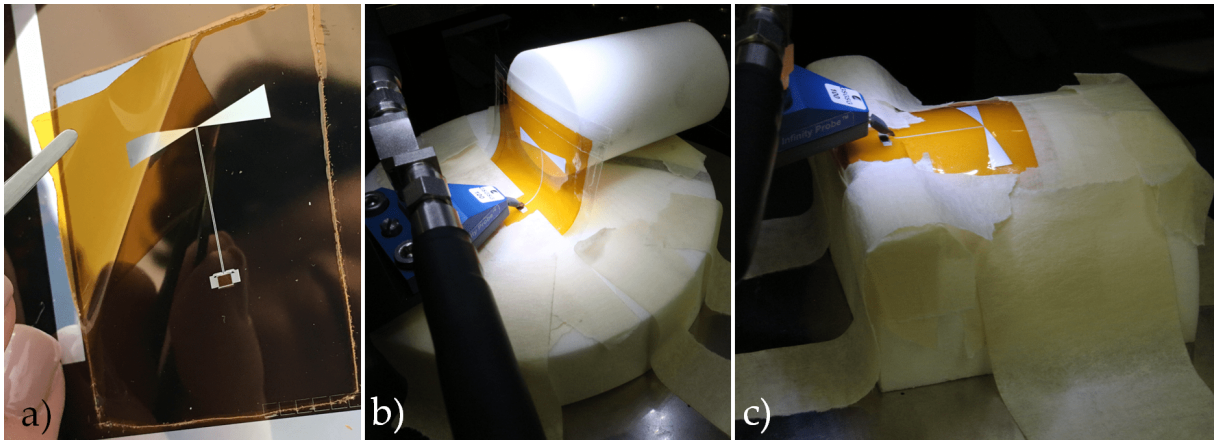


Figure 5.36: Graphical illustration of the bowtie antenna measurement on the polymer foil using VNA, a) releasing the antenna from the temporary silicon carrier, b) measurement as a straight bow tie, c) measurement during bent status.

uncertainty in material parameters (thickness and electrical properties) of the substrate and metal layers used in the simulation [153].

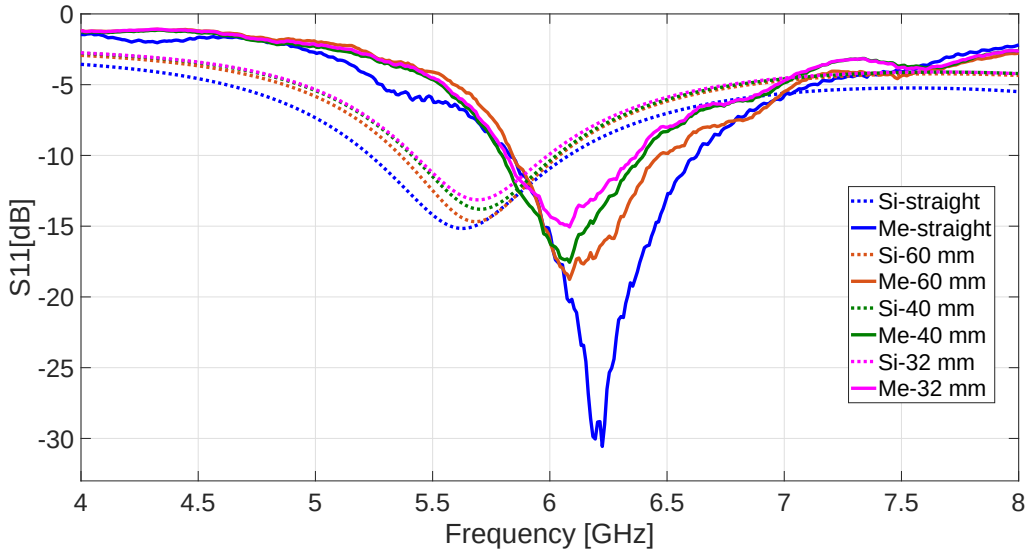


Figure 5.37: Measured S_{11} of the bowtie antenna. In this plot, "Me" and "Si" stand for the measurement and the simulation, respectively. The bowtie is measured for the various radius of the curvature [153].

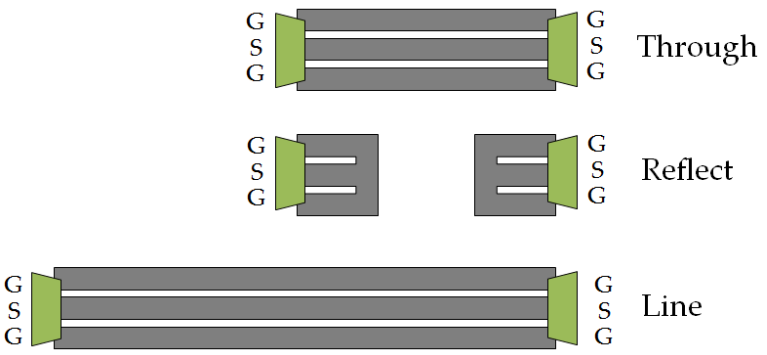
TLR calibration chip

To model the real behavior of the high-frequency antenna, the extrinsic parasitics of the measuring pads and input/output interconnections must be subtracted from the measurement results. This procedure is called de-embedding [168]. The Thru-Reflect-Line (TRL) calibration technique is an effective technique while using the Vector Network Analyzer (VNA) [169].

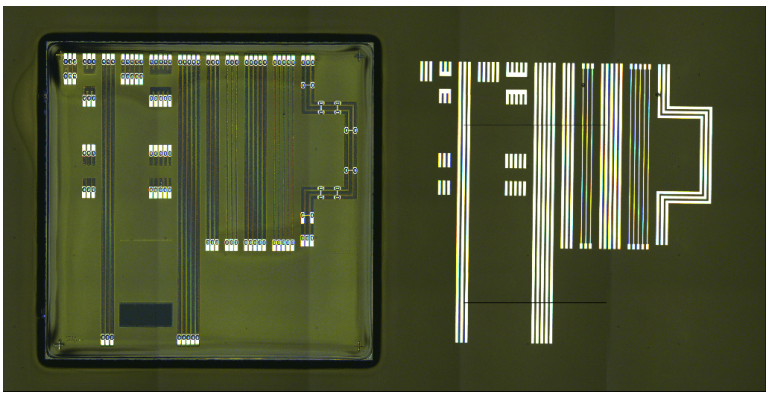
In order to characterize the transitions from the thinned foil-embedded chip to the transmission lines on the foil, an on-chip and on-foil calibration line structures for TRL-type RF calibration are designed, embedded, and characterized and allowed to de-embed the effects of the transition. The TLR calibration chip is designed based on the below definitions (Fig 5.38a). The test chip (Fig 5.38b) follows the same thickness of the top metal pad and the chip thickness as the final RF chip which is going to be integrated and interconnected with the antenna.

Through – connection of port 1 and port 2 with a short length of transmission line.

Reflect – short termination.



(a)



(b)

Figure 5.38: Based on the TLR calibration definition, the TLR test chips are designed, thinned, and embedded in the CFP, (a) Definition of TLR, (b) TRL calibration chip embedded in the CFP.

Line – connection of port 1 and port 2 with a long length of the transmission line (compared to Through).

The TLR test chips are designed, thinned (45 µm), and embedded in the CFP. The CFP process is done by following the same thickness and process flow which is going to be performed on the final and functional system. All the lithographic steps are performed after adopting the original layout with help of the adaptive layout technique. The measurement results of the embedded TLR chips in the CFP foil are plotted in Appendix C.

5.5 Summary

In this chapter, the Chip-Film Patch (CFP) technology or the system integrated into foil is characterized in four categories: (I) electrical characterization including reliability test, failure analysis, passive element fabrication on foil, and on-chip active device embedded inside CFP foil, (II) mechanical characterization including investigation and compensation of induced warpage during CFP process and after chip embedding inside polymer foil, (III) thermal characterization, measurement, and management of the thin high power chips which are embedded inside polymer foil and, (IV) RF characterization and process flow for the antenna fabrication on foil. Each of the characterizations can be helpful for related applications, such as a sensor, antenna, NFC, and chip integration inside or on polymer foil.

CHAPTER 6

APPLICATIONS

"I am enough of an artist to draw freely upon my imagination. Imagination is more important than knowledge. Knowledge is limited. Imagination encircles the world."

— Albert Einstein, Cosmic Religion and Other Opinions and Aphorisms

This chapter reports the demonstrated and proposed applications for the CFP technology. It is divided into three parts; complex system-in-foil (KoSiF), high-frequency applications (FFLexCom), and biomedical applications (Smart implant).

6.1 Complex System-in-Foil (KoSiF)

The KoSiF project's [170] main purpose is to explore, expand, and evaluate the available technologies to fulfill future demands in the field of a flexible and hybrid system-in-foil (HySiF). As shown in Fig 6.1, HySiF technology includes integration and interconnection of multiple ultra-thin chips in flexible polymer foil in combination with large-area electronics, such as OTFTs, printed sensors, and antennas. The KoSiF demonstration includes three flexible foils mounted on three adaptive grippers. In Fig 6.2[1], the illustration of the smart skin wireless adaptive gripper is shown which is part of the

[1]Illustration by Festo AG.

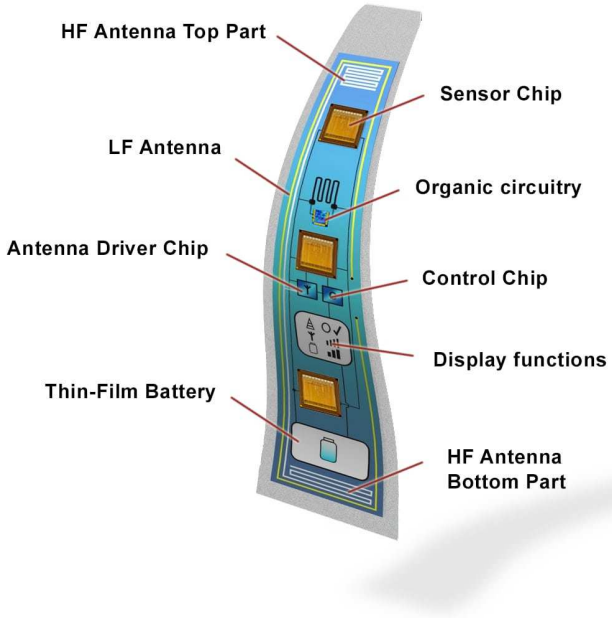


Figure 6.1: Graphic illustration of a HySiF in the KoSiF project [9].

KoSiF project. In this work, the challenges and possible solutions to fabricate "smart skin" system-in-foil on one of the adaptive gripper are explored. The smart skin is a two-dimensional stress sensing system which after fabrication is mounted on an adaptive gripper. The adaptive gripper systems allow the adaptive adjustment of the gripper to a different object according to their shapes which makes gripping and handling safe and damage-free [119], [171].

The smart skin is fabricated using the face-up two-polymer CFP technology using the adaptive layout technique. The hybrid system-in-foil includes two interconnected ultra-thin chips, two antennas, strain gauges, and OTFTs (see Fig 6.3). The completed system is then released as a foil and mounted on the adaptive gripper. The first generation of the smart skin system is connected to the external readout circuitry by wires. As illustrated in Fig 6.3, chip 1 is communicating with an antenna to transfer data from chip 2 (readout) to the outside world. The interconnection between two chips is achieved with the adaptive layout technique. Chip 2 reads the data from three strain gauges which act as stress sensors and sense the bending of the gripper. In addition, OTFTs work as switches to control the output signal from each strain gauge to the readout chip (chip 2). The challenges and corresponding solutions can be summarized as;

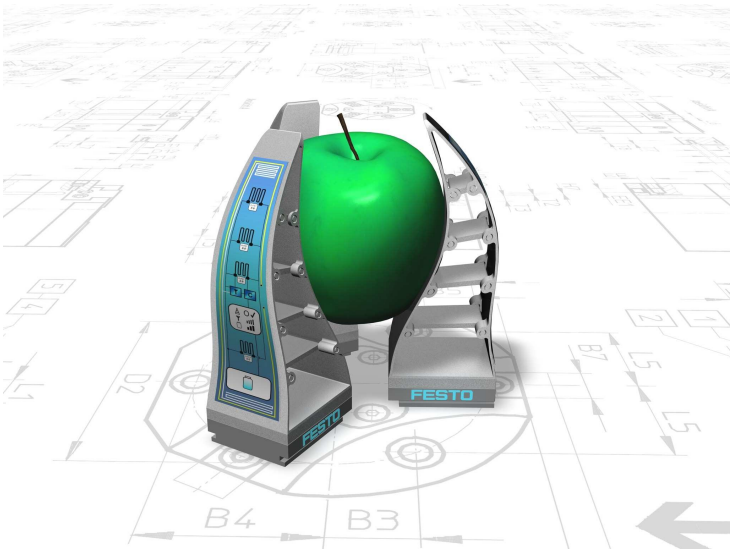


Figure 6.2: Schematic illustration of the wireless smart skin adaptive gripper [119].

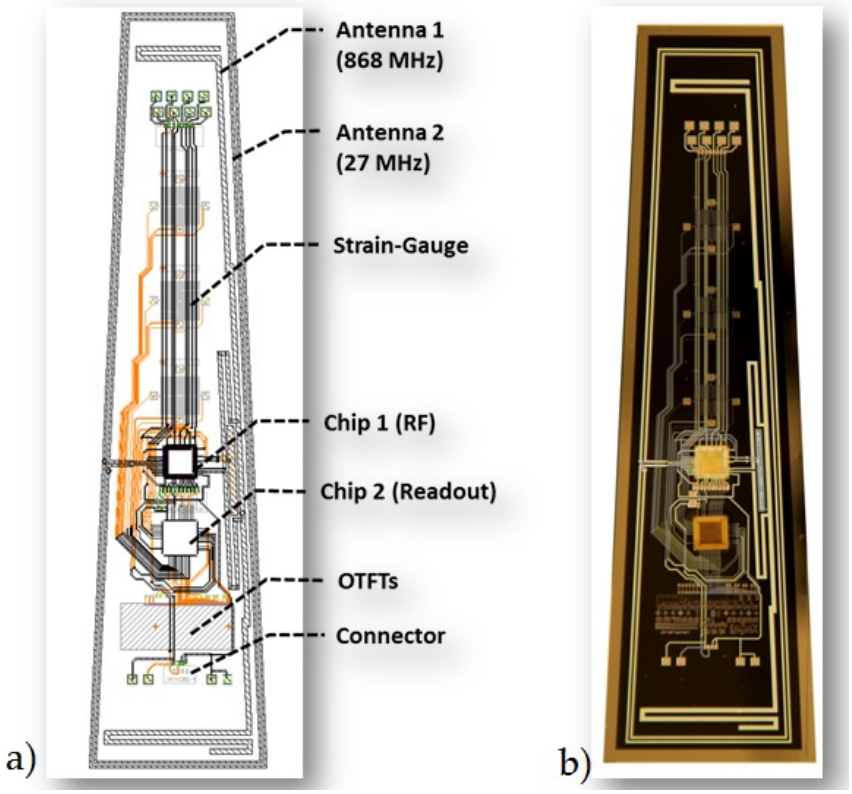


Figure 6.3: The KoSiF demonstration SmartInkSense, a) Layout including required modules, b) Ultra-thin chips integrated and interconnected in CFP foil in combination with OTFTs, strain gauges, and antenna.

- The organic TFTs are fabricated using high-resolution silicon stencil mask in the last step of the CFP technology. In this step, the silicon carrier should be planar to provide minimum resolution. ⇒ The solution is PECVD Si_3N_4 to induce stress on the silicon wafer to compensate unwanted warpage during the next steps of the CFP fabrication (described in 3.4.1) [125].
- The interconnection between two chips despite rotation and offset ⇒ The adaptive layout is proposed as a solution (described in Section 4.4).
- Two times metallization in-house process ⇒ First step metallization is AlSiCu and second step metallization is performed by Ti+Au.
- Interconnection from the top metal layer on the foil to external readout circuitry using a connector ⇒ The interconnection is performed by using silver glue.

The flow chart of the KoSiF CFP technology is shown in Fig 6.4. In Fig 6.4, the strain gauges are printed using the Aerosol Jet™ formula printing technique [172]. The wafer must be baked at temperatures of up to 180 °C to ensure sintering of the silver particles. These temperatures are not tolerable for the OTFTs, so the printing process must be done before the organic transistors are completed. In the final demonstration, the electrical functionality of the embedded and interconnected chip inside the CFP polymer foil is tested and proved.

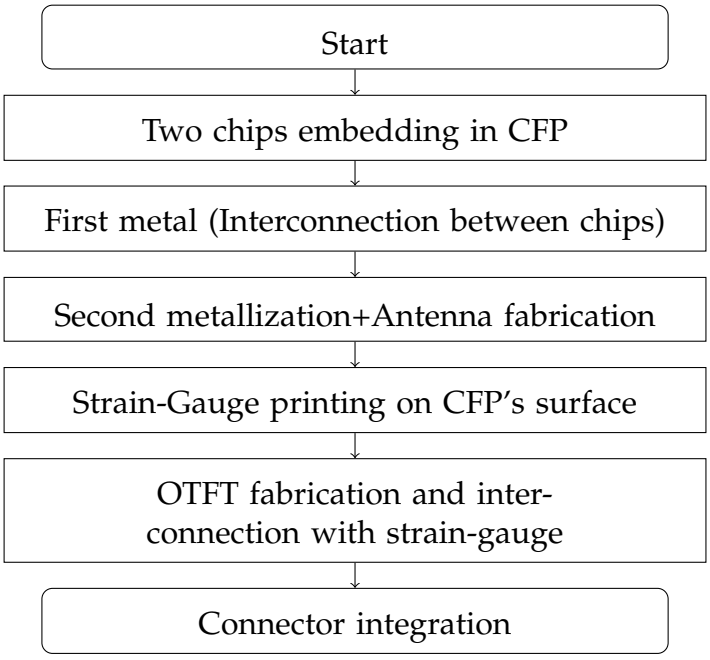


Figure 6.4: Flow chart of the KoSiF process flow.

6.2 High Frequency System-in-Foil

Radio-frequency identification (RFID) applications are countless. However, the combination of the specifications, such as long-range, high communication data-rates, lower power consumption, and flexibility of device is restricted. In this case, the Flexible and Adaptive Energy-Efficient High-Speed Wireless Hub (part of FFLexCom project) is a research project with the criterion of a "long-range, environment agnostic wireless reading range" which means that the device must be small, thin, and mechanically flexible in order to conform to arbitrary surfaces and to accommodate to mechanical cycling. It should also connect "wirelessly" in environments with various permittivities, such as textile fabric and animal/human skin or other body materials, such as bone or blood. The carrier frequency should be in GHz range. Therefore, the very fast and low-parasitic transistor is needed which is fabricated using silicon technology.

This project provides an application to integrate high power ultra-thin silicon chips in the CFP technology in combination with the fabricated high-frequency antenna on top of low-loss dielectric polymer foil. The conventional two-polymer face-up CFP technology needs to be optimized in order to meet the requirements. The schematic illustration of the FFLexCom is shown in Fig 6.5.

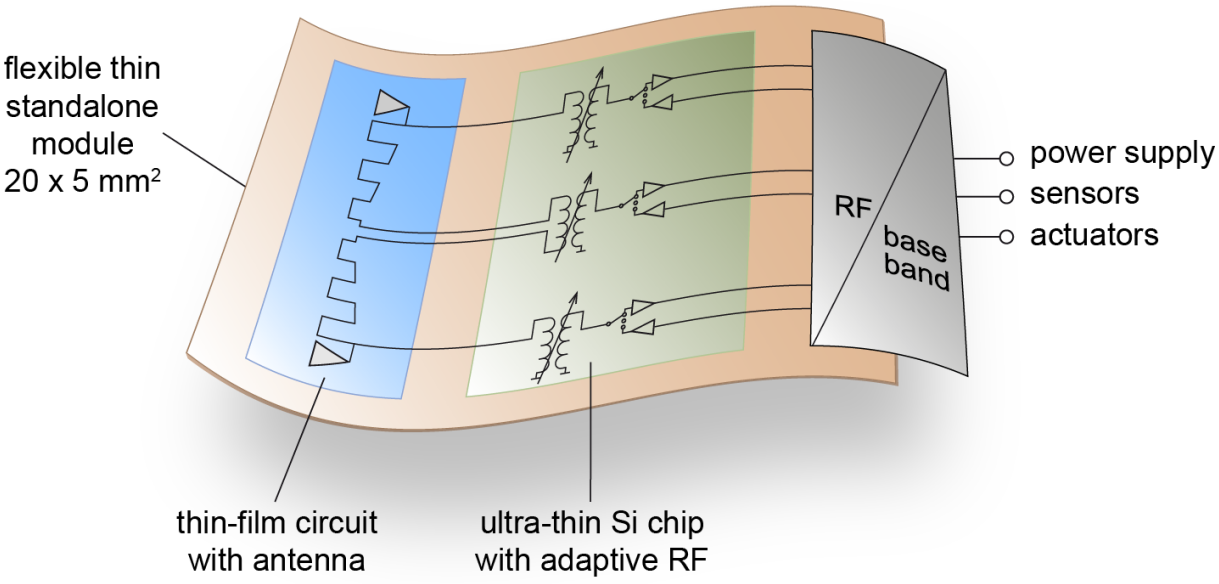


Figure 6.5: Schematic illustration of the FFLexCom project [153].

First, the high-speed silicon chips are fabricated by 0.25 µm BiCMOS (IHP process SGB25V) for energy efficient RF circuits operating at up to 6 GHz. Single chip back

thinning and DC characteristic measurements of CMOS and HBTs before and after thinning are performed and the low difference is observed (described in subsection 5.1.4). From earlier works, the initial chip thickness down to 20 µm was intended. However, in practice, the minimum chip thickness down to 35 µm ± 10 % is achieved. This difference is due to internal stress on the chip which is caused by a number of metallizations, and chip layout. Therefore, the process flow is adapted to the accomplished chip thickness.

Second, ultra-thin chips embedded in foil are prone to self-heating inside low-thermal conductive thermal foil. Therefore, the leakage current rises and overall reliability decreases. As a first solution, the power optimization at the circuit level is performed. Then, the thermal behavior of the chip inside the polymer is investigated. In addition, the process flow to fabricate a heat spreader at the back side of the chip is developed. Besides the heat spreader, the idea of sub-structuring the thin chip as a physical barrier is developed and the concept is practically performed (described in subsection 3.4.5).

Third, the process flow of dipole antenna fabrication (GHz range) on top of the polymer foil is developed and further optimized. In this case, the CFP technology is adapted to use the low-loss tangent material. This polymer acts as a barrier between the embedded lossy silicon chip and the interconnected antenna (described in subsection 5.4.3).

As shown in Fig 6.6, as a demonstration for the FFLexCom project, a thin amplifier chip is connected to a flexible antenna and both are embedded into a thin CFP polymer foil, showing mechanical flexibility (bending) and signal transmission at frequency of 5.5 GHz.

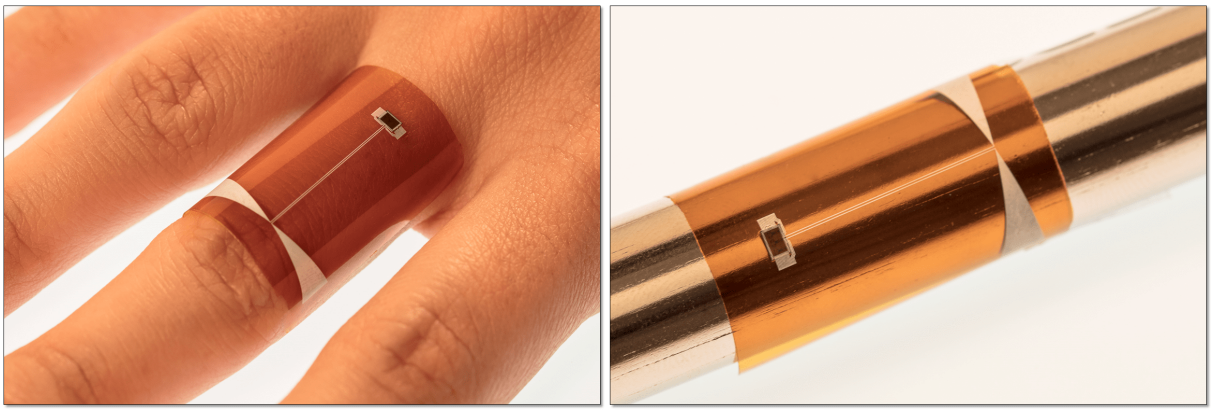


Figure 6.6: Thin, flexible amplifier integrated circuit operating at 5.5 GHz, embedded in a flexible foil and connected to a broadband dipole antenna.

6.3 Flexible Electronics for Biomedical Engineering

The development and integration of flexible biocompatible electronics can make a huge difference in the biomedical community. Recent developments in material science and microfabrication technologies enable the system-in-foil capable of integrating with soft tissues, curvilinear, and dynamic surfaces [173], [174]. Temperature sensors, strain sensors, pressure sensors, pH sensors, glucose sensors are a group of examples for biomedical applications and track of symptoms in various organs and tissues.

In this case, the SMARTImplant project is developed in vivo biosensor applications. The measurements include on-chip temperature measurement and electrodes that measure O_2, pH. The ultra-thin chips are embedded face-up in two-polymer CFP technology and electrodes are fabricated on polymer foil and contacted with chip [175]. However, the integrated polymers in two-polymer CFP technology are not biocompatible. On the other side, the low-stress CFP technology is biocompatible but is not allowed in the vivo biosensors or applications. Two examples of the system-in-foil for biomedical purposes are shown in Fig 6.7.

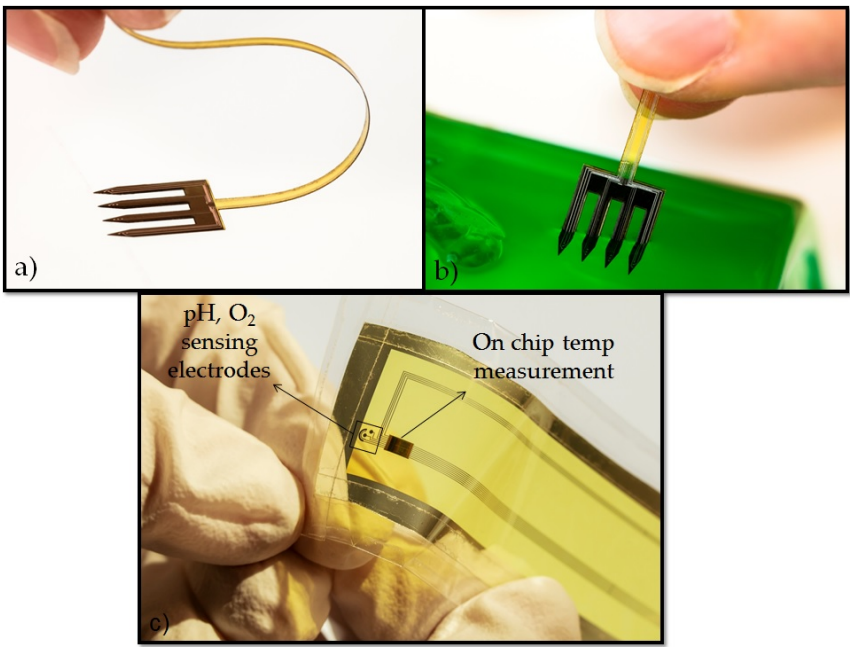


Figure 6.7: Demonstration of the CFP technology for a biomedical application, a) Bendable and flexible micro-needle embedded in polymer foil, b) The silicon micro-needle can act as an injecting needle in a drug delivery application. In this demonstration, pudding's surface acts as body tissue. c) The SMARTImplant demonstration includes embedded chip and on foil sensing electrodes [175].

Chapter 7

General Conclusions and Outlook

> "Begin at the beginning", the King said gravely, "and go on till you come to the end: then stop."
>
> — Lewis Carroll, Alice in Wonderland

In this final chapter, several conclusions of this thesis are depicted. Together with project partners IMS CHIPS, IHF, INT, and MPI, ultra-thin chip embedding and interconnection inside the Chip-Film Patch technology in combination with on foil fabricated sensors, antennas, and OTFTs are presented. This work is performed to develop a new technology to embed multiple chips inside a polymer foil in combination with other modulars towards an intelligent system fabrication.

Chip-Film Patch Technology – The CMOS fabrication compatible Chip-Film Patch (CFP) based on face-up or face-down chip embedding and integration in polymer foil is developed and optimized. The superior features of the CFP technology in comparison with other available technologies are fine-pad pitches, fine-pad sizes, bendability, and an IC process line compatibility. The CFP technology is developed into categories: two-polymer CFP technology and low-stress CFP technology. The two-polymer CFP is mainly optimized for the fabrication and integration of RF-components in or on polymer foil. In addition, the two-polymer CFP technology is chosen to fabricate passive elements and various sensors, such as humidity sensors. Moreover, the process flow of the low-stress CFP technology is developed and optimized by using low CTE polymer materials. In this technology, the deposited polymer layers have close CTE to the embedding ultra-silicon chip to avoid a CTE mismatch and unwanted thermomechanical stress on top of the embedded chip and, therefore, assure longer lifetime reliability. Furthermore, the face-down concept based on low-stress CFP technology is presented

and the related process flow is developed. Finer-pitch pad interconnectivity by leveling the chip and the foil surface, embedding components with various thicknesses as a micro-hybrid system, and chip backside processing after embedding inside foil, such as heat spreader fabrication and back-thinning are the groups of the manifest properties of the face-down CFP technology.

Adaptive Layout Technique – In this work, the CFP technology is extended to embed and interconnect of more than one ultra-thin chip-in-foil. However, while the chip is embedded, an unwanted movement of each chip during the embedding and curing step causes an undefined offset for each chip. This misalignment and rotation error has detrimental consequences in the metal interconnection steps between the embedded chips. Therefore, as a solution, the wafer level adaptive layout technique using a maskless laser writer lithography tool is proposed and developed. After the proof of concept and during the optimization level, the overlay accuracy of the adaptive layout technique is extracted using a designed test chip. Furthermore, the parameters which are involved in the overlay error are found and based on the proposed solutions, the best possible accuracy is achieved. Moreover, the OTFTs and ring oscillator are fabricated and characterized in the two-polymer CFP technology and the final demonstration including silicon chips, strain gauges, and OTFTs with the help of adaptive layout technique is presented.

Electrical Characterization – The electrical interconnection between embedded and interconnected multiple test chips face-up in the two-polymer CFP technology using the adaptive layout technique, is tested and verified. In addition, the reliability test on the two-polymer CFP technology including three conditions, i. e. bending test, thermal ageing test, and thermal and humidity storage are performed and electrically verified. Based on the measurements, the corresponding failure analysis is pursued and the solutions are provided. Also, the passive components, such as the capacitor and the inductors are fabricated based on two-polymer CFP technology and characterized to be used in further applications, such as NFC and humidity sensor fabrication on polymer foil. Furthermore, the RF chips including bipolar and CMOS transistors are electrically characterized from the first step of the silicon chip back grinding until the embedding inside polymer foil is completed. All the embedded chips inside the CFP polymer foil are functional and show a low degradation in comparison to the bulk equivalent RF chip.

Thermal Characterization – To investigate the effect of embedding an ultra-thin power chip into low thermal conductive polymer, on-chip thermal sensors are designed to measure the behavior of the thermal source on the same chip. The thermal behavior of each temperature sensor for five conditions, namely thick chip, thinned chip, the thinned chip embedded on foil, the thinned chip embedded inside CFP foil, and the thinned chip embedded inside CFP foil with a heat spreader on the backside of the chip, are measured. The measurements confirm the already published thermal

research regarding lateral thermal resistance reduction after the chip thinning. In addition, the effect of self-heating on the chip after embedding on/in polymer foil due to the poor thermal conductivity of the polymer substrate is proven. The process flow of fabricating heat spreaders on the chip backside as a cooling method is developed and illustrated in this work. In addition, the process flow for sub-structuring of the thin chip after embedding into polymer foil is developed and the results are presented. This method is proposed as another thermal cooling concept in which sub-structuring of the chip creates a thermal barrier and separates the thermal source of the chip from other parts.

RF Components Fabrication and Characterization – The process flow to fabricate BCB silicon-based millimeter wave antennas is developed and after optimization, a reproductive yield of up to 80 %-85 % in functional devices per wafer is achieved. Besides all the RF measurements, the characterization of dielectric materials and conductivity of interconnection lines are measured and compared with the simulations. The measurements are in close agreement with literature. In addition, the process flow to fabricate a dipole antenna (5.5 GHz) and interconnect it with a RF chip using the face-up two-polymer CFP technology and adaptive layout technique is proposed. The two-polymer CFP polymer stacks are optimized in the way that BCB polymer with low loss tangent acts as a barrier between an embedded lossy silicon chip and a fabricated dipole antenna on foil.

Outlook – Although in this work the required tasks, challenges, and restrictions are solved and optimized, there are still open questions regarding the manufacture which need to be answered and modified. The face-down concept using lamination foil is proved. However, the process should be optimized towards reproducibility. In addition, the face-down technique using the laser excimer transfer is a promising technology that should be considered in the future. For the time being, the reliability tests for the face-up two-polymer CFP technology are performed. However, the other proposed technology, namely low-stress CFP technology should undergo similar and detailed reliability tests.

One of the interesting and challenging topics is the micro-hybrid integration and interconnection of high power devices with silicon chips in polymer foil. Self-heating, parasitic, and non-equal thickness of the elements are challenges which we face. Furthermore, the chip array fine placement and interconnection, diverse sensors fabrication (ex: pressure sensor, temperature sensor) on foil, and improving antenna fabrication on foil can lead the available technology towards IoT future demands. In addition, moving from wafer level packaging towards panel level packaging can increase the throughput and reduce the costs.

Appendix A

Code Listing

In this appendix, *Perl* codes of the adaptive layout script are listed. With this script, the originally designed layout to interconnect chips will be adopted into a new interconnection layout including the calculated offset, rotation, measured coordinates, and center of rotation for each individual chip [1].

```
# transforms layout for Chip-Film Patch

use strict;
use constant CIF  => 1000; # CIF units
use constant GRID => 10;
use constant SEP1 => ","; # separator in coordinate pairs

my $program="trans.pla";
my $version="a1.2";
my $usage= $program." cif-datei chip-datei";
my $ARGVL = @ARGV;
if ($ARGVL <2 ) {  die "\nusage: $usage \n"; }

# open Files
   my $infile=$ARGV[0];
   open IF , "<".$infile or die "cannot open $infile for read\n" ;

   my $outfile=$infile;
   $outfile =~ s/.cif/-t.cif/;
   open OF, ">".$outfile or die "cannot open $outfile for write\n" ;
   my $root = $infile;
   $root =~ s/.cif//;

   my $chipfile=$ARGV[1];
   open CH, "<".$chipfile or die "cannot open $chipfile for read\n" ;

   my $cntchip =0;
```

[1] This code is written with great support of Dr. Harald Richter at IMS CHIPS.

```
28    my @chips;
29    my @xl;my @xr;my @yb;my @yt;my @dx;my @dy;my @alf; my @sca;
30
31    printf ("================================\n" );
32    printf ("%-s vers. %-s \n",$program, $version );
33    printf ("using : %-s / %-s \n",$infile, $chipfile );
34    printf ("output: %-s \n",$outfile );
35    printf ("================================\n" );
36
37 # work on .chips file
38    while (my $line = <CH> ) {
39
40   chomp $line;
41   @chips = split "[, ]", $line;
42   if ($#chips != 7 ) {
43       printf ("Chip %d : number of parameters/ format not correct: %d\n",
      $cntchip , $#chips +1 );
44       print $line;
45       exit;
46   }
47
48   printf ("Chip %d :",$cntchip );
49   for ( my $i=0; $i<= $#chips ; $i++ ) {
50       printf ("%10.4f  ",$chips[$i]) ; }
51         printf ("\n" );
52
53   $xl[$cntchip]=($chips[0] < $chips[2] ? $chips[0] : $chips[2])*CIF;
54   $xr[$cntchip]=($chips[0] > $chips[2] ? $chips[0] : $chips[2])*CIF;
55   $yb[$cntchip]=($chips[1] < $chips[3] ? $chips[1] : $chips[3])*CIF;
56   $yt[$cntchip]=($chips[1] > $chips[3] ? $chips[1] : $chips[3])*CIF;
57   $dx[$cntchip]=$chips[4]*CIF;
58   $dy[$cntchip]=$chips[5]*CIF;
59   $alf[$cntchip]=$chips[6];
60   $sca[$cntchip]=$chips[7];
61 # printf ("read transform:%8d %8d %8d %4f",$dx[$cntchip]/CIF,$dy[$cntchip]/
     CIF,$alf[$cntchip], %4f $sca[$cntchip]);
62   $cntchip++;
63    }
64    close CH;
65    printf ("================================\n" );
66
67    my $cntbox=0;
68    my $cntpol=0;
69    my $cntwir=0;
70    my $cntins=0;
71
72 # work on cif input file
73    while (my $line = <IF> ) {
74   my @fields = split "[, ]", $line;
```

```
75    $line =~ s/$root/$root-t/;
76
77  #       print $fields[0].":".$#fields.":".$line;
78
79  # Wire and Polygon
80    if ( $fields[0] eq "W" || $fields[0] eq "P" ) {
81  #           print $fields[0].":".$#fields.":".$line;
82        chomp $fields[$#fields];
83  #     print $fields[$#fields].":\n";
84        $fields[$#fields] =~ s/;.//;
85  #     print $fields[$#fields].":\n";
86
87  #     for ( my $i=2; $i<= $#fields ; $i++ ) {
88  #    print $fields[$i]."  ";
89  #     }
90  #     print "\n";
91
92        my $offset = ($fields[0] eq "W") ? 2 : 1;
93        if ($fields[0] eq "W") { $cntwir++; } else {$cntpol++; };
94
95        for ( my $i=$offset; $i<= $#fields ; $i=$i+2 ) {
96      my $in = is_in_chip ($fields[$i],$fields[$i+1] );
97  #    print $fields[$i].",".$fields[$i+1].":in:".$in."\n";
98      if ($in > -1 ) {
99  #       print $fields[$i].",".$fields[$i+1].":in:".$in."\n";
100       (my $xn,my $yn) = transf ( $fields[$i],$fields[$i+1],$in);
101 #       print $xn.",".$yn."\n";
102       my $str1=$fields[$i].",".$fields[$i+1];
103       my $str2=$xn.SEP1.$yn;
104       $line =~ s/$str1/$str2/;
105     }
106       }
107   }
108
109 # Boxes
110   if ( $fields[0] eq "B" ) {  # convert Box to Poly
111      my @box = split "[, ]", $line;
112      chomp $box[$#box];
113      $box[$#box] =~ s/;//;
114 # calculate box corners
115      $fields[2]=$box[3]-$box[1]/2; $fields[3]=$box[4]-$box[2]/2;
116      $fields[4]=$box[3]-$box[1]/2; $fields[5]=$box[4]+$box[2]/2;
117      $fields[6]=$box[3]+$box[1]/2; $fields[7]=$box[4]+$box[2]/2;
118      $fields[8]=$box[3]+$box[1]/2; $fields[9]=$box[4]-$box[2]/2;
119      $cntbox++;
120
121      my $needtr=0;
122      for ( my $i=2; $i<= $#fields ; $i=$i+2 ) {
123     my $in = is_in_chip ($fields[$i],$fields[$i+1] );
```

```
124     if ($in > -1 ) {
125 #       print $fields[$i].",".$fields[$i+1].":in:".$in."\n";
126         (my $xn,my $yn) = transf ( $fields[$i],$fields[$i+1],$in);
127 #       print $xn.",".$yn."\n";
128         $fields[$i]=$xn; $fields[$i+1]=$yn;
129         $needtr=1;
130     }
131      }
132 # if transformation is needed, convert to Polygon
133      if ($needtr ) {
134     $line = "P";
135       for ( my $i=2; $i<= $#fields ; $i=$i+2 ) {
136        $line=$line." ".$fields[$i].",".$fields[$i+1]; }
137     $line = $line.";\n";
138      }
139   }
140
141 # instance calls
142   if ( $fields[0] eq "C" ) {
143      print "Instances not implemented yet\n";
144   }
145   print OF $line;
146    }
147    close IF;
148    close OF;
149
150    printf ("done processing %d boxes, %d polygons, %d wires(pathes), %d
       instances \n",$cntbox,$cntpol,$cntwir,$cntins);
151    printf ("================================\n" );
152
153    exit ;
154 # End main program
155
156 #=========================================================================
157 # is_in_chip: tests whether point $x,$y is in one of the chip boundaries
158 # return chip number, -1 if non is found
159    sub is_in_chip {
160   my $x =$_[0];
161   my $y =$_[1];
162   my $in=-1;
163
164   for ( my $j= 0; $j< $cntchip ; $j++ ) {
165 #     print $j.":".$xl[$j].",".$xr[$j].",".$yb[$j].",".$yt[$j]."\n";
166       if ( $x >= $xl[$j] && $x <= $xr[$j] && $y >= $yb[$j] && $y <= $yt[$j]
       ) { $in = $j; last; }
167   }
168   return $in;
169   };
170
```

```
#=========================================================================
# transf: transforms point $x,$y with repect to chip $in misallignment
# return new coordinates (grid to grid)
   sub transf {
  my $x =$_[0];
  my $y =$_[1];
  my $in=$_[2];

# print $x.":".$y.":".$in."\n";
# return ($x+$dx[$in],$y+$dy[$in]);

  my $xOchip= $x-$xl[$in];
  my $yOchip= $y-$yb[$in];
  my $sina  = sin($alf[$in]/180*3.14159);
  my $cosa  = cos($alf[$in]/180*3.14159);
  my $xn    = $xOchip*$cosa*$sca[$in] - $yOchip*$sina*$sca[$in] + $xl[$in]
    + $dx[$in];
  my $yn    = $xOchip*$sina*$sca[$in] + $yOchip*$cosa*$sca[$in] + $yb[$in]
    + $dy[$in];
   return (GRID * int ($xn/GRID),GRID * int ($yn/GRID) );

# print $x+$dx[$in].":".$y+$dy[$in]."\n";
  };
#=========================================================================
```

As described in Section 4.4, the coordinates of each chip after embedding it in polymer foil, is measured using the laser direct writer. To calculate offset and rotation of each chip, two methods can be followed namely, direct coordinate measurements using the laser writer and script generation, or manual coordinates measurements and further data calculations. With the full automatic adaptive layout, the coordinates of the determined alignment marks on each embedded chip inside the foil will be detected and data will be stored in the text format by the laser writer. However, a fully automatic technique is feasible for the chips which stay in the defined window of the laser writer, i.e. for the chips with low rotation and offset. Following automatic or semi-automatic coordinate measurements in the laser writer, calculating the corresponding offset, rotation, scaling factor, and communication with the above *Perl* script is done by compiling the below codes[2].

```
##########################################
# watch out!
# the program will stop working if
# the user types in something
# different from an integer number two
# times in a row
##########################################

```

[2]This code is written in collaboration with Mr. Jan Kerner.

```
import subprocess
import math
import sys

if(len(sys.argv)==2):

  f=open("chip.chips", "w")

  try:
    numChips = input("Insert the amount of chips: ")
  except:
    print "Please try again (you have to insert an integer!)"
    numChips = input("Insert the amount of chips: ")


  i=1
  eingabe='n'


  while i<=numChips:

    if(len(sys.argv)!=2):
      print "coordinate.py usage: coordinates.py cif-file"
      break

    while eingabe=='n':
########usereinput#####################
      print ("\n\nChip Nr."+str(i)+"\n")
      print ("BEFORE POSITION MEASUREMENTS: ")

      try:
        x1 = input("\ninsert x1 : ")
      except:
        print "Please try again (you have to insert an integer!)"
        x1 = input("\ninsert x1 : ")
      try:
        y1 = input("insert y1 : ")
      except:
        print "Please try again (you have to insert an integer!)"
        y1 = input("\ninsert y1 : ")
      try:
        x2 = input("insert x2 : ")
      except:
        print "Please try again (you have to insert an integer!)"
        x2 = input("\ninsert x2 : ")
      try:
        y2 = input("insert y2 : ")
      except:
        print "Please try again (you have to insert an integer!)"
```

```
58          y2 = input("\ninsert y2 : ")
59
60        print ("\nCENTER OF ROTATION")
61        print ("\ndown left: \n")
62
63        try:
64          xc = input("insert x-coordinate: ")
65        except:
66          print "Please try again (you have to insert an integer!)"
67          xc = input("\ninsert xc : ")
68        try:
69          yc = input("insert y-coordinate: ")
70        except:
71          print "Please try again (you have to insert an integer!)"
72          yc = input("\ninsert yc : ")
73
74        print ("\nupper right\n")
75        try:
76          x2c = input("insert x-coordinate: ")
77        except:
78          print "Please try again (you have to insert an integer!)"
79          x2c = input("\ninsert x2c : ")
80        try:
81          y2c = input("insert y-coordinate: ")
82        except:
83          print "Please try again (you have to insert an integer!)"
84          y2c = input("\ninsert y2c : ")
85
86        print ("\nAFTER POSITION MEASUREMENTS: \n")
87
88        try:
89          x1new = input("insert x1 : ")
90        except:
91          print "Please try again (you have to insert an integer!)"
92          x1new = input("\ninsert x1 : ")
93        try:
94          y1new = input("insert y1 : ")
95        except:
96          print "Please try again (you have to insert an integer!)"
97          y1new = input("\ninsert y1 : ")
98        try:
99          x2new = input("insert x2 : ")
100       except:
101         print "Please try again (you have to insert an integer!)"
102         x2new = input("\ninsert x2 : ")
103       try:
104         y2new = input("insert y2 : ")
105       except:
106         print "Please try again (you have to insert an integer!)"
```

```
107         y2new = input("\ninsert y2 : ")
108
109       eingabe = raw_input("\nInputs correct? <y/n>")
110
111
112 ####do the math#3######################
113     x1_x2 = x1 - x2
114     x1_x2new =  x1new - x2new
115     y1_y2 = y1 - y2
116     y1_y2new = y1new - y2new
117
118     if(x1_x2 == 0 or x1_x2new ==0 or y1_y2 == 0 or y1_y2new ==0):
119
120       print ("\n\nDIVIDED BY 0\n\n")
121       break
122
123     else:
124
125       scale = (math.sqrt(y1_y2new * y1_y2new + x1_x2new * x1_x2new)) / (
    math.sqrt(x1_x2 * x1_x2 + y1_y2 * y1_y2))
126       alpha = (math.atan(float(y1_y2new) / float(x1_x2new))) - (math.atan(
    float(y1_y2) / float(x1_x2)))
127       A = scale * math.cos(alpha)
128       B = scale * math.sin(alpha)
129       xoffalt = x1new - A * x1 + B * y1
130       yoffalt = y1new - B * x1 - A * y1
131       alpha_deg = (alpha/math.pi)*180
132       xoff = xoffalt - xc * (1 - A) - yc * B
133       yoff = yoffalt - yc * (1 - A) + xc * B
134
135       if(i<numChips):
136
137         f.write("%.2f,%.2f,%.2f,%.2f,%.4f,%.4f,%.6f,%.9f\n" % (xc, yc, x2c,
     y2c, xoff, yoff, alpha_deg, scale))
138
139       else:
140
141         f.write("%.2f,%.2f,%.2f,%.2f,%.4f,%.4f,%.6f,%.9f" % (xc, yc, x2c,
    y2c, xoff, yoff, alpha_deg, scale))
142
143     eingabe='n'
144     i=i+1
145
146   f.close()
147
148   subprocess.call(['trans.pl',sys.argv[1],"chip.chips"])
149
150
151
```

```
152 else:
153   print "usage of coordinates.py: cif-file"
```

APPENDIX B

CHIP THINNING AND CHARACTERIZATION

B.1 Bipolar Transistors

In this section the impact of silicon chip back-thinning in the SiGe heterojunction bipolar transistors (HBTs) is determined. We studied the collector (I_C) and base currents (I_B) regarding the emitter-base voltage while the collector and the base are at the same reference potential. During the measurement step, the sensibility of the HBTs to the light needs to be taken into the account. The following study is focused on the forward mode characteristic of the silicon bipolar chip before thinning and after back-thinning (45 µm) and embedding on polymer foil using the 3 µm BCB adhesive layer. Fig B.1 shows the evolution of the base and collector currents which are shown in the Gummel plot. In these graphs, the base current for the thinned and embedded chip on polymer foil show a moderated increase at the low current level. Therefore, the corresponding current gain decreases. Similar behavior and variations can be observed in the work of other groups [140]. The measurements are repeated for two more samples while the same degradation is observed for all of them. However, the exact dependence of the base current change through specific handling, thinning, and embedding cannot be identified. But one assumption to determine the gain reduction of the bipolar silicon chips after thinning is the change of the interface state density on top of the thin oxide layer which is caused by the induced stress during the thinning or handling process.

B.2 MOS Transistors

The test is done on chips with a final thickness of 45 µm and various gate Width/Length ratios. The purpose is to evaluate the impact of the back-thinning on DC output characteristics of the CMOS devices. Therefore, the current curve $I_D(V_{DS})$ with sweeping V_{GS} in on and off state is measured. In MOS transistor measurements, the ambient temper-

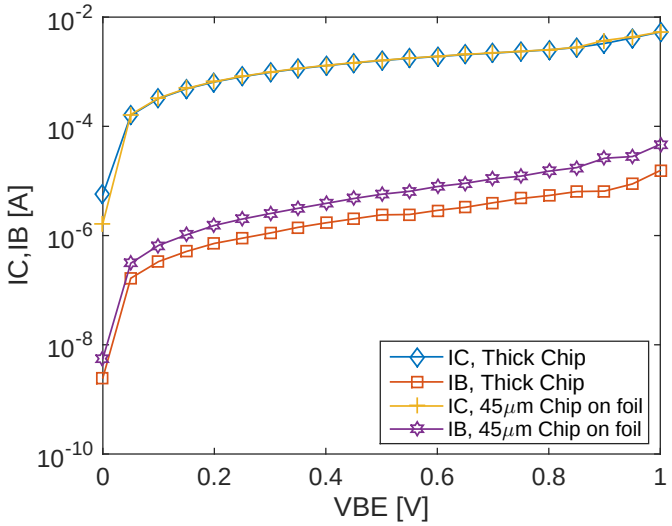


Figure B.1: SiGe HBT Gummel plot. Collector and base current, I_C and I_B, as a function of the emitter-base voltage (V_{BE}).

ature plays an important role. Therefore, the ambient temperature in which the silicon chips are measured is controlled using Pt100 close to the chip on the same chuck. The results for output characteristics of the NMOS device with a channel Width/Length ratio of (10 µm/0.3 µm) in an ON and OFF state are shown in Fig B.2 and Fig B.3, respectively.

The increase of the gate leakage in an OFF state can be interpreted as the result of the induced stress by the mechanical strain of back-thinning on the silicon chip [140]. Such a leakage current variation does not affect the functionality of the device. However, when gate leakage rises it can lead to an increase in power consumption in the OFF state for low-power CMOS devices. The subthreshold current which belongs to the exponential part is not affected by thinning. This is important regarding the reliability and functionality of the CMOS chip after back-thinning. However, the subthreshold current is reduced after chip thinning and embedding on foil by using BCB as an adhesive layer. In addition to thermomechanical induced stress, the current reduction can be caused due to the low thermal conductivity of the below BCB in comparison to the thermal conductivity of the measurement chuck. The vertical thermal conduction of the thinned silicon chip is lower than the similarly thick silicon chip. In addition to that, the embedded thin chip on foil may be exposed to self-heating due to the low conductivity of the below substrate. Therefore, the power dissipation is lower, causing an increase in temperature in the active layer in comparison to the non-thinned and thinned device on the measurement chuck.

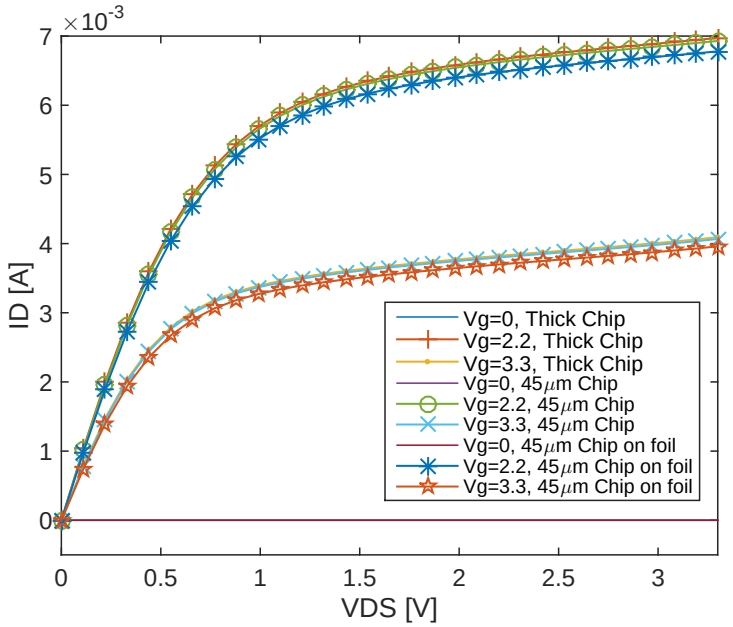


Figure B.2: Output characteristics $I_D(V_{DS})$ of NMOS device which is thinned down to 45µm (10 µm/0.3 µm)

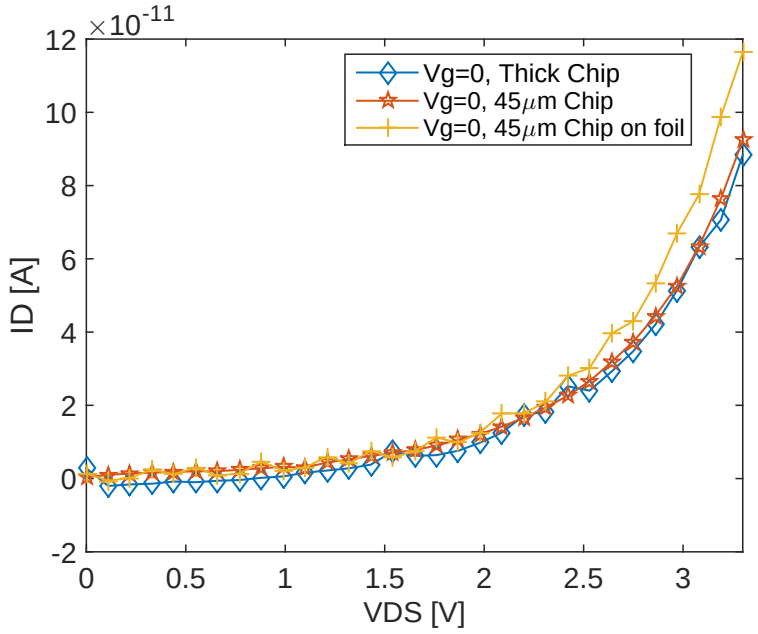


Figure B.3: Output characteristics $I_D(V_{DS})$ of NMOS device in off-state which is thinned down to 45µm (10 µm/0.3 µm)

Appendix C

TLR Calibration Chip

TLR S-parameter extraction for the TLR chip embedded in polymer foil are measured at Institut für Hochfrequenztechnik (IHF) and plotted in the below graphs.

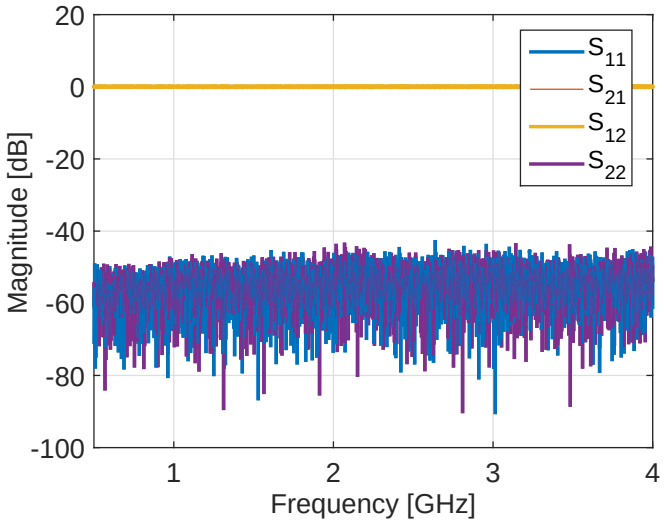


Figure C.1: S-parameters of through. S_{11}= S_{22}= reflection and S_{12}= $S_{21} \simeq$ 0dB= transmission.

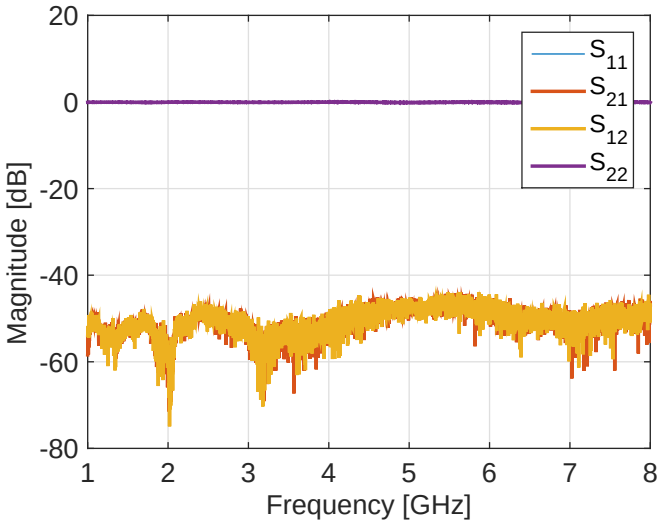


Figure C.2: S-parameters of reflection. S_{11}= S_{22} $\simeq$ 0 dB= reflection and S_{12}= S_{21}= transmission.

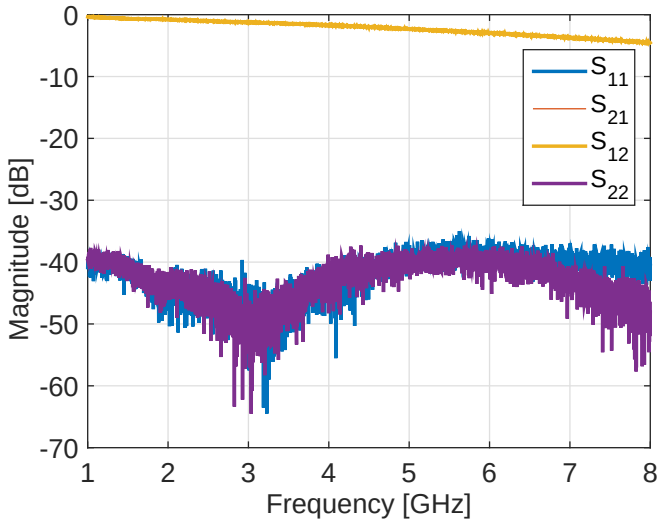


Figure C.3: S-parameters of line. S_{11}= S_{22}= reflection and S_{12}= S_{21}= transmission.

BIBLIOGRAPHY

[1] J.-N. Burghartz, in *Ultra-Thin Chip Technology and Applications*. Springer, Editor, 2011.

[2] M. James E, "Nanopackaging: Nanotechnologies and electronics packaging," Dec 2008.

[3] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "'"more-than-moore" white paper," *International Technology Roadmap for Semiconductors (ITRS)*, 2010.

[4] G. Q. Zhang, "'"more than moore" - the changing international landscape, strategy and solutions of micro/nanoelectronics," in *2007 8th International Conference on Electronic Packaging Technology*, Aug 2007, pp. 1–1.

[5] R. D. Bringans and J. Veres, "Challenges and opportunities in flexible electronics," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 6.4.1–6.4.2.

[6] T.-Y. Kuo, Y.-C. Shih, Y.-C. Lee, H.-H. Chang, Z.-C. Hsiao, C.-W. Chiang, S.-M. Li, Y.-J. Hwang, C.-T. Ko, and Y.-H. Chen, "Flexible and ultra-thin embedded chip package," in *2009 59th Electronic Components and Technology Conference*, May 2009, pp. 1749–1753.

[7] G. Alavi, H. Sailer, H. Richter, B. Albrecht, M. Alshahed, C. Harendt, and J. N. Burghartz, "Micro-hybrid system in polymer foil based on adaptive layout," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, Sept 2016, pp. 1–5.

[8] J. N. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chips and related applications, a new paradigm in silicon tech-

nology," in *2009 Proceedings of the European Solid State Device Research Conference*, Sept 2009, pp. 29–36.

[9] C. Harendt, Z. Yu, J. N. Burghartz, J. Kostelnik, A. Kugler, and S. Saller, "Hybrid systems in foil (hysif) exploiting ultra-thin flexible chips," in *2014 44th European Solid State Device Research Conference (ESSDERC)*, Sept 2014, pp. 210–213.

[10] G. Moore, "Cramming more components onto integrated circuits," pp. 114–117, 1965.

[11] H. K. C. Jr, "Miniaturized electronics," pp. 402–413, Jan 2005.

[12] "Evolutionary advances in conventional packaging technologies," in *INTEGRATED CIRCUIT ENGINEERING CORPORATION*.

[13] R. R. Tummala, "Packaging: past, present and future," in *2005 6th International Conference on Electronic Packaging Technology*, Aug 2005, pp. 3–7.

[14] H. K. C. Jr., "Apl's packaging future: The next few years," in *Johns Hopkins Apl Technical Digest*, 1999, pp. 101–110.

[15] J. G. Aday, C. Koehler, T. Tessier, B. Carpenter, Y. Matsuda, and C. Estes, "Flip chip chip scale packaging: transferring the flip chip density requirements from the motherboard to the chip carrier," in *Proceedings. 1998 International Conference on Multichip Modules and High Density Packaging (Cat. No.98EX154)*, Apr 1998, pp. 229–235.

[16] Y. Lin, K. Chen, K. M. Heng, L. Chua, and S. W. Yoon, "Encapsulated water level chip scale package (ewlcs) for cost effective and robust solutions in flexline," in *2014 9th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Oct 2014, pp. 158–161.

[17] Q. Shichun and L. Yong, "Wafer-level chip-scale packaging analog and power semiconductor applications," 2015.

[18] W. Koh, "System in package (sip) technology applications," in *2005 6th International Conference on Electronic Packaging Technology*, Aug 2005, pp. 61–66.

[19] L. Hu, Z. Jin, X. Liao, Y. Ouyang, and J. Dong, "Study of 3d sip (system-in-package) module for package-on-package application using multi-layer pcb manufacturing process," in *2014 15th International Conference on Electronic Packaging Technology*, Aug 2014, pp. 109–112.

[20] F. P. Carson, Y. C. Kim, and I. S. Yoon, "3-d stacked package technology and trends," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 31–42, Jan 2009.

[21] J. Charbonnier, D. Henry, F. Jacquet, B. Aventurier, C. Brunet-Manquat, G. Enyedi, N. Bouzaida, V. Lapras, and N. Sillon, "Wafer level packaging technology development for cmos image sensors using through silicon vias," in *2008 2nd Electronics System-Integration Technology Conference*, Sept 2008, pp. 141–148.

[22] M. Puech, J. M. Thevenoud, J. M. Gruffat, N. Launay, N. Arnal, and P. Godinat, "Fabrication of 3d packaging tsv using drie," in *2008 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS*, April 2008, pp. 109–114.

[23] J. R. Minz, S. Thyagara, and S. K. Lim, "Optical routing for 3-d system-on-package," *IEEE Transactions on Components and Packaging Technologies*, vol. 30, no. 4, pp. 805–812, Dec 2007.

[24] K. Bock, "Polytronics - electronics and systems on flexible substrates," in *IEEE VLSI-TSA International Symposium on VLSI Technology, 2005. (VLSI-TSA-Tech).*, April 2005, pp. 53–56.

[25] S. W. William and S. Alberto, "Flexible electronics: Materials and applications," *Springer*, 2009.

[26] K. Bock, "Polymer electronics systems - polytronics," *Proceedings of the IEEE*, vol. 93, no. 8, pp. 1400–1406, Aug 2005.

[27] J. D. MacKenzie and C. Ho, "Perspectives on energy storage for flexible electronic systems," *Proceedings of the IEEE*, vol. 103, no. 4, pp. 535–553, April 2015.

[28] S. TAKAO. (2013). [Online]. Available: https://spectrum.ieee.org/biomedical/bionics/bionic-skin-for-a-cyborg-you

[29] (2008). [Online]. Available: http://www.flickr.com/photos/rdecom/4146880795/

[30] (2016). [Online]. Available: https://www.printedelectronicsworld.com/articles/10163/high-growth-printable-electronics-market-for-silicon-based-technology

[31] W. J, J. Kostelnik, K. Berschauer, A. Kugler, E. Lorenz, T. Gneiting, C. Harendt, and Z. Yu, "Ultra-thin silicon chips in flexible microsystems," *ECWC13*, 2014.

[32] L. Boettcher, D. Manessis, A. Ostmann, S. Karaszkiewicz, and H. Reichl, "Embedding of chips for system in package realization - technology and applications," in *2008 3rd International Microsystems, Packaging, Assembly Circuits Technology Conference*, Oct 2008, pp. 383–386.

[33] L. Böttcher, "System integration and interconnection technologies," *SMTA International Conference*, Oct 2010.

[34] D. Manessis, S. F. Yen, A. Ostmann, R. Aschenbrenner, and H. Reichl, "Technical understanding of resin-coated-copper (rcc) lamination processes for realization of reliable chip embedding technologies," in *2007 Proceedings 57th Electronic Components and Technology Conference*, May 2007, pp. 278–285.

[35] C. Harendt and J. N. Burghartz, "Flexible systeme in folie - intelligente haut für maschinen," *MST-Kongress 2013*, 2013.

[36] T. Löher, D. Schütze, A. Ostmann, and R. Aschenbrenner, "Module miniaturization by ultra thin package stacking," in *2010 IEEE CPMT Symposium Japan*, Aug 2010, pp. 1–4.

[37] T. Y. Kuo, Z. C. Hsiao, Y. P. Hung, W. Li, K. C. Chen, C. K. Hsu, C. T. Ko, and Y. H. Chen, "Process and characterization of ultra-thin film packages," in *2010 5th International Microsystems Packaging Assembly and Circuits Technology Conference*, Oct 2010, pp. 1–4.

[38] Y. C. Shih, T. Y. Kuo, Y. P. Hung, J. Y. Chang, C. Y. Cheng, K. C. Chen, C. K. Lee, C. K. Hsu, J. H. Huang, Z. C. Hsiao, C. T. Ko, and Y. H. Chen, "Manufacturing and stacking of ultra-thin film packages," in *2009 59th Electronic Components and Technology Conference*, May 2009, pp. 1440–1446.

[39] C.-T. Ko, Y.-C. Shih, J.-Y. Chang, T.-Y. Kuo, Y.-H. Chen, A. Ostmann, and D. Manessis, "Stacking of ultra-thin film packages," in *2008 2nd Electronics System-Integration Technology Conference*, Sept 2008, pp. 125–130.

[40] J. Govaerts, E. Bosman, W. Christiaens, and J. Vanfleteren, "Fine-pitch capabilities of the flat ultra-thin chip packaging (utcp) technology," *IEEE Transactions on Advanced Packaging*, vol. 33, no. 1, pp. 72–78, Feb 2010.

[41] J. van den Brand, J. de Baets, T. van Mol, and A. Dietzel, "Systems-in-foil - devices, fabrication processes and reliability issues," *Microelectronics Reliability*, vol. 48, no. 8, pp. 1123 – 1128, 2008, 19th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008). [Online]. Available: http://www.sciencedirect.com/science/article/pii/S002627140800190X

[42] P. Ekkels, "Ultra-thin packaging technology (utcp) for embedding in flexible substrates," *IMAPS UK Embedded Device Technology*, Sep 2016.

[43] J. Govaerts, W. Christiaens, E. Bosman, and J. Vanfleteren, "Fabrication processes for embedding thin chips in flat flexible substrates," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 1, pp. 77–83, Feb 2009.

[44] L. Wang, "Design and technology of ultra thin chip packages for high-frequency applications up to 60 ghz," *PhD thesis*, 2014.

[45] W. Christiaens, E. Bosman, and J. Vanfleteren, "Utcp: A novel polyimide-based ultra-thin chip packaging technology," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, no. 4, pp. 754–760, Dec 2010.

[46] F. Niklaus, P. Enoksson, E. Kälvesten, and G. Stemme, "Low-temperature full wafer adhesive bonding," *Journal of Micromechanics and Microengineering*, vol. 11, no. 2, p. 100, 2001. [Online]. Available: http://stacks.iop.org/0960-1317/11/i=2/a=303

[47] T. Loher, M. Seckel, B. Pahl, L. Bottcher, A. Ostmann, and H. Reichl, "Highly integrated flexible electronic circuits and modules," in *2008 3rd International Microsystems, Packaging, Assembly Circuits Technology Conference*, Oct 2008, pp. 86–89.

[48] T. Sterken, F. Vermeiren, P. Tremlett, W. Christiaens, and J. Vanfleteren, "Embedding thinned chips in flexible pcbs," in *2012 4th Electronic System-Integration Technology Conference*, Sept 2012, pp. 1–4.

[49] J. Vanfleteren, "Ultra-thin chip packages (utcps) forembedding in mainstream flex circuits," *IMEC-EDM Workshop*, June 2012.

[50] T. Sterken, J. Vanfleteren, T. Torfs, M. O. de Beeck, F. Bossuyt, and C. V. Hoof, "Ultra-thin chip package (utcp) and stretchable circuit technologies for wearable ecg system," in *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, Aug 2011, pp. 6886–6889.

[51] T. T. F. V. C. V. H. J. V. T. Sterken, M. Op de Beeck, "Embedded utcp interposers for miniature smart sensors," *IMAPS medical applications workshop*, Dec 2012.

[52] M.-U. Hassan, C. Schomburg, E. Penteker, C. Harendt, T. Hoang, and J. N. Burghartz, "Imbedding ultra-thin chips in polymers," *ICT.OPEN 2011, Veldhoven, Netherlands*, 2011.

[53] M. U. Hassan, C. Schomburg, C. Harendt, E. Penteker, and J. N. Burghartz, "Assembly and embedding of ultra-thin chips in polymers," in *2013 Eurpoean Microelectronics Packaging Conference (EMPC)*, Sept 2013, pp. 1–6.

[54] S.-T. Lu and W.-H. Chen, "Reliability of ultra-thin chip-on-flex (utcof) with anisotropic conductive adhesive (aca) joints," in *2008 58th Electronic Components and Technology Conference*, May 2008, pp. 1287–1293.

[55] S. T. Lu and W. H. Chen, "Reliability and flexibility of ultra-thin chip-on-flex (utcof) interconnects with anisotropic conductive adhesive (aca) joints," *IEEE Transactions on Advanced Packaging*, vol. 33, no. 3, pp. 702–712, Aug 2010.

[56] C. Landesberger, N. Palavesam, W. Hell, A. Drost, R. Faul, H. Gieser, D. Bonfert, K. Bock, and C. Kutter, "Novel processing scheme for embedding and interconnection of ultra-thin ic devices in flexible chip foil packages and recurrent bending reliability analysis," in *2016 International Conference on Electronics Packaging (ICEP)*, April 2016, pp. 473–478.

[57] H. Mahadi, "Ultra-thin chip embedding and interconnect technology for system-in-foil applicationsl," in *Ph.D. Thesis, University of Stuttgart*, Feb 2017.

[58] R. Rajoo, Y. Y. Lim, S. C. Chong, M. Paing, F. D. Moses, J. S. T. W. Hong, V. N. Sekhar, S. W. Ho, S. Thew, J. W. K. Soon, and X. Zhang, "Embedding of 15um thin chip and passives in thin flexible substrate," in *2010 12th Electronics Packaging Technology Conference*, Dec 2010, pp. 489–496.

[59] L. Huang, W. Rieutort-Louis, Y. Hu, J. Sanz-Robinson, S. Wagner, J. C. Sturm, and N. Verma, "A super-regenerative radio on plastic based on thin-film transistors and antennas on large flexible sheets for distributed communication links," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 458–459.

[60] T. Moy, S. Wagner, W. Rieutort-Louis, Y. Hu, L. Huang, J. Sanz-Robinson, J. C. Sturm, and N. Verma, "Hybrid large-area systems: Challenges in interfacing," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1374–1377.

[61] W. S. A. Rieutort-Louis, J. Sanz-Robinson, T. Moy, L. Huang, Y. Hu, Y. Afsar, J. C. Sturm, N. Verma, and S. Wagner, "Integrating and interfacing flexible electronics in hybrid large-area systems," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 9, pp. 1219–1229, Sept 2015.

[62] N. Verma, Y. Hu, L. Huang, W. S. A. Rieutort-Louis, J. S. Robinson, T. Moy, B. Glisic, S. Wagner, and J. C. Sturm, "Enabling scalable hybrid systems: Architectures for exploiting large-area electronics in applications," *Proceedings of the IEEE*, vol. 103, no. 4, pp. 690–712, April 2015.

[63] J. N. Burghartz, S. Ferwana, and C. Harendt, "Ultrathin chips for flexible electronics and 3d ics," in *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2015, pp. 1–3.

[64] K. Gurnett and T. Adams, "Ultra-thin semiconductor wafer applications and processes," *III-Vs Review*, vol. 19, no. 4, pp. 38 – 40, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S096112900671643X

[65] J. N. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chip technology and applications, a new paradigm in silicon technology," *Solid-State Electronics*, vol. 54, no. 9, pp. 818 – 829, 2010, selected Papers from the ESSDERC 2009 Conference. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110110001590

[66] E.-B. Jeon, J.-D. Park, J. H. Song, H. J. Lee, and H.-S. Kim, "Bi-axial fracture strength characteristic of an ultra-thin flash memory chip," *Journal of Micromechanics and Microengineering*, vol. 22, no. 10, p. 105014, 2012. [Online]. Available: http://stacks.iop.org/0960-1317/22/i=10/a=105014

[67] E.-M. Tropper, C. Harendt, S. Schmiel, and J. N. Burghartz, "Development and characterization of a grinding process for ultra-thin chip fabrication," *ictopen*, March 2015.

[68] S. Takyu, T. Kurosawa, N. Shimizu, and S. Harada, "Novel wafer dicing and chip thinning technologies realizing high chip strength," in *56th Electronic Components and Technology Conference 2006*, 2006, pp. 5 pp.–.

[69] O. S. Hamad, O. Sidek, M. Rehman, K. Ibrahim, and M. H.Mourad, "Brief: Fabrication processes of silicon-on- insulator and lateral bipolar transistors," *2nd INTERNATIONAL CONFERENCE ON BUILT ENVIRONMENT IN DEVELOPING COUNTRIES*, 2008.

[70] J. N. Burghartz, E. Angelopoulos, W. Appel, S. Endler, S. Ferwana, C. Harendt, M. U. Hassan, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chips for flexible electronics," in *2013 IEEE International Conference of Electron Devices and Solid-state Circuits*, June 2013, pp. 1–2.

[71] M. Zimmermann, J. N. Burghartz, W. Appel, N. Remmers, C. Burwick, R. Wurz, O. Tobail, M. Schubert, G. Palfinger, and J. Werner, "A seamless ultra-thin chip fabrication and assembly process," in *2006 International Electron Devices Meeting*, Dec 2006, pp. 1–3.

[72] H. Rempp, J. Burghartz, C. Harendt, N. Pricopi, M. Pritschow, C. Reuter, H. Richter, I. Schindler, and M. Zimmermann, "Ultra-thin chips on foil for flexible electronics," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2008, pp. 334–617.

[73] R. Fillion, "Advanced packaging technology for leading edge microelectronics and flexible electronics," in *GE Global Research*, 2013. [Online]. Available: https://www.yumpu.com/en/document/view/4032515/advanced-packaging-technology-for-leading-edge-microelectronics

[74] G. Alavi, J. N. Burghartz, H. Sailer, B. Albrecht, C. Harendt, and J. N. Burghartz, "Optimized adaptive layout technique for hybrid systems in foil," in *2017 21st European Microelectronics and Packaging Conference (EMPC) Exhibition*, Sept 2017, pp. 1–5.

[75] in *Processing Procedures for CYCLOTENE 4000 Series Photo BCB Resins*. [Online]. Available: http://www.microchem.com/PDFs_Dow/cyclotene_4000_immersion_dev.pdf

[76] in *TECHNICAL PRODUCT INFORMATION FUJIFILM ELECTRONIC MATERIALS Polyamic Acid. Durimide 100*. [Online]. Available: https://www.fujifilmusa.com/shared/bin/Durimide%20100_US12.pdf

[77] H. P. P. Guide. [Online]. Available: http://www.hdmicrosystems.com/

[78] J. M. Ryan, "Flexible, ultra-thin, embedded die packaging," *Ph.D. Thesis, Auburn, Alabama*, Dec 2010.

[79] M. Woehrmann and M. Toepper. Polymerization of thin film polymers. [Online]. Available: http://cdn.intechopen.com/pdfs/38962/InTech-Polymerization_of_thin_film_polymers.pdf

[80] D. T.-B. Science. [Online]. Available: http://www.brewerscience.com/products/debonding-technologies/

[81] H. Jesmin, "Thermo-mechanical analysis of temporary bonding systems for flexible microelectronics fabrication applications," *Ph.D. Thesis, ARIZONA STATE UNIVERSITY*, May 2011.

[82] MicroChemicals. [Online]. Available: https://www.profactor.at

[83] K. Zoschke, T. Fischer, M. Töpper, T. Fritzsch, O. Ehrmann, T. Itabashi, M. P. Zussman, M. Souter, H. Oppermann, and K. D. Lang, "Polyimide based temporary wafer bonding technology for high temperature compliant tsv backside processing and thin device handling," in *2012 IEEE 62nd Electronic Components and Technology Conference*, May 2012, pp. 1054–1061.

[84] A. Lee, J. Su, B. Huang, D. Bai, W. W. Shen, H. H. Chang, and C. W. Chiang, "A low-temperature temporary lamination and laser debonding technology to enable cost-effective fabrication of a through-glass-via (tgv) interposer on

a panel substrate," in *2015 IEEE 17th Electronics Packaging and Technology Conference (EPTC)*, Dec 2015, pp. 1–5.

[85] P. Andry, R. Budd, R. Polastre, C. Tsang, B. Dang, J. Knickerbocker, and M. Glodde, "Advanced wafer bonding and laser debonding," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, May 2014, pp. 883–887.

[86] K. Zoschke, M. Wegner, T. Fischer, and K. D. Lang, "Temporary handling technology by polyimide based adhesive bonding and laser assisted de-bonding," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, Sept 2016, pp. 1–6.

[87] M. Focke, D. Kosse, C. Mueller, H. Reinecke, R. Zengerle, and F. von Stettena, "Lab-on-a-foil: microfluidics on thin and flexible films," Feb 2010.

[88] E. Commission. (2014-2015) G. technology readiness levels (trl). [Online]. Available: https://ec.europa.eu/research/participants/data/ref/h2020/wp/2014_2015/annexes/h2020-wp1415-annex-g-trl_en.pdfn

[89] Y.-H. So, P. Garrou, J.-H. Im, and D. M. Scheck. Benzocyclobutene-based polymers for microelectronics. [Online]. Available: http://pubs.acs.org/subscribe/archive/ci/31/i12/html/12so.html

[90] in *Processing Procedures for CYCLOTENE 3000 Series Dry Etch Resins*. [Online]. Available: http://www.dow.com/cyclotene/docs/cyclotene_3000_dry_etch.pdf

[91] J. Oberhammer, F. Niklaus, and G. Stemme, "Selective wafer-level adhesive bonding with benzocyclobutene for fabrication of cavities," *Sensors and Actuators A: Physical*, vol. 105, no. 3, pp. 297 – 304, 2003. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0924424703002024

[92] S. A. Vitale, H. Chae, and H. H. Sawin, "Etching chemistry of benzocyclobutene âĂđbcbâĂę low-k dielectric films in f2+o2 and cl2+o2 high density plasmas," *American Vacuum Society*, vol. 18, no. 6, 2000. [Online]. Available: http://ece.umd.edu/courses/enee719f.S2003/papers/2000_Etching%20Chemistery%20of%20BCB.pdf

[93] [Online]. Available: http://www.microchemicals.com/products/adhesion_promotion/hmds.html

[94] MicroChemicals. [Online]. Available: http://microchemicals.com/micro/tds_ti_prime.pdf

[95] G.Alavi, M.-U. Hassan, C. Harendt, and J. N. Burghartz, "Compensation of stress-induced warpage for polymer embedding of ultra-thin chips," in *Proc. of ICT-OPEN, Amersfoort, The Netherlands*, 2015, pp. 42–45.

[96] L. McCaslin, "Methodology for predicting microelectronic substrate warpage incorporating copper trace pattern characteristics," 2008.

[97] H. Kaspar, "Integration of ultrathin silicon chips," *Diplom-Ingenieur Thesis*, April 2009.

[98] F. Johannes, "Construction of a mask alignment table for photolithography," *Diploma thesis, University of Applied Science, Regensburg*, Dec 2005.

[99] J. Yeom, Y. Wu, and M. A. Shannon, "Critical aspect ratio dependence in deep reactive ion etching of silicon," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 2, June 2003, pp. 1631–1634 vol.2.

[100] C. Wim, "Integratie van actieve en passieve componenten in polyimide interconnectie substraten," *Ph.D. Thesis, University of Gent*, 2009.

[101] M. Nordstr "Investigation of the bond strength between the photo-sensitive polymer su-8 and gold," *Microelectronic Engineering*, vol. 78, pp. 152 – 157, 2005, proceedings of the 30th International Conference on Micro- and Nano-Engineering. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931704005556

[102] H. Ito, K. Hasegawa, T. Matsuki, and S. Kusumoto, "Lift-off photoresists for advanced ic packaging metal paternning," in *2015 16th International Conference on Electronic Packaging Technology (ICEPT)*, Aug 2015, pp. 1352–1356.

[103] MicroChemicals. [Online]. Available: http://microchemicals.com/technical_information/lift_off_photoresist.pdf

[104] J. Erb, "Entwicklung folienbasierter nadelelektroden," *Studienarbeit, IMS-CHIPS*, 2016.

[105] C.Harendt, "Komplexe Systeme in Folie, Heterogene Systemintegration auf Basis dünner Si-Chips und flexibler Substrate," in *MikroSystemTechnik Kongress 2015, Karlsruhe, Deutschland*, Oct 2015.

[106] M. I. Systems. [Online]. Available: https://www.hindawi.com/journals/misy/si/961413/cfp/

[107] BMBF-Internetredaktion. [Online]. Available: http://www.vdi-nachrichten.com/Technik-Gesellschaft/Industrie-40-Mit-Internet-Dinge-Weg-4-industriellen-Revolution

[108] R. Christoph. [Online]. Available: https://www.isa.org/intech/20160601/

[109] K. Takei, "High performance, flexible cmos circuits and sensors toward wearable healthcare applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 6.1.1–6.1.4.

[110] J. M. Nassar, G. A. T. Sevilla, S. J. Velling, M. D. Cordero, and M. M. Hussain, "A cmos-compatible large-scale monolithic integration of heterogeneous multisensors on flexible silicon for iot applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 18.6.1–18.6.4.

[111] B. W. I. K. Charles W. Eichelberger, Robert J. Wojnarowski, "Adaptive lithography system to provide high density interconnect," Patent US4 835 704A, 1986.

[112] C. Bishop, B. Rogers, C. Scanlan, and T. Olson, "Adaptive patterning design methodologies," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, May 2016, pp. 7–12.

[113] H. Instrument. [Online]. Available: http://www.himt.de/index.php/vpg-small-area-systems.html

[114] G. Alavi, H. Sailer, B. Albrecht, C. Harendt, and J. N. Burghartz, "Adaptive layout technique for microhybrid integration of chip-film patch," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 5, pp. 802–810, May 2018.

[115] C. A. Mack. [Online]. Available: http://www.lithoguru.com/

[116] M. U. Hassan, E. A. Angelopoulos, H. Rempp, S. Endler, and J. N. Burghartz, "Packaging challenges associated with warpage of ultra-thin chips," in *3rd Electronics System Integration Technology Conference ESTC*, Sept 2010, pp. 1–5.

[117] J. K. S. Kevin T. Turner, Sathish Veeraraghavan, "Predicting distortions and overlay errors due to wafer deformation during chucking on lithography scanners," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 8, pp. 8 – 8 – 8, 2009. [Online]. Available: http://dx.doi.org/10.1117/1.3247857

[118] H. Marien, M. S. J. Steyaert, E. v. Veenendaal, and P. L. Heremans, "On the other applications of organic electronics on foil," *IEEE Solid-State Circuits Magazine*, vol. 4, no. 4, pp. 43–49, Dec 2012.

[119] M. U. Hassan, J. Keck, H. Klauk, J. Kostelnik, Y. Mahsereci, S. Sailer, A. Schreivogel, T. Zaki, and J. N. Burghartz, "Combining organic and printed electronics in hybrid system in foil (hysif) based smart skin for robotic applications," in *2015 European Microelectronics Packaging Conference (EMPC)*, Sept 2015, pp. 1–6.

[120] G. Alavi, M.-U. Hassan, C. Harendt, and J. N. Burghartz, "Compensation of stress-induced warpage for polymer embedding of ultra-thin chips," in *Proc. of ICT-OPEN*, 2015, pp. 42–45.

[121] Z. Tarek, "Short-channel organic thin-film transistors: Fabrication, characterization, modeling and circuit demonstration," *Ph.D. Thesis, University of Stuttgart*, Nov 2014.

[122] M. Aghamohammadi, R. Rödel, U. Zschieschang, C. Ocal, H. Boschker, R. T. Weitz, E. Barrena, and H. Klauk, "Threshold-voltage shifts in organic transistors due to self-assembled monolayers at the dielectric: Evidence for electronic coupling and dipolar effects," *ACS Applied Materials & Interfaces*, vol. 7, no. 41, pp. 22 775–22 785, 2015, pMID: 26415103. [Online]. Available: http://dx.doi.org/10.1021/acsami.5b02747

[123] U. Zschieschang, H. Klauk, M. J. Kang, K. Takimiya, T. Sekitani, T. Someya, T. W. Canzler, A. Werner, and J. Blochwitz-Nimoth, "Performance and stability of flexible low-voltage organic thin-film transistors based on c10-dntt," in *2012 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS)*, March 2012, pp. 1–4.

[124] M.Elsobky, G.Alavi, U. Zschieschang, M. Aghamohammadi, M. U. Hassan, H. Klauk, C. Harendt, H. Richter, and J. N. Burghartz, "Application of bcb-on-si based substrate in combining flexible organic electronics and high frequency antenna," 2016.

[125] M. Elsobky, M. Elattar, G. Alavi, F. Letzkus, H. Richter, U. Zschieschang, M. Strecker, H. Klauk, and J. N. Burghartz, "A digital library for a flexible low-voltage organic thin-film transistor technology," *Organic Electronics*, vol. 50, no. Supplement C, pp. 491 – 498, 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1566119917304275

[126] K. Ulrike, "Synthesis and characterization of functionalized thioacenes for organic thin-film transistors," *Ph.D. Thesis, University of Freiberg*, 2015.

[127] U. Zschieschang, R. Rödel, U. Kraft, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J. N. Burghartz, W. Xiong, B. Murmann, and H. Klauk, "Low-voltage organic transistors for flexible electronics," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2014, pp. 1–6.

[128] T. resources. Differences between three point and four point bending tests. [Online]. Available: http://www.testresources.net/blog/what-are-the-differences-between-3-point-and-4-point-bending-test/

[129] H. Chandra, S. W. Allen, S. W. Oberloier, N. Bihari, J. Gwamuri, and J. M. Pearce, "Open-source automated mapping four-point probe," 2017.

[130] S. Logothetidis, "Handbook of flexible organic electronics," *Elsevier Science*, 2014.

[131] J. Lewis, "Material challenge for flexible organic devices," *Materials Today*, vol. 9, no. 4, pp. 38 – 45, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369702106714468

[132] H. Chen, B. W. Lu, Y. Lin, and X. Feng, "Interfacial failure in flexible electronic devices," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 132–134, Jan 2014.

[133] T. Braun, J. Bauer, K. F. Becker, O. Hölck, H. Walter, M. van Dijk, R. Aschenbrenner, and K. D. Lang, "Influence of humidity on reliability of plastic packages," in *2015 European Microelectronics Packaging Conference (EMPC)*, Sept 2015, pp. 1–6.

[134] E. Terzic, J. Terzic, R. Nagarajah, and M. Alamgir, "Capacitive sensing technology," in *A Neural Network Approach to Fluid Quantity Measurement in Dynamic Environments*, 2012.

[135] M. Elsobky, B. Albrecht, P. Ganter, K. Szendrei, T. Deuble, C. Harendt, B. V. Lotsch, and J. N. Burghartz, "Relative humidity sensors for system-in-foil applications," 2017.

[136] L. Sun, G. Qin, H. Huang, H. Zhou, N. Behdad, W. Zhou, and Z. Ma, "Flexible high-frequency microwave inductors and capacitors integrated on a polyethylene terephthalate substrate," *Applied Physics Letters*, vol. 96, Jan 2010.

[137] A. E. Ostfeld, I. Deckman, A. M. Gaikwad, C. M. Lochner, and A. C. Arias, "Screen printed passive components for flexible power electronics," *Scientific Reports*, vol. 5, pp. 15 959 EP –, Oct 2015, article. [Online]. Available: http://dx.doi.org/10.1038/srep15959

[138] M. Elsobky, G. Alavi, B. Albrecht, T. Deuble, C. Harendt, H. Richter, Z. Yu, and J. N. Burghartz, "Ultra-thin sensor systems integrating silicon chips with on-foil passive and active components," *Proceedings*, vol. 2, no. 13, 2018. [Online]. Available: http://www.mdpi.com/2504-3900/2/13/748

[139] L. Li, Z. Gao, and Y. Wang, "Nfc antenna research and a simple impedance matching method," in *Proceedings of 2011 International Conference on Electronic Mechanical Engineering and Information Technology*, vol. 8, Aug 2011, pp. 3968–3972.

[140] F. Lepinois, S. Pinel, A. Cazarre, J. Tasselli, A. Marty, J. P. Bailbe, J. R. Morante, F. Murray, and O. Gonnard, "Ultra-thinned chips integration: technological approach and electrical qualification," in *2002 23rd International Conference on Microelectronics. Proceedings (Cat. No.02TH8595)*, vol. 2, 2002, pp. 521–524.

[141] G. Alavi, S. Özbek, M. Rasteh, M. Grözing, M. Berroth, J. Hesselbarth, and J. N. Burghartz, "Towards a flexible and adaptive wireless hub by embedding power amplifier thinned silicon chip and antenna in a polymer foil," in *International Journal of Microwave and Wireless Technologies*, 2019, in press.

[142] D. M. Krafcsik and D. E. Dawson, "A closed-form expression for representing the distributed nature of the spiral inductor," in *Microwave and Millimeter-Wave Monolithic Circuits*, vol. 86, no. 1, Jun 1986, pp. 87–92.

[143] E. Stefan, "Bending-stress management by stacking of ultrathin integrated circuit chips," *PhD Thesis*, July 2012.

[144] G. N. Greaves, "Poisson's ratio over two centuries: challenging hypotheses," *Notes and Records*, vol. 67, no. 1, pp. 37–58, 2013. [Online]. Available: http://rsnr.royalsocietypublishing.org/content/67/1/37

[145] T. Engineering. [Online]. Available: https://www.teachengineering.org/lessons/view/cub_surg_lesson02

[146] S. Seok, J. Kim, N. Rolland, P. A. Rolland, and S. Bouwstra, "Thermo-mechanical simulation of bcb membrane thin-film package," in *2010 11th International Thermal, Mechanical Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE)*, April 2010, pp. 1–4.

[147] K. Wang, Y. Huang, A. Chandra, and K. X. Hu, "Interfacial shear stress, peeling stress, and die cracking stress in trilayer electronic assemblies," in *ITHERM 2000. The Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No.00CH37069)*, vol. 2, 2000, pp. 56–64 vol. 2.

[148] M. S. Alshahed, Z. Yu, H. Rempp, H. Richter, and J. N. Burghartz, "Thermal investigation of ultra-thin si chips," *ictopen*, pp. 1–4, 2013.

[149] T. L. Bergman, A. S. Lavine, F. P. Incropera, and D. P. DeWitt, "Fundamentals of heat and mass transfer," *New York: J. Wiley*, 2002.

[150] M. Alshahed, "Thermal investigations and characterization of ultra-thin silicon chips," *Master thesis*, 2013.

[151] (2015, Sep) Heat transfer mechanisms. [Online]. Available: http://www.engr.colostate.edu/~allan/heat_trans/page4/page4.html

[152] M. S. Alshahed, Z. Yu, H. Richter, C. Harendt, and J. N. Burghartz, "Measurement-based compact thermal model extraction methodology for packaged ics," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 11, pp. 1786–1794, Nov 2017.

[153] G. Alavi, S. Özbek, M. Rasteh, M. Grözing, M. Berroth, J. Hesselbarth, and J. N.Burghartz, "Embedding and interconnecting of ultra-thin rf chip in combination with flexible wireless hub in polymer foil," in *2018 7th Electronic System-Integration Technology Conference (ESTC)*, Sept 2018, pp. 1–5.

[154] S. Özbek, G. Alavi, J. Digel, M. Grözing, J. N. Burghartz, and M. Berroth, "3-path sige bicmos power amplifier on thinned substrate for iot applications," 2018. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S016792601730634X

[155] G. P. Peterson, "An introduction to heat pipes: Modeling, testing, and applications," *Hoboken, NJ, USA: Wiley*, 1994.

[156] R. Lewis, S. Xu, L. A. Liew, C. Coolidge, R. Yang, and Y. C. Lee, "Thin flexible thermal ground planes: Fabrication and scaling characterization," *Journal of Microelectromechanical Systems*, vol. 24, no. 6, pp. 2040–2048, Dec 2015.

[157] J. Semple, D. G. Georgiadou, G. Wyatt-Moon, G. Gelinck, and T. D. Anthopoulos, "Flexible diodes for radio frequency (rf) electronics: a materials perspective," *Semiconductor Science and Technology*, vol. 32, no. 12, p. 123002, 2017. [Online]. Available: http://stacks.iop.org/0268-1242/32/i=12/a=123002

[158] Agilent basics of measuring the dielectric properties of materials. [Online]. Available: http://academy.cba.mit.edu/classes/input_devices/meas.pdf

[159] D. L. Cuenca, "On-chip spherical dielectric resonator-based millimeter-wave components," *PhD Thesis, University of Stuttgart*, 2017.

[160] G. Breed, "The fundamentals of patch antenna design and performance," in *High Frequency Electronics*, March 2009. [Online]. Available: https://www.highfrequencyelectronics.com/Mar09/HFE0309_Tutorial.pdf

[161] B. D. Orban and G. Moernaut, "The basics of patch antennas," in *RF Globalnet*, Sep 2009.

[162] S. Winder and J. Carr, in *Newnes Radio and RF Engineering Pocket Book*. Newnes, 2002.

[163] S. Costanzo, I. Venneri, G. Di Massa, and A. Borgia, "Benzocyclobutene as substrate material for planar millimeter-wave structures: Dielectric characterization and application," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 31, no. 1, p. 66, Jul 2009. [Online]. Available: https://doi.org/10.1007/s10762-009-9552-0

[164] D. L. Cuenca, J. Hesselbarth, and G. Alavi, "Chip-mounted dielectric resonator antenna with alignment and testing features," in *2016 46th European Microwave Conference (EuMC)*, Oct 2016, pp. 723–726.

[165] D. L. Cuenca, G. Alavi, and J. Hesselbarth, "Low-loss mm-wave transition from on-chip microstrip to rectangular waveguide," in *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Oct 2017.

[166] ——, "On-chip mm-wave spherical dielectric resonator bandpass filter," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, June 2017, pp. 1460–1463.

[167] T. Meister, F. Ellinger, J. W. Bartha, M. Berroth, J. Burghartz, M. Claus, L. Frey, A. Gagliardi, M. Grundmann, J. Hesselbarth, H. Klauk, K. Leo, P. Lugli, S. Mannsfeld, Y. Manoli, R. Negra, D. Neumaier, U. Pfeiffer, T. Riedl, S. Scheinert, U. Scherf, A. Thiede, G. Tröster, M. Vossiek, R. Weigel, C. Wenger, G. Alavi, M. Becherer, C. A. Chavarin, M. Darwish, M. Ellinger, C. Y. Fan, M. Fritsch, F. Grotjahn, M. Gunia, K. Haase, P. Hillger, K. Ishida, M. Jank, S. Knobelspies, M. Kuhl, G. Lupina, S. M. Naghadeh, N. MÃijnzenrieder, S.Özbek, M. Rasteh, G. A. Salvatore, D. Schrüfer, C. Strobel, M. Theisen, C. Tückmantel, H. von Wenckstern, Z. Wang, and Z. Zhang, "Program fflexcom - high frequency flexible bendable electronics for wireless communication systems," in *2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, Nov 2017, pp. 1–6.

[168] L. Haiyan, C. Wei, Z. Zhijiang, Z. Jianjun, W. Yuan, K. Yuechan, and C. Tangshen, "220ghz on-wafer measurement based on trl calibration method," in *2015 12th IEEE International Conference on Electronic Measurement Instruments (ICEMI)*, vol. 02, July 2015, pp. 868–871.

[169] S. S. Hamid, M. F. Ain, S. K. K. Mohd, R. A. Zawawi, N. Rhaffor, and A. A. Manaf, "Implementation of trl (thru-reflect-line) calibration kit for power amplifier measurement," in *2016 IEEE International Conference on Automatic Control and Intelligent Systems (I2CACIS)*, Oct 2016, pp. 147–150.

[170] Komplexe Systeme in Folie (kosif). [Online]. Available: http://kosif.ims-chips.de/

[171] M. Giousouf, R. Kaminski, and S. Saller, "Haltevorrichtung zum Festhalten von Gegenständen," Sep 2012. [Online]. Available: https://www.google.ch/patents/EP2502714A1?cl=de

[172] V. Matic, J. Keck, A. Ilchmann, B. Polzinger, W. Eberhardt, and H. Kück, "Printing of functional silver structures on polymer based 3d-packages," Aug 2012.

[173] M. Klopfer, C. Cordonier, K. Inoue, G. P. Li, H. Honma, and M. Bachman, "Flexible, transparent electronics for biomedical applications," in *2013 IEEE 63rd Electronic Components and Technology Conference*, May 2013, pp. 494–499.

[174] P. Mostafalu, A. S. Nezhad, M. Nikkhah, and M. Akbari, "Flexible electronic devices for biomedical applications," in *Advanced Mechatronics and MEMS Devices II - 2017*, 2017.

[175] G.Alavi, M. Nawito, R. Saleh, M.-U. Hassan, C. Harendt, H. Richter, A. Stett, and J. Burghartz, "Embedding ultra-thin implantable biosensor system in polymer foils." Süd-west-kongress, 2016.

Author Publications

Journal Articles

1. **G. Alavi**, H. Sailer, B. Albrecht, C. Harendt, and J. N.Burghartz, "Adaptive Layout Technique for Micro Hybrid Integration of Chip-Film Patch", in IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 8, 2018, Pages 802-810, ISSN 2156-3950, doi: 10.1109/TCPMT.2018.2818762.

2. **G. Alavi**, S. Özbek, M. Rasteh, M. Grözing, M. Berroth, J. Hesselbarth, snd J. N.Burghartz, "Towards a Flexible and Adaptive Wireless Hub by Embedding Power Amplifier Thinned Silicon Chip and Antenna in a Polymer Foil", in International Journal of Microwave and Wireless Technologies, 2019, in press.

3. J. N. Burghartz, **G. Alavi**, B. Albrecht, T. Deuble, M. Elsobky, S. Ferwana, C. Harendt, Y. Mahsereci, H. Richter, and Z. Yu, "Hybrid Systems-in-Foil - Combining the Merits of Thin Chips and of Large-Area Electronics", in IEEE Journal of the Electron Devices Society, 2018, in press.

4. S. Özbek, **G. Alavi**, J. Digel, M. Grözing, J. N. Burghartz, and M. Berroth, " 3-Path SiGe BiCMOS Power Amplifier for IoT Applications on Thin Substrate", Integration, Available online 18 May 2018, ISSN 0167-9260, https://doi.org/10.1016/j.vlsi.2018.04.010.

5. M. Elsobky, **G. Alavi**, B. Albrecht, T. Deuble, C. Harendt, H. Richter, Z. Yu, J. N. Burghartz, "Ultra-thin sensor systems integrating silicon chips with on-foil passive and active components," Proceedings 2018, vol 2, no. 13, 2018. [Online]. Available: http://www.mdpi.com/2504-3900/2/13/748.

6. M. Elsobky, M. Elattar, **G. Alavi**, F. Letzkus, H. Richter, U. Zschieschang, M. Strecker, H. Klauk, J. N. Burghartz, "A digital library for a flexible low-voltage organic thin-film transistor technology", Organic Electronics, Volume 50, 2017, Pages 491-498, ISSN 1566-1199, https://doi.org/10.1016/j.orgel.2017.08.028.

Conferences

1. **G. Alavi**, M.-U. Hassan, C. Harendt and J. N. Burghartz, "Compensation of Stress-Induced Warpage for Polymer Embedding of Ultra-thin Chips", Proc. of ICT-OPEN, Amersfoort, The Netherlands, pp. 42-45, 2015.

2. **G. Alavi**, M. Nawito, R. Saleh, M.-U. Hassan, C. Harendt, H. Richter, A. Stett and J. N. Burghartz, "Embedding Ultra-Thin Implantable Biosensor System in Polymers Foil", Proc. of Clusterkonferenz des Spitzenclusters MicroTEC Südwest, Freiburg, Germany, 2016.

3. **G. Alavi**, H. Sailer, H. Richter, B. Albrecht, M. Alshahed, C. Harendt, and J. N. Burghartz, "Micro-hybrid system in polymer foil based on adaptive layout", 2016 6th Electronic System-Integration Technology Conference (ESTC), Grenoble, 2016, pp. 1-5. doi: 10.1109/ESTC.2016.7764465.

4. **G. Alavi**, H. Sailer, B. Albrecht, C. Harendt, and J. N. Burghartz, "Optimized adaptive layout technique for hybrid systems in foil," 2017 21st European Microelectronics and Packaging Conference (EMPC) & Exhibition, Warsaw, Poland, 2017, pp. 1-5. doi: 10.23919/EMPC.2017.8346851.

5. **G. Alavi**, S. Özbek, M. Rasteh, M. Grözing, M. Berroth, J. Hesselbarth and J. N. Burghartz, "Embedding and Interconnecting of Ultra-Thin RF Chip in Combination with Flexible Wireless Hub in Polymer Foil," 2018 7th Electronic System-Integration Technology Conference (ESTC), Dresden, 2018.

6. D. L. Cuenca, **G. Alavi**, and J. Hesselbarth, "Chip-mounted dielectric resonator antenna with alignment and testing features," 2016 46th European Microwave Conference (EuMC), London, 2016, pp. 723-726. doi: 10.1109/EuMC.2016.7824445

7. M. Elsobky, **G. Alavi**, Ute Zschieschang, M. Aghamohammadi, M.-UI Hassan, H. Klauk, C. Harendt, H. Richter, and J. N. Burghartz, " Application of BCB-on-Si based substrate in combining flexible organic electronics and high frequency antenna", Oe-2016, Max Planck Institute (MPI), Stuttgart, 2016.

8. B. Albrecht, **G. Alavi**, M.-U. Hassan, S. Ferwana, H. Sailer, C. Harendt, und J. Burghartz, "Hybride Systeme in Folie mittels Adaptivem Layout und einem Laserdirektschreiber für die Herstellung von Prototypen", Der MikroSystemTechnik Kongress (MST) 2017, October 2017, Munich, Germany.

9. D. L. Cuenca, **G. Alavi** and J. Hesselbarth, "On-chip mm-wave spherical dielectric resonator bandpass filter," 2017 IEEE MTT-S International Microwave Symposium (IMS), Honololu, HI, 2017, pp. 1460-1463.
doi: 10.1109/MWSYM.2017.8058896

10. D. L. Cuenca, **G. Alavi** and J. Hesselbarth, "Low-loss mm-wave transition from on-chip microstrip to rectangular waveguide," 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, 2017, pp. 325-328. doi: 10.23919/EuMIC.2017.8230724.

11. B. Albrecht, **G. Alavi**, M. Elsobky, S. Ferwana, U. Passlack, C. Harendt, und J. Burghartz, "Multi-Chip patch in low stress polymer foils based on an adaptive layout for flexible sensor systems," 2018 7th Electronic System-Integration Technology Conference (ESTC), Dresden, 2018.

12. J. N.Burghartz, **G. Alavi**, B. Albrecht, T. Deuble, M. Elsobky, S. Ferwana, C. Harendt, Y. Mahsereci , H. Richter, Z. Yu, "Hybrid Systems-in-Foil - Combining Thin Chips with Large-Area Electronics," 2018 International Flexible Electronics Technology Conference (IFETC), Invited speaker.

13. S. Özbek, J. Digel, M. Grözing, M. Berroth, **G. Alavi** and J. N. Burghartz, "3-Path 5-6 GHz 0.25 µm SiGe BiCMOS power amplifier on thin substrate," 2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Giardini Naxos, 2017, pp. 49-52. doi: 10.1109/PRIME.2017.7974104.

14. S. Özbek, J. Digel, M. Grözing, M. Berroth, **G. Alavi** and J. N. Burghartz, "Three-Path SiGe BiCMOS LNA on Thinned Silicon Substrate for IoT Applications," 2018 European Microwave Week (EuMW2018), Madrid, 2018.

15. T. Meister, F. Ellinger, J. W. Bartha, M. Berroth , J. Burghartz, M. Claus, L. Frey, A. Gagliardi , M. Grundmann , J. Hesselbarth, H. Klauk, K. Leo, P. Lugli , S. Mannsfeld, Y. Manoli, R. Negra, D. Neumaier, U. Pfeiffer, T. Riedl, S. Scheinert , U. Scherf, A. Thiede , G. Tröster, M. Vossiek, R. Weigel, C. Wenger, **G. Alavi**, M. Becherer , C. Alvarado Chavarin, M. Darwish , M. Ellinger, C. Fan, M. Fritsch, F. Grotjahn, M. Gunia, K. Haase, P. Hillger, K. Ishida, M. Jank, S. Knobelspies, M. Kuhl, G. Lupina, S. Mohammadi Naghadeh, N. Münzenrieder, S. Özbek, M. Rasteh , G. A. Salvatore, D. Schrüfer, C. Strobel, M. Theisen, C. Tückmantel, H. von Wenckstern , Z. Wang , Z. Zhang, "Program FFlexCom - High frequency flexible bendable electronics for wireless communication systems," 2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Tel-Aviv, 2017, pp. 1-6. doi: 10.1109/COMCAS.2017.8244733

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