Realization of Silicon-Based Monolithic E-Band IMPATT-Transmitter and Schottky-Receiver for Wireless Applications

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Erklärung über die Eigenständigkeit der Dissertation

Ich versichere, dass ich die vorliegende Arbeit mit dem Titel:

"Realisierung eines monolithischen, Silizium-basierten E-Band-IMPATT-Sender- und Schottky-Empfängermoduls für Drahtlosekommunikationsanwendungen"

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I hereby certify that the dissertation entitled:

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is entirely my own work except where otherwise indicated; Passages and ideas from other sources have been clearly indicated. This thesis has never been submitted in the same or substantially similar version to any other examination office.

Name/ Name: Wogong Zhang

Unterschrift/ Signed: ______________________________

Stuttgart, den 25.06.2019

To my beloved wife Sui and our daughter Lia

&

our parents

&

my grandparents

Zusammenfassung der Dissertation:

Realisierung eines monolithischen, Silizium-basierten E-Band-IMPATT-Sender- und Schottky-Empfängermoduls für Drahtlosekommunikationsanwendungen

von Wogong Zhang

Die vorliegende Arbeit beschäftigt sich mit dem Design und der monolithischen Implementierung eines Silizium-basierten Sender- und Empfängermoduls für das E-Band (60 GHz $\leq f \leq$ 90 GHz). Bei dem Sendermodul handelt es sich um einen spannungsgesteuerten Oszillator (VCO, engl. für Voltage-Controlled Oscillator), dessen Kernelement eine IMPATT-Diode (IMPATT, engl. für Impact-Ionization Avalanche Transit-Time) mit einem negativ-differentiellen Widerstand (NDR, engl. für Negative Differential Resistance) ist und die durch Kleinsignal-S-Parametermessungen charakterisiert wird. Die IMPATT-Diode speist mit Hilfe einer angepassten Koplanarwellenleiter-struktur (CPW, engl. für Co-Planar Waveguide) eine Patchantenne mit der Betriebsfrequenz $f_{op} =$ 82 GHz, die sich aus der zuvor bestimmten Betriebsfrequenz der IMPATT-Diode ergibt. Die Charakterisierung der Patchantenne erfolgt in einer Absorberkammer. Das komplette Sendermodul wird monolithisch auf einen Silizium-Chip integriert.
Das final hergestellte Sendermodul besitzt eine Chipfläche von $A_{chip} = 4$ mm^2 und emittiert bei einer Frequenz von $f_{op} = 82{,}17$ GHz die äquivalente, isotrop emittierte Strahlungsleistung (EIRP, engl. für Equivalent Isotropically Radiated Power) $EIRP = 18{,}43$ dBm. Mit einem Verstärkungsfaktor $G_{ant} = 7{,}35$ dBi der CPW-Patchantenne und einem Leitungsverlust von 0,57 dB wird bei einer Betriebsfrequenz von $f_{op} = 82$ GHz (DC-„Bias“-Bedingungen: $I_{bias} = 25$ mA, $V_{bias} =$ 13,4 V) eine „DC-zu-RF“-Effizienz (DC, engl. für Direct Current; RF, engl. für Radio Frequency) $\eta_{DC-RF} = 4{,}36$ % erreicht.

Kernelement des Empfängermoduls ist eine Schottky-Diode mit einer Querschnittsfläche $A_d = 6$ µm^2, die im sog. MOTT-Betrieb als Gleichrichter des empfangenen Hochfrequenzsignals dient. Das Hochfrequenzsignal selbst wird entweder mit einer Halbwellengleichrichterantenne oder mit einer Vollwellenbrückengleichrichterantenne detektiert. Diese werden zusammen mit der Schottky-Diode monolithisch auf einem Silizium-Chip entweder aus einem seriell gespeisten CPW-Patchantennenfeld mit einer Chipfläche $A_{chip} = 60$ mm^2 und einer Abstrahlfrequenz $f_R =$

85 GHz oder aus einer „Bow Tie“-Antenne mit einer Chipfläche $A_{chip} = 4$ mm^2 und einer Abstrahlfrequenz $f_R = 80$ GHz aufgebaut. Dank der hohen Grenzfrequenz der integrierten Schottky-Dioden im MOTT-Betrieb ($f_{co} > 0{,}5$ THz unter der Bedingung $I_{bias} = 0$ A) können die Konversionsspannungen ΔV_{conv} der Halbwellengleichrichterantenne bei einer Betriebsfrequenz $f_{op} = 85$ GHz im Bereich 1 mV $\leq \Delta V_{conv} \leq$ 17 mV (0,1 μA $\leq I_{bias} \leq$ 0,44 mA) bzw. der Vollwellenbrückengleichrichterantenne bei einer Betriebsfrequenz $f_{op} = 80$ GHz im Bereich 1 mV $\leq \Delta V_{conv} \leq$ 40 mV (0,1 nA $\leq I_{bias} \leq$ 0,6 mA*)* abgestimmt werden. Unter Berücksichtigung der gemessenen Spannungskonversion, der geometrischen Dimension des Chips und des Detektionsbereichs erweist sich bezüglich Gleichrichteeffizienz die Vollwellenbrückengleichrichterantenne gegenüber der Halbwellengleichrichterantenne als leistungsstärker.

Damit ist die Realisierbarkeit eines hochperformanten, integrierten E-Band-IMPATT-Sender- und Schottky-Empfängermoduls in SIMMWIC-Technologie (SIMMWIC, engl. für Silicon mm-Wave Integrated Circuit) mit einer Chipfläche $A_{chip} = 4$ mm^2 erfolgreich demonstriert. Im Vergleich zur Silizium-basierten RF-CMOS- bzw. BiCMOS-Technologie (BiCMOS, engl. für Bipolar Complementary Metal-Oxide-Semiconductor) könnte somit die SIMMWIC-Technologie eine kostengünstigere Alternative für moderne, hochperformante Drahtloskommunikationsanwendungen darstellen.

Abstract of the dissertation:

Realization of Silicon-Based Monolithic E-Band IMPATT-Transmitter and Schottky-Receiver for Wireless Applications

of Wogong Zhang

This thesis investigates extensively the design and implementation each of silicon-based monolithically integrated E-band (60 GHz $\leq f \leq$ 90 GHz) transmitter and receiver modules.

Based on the small-signal S-parameter characterized negative differential resistance (NDR) spectra offered by impact-ionization avalanche transit-time (IMPATT) diodes as active device, voltage-controlled oscillator (VCO) circuits have been designed and implemented simply by using one-metal-layer coplanar waveguides (CPWs) as passive structures. To realize the monolithic IMPATT-transmitter an on-chip CPW-fed patch antenna with operation frequency f_{op} = 82 GHz is designed and integrated to IMPATT-VCOs with similar working frequencies. According to the link budget calculation, an equivalent isotropically radiated power (EIRP) of $EIRP$ = 18.43 dBm is achieved at f = 82.17 GHz for the monolithic IMPATT-transmitter chip with chip area A_{chip} = 4 mm^2. With simulated antenna gain G_{ant} = 7.35 dBi of the CPW patch antenna and measured transmission line loss of 0.57 dB, the DC-to-RF efficiency of the IMPATT transmitter achieves η_{DC-RF} = 4.36 % under the DC biasing condition of I_{bias} = 25 mA and V_{bias} = 13.4 V.

To effectively detect high frequency signals, Schottky diodes under fast MOTT operation were adopted as the basic rectifying element for the receiver modules. A half-wave rectifying antenna (rectenna) with chip area of A_{chip} = 60 mm^2 has been designed and implemented with an integrated serially-fed patch antenna array at f_R = 85 GHz. A full-wave bridge rectenna with chip area of A_{chip} = 4 mm^2 has been designed and implemented with an integrated bow-tie dipole antenna at f_R = 80 GHz. Due to the integrated Schottky diode with device area of A_d = 6 µm^2 under fast MOTT operation with high cut-off frequency f_{co} > 0.5 THz near zero biasing condition I_{bias} = 0 A, the conversion voltage ΔV_{conv} at f = 85 GHz can be widely tuned from ΔV_{conv} = 1 mV to ΔV_{conv} = 17 mV under biasing currents in range of 0.1 µA $\leq I_{bias} \leq$ 0.44 mA for the half-

wave design and at $f = 80$ GHz from $\Delta V_{conv} = 1$ mV to $\Delta V_{conv} = 40$ mV under biasing currents from $I_{bias} = 0.1$ nA to $I_{bias} = 0.6$ mA for the full-wave bridge design. According to measured conversion voltage value, dimension of rectenna chip, detecting range, the full-wave bridge design shows superior performance with high rectifying efficiency compared to the half-wave design.

As demonstrated in this dissertation, it is feasible to realize high performance integrated E-band transmitting-receiving module using silicon-based monolithic millimeter-wave integrated circuit (SIMMWIC) technology. With successful antenna integration both on the IMPATT-transmitter and the Schottky-receiver chip, the entire dimension is restricted within $A_{chip} = 4$ mm^2 without any performance trade-off. Compared with mainstream radio frequency complementary metal-oxide-semiconductor (RF CMOS) or bipolar transistor technology, the SIMMWIC technology offers a cost-effective option for various modern wireless applications.

CONTENTS

LIST OF ACRONYMS

2-D	Two Dimensional
2.5-D	Two-Point-Five Dimensional
3-D	Three Dimensional
AC	Alternating Current
Al	Aluminium
AoC	Antenna on Chip
BCB	Benzocyclobutene
BEOL	Back-End-Of-Line
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
B	Boron
CHF_3	Fluoroform
CMOS	Complementary Metal-Oxide-Semiconductor
CPS	Coplanar Strip
CPW	Coplanar Waveguide
CPWG	CPW with Ground
C-V	Capacitance-Voltage
CW	Continuous Wave
DC	Direct Current
DD	Double-Drift
DSI	Doping by Secondary Implantation
DUT	Device Under Test
EBL	Electron-Beam Lithography
EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
FET	Field-Effect Transistor

GaAs	Gallium-Arsenide
GaP	Gallium-Phosphor
GPIB	General Purpose Interface Bus
GSG	Ground-Signal-Ground
HD	High-Definition
HBr	Hydrogen Bromide
IC	Integrated Circuit
IF	Intermediate Frequency
IMPATT	Impact-Ionization Avalanche Transit-Time
InP	Indium-Phosphor
IOT/E	Internet of Things/Everything
ISM	Industrial, Scientific and Medical
I-V	Current-Voltage
LBE	Local Backside Etching
MBE	Molecular Beam Epitaxy
MOS	Metal-Oxide-Semiconductor
MIC	Microwave Integrated Circuit
NDR	Negative Differential Resistance
OS	Open-Short
PDK	Process Design Kit
PECVD	Plasma-Enhanced Chemical Vapor Deposition
Rectenna	Rectifying Antenna
RF	Radio Frequency
RIE	Reactive Ion Etching
Sb	Antimony
SCR	Space Charge Region
SD	Single-Drift
SEM	Scanning Electron Microscopy
Si	Silicon
SiGe	Silicon-Germanium
SIMMWIC	Silicon-based Monolithic Millimeter-Wave Integrated Circuit

SO	Short-Open
S-parameter	Scattering Parameter
SPICE	Simulation Program with the Integrated Circuit Emphasis
TEOS	Tetraethyl Orthosilicate
TLM	Transmission-Line Model
TRAPATT	Trapped Plasma Avalanche Triggered Transit
TRL	Thru-Reflect-Line
VLSI	Very-Large-Scale Integration
VNA	Vector Network Analyzer
WPAN	Wireless Personal Area Network

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LIST OF SYMBOLS

A	General Area (m^2)
A_{ant}	Antenna Area (mm^2)
A_d	Device Area (μm^2)
A_{chip}	Chip Area (mm^2)
A_j	Area of p-n Junction (μm^2)
$A(j\omega)$	Amplification Gain
C_j	Junction Capacitance (fF)
d	General Layer Thickness (nm)
d_{ADR}	Thickness of Avalanche & Drift Region Layer (nm)
d_{BL}	Thickness of Buried Layer (nm)
d_{Buf}	Thickness of Si Buffer Layer (nm)
d_{ff}	Far-Field Distance (cm)
d_{td}	Transmission Distance (m)
d_{TL}	Thickness of Top Layer (nm)
d_{sio_2}	Thickness of SiO_2 Film (nm)
d_{sub}	Thickness of Substrate (µm)
D	Largest Dimension of Antenna (m)
D_{detec}	Detecting Distance (cm)
E_g	Band Gap (eV)
E_m	Maximum Electric Field (V/m)
f	General Frequency (GHz)
f_0	Fixed Operation Frequency of Rectenna (GHz)
f_{amp}	Amplification Frequency (GHz)
f_{av}	Avalanche Frequency (GHz)
f_c	Center Frequency (GHz)

f_{co}	Cut-Off Frequency (GHz)
f_{max}	Maximum Oscillation Frequency of Transistor (GHz)
f_{mid}	Middle Frequency (GHz)
f_o	Oscillation Frequency (GHz)
f_{op}	Operating Frequency (GHz)
f_R	Radiation/Resonance Frequency of Antenna (GHz)
f_{sp}	Span Frequency (MHz)
f_T	Transit Frequency of Transistor (GHz)
$FSPL$	Free Space Path Loss (dB)
$FWHM$	Full-Width-at-Half-Maximum (GHz)
G	Conductance of IMPATT Diode (Ω^{-1} or Siemens)
G_{ant}	Antenna Gain (dBi)
G_{max}	Maximum Amplification Gain (dB)
G_P	Conductance of Junction (Ω^{-1} or Siemens)
$i(t)$	AC Current in Function of Time t (A)
$i_p(t)$	AC Parallel Junction Current in Rectification-Relevant Branch (A)
I	General Current (A)
I_{bias}	Biasing Current (mA)
I_j	DC Junction Current (A)
$Im\{Z_{IMPATT}\}$	Imaginary Part of IMPATT Diode Impedance (Ω)
I_s	Reverse Saturation Current or Leakage Current (A)
j	Imaginary Unit
J	Current Deisity (A/cm^2)
l	Pad Distance (μm)
l_{mesa}	Mesa Length (μm)
l_n	Depletion Width in n-Type Side for p-n Junction (nm)
l_p	Depletion Width in p-Type Side for p-n Junction (nm)
l_{pad}	Pad Length (μm)

l_T	Transfer Length or Effective Contact Length (µm)
L_j	Junction Inductance of IMPATT Diode (pH)
L_{match}	Length of CPW Matching Line (µm)
L_{short}	Length of Short-Ended CPW Resonator (µm)
N_A	Doping of Acceptor (cm^{-3})
N_b	Background Doping Level (cm^{-3})
N_{car}	Carrier Concentration (cm^{-3})
N_D	Doping of Donor (cm^{-3})
NFL	Noise Floor Level (dBm)
n_i	Intrinsic Carrier Concentration (cm^{-3})
P	General Power (mW or dBm)
P_{detec}	Detected Power (mW or dBm)
$EIRP$	Equivalent Isotropically Radiated Power (EIRP) (mW or dBm)
P_{exc}	RF Excitation Power (mW or dBm)
P_{out}	Output Power (mW or dBm)
P_p	Power in Rectification-Relevant Branch (mW or dBm)
P_{sig}	Signal Power (mW or dBm)
q	Elementary Charge: 1.602176620898…× 10^{-19} (Coulomb)
r	Resistance Value (Ω)
R	Negative Differential Resistance of IMPATT Diode (Ω)
RBW	Resolution Bandwidth (kHz)
R_c	Contact Resistance (Ω)
$Re\{Z_{IMPATT}\}$	Real Part of IMPATT Diode Impedance (Ω)
R_L	Load Resistance of IMPATT Diode (Ω)
R_p	Blocked Junction Resistance of Diode (Ω)
R_s	Series Resistance of Diode (Ω)
R_{sh}	Sheet Resistance (Ω)
R_{semi}	Semiconductor Resistance (Ω)
R_{tot}	Total Resistance (Ω)
$S_{N,N}$	Scattering Parameters of N Port System

t	Time (s)
T	Temperature (°C or K)
u	Real Part in Rectangular Coordinates System
$u(t)$	AC Voltage in Function of Time t (V)
$u_j(t)$	AC Junction Voltage (A)
v	Imaginary Part in Rectangular Coordinates System
v_s	Carrier Saturation Drift Velocity (cm/s)
V	General Voltage (V)
V_{appl}	Applied External Voltage (V)
V_{bi}	Internal Built-in Voltage (V)
V_{bias}	Biasing Voltage (V)
V_{br}	Breakdown Voltage (V)
VBW	Video Bandwidth (Hz)
V_{DC}	DC Output Voltage of Rectenna (V)
V_j	DC Junction Voltage (V)
$V_{r,N}$	Voltage Amplitude of Reflected Wave at Port N (V)
V_{RF}	DC Output Voltage of Rectenna under RF Excitation (V)
$V_{t,N}$	Voltage Amplitude of Transmitted Incident Wave at Port N (V)
V_T	Temperature Voltage (mV)
w_{lw}	Line Width of Technology (µm)
w_{mesa}	Mesa Width (µm)
w_{pad}	Pad Width (µm)
w_{dep}	Depletion Width of Space Charge Region (nm)
x	Reactance Value (Ω)
Y_p	Parallel Parasitic Admittance (Ω^{-1} or Siemens)
Z	Impedance (Ω)
Z_0	Normalizing or Reference Impedance: 50 (Ω)
$Z_{Amplifier}$	Impedance of Amplifier (Ω)
Z_{DUT_OS}	Impedance of Device under Test after Open-Short De-embedding (Ω)
Z_{DUT_SO}	Impedance of Device under Test after Short-Open De-embedding (Ω)

$Z_{Feedback\ Network}$	Impedance of Feedback Network (Ω)
Z_{IMPATT}	Impedance of IMPATT Diode (Ω)
Z_{in}	Input Impedance (Ω)
Z_{MEAS}	Impedance of Raw Measurement (Ω)
Z_n	General Normalized Impedance (Ω)
Z_{OPEN}	Open-Structure Impedance (Ω)
Z_s	Serial Parasitic Impedance (Ω)
Z_{SHORT}	Short-Structure Impedance (Ω)
α	Ionization Coefficient per Unit Length
α'	Derivative of Ionization Coefficient with Respect to Electrical Field
$\beta(j\omega)$	Transfer Function
Γ	Reflection Coefficient
Δf	Frequency Shift (GHz)
ΔI_{bias}	Biasing Current Tolerance (mA)
ΔV_{conv}	DC Conversion Voltage of Rectenna (mV)
ΔV_{br}	Breakdown Voltage Difference (V)
$\Delta\varphi\{A(j\omega), \beta(j\omega)\}$	Phase Shift through Amplifier and Feedback Network (°)
ε	Permittivity of Material (F/m)
ε_0	Permittivity of Vacuum: 8.854187817…× 10^{-12} (F/m)
ε_r	Relative Permittivity of Material
$\varepsilon_{r,Si}$	Relative Permittivity of Silicon: 11.7 – 11.9
$\varepsilon_{r,SiO2}$	Relative Permittivity of Silicon-Dioxide: ~ 4.1
η	Ideality Factor of Diode: 1 – 2
η_{DC-RF}	DC-to-RF efficiency (%)
θ	Rotation Angle in 3-D Polar Coordinates System (°)
λ	Wavelength (mm)
μ_n	Mobility of Electrons in Semiconductor Material (cm^{2}·V^{-1}·s^{-1})
μ_p	Mobility of Holes in Semiconductor Material (cm^{2}·V^{-1}·s^{-1})
ρ	Radius of Vector or Magnitude in 2-D Polar Coordinates System
ρ_{BL}	Specific Resistivity of Buried Layer (Ω·cm)

ρ_c	Specific Contact Resistance ($\Omega \cdot cm^2$)
ρ_s	Specific Resistivity of Material ($\Omega \cdot cm$)
ρ_{TL}	Specific Resistivity of Top Layer ($\Omega \cdot cm$)
φ	Angle of Vector/ Rotation Angle in 2-/3-D Polar Coordinates System (°)
$\varphi_{AC(V,I)}$	Phase Delay between Voltage and Current of AC Signal (°)
ω	Angular Frequency (Hz)
ω_0	Fixed Operation Angular Frequency (Hz)
ω_p	Parallel Cut-Off Angular Frequency (Hz)
$\omega_{p,max}$	Optimum Parallel Cut-Off Angular Frequency (Hz)
ω_s	Serial Cut-Off Angular Frequency (Hz)

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Chapter 1. INTRODUCTION

1.1 AIM AND MOTIVATION

Since the first wireless telephone message was successfully transmitted over 213 meter distance on April 1st, 1880 by American inventor Alexander Graham Bell and his assistant Charles Summer Tainter using the photophone [1]-[2], our world has been changed significantly by this "magical" wireless technology. Taking the experimental verification of electromagnetic (EM) waves (Hertzian waves or aetheric waves) by Heinrich Hertz in 1888 [3] as solid theoretical foundations for academic researches, the transatlantic transmission experiment demonstrated by Guglielmo Marconi in 1902 [4] fairly sparked the worldwide attention on the wireless communication and broadcasting applications in people's daily lives.

With the great success in semiconductor technology as bipolar junction transistors (BJT) [5], metal-oxide-semiconductor (MOS) field-effect transistors (FET) [6]-[7], and integrated circuits (ICs) technique [8] the wireless systems can be implemented in a low-profile, low-power, and low-cost fashion. This opens a new era of diverse modern wireless applications such as announced 5G millimeter-wave communication with larger bandwidth, higher data rate to meet the increasing demands of high-definition (HD) multimedia data transmission or short distance detecting/sensing/imaging applications required by recently emerging internet of things/everything (IOT/E), radar for civil applications (distance control for automobiles or unmanned aerial vehicles), gesture control/capture in wearable electronics, and biomedical/vital-sign detection (lab-on-chip, breath monitoring).

Strongly driven by these modern wireless applications, the commercialized transistor-based complementary MOS (CMOS) and bipolar CMOS (BiCMOS) technologies have been well developed and successfully applied for radio frequency (RF), micro-/millimeter-wave, or even

Terahertz regimes. However, system-level integration stays still challenging for high-performance wireless applications with $f \geq 60$ GHz due to the following two factors: 1. output power decreases dramatically with increasing frequency ($\sim f^{-2}$), which physically limits the maximum achievable output power level of transistor-based power sources (e.g. silicon-based (Si-based) power amplifier $P_{out} =\sim 20$ dBm in the E-band (60 GHz $\leq f \leq$ 90 GHz) and the W-band (75 GHz $\leq f \leq$ 110 GHz) [9]). For other more powerful two-terminal power sources such as impact-ionization avalanche transit-time (IMPATT) diode, Gunn diode, or resonant tunneling diode (RTD), their process design kits (PDK) are rare to be found in standard component libraries of CMOS/BiCMOS technologies, since front-end-of-line (FEOL) processes are mainly optimized for CMOS FETs or silicon-germanium (SiGe) hetero-junction bipolar transistors (HBTs). Thus above mentioned two-terminal alternatives are mostly only applied as discrete devices rather than monolithically in millimeter-wave or terahertz systems; 2. the construction of back-end-of-line (BEOL) processes in CMOS/BiCMOS technologies is mainly concerned and optimized for mechanical robustness of interconnects (residual stress as low as possible) over large-sized wafer, which quietly marginalizes the high-efficiency antenna design and integration. Even with the bottom-metal-layer isolation from the lossy low-resistivity high-permittivity Si substrate, an efficient integration of high-performance on-chip antenna is limited by high ohmic loss, unwanted surface waves, narrow bandwidth, and many other constraints.

In regards to the introduced shortcomings of mainstream CMOS/BiCMOS technologies, this dissertation conducts a successful attempt for designing and implementing a transmitter and a receiver with two-terminal devices (IMPATT diode for transmitter; Schottky diode for receiver) and integrated antennas in E-band regime by applying an elementary Si-based monolithic millimeter-wave integrated circuit (SIMMWIC) technology.

IMPATT diode has been well known as the most powerful microwave source generator, since the concept was proposed by W. T. Read of Bell Laboratories in 1956 and soon widely proved in late 1950s. Discrete Si IMPATT diodes can generate power at lower microwave frequencies up to several Watts in continuous wave (CW) mode or even tens of Watts in pulsed mode [10]. However, the rarely found monolithic IMPATT components [11]-[16] do not show apparently the specialty to efficiently generate millimeter-wave power due to the following factors in monolithic design scenarios: 1. to fabricate IMPATT diodes with matched low on-chip impedance level ($Z < 200\ \Omega$)

at desired frequency window is challenging; 2. enormously reduced tuning possibility for passive structures; 3. low Q-factor of on-chip resonator; 4. low thermal robustness of miniaturized device (high current density). Generally speaking, the monolithic design window for efficient millimeter-wave power generation is much narrower compared with the conventional discrete design. The IMPATT transmitter design in this dissertation has overcome the above mentioned four challenges and successfully demonstrated the high output power property of IMPATT diode in monolithic design scenario.

Schottky diode is considered as fastest rectifying element. Due to its "majority carrier" property [17], the cut-off frequency (f_{co}) of Schottky diode can be well achieved in the Terahertz regime (0.3 THz $\leq f \leq$ 3 THz) [18]. With integrated antenna, two types of Schottky rectifying antenna (rectenna) have been implemented as receiver. For the Schottky receiver in this dissertation, both half- and full-wave concepts have been implemented each with an integrated serial-fed patch antenna array and a broadband bow-tie antenna. According to measurement results, the full-wave bridge concept shows superior performances over half-wave design in terms of chip dimension, conversion voltage, and detecting range.

SIMMWIC technology has the greatest advantage of high-resistivity Si substrate (ρ_s> 1000 Ω·cm), which leads to much less resistive loss in substrate and offers larger design freedom for high-efficiency antenna integration compared with available BEOL processes in mainstream CMOS/BiCMOS technologies. In addition, complex post-fabrication processes become un-necessary for achieving reasonable efficiency of integrated antenna.

In March 2016 the global semiconductor industry officially announced the coming end of the famous Moore's law [19], which has been leading a semiconductor revolution since the 1960s. In fact, academia and corporate researchers have seriously been seeking possible solutions to the so-called "Moore's wall" already since the beginning of the 21st century. "More-Moore" developments by further shrinking the technology node have been carefully braked for classical microprocessors, memories, and digital logic applications on mass commercial market. On the other side, "More-Than-Moore" activities grow rapidly in these years for applications such as high-frequency analog front-ends, power electronics, photonics, and nano-electronics. In a nutshell, the potential of the well-established semiconductor technologies will be more focused and released in those fields or markets, where performance (quality) has more priority than yielding issue (quantity). This trend will end the traditional downscaling (technology node) competition, which only large companies could afford. Academia researchers regain chances and attentions to “play the game” under new rules more emphasized with innovative ideas as demonstrated in this dissertation.

1.2 OUTLINE OF DISSERTATION

Figure 1.1 shows the chapter-structure of this dissertation.

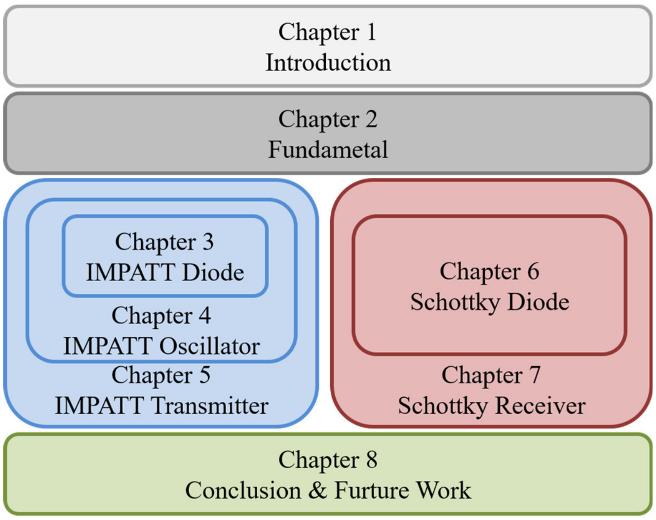


Figure 1.1: Chapter structure of the dissertation.

Chapter 2 summarizes all fundamentals which are necessary for better understanding of specified technical implementations from chapters 3 to chapter 7.

Chapter 3 begins with the introduction of the IMPATT diode. The IMPATT functionality in frequency domain is qualitatively analyzed from device physics aspect, which guides and finalizes the molecular beam epitaxy (MBE) growth of the appropriate IMPATT layer stacks required by the E-band circuit design. The fabricated IMPATT diodes are then characterized in direct current (DC) mode and in alternating current (AC) mode regarding to small-signal S-parameters (“S” refers to “Scattering”, section 2.5). From these characterization results, relevant parameters related to device performance and to technological information can be extracted. An accurate lumped-element model is established to describe IMPATT functionality in a straightforward way. The temperature effect on device performance under the CW IMPATT operation is extensively studied. This study verifies the thermal robustness of the applied IMPATT device in objective way.

In chapter 4 the design principle, realization and characterization of E-band IMPATT oscillators are introduced in detail. On-chip passive components are implemented only with simple coplanar waveguide (CPW) lines. Together with an active element IMPATT diode and a load with Z_{load}= 50 Ω, a complete oscillator loop is built up. Oscillation frequency can be quantitatively verified through amplification spectrum measurement using vector network analyzer (VNA, section 2.5) to finalize oscillator designs in the desired frequency range. Small-signal-based Kurokawa condition and Barkhausen's criteria for steady-state oscillation are verified for instance at $f = 70$ GHz by "assembling" measurement data of all separate oscillator parts (short-ended CPW resonator with length L_{short} =340 µm; IMPATT diode with A_d= 40×2 μm^2; CPW matching line with length L_{match} =100 µm). The measured amplification spectra of this corresponding design showed consistently the maximum gain at f_{amp} =70.54 GHz within the predicted biasing range. Different combination of design parameters (diode dimension, length of short-ended CPW resonator, length of CPW matching line) offers a wide tuning possibility of the oscillation frequency, which covers almost the entire E-band.

Chapter 5 focuses on the implementation and characterization of the monolithic IMPATT transmitter. A coplanar patch antenna with radiation frequency $f_R = 82.5$ GHz is designed and simulated using three dimensional (3-D) EM tool CST microwave studio. Combined with an oscillator with $f_{op} = 82$ GHz (short-ended CPW resonator with length $L_{short} = 260$ µm; IMPATT diode with A_d= 20×2 µm^2; CPW matching line with length $L_{match} = 150$ µm), the monolithic IMPATT transmitter can radiate the power exactly at $f_{op} = 82.17$ GHz under DC biasing condition of $I_{bias} = 25$ mA with $V_{bias} = 13.4$ V, which is characterized in an anechoic chamber. Through a link budget calculation the equivalent isotropically radiated power (EIRP) of the finalized IMPATT transmitter achieves $P_{EIRP} = 18.43$ dBm. With simulated antenna gain of $G_{ant} = 7.35$ dBi and measured transmission line loss of 0.57 dB, the DC-to-RF efficiency reaches $\eta_{DC-RF} = 4.36$ %. The measured H-plane radiation pattern of the transmitter chip agrees well with antenna simulation results. Compared with other published monolithic IMPATT transmitter designs, the finalized IMPATT transmitter demonstrates the highest output power in E-band regime to the date and has yet strong potential for further improvement.

Schottky diode with MOTT operation (named after Nevill Mott [77]-[78], section 2.7) is discussed in chapter 6 linked to the corresponding MBE layer stacks. The speciality and advantage of MOTT diode for high frequency rectification application compared to normal Schottky diode are explained. Standard current-voltage (I-V) DC characterization is carried out to extract diode series resistance and ideality factor. With S-parameter measurement and lumped-element modeling relevant parameters are extracted to estimate the biasing-dependent cut-off frequency in a real rectification scenario. Analysis of parallel cut-off frequency for its impact on the rectifying efficiency is discussed, too.

In chapter 7 the implementation of half-wave and full-wave Schottky rectenna as receiver is systematically presented. As two different topologies microstrip with serial-fed patch antenna and with bow-tie dipole antenna are designed and fabricated. The conversion voltage spectra $\Delta \mathrm{V}_{con}(f)$ are characterized as the key parameter for rectenna measurement. At desired frequencies the characteristics of conversion voltage over biasing currents $\Delta \mathrm{V}_{con}(I_{bias})$ are well understood and explained. Additionally a detecting range study is performed on the superior full-wave bridge rectenna with f_{op} = 80 GHz. Finally the conversion voltage over RF excitation power at different frequencies $\Delta \mathrm{V}_{con}(P_{exc})@f$ is performed without observing power saturation at f_{op} = 80 GHz under maximum available excitation power P_{exc} = -5 dBm, which confirms the high efficiency property of the full-wave bridge design, too.

Chapter 8 will conclude the entire works of this dissertation, based on which several promising outlooks for future research are proposed.

1.3 MAIN CONTRIBUTIONS

The main contributions of this dissertation are the following:

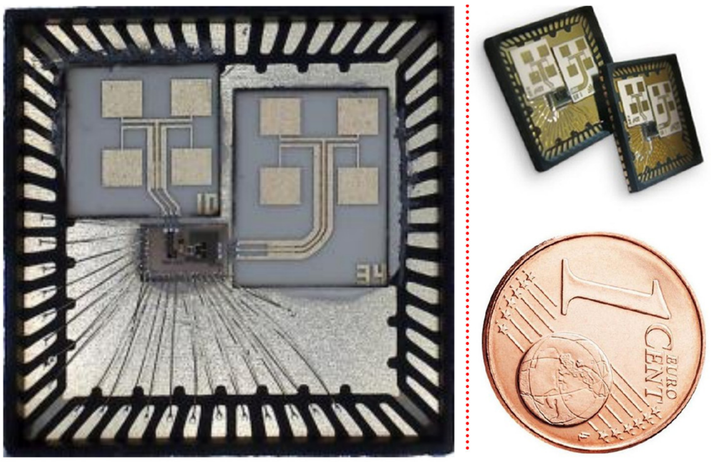
- Demonstration of complete design flow from material growth, device fabrication + selection to circuit implementation of E-band monolithic IMPATT transmitter [20] and Schottky receiver [26] using SIMMWIC technology.
- Monolithic E-band oscillator design by applying easily-implemented CPWs as passive network and embedded IMPATT diode as active device [21].
- Experimental verification and confirmation of Kurokawa condition and Barkhausen's criteria for steady oscillation using small-signal S-parameter data to finalize IMPATT oscillator design with the help of amplification spectrum measurement [21], [25].
- Systematic characterization (I-V, C-V, Transmission-line Model (TLM), S-parameter), evaluation, and small-signal lumped-element modeling for IMPATT [24], [28] and Schottky diodes [26].
- Establishment of the S-parameter based device-level C-V measurement for small-dimensional two-terminal p-i-n structural devices, e.g. single-drift IMPATT diode in real millimeter-wave application scenarios [22].
- Impact of key parameters on IMPATT functionality with the help of measurement based lumped-element modeling [23], [24].
- Study of rectification mechanism with Schottky diode under MOTT operation [27].
- Establishment of standard characterization procedure of IMPATT transmitter and Schottky rectenna [20], [26].
- Design and drawing of mask set “IHT2015: SIMMWIC-IMPATT-Tx” (see Appendix-A).
- Successful completion of the corresponding project (Grant-N.O. KA 1229/11-1: Monolithisch integrierter mm-Wellen Radarchip für Anwendung in der Medizin) financed by German Research Foundation (Deutsche Forschungsgemeinschaft/ DFG).

Chapter 2. FUNDAMENTAL

2.1 SILICON-BASED MONOLITHIC MILLIMETER-WAVE INTEGRATED CIRCUIT (SIMMWIC) TECHNOLOGY FOR WIRELESS MILLIMETER-WAVE APPLICATIONS

Since the invention of the integrated circuit in 1958 [8], much progress had been made to realize circuits or even systems in a miniaturized way, especially related to high complexity and to high-speed, high-frequency performance. Thus, the era of microwave integrated circuits (MICs) was opened in 1964. Prior to that time, nearly all microwave components were built with waveguides, coaxial or strip-line cables. Thereby the microwave systems were bulky and rather expensive due to the wavelength-determined small size and the corresponding highly precise fabrication tolerance. After decades of fighting against high-temperature induced lossy substrates during the process sequences [29], SIMMWIC was then officially announced firstly by P. J. Stabile and A. Rosen in 1984 [30]. Years after that the progress on high-resistivity ($\rho_s > 1000$ Ω·cm) Si substrate technology [31] and low-temperature MBE growth technique [32] further enhanced the development of SIMMWIC technology. A mature form of SIMMWIC has been available since 1994 [33].

In the meantime the tremendous progresses of the high-speed Si technologies, e.g. SiGe HBT towards higher transistor cut-off frequencies ($f_T/f_{max} = 300/500$ GHz [34]) have been made continuously. This makes Si technology with its high integration potential and low fabrication cost a promising competitor of the conventional “fast” III-V technologies (as gallium-arsenide (GaAs), indium-phosphide (InP)) in RF and micro-/millimeter-wave applications [35]. Taking an overview at the millimeter-wave wireless applications nowadays as wireless personal area networks (WPANs) at $f_{op} = 60$ GHz, automotive radar at $f_{op} = 77$ GHz, imaging at $f_{op} = 94$ GHz, and other diverse applications developing at license-free industrial, scientific and medical (ISM) bands of $f_{op} = 122$ GHz, $f_{op} = 124$ GHz, and $f_{op} = 245$ GHz, it is clearly realized that almost all building blocks for wireless transceiver systems operating in the millimeter-wave frequency range can be monolithically implemented in Si technologies with the expectation of high electrical performance in a low-profile, low-power consumption, low-cost fashion. However, the monolithic system-level integration for wireless applications remains still challenging because of the lack of high-quality passive components operating in millimeter-wave range, especially the antennas and their interconnects (Figure 2.1 [36]). The standard mainstream SiGe CMOS or BiCMOS technologies usually include five to seven metal layers with silicon-dioxide (SiO2) ($\varepsilon_{r,SiO_2} \approx 4.1$) in between defined as BEOL. Due to increase of unwanted residual stress over large wafer surface ($A \geq 8$ inches) the distance between the top metal layer and the bottom one is usually limited within 20 μm, which is too thin to design a high efficiency antenna with the bottom metal layer as ground shielding because of high ohmic loss. Additionally the bandwidth is extremely limited. However, without ground shielding to isolate the antenna from the Si substrate ($\varepsilon_{r,Si} = 11.7 - 11.9$) beneath the bottom metal layer, strong substrate modes are excited, which causes much loss in low-resistive Si substrate (5 Ω·cm $\leq \rho_s \leq$ 60 Ω·cm). Thus the efficiency of the antenna is again significantly degraded [37].



TRX_120_01: 120 GHz Highly Integrated IQ Transceiver With Antenna in Package
Silicon Radar GmbH Product
IC by IHP-Microelectronics SG13S SiGe BiCMOS technology

Figure 2.1: Hybrid system-level integration example of a SiGe 122 GHz IQ transceiver IC with bonding interconnects to patch antenna arrays on Rogers Ultralam 3850 liquid crystalline polymer substrate (www.siliconradar.com/datasheets/160721_Datenblatt_TRX_120G.pdf).

Compared with mainstream CMOS/BiCMOS the SIMMWIC technology has the greatest advantage of the high-resistivity Si substrate ($\rho_s > 1000$ Ω·cm), which can suppress the resistive loss of substrate modes sufficiently. This enables an implementation of millimeter-wave circuits and antennas together with relatively simple metallization process. The bulk substrate can be polished comfortably down to several hundreds of micrometer, which is thinner than the millimeter-wave cut-off thickness of the substrate mode TE_0 . In addition the backside metallization offers a simple but efficient ground shielding solution (Figure 2.2: a) to design microstrip patch antenna with reasonable efficiency [38]. The flexibility to design coplanar patch antenna using SIMMWIC technology is available, too (Figure 2.2: b) [39]. The backside metallization is not necessary anymore, because the chip could be mounted up-side down due to higher radiation through the high-permittivity Si substrate [14], [40].

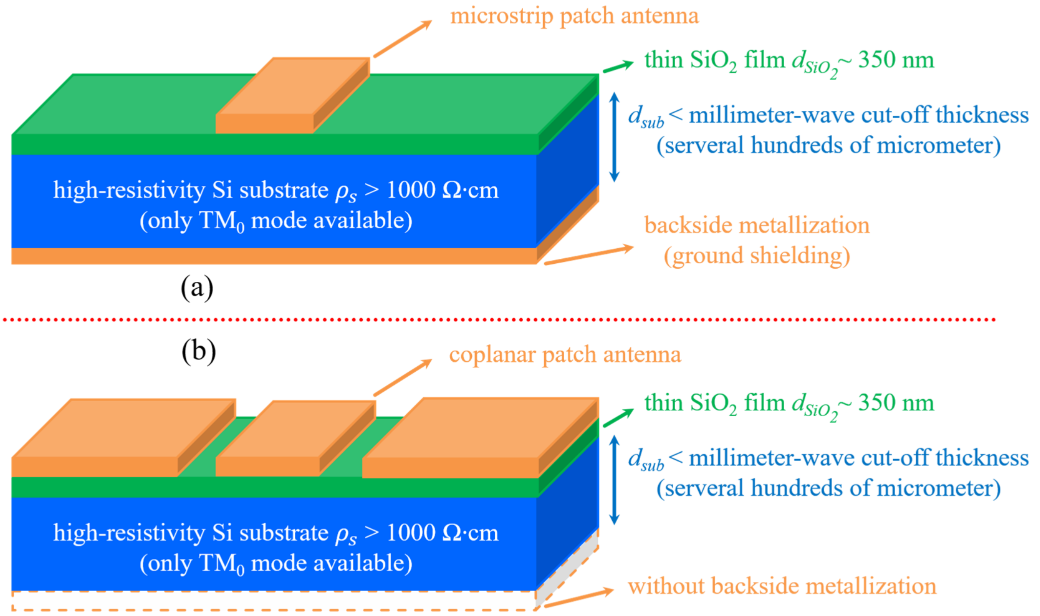


Figure 2.2: Two design possibilities of integrated antennas in SIMMWIC technology with elementary metallization process: microstrip patch antenna (a) and coplanar patch antenna (b).

With the design freedom brought by the high-resistivity ($\rho_s > 1000$ Ω·cm) substrate it is much comfortable to efficiently integrate RFICs and antennas together in SIMMWIC technology without complex post-fabrication processes, e.g. local backside etching (LBE) [41] or deposition of thick benzocyclobutene (BCB) layers [42] in extra BEOL process etc. Thus interconnects loss can be sufficiently minimized and the monolithic system-level integration for millimeter-wave wireless applications becomes feasible.

2.2 FABRICATION PROCESS FLOW AND DEVICE INTEGRATION

The device layer stacks were grown in-house with the MBE technique, which offers an accurate growth profile both in doping level and in layer thickness with a temperature budget $T < 600$ °C. For the in-house Si MBE technology, boron (B) is adopted for p-type (acceptor) and antimony (Sb) for n-type (donor) dopants. A p-type high-resistivity ($\rho_s > 1000$ Ω·cm) Si (100) substrate with thickness of $d_{sub} = 500$ µm was chosen, on which a heavily doped ($N_A \sim 10^{20}$ cm^{-3}) buried layer with thickness of 300 nm $< d_{BL} < 400$ nm was grown. Depending on desired device property other necessary layers could be grown. Figure 2.3 shows the layer stacks each of p-i-n structural IMPATT diode and n-type Schottky diode, which are two one-port devices extensively studied in chapter 3 and chapter 6 of this dissertation.

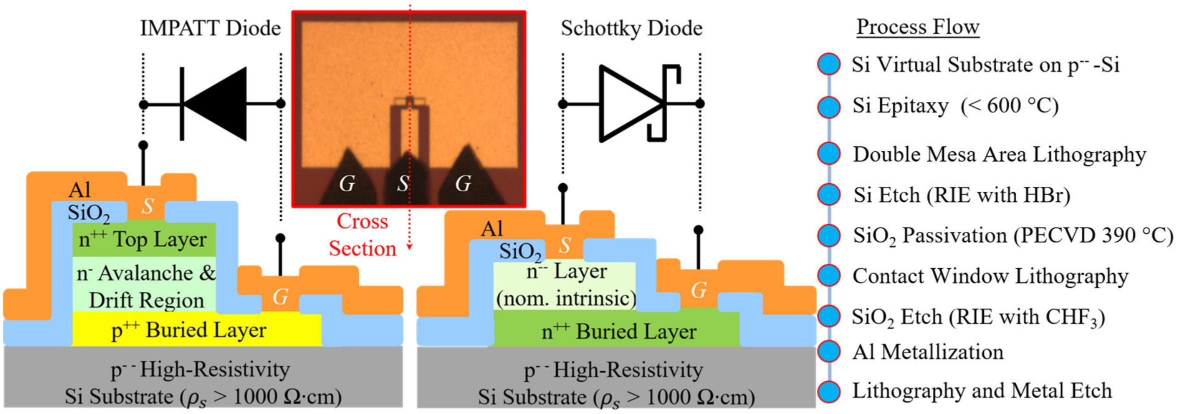


Figure 2.3: MBE layer stacks of IMPATT & Schottky diodes and in-house process flow for device/circuit integration (inset: fabricated diode embedded in CPW RF contact pads with a GSG configuration).

For IMPATT layer stacks, a heavily p-type doped ($N_A \sim 10^{20}$ cm^{-3}) buried layer serves as good ohmic contact to the aluminium (Al) ground line and meantime forms a p-n junction together with lightly n-type doped ($N_D \sim 10^{17}$ cm^{-3}) layer of avalanche and drift region above. A heavily n-type doped ($N_D \sim 10^{20}$ cm^{-3}) top layer with thickness $d_{TL} = 200$ nm ends up the entire MBE layer growth eventually.

For Schottky layer stacks, a heavily n-type doped ($N_D \sim 10^{20}$ cm^{-3}) buried layer serves only as good ohmic contact to the Al ground line. An n^{--} doped layer with a background doping level of N_b~10^{15} cm^{-3} was then grown, which forms the Schottky contact together with Al signal line at their interface.

Device fabrication and integration were carried out with process temperature $T \leq 390$ °C (Figure 2.3: Process Flow). A double-mesa structure for good device isolation was fabricated after lithography and reactive ion etching (RIE) with the hydrogen bromide (HBr) process. Low temperature ($T = 390$°C) SiO_2 as an isolation layer was deposited in a plasma-enhanced chemical vapor deposition (PECVD) chamber using a tetraethyl orthosilicate (TEOS) precursor. Contact window etching was performed in RIE using a fluoroform (CHF_3) process after lithography. Finally, sputter deposition of the contact metal (Al) and dry etching are employed to construct the device, which is embedded in CPW RF contact pads with a ground-signal-ground (GSG) configuration (Figure 2.3: inset).

2.3 FUNCTIONAL PRINCIPLE OF IMPATT DIODE

The IMPATT concept was first proposed by W. T. Read in 1958 as “high-frequency, negative-resistance diode” [43], which can be applied as active device in oscillator design [44] to generate high frequency power under certain DC biasing condition. Different to any other diodes the IMPATT diode operates under reverse-biased condition near the breakdown voltage, which enables sufficiently strong electrical fields to induce the carrier (electrons and holes) multiplication near the p-n junction interface due to the avalanche effect. The carriers arisen from the avalanche process drift then through intrinsic or lightly doped semiconductor region towards electrode under applied DC electrical fields. According to Read’s theory, the negative IMPATT resistance appears owing to the phase delay of $\varphi_{AC(V,I)} = 180°$ between AC voltage and current, which is contributed by both the injection delay during the avalanche mechanism and the optimum transit-time delay caused by the drift mechanism [45].

Besides the above mentioned IMPATT mode, there are several other modes of the so-called “avalanche diodes” [46], e.g. trapped plasma avalanche triggered transit (TRAPATT) mode [47]-[50], parametric mode, and thermal modes. The thermal modes induce a self-destruction mechanism (filaments formation) due to large temperature swing through the device, which is actually not usable by designer in reality. The TRAPATT and parametric modes need large voltage swings across the diode, which means, both are large-signal operative. Only IMPATT mode presents small-signal negative differential resistances (NDRs) over a broad frequency band, which can be well characterized by applying VNA-assisted small-signal S-parameter measurement. Therefore, in this chapter the p-n structural diodes for IMPATT mode operation are extensively studied and discussed from device layer growth, fabrication to characterization concretely aiming at the monolithic design of E-band IMPATT oscillator and transmitter, respectively.

2.4 CONCEPT OF TRANSMISSION-LINE MODEL (TLM) MEASUREMENT

Since the TLM method was originally proposed by W. Shockley in 1964, practically improved by G. K. Reeves and H. B. Harrison in 1982 [51], this method has been widely employed to extract the quality of ohmic contact, electrical properties of semiconductor films, and electrically activated doping concentration in semiconductor materials.

The measured TLM structures of IMPATT samples are illustrated as an example in Figure 2.4 each for nominally N_A~10^{20} cm^{-3} doped buried layer and N_D~10^{20} cm^{-3} doped top layer. I-V characteristics of the two adjacent Al contact pads with distances (e.g. l_{1-5} are measured firstly, from which the total resistances $R_{tot_{1-5}}$ can be extracted as the slope of the I-V characteristics.

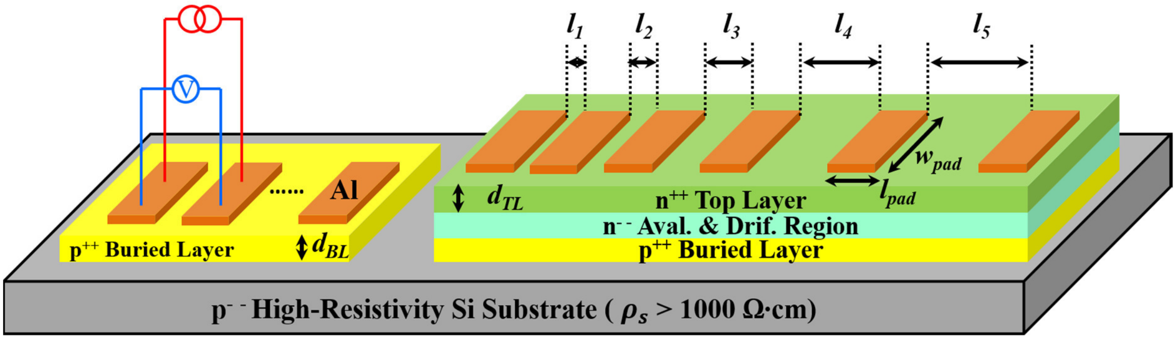


Figure 2.4: TLM structures and measurement setup for extracting contact parameters and doping states of the buried and top layer for IMPATT samples.

The directly measured total resistance R_{tot} consists of the contact resistance R_c to two adjacent Al pads and the semiconductor resistance R_{semi}. The semiconductor resistance R_{semi} can be expressed further as

$$R_{semi} = \rho_s \cdot \frac{l}{d \cdot w_{pad}} \qquad , \tag{1}$$

with ρ_s the specific resistivity of the semiconductor material, l the pad distance, d the layer thickness, and w_{pad} the pad width. Since the sheet resistance R_{sh} is defined as

$$R_{sh} = \frac{\rho_s}{d} \quad , \tag{2}$$

we have then the final expression of R_{tot} as following

$$R_{tot} = 2 \cdot R_c + R_{sh} \cdot \frac{l}{w_{pad}} \quad . \tag{3}$$

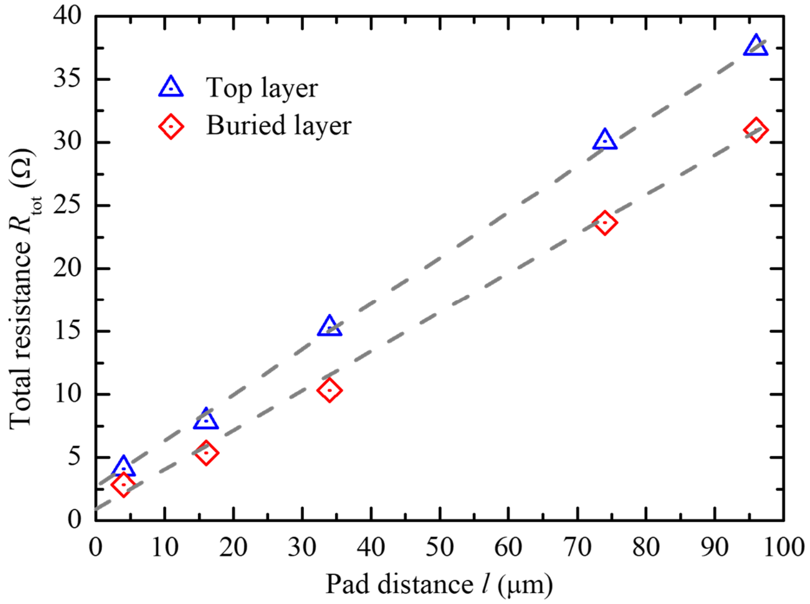


Figure 2.5: Total resistance R_{tot} vs. pad distance l extracted by TLM measurement for buried layer and top layer of one investigated sample.

After plotting the measured total resistances ($R_{tot_{1-5}}$) over the corresponding distances (l_{1-5}), the characteristics each of buried layer and top layer on one investigated sample are shown in Figure 2.5. A linear fit should be observed as an indicator of a good ohmic contact. From equation (3) the contact resistance R_c can be easily extrapolated from the graphics as the half value of the y-intercept:

$$R_c = \frac{R_{tot}(l = 0)}{2} \quad . \tag{4}$$

The sheet resistance R_{sh} can be extracted from the graphics as the product of the slope and pad width w_{pad}, too. With the layer thickness d, the specific resistivity ρ_s of the semiconductor material can be extracted using equation (2). In practice an overetch (10 % -15 %) is usually performed to ensure electrical contact down to buried layer for device functionality, this thickness variation must be considered by the buried layer thickness d_{BL}. But the overetch will not affect the measured top layer thickness d_{TL} at all (Figure 2.4). To link the extracted specific resistivity ρ_s with the doping concentration (N_A for acceptor; N_D for donor) ignoring the minority effect and under the assumption of 100 % activated dopants we have:

$$\rho_{BL} \cong \frac{1}{q \cdot \mu_p \cdot N_A} \tag{5}$$

for p-type buried layer, and

$$\rho_{TL} \cong \frac{1}{q \cdot \mu_n \cdot N_D} \tag{6}$$

for n-type top layer. With literature values [52] of the majority carrier mobility in B-doped (p-type buried layer) and Sb-doped (n-type top layer) Si within doping range of 10^{19} cm^{-3}$< N_{A\ or\ D} <$$10^{20}$ cm^{-3}, the plot of specific resistivity ρ_s over doping concentration N_A (p-type) or N_D (n-type) each for buried layer and top layer can be obtained (refer to subsection 3.2.3 for IMPATT samples; subsection 6.2.2 for Schottky samples). This gives us an objective impression of the discrepancy between the aimed nominal doping concentration (e.g. 10^{20} cm^{-3}) and the electrically activated carrier concentration N_{car} in reality. Compared with the classic four-point probe [53] method to extract ρ_s, TLM can reflect additionally the quality of technological fabrication processes.

To finally obtain the specific contact resistance ρ_c, the transfer length l_T (also known as effective contact length for the required distance by current flow into or out of the ohmic contact) can be extracted from the graphics in Figure 2.5 conveniently as:

$$l_T = -\frac{l(R_{tot} = 0)}{2} \quad , \tag{7}$$

with $l(R_{tot} = 0)$ the x-intercept of linear extrapolated curves according to equation (3). Under a good ohmic contact condition l_T<< l_{pad} (l_{pad}= 80 µm in our case), the specific contact resistance is defined as:

$$\rho_c = \frac{(R_c \cdot w_{pad})^2}{R_{sh}} \quad . \qquad (8)$$

For the in-house cleanroom technology the specific contact resistance ρ_c = 10^{-6} – 10^{-5} $\Omega \cdot cm^2$ is well achieved, which can be much improved to ρ_c =10^{-8} – 10^{-7} $\Omega \cdot cm^2$ by the commercialized industrial technologies.

2.5 THEORY OF SCATTERING PARAMETERS (S-PARAMETER)

Owing to the frequency regime 30 GHz $\leq f \leq$ 300 GHz in the millimeter-wave world, with corresponding electrical wavelength in free space 1 cm $\geq \lambda \geq$ 1 mm (for monolithic design on Si substrate, the effective guided wavelength goes even to sub-millimeter), the classical circuit theory is not accurate enough to explain microwave phenomena. The fact is that the important parameters of lumped circuits such as voltages and currents cannot be defined for a general case anymore, because the circuit dimensions are on the same level of the electrical wavelength. According to Maxwell's equations [54], the intuitive expression is that the voltage or the current across the circuit changes much with both time and position (basically due to the phase variation), which is far beyond the valid condition of the classical circuit theory.

The concept of "scattering matrix" was first proposed by K. Kurokawa of Bell Labs in 1965 [55] to describe the complex microwave networks in the behavior of a simple "black box". This concept skips the tough analysis of the complex microwave networks and offers a convenient solution for the characterization of microwave components in a unique way. Nowadays, this concept is well known as "S-parameters" ("S" refers to "Scattering") and it is widely applied for most microwave designs.

Generally speaking, the S-parameter is a mathematical description that quantifies the high frequency energy propagation through a multiport network. For instance, incident signals touch on one port, and part of them are reflected back out of this port immediately, while part of them are scattered further into the network and finally exit from other ports. Some of signals may even disappear in the form of heat loss or EM radiation. Some of the signals may also be amplified or stored. The “scattering matrix” for an N-port network contains N^2 coefficients (S-parameters), each one representing an input-output path of all possible high frequency energy flows in the network.

$$\begin{pmatrix} V_{r,1} \\ V_{r,2} \\ \cdot \\ \cdot \\ \cdot \\ V_{r,N} \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & S_{22} & \dots & S_{2N} \\ \dots & \dots & \dots & \dots \\ S_{N1} & S_{N2} & \dots & S_{NN} \end{pmatrix} \cdot \begin{pmatrix} V_{t,1} \\ V_{t,2} \\ \cdot \\ \cdot \\ \cdot \\ V_{t,N} \end{pmatrix} \quad , \qquad (9)$$

where $V_{r,N}$ is the voltage amplitude of the reflected wave at port N and $V_{t,N}$ the voltage amplitude of the transmitted incident wave at port N.

Both the magnitude and phase of the input signals are changed by the network. Hence, S-parameters are complex numbers. Depending on the design demands, S-parameters could be expressed in other forms, e.g. Z-parameters (impedance-matrix), Y-parameters (admittance-matrix), H-parameters (hybrid-matrix), ABCD-parameters (chain- or cascade-matrix), or T-parameters (chain-transfer- or chain-scattering-matrix) by applying linear algebraic matrix transformation [56].

To measure the S-parameters of the microwave components, a VNA [57] offered by commercial companies, e.g. Keysight (former Agilent), Anritsu, Rohde & Schwarz etc. is usually employed. This is a small-signal characterization method, which means the signals are small enough (typically -20 dBm $\leq P_{sig} \leq$ -10 dBm) and does not change the linearity of the measured network itself. The VNA is designed to extract the magnitude and phase information of the transmitted and reflected waves from the measured active or passive network under small-signal excitations. S-parameter characterization in this dissertation was performed with an in-house Anritsu ME7808C Broadband (0.04 GHz $\leq f_{op} \leq$ 110 GHz) VNA system.

For one-port network (Figure 2.6) equation (9) is specified as follows:

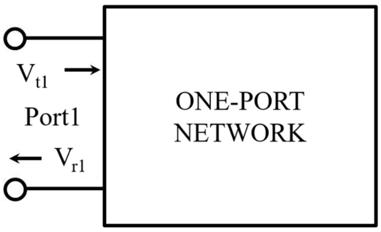


Figure 2.6: One-port network with the voltage amplitude of reflected wave $V_{r,1}$ and the voltage amplitude of the transmitted incident wave $V_{t,1}$.

$$S_{11} = \frac{V_{r,1}}{V_{t,1}} \quad . \tag{10}$$

In practice, to match the GSG configuration of the HF probe head the device under test (DUT) of small footprint has normally contact pads formed by CPW structure (Figure 2.7).

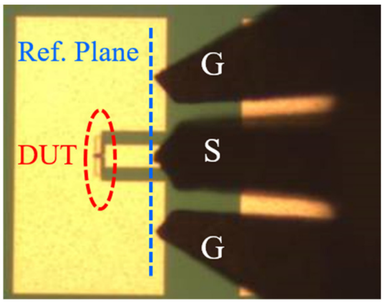


Figure 2.7: DUT with GSG contact pad and probe tips.

Notice that, after calibration the reference plane of the measurement system can be only shifted to the probe tips. That means, the raw measurement S-Parameters still include information both of DUT and the coplanar contact pad. The procedure that extracts the S-Parameters of DUT from the raw measurement data is called “De-embedding”. Two of the most common methods “Open-Short” (OS) and “Short-Open” (SO) that are based on discrete lumped element model are widely employed for one- or two-port network de-embedding (Figure 2.8) due to its simplicity. For the OS lumped model approach all parallel parasitic Y_p are assumed to be located in the signal path and all serial parasitic Z_s in the interconnect path. For the SO approach Z_s are assumed to be located in the signal path and Y_p in the interconnect path.

For OS case the impedance of DUT Z_{DUT_OS} results in:

$$Z_{DUT\_OS} = \frac{1}{\frac{1}{Z_{MEAS}} - \frac{1}{Z_{OPEN}}} - \frac{1}{\frac{1}{Z_{SHORT}} - \frac{1}{Z_{OPEN}}} \quad , \tag{11}$$

and for SO case the impedance of DUT Z_{DUT_SO} results in:

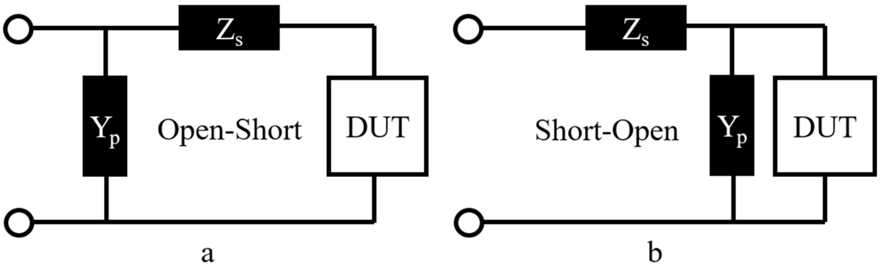


Figure 2.8: Equivalent lumped models for OS (a) and SO (b) de-embedding.

$$Z_{DUT\_SO} = \frac{1}{\frac{1}{Z_{MEAS} - Z_{SHORT}} - \frac{1}{Z_{OPEN} - Z_{SHORT}}} \quad , \tag{12}$$

with Z_{MEAS} the raw measured impedance of the one-port network, Z_{OPEN} the impedance of the measured “Open” test structure and Z_{SHORT} the impedance of the measured “Short” test structure.

The transformation of the Z-Parameter to S-Parameter for one-port is defined by:

$$S_{11} = \frac{Z - Z_0}{Z + Z_0} \quad , \qquad (13)$$

with Z the input impedance of the one-port network and Z_0 the normalizing or reference impedance, which is normally set to $Z_0 = 50\ \Omega$ by most of measurement systems.

As mentioned, both OS and SO de-embedding approaches are based on the discrete lumped element models. Because this assumption could not fully describe the real situation for wave propagation, a limitation of these two approaches is noticed for frequency $f > 40$ GHz.

A more reliable one-port de-embedding approach for higher frequency range is proposed and verified up to $f = 110$ GHz under assumption of a symmetry condition [58]. This approach provides a broader valid range for the one-port de-embedding algorithm in microwave applications. Based on this de-embedding approach, let us take IMPATT diode as an example for one-port active device HF characterizations. The IMPATT diode is well known as microwave power sources. Different from most of diodes, it operates in the avalanche breakdown region. Near that working point, NDR can be provided, which means an amplifying effect. This amplifying effect can be well characterized by the small signal VNA S-Parameters measurement. In Figure 2.9 the real and imaginary parts of IMPATT diode with mesa size $A_d = 30\times2\ \mu\text{m}^2$ under biasing current $I_{bias} = 40$ mA are shown. The avalanche frequency f_{av} has an obvious shift of nearly 30 GHz after de-embedding. In addition, the resonance amplitudes of the real and imaginary part of impedance are influenced much by the parasitic due to the contact pads. This example shows the necessity of a proper de-embedding for a precise HF characterization of microwave components and for the further circuits design as well.

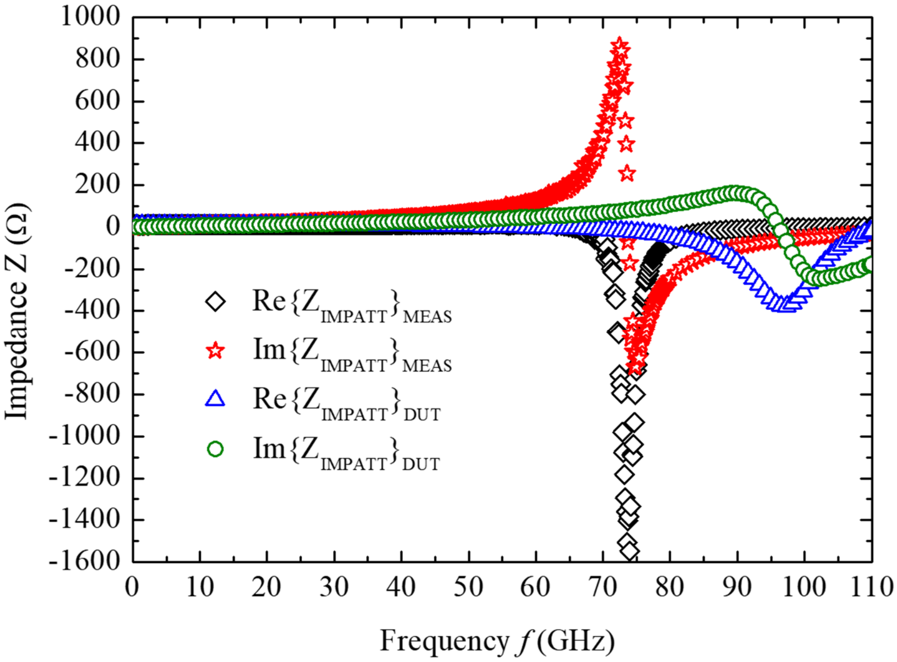


Figure 2.9: Real and imaginary parts of the evaluated IMPATT diode over frequency before de-embedding (MEAS) and after de-embedding (DUT).

2.6 BASICS OF SMITH CHART

The Smith chart is invented by P. H. Smith in the 1930s, which is originally thought for a straightforward graphical solution of impedances transform through transmission lines of certain lengths [59]-[60]. Because no computer-aided tools were available for engineers at that time, the Smith chart has become an essential tool to the design of matching circuits in high frequency technique. Even nowadays the display of measured RF data in Smith chart helps RF engineers to have an intuitive understanding of investigated circuits.

The key contribution of Smith chart is to successfully transform impedance plane to reflection coefficient plane (Smith chart) based on one fact, that the reflection coefficient changes only the angle but not the magnitude when traveling wave propagates through a lossless transmission line. This invention brings the straightforward insight into impedance transform by skipping impedance change in complex form. In this sense, P. H. Smith's effort offers a solid basis for the S-parameter theory introduced in section 2.5. Actually for the Smith chart user, the reflection coefficient is written preferred as Γ than $S_{N,N}$ with N =1 (reflection coefficient in S-parameter form for port-N). Thus, Smith chart plane is usually named as Γ-plane.

Let us dive into more details how this plane transform works. Normally the reflection coefficient is expressed as:

$$\Gamma = \rho \cdot e^{j\varphi} \qquad , \tag{14}$$

with ρ the radius of vector (magnitude); φ the angle of vector in polar coordinates system and

$$\Gamma = u + j \cdot v \qquad , \tag{15}$$

with u the real part; v the imaginary part in rectangular coordinates system.

Based on equation (14) and (15), the following relations can be derived from polar to rectangular:

$$u = \rho \cdot cos\varphi; v = \rho \cdot sin\varphi \qquad , \tag{16}$$

and from rectangular to polar:

$$\rho = \sqrt{u^2 + v^2};\ \varphi = tan^{-1}(\frac{v}{u}) \qquad . \tag{17}$$

For correctly mapping the impedance plane to reflection coefficient plane we have following normalized impedance Z_n defined as:

$$Z_n = r + j \cdot x \qquad , \tag{18}$$

with r the resistance value; x the reactance value, j the imaginary unit.

From equation (13) the normalized impedance Z_n can be expressed in reflection coefficient Γ (also written as S_{11} for one-port network) as:

$$Z_n = \frac{1 + \Gamma}{1 - \Gamma} \qquad . \tag{19}$$

By applying equation (14) and (18) to equation (19), the following equation can be rewritten with a small trick:

$$r + j \cdot x = \left(\frac{1 + \rho \cdot e^{j\varphi}}{1 - \rho \cdot e^{j\varphi}}\right) \cdot \left(\frac{1 - \rho \cdot e^{-j\varphi}}{1 - \rho \cdot e^{-j\varphi}}\right) \qquad . \tag{20}$$

With $e^{j\varphi} + e^{-j\varphi} = 2 \cdot cos\varphi$ and $e^{j\varphi} - e^{-j\varphi} = 2 \cdot j$, equation (20) can be simplified as:

$$r + j \cdot x = \frac{1 - \rho^2 + j \cdot 2 \cdot \rho \cdot sin\varphi}{1 + \rho^2 - 2 \cdot cos\varphi} = \frac{1 - u^2 - v^2 + j \cdot 2 \cdot v}{1 + u^2 + v^2 - 2 \cdot u} \quad , \qquad (21)$$

which determines the real part expression as:

$$r = \frac{1 - u^2 - v^2}{1 + u^2 + v^2 - 2 \cdot u} \quad , \qquad (22)$$

and the imaginary part expression as:

$$x = \frac{2 \cdot v}{1 + u^2 + v^2 - 2 \cdot u} \quad . \qquad (23)$$

To finally recognize the mapping from Z-plane to Γ-plane, equation (22) and (23) are rewritten in the following forms:

$$\left(u - \frac{r}{1 + r}\right)^2 + v^2 = \left(\frac{1}{1 + r}\right)^2 \qquad (24)$$

for resistance mapping, and

$$(u - 1)^2 + \left(v - \frac{1}{x}\right)^2 = \left(\frac{1}{x}\right)^2 \qquad (25)$$

for reactance mapping in Γ-plane.

Figure 2.10 illustrates some concrete cases for the introduced mapping within unity circle, which are valid for passive networks.

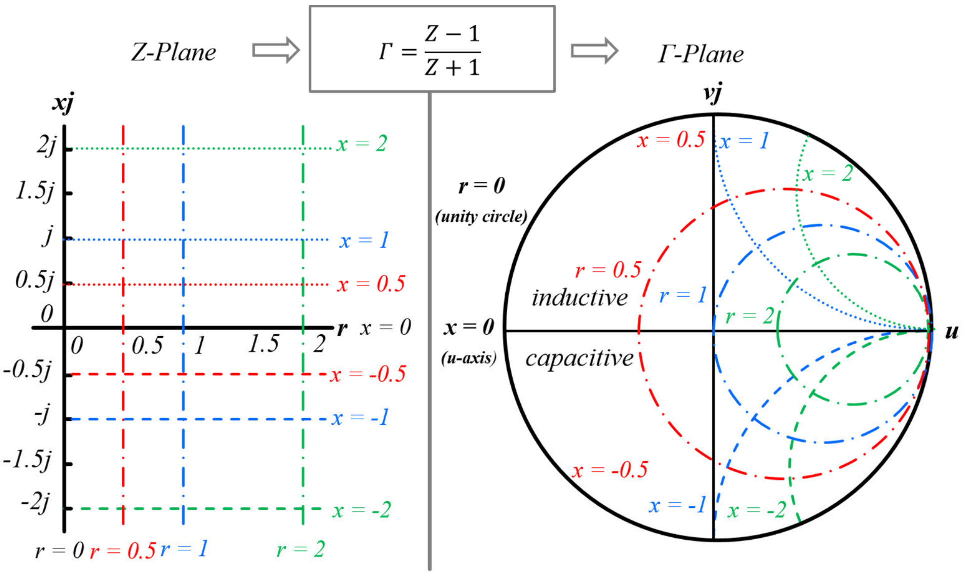


Figure 2.10: Mapping of constant resistances (r = 0; 0.5; 1; 2) and constant reactance (x = 0; ±0.5; ±1; ±2) in Z-plane to Γ-plane (impedance Smith chart).

2.7 GLANCE AT SCHOTTKY DIODE

Schottky barrier diode (known commonly as Schottky diode) is named after German Scientist Walter Schottky, who is one of the three most dedicated scientists of 1930s (other two are Boris Davydov, Russia and Nevill Mott, England) in explaining the rectification phenomenon in semiconductor surface. Schottky diode is well known as the fastest two-terminal rectifying device. Benefiting from its "majority carrier" property [17], the cut-off frequency (f_{co}) [18] of Schottky diode can be well achieved in the Terahertz regime (0.3 THz $\leq f \leq$ 3 THz) [61]-[65]. Together with an antenna, the rectifying antenna (rectenna) can be realized commonly for wireless RF signal detection [66]-[68] or energy harvesting applications [69]-[71].

Based on his own theoretical work on quantum-mechanical explanation for the first time in electronic semiconductors in 1931 [72]-[73], the English Mathematician/Physicist Sir Alan Herries Wilson proposed one year later a general thoery [74] to consummate the then incomplete rectification theory in semiconductor crystal. Seven years later, Boris Davydov [75]-[76], Nevill Mott [77]-[78], and Walter Schottky [79] explained finally rectification independently, who attributed the phenomenon mainly to a majority carrier concentration on the semiconductor surface which set up an asymmetric barrier to real current flows, namely rectification.

In chapter 6, a special MOTT operation mode (named after Nevill Mott [77]-[78]) of metal-semiconductor Schottky barrier diodes appropriate for RF rectification is investigated. Based on comprehensive DC and AC characterization data of fabricated Schottky diodes, the classic cut-off frequency can be well estimated with a small-signal lumped-element model. Additionally a numerical analysis considered in real application scenario is performed to reveal the key point for high rectifying efficiency design.

Chapter 3. IMPATT DIODE

3.1 IMPATT LAYER GROWTH FOR E-BAND APPLICATION

There are several available doping strategies to realize the desired doping profiles by applying MBE technique, e.g. pre-buildup [80], co-evaporation [81], doping by secondary implantation (DSI) [82], and low-energy implantation [83]. In reality combinations of these strategies during MBE growth are often performed according to the properties of dopant materials (e.g. temperature budget) and aimed doping levels [84].

Dependent on how carriers participate in drift mechanism two definitions of IMPATT layer stacks are mainly available. If only one carrier type (electron or hole) is involved in drift mechanism with layer stacks as p^{++}-n^{-}-(i)-n^{++} or n^{++}-p^{-}-(i)-p^{++} the device is defined as single-drift (SD) IMPATT diode. If both electrons and holes are to be considered in drift mechanism with layer stacks as p^{++}-p^{-}-(i)-n^{-}-n^{++} the device is defined then as double-drift (DD) IMPATT diode. Generally speaking DD IMPATT diodes present lower noise for high frequency power generation due to the larger efficiency compare to SD diodes but meantime require firstly more effort for extra process steps

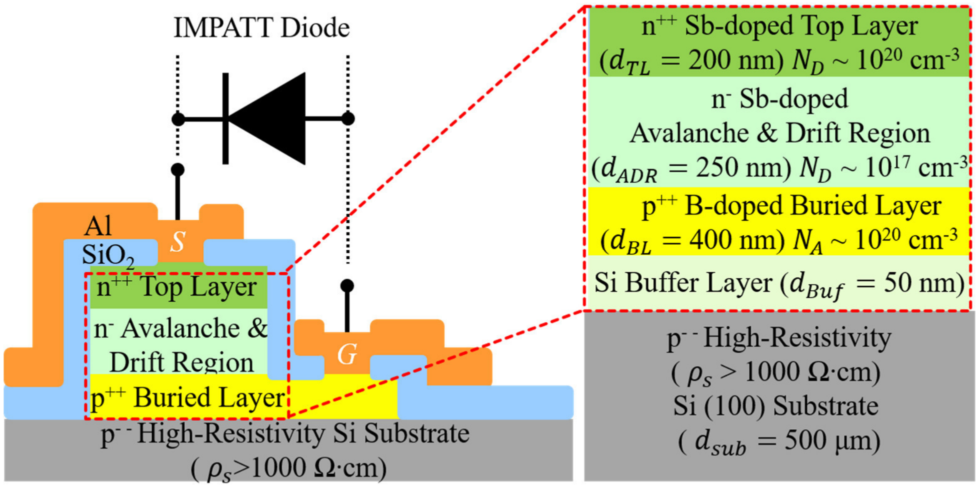


Figure 3.1: Layer stacks prepared for SD IMPATT mode operation.

and precise control by the challenging MBE growth, secondly higher voltages to operate, and are, therefore, less appropriate for monolithic integration purposes.

For MBE samples prepared for this dissertation, the p^{++}-n^{-}-n^{++} structural SD IMPATT layers are grown instead of the conventional Read type [86] p^{++}-n^{-}-i-n^{++} structure due to mainly two reasons: 1. the quality of intrinsic layer is difficult to control because of the unwanted n-type background doping ($N_b \sim$ 10^{-15} cm^{-3}) of in-house technology; 2. extra effort is required for separately controlling the thickness of avalanche layer and drift region layer. Figure 3.1 shows the detailed layer stacks presented together with the device integration concept (section 2.2). Both the pre-buildup and the co-evaporation strategies were experimented in-house for the lightly n-type doped avalanche and drift region.

3.1.1 *Design of "avalanche and drift region" for IMPATT mode operation*

In order to guide the growth of the layer stacks required by the desired small-signal IMPATT operation mode, a qualitative analysis from device physics aspect is given related to the important two basic mechanisms, avalanche and drift.

The structure p^{++}-n^{-}-n^{++} in Figure 3.2 is chosen with the combined avalanche and drift region for minimized effort but performance-stabilized technological process by MBE growth. Different to Read type [43], normal abrupt p-n IMPATT [44] and Misawa [85] p-i-n diodes in discrete devices at low frequency era, the total thickness of the n^{-} layer is limited only within $d = 300$ nm, which have to be shared both by avalanche and drift mechanisms with the same doping level. Under this thickness scale the usually "short" avalanche region width compared with "long" drift region cannot be neglected anymore but influences the transit-time delay dramatically related to the frequency range of the NDR under IMPATT operation mode.

In addition, the doping level in n^{-} layer plays an important role on the distribution of the avalanche and drift region. Too low or too high doping levels could both shift the IMPATT functionality out of the desired frequency band. Figure 3.2 shows the depletion states at the breakdown voltage of the investigated SD IMPATT diode model with a certain n^{-} layer thickness and different doping levels. The green state can be considered as reference for the analysis. The total doping concentration in this layer enables a complete depletion of the space charge region (SCR) with ignorable width in highly doped p^{++} layer due to at least two-magnitude doping difference to the n$^-$ side. The extension of the avalanche region is drawn oval in Figure 3.2, and the drift region is marked by an arrowed solid line. The red state shows the lower doping case compared with the green reference case. The SCR depletion width is supposed to be larger but limited physically by the thickness of the n$^-$ layer in reality. However the lower doping leads to a wider avalanche region. Thus, the drift region width is eventually reduced, so that only signals with higher frequencies (smaller wavelengths) could possibly meet the delay condition of the NDR. On the other hand, the thermal endurance of the whole device should also be taken into account. A lower doping level increases the breakdown voltage, which reduces the maximum biasing current by the same injected DC power. As defined by Read, the avalanche frequency is roughly proportional to the square root of the current density. Thus, the device can be driven without damage only up to a lower frequency, but shows no NDR for the whole measurement range until burned out [23]. This experimental observation confirms and complements the theory about the frequency band properties of Read or abrupt junction IMPATT diodes [86] from device thermal endurance aspect. The blue state shows the higher doping case with a reduced SCR width limited inside the n$^-$ layer. Although the avalanche region shrinks slightly, the drift region width could be strongly reduced. The IMPATT operational range could be shifted again into higher frequencies.

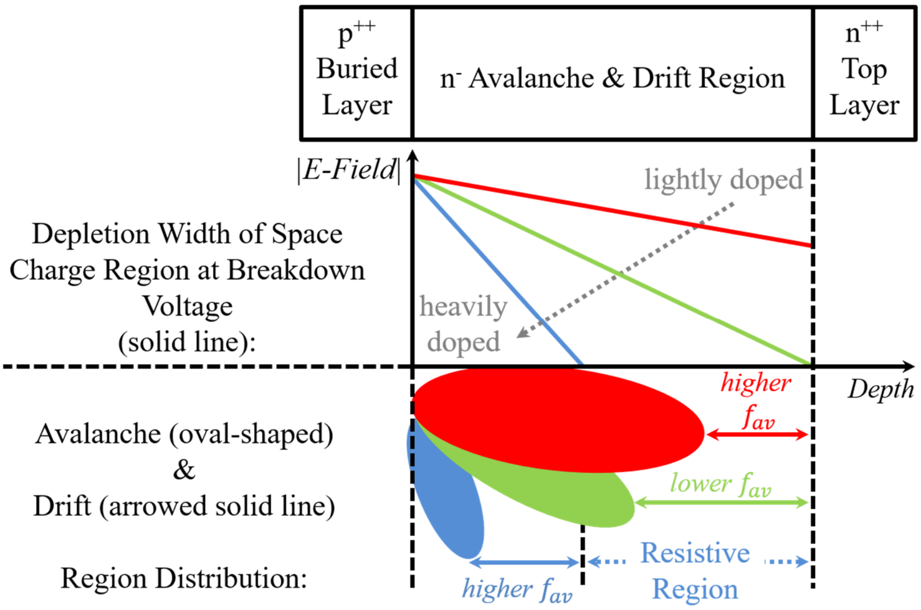


Figure 3.2: Depletion states of SCR at breakdown voltage V_{br} and distribution of avalanche and drift region with different doping concentration N_D in the n$^-$ layer.

To ensure the device-level IMPATT functionality at desired frequencies, the resonance frequencies have to be matched by choosing the proper device dimensions, too. However, the fulfillment of the layer stacks for the transit-time based IMPATT mode operation is the prerequisite, whether the required NDR within certain frequency bands can be generated at all.

3.1.2 *Recipe optimization of IMPATT layer stacks for E-band design*

To set a reliable and realistic growth initial point before starting any technological experiment an estimation of the n$^-$ layer thickness and doping level appropriate for E-band design becomes necessary. A practical equation is proposed by S. M. Sze and R. M. Ryder to roughly predict the frequency f, around which the Read type p^{++}-n$^-$-i-n^{++} IMPATT diodes operates optimally [86]:

$$f \cong \frac{v_s}{2 \cdot w_{dep}} \quad , \tag{26}$$

with v_s the carrier saturation velocity and w_{dep} approximately the depletion width of SCR. The middle frequency f_{mid} = 75 GHz of E-band (60 GHz $\leq f \leq$ 90 GHz) is taken for instance with v_s= 10^7 cm/s for electrons in Si with high purity, which gives the required w_{dep} = 666.7 nm contributed mainly by intrinsic drift region. However due to high current density the device temperature during the IMPATT operation increases considerably above room temperature (T = 300 K) as theory assumes. The v_s in Si degrades up to 30% with temperature change from T = 300 K to T = 500 K [87]. Additionally in the chosen p^{++}-n$^-$-n^{++} structural IMPATT layer stack for this dissertation the drift region is not anymore intrinsic but doped at N_D ~10^{17} cm^{-3} level. The impurity induced scattering [88]-[89] might contribute extra 10% to 40% degradation of the v_s. Thus with the estimated carrier saturation velocity of $3 \cdot 10^6$ cm/s $\leq v_s \leq 6 \cdot 10^6$ cm/s, the depletion width of 200 nm $\leq w_{dep} \leq$ 400 nm was set roughly as expected thickness reference for E-band IMPATT mode operation.

As mentioned, the distribution of the avalanche and drift region defines eventually the functional frequency band of IMPATT operation with the fixed n$^-$ layer thickness. For catching the desired IMPATT functionality in reality it is very challenging to adjust the doping concentration in the n$^-$ layer shared both by avalanche and drift region with comparable widths within hundreds of nanometers. This requires the precisely controlled doping and thickness as well through the MBE growth process.

Table I: An overview of experimental information linked to the n$^-$ layer for avalanche and drift region for all grown and processed IMPATT samples.

MBE A-N.O.	Process V-N.O.	Thickness (nm)	IMPATT NDR	Doping Strategy	nom. Doping (10^{17}cm^{-3})	act. Doping (10^{17}cm^{-3})
3538-1	822-1-1	322	no	pre-buildup	1.5	4.0
3539-1	822-1-2	350	no	pre-buildup	1.0	3.0
3540-1	822-1-3	320	no	pre-buildup	2.0	4.5
3887-1	908-1-1	299	no	pre-buildup	1.0	1.1
3888-1	908-1-2	276	no	pre-buildup	1.0	1.7
3889-1	908-1-3	299	no	pre-buildup	1.0	1.5
3890-1	908-1-4	305	yes	co-evaporation	1.0	0.5
4136-1	984-1-1	255	yes	co-evaporation	0.5	< 0.2
4137-1	984-1-2	286	yes	co-evaporation	1.0	0.2
4138-1	984-1-3	261	yes	co-evaporation	1.5	0.4
4172-1	14-1-1	243	yes	co-evaporation	0.4	0.3
4173-1	14-1-2	248	yes	co-evaporation	1.0	0.9
4174-1	14-1-3	243	yes	co-evaporation	1.5	1.4
4175-1	14-1-4	251	yes	co-evaporation	2.0	2.2
4172-2	72-1-1	243	yes	co-evaporation	0.4	0.3
4173-2	72-1-2	248	yes	co-evaporation	1.0	0.9
4174-2	72-1-3	243	yes	co-evaporation	1.5	1.4
4175-2	72-1-4	251	yes	co-evaporation	2.0	2.2

Both pre-buildup and co-evaporation doping strategies were applied by growing n$^-$ layer in-house. Through amounts of experiments from MBE growth to device fabrication and characterization the co-evaporation strategy was proved as appropriate for IMPATT mode operation. In Table I all MBE and process runs are listed with key information related to the sensitive n$^-$ layer of avalanche and drift region. The layer thickness varies within 243 nm $\leq d_{ADR} \leq$ 350 nm with the achieved doping concentration range of $0.2 \cdot 10^{17}$ cm^{-3} $\leq N_D \leq$ $4.5 \cdot 10^{17}$ cm^{-3}. For the desired E-band IMPATT mode operation, the optimum n$^-$ layer thickness is finalized as $d_{ADR} = 250$ nm with the corresponding doping concentration level of $0.3 \cdot 10^{17}$ cm^{-3} $\leq N_D \leq$ $1.4 \cdot 10^{17}$ cm^{-3}. Based on this verified recipe of IMPATT layer stacks for E-band design specifically calibrated to the in-house MBE technology the further performance optimization at device-level becomes then realistic.

3.2 DC CHARACTERIZATION OF IMPATT DIODE

Focused on breakdown voltage, series resistance and ideality factor, the I-V characteristics of fabricated IMPATT diodes were measured. By characterizing TLM structures on the same chip, the quality of the heavily doped buried and top layers can be verified experimentally and compared with nominal doping concentration aimed by the MBE growth. The size of the small mesa (top layer + n$^-$ layer) defines the diode dimension, e.g. a diode with the small mesa of width w_{mesa} = 30 µm and length l_{mesa} = 10 µm is denoted for short as diode with device area A_d = 30×10 µm^2 in this dissertation.

3.2.1 *Breakdown voltage V_{br} of IMPATT diode*

For IMPATT diode, which operates in the avalanche breakdown region, the breakdown voltage V_{br} is an important parameter extracted by I-V characteristics. Figure 3.3 shows all I-V characteristics of the IMPATT diodes with different dimensions. Within doping concentration range of $0.3 \cdot 10^{17}$ cm^{-3} $\leq N_D \leq 2.2 \cdot 10^{17}$ cm^{-3}, $\Delta V_{br} = 3$ V is experimentally obtained. Slightly increased current level in reverse direction with the increasing diode dimension can be observed, too. This implies an acceptable crystal quality for low leakage current.

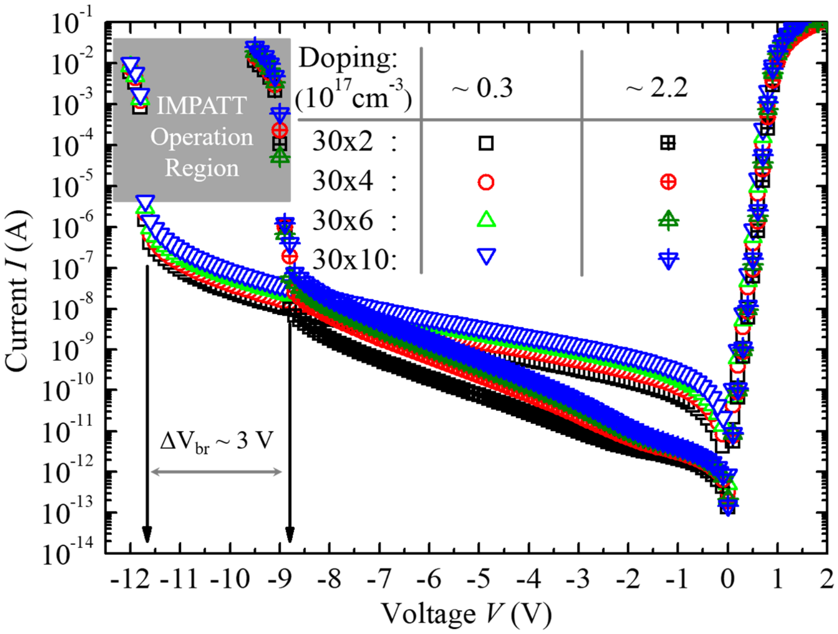


Figure 3.3: I-V characteristics of A_d = 30×2 μm^2, 30×4 μm^2, 30×6 μm^2, and 30×10 μm^2 IMPATT diodes from two samples each with $N_D = 0.3 \cdot 10^{17}$ cm^{-3} and $N_D = 2.2 \cdot 10^{17}$ cm^{-3} doping concentration.

The measured V_{br} informs not only the proper biasing compliance for the RF characterization to avoid over-biasing caused burnout but also the breakdown type (“avalanche” or “punch through”) of the n$^-$ layer, which influences the IMPATT functionality eventually. To practically predict V_{br} of abrupt p-n junctions in semiconductors (e.g. Si, Ge, GaAs, and GaP), an approximate expression for pure bulk material (also valid for SCR width w_{dep} < epitaxy layer thickness of avalanche and drift region d_{ADR}) was given by S. M. Sze and G. Gibbons [90] as follows:

$$V_{br} = 60\left(\frac{E_g[eV]}{1.1}\right)^{3/2}\left(\frac{N_b[cm^{-3}]}{10^{16}}\right)^{-3/4}(V) \quad , \qquad (27)$$

with E_g the band gap (E_g =1.12 eV for Si) and N_b is the background doping of the semiconductor materials. In Figure 3.4, V_{br} is plotted over doping concentration in n$^-$ layer. A discrepancy between approximation and praxis occurs only for the sample with $N_D = 0.3\cdot10^{17}$ cm^{-3}, whose natural depletion width w_{dep} exceeds the layer thickness of n$^-$ avalanche and drift region d_{ADR}.

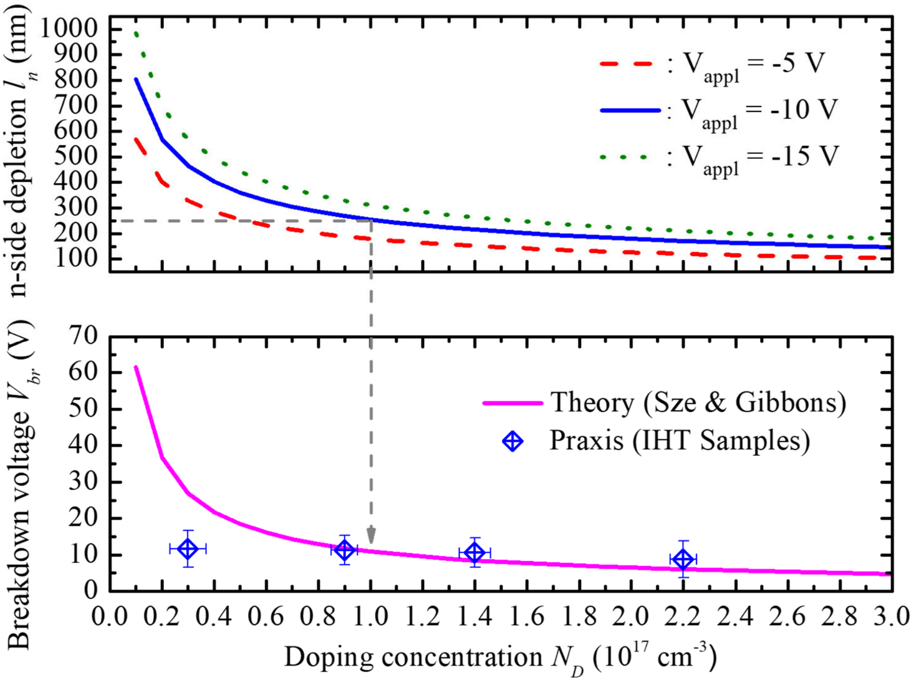


Figure 3.4: Theoretical estimation (Sze & Gibbons) vs. experimental verification (IHT samples) of the breakdown voltage V_{br}; punch through breakdown mechanism for lower doping concentration ($N_D < 1.0\cdot10^{17}$ cm^{-3}) explained by calculated depletion width w_{dep} = 250 nm.

Considering the relationship between the applied external voltage V_{appl}, the internal built-in voltage V_{bi}, the maximum electric field E_m, and the depletion width both in p-type side l_p and n-type side l_n for p-n junction:

$$V_{bi} - V_{appl} = \frac{E_m \cdot (l_p + l_n)}{2} \quad , \qquad (28)$$

and for E_m at the metallurgic interface of p-n junction:

$$E_m = \frac{q \cdot N_D \cdot l_n}{\varepsilon} = \frac{q \cdot N_A \cdot l_p}{\varepsilon} \qquad , \qquad (29)$$

with q the elementary charge, N_D the donor doping concentration in n-type side, N_A the acceptor doping concentration in p-type side, ε the permittivity of the material (ε = $\varepsilon_0 \cdot \varepsilon_r$ with ε_0 the permittivity of vacuum and ε_r the relative permittivity of the material), we have then:

$$l_n\left(l_p + l_n\right) = \frac{2 \cdot \varepsilon \cdot (V_{bi} - V_{appl})}{qN_D} \qquad . \qquad (30)$$

In our case $l_n \gg l_p$ due to three-magnitude doping level difference for the p-n junction and together with

$$V_{bi} = V_T \cdot \ln \frac{N_D \cdot N_A}{n_i^2} \qquad , \qquad (31)$$

the final expression for the dominant depletion width in n-side l_n can be written as:

$$l_n = \sqrt{\frac{2 \cdot \varepsilon \cdot (V_T \cdot \ln \frac{N_D \cdot N_A}{n_i^2} - V_{appl})}{q \cdot N_D}} \qquad , \qquad (32)$$

with V_T the temperature voltage ($V_T = 25$ mV at $T = 300$ K), n_i the intrinsic carrier concentration ($n_i = 1.0 \cdot 10^{10}$ cm^{-3} at $T = 300$ K), and N_A=10^{20} cm^{-3} at $T = 300$ K. The l_n can be also plotted over doping concentration N_D each for the applied voltages V_{appl} = -5 V, -10 V, and -15 V in Figure 3.4.

Since the n$^-$ layer thickness is about $d_{ADR} = 250$ nm for the grown samples as previously mentioned, with the applied external voltage V_{appl} = -10 V (blue solid line), the doping concentration of $N_D = 1.0 \cdot 10^{17}$ cm^{-3} is the critical doping point for an exactly complete depletion through the $d = 250$ nm n$^-$ layer. This explains the discrepancy compared with the theory estimation for bulk material for the sample with doping level of $N_D = 0.3 \cdot 10^{17}$ cm^{-3}. Additionally, it confirms the breakdown type for this sample as “punch through”, because the electrical field distribution is not anymore triangular as assumed in equation (28) and (29) but trapezoidal. In real design the punch through breakdown has an advantage for the fine tuning of the IMPATT functionality related to the desired frequency band (thickness is all-in-all easier to control than doping by MBE growth). Furthermore, the driven current (density) is increased slightly due to the intentionally reduced breakdown voltage V_{br} under the same injected DC power, which could lead to a higher IMPATT operation frequency.

3.2.2 *Extraction of series resistance R_s and ideality factor η of IMPATT diode*

From the forward I-V characteristics of diode the series resistance R_s and ideality factor η of IMPATT diodes can be extracted [91] based on the diode I-V equation:

$$I = I_s \cdot (e^{\frac{V - R_s \cdot I}{\eta \cdot V_T}} - 1) \qquad , \qquad (33)$$

I_s is the reverse saturation current, R_s is responsible for the forward current deviation at high currents and relevant for the small-signal lumped-element modeling in section 3.4. An ideal diode without the recombination effect in the SCR offers η = 1. A simple model with energy levels exactly in the middle of the band gap delivers for η = 2. In reality η is an indicator for semiconductor crystal quality in p-n junction and surface passivation on the range of diodes.

Figure 3.5 presents the differential ideality factor η over the ideal voltage (voltage drop due to R_s is calibrated) for different diodes on sample V14-1-1 with corresponding R_s values extracted from the forward I-V characteristics.

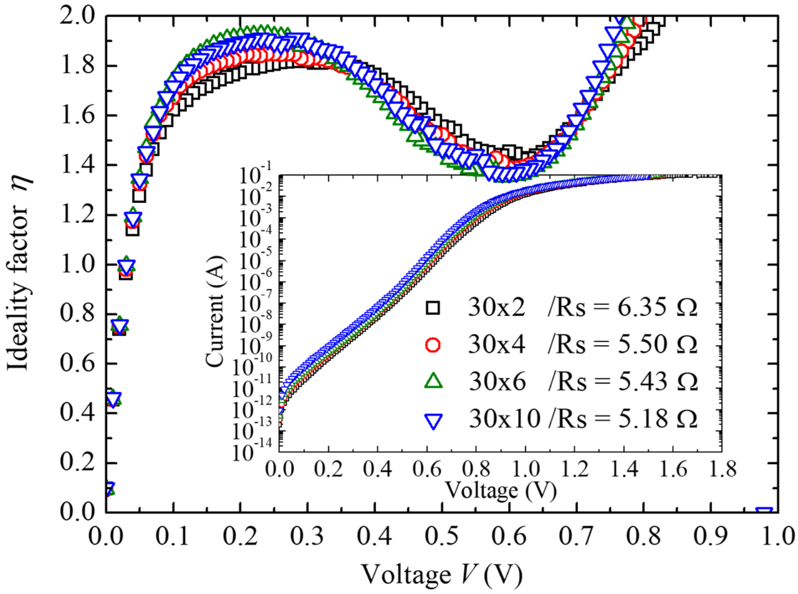


Figure 3.5: Extraction of series resistance R_s and ideality factor η for A_d = 30× n (n = 2, 4, 6, and 10) μm^2 diodes on sample V14-1-1 with corresponding forward I-V characteristics (inset).

The surface defects are probably responsible for the extracted ideality factor of $1.6 < \eta < 1.9$ in voltage range 0.1 V $< V <$ 0.4 V [91], but for strong IMPATT operation mode (current level $I >$ mA) in reverse breakdown region, the point defects or imperfect surface oxide structures induced recombination current (I < 0.1 μA) are not that critical. Once the IMPATT layer stacks are grown R_s becomes a relevant indicator for a reliable device fabrication. It is clearly to observe that R_s increases with decreasing diode area due to the top contact resistance. All extracted series resistances R_s from the sample V14-1-1 are at a reasonable level, which verifies a reliable process run by device fabrication. Otherwise high series resistances R_s can degrade the efficiency of the IMPATT diode applied to RF power generation.

3.2.3 *Results of transmission-line model (TLM) measurement of IMPATT diode*

To verify the actual doping concentration of n^{++} top layer and p^{++} buried layer for good ohmic contact, TLM measurements as introduced in section 2.4 were performed for TLM structures on IMPATT sample V14-1-1. The specific resistivity over doping concentration characteristics are shown in Figure 3.6 each for top layer and buried layer. Compared to the literature course, N_A ~$5\cdot10^{19}$ cm^{-3} for buried layer and N_D ~$7\cdot10^{19}$ cm^{-3} for top layer were achieved as electrically activated carrier concentration N_{car}, which ensures a quite reasonable ohmic contact layers with respect to the in-house MBE technology.

Table II summarizes all in section 2.4 introduced parameters extracted from TLM measurement for the sample V14-1-1.

Table II: Experimentally extracted information from TLM measurement results of buried layer and top layer of the sample V14-1-1.

V14-1-1	R_c (Ω)	R_{sh} ($\Omega/\square$)	l_T (μm)	d (nm)	ρ ($\Omega\cdot cm$)	ρ_c ($\Omega\cdot cm^2$)
Buried layer	1.24	75.1	3.4	319	$2.40\cdot10^{-3}$	$8.85\cdot10^{-6}$
Top layer	0.73	53.8	2.8	194	$1.05\cdot10^{-3}$	$4.16\cdot10^{-6}$

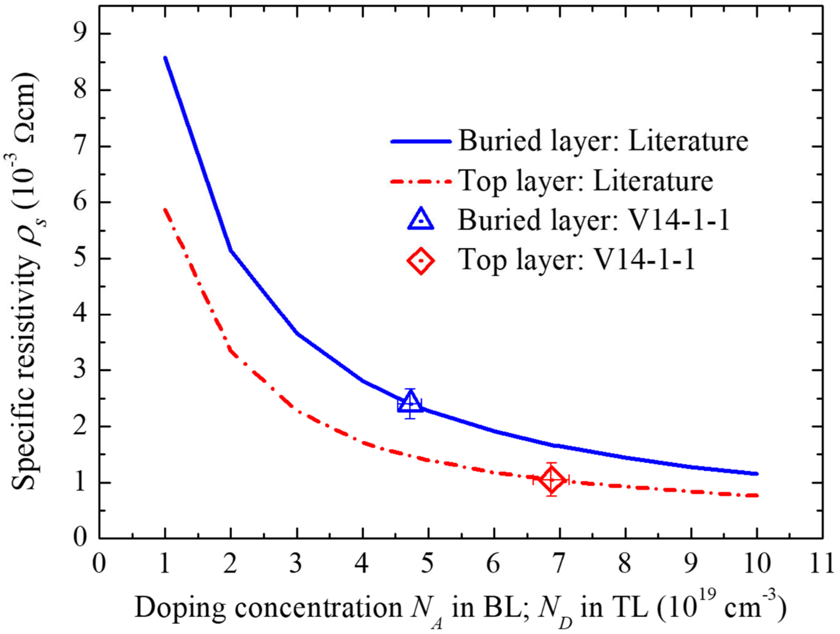


Figure 3.6: Specific resistivity ρ_s vs. doping concentration N_A in buried layer and N_D in top layer for the sample V14-1-1.

3.3 S-PARAMETER CHARACTERIZATION OF IMPATT DIODE

3.3.1 *Impedance spectra $Z_{IMPATT}(f)$ and avalanche frequency f_{av}*

By applying a reliable one-port de-embedding procedure [58] the parasitic effect due to CPW contact pads could be well eliminated. Thus, the S-parameters of the embedded inner diode can be obtained. From these S-parameters, the real and imaginary parts of the embedded IMPATT diode impedance Z_{IMPATT} can be calculated over the frequency by above mentioned linear algebra matrix transformation (S-matrix to Z-matrix) [56]. Figure 3.7 shows the obtained real $Re\{Z_{IMPATT}\}(f)$ and imaginary $Im\{Z_{IMPATT}\}(f)$ spectra (0.04 GHz $< f <$ 110 GHz) of $A_d =$ 30×2 µm^2 IMPATT diode impedances Z_{IMPATT} on the sample V14-1-1 under biasing currents of 5 mA $\leq I_{bias} \leq$50 mA with 5-mA step.

Large NDRs over a quite broad frequency band (core of the IMPATT functionality) are clearly observed near the so-called avalanche frequencies f_{av} in real-part spectra (resistance), at which the imaginary-parts (reactance) of the IMPATT diode are equal to zero, respectively. In addition, with increasing biasing current the avalanche frequency f_{av} can be shifted in higher frequencies, this phenomenon is discussed extensively in section 3.5 from the thermal endurance aspect during the IMPATT operation.

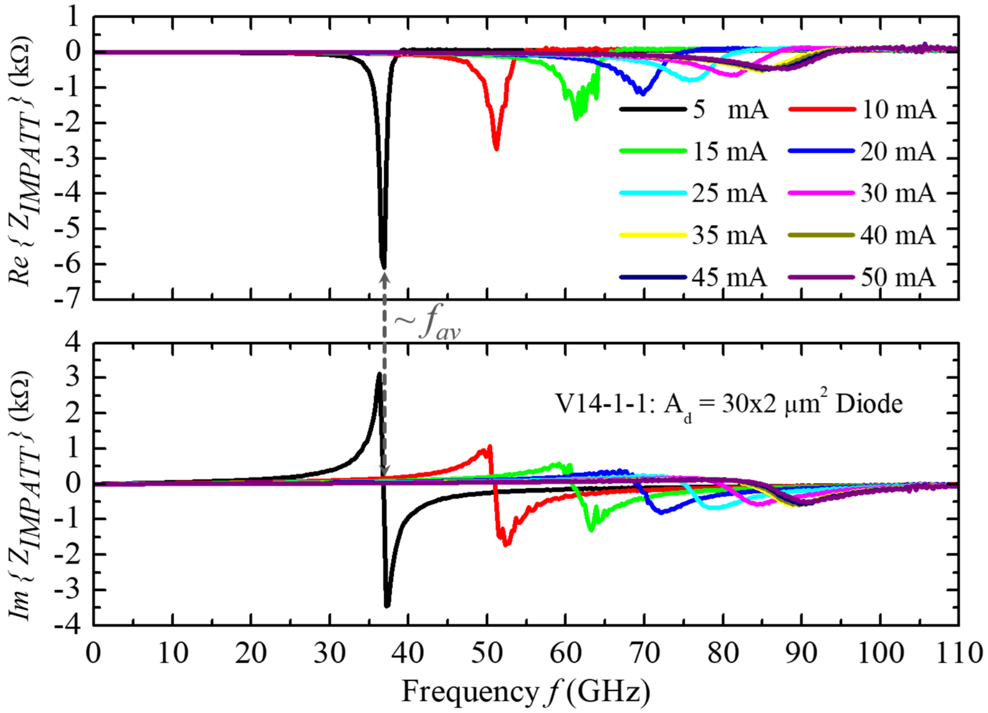


Figure 3.7: The real $Re\{Z_{IMPATT}\}(f)$ and the imaginary $Im\{Z_{IMPATT}\}(f)$ impedance spectra in frequency range 0.04 GHz $< f <$ 110 GHz of A_d = 30×2 μm^2 IMPATT diode impedances Z_{IMPATT} on the sample V14-1-1 under biasing currents of 5 mA ≤ I_{bias} ≤50 mA with 5-mA step.

3.3.2 *Device-level capacitance-voltage (C-V) measurement*

As described above, by applying TLM measurement we can conveniently verify the reliability of MBE layer growth and technological processes for heavily doped buried and top layers. However, for lightly doped n$^-$ layer (N_D ~10^{17} cm^{-3}) which forms Schottky instead of good ohmic contact with Al layer, the TLM measurement can no longer be used. A non-destructive capacitance-voltage

(C-V) measurement was proposed by J. Hilibrand and R. D. Gold in 1960 for determination of impurity distribution in junction diodes [92]. Actually it can be universally applied to all barrier capacitance of semiconductor junctions such as p-n junction, metal-semiconductor junction and MOS structure. Nowadays the C-V measurement is mostly employed for process verification in very-large-scale integration (VLSI) fabrication such as dose calibration and activation study of ion implantation process [93]-[94], for device characterization of MOS capacitors [95]-[96] and even for capacitive micro electrical mechanical system (MEMS) switches or varactors [97].

Basically, there are two approaches to perform C-V measurement depending on the measuring instruments and the frequency range. The most common approach in commercialized C-V instruments is based on impedance analysis with the simplified resistor-capacitor model. The measuring range goes usually from several Hertz to several hundred Megahertz. This approach can be well applied to process verification and for characterization of devices with sufficiently large dimensions in application scenarios below Gigahertz. However, this conventional approach shows limitation for characterization of aggressively downscaled CMOS devices, especially for millimeter-wave applications (f > 30 GHz). Two aspects are mainly concerned: 1. Due to downscaling the capacitances in focus (e.g. gate capacitance) become comparable to the embedded surrounding parasitic, which cannot be easily removed using the standard calibration procedure of the conventional C-V approach; 2. The operational frequency of the DUT is much higher than the measuring signal frequencies offered by the C-V instruments. This leads often to wrong estimation of the capacitances in a real device application scenario. Thus the other approach offered by the small-signal S-parameter characterization and the precise device modeling becomes main stream for C-V characterization of small-dimensional devices for millimeter-wave applications [98]-[99].

To perform the S-parameter-based device-level C-V measurement for one-port (two-terminal) device as the IMPATT diode [22], two steps are essential: (1) De-embedding procedure as mentioned to remove the parasitic effect on the DUT (the embedded inner diode); (2) Good device model to extract the relevant parameters from the measured S-parameter data of the DUT.

Figure 3.8 presents the measured “RAW” data (before de-embedding), “OPEN” data, and “SHORT” data together with the extracted “DUT” data (after de-embedding) of $A_d = 30\times10$ μm^2 diode on the sample V14-1-1 under a biasing voltage of $V_{bias} =$ -7 V within the frequency range of 0.04 GHz $\leq f \leq$ 40 GHz on impedance Smith chart as an example. The parasitic effect due to contact pads can be clearly reflected via the phase difference between the courses of the "RAW" and the "DUT", which is mainly caused by the parasitic capacitance. The de-embedded DUT data under the measurement biasing conditions were extracted (-1 V ≤ V_{bias} ≤ 0.2 V with 0.1-V steps; -4 V ≤ V_{bias} ≤ -1 V with 0.5-V steps; -11 V ≤ V_{bias} ≤ -4 V with 1-V steps, and V_{bias} =-11.5 V right before IMPATT operation for the sample V14-1-1). The phase variation between different biasing states is due to the increasing SCR width under increasing biasing voltage V_{bias}, which eventually leads to the reduction of junction capacitance C_j.

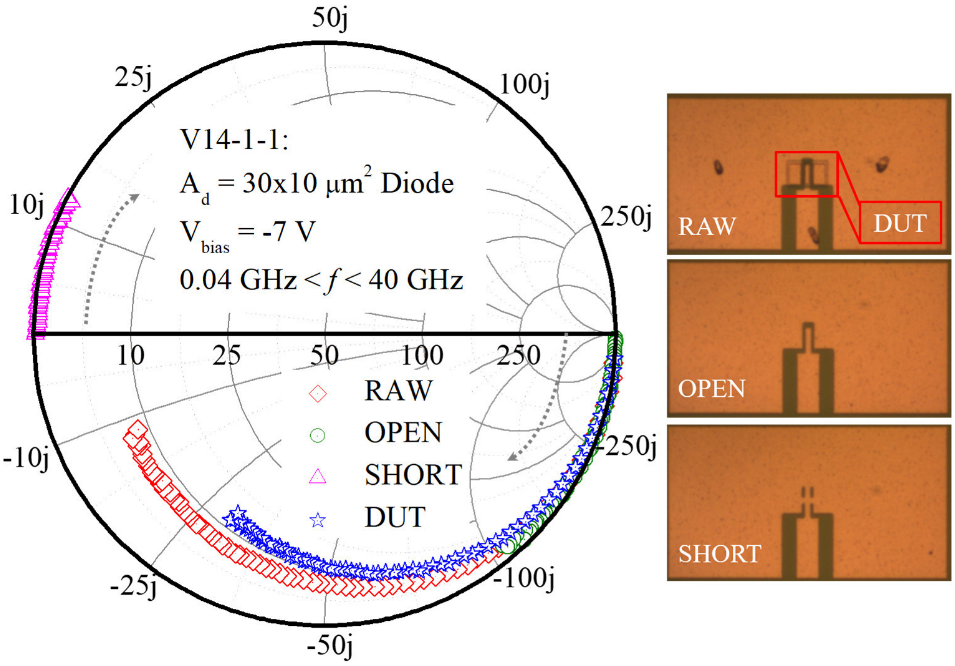


Figure 3.8: Courses of the measured "RAW" with biasing voltage V_{bias} = -7 V, "OPEN" and "SHORT" data with de-embedded "DUT" data on impedance Smith chart within frequency range 0.04 GHz ≤ f ≤ 40 GHz for A_d = 30×10 µm^2 diode of the sample V14-1-1.

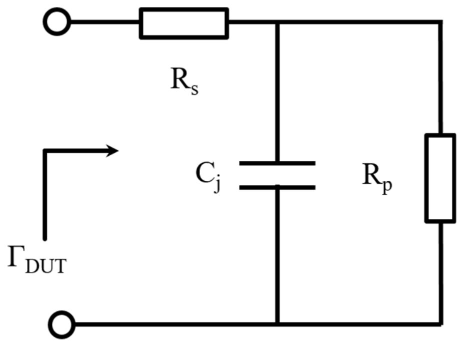


Figure 3.9: Classic small-signal lumped-element model of a reversely biased diode.

Together with DUT data which are de-embedded at an appropriate condition, the classic small-signal model for a reversely biased diode (Figure 3.9) is necessary to extract C-V characteristics. R_s, R_p, C_j represent each the series resistance of the diode, the blocked junction resistance, and the junction capacitance. R_s can be extracted from the measured I-V characteristics (subsection 3.2.2). The remaining two parameters (R_p and C_j) can then be conveniently found out by fitting the model to the de-embedded reflection coefficient Γ_{DUT} through the entire biasing voltage range -11.5 V $\leq V_{bias} \leq$ 0.2 V. Magnitude and phase diagrams of Γ_{DUT} at V_{bias} = -7 V are shown in Figure 3.10 for instance (comparison courses on impedance Smith chart also in inset). A broadband matching is achieved for the entire measuring frequency range of 0.04 GHz $\leq f \leq$ 40 GHz. Thus the extracted capacitance values can be well approximated to the real millimeter-wave application scenario.

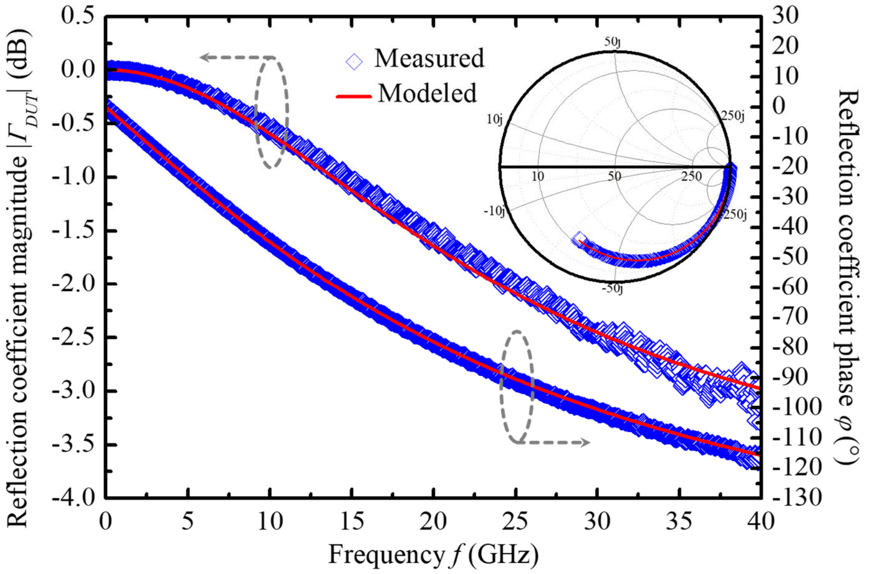


Figure 3.10: Measurement vs. modeling (biasing voltage V_{bias} = -7 V for A_d = 30×10 μm^2 diode of the sample V14-1-1) for parameter extraction (inset: comparison courses on impedance Smith chart).

All C-V characteristics gained by the S-parameter-based device-level approach for diodes of $A_d = 30\times10\ \mu m^2$ on samples V14-1-1, V14-1-2, V14-1-3, and V14-1-4 are plotted in Figure 3.11. To exemplify the variation of the junction capacitance C_j under the applied voltage V, the C_j^{-2} can be plotted over voltage (Figure 3.11). The depletion states are clearly reflected for all four samples. The lower the doping concentration is, the earlier the complete depletion occurs.

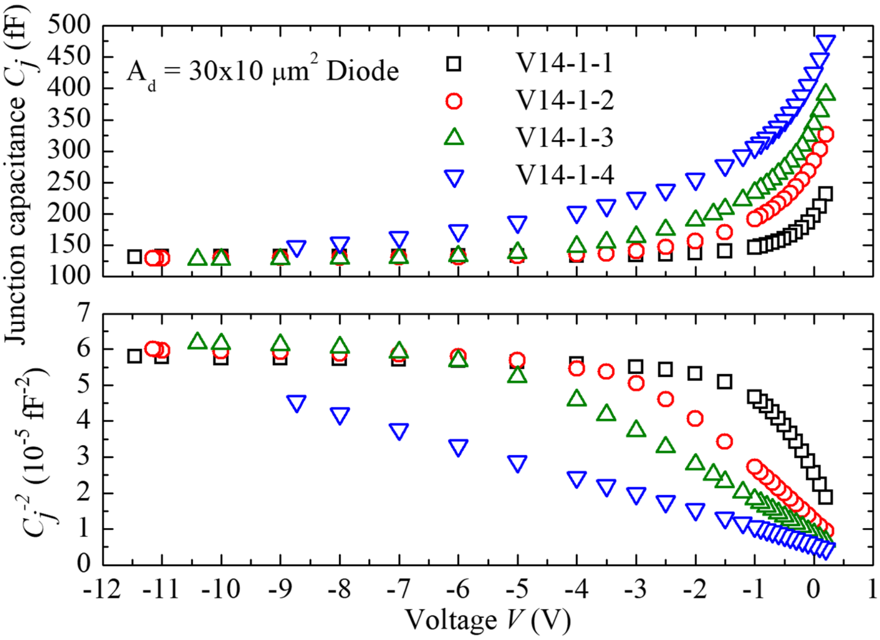


Figure 3.11: C-V characteristics extracted from the S-parameter based approach for $A_d = 30\times10\ \mu m^2$ diodes on samples V14-1-1, V14-1-2, V14-1-3, and V14-1-4.

The following equation is employed to calculate carrier concentration N_{car} over SCR depletion width w_{dep} from C-V characteristics:

$$N_{car} = -\frac{2}{q\cdot\varepsilon A_j^2\frac{d(\frac{1}{C_j{}^2})}{dV}}\quad, \tag{34}$$

where N_{car} is the carrier concentration, q is the elementary charge, ε is the permittivity of material ($\varepsilon = \varepsilon_0\cdot\varepsilon_r$ with ε_0 the permittivity of vacuum and ε_r the relative permittivity of material), A_j is the area of the p-n junction, C_j is the junction capacitance, and V is the applied voltage. The voltage dependent SCR depletion width w_{dep} can then be calculated by using the plate capacitor equation. Figure 3.12 shows the calculated carrier concentration N_{car} over SCR depletion width w_{dep}. By sample V14-1-1, V14-1-2, and V14-1-3, full depletion around w_{dep} = 250 nm is observed, which agrees very well with the growth thickness of the n$^-$ layer. Under the assumption of 100 % activated dopants, the extracted carrier concentration N_{car} can be taken as a reliable indicator for the achieved doping concentration by the MBE layer growth. Sample V14-1-4 cannot reach the punch through depletion at w_{dep} = 250 nm due to its highest doping concentration among all samples (refer to subsection 3.2.1).

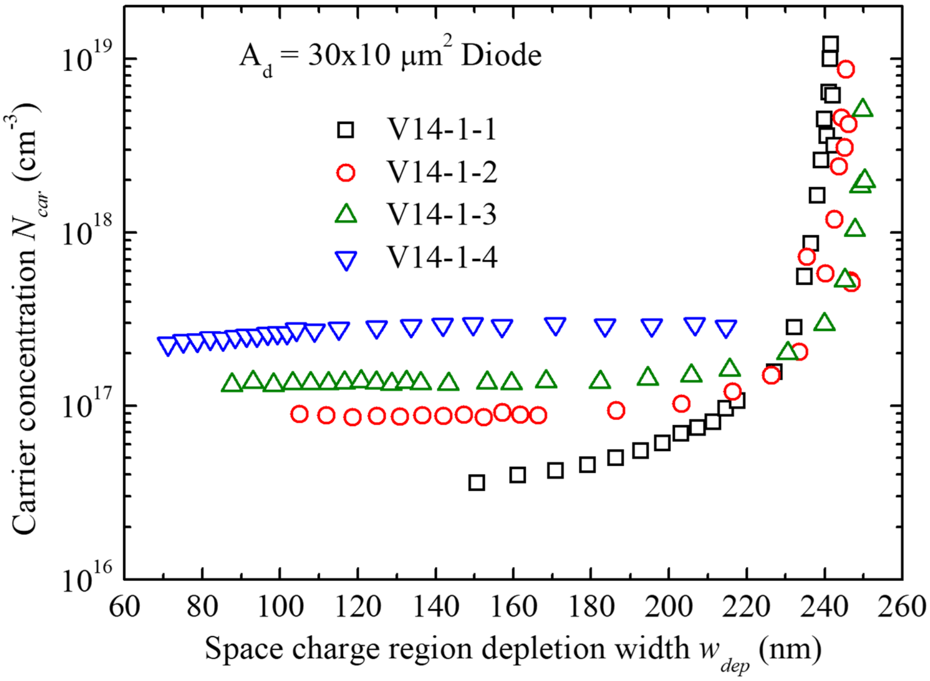


Figure 3.12: Carrier concentration N_{car} vs. SCR depletion width w_{dep} calculated from C-V characteristics for A_d = 30×10 µm^2 diodes on samples V14-1-1, V14-1-2, V14-1-3, and V14-1-4.

3.4 SMALL-SIGNAL LUMPED-ELEMENT MODELING OF IMPATT DIODE

Many small-signal models of Read type IMPATT diodes based on sets of state equations were established previously and gave reasonable explanations to the IMPATT behavior from the device physics aspect [100]-[103]. However, end-users (circuit or system designers) often suffer from a large number of mathematical derivations if only to understand the fundamental IMPATT functionality and to possibly benefit from huge physical parameter sets of the modeling by real design. In addition, even in the most popular G&H model (named after M. Gilden and M. E. Hines) [104], imperfectness due to some ideal assumptions in the original Read's proposal [105] still exists. For instance, the IMPATT resistance in the G&H model has the same characteristics of reactance, which conflicts with the real measurement. Thus, a practical modeling experiment to bridge the gap between device physics and the IMPATT model as a realistic circuit component has been performed in this part. The results show that the established measurement-based lumped-element model can be effectively applied to both the IMPATT functional and nonfunctional samples. Additionally, the numerical analysis offers interesting hints to the key links between device physics and the circuit component level. On the five adopted modeling parameters, the simulation program with the integrated circuit emphasis (SPICE [106]-[107]) model could be conveniently generated, which enables the comfortable integration of the fabricated IMPATT devices into the PDK as the standard device model.

3.4.1 *Principle for modeling of IMPATT diode*

To describe the IMPATT functionality more straightforward from the circuit component aspect, a small-signal lumped-element model has been developed as shown in Figure 3.13.

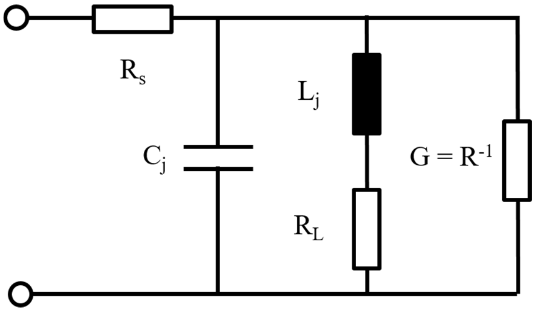


Figure 3.13: Small-signal lumped-element model of IMPATT diode.

R_s and C_j represent series resistance and junction capacitance as in the classic diode model (Figure 3.9). With C_j together the junction inductance L_j defines the avalanche frequency f_{av} of the IMPATT diode (refer to subsection 3.3.1). The load resistance R_L includes all noise-coupled resistive losses, which occur during the avalanche and drift mechanisms. The conductance $G\ (or\ R^{-1})$ is always negative in this model, which describes the avalanche-induced carrier multiplication and is thus relevant for the modeling of the NDR.

3.4.2 *Modeling vs. measurement*

Three out of five parameters from the model developed in subsection 3.4.1 could be extracted from the measurement directly (R_s from I-V characteristics, subsection 3.2.2; C_j from C-V measurement, subsection 3.3.2) or indirectly (L_j determined by C_j from C-V measurement and f_{av} from small-signal S-parameter characterization, subsection 3.3.1).

The remaining two parameters G and R_L cannot be verified via a single measurement, since both are related to the random sensitive avalanche mechanism and coupled to each other. However the combination of G and R_L offers a wide fitting range to the measured amplitude on both the real and imaginary parts of the IMPATT impedance spectra.

Based on the proposed modeling principle and the S-parameter characterization data, all $A_d =$ 30×2 μm^2 diodes of the five reference IMPATT samples (Table III) have been modeled. In Figure 3.14, the three IMPATT functional samples (Sample 3-5) with the same biasing current $I_{bias} = 30$ mA are presented each in the real and imaginary part impedance spectra. The modeling fits the measurement quite well. Slight variation in f_{av} is observed due to process tolerances.

Table III: n$^-$ layer information of five reference IMPATT samples.

Ref. Sample No.	Layer thickness d_{ADR} (nm)	Doping concentration N_D (10^{17} cm^{-3})	NDR observed? (0.04 GHz $\leq f \leq$ 110 GHz)
1	325	1.0	no
2	335	1.2	no
3	325	1.4	yes
4	325	1.7	yes
5	325	2.2	yes

The same procedure is also applied to the IMPATT nonfunctional samples (Sample 1&2) with a biasing current of $I_{bias} = 25$ mA. The results are shown in Figure 3.15. Interestingly, note that the modeling fits with the measurement to the same degree of accuracy in a broadband frequency range.

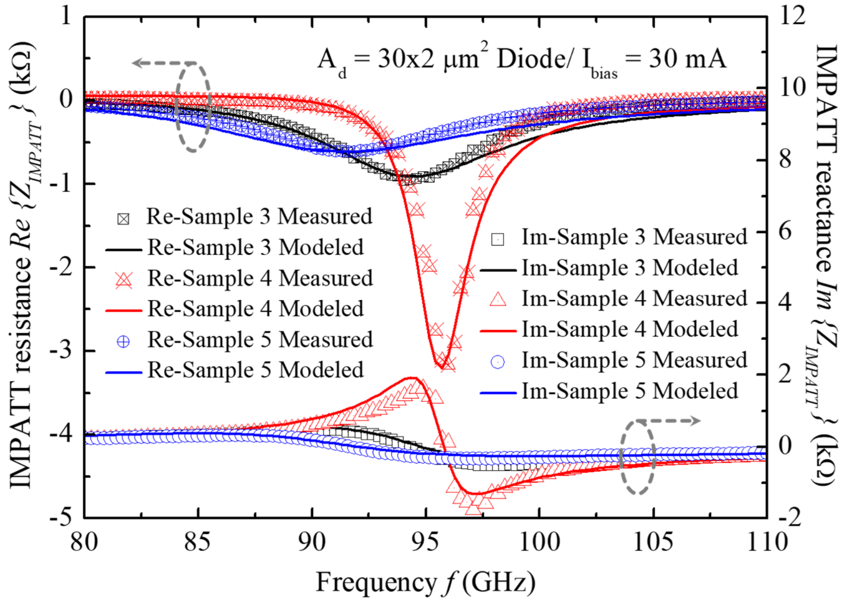


Figure 3.14: Modeling vs. measurement for the IMPATT functional $A_d = 30\times2$ μm^2 diodes of Sample 3-5 under biasing current of $I_{bias} = 30$ mA.

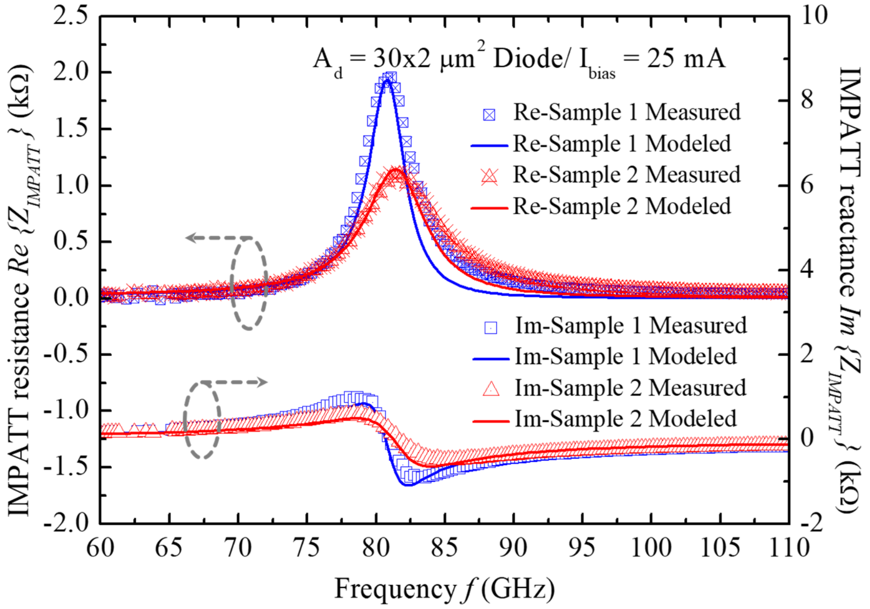


Figure 3.15: Modeling vs. measurement for the IMPATT nonfunctional $A_d = 30\times2$ μm^2 of Sample 1&2 under biasing current of $I_{bias} = 25$ mA.

3.4.3 *Numerical analysis on IMPATT functionality*

As mentioned, the two parameters G and R_L in the lumped-element model cannot be verified via single measurement. In particular, the noise-coupled resistive loss R_L is difficult to predict for the following reasons: (1) $1/f$-noise is quite sensitive to technology process [108] (e.g. material purity and surface properties of the device); (2) thermal noise shows a strong instability even with a slight temperature variation; (3) total noise could be amplified further by the avalanche mechanism, which is again dependent on the temperature effects on ionization coefficient and carrier velocity. For modeling, the combination of G and R_L determines the amplitude on both the real and imaginary part spectra of the IMPATT impedance at and near the avalanche frequencies. The relationship between G and R_L still needs further investigations from the device physics aspect, which makes the quantitative separation of the parameter pair difficult.

However, according to the measurement, the fitted model in subsection 3.4.1 enables a numerical analysis of the relevant IMPATT resistance, which shows the effects of the G and R_L pair on the basic IMPATT functionality (NDR).

Based on the established lumped-element model in Figure 3.13, the IMPATT impedance (Z_{IMPATT}) can be written as:

$$Z_{IMPATT} = R_s + \frac{R_L + R_L^2 \cdot G + L_j^2 \cdot G \cdot \omega^2 + j \cdot \omega \cdot (L_j - R_L^2 \cdot C_j - L_j^2 \cdot C_j \cdot \omega^2)}{(1 + R_L \cdot G - L_j \cdot C_j \cdot \omega^2)^2 + (R_L \cdot C_j + L_j \cdot G)^2 \cdot \omega^2} \quad , (35)$$

with $\omega = 2 \cdot \pi \cdot f$ and $G < 0$. The real part of the IMPATT impedance can then be expressed as:

$$Re\{Z_{IMPATT}\} = R_s + \frac{R_L + R_L^2 \cdot G + L_j^2 \cdot G \cdot \omega^2}{(1 + R_L \cdot G - L_j \cdot C_j \cdot \omega^2)^2 + (R_L \cdot C_j + L_j \cdot G)^2 \cdot \omega^2} \quad , (36)$$

which represents the total IMPATT resistance.

Let us take the parametric values of the modeled IMPATT nonfunctional Sample 1 with biasing current $I_{bias} = 25$ mA (Table IV) as an example to initialize equation (36).

Table IV: Parameters of the modeled $A_d = 30\times2$ µm^2 diode on Sample 1 with biasing current $I_{bias} = 25$ mA

$A_d = 30\times2$ µm^2 diode	R_s (Ω)	C_j (fF)	L_j (pH)	R_L (Ω)	G (Ω^{-1})
Sample 1	6.6	20.0	190.0	9.0	$-4.0\cdot10^{-4}$

Initially, R_L is taken from the measurement-matched case to $R_L = 9.0\ \Omega$ (Table IV). Figure 3.16 shows the IMPATT resistance $Re\{Z_{IMPATT}\}$ as function of frequency 0 GHz $\leq f \leq$110 GHz with G varied in the range of -0.005 $\Omega^{-1} \leq G \leq$ -1.0·10^{-14} Ω^{-1}. There are three interesting points to be observed: (1) A transition at $G \approx$ -0.001 Ω^{-1} between positive and negative IMPATT resistances occurs (the measurement-matched curve is on the positive side); (2) A very weak carrier amplification is not sufficient to achieve a negative IMPATT resistance; (3) A strong carrier amplification could also weaken the negative IMPATT resistance.

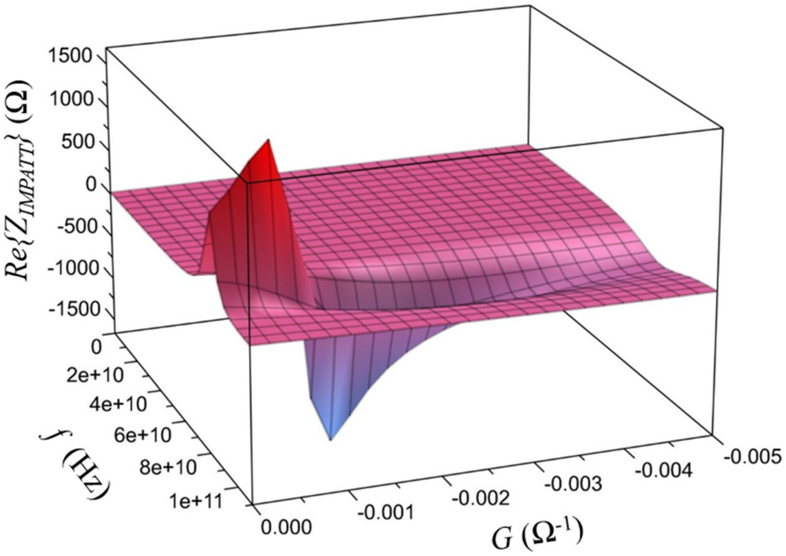


Figure 3.16: Effect of avalanche-induced carrier amplification G varied in range of -0.005 Ω^{-1} $\leq G \leq$ -1.0·10^{-14} Ω^{-1} on IMPATT resistance $Re\{Z_{IMPATT}\}$ with noise-coupled resistive load R_L= 9.0 Ω (measurement-matched).

Then, G is taken from the measurement-matched case as $G =$ -4.0·10^{-4} Ω^{-1} from Table IV. R_L varies within 0 $\Omega \leq R_L \leq$ 50 Ω to study its effect on IMPATT resistance in Figure 3.17. The transition between positive and negative IMPATT resistances occurs again. The measurement-matched curve belongs to the positive IMPATT resistance region. Only with a sufficiently small R_L < 3 Ω the IMPATT functionality (negative resistance) can be regained near an avalanche frequency of $f_{av} \approx$ 80 GHz.

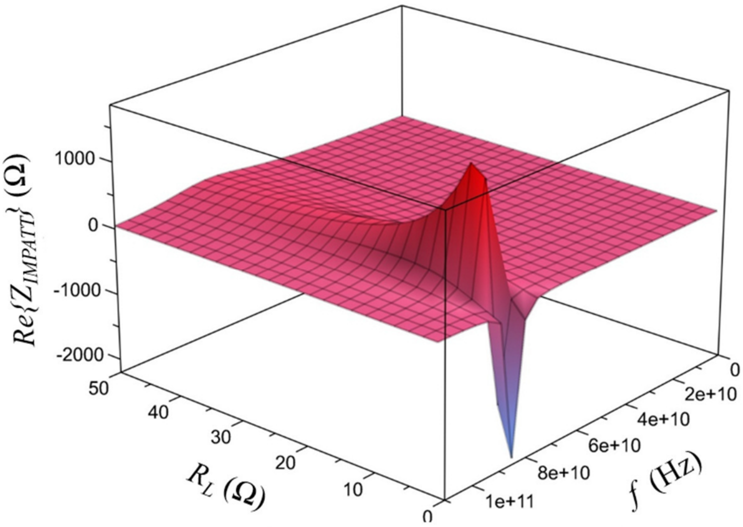


Figure 3.17: Effect of noise-coupled resistive load R_L varied in range of 0 Ω ≤ R_L ≤ 50 Ω on IMPATT resistance $Re\{Z_{IMPATT}\}$ with avalanche-induced carrier amplification G = -4.0·10^{-4} Ω^{-1} (measurement-matched).

This numerical study shows the impact of the $R_L - G$ combination on the fundamental IMPATT functionality intuitively. The avalanche frequency f_{av} remains uninfluenced as expected.

3.5 STUDY ON DEVICE THERMAL ENDURANCE UNDER IMPATT OPERATION

As discussed in subsection 3.3.1, the avalanche frequency f_{av} can be shifted in higher range just by increasing biasing current, which is very advantageous for IMPATT devices to gain the NDR over a large frequency range by circuit design. However, the Si-based IMPATT operation in CW mode is limited mainly by the thermal considerations due to high current density for applications with $f < 100$ GHz [86], as for monolithic design concretely, by the power which can be dissipated in a semiconductor chip. Thus, the huge heat sink directly mounted underneath IMPATT diode for the conventional discrete design became a must to ensure the CW performance with high output power under an acceptable thermal frame. For monolithic IMPATT design in this dissertation an externally mounted heat sink is technologically excluded, which means, that the thermal endurance of the chosen embedded IMPATT diodes should be experimentally precisely predicted before any concrete circuit design starts.

According to the definition of the IMPATT avalanche frequency f_{av}, proposed by Read [43] and complemented by Gilden and Hines [104] as:

$$f_{av} = \frac{1}{2 \cdot \pi} \sqrt{\frac{2 \cdot v_s \cdot \alpha'}{\varepsilon}} \sqrt{J} \qquad , \qquad (37)$$

where v_s is the saturation drift velocity of the carriers, α is the ionization coefficient, α' is its derivative with respect to the electrical field, ε is the permittivity of the material ($\varepsilon = \varepsilon_0 \cdot \varepsilon_r$ with ε_0 the permittivity of vacuum and ε_r the relative permittivity of material), and J is the current density through the device. Without considering the temperature effect during IMPATT operation (constant v_s and α'), f_{av} is supposed to be proportional to the square root of the DC biasing current density $\sqrt{J}$.

To understand how the device thermal endurance influences the IMPATT performance for monolithic circuit design, a comparison between the theoretically defined avalanche frequency f_{av} without temperature consideration and the measured ones with temperature effect has been made. Diodes with different dimensions ($A_d = 30\times2$ µm^2; 30×4 µm^2; 30×6 µm^2; 30×10 µm^2) on sample V984-1-1 have been measured under carefully increased DC currents until they just burned out due to over biasing.

In Figure 3.18 the estimated and measured avalanche frequencies f_{av} over square root of current density $\sqrt{J}$ characteristics of investigated IMPATT diodes are presented. The solid line shows the theoretical estimation without considering the temperature effects on v_s and α'. However, this proportionality is limited by the increasing device temperature which is decided by high delivered power for the given diode area and degrades both v_s and α' in reality. Thus, to drive the given diode in higher-frequency regime, a biasing current density larger than the theoretically estimated case has to be applied. This indicates both the importance of the heat sink in conventional discrete design and the challenge for monolithic implementation due to the thermal consideration of the embedded device. Additionally, under increasing $\sqrt{J}$ the diode with large dimension (e.g. $A_d =$ 30×10 μm^2) shows early the temperature limitation, which is not shown by the diode with small dimension (e.g. $A_d =$ 30×2 μm^2) until further increased $\sqrt{J}$. Thus, by simply shrinking the device dimension the IMPATT diode can be driven in higher frequency regime. Furthermore, if the devices offer similar avalanche frequency, the low operation current range of small dimension diode is preferred for circuit design to avoid the overheating problem. This is a relevant consideration to optimize the IMPATT diode design before the monolithic component or circuit implementation.

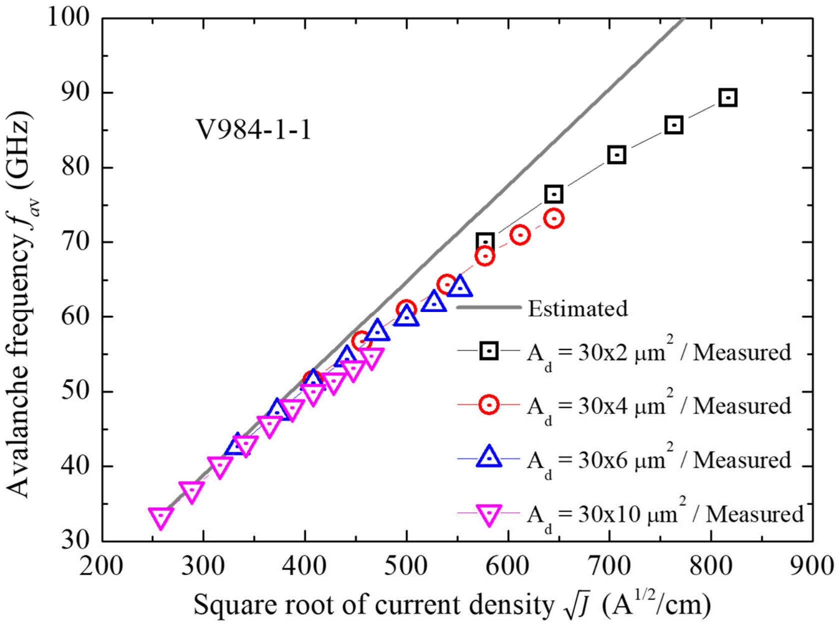


Figure 3.18: Estimated and measured avalanche frequency over square root of current density characteristics for A_d = 30×2 μm^2 ; 30×4 μm^2; 30×6 μm^2; and 30×10 μm^2 IMPATT diodes on sample V984-1-1.

Plenty of literature can be found for the basic thermal flow/limitation analysis [109]-[110] and measurement/improvement [111]-[112] based on avalanching devices with large dimension (A_d ~10^{-4} cm^2) for discrete design. But for monolithic design with much smaller IMPATT devices (A_d ~ 10^{-8} cm^2) burn out tests show that, even the layout design could significantly influence the overall device thermal endurance.

Figure 3.19 shows the scanning electron microscopy (SEM) pictures of burned out IMPATT diodes with different layout designs due to over biasing. Two $A_d = 30\times2$ μm^2 diodes with the same active layers but different layout designs were chosen for burning out tests. Under the carefully increased biasing currents, the design “Layout 1” (Figure 3.19-a) burned out earlier than the “Layout 2” (Figure 3.19-b) and explosively (Figure 3.19-c). After further increased $\Delta I_{bias} =$ 7 mA, “Layout 2” burned out too, but in a smoother manner (Figure 3.19-d).

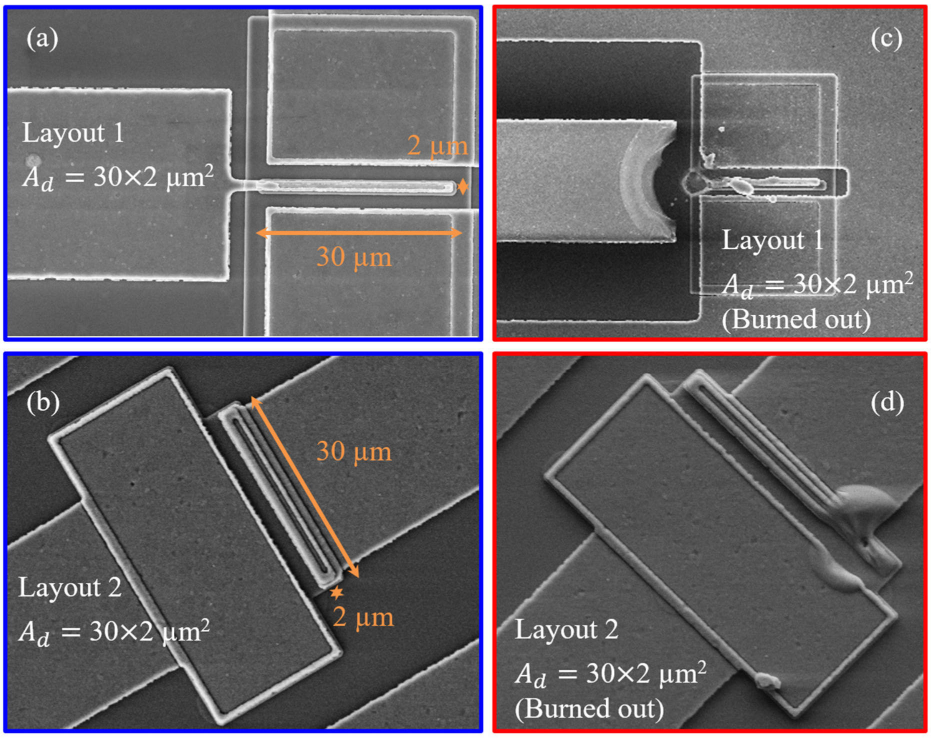


Figure 3.19: SEM pictures of $A_d = 30\times2$ μm^2 diodes only with different layout designs before and after burning out.

With the second look, it is found out that, the explosive burning out center of the “Layout 1” design occurred not at the p-n junction but the thin Al contact line, which was limited by the corresponding process quality. This indicates that, the thermal weak point of the embedded IMPATT device could be restricted by other technological factors than the “fragile” p-n junction itself. Before starting a reliable monolithic IMPATT circuit design, it is necessarily suggested to perform the burning out test experimentally for the chosen embedded diode to predict the upper limit of the device thermal endurance related to the allowed biasing condition in reality. At least $\Delta I_{bias} = 5$ mA biasing tolerance prior to the critical value extracted from burning out tests was taken for IMPATT circuit designs in this dissertation.

Chapter 4. IMPATT OSCILLATOR

Once the device properties are well understood, the design and monolithic implementation of IMPATT oscillators can be further performed. An oscillator is the circuit component, which can convert the NDR property of the IMPATT device eventually into microwave power out of DC biasing. An extensive design and characterization flow of IMPATT oscillators are given in this chapter.

4.1 PRINCIPLE FOR DESIGN OF IMPATT OSCILLATOR

The design principle of an IMPATT oscillator is straightforward to understand and very practical to use in the discrete-design dominated 1970s. The IMPATT diode, as illustrated in Figure 4.1, whose top side is contacted via a helical spring to a DC biasing block and whose bottom side is tightly pressed on a huge heat sink, is mounted vertically inside bulky hollow waveguides.

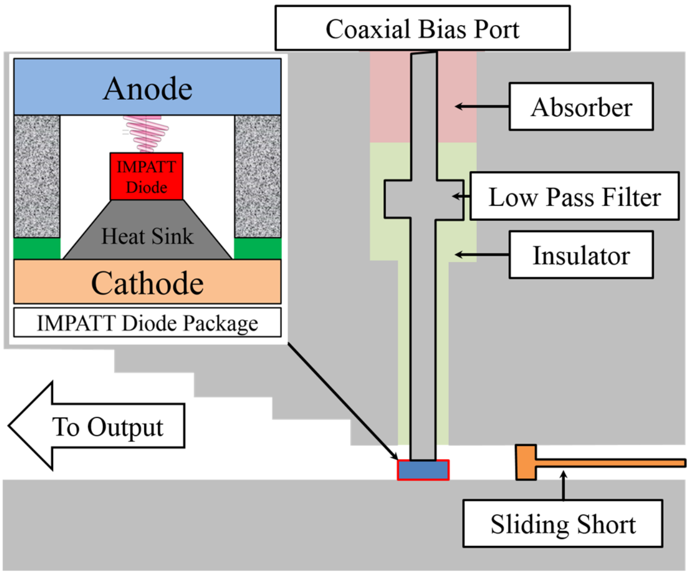


Figure 4.1: Principle of discrete design for a conventional IMPATT oscillator.

Laterally, a waveguide sliding short structure offers a wide tuning possibility on the right side of the IMPATT diode, while the output is formed by a tapered waveguide on the left side.

There are mainly three advantages of this design strategy: (1) DC biasing together with a sliding short could offer a sufficient tuning degree of freedom to meet the impedance matching condition for steady oscillation, as long as the IMPATT diode is functional; (2) a huge heat sink directly beneath the IMPATT diode improves the thermal endurance of the total device efficiently, thus the insurance of the impedance tuning range; and (3) it is straightforward to understand and convenient to perform in practice. Therefore, various IMPATT components like amplifiers, oscillators or even transceiver systems from several to even hundreds of gigahertz were successfully designed simply by mounting the device to a suitable cavity resonator previously without precise RF characterization of the IMPATT diode itself [113]-[115].

Owing to progress in VLSI technology, the implementation of monolithic IMPATT components like oscillators [116]-[122], or even transmitter-receiver systems [123] becomes increasingly attractive. A monolithic solution meets the general trend of small footprint, high yield, and low power consumption compared with discrete designs. However, the on-chip tuning possibility is largely reduced, thus the IMPATT device itself needs to be sufficiently precise, so that the fulfillment of the condition for steady oscillation under various design and technological uncertainties could still be well met.

4.1.1 *Short-ended CPW resonator*

For the monolithic IMPATT oscillator design using SIMMWIC technology in this dissertation, a similar construction to the one illustrated in Figure 4.1 has been employed. Only the active IMPATT device becomes embedded and the bulky hollow passive networks have been replaced by planar CPW lines on high-resistivity Si with $\rho_s > 1000$ Ω·cm.

The CPW concept was invented by C. P. Wen in 1969 [124] and its attenuation behavior was well studied a year later [125]. Different from the classic microstrip transmission-line placed on the substrate's top with its corresponding ground plane setting on the substrate's bottom, CPW line has the configuration of two ground electrodes placing adjacent and parallel to the signal strip line on the same side of the substrate.

Besides the specific nonreciprocal gyromagnetic device applications emphasized in the title of Wen's first CPW publication [124], the reason for such a widespread application of the CPW transmission-line nowadays is actually the convenience for the characteristic-impedance-stable connections to further active microwave components. As the other name of the CPW line indicates, under certain substrate thickness the characteristic impedance of this "surface-strip transmission-line" is determined mainly by the configuration of (1) the width of the signal line and (2) the gap distance between the signal line in the middle and the symmetrical ground planes aside. This scaling flexibility meets also the requests of on-wafer microwave measurements for small-dimensional DUTs but impedance-continued contact interface with well-defined reference planes. Thus, over 80 % of analog RF components designed for on-wafer measurement have CPW inputs or outputs. Even for the on-wafer differential coplanar strip (CPS) line designs the ground planes are often preferred to be located on the same side (GSSG configuration) for easy bonding access to off-wafer coaxial cables or on-wafer probe tips for measurement purpose.

The CPW solution can be adapted conveniently to any available technologies. For the mainstream CMOS or BiCMOS technologies with advanced BEOL processes the CPW lines could be flexibly developed in many variations e.g. CPW with ground (CPWG, also as grounded CPW), which enables fields propagation combined with microstrip and CPW modes. For locally potential-stable RF grounds design in complex system, a stacked CPW solution with different metal layers in BEOL is also available.

On the other hand, for academia clean-room technologies only with elementary one-layer metallization processes, reliable CPW transmission or reflection lines with desired characteristic impedance could still be well realized. The S-parameter characterization of the short-ended CPW resonator was performed. The in-house fabricated short-ended CPW resonators with different lengths from $L_{short} = 200$ µm to $L_{short} = 380$ µm (in 20-µm steps) were measured with the aimed frequency band (66 GHz $\leq f \leq$ 76 GHz with 6.25-MHz step) to illustrate the corresponding reflection coefficient Γ for an IMPATT oscillator design with operating frequency $f_{op} = 70$ GHz in the impedance Smith chart (Figure 4.2).

According to these measurement results, an efficient tuning effect of the inductive reactance in the range of 50 $\Omega \leq x \leq$ 300 Ω was achieved through the adopted length variation. This is the main factor to compensate the comparable capacitive reactance offered by the active IMPATT diode at the same frequency band. Extracted from the measured data in Figure 4.2, a small resistance $r < 10\ \Omega$ was characterized, which should be taken into account for resistive compensation during the oscillator design.

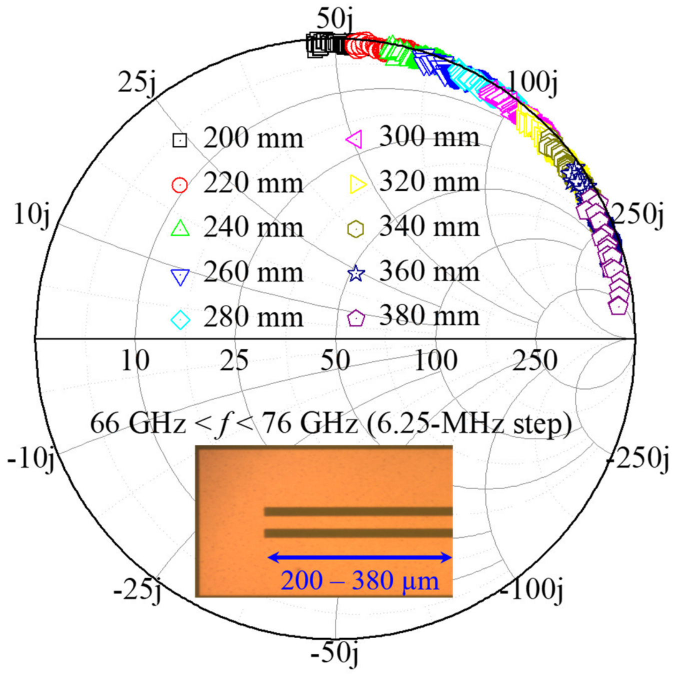


Figure 4.2: Reflection coefficient Γ of short-ended CPW resonators with lengths from $L_{short} = 200$ µm to $L_{short} = 380$ µm in measuring frequency range 66 GHz $\le f \le$ 76 GHz (6.25-MHz steps) on the impedance plane of Smith chart.

4.1.2 *Verification of Barkhausen's criteria and Kurokawa condition*

The experimental observation of a stable oscillation was first given by German physicist Heinrich Georg Barkhausen and his assistant in 1920 during their study on a vacuum tube feedback oscillator [126]. Fifteen years later Barkhausen condensed systematically the mathematical description of the necessary condition in frequency domain from transfer function matching aspect for steady oscillation in his textbook [127], which is known as the famous "Barkhausen's criteria" and widely applied to transistor-based oscillator and amplifier designs with modern CMOS technologies [128].

For an oscillation loop specifically built up by one-port active devices such as an IMPATT diode, Esaki diode [129], Gunn element [130], which can offer broadband NDRs, Kaneyuki Kurokawa at Bell Labs derived extensively the condition in time domain from impedance matching aspect for free-running stable oscillations and the injection-locking phenomena in 1969 thus provided a systematic guide for the design of broadband negative resistance oscillator circuits [131]-[132]. Even the mathematical core remains the same as Barkhausen's criteria, Kurokawa condition is better known for the NDR-based oscillator design due to its easily understood impedance matching expression.

Figure 4.3 illustrates a general oscillator loop consisting of an amplifier block (active element) and a feedback network block (passive component). In Barkhausen's criteria, two conditions have to be fulfilled at the same time so that a stable oscillation occurs: (1) the multiplication of amplifier gain $A(j\omega)$ and the transfer function $\beta(j\omega)$ of the feedback network $|A(j\omega)\cdot\beta(j\omega)|$ should equal to 1 in absolute magnitude; (2) the loop phase shift through the amplifier and the feedback network $\Delta\varphi\{A(j\omega), \beta(j\omega)\}$ should be zero or an integer multiple of $2\cdot\pi$. The same mathematical core of the Barkhausen's criteria can be expressed as Kurokawa condition from the aspect of the impedance matching, that the sum of all loop impedances ($Z_{Amplifier} + Z_{Feedback\ Network}$) should be equal to zero. Since the impedance yet consists of resistance and reactance, which includes both the magnitude and phase information of the entire loop in Kurokawa condition.

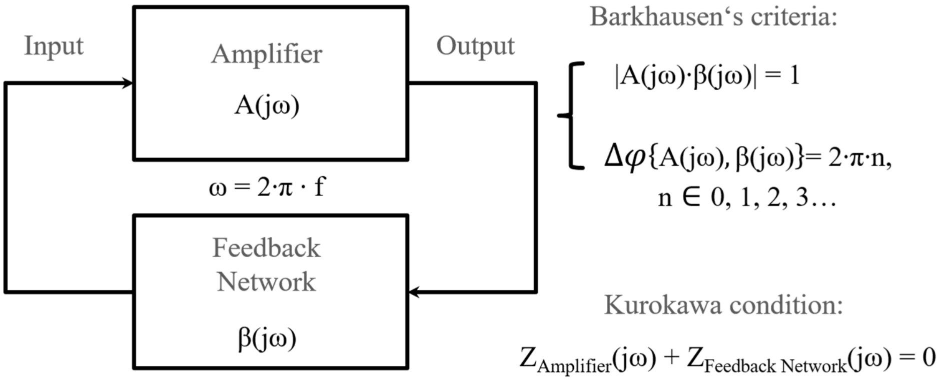


Figure 4.3: Oscillator block diagram with Barkhausen's criteria and Kurokawa condition.

The topology of the designed E-band oscillators is shown in Figure 4.4 with its corresponding equivalent circuit. It contains on one side of the monolithic integrated IMPATT diode a CPW short-ended resonator with length of L_{short} and on the other side a CPW line with length of L_{match} which provides smooth impedance matching towards the standard $Z_{load} = 50\ \Omega$ of the VNA measurement system.

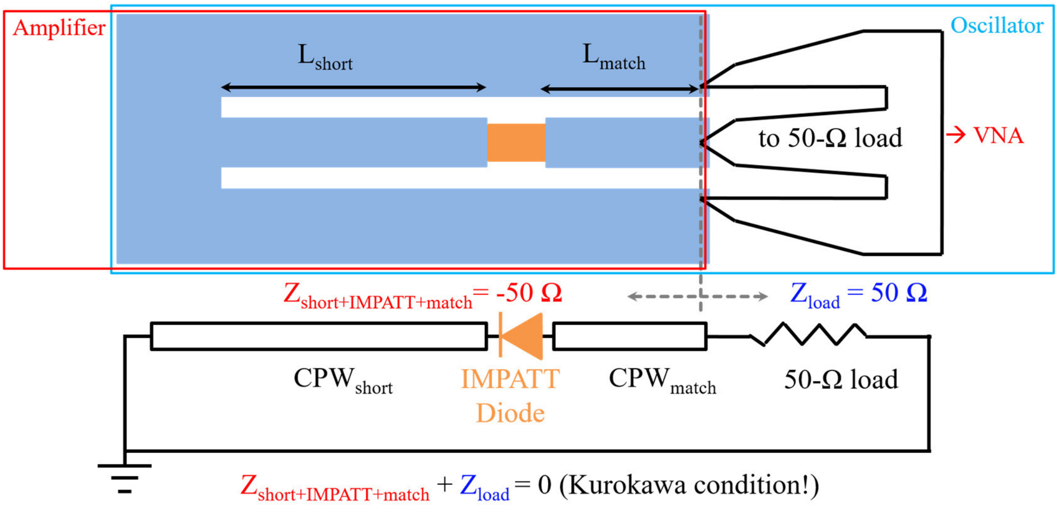


Figure 4.4: Design topology of monolithic IMPATT oscillators with its corresponding equivalent circuit model under VNA characterization and Kurokawa condition for steady oscillation.

According to the Kurokawa condition for steady state oscillation, the total impedance should be zero at the oscillation frequency f_o:

$$Z_{short+IMPATT+match+load}(f_o) = 0 \quad . \tag{38}$$

With $Z_{load} = 50\ \Omega$ at the reference plane (grey-dotted line in Figure 3.4) defined by S-parameter VNA measurement, equation (38) can be simplified as the following:

$$Z_{short+IMPATT+match} = -50\ \Omega \quad . \tag{39}$$

This means, to meet the Kurokawa condition in real design, the short-ended CPW resonator, the embedded IMPATT diode, and the CPW matching line should offer totally $Z_{short+IMPATT+match}$ = -50 Ω together at exactly the same desired oscillation frequency f_o. Otherwise no oscillation occurs.

Besides the S-parameter measurement results of short-ended CPW resonator with different lengths (Figure 4.2), IMPATT diodes with different dimensions under certain biasing currents were characterized, too. Figure 4.5 presents the results of the small-signal S-parameter characterization for a A_d = 40×2 μm^2 IMPATT diode under biasing current from I_{bias} = 20 mA to I_{bias} = 40 mA with measuring frequency range 40 GHz ≤ f ≤ 80 GHz.

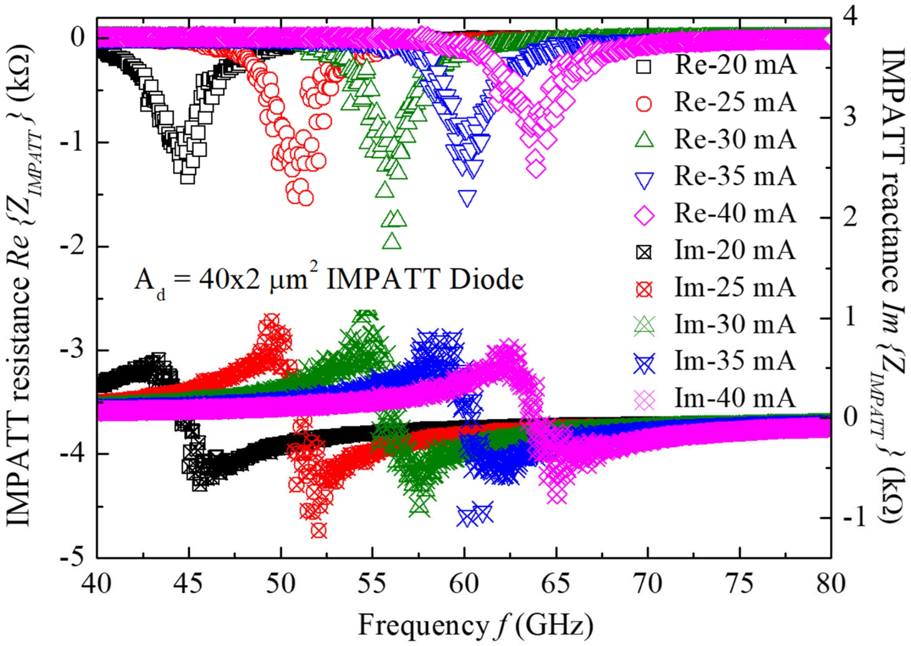


Figure 4.5: Real- and imaginary-impedance spectra (frequency range: 40 GHz $\leq f \leq$ 80 GHz) of a A_d = 40×2 μm^2 IMPATT diode extracted from small-signal S-parameter characterization within biasing current from I_{bias} = 20 mA to I_{bias} = 40 mA (5-mA steps).

With the positive impression of the large bandwidth of characterized NDR is not enough yet to design an efficient monolithic IMPATT oscillator in reality, since the usable design bandwidth is quite limited due to frequency-correlated impedance level offered by CPW lines. Thus, with overall consideration of the impedance matching possibility offered by the chosen passive component (short-ended CPW resonator and matching line), the flatness of the impedance change with biasing current, and the biasing current tolerance defined in section 3.5, the suitable design bandwidth was aimed within 66 GHz $\leq f \leq$ 76 GHz for A_d = 40×2 μm^2 diode under the biasing current of I_{bias} = 40 mA.

In Figure 4.6 the impedance courses of the real- and imaginary-part at f = 70.5 GHz are shown as an example for indicating a usable design band for the above mentioned A_d = 40×2 μm^2 diode. The biasing dependent IMPATT impedance level for resistance –100 Ω $\leq Re\{Z_{IMPATT}\} \leq$ 0 Ω and reactance –370 Ω $\leq Im\{Z_{IMPATT}\} \leq$ -70 Ω is concretely presented at the aiming frequency f = 70.5 GHz over biasing range of 20 mA $\leq I_{bias} \leq$ 40 mA. The different changing gradient of the resistance and reactance over biasing current indicates that, using passive component to compensate resistance, reactance and in the meantime at the same desired frequency is quite challenging.

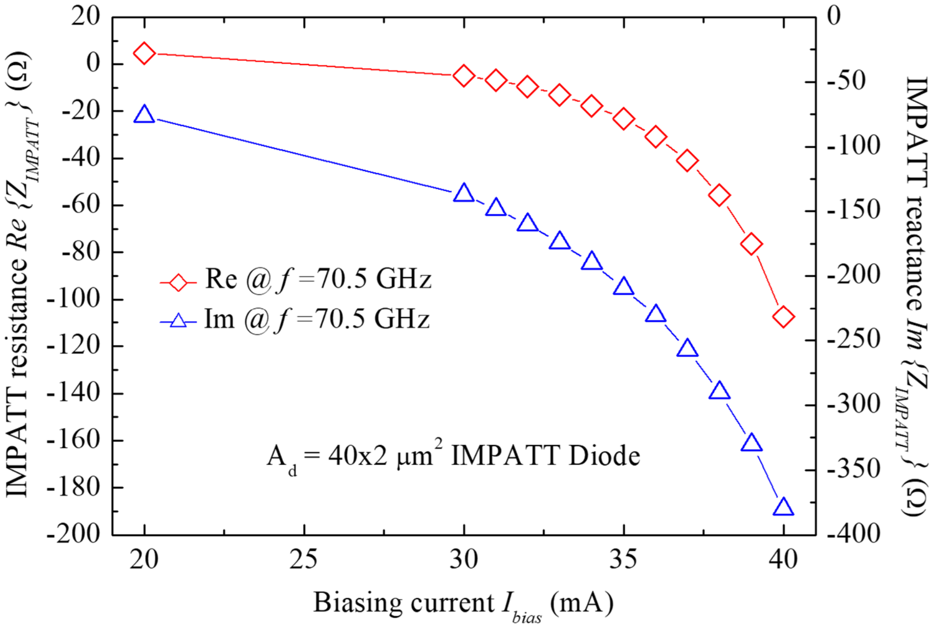


Figure 4.6: Impedance courses of a $A_d = 40\times2$ µm² IMPATT diode under different biasing currents (20 mA ≤ I_{bias} ≤ 40 mA) at $f = 70.5$ GHz. IMPATT area and bias conditions were chosen considering the realistic impedance level offered by employed CPW resonator and matching line.

Thus a practical designing-by-characterizing procedure has been performed to “measure out” the optimal combination of short-ended CPW resonator, IMPATT diode (with appropriate biasing condition), and the CPW matching line for oscillator design at the aimed frequency. All measured S-parameter data of these separate oscillator parts were transformed firstly to impedance spectra in real- and imaginary-part, then “assembled” together to check, if the total impedance both in real- and imaginary-part fulfills the Kurokawa condition expressed in equation (39).

Figure 4.7 demonstrates the above mentioned procedure concretely for the design of a oscillator with $f_{op} = 70$ GHz as an example. The total impedance $Z_{short+IMPATT+match}$ at $f = 70$ GHz is plotted each in resistance $Re\{Z_{IMPATT}\}$ @ 70 GHz and reactance $Im\{Z_{IMPATT}\}$ @ 70 GHz over biasing current 32 mA ≤ I_{bias} ≤ 40 mA of a $A_d = 40\times2$ µm² IMPATT diode, short-ended CPW resonator within length of 200 µm ≤ L_{short} ≤ 380 µm, and CPW matching line with $L_{match} =$ 100 µm. In spite of different changing gradients of the biasing-dependent IMPATT resistance and reactance, a biasing window of 37 mA ≤ I_{bias} ≤ 38 mA exists indeed within 340 µm ≤ L_{short} ≤ 360 µm of short-ended CPW resonator, in which the resistance varies between -40 Ω ≤ $Re\{Z_{IMPATT}\}$ ≤ –60 Ω, the reactance changes in range of -50 Ω ≤ $Im\{Z_{IMPATT}\}$ ≤ 50 Ω with maximal corresponding parasitic inductance value of L_{para} = 0.1 nH and capacitance of C_{para} = 45 fF. This indicates that the Kurokawa condition at f = 70 GHz in real design should be optimally fulfilled within biasing range 32 mA ≤ I_{bias} ≤ 40 mA for the monolithic design, which is the assembled version of the short-ended CPW resonator with L_{short} = 340 µm, A_d = 40×2 µm^2 IMPATT diode, and CPW matching line with L_{match} = 100 µm.

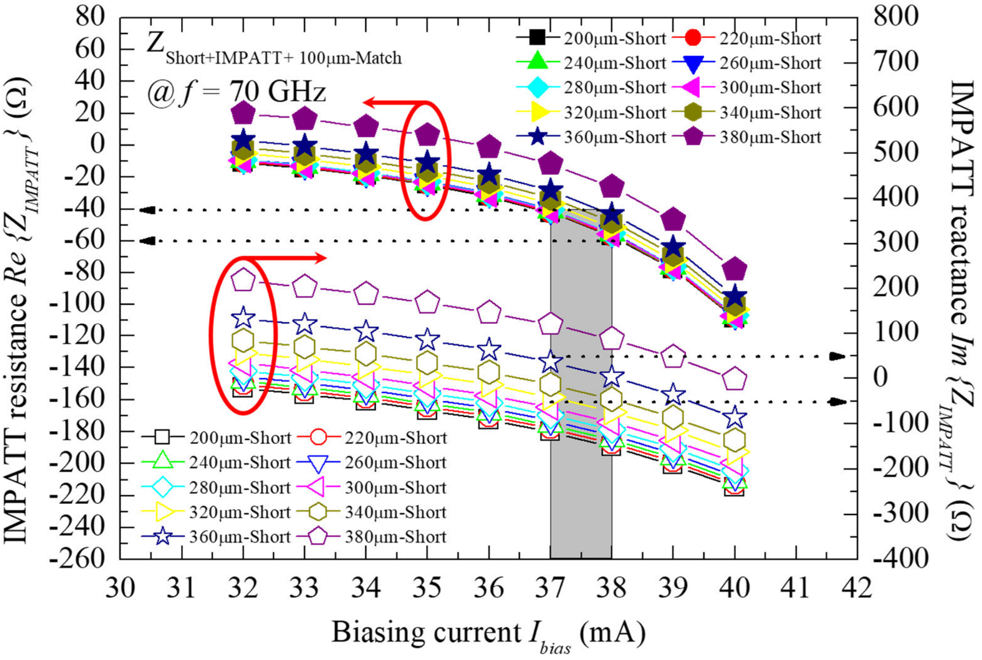


Figure 4.7: Demonstration of designing-by-characterizing procedure via an oscillator with f_{op} = 70 GHz is showing optimally fulfilled Kurokawa condition by assembling data of all separately characterized parts.

As mentioned above, Kurokawa condition and Barkhausen's criteria describe the same oscillation principle, only in different forms. This argument can be experimentally well verified in our design case. To convert an impedance matrix (Z-matrix) to S-parameter matrix (S-matrix) for one-port network (S_{11} normally represented as reflection coefficient Γ), the following equation is given:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \quad , \qquad (40)$$

with Z_0 the reference impedance of the system.

For the designed oscillator topology (Figure 4.4 & Figure 4.8), once the oscillation condition is verified as fulfilled at one chosen interface, the same condition should be fulfilled at any arbitrary interface. The reference plane is chosen for instance between the short-ended CPW resonator and the embedded IMPATT diode (grey-dotted line in Figure 4.8).

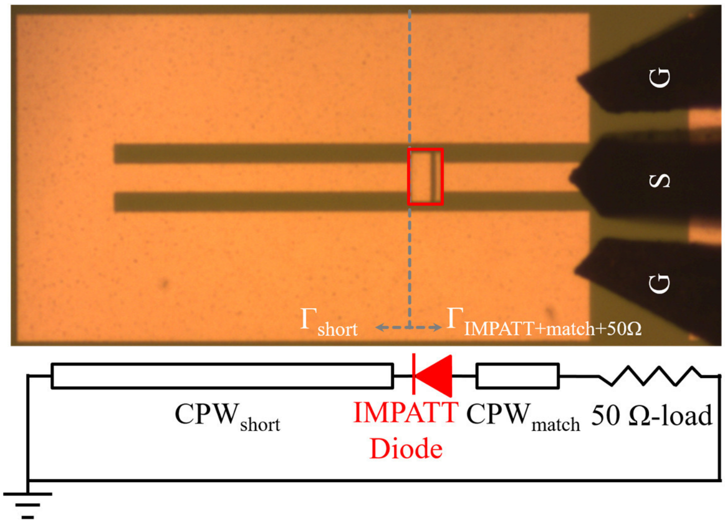


Figure 4.8: Oscillation condition expressed in form of reflection coefficient for the employed oscillator topology.

According to equation (40), we have:

$$\Gamma_{short} = \frac{Z_{short} - Z_0}{Z_{short} + Z_0} \quad , \qquad (41)$$

and

$$\Gamma_{IMPATT+match+50\Omega} = \frac{Z_{IMPATT+match+50\Omega} - Z_0}{Z_{IMPATT+match+50\Omega} + Z_0} \quad . \qquad (42)$$

If we transform equation (41) and (42) each in form of $Z_{short}(\Gamma_{short})$ and $Z_{IMPATT+match+50\Omega}(\Gamma_{IMPATT+match+50\Omega})$, we have then:

$$Z_{short} = Z_0 \cdot \frac{1 + \Gamma_{short}}{1 - \Gamma_{short}} \quad , \qquad (43)$$

and

$$Z_{IMPATT+match+50\Omega} = Z_0 \cdot \frac{1 + \Gamma_{IMPATT+match+50\Omega}}{1 - \Gamma_{IMPATT+match+50\Omega}} \quad . \qquad (44)$$

Equation (43) and (44) can be applied to equation (38), which describes the fulfilled Kurokawa condition at oscillation frequency f_o, as follows:

$$Z_0 \cdot \left(\frac{1+\Gamma_{short}}{1-\Gamma_{short}} + \frac{1+\Gamma_{IMPATT+match+50\Omega}}{1-\Gamma_{IMPATT+match+50\Omega}}\right) = 0 \qquad , \qquad (45)$$

which can be eventually simplified as:

$$\Gamma_{short}(f_o) \cdot \Gamma_{IMPATT+match+50\Omega}(f_o) = 1 \qquad . \qquad (46)$$

Equation (46) is exactly Barkhausen's criteria in Figure 4.3!

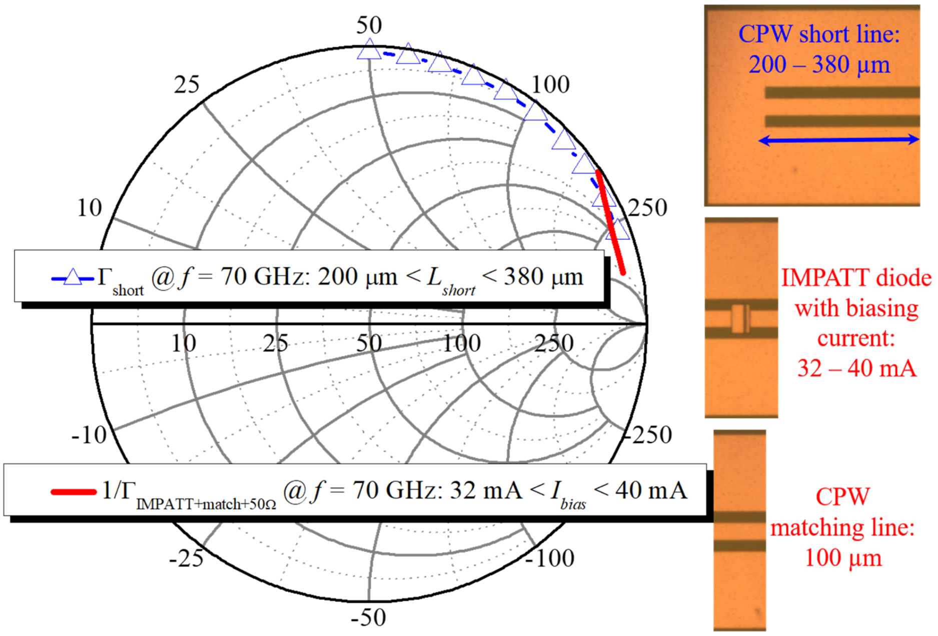


Figure 4.9: Demonstration of designing-by-characterizing procedure via an oscillator with f_{op} = 70 GHz is showing optimally fulfilled Barkhausen's criteria by assembling data of all separately characterized consisting parts.

In Figure 4.9, Γ_{short} and the reciprocal value of the reflection coefficient $1/\Gamma_{IMPATT+match+50\Omega}$ are plotted together at f = 70 GHz with exactly the same configurations of components listed in Figure 4.7 (CPW short line with 200 µm ≤ L_{short} ≤ 380 µm, A_d = 40×2 µm^2 diode with biasing current 32 mA ≤ I_{bias} ≤ 40 mA, and CPW matching line with length of L_{match} = 100 µm). The intersection of these two courses clearly verifies the fulfillment of the oscillation condition in Barkhausen's criteria as theoretically predicted.

4.2 CHARACTERIZATION OF IMPATT OSCILLATOR

With the experimentally step-by-step verified oscillation condition introduced in section 4.1, the design strategy by “assembling” all separate consisting parts together turns out to be reliable. However, to finalize the functionality of monolithically “assembled” oscillators, the oscillator-level characterization needs to be performed.

4.2.1 *Verification of oscillation condition via amplification spectrum measurement*

To qualitatively present the fulfillment state of the oscillation condition in an efficient way, all fabricated monolithic E-band IMPATT oscillators were characterized as reflective amplifier using VNA. As illustrated in subsection 4.1.2, Figure 4.4, the oscillation frequency is identical to the amplification frequency, only to transfer measured amplification spectrum quantitatively to oscillator power spectrum requires more carefulness and effort [133]-[134]. Concretely aiming at the final implementation of a functional monolithic E-band IMPATT transmitter, the quantitative verification of the oscillation frequency is more essential than that of output power for the antenna integration. By using Anritsu ME7808C Broadband (0.04 GHz $\leq f \leq$ 110 GHz) VNA system in-house, the oscillation frequency could be conveniently represented in amplification spectrum.

Figure 4.10 shows the measured spectra of the finalized f_{op} = 70 GHz monolithic IMPATT oscillator with L_{short} = 340 µm short-ended CPW resonator, A_d = 40×2 µm^2 IMPATT diode, and L_{match} = 100 µm CPW matching line. In non-biased state (I_{bias}= 0 mA), the IMPATT mode was not activated yet. Thus, no gain was observed for the entire frequency span in range 66 GHz $\leq f \leq$ 76 GHz with 6.25-MHz step. Under biasing current of I_{bias}= 37.11 mA, the IMPATT mode was switched on for the optimally fulfilled oscillation condition as verified in subsection 4.1.2. This leads to the measured maximum amplification gain of G_{max} = 45.7 dB at f = 70.54 GHz, which confirmed the optimally fulfilled oscillation condition in real design as expected.

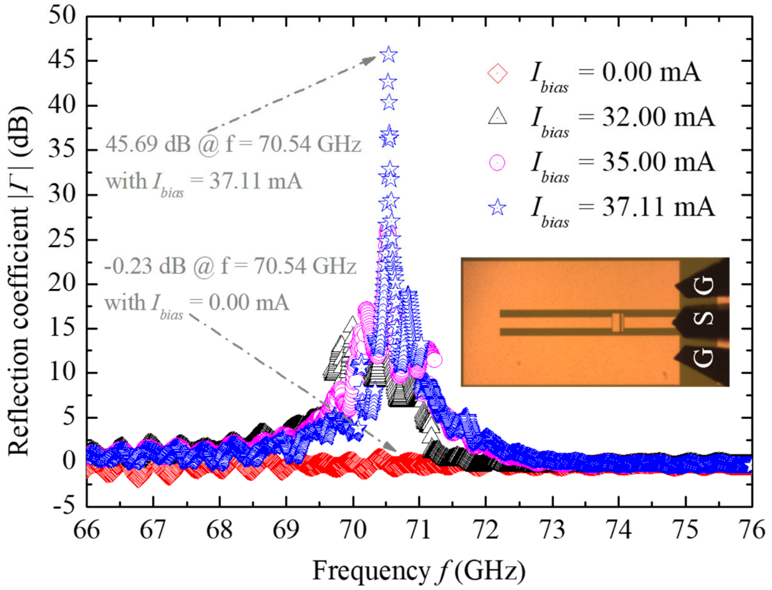


Figure 4.10: As reflective amplifier, the amplification spectra of the finalized monolithic IMPATT oscillator with f_{op} = 70 GHz is characterized by VNA under biasing current I_{bias} = 0 mA and 37.11 mA in frequency range of 66 GHz ≤ f ≤ 76 GHz.

Compared with the cases of I_{bias}= 32 mA and I_{bias}= 35 mA, the development process from initial state (I_{bias}= 0 mA) to meeting the optimal oscillation condition (I_{bias}= 37.11 mA within the predicted range 37 mA ≤ I_{bias} ≤ 38 mA in subsection 4.1.2) by tuning DC biasing current (impedance level offered by the embedded IMPATT diode) can be clearly comprehended. Under CW biasing the f_{op} = 70-GHz IMPATT oscillator was working without extra cooling element free of damage over 20 minutes, which indicates an efficient DC-to-RF conversation, too.

4.2.2 *Amplification spectra of all designed E-band IMPATT oscillators*

In spite of much less in-time tuning freedom by the monolithic design compared with the conventional discrete design introduced at beginning of section 4.1, the proposed designing-by-characterizing procedure for monolithic IMPATT oscillators is proven to be practical and reliable. The freedom to combine small-signal characterization results of separate consisting parts emulates the final monolithic designs in a much more reliable way. On the other hand, the essential huge heat sink in the discrete designs could be saved due to burn-out test of employed IMPATT diodes under proper thermal considerations (see section 3.5).

Different types of monolithic IMPATT oscillators were designed and characterized as reflective amplifier using VNA. Figure 4.11 presents their measured amplification spectra in the frequency range of 65 GHz $\leq f \leq$ 110 GHz. It is clearly observed, that almost the entire E-band (60 GHz $\leq f \leq$ 90 GHz) is well covered as intended. This is exactly due to the flexibility and the accuracy of the proposed designing-by-characterizing procedure.

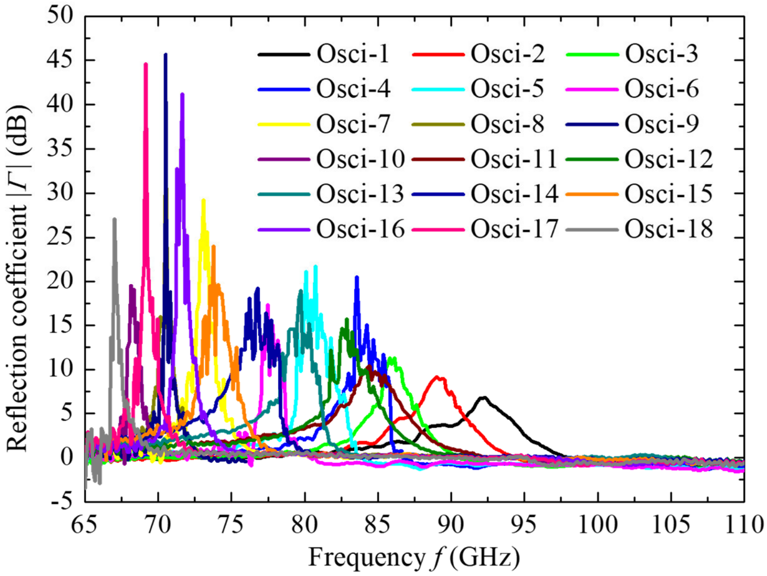


Figure 4.11: Amplification spectra of all designed E-band monolithic IMPATT oscillators.

Different gain amplitudes indicate the degree of the oscillation condition fulfillment. As presented in Figure 4.6, the biasing dependent IMPATT resistance and reactance change with different gradients. Thus, an optimally fulfilled oscillation condition is difficult to catch in real design for the entire E-band.

Considering the limited layout area and antenna design tolerance, the large integrated on-chip antenna was designed at $f_{op} = 82.5$ GHz (refer to section 5.2), which means only oscillators working around $f = 82.5$ GHz were chosen for the monolithic IMPATT transmitter design in this dissertation.

4.2.3 *Idea about power spectrum measurement in CW mode and in pulse mode*

For most of applications at millimeter-wave regime, a CW operation at certain frequency or in a tunable frequency range is desired. However much higher peak power (maximum 8 times larger [135]) can be obtained, if an oscillator is driven under a pulse rather than a continuous biasing. Specifically for IMPATT oscillator, the performance of DD diodes for high-efficiency power generation was experimentally verified as superior to that of SD diodes both in CW [136] and pulse mode [135]. Additionally, the pulse operation mode generates much less heat than CW mode, which protects IMPATT diodes from overheating (burning out).

The principle hardware setups for on-wafer oscillator power spectrum measurement are sketched in Figure 4.12. For approximately estimated power spectrum measurement (Figure 4.12-a), the setup consists of a spectrum analyzer as core, a harmonic mixer to mix high frequency signals directly generated by the oscillator as DUT down to the measurable range of the spectrum analyzer. This is the most common setup for approximately measuring power spectrum. The inaccuracy is mainly due to the difficulty to extract the conversion loss data of the harmonic mixer in its entire operation band.

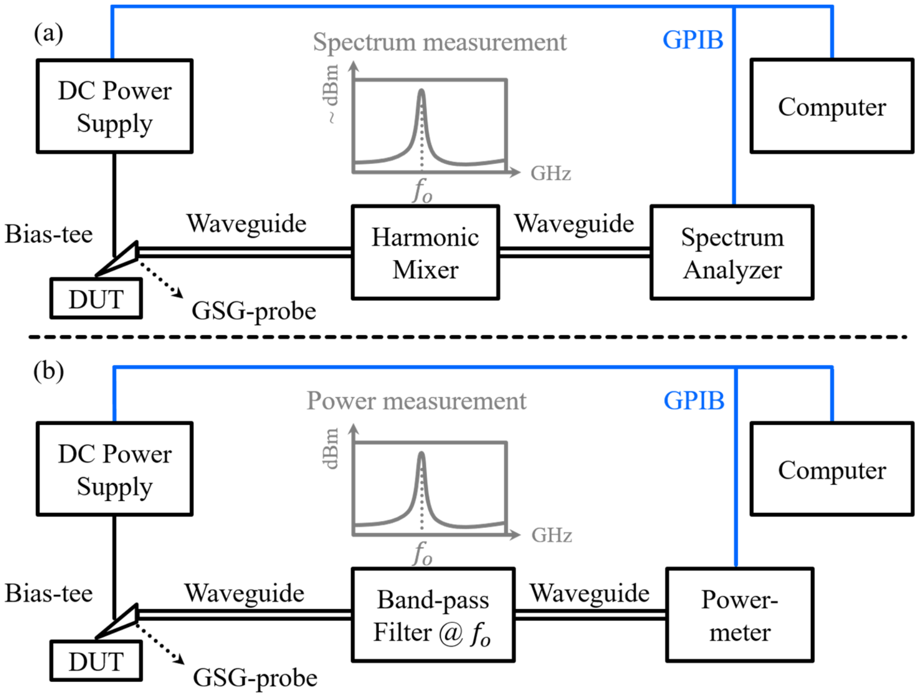


Figure 4.12: The principle setups for on-wafer power spectrum measurement in CW mode and in pulse modes.

To accurately measure the power spectrum, a setup based on power-meter in Figure 4.12-b can be used. A band pass filter ensures only signals within the interesting frequency band are led to the power-meter which normally has a much larger operation frequency band. In reality, spectrum-analyzer-based measurement setup is applied firstly to catch the general power spectrum. Power-meter-based setup is then used for the accurate power calibration at the most interesting frequency with peak output power. Combined with the general power spectrum measured by the spectrum analyzer and the accurate peak output power measured by the power-meter, the power spectrum of oscillators can be precisely extracted eventually. From this power spectrum, the oscillator phase noise can be extracted, too. In praxis, an E-H impedance tuner between GSG-probe and harmonic mixer/band pass filter is quite necessary for both setups in Figure 4.12, since an oscillator as DUT requires certain load resistance.

A general purpose interface bus (GPIB) cable connected with a control computer distinguishes power spectrum measurement setup in pulse mode from that in CW mode. The GPIB cable enables the synchronization between the DC power supply and the detecting equipment (spectrum analyzer or power-meter). For measurement in CW mode, the communication between the DC power supply for continuous biasing and the detecting equipment is not necessary. But to properly measure the power spectrum in pulse mode, the detecting equipment must "know" exactly the appropriate starting point in time-domain right after the corresponding DC excitation with certain pulse width and duty cycle, so that the original oscillator response can be well characterized.

4.2.4 *Possible idea for on-wafer injection- locking measurement*

In terms of the operation mode of the oscillator itself, two main modes are available: the free-running and the injection-locking. Free-running means, the system begins to oscillate without any externally injected signal. Injection-locking means, if a signal near to the free-running frequency is injected in to the system, the oscillator is then synchronized or locked to the injected signal. Here we just discuss the small-signal injection, which does not change the linearity of the investigated oscillators. The benefit of injection-locking operation is that the oscillator can be synchronized to an external signal, thus offers a better stability against surrounding noises.

For injection-locking measurement related to IMPATT oscillator, a circulator is normally required to separate the injection path and the output loading path [132]. An occasionally observed phenomenon during the amplification spectrum measurement (see subsection 4.2.1) sparked a possible idea for on-wafer injection-locking characterization without circulator.

In Figure 4.13 the local setup for on-wafer amplification spectrum measurement is shown. After the two-port thru-reflect-line (TRL) calibration [137], port 1 was moved about 1 cm away horizontally and about 7 mm vertically from the calibrating position, fully suspending in the air. Port 2 was employed to measure the oscillator with f_{op} = 70 GHz, whose amplification spectra are characterized in subsection 4.2.1.

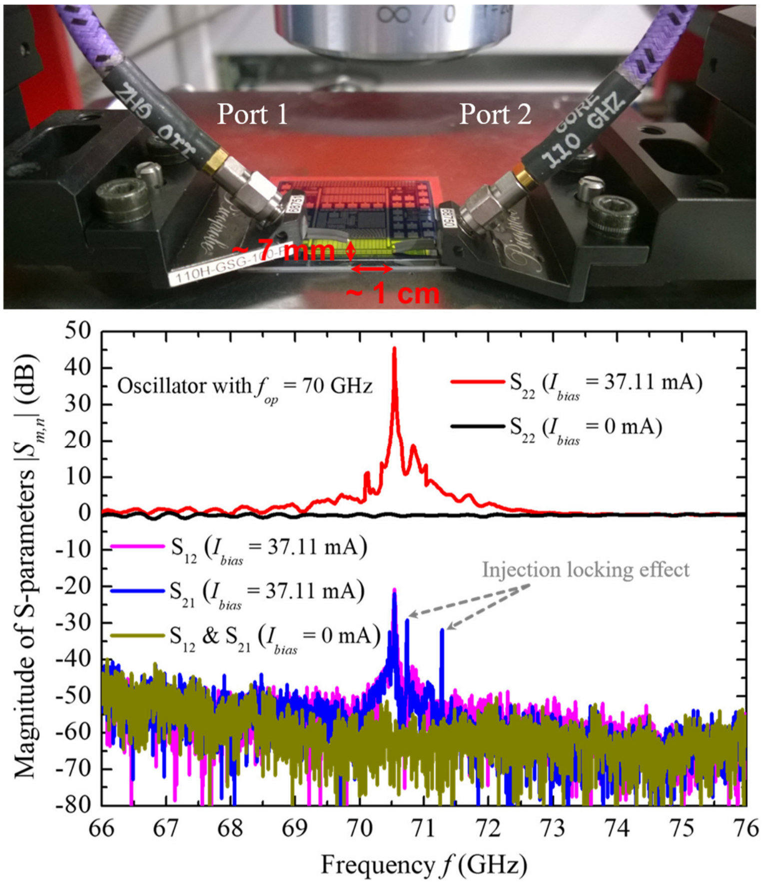


Figure 4.13: Possible injection-locking effect observed by amplification spectrum measurement using VNA.

S_{22} with biasing current I_{bias} = 0 mA (black) was taken as reference for port 2 measuring the oscillating case with I_{bias} = 37.11 mA. Compared with the noise floor for transmission S_{12} & S_{21} with I_{bias} = 0 mA (dark yellow), S_{12} (transmission from port 2 to port 1, pink) showed interestingly the same amplification spectrum as S_{22} (reflection from port 2, red) in the meantime with $I_{bias} = 37.11$ mA. More interestingly S_{21} (transmission from port 1 to port 2, blue) showed similar amplification spectrum but additionally some new peaks, which appeared neither in S_{22} nor in S_{12} spectra. Two things can be concluded from this phenomenon: (1) by port 2 generated oscillation signals could be transmitted via certain distance in free space and well received by GSG-probe of port 1; (2) port 1 could send out signals via GSG-probe and influence the original amplification spectrum of the oscillator under test at port 2, which indicates an injection-locking effect.

Chapter 5. IMPATT TRANSMITTER

As explained in section 2.1, in mainstream CMOS/BiCMOS technology the bottleneck of monolithic solution of entire transceiver is due to the on-chip antenna integration. This chapter extensively describes the on-chip antenna design and its integration with IMPATT oscillators, which are successfully characterized as monolithic IMPATT transmitter.

5.1 PRINCIPLE FOR DESIGN OF IMPATT TRANSMITTER

As extension of IMPATT oscillators, the design principle of the IMPATT transmitter becomes straightforward. Figure 5.1 shows the basic idea to extend the available IMPATT oscillator to transmitter. A CPW patch antenna with input impedance $Z_{in} = 50\ \Omega$ is chosen to replace the same load resistance of the VNA system. Then an IMPATT transmitter is supposed to be working.

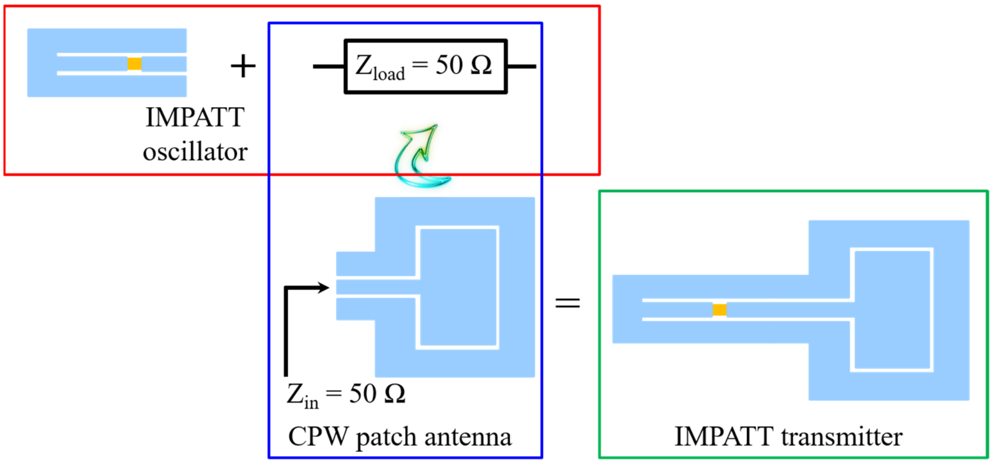


Figure 5.1: Design principle of monolithic IMPATT transmitter.

To realize this design principle, two challenges in reality are mostly concerned: (1) CPW patch antenna should offer precise 50-Ω input impedance to close the oscillator loop appropriately, thus ensures the generation of the exactly desired RF signals as it is by IMPATT oscillator; (2) the working frequency of narrow-bandwidth CPW patch antenna should well meet the generated RF signals, so that the RF signals can be efficiently radiated via CPW patch antenna into free space.

5.2 DESIGN OF CPW PATCH ANTENNA AT OPERATING FREQUENCY $f_{op} = 82.5$ GHZ

Since the IMPATT oscillator has a CPW output interface, a CPW-fed patch antenna [138]-[139] was chosen for monolithic integration. Additionally the CPW patch antenna has a radiating direction vertical to chip plane, which is quite convenient by spatial adjustment for transmitter test in far-field environment.

As mentioned above, the antenna should be on one hand part of the oscillator circuit and in charge of radiating the generated RF signals into free space on the other hand. To ensure the functionality of monolithic IMPATT transmitter as final product, the CPW patch antenna design has to be precise and feasible for the available SIMMWIC technology in house.

5.2.1 *Design specifications and dimensions of CPW patch antenna*

Two transmitter-relevant design specifications for the chosen CPW patch antenna were well met: (1) considering both the gain and the bandwidth of the amplification spectra offered by all available E-band oscillators, which are characterized in subsection 4.2.2 (Figure 4.11), the CPW patch antenna was designed with the center resonance frequency in reflection coefficient (S_{11}) spectrum at $f_{op} = 82.5$ GHz; (2) the input impedance $Z_{in} = 50\ \Omega$ of the CPW patch antenna was matched to $f_{op} = 82.5$ GHz to close the oscillator loop exactly as the oscillation condition (Barkhausen's criteria and Kurokawa condition) requires in subsection 4.1.2.

With the requirements above, the configuration with detailed dimensions of the designed CPW patch antenna is shown in Figure 5.2. Considering the line width resolution of $w_{lw} = 200$ nm by mask set manufacturing, all parameters are given to 0.2-µm precision. The in-house SIMMWIC technology could well achieve line width of $w_{lw} = 500$ nm with photolithography and $w_{lw} = 200$ nm with electron-beam lithography (EBL).

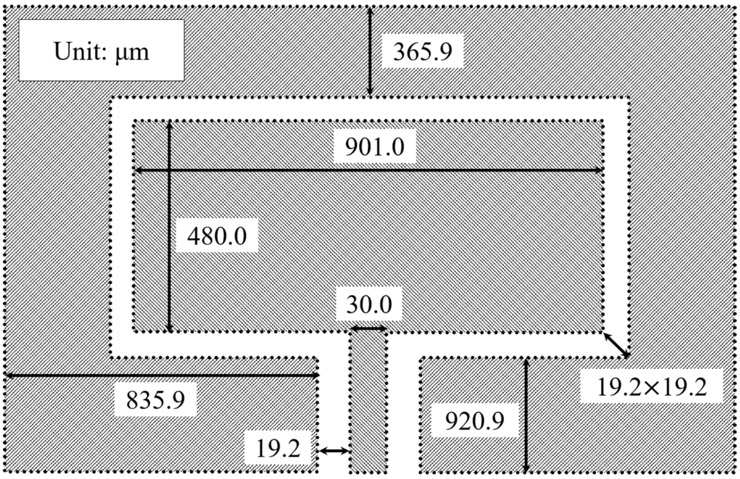
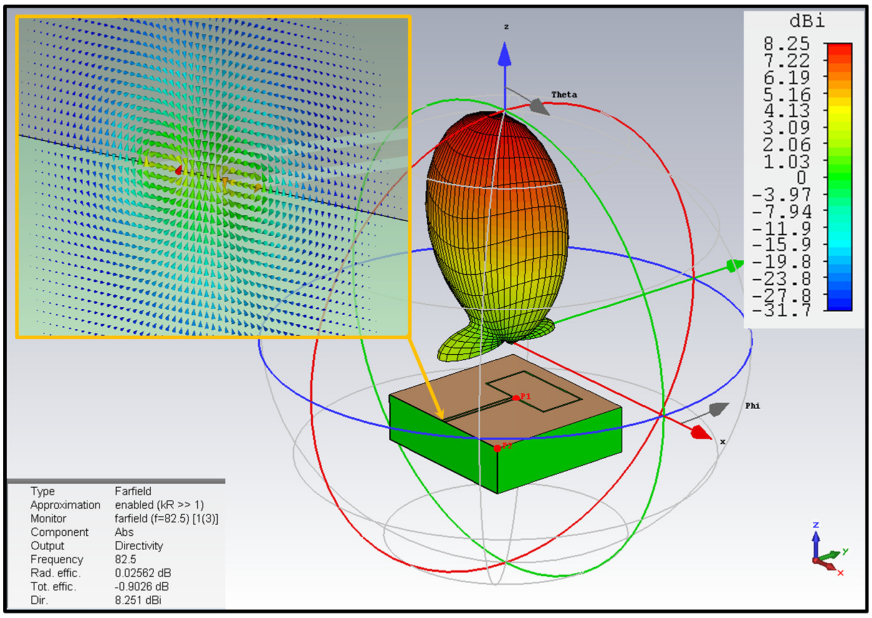


Figure 5.2: Configuration of the designed CPW patch antenna (unit: μm).

5.2.2 *3-D EM modeling of CPW patch antenna*

Until 1990s antenna EM simulation based mainly on 2-D and 2.5-D modeling, which were sufficient enough for the applications below $f \leq 40$ GHz (most of them for a few Gigahertz applications, e.g. communication band). The design flow was quite user-convenient and Si-based antenna on chip (AoC) were not that in demand.

Until recent years, AoC designers (especially with mainstream Si material which has a relatively high relative permittivity $\varepsilon_{r,si} \approx 11.7$) realize more and more clearly the challenges and problems by millimeter-wave AoC designing, which cannot be well predicted by 2-D or 2.5-D EM tools anymore. Due to wavelength comparable dimension of AoC, the design environment is getting more complex. Besides the conventional antenna configurations (radiation lengths, impedance matching) more effects from surroundings have to be taken into account, as surface wave, substrate modes, boundary effect, and etc. This exceeds the algorithms limitation of the user-friendly 2-D or 2.5-D tools, since the overall 3-D interactions, not only related to consisting parts of antenna but also to its environment, could much influence the antenna performance. Thus the 3-D full-wave EM solution becomes the mainstream design tool for AoC design nowadays. Compared with 2-D or 2.5-D tools, it offers more possibilities to set well-defined boundaries or types of excitation ports. The far-field radiation pattern is also much more sensitive to the change of chip dimension or position of the reflectors. These entirely base on the amount of 3-D meshed cells which offer reliable full-wave solutions of Maxwell's equations [54]. Figure 5.3 shows the modeled CPW patch antenna in 3-D EM tool CST Microwave Studio. Under the wave port excitation with the CPW mode (Figure 5.3: inset), the 3-D far-field radiation pattern with approximate directivity at certain frequency can be well simulated for example.



Type	Farfield
Approximation	enabled (kR >> 1)
Monitor	farfield (f=82.5) [1(3)]
Component	Abs
Output	Directivity
Frequency	82.5
Rad. effic.	0.02562 dB
Tot. effic.	-0.9026 dB
Dir.	8.251 dBi

Figure 5.3: CPW patch antenna far-field simulation under waveguide port excitation with CPW mode (inset) in CST Microwave Studio.

5.2.3 *Simulation results of CPW patch antenna*

Figure 5.4-a shows the simulated reflection coefficient S_{11} spectrum of the selected CPW patch antenna each in decibel (dB) and phase. A sharp resonance of S_{11} is designed at $f_R = 82.5$ GHz with zero phases. To extract exactly the input impedance of the designed CPW patch antenna near $f_R = 82.5$ GHz, the complex impedance courses are plotted on impedance Smith chart in Figure 5.4-b.

Due to the narrow band property of resonance structures as the CPW patch antenna on Si, the input impedance Z_{in} matching to 50 Ω near a certain frequency is quite challenging. After optimization of the antenna geometrical parameters, the input impedance was quite well matched to Z_{in}= (50.45 + j·0.25) Ω at $f_R = 82.42$ GHz according to simulation results shown in Figure 5.4-b.

The far-field radiation pattern with maximum gain has been optimized in perpendicular direction upward to the chip plane as shown in Figure 5.4-b inset. Due to relative thick Si substrate ($d_{sub} = \sim 500$ µm) which induces amounts of surface wave, the direction of far-field radiation pattern has become quite sensitive to the chip size. Meantime the aimed working frequency and input impedance should be well maintained, thus a precise 3-D EM model of the CPW patch antenna is challenging and very important for the transmitter functionality. The maximum directive gain of the CPW patch antenna has achieved $G_{ant} = 7.35$ dBi (calculated with simulated directivity 8.25 dBi and total efficiency -0.9 dB in Fig. 5.3) and been used for oscillator output power calculation of the measured link budget. More details will be introduced in subsection 5.3.3 and 5.3.4.

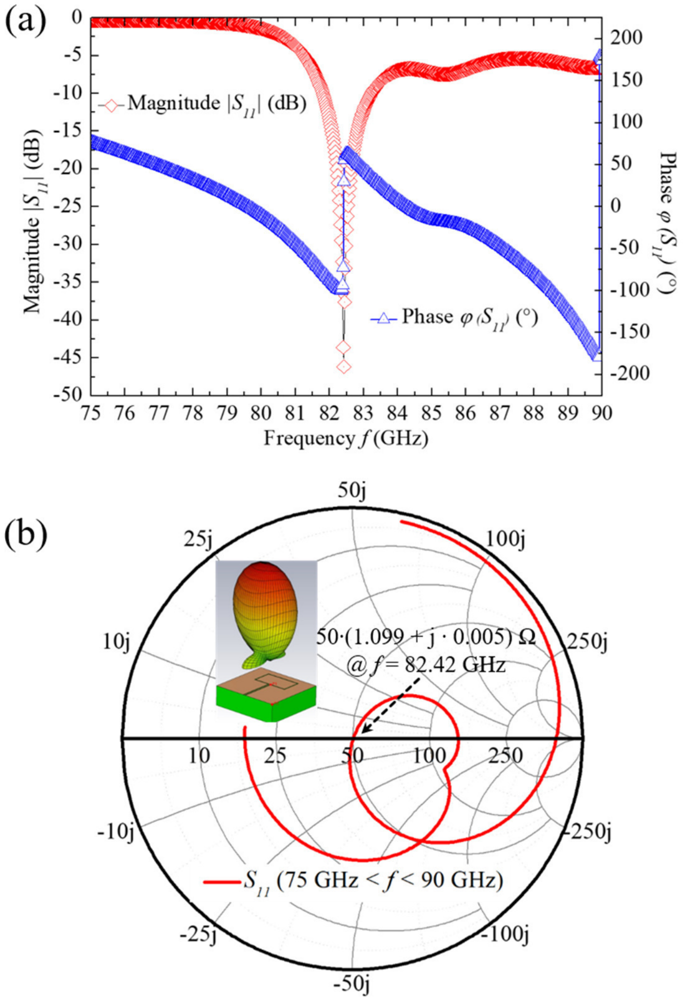


Figure 5.4: Reflection coefficient S_{11} in magnitude and phase (a); complex impedance courses on impedance Smith chart of the designed CPW patch antenna (b).

5.3 CHARACTERIZATION OF IMPATT TRANSMITTER

Finally an IMPATT oscillator (f_o ~ 82 GHz) was monolithically "assembled" with the designed CPW antenna (f_R = 82.5 GHz) together as the design principle illustrated in section 5.1.

Figure 5.5 presents the monolithic IMPATT transmitter chip mounted on a $A = 6 \times 6$ mm^2 metallic plane for test purposes with extra two bonding wires only for DC biasing consideration. The interface between the monolithically integrated CPW patch antenna and the IMPATT oscillator is marked out with blue dotted line. The integrated IMPATT oscillator has an area of A_d = 0.2 mm^2.

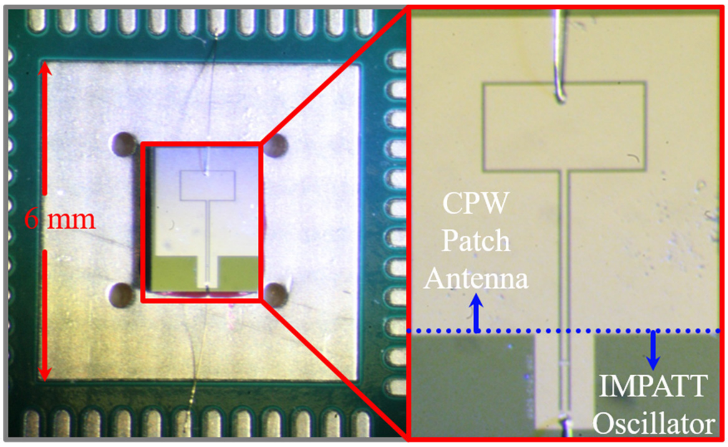


Figure 5.5: The IMPATT transmitter chip of A_{chip} = 4.08 mm^2 mounted on a $A = 6 \times 6$ mm^2 metallic plane for test purposes with bonding wires only for DC biasing (left) and the marked-out interface between embedded IMPATT oscillator and the CPW patch antenna (right).

In this section the characterization of the above mentioned monolithic IMPATT transmitter will be extensively studied and discussed.

5.3.1 *Qualitative verification of transmitter functionality*

To qualitatively verify the functionality of the monolithic IMPATT transmitter, a power meter (e.g. ELVA-1 DPM-10 W-band Power Meter) was employed. A power meter consists of a sensor head and a processing unit with display. Based on a calorimetry method, the sensor head can measure millimeter-wave signal power. Two broadband well calibrated sensing elements (e.g. Schottky Barrier Diodes) which are embedded in two identical W-band waveguides. One is the testing sensor which absorbs any incident millimeter-wave signals and converts it into heat resulting in an increase of temperature. The other is a reference sensor and connected to the control unit. A precisely controlled current leads to a temperature change of the reference sensor. A sensitive temperature comparator connects both sensors and detects the temperature difference between them. Once a millimeter-wave signal is incident on the test waveguide, the temperature rises immediately. At meantime the temperature comparator detects the temperature difference between the two sensors and informs the control unit, which then increases the current for the reference sensor until the temperature in both sensors are equal. By calculating the current applied to the reference sensor, the power the testing sensor (sensor head) has absorbed from the incident signal is eventually calculated.

Therefore, for unknown millimeter-wave incident signals, no quantitative power level is able to be detected. However, to judge whether there is a millimeter-wave power generated by the designed IMPATT transmitter or not, the setup with power meter is quite straightforward and efficient (Figure 5.6).

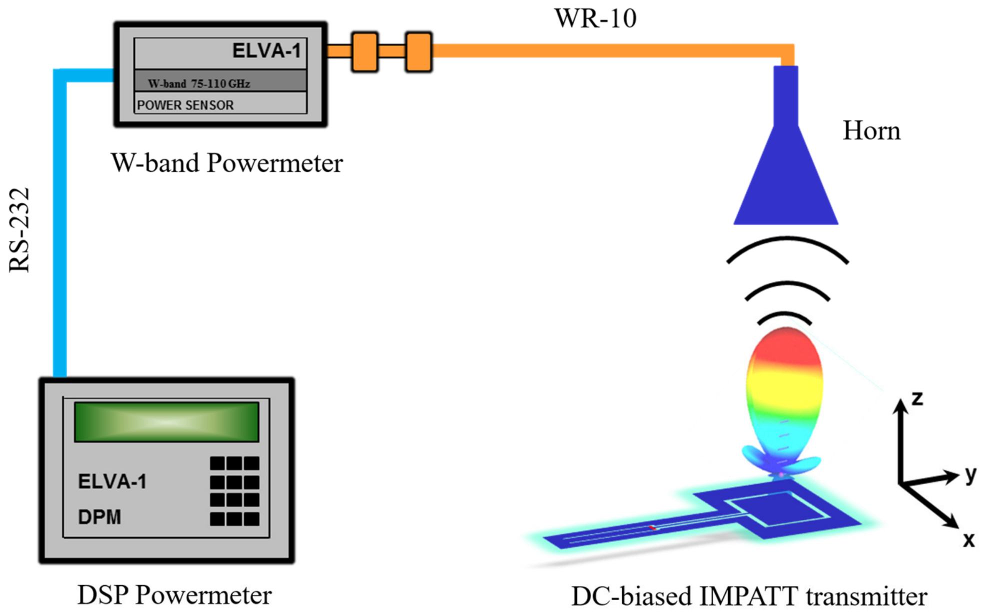


Figure 5.6: The setup with ELVA-1 DPM-10 W-band Power Meter for qualitative verification of transmitter functionality.

5.3.2 *Far-field measurement setup in anechoic chamber*

To quantitatively characterize the monolithic IMPATT transmitter, a measurement setup introduced in subsection 4.2.3 was built up in an anechoic chamber as shown in Figure 5.7. The distance between the IMPATT transmitter chip under test and the receiving standard W-band horn antenna is about a half meter. Only under DC biasing ($I_{bias} = 25$ mA/ $V_{bias} = 13.4$ V) the transmitter chip radiated power towards the receiving horn antenna. The received signals were first led via waveguides through an isolator (Millitech FBI-10) and further down converted by a harmonic mixer (Anritsu M10HW) and detected eventually by a spectrum analyzer (Anritsu MS2830A-044/045).

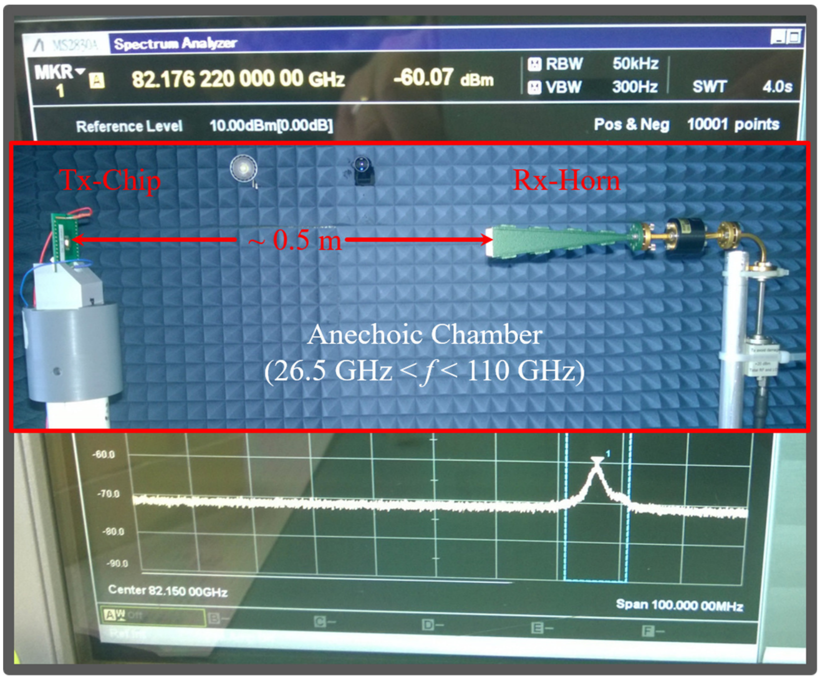


Figure 5.7: The measured radiation power spectrum of the monolithic IMPATT transmitter at the initial position and setup for far-field radiation pattern measurement in anechoic chamber (inset).

The measured spectrum is shown in Figure 5.7 with the center frequency $f_c = 82.15$ GHz, the span frequency $f_{sp} = 100$ MHz, the resolution bandwidth RBW= 50 kHz and the video bandwidth VBW= 300 Hz as setup parameters. A peak at $f = 82.17$ GHz with the detected power of $P_{detec} =$ -60 dBm was locked as expected (designed design frequency $f \sim 82.5$ GHz), which successfully verifies the efficient integration of the CPW patch antenna and the IMPATT oscillator. The noise floor level (NFL) was NFL = -70 dBm.

5.3.3 *Link budget and equivalent isotropically radiated power (EIRP)*

For wireless communication a link budget accounts for the entire power flow from transmitter to receiver or vice versa. It is the most common way to quantify the link performance in a wireless system. Usually the link budget is calculated for estimating the difference between the minimum received signal level and the actual received power, which is named the link margin and regarded as an important parameter in various wireless applications as telecommunication [140], visible light/optical fiber communication [141]-[142], low power wireless medical application [143], satellite/aerospace communication [144]-[145] and etc. In this dissertation the link budget was calculated mainly to estimate the EIRP of the designed monolithic IMPATT transmitter and the output power of the embedded IMPATT oscillator.

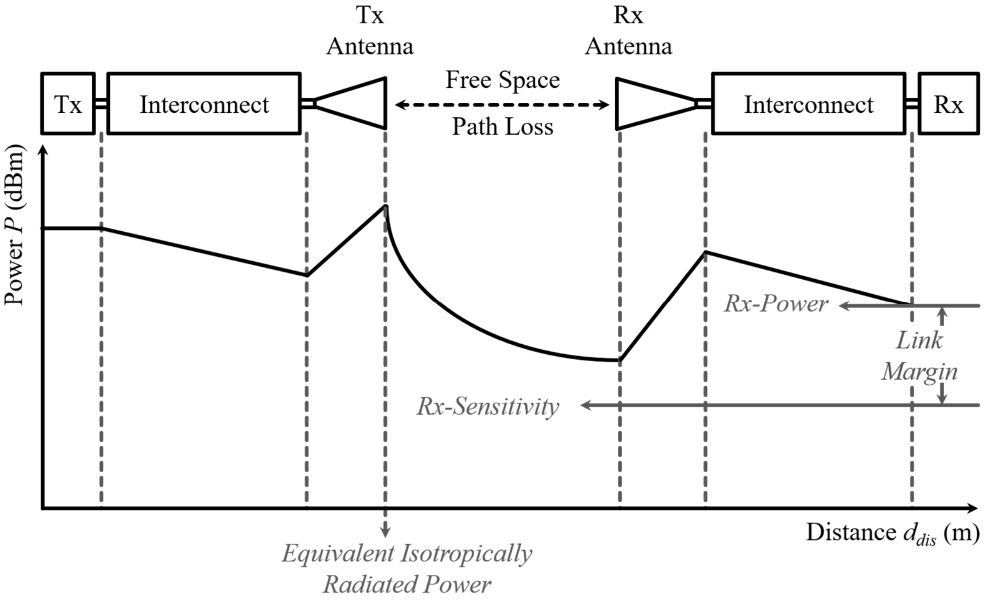


Figure 5.8: The block diagram of the link budget with power flow in a simplified RF wireless transmitting-receiving system.

Figure 5.8 illustrates the link budget block diagram with its corresponding power flow for a simplified RF wireless transmitting-receiving system. Besides all interconnect losses and antenna gain effects between transmitter and receiver, the free space path loss (FSPL) has also to be considered for a complete link budget. FSPL describes the loss between two isotropic radiators in free space without any obstacles nearby to induce reflection or diffraction. Actually it accounts purely for the distance and the wavelength of the EM wave propagating in “free space” (most commonly: air) and is not influenced by any other loss associated with hardware. A practical expression of FSPL is commonly written as:

$$FSPL\ (dB) = 20 \cdot log_{10}(\frac{4 \cdot \pi \cdot f \cdot d_{td}}{c}) \qquad , \qquad (47)$$

with f the signal frequency, d_{td} the transmission distance, and c the speed of light in vacuum. The famous Friis transmission equation [146] includes actually the FSPL definition with both transmitter- and receiver-gain of $G_{ant} = 0$ dBi.

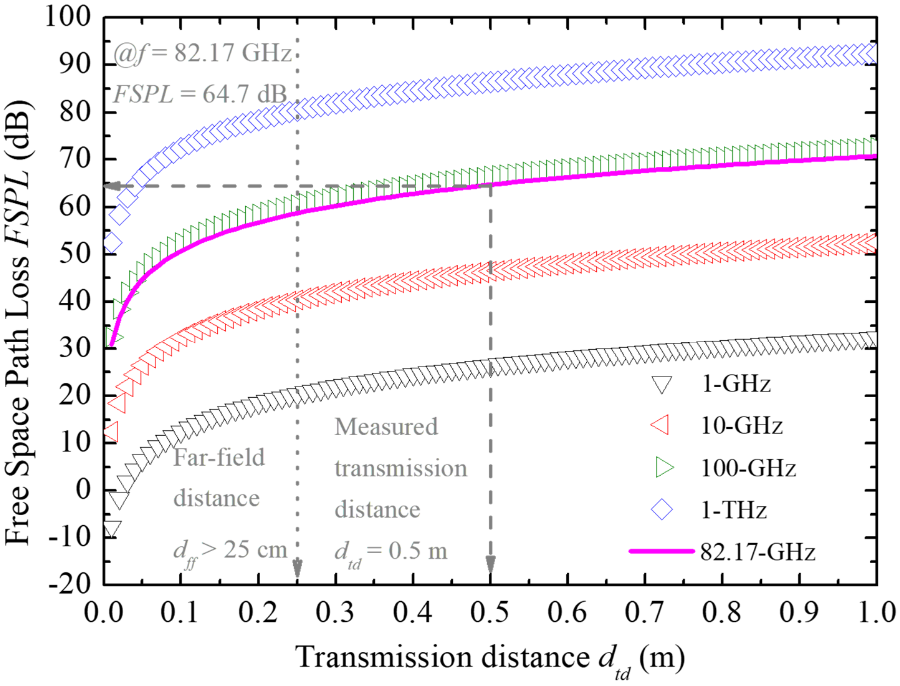
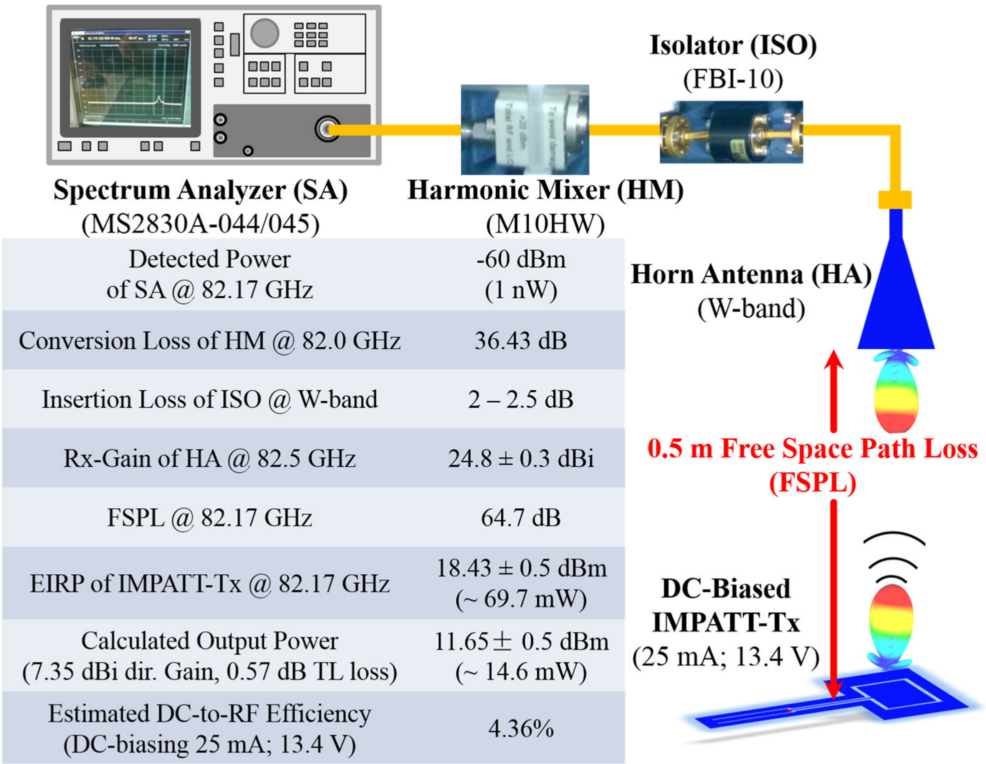


Figure 5.9: FSPL plot for $f = 1$ GHz, 10 GHz, 100 GHz, 1 THz, and 82.17 GHz (characterized IMPATT transmitter frequency in this work) within transmission distance of $d_{td} = 0.5$ m under far -field condition.

FSPL-distance characteristics for frequencies $f = 1$ GHz, 10 GHz, 100 GHz, and 1 THz, and 82.17 GHz are plotted in Figure 5.9. The FSPL formula and Friis transmission equation are only valid under far-field condition [147], that two antennas are separated by a distance

$$d_{td} > \frac{2 \cdot D^2}{\lambda} \qquad , \qquad (48)$$

where λ is the wavelength and D is the largest dimension of either transmitter- and receiver-antennas. Far-field distance $d_{ff} = 25$ cm was calculated for receiving horn, since it has much larger dimension than the CPW patch antenna of the tested monolithic IMPATT transmitter. Transmission distance in anechoic chamber was d_{td} = 0.5 m (two times further than far-field distance d_{ff} = 25 cm), which verified the far-field condition of the link budget calculation. FSPL = 64.7 dB was extracted from Figure 5.9 which enables a complete link budget calculation with hardware information mentioned in subsection 5.3.2.



Detected Power of SA @ 82.17 GHz	-60 dBm (1 nW)
Conversion Loss of HM @ 82.0 GHz	36.43 dB
Insertion Loss of ISO @ W-band	2 – 2.5 dB
Rx-Gain of HA @ 82.5 GHz	24.8 ± 0.3 dBi
FSPL @ 82.17 GHz	64.7 dB
EIRP of IMPATT-Tx @ 82.17 GHz	18.43 ± 0.5 dBm (~ 69.7 mW)
Calculated Output Power (7.35 dBi dir. Gain, 0.57 dB TL loss)	11.65± 0.5 dBm (~ 14.6 mW)
Estimated DC-to-RF Efficiency (DC-biasing 25 mA; 13.4 V)	4.36%

Figure 5.10: Link budget calculation: detailed information of hardware setup & calculated EIRP and DC-to-RF efficiency of the monolithic IMPATT transmitter.

Figure 5.10 shows all necessary information for link budget calculation based on the measurement setup introduced in subsection 5.3.2. The EIRP at f = 82.17 GHz of the IMPATT transmitter under test achieved EIRP = 18.43±0.5 dBm. With maximum directive gain of the CPW patch antenna G_{ant} = 7.35 dBi (calculated based on simulated directivity and total efficiency in subsection 5.2.2) and 0.57 dB transmission line loss, the output power of the embedded IMPATT oscillator achieved at least P_{out} = 11.65±0.5 dBm (14.6 mW) at f = 82.17 GHz, which is quite promising for monolithic E-band designs without employing complex design technique (e.g power combining [148]-[149], injection-locking [150], etc.). A DC-to-RF efficiency of η_{DC-RF} = 4.36% was estimated under DC biasing condition of I_{bias} = 25 mA with V_{bias} = 13.4 V, where the spectrum matching between the IMPATT oscillator and the CPW patch antenna were not taken into account.

5.3.4 *H-plane radiation pattern of IMPATT transmitter*

During the H-plane far-field radiation pattern measurement, the revolving arm which holds the transmitter chip at the initial position ($\theta = 0°$; $\varphi = 0°$) keeps $\varphi = 0°$ and rotates in θ with angle range $0° \leq \theta \leq 360°$. The transmission distance stays $d_{td} = 0.5$ m and fulfills the far-field conditions both for the transmitter and receiver side as mentioned.

Figure 5.11 shows the H-plane radiation pattern of the IMPATT transmitter at $f = 82.17$ GHz under the previously mentioned DC biasing condition. The main lobe stayed within θ range from θ = -30° (330°) to θ = 30°, showed a symmetrical profile as simulated. Side lobes were captured within θ range from θ = (±) 60° to θ = (±) 90°. Since the edge effect and the oscillator chip area were not considered by the 3-D EM antenna simulation, the measured transmitter pattern showed some ripples and had a narrower main lobe compared with the simulated normalized H-plane pattern of the integrated CPW patch antenna.

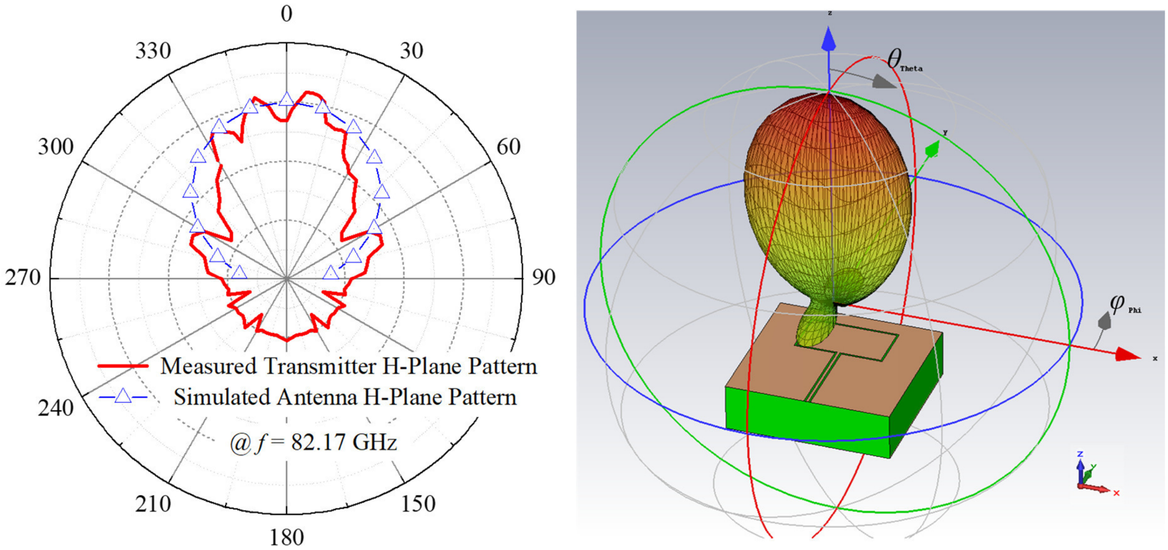


Figure 5.11: The measured H-plane far-field radiation pattern at $f = 82.17$ GHz of only DC-biased IMPATT transmitter chip and the simulated normalized H-plane radiation pattern of the integrated CPW patch antenna.

5.3.5 *Comparison with published (quasi-)monolithic IMPATT transmitter designs*

Table V compares the implemented IMPATT transmitter in this dissertation to the published state-of-the-art monolithic and quasi-monolithic designs.

Table V: Comparison with published (quasi-)monolithic IMPATT transmitter designs.

Freq. (GHz)	Operation Mode	Output Power	DC-to-RF Efficiency	Technology	Antenna	Area (mm^2)	Ref.
76	CW	6.3 nW*	$2\cdot10^{-6}$ %**	CMOS/SiGe	Patch	4	[16]
80	CW	1 mW	---	SIMMWIC	Patch	6	[15]
71	CW	<0.1 mW	---	SIMMWIC	Slot	49	[151]
109	Pulse	7 mW	---	SIMMWIC	Slot	1.9	[152]
43	Pulse	27 mW	7.2%	GaAs	Dipole Array	0.9	[11]
32	CW	300 mW	4.4%	Duroid+Diamond Heat Sink	Patch	6.4	[153]
82	**CW**	**14.6 mW**	**4.4%**	**SIMMWIC**	**Patch**	**4**	***This Work [20]***

* from published measured transmitted power -62 dBm (0.63 nW) and losses of the measurement setup 10 dB;

** from *calculated transmitter output power -52 dBm (6.3 nW) and 25 dBm (330 mW) DC power.

It can be seen that at comparable frequencies (71 GHz $\leq f \leq$ 82 GHz) under CW operation mode [15]-[16], [151] maximum output power P_{out} = 1 mW can be achieved. Thanks to the well-designed oscillator and the efficient antenna integration, this work [20] achieved highest output power P_{out} = 14.6 mW to the date. Especially compared to the design implemented with a standard SiGe CMOS technology [16], the advantage of SIMMWIC for high power and high efficiency IMPATT transmitter implementation is obvious. Compared to f_{op} = 82 GHz in this work, the design [152] achieves P_{out} = 7 mW under pulse operation mode with f_{op} = 109 GHz, which motivates the pulse mode characterization of the IMPATT transmitter in this dissertation for future work. The design [11] is the only one with the "fast" GaAs technology. Under pulse mode it achieves P_{out} = 27 mW but at lower operation frequency f_{op} = 43 GHz. The design [153] is a quasi-monolithic actually, which employed typical Duroid RF substrate and diamond heat sink to achieve P_{out} = 300 mW at f_{op} = 32 GHz without burning out the IMPATT diode. As for the listed DC-to-RF efficiency, this work does not yet take the spectrum matching condition between IMPATT oscillator and the CPW patch antenna, which would result in a higher efficiency value.

Chapter 6. SCHOTTKY DIODE

6.1 MOTT OPERATION AND LAYER GROWTH OF MOTT DIODE

Usual Schottky diodes exhibit an increasing junction capacitance with forward voltage which is the chosen operation regime for rectification. Schottky diodes with low doped epitaxial layers (known as MOTT diodes) are preferred for rectification purposes because the junction capacitance stays constant up to a threshold voltage which is equal to the built-in voltage of the junction in ideal MOTT diodes but smaller in real MOTT diodes with finite background doping. Compared to an ordinary Schottky diode, MOTT diode can achieve or maintain a higher cut-off frequency until built-in voltage in forward biasing direction.

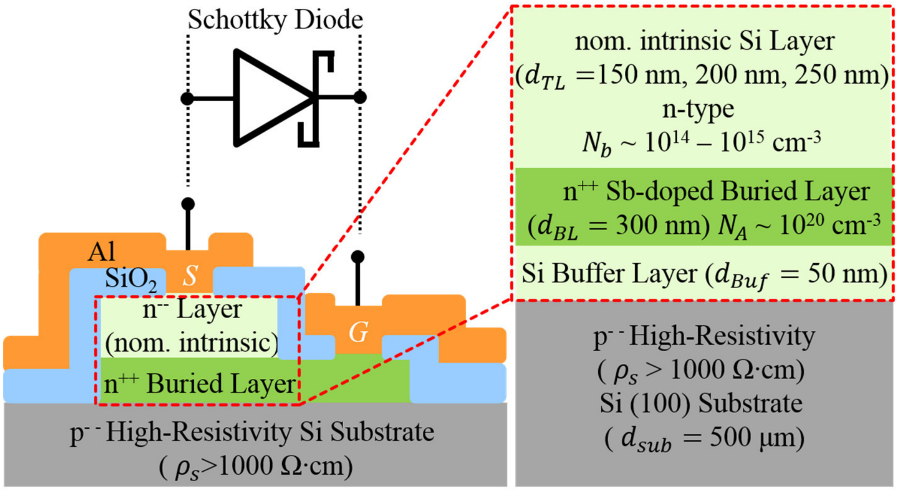


Figure 6.1: Layer stacks prepared for Schottky diode under MOTT mode operation.

For MBE samples prepared for this dissertation, the Schottky layers are grown. Figure 6.1 shows the detailed layer stacks presented together with the device integration concept (section 2.2). For the in-house fabrication technology the nominal intrinsic Si layer achieved n-type background doping level of $N_b \sim 10^{14}$ –10^{15} cm^{-3}, which is sufficiently low for MOTT operation mode. The

Schottky contact is built up at the interface between this nominal intrinsic layer and the Al layer of the signal line.

In Table VI all MBE and process runs are listed with key information related to the nominal intrinsic layer. The top layer thickness varies from $d_{TL} = 140$ nm to $d_{TL} = 230$ nm with quite low n-type background doping of $N_b \sim 0.1 - 1.0 \cdot 10^{15}$ cm^{-3}. Maximum grown epitaxial layer thickness is $d_{TL} = 230$ nm as punch-through layer in this dissertation.

Table VI: An overview of experimental information linked to the nominal intrinsic layer for for all grown and processed Schottky samples.

MBE A-N.O.	Process V-N.O.	act. Thickness (nm)	MOTT-Function	Doping Strategy	nom. Doping (cm^{-3})	act. Doping (10^{15} cm^{-3})
3541-1	823-1-1	230	yes	---	Intrinsic	0.1 – 1.0
3542-1	823-1-2	190	yes	---	Intrinsic	0.1 – 1.0
3543-1	823-1-3	140	yes	---	Intrinsic	0.1 – 1.0
3541-4	926-1-1	230	yes	---	Intrinsic	0.1 – 1.0
3542-2	926-1-2	190	yes	---	Intrinsic	0.1 – 1.0
3543-3	926-1-3	140	yes	---	Intrinsic	0.1 – 1.0
3542-4	94-1-1	190	yes	---	Intrinsic	0.1 – 1.0
3543-4	94-1-2	140	yes	---	Intrinsic	0.1 – 1.0
3542-3	155-1-1	190	yes	---	Intrinsic	0.1 – 1.0

6.2 DC CHARACTERIZATION OF MOTT DIODE

6.2.1 *Extraction of series resistance R_s and ideality factor η of MOTT diode*

With the same procedure as introduced in subsection 3.2.2 for IMPATT diodes, series resistance and ideality factor can be extracted from the fundamental I-V characteristics of the investigated Schottky diodes. Figure 6.2 presents the I-V characteristics of two 6x1 μm² Schottky diodes, which were chosen each for a half-wave (sample V823-1-1) and a full-wave rectenna (sample V94-1-1) designs in section 7.2.

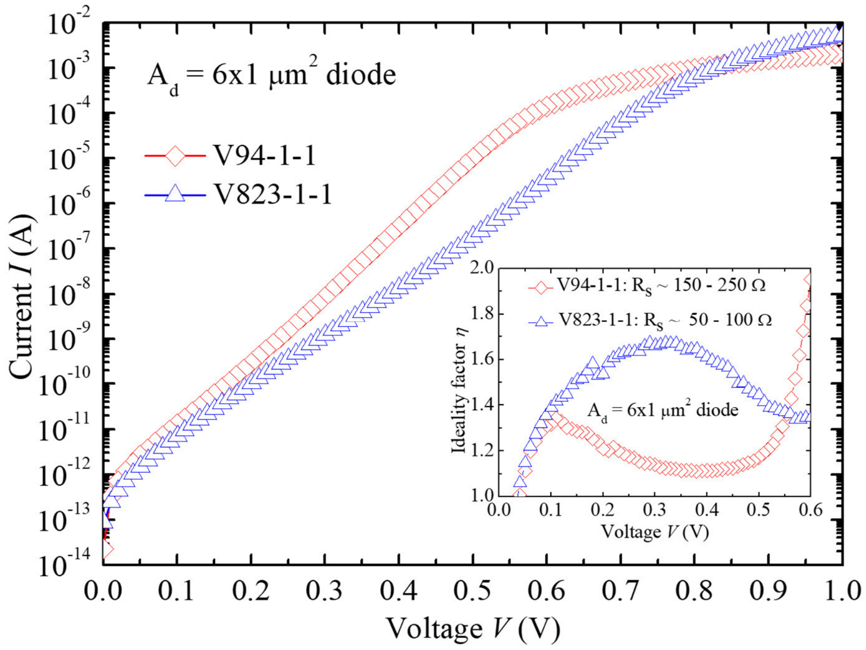


Figure 6.2: Forward I-V characteristics with corresponding series resistance R_s and ideality factor η extraction for $A_d = 6\times1$ μm² diodes each on sample V94-1-1 and V823-1-1.

The extracted series resistances and ideality factors are presented in Figure 5.2 (inset), too. In practice the series resistance is strongly dependent on many factors of the in-house fabrication technology, e.g. quality of the MBE layer stacks, quality of the Schottky contact, precision of the etching depth of n^{++} buried layer, stability of the oxidation process and metallization, etc. A key indicator of a good Schottky contact is the ideality factor. Since Schottky is a “majority” device, the recombination possibility of carriers (electrons and holes) should theoretically be zero. In reality due to limited crystal quality (impurities and contaminations), the extracted ideality factor of Si Schottky reaches maximally $\eta = 1.2 - 1.3$ in the low current region (diffusion current mixed with recombination current) and drops down to $\eta = 1.1$ in the medium current region (less affected by recombination current in depletion layer but dominated more by favored ballistic current). Therefore sample V94-1-1 has a better Schottky behavior, even though the series resistance extracted from high current region from I-V characteristics is much larger compared with sample V823-1-1. In subsection 6.3.1 and 6.3.2, the influence of series resistances (extracted from I-V and RF characterization) on rectification is discussed extensively.

6.2.2 *Results of transmission-line model (TLM) measurement of MOTT diode*

To verify the actual doping concentration of n^{++} buried layer for good ohmic contact, TLM measurements as introduced in section 2.4 were performed for the n^{++} buried layer TLM structures on Schottky sample V94-1-1 and V823-1-1.

The specific resistivity over doping concentration characteristics are shown in Figure 6.3 each for sample V94-1-1 and V823-1-1. Compared to the literature, $5\cdot10^{19}$ cm^{-3} $\leq N_{car} \leq 6\cdot10^{19}$ cm^{-3} electrically activated carrier concentration was achieved, which ensures a reasonable ohmic buried contact layer from MBE growth aspect.

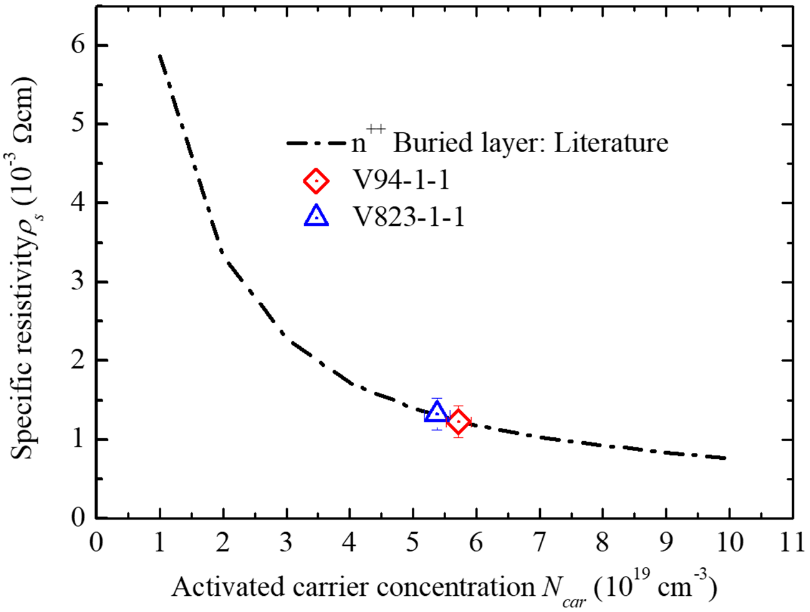


Figure 6.3: Specific resistivity ρ_s vs. carrier concentration N_{car} extracted from TLM structures for n^{++} Sb-doped buried layer on sample V94-1-1 and V823-1-1.

6.3 S-PARAMETER CHARACTERIZATION AND SMALL-SIGNAL LUMPED-ELEMENT MODELING OF MOTT DIODE

6.3.1 *Estimation of cut-off frequency f_{co}*

The cut-off frequency f_{co} is usually estimated as the figure of merit for Schottky diode's RF performance by using the following formula:

$$f_{co} = \frac{1}{2 \cdot \pi \cdot R_s \cdot C_j} \quad , \tag{49}$$

where R_s is the series resistance and C_j is the junction capacitance of a diode at zero biasing point. Commonly R_s value is directly extracted from diode I-V characteristics and C_j value from commercial C-V measurement (normally $f < 1$ GHz). However, this DC and low-frequency data based estimation excludes an important fact in real millimeter-wave scenarios, namely the biasing effect on resistance and capacitance values. Thus, the estimated cut-off frequency predicted by capacitance at zero biasing point is lower than it is in reality. For the MOTT operation mode, even more details should be taken into consideration.

In Figure 6.4, state-A, -B, and -C are marked on I-V characteristics of a $A_d = 6\times1$ μm^2 MOTT diode for three different working points by rectification. If we take state-B as the critical point of MOTT operation, then state-A still fulfils MOTT operation, which means C_j stays nearly constant until built-in voltage where state-B is. After state-B MOTT operation will be damaged due to dramatically increased C_j and R_s only with small increasing applied voltage. Until state-C, no capacitive behavior for RF signals can be measured, the reactance is dominated not anymore in capacitive form but inductively. This reveals the fact that the R_s value extracted from I-V characteristics never even has a chance to meet C_j under the same applied voltage. Therefore a biasing condition dependent modeling for investigated Schottky diodes under MOTT operation was performed based on small-signal S-parameter measurements.

By applying the S-parameter-based device-level C-V measurement as proposed in subsection 3.3.2, R_s and C_j in real millimeter-wave scenario were extracted according to a small-signal lumped-element model (Figure 6.4: inset) for MOTT operation mode. This model consists of the inner diode with parallel conductance G_p, junction capacitance C_j and the series resistance R_s (exactly the same model of a reverse-biased p-n junction diode). Table VII summarizes the cut-off frequency f_{co} estimation of investigated $A_d = 6\times1$ µm² diodes under MOTT operation both for I-V and RF-modeling extracted series resistances. Junction capacitance was extracted from S-parameter-based device-level C-V measurements. The cut-off frequencies of the chosen diodes with $A_d = 6\times1$ µm² have been estimated each from DC and RF data. In both cases, the cut-off frequencies are larger than aimed design frequency 60 GHz $\leq f \leq$ 90 GHz.

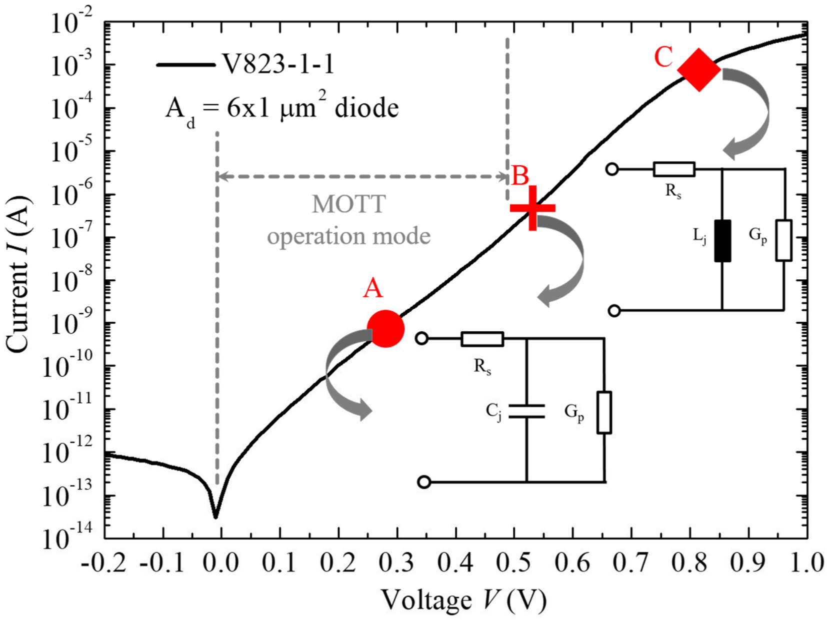


Figure 6.4: Small-signal lumped-element models for Schottky diodes under MOTT operation at different working points (State-A, -B, and -C).

Table VII: Cut-off frequency estimation of $A_d = 6\times1$ µm² Schottky diodes under MOTT operation mode for sample V94-1-1 and sample V823-1-1.

$A_d = 6\times1$ µm² Diode Process V-N.O.	R_s (Ω)		C_j (fF)	f_{co} (GHz)	
	DC	RF		DC	RF
94-1-1	150 – 250	30 – 50	~ 5	127 – 212	636 – 1061
823-1-1	50 – 100	20 – 40	~ 5	318 – 636	795 – 1591

6.3.2 *Analysis on optimum rectifying efficiency*

Actually the frequency dependence of the rectifying property is much more complicated than only described by a single cut-off frequency as commonly assumed [154]. Figure 6.5 illustrates the scenario of RF wave with corresponding AC voltage $u(t)$ and current $i(t)$ incident to a small-signal Schottky diode model.

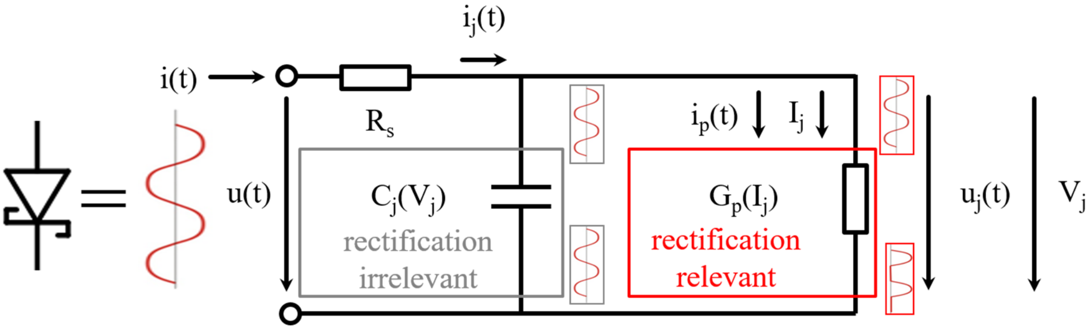


Figure 6.5: Small-signal lumped-element model for Schottky diode under incident RF wave.

The high frequency losses stem from the voltage drop across the series resistance R_s and the non-rectifying current path along the junction capacitance C_j. The incident RF wave from the antenna has a power P proportional to the product of $u(t) \cdot i(t)$. The power P_p in the rectification-relevant branch (represented in Figure 6.5 by the DC biasing current dependent G_p) is smaller and given proportional to the product $u_j(t) \cdot i_p(t)$.

According to Kirchhoff's current and voltage law

$$\frac{u_j(t)}{u(t)} = \frac{1}{(G_p + j \cdot \omega \cdot C_j) \cdot (R_s + \frac{1}{G_p + j \cdot \omega \cdot C_j})} \quad , \qquad (50)$$

and

$$\frac{i_p(t)}{i(t)} = \frac{G_p}{G_p + j \cdot \omega \cdot C_j} \quad , \qquad (51)$$

following equation can be derived:

$$|\frac{P_p}{P}|^2 = \frac{|u_j(t) \cdot i_p(t)|^2}{|u(t) \cdot i(t)|^2} = [1 + (\frac{\omega}{\omega_p})^2]^{-1} \cdot [(1 + \frac{\omega_p}{\omega_s})^2 + (\frac{\omega}{\omega_s})^2]^{-1} \quad , \qquad (52)$$

where the following abbreviations are used for the parallel cut-off angle frequency

$$\omega_p = \frac{G_p}{C_j} \quad , \qquad (53)$$

and for the serial cut-off angle frequency

$$\omega_s = \frac{1}{R_s \cdot C_j} \qquad . \qquad (54)$$

Equation (52) shows that only a part of the incident power is directed towards the rectification branch of the Schottky diode. In order to investigate the optimum rectifying behavior a fixed operation frequency $f_0 = \frac{\omega_0}{2 \cdot \pi}$ for an ideal Schottky diode under MOTT operation (C_j constant up to the built-in voltage) is assumed. Under this assumption, there are a constant serial cut-off angle frequency ω_s and a forward current dependent parallel cut-off angle frequency

$$\omega_p = \frac{I_{bias}}{V_T \cdot C_j} \qquad , \qquad (55)$$

where I_{bias} is the DC biasing current, V_T is the thermal voltage ($V_T = \frac{K_B \cdot T}{q}$ with K_B the Boltzmann constant, T the temperature, and q the elementary charge).

ω_p occurs in equation (52) in the nominator and denominator terms giving an optimum rectifying efficiency at

$$\frac{\omega_{p,max}}{\omega_0} = (1 + \frac{\omega_s^2}{\omega_0^2})^{1/4} \qquad . \qquad (56)$$

The optimum rectifying efficiency at $\omega_{p,max}$ value, which is adjustable by the DC biasing current level, accounts then for

$$|\frac{P_p}{P}|_{max} = [1 + (1 + \frac{\omega_s^2}{\omega_0^2})^{-1/2}]^{-1/2} \cdot [1 + \frac{\omega_0^2}{\omega_s^2} + \frac{\omega_0}{\omega_s} \cdot (1 + \frac{\omega_s^2}{\omega_0^2})^{1/4}]^{-1/2} \qquad . \qquad (57)$$

Equation (57) reveals the importance of the parallel cut-off frequency on the optimum rectifying efficiency in real application scenarios.

Chapter 7. SCHOTTKY RECEIVER

Receivers are commonly referred to wireless communication systems for RF signal receiving, amplifying, mixing / down-converting to the intermediate frequency (IF) or base band, which enable a reasonable demodulation of transmitted messages (voice or image information) from carrier signals and noises. Concepts such as superheterodyne receiver [155]-[156], direct-conversion receiver [157]-[158], and direct RF sampling receiver [159]-[161] are for example often applied in many wireless communication systems.

All above mentioned three receiver types for communication purposes require mixers driven by a local oscillator (LO) (for superheterodyne and direct-conversion types) or RF analog-to-digital converter (ADC) with low noise and good linearity (for RF sampling type), which exceed by far the maximally achievable complexity of monolithic implementation with the in-house clean-room technology.

Therefore, based on the well-studied rectification effect of the Schottky diode under fast MOTT operation mode (chapter 5), rectenna with minimum design complexity was chosen as a receiver demonstrator for RF signal detection applications [26], [66], [154], [162]-[167].

7.1 PRINCIPLE FOR DESIGN OF RECTENNA

Basically there are two principles for rectennas designs, half-wave and full-wave, respectively. In this section, two design principles are both introduced with their pros and cons.

7.1.1 *Concept of half-wave rectenna*

The block diagram of a typical half-wave rectenna design is illustrated in Figure 7.1. It consists of an antenna, a matching network, a rectifier (e.g. Schottky diode), a low-pass filter and a DC output. As signals of various frequencies are incident at the antenna, only signals with certain frequencies can be received by the antenna due to its bandpass property. The matching network ensures the impedance between the antenna and the rectifier (Schottky diode), so that the received signals can be guided to the rectifier with minimum loss. Part of signals can pass through the rectifier and conduct themselves into the RF ground. The rest is smoothed by the low-pass filter which offers a detectable voltage potential at the DC output.

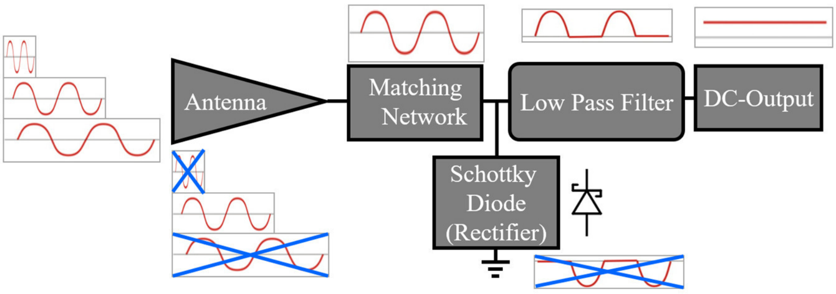


Figure 7.1: Block diagram of a half-wave rectenna design.

The half-wave principle is popular in many applications (e.g. signal detection [167], thermal energy sensor [168], energy harvesting [169], and wireless power transmission [70], [170]-[172]) due to non-complexity. Additionally the robustness against technology instability and cost-effective fabrication due to single-diode property make it attractive in practice, especially for monolithic designs. However, since only part of received RF signals contributes to the final DC output, this design principle is theoretically not appropriate for high RF-to-DC conversion applications. In practice, a half-wave rectenna can also achieve reasonable rectifying efficiency due to proper design and implementation [173].

7.1.2 *Concept of full-wave bridge rectenna*

In a full-wave rectifier circuit two diodes are normally necessary for each half of the AC wave cycle. A multiple winding transformer [174]-[176] with a secondary winding, which is split into two half parts with a common center-tapped connection, enables theoretically a 100 % rectifying efficiency. The two diodes are in conducting states in turn according to even or odd half cycles of the incident AC waves. As every coin has two sides, the introduction of multiple winding transformers improves the rectifying efficiency but makes the two-diode full-wave rectifier design costly and complex. For a monolithic millimeter-wave design using the in-house SIMMWIC technology, this is a huge drawback from feasibility aspect.

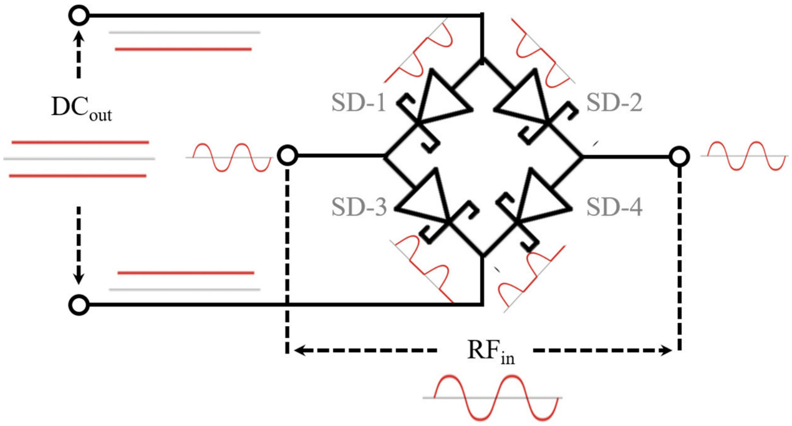


Figure 7.2: Block diagram of a full-wave bridge rectifier design.

Therefore, a full-wave bridge rectifier circuit [177]-[179] was adopted to improve both the rectifying efficiency and the feasibility with the fabrication technology. In a full-wave bridge rectifier, four individual rectifying diodes (e.g. Schottky diodes in Figure 7.2) are connected in a closed loop like a “bridge”. The main advantage of this concept compared with two-diode full-wave design is that a special center tapped transformer is not needed. The four diodes are so arranged with DC output and RF input, that only two diodes are conducting during each half cycle of the AC waves. During the positive half cycles, diodes (marked as SD-3 and SD-4 in Figure 7.2) conduct RF signals while reversely set diodes (marked as SD-1 and SD-2 in Figure 7.2) are blocking. During the negative half cycles, reversely set SD-1 and SD-2 conduct RF signals while SD-3 and SD-4 show blocking behavior. This mechanism enables a constructive superposition both for positive and negative half cycles of RF input signals, whose DC parts are eventually represented or detected on the DC output.

7.2 TWO TOPOLOGIES OF IMPLEMENTED RECTENNAS

According to above introduced half-wave and full-wave bridge design principles for rectification, two rectennas have been implemented by using $A_d = 6\times1$ µm^2 MOTT-operational Schottky diodes, which are well-characterized from device aspect in chapter 5.

7.2.1 *Microstrip topology of integrated serial-fed patch antenna array with operating frequency f_{op} = 85 GHz*

The half-wave rectenna is designed in microstrip topology. The functionality scheme of the rectenna with f_{op} = 85 GHz and its related layout are shown in Figure 7.3. A serial fed four-patch antenna array with f_R = 85 GHz is adopted to increase the effective area and the gain of the antenna. The $\frac{\lambda}{4}$ transformer offers a smooth impedance transition between the antenna array and the further parts. Two Schottky diodes are embedded between the microstrip line and the radial stub, which electrically shorts the RF signals via a large capacitor formed together with the back side metallized ground plane.

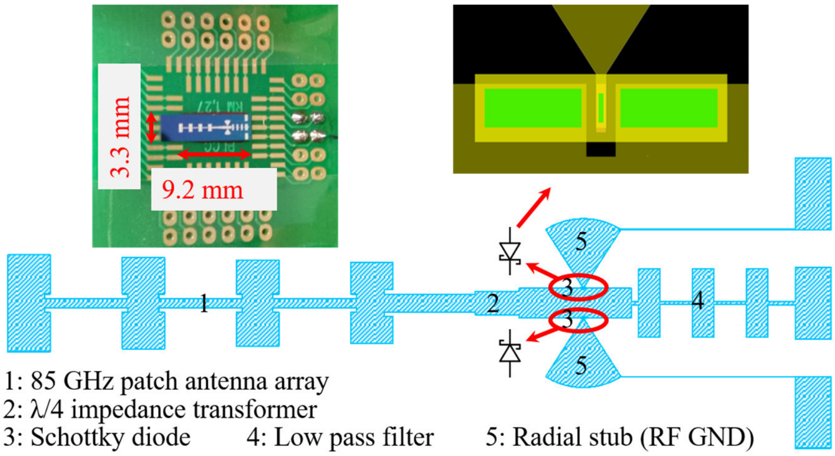


Figure 7.3: Functionality scheme of the designed half-wave rectenna (f_{op} = 85 GHz) with its layout for Schottky diode integration; rectenna chip mounted on board for test purposes (inset).

This topology is meant to keep the wave transition smooth and the rectifying position as symmetrical as possible. The remaining RF signals (not conducted via the Schottky diodes to RF ground) are further smoothed by a low-pass filter, which consists of three-stage LC elements. The dimension of the designed rectenna is A_{chip} = 3.3×9.2 mm^2, which is relatively large due to patch antenna array and three-stage LC low-pass filter.

7.2.2 *Microstrip topology of integrated bow-tie dipole antenna with operating frequency f_{op} = 80 GHz*

To improve the bandwidth of the receiving antenna, a bow-tie antenna designed for f_R = 80 GHz was applied for the full-wave bridge design. Compared with the serial-fed patch antenna array (A_{ant} = ~ 5.6 mm^2), the bow-tie antenna is much smaller (A_{ant} = ~ 0.07 mm^2) and reduces the entire rectenna design to only A_{chip} = 4 mm^2. Even though the gain and the effective area of the receiving antenna are reduced at the meantime the improved rectifying efficiency due to full-wave bridge design was the hope to compensate these concerned cons.

Figure 7.4 shows the microscope images of the fabricated full-wave bridge rectenna chip with f_{op} = 80 GHz. The bridge circuit consists of four embedded A_d = 6×1 µm^2 Schottky diodes, whose RF ports are connected with the integrated bow-tie antenna at f_R = 80 GHz.

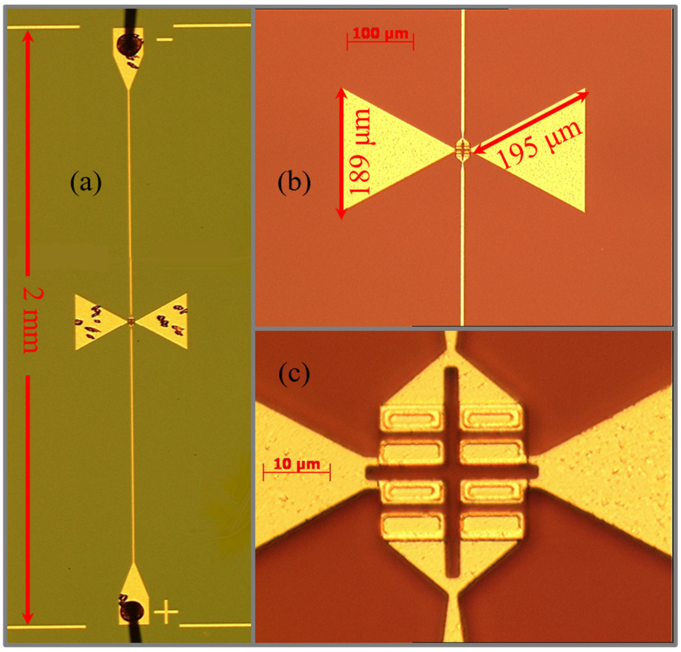


Figure 7.4: Microscope images of the fabricated full-wave bridge rectenna at f_{op} = 80 GHz with DC bonding wires (a); dimensions of the integrated bow-tie antenna (b) and the embedded bridge circuits with four A_d = 6×1 µm^2 Schottky diodes (c).

7.3 CHARACTERIZATION OF RECTENNAS

In this section, the measurement setup and the characterization results of the implemented half-wave and full-wave bridge rectennas are introduced and analyzed.

7.3.1 *Measurement setup and settings for rectenna characterization*

Figure 7.5 (a) takes the half-wave design with $f_{op} = 85$ GHz as an example to explain the basic measurement principle of the rectenna characterization.

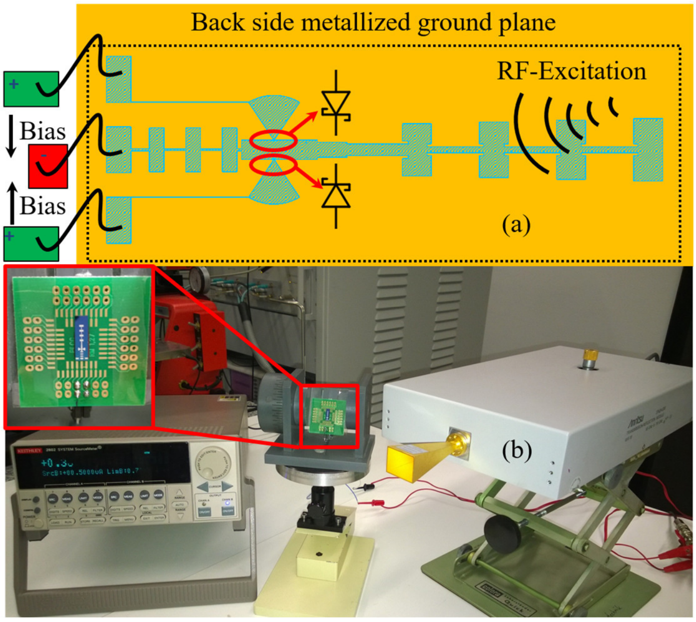


Figure 7.5: The principle of the rectenna characterization (a); the measurement setup in RF laboratory (b).

The rectenna is firstly biased with a certain DC biasing current I_{bias} and a reference DC voltage V_{DC} is measured. Then the RF excitation source is activated and aimed to the patch antenna array with optimal transmission position. With the same biasing current I_{bias} the DC output voltage under RF excitation V_{RF} is measured. The difference between V_{DC} and V_{RF} is the conversion voltage ΔV_{conv}, which is the key parameter for the final characterization of the rectenna. Figure 7.5 (b) shows the measurement setup in RF laboratory. A VNA port (Anritsu ME7808 System) with a W-band standard gain horn antenna was employed as the source of RF excitation. To drive the Schottky diodes at certain operating point and to extract the conversion voltage, a source meter (Keithley 2602 System Source Meter) was used.

7.3.2 *Conversion voltage ΔV_{conv} spectra of characterized rectennas*

A frequency sweep in a range of 75 GHz $\leq f \leq$ 90 GHz was carried out under biasing current from I_{bias} = 0.1 µA to I_{bias} = 0.44 mA for the half-wave rectenna with f_{op} = 85 GHz and from I_{bias} = 0.1 nA to I_{bias} = 0.6 mA for the full-wave rectenna with f_{op} = 80 GHz. The maximum conversion voltage spectra $\Delta V_{conv}(f)$ of the full-wave rectenna with f_{op} = 80 GHz (under biasing current I_{bias} = 10 nA) and the half-wave rectenna with f_{op} = 85 GHz (under biasing current I_{bias} =1 µA) are shown in Fig 7.6, so are the minimum conversion voltage spectra $\Delta V_{conv}(f)$ of both designs under corresponding biasing currents each of I_{bias} = 0.6 mA and I_{bias} = 0.44 mA.

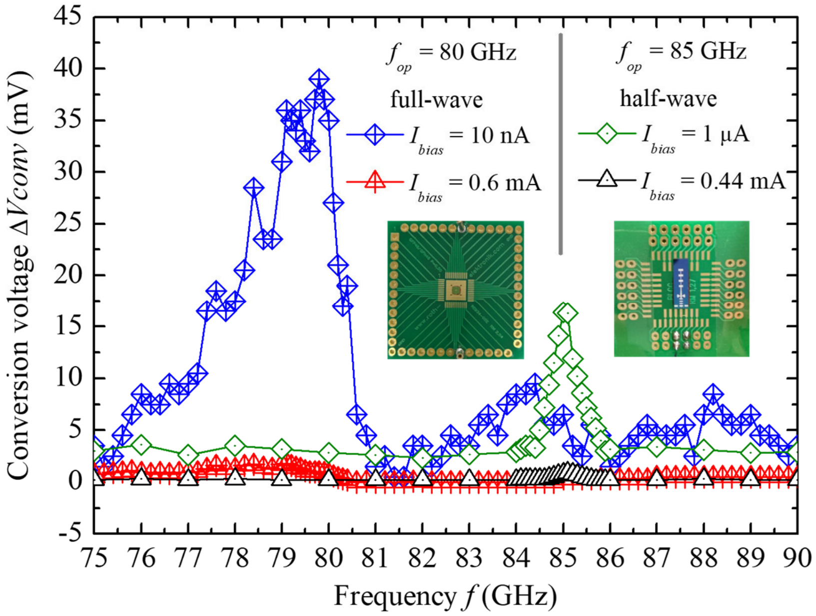


Figure 7.6: Characterized maximum and minimum conversion voltage spectra $\Delta V_{conv}(f)$ of the half-wave rectenna with f_{op} = 85 GHz and the full-wave rectennas with f_{op} = 80 GHz under corresponding biasing currents.

Clear conversion voltage peaks were detected at designed antenna frequencies (f_{op} = 85 GHz for half-wave and f_{op} = 80 GHz for full-wave) of both implemented designs. In spite of reduced gain and effective area of the integrated antenna, the full-wave bridge design achieved maximum conversion voltage of $\Delta V_{conv} = 40$ mV at $f = 80$ GHz while the half-wave design was reaching only maximum conversion voltage of $\Delta V_{conv} = 17$ mV at $f = 85$ GHz. Compared with the half-wave design, the full-wave bridge design shows overall superior performance mainly due to its higher rectifying efficiency and proper antenna design.

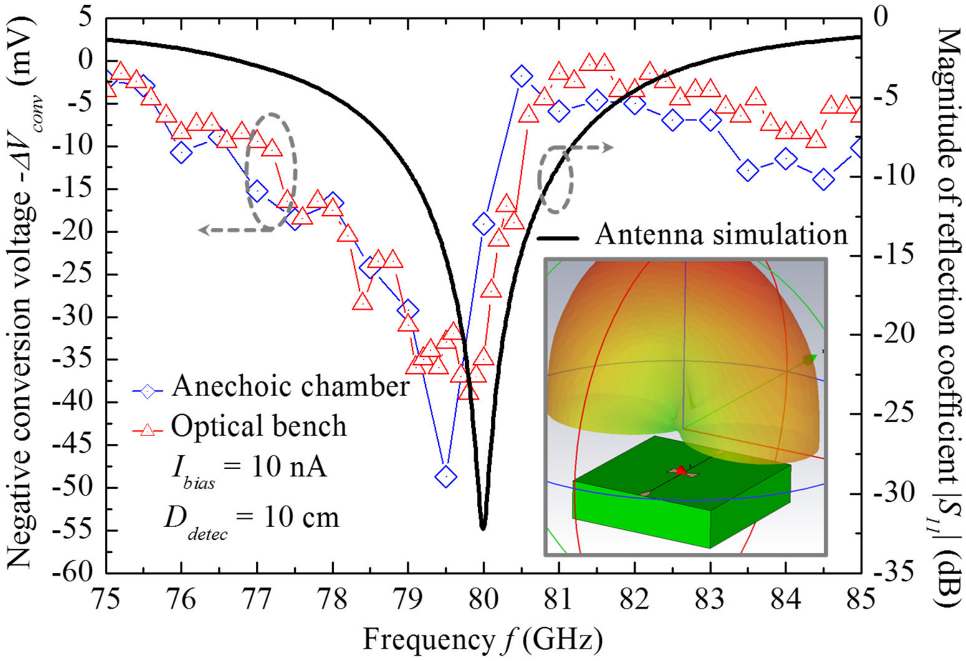


Figure 7.7: Conversion voltage (negative value) spectra $-\Delta V_{conv}(f)$ of the full-wave rectenna under biasing current of $I_{bias} = 10$ nA at detecting distance of $D_{detec} = 10$ cm each measured in anechoic chamber and on optical bench; the simulated reflection coefficient spectrum $S_{11}(f)$ of the integrated bow-tie antenna and its 3-D EM model (inset).

From a bandwidth aspect, an obvious improvement by the bow-tie antenna full-wave design is also observed in Figure 7.5 compared with the patch antenna array half-wave design. The full-width-at-half-maximum (FWHM) achieves FWHM >3 GHz by the full-wave rectenna while the half-wave rectenna is reaching only FWHM < 1 GHz. To compare the conversion voltage spectrum of the full-wave rectenna to the simulated bow-tie antenna S_{11} spectrum, the conversion voltage is intentionally set to its negative value in Figure 7.7. In an anechoic chamber with less environment interferences (at Institute of Radio-Frequency Technology/IHF, University of Stuttgart) an even higher peak conversion voltage $\Delta V_{conv} = \sim 50$ mV was detected compared with the measurement performed on an optical bench under the same biasing current $I_{bias} = 10$ nA and at the same detecting distance $D_{detec} = 10$ cm. With a frequency shift of about $\Delta f = 0.5$ GHz, both measured conversion voltage spectra are consistent quite well with the simulated reflection coefficient results of the integrated bow-tie antenna. For the simulation result of the serial-fed patch antenna array, previous works [180]-[181] of Institute of Semiconductor Engineering/IHT, University of Stuttgart are referred to.

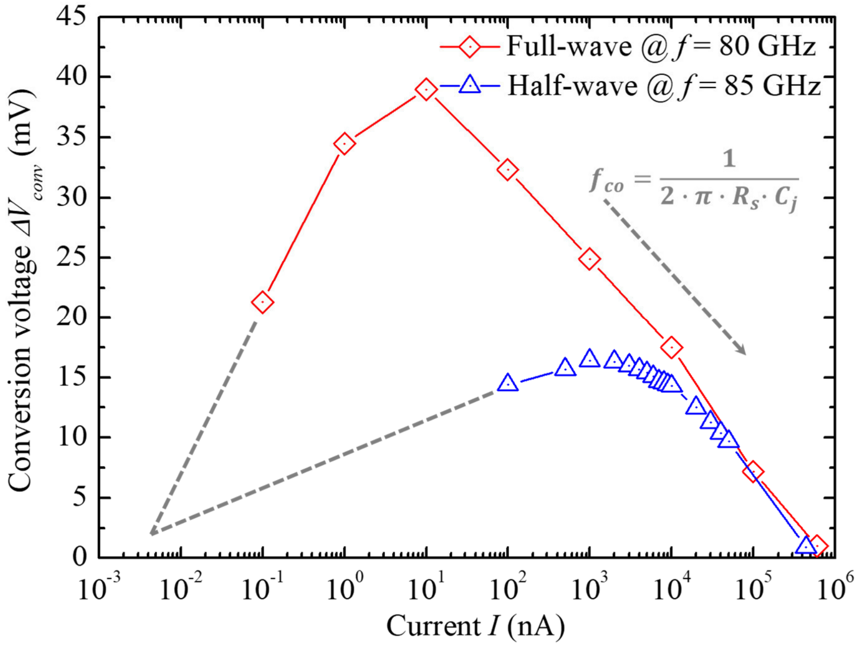


Figure 7.8: Conversion voltage ΔV_{conv} versus biasing current I_{bias} characteristics for the f = 80 GHz full-wave (0.1 nA ≤ I_{bias} ≤ 0.6 mA) design and the f = 85 GHz half-wave (0.1 µA ≤ I_{bias} ≤ 0.44 mA) design.

The conversion voltage ΔV_{conv} at f = 85 GHz for the half-wave design and at f = 80 GHz for the full-wave design was plotted in Figure 7.8 under biasing currents varied each from I_{bias} = 0.1 µA to I_{bias} = 0.44 mA (half-wave) and from I_{bias} = 0.1 nA to I_{bias} = 0.6 mA (full-wave).

With increasing forward biasing currents, the first-rising-then-falling characteristics are observed for both rectennas at their functional frequencies (f = 80 GHz for the full-wave bridge design and f = 85 GHz for the half-wave design). This is due to the trade-off between the rectifying efficiency and the biasing dependent cut-off frequency. With increasing biasing current, the Schottky diode is driven from linear region to exponential region (the slope of the I-V characteristics increases dramatically), which causes a stronger rectifying effect and leads to an increasing conversion voltage. However the junction capacitance C_j increases drastically if the diode operating point exceeds the MOTT operation region with further increasing biasing current. Therefore, the cut-off frequency f_{co} of embedded Schottky diodes is degraded correspondingly, so that only very small conversion voltage is visible (with biasing current of $I_{bias} = 0.6$ mA for the full-wave design at $f_{op} = 80$ GHz and $I_{bias} = 0.44$ mA for the half-wave design at $f_{op} = 85$ GHz). The minimum biasing currents $I_{bias} = 0.1$ nA (full-wave) and $I_{bias} = 0.1$ µA (half-wave) were determined by the lowest readable level of the DC source meter during the measurement. The extrapolated curves are expected to be measured with ultra-low-noise source meter.

With above explained overall effect of biasing-dependent rectification, the conversion voltage of the designed full-wave bridge rectenna can be dynamically tuned from 1 mV $\leq \Delta V_{conv} \leq$ 40 mV at $f = 80$ GHz and from 1 mV $\leq \Delta V_{conv} \leq$ 17 mV at $f = 85$ GHz for half-wave rectenna, respectively.

7.3.3 *Detecting range D_{detec} study on full-wave bridge rectenna*

All comparisons of half-wave and full-wave results until now are based on the fact that the detecting distances were quite different. For the half-wave rectenna with $f_{op} = 85$ GHz, the measurement was performed with detecting distance of $D_{detec} = 5$ mm, but with detecting distance of $D_{detec} = 10$ cm for the full-wave bridge rectenna with $f_{op} = 80$ GHz. No more detectable conversion voltage was observed for the half-wave rectenna if the detecting distance $D_{detec} > 1$ cm. Therefore, a study was carried out for the full-wave bridge rectenna to test its limit of the detecting range.

Under biasing current of $I_{bias} = 10$ nA, the full-wave bridge rectenna chip was excited by signals at $f = 80$ GHz continuously. The distance between the W-band horn antenna and the rectenna chip plane varied from $D_{detec} = 5$ cm to $D_{detec} = 40$ cm on an optical bench with quantified scale (Figure 7.9: inset). Figure 7.9 shows the measured characteristics of conversion voltage ΔV_{conv} over detecting distance D_{detec}. An exponential-like drop is observed with the increasing detecting distance. $D_{detec} = 25$ cm is the beginning of the far-field region of the adopted standard W-band horn antenna, still conversion voltage of $\Delta V_{conv} = \sim 5$ mV could be well detected. $D_{detec} = 40$ cm is the maximum limit of the detecting distance. $\Delta V_{conv} = 57$ mV could be maximally achieved under the near-field excitation with the detecting distance of $D_{detec} = 5$ cm, which is an absolutely superior performance compared to the half-wave rectenna design only within $D_{detec} = 5$ mm.

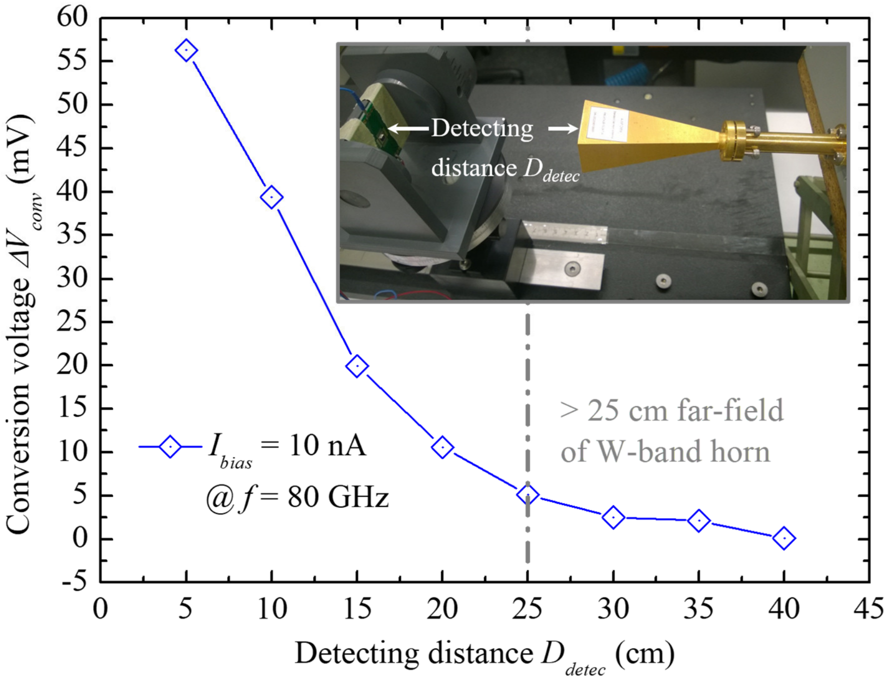


Figure 7.9: Detecting range study on full-wave bridge rectenna with variation of detecting distance from 5 cm ≤ D_{detec} ≤ 40 cm and measurement setup on an optical bench with quantified scales (inset).

7.3.4 *Excitation power P_{exc} study on full-wave bridge rectenna*

With the help of ELVA-1 W-band power meter, a power calibration was carried out at the WR-10 interface between the W-band horn antenna and the VNA port for frequencies at f = 75 GHz, 80-GHz, 85 GHz, and 90 GHz.

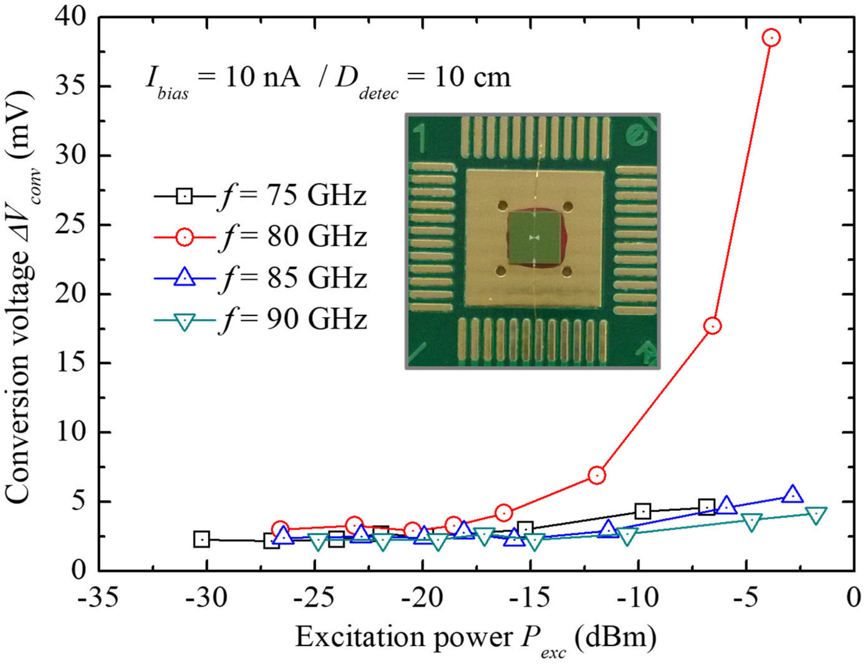


Figure 7.10: Excitation power study for the full-wave bridge rectenna (inset) at f = 75 GHz, 80 GHz, 85 GHz, and 90 GHz with biasing current of I_{bias} = 10 nA and measuring distance of D_{detec} = 10 cm.

In Figure 7.10 the characteristics of conversion voltage versus excitation power are shown for the full-wave bridge rectenna (inset). With the calibrated excitation power level of-30 dBm ≤ P_{exc} ≤ -2 dBm for above mentioned frequencies, the designed operating frequency at f_{op} = 80 GHz shows an obviously increased conversion voltage ΔV_{conv} above power level P_{exc} ≥ -15 dBm and no saturation trend until the maximum power level of P_{exc} = -5 dBm offered by VNA. At other frequencies f = 75 GHz, 85 GHz, and 90 GHz only maximum conversion voltages ΔV_{conv} ~ 5 mV are observed, which are quite consistent with the band property of the integrated bow-tie antenna as simulated.

Chapter 8. CONCLUSION AND FUTURE WORK

8.1 CONCLUSION

In this dissertation an E-band (an attractive band for millimeter-wave applications) transmitting-receiving module with integrated antennas (bottleneck for mainstream CMOS/BiCMOS technology) is successfully implemented by using only IMPATT and Schottky diodes (two-terminal devices instead of the dominating three-terminal transistors) with SIMMWIC technology (academia clean room level, not-competitive to commercial CMOS/BiCMOS technologies) under the large frame of various modern wireless applications (refer to chapter 1). The performance of the implemented module is proved as very promising due to the measurement results.

The IMPATT transmitter realization has systematically followed an entire trace from material growth (section 3.1); device design-fabrication-characterization (section 3.2; 3.3; 3.4); oscillator design-fabrication-characterization (chapter 3); antenna design (section 5.2) and finally to transmitter design-fabrication-characterization (section 5.1; 5.3). The enforcement of this complete implementation chain ensures not only the basic functionality but also the most competitive performance of the implemented final transmitter design (Table V of subsection 5.3.5). The interfaces between material and device, device and sub-circuit, sub-circuit and final circuit have been clearly defined and proven as necessary, e.g. the analysis of avalanche and drift region for IMPATT mode operation (subsection 3.1.1) has linked successfully the layer growth to the desired device performance (subsection 3.1.2); the precise measurement-based device modeling and key parameters analysis (section 3.4) have contributed much to understanding the important device properties related to sub-circuit design (section 4.1). Besides theoretical analysis and simulation, the design feasibility has been also well verified by real measurement data such as the thermal endurance of IMPATT devices (section 3.5) and the oscillation condition of IMPATT oscillators (section 4.1). Some exciting "intermediate" results have been observed additionally, such as the theoretical unification of Barkhausen's criteria and Kurokawa condition for oscillating circuit with a two-terminal active device during the measurement-based verification of the oscillation condition (subsection 4.1.2) and the injection locking effect during amplification spectrum characterization of IMPATT oscillator (subsection 4.2.4). The successful transmitter characterization (section 5.3) has proven that both the on-chip antenna design (section 5.2) and its integration to the oscillator (chapter 4) have achieved or even exceeded the expected design specifications.

The Schottky receiver has followed exactly the same implementation chain as the IMPATT transmitter. The key elements of the chosen circuit topology (rectenna) are a rectifying device (Schottky diode) and an on-chip antenna. A special operation mode (MOTT) of Schottky diode has been investigated both from functional principle and layer growth aspects (section 6.1). Despite the tolerance of technological fabrication process, the dimension of embedded rectifying element for rectenna design has been chosen low-profile enough ($A_d = 6\times1\ \mu\text{m}^2$), so that the cut-off frequencies estimated both from DC and RF data are larger than the aimed design frequency (section 6.2; 6.3). This ensures the functionality of the rectifying element in a real rectenna circuit under verified DC biasing condition for MOTT operation. In addition, a theoretical analysis considered in real application scenario is performed to reveal the key point for high rectifying efficiency design (subsection 6.3.2). In practice, two rectennas have been implemented (section 7.2), one with integrated serial-fed patch antenna array (half-wave) and the other with bow-tie dipole antenna (full-wave) based on half-wave (subsection 7.1.1) and full-wave (subsection 7.1.2) principles. Both rectennas have been characterized as functional. Conversion voltages occur at expected frequency bands which are consistent with the radiating frequencies of integrated antennas; trade-off between biasing dependent rectifying efficiency and cut-off frequency explains well the characteristics of maximum conversion voltage over biasing current (subsection 7.3.2). The full-wave rectenna design shows in general much more superior performance than the half-wave design in detected signal strength (subsection 7.3.2), detected bandwidth (subsection 7.3.2), and detection range (subsection 7.3.3) with lower geometrical profile (subsection 7.2.1; 7.2.2). A study about conversion voltage over excitation power for the implemented full-wave rectenna has confirmed the functionality of the designed Schottky receiver once again without observing any power saturation under excitation of available power levels (subsection 7.3.4).

Finally a design-by-characterizing strategy has been well established and reflected through the performance emphasized circuit design in this dissertation.

8.2 FUTURE WORK

Standing on the work already done in this dissertation, there are mainly nine points which could further improve design and characterization of investigated modules or at least interestingly valuable for future research from the author's point of view.

8.2.1 *Double-drift IMPATT diode with higher efficiency*

For minimizing the MBE growth effort, only single-drift (SD) IMPATT structure is investigated in this dissertation. To further increase the efficiency of high frequency power generation, double-drift (DD) IMPATT structure is worthy to try, which meanwhile requires more precise layer growth control in thickness and doping concentration.

8.2.2 *Power spectra measurement for E-band IMPATT oscillators in CW mode and in pulse mode*

With the main focus on oscillator and on-chip antenna integration, only amplification spectra were referred to as qualitative indication for the IMPATT transmitter design in this dissertation. It is very worthy to characterize the fabricated E-band IMPATT oscillators with the appropriate measurement setup introduced in subsection 4.2.3. Then, the quantitative output power spectra for implemented E-band IMPATT oscillators could be characterized both in CW mode and in pulse mode, respectively.

8.2.3 *Output power P_{out} measurement for the IMPATT transmitter at operating frequency f_{op} = 82.5 GHz in pulse mode*

Under CW mode the implemented IMPATT transmitter with f_{op} = 82.5 GHz has already shown the record output power to date in monolithic designs (Table V of subsection 5.3.5). It becomes very interesting to know how much output power could be detected under pulse mode, which is normally at least 3 times larger than under CW mode. Additionally pulse mode operation causes much less thermal problem, which is very attractive for monolithic high power and high efficiency applications.

8.2.4 *Design of a CPW patch antenna array with high gain at operating frequency f_{op} = 70 GHz*

Considering the limited layout area and antenna design tolerance, the large integrated on-chip antenna was designed at f_{op} = 82.5 GHz (section 5.2), which means only oscillators working around f = 82.5 GHz were chosen for the monolithic IMPATT transmitter design in this dissertation. However as amplification spectra of all implemented IMPATT oscillators shown in subsection 4.2.2, the highest gain is characterized for the oscillators at f = 70 GHz only with much narrower bandwidth. Thus, a redesign of a CPW patch antenna array at f_R = 70 GHz with high gain should further boost the final transmitter performance.

8.2.5 *Implementation of an IMPATT transmitter at operating frequency f_{op} = 70 GHz with higher output power P_{out}*

By integrating the well-designed CPW patch antenna array at f_R = 70 GHz with high gain and high efficiency to the IMPATT oscillator at f_{op} = 70 GHz with high output power, a IMPATT transmitter at f_{op} = 70 GHz with superior performance should be feasible. The most challenging step is the frequency matching between the two components (oscillator and antenna array) with narrow bandwidth. Meanwhile a reliable impedance matching is very necessary.

8.2.6 *Large-signal excitation for the full-wave bridge rectenna at operating frequency f_{op} = 80 GHz*

Since no power saturation was observed (subsection 7.3.4) by excitation power study for full-wave rectenna using available hardware test setup (VNA port only up to P_{exc} = -5 dBm). A large-signal excitation with higher power-level is worthy to perform, so that the power saturation level of implemented rectenna can be verified.

8.2.7 *Energy-harvesting experiment for the full-wave bridge rectenna at operating frequency f_{op} = 80 GHz*

For the excitation power level which could shift the DC working point of the embedded Schottky diode, the extra DC biasing becomes not necessary and the rectenna is working then under large signal mode. Thus, an energy-harvesting experiment for the full-wave rectenna design is worthy to try as well.

8.2.8 *Test prototype for IMPATT transmitter and Schottky receiver module*

A transmission test prototype can be built up, firstly under CW driven mode of the IMPATT transmitter. As long as the transmitter's working frequency matches the receiver's, the conversion voltage could be observed by receiver side. The transmission path between the IMPATT transmitter and the Schottky receiver is then verified. For further steps, pulse width modulated DC biasing signals can be applied to drive the IMPATT transmitter in different pulse modes, for instance with varied duty cycles, and send these modulated RF signals to the Schottky receiver. With this test prototype a primary communication scenario can be well demonstrated.

8.2.9 *Full integration of IMPATT transmitter and Schottky receiver module on single chip*

Once the active layer profile of IMPATT diode is changed from p^{++}-n^{-}-n^{++} to n^{++}-n^{-}-p^{++} as illustrated in Figure 8.1, a co-integration of IMPATT transmitter and Schottky receiver could be finally realized. Besides the monolithic integration of transceiver, a universal recipe both for IMPATT and Schottky diode can be applied by growing active layers using MBE technology, which could save a lot effort in time and cost, respectively.

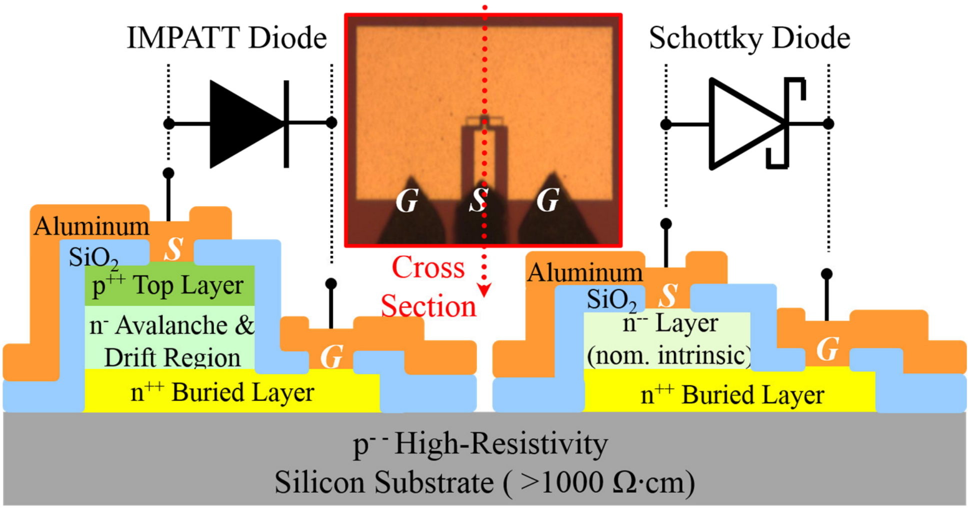


Figure 8.1: Full integration of IMPATT transmitter and Schottky receiver on one chip.

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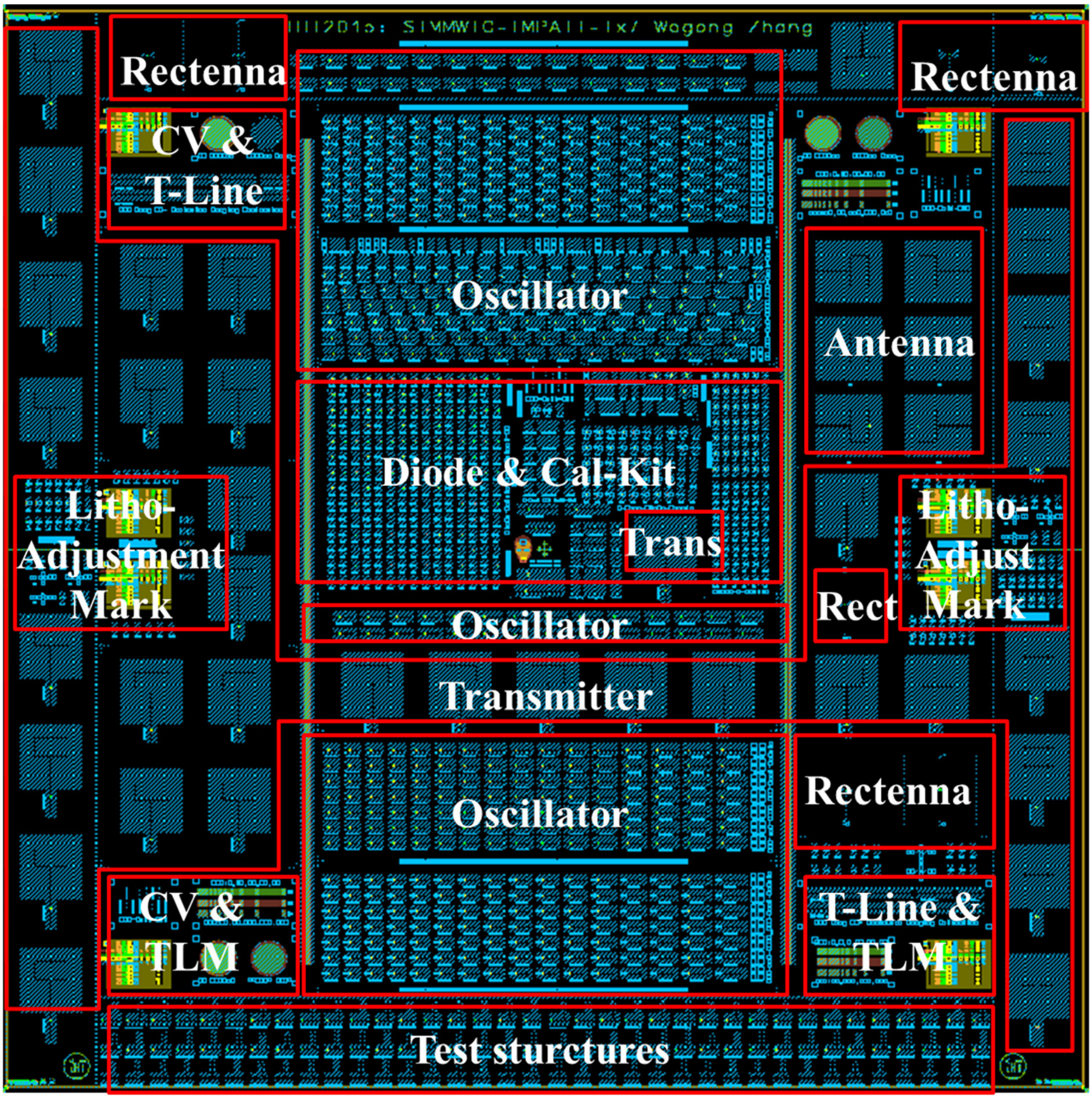
APPENDIX A

Layout Mask Set for SIMMWIC mm-Radar Project



APPENDIX B

MATLAB Control Code for Power-Meter ELVA-1 via RS232 Interface

```
                % This program write data to RS232 interface %

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
           %Please change the parameters before using the program%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function write_to_RS232_elva

% % Create a serial port object.
obj1 = instrfind('Type', 'serial', 'Port', 'COM4', 'Tag', '');

% fopen(obj1);
% Create the serial port object if it does not exist
% otherwise use the object that was found.
if isempty(obj1)
      obj1 =
serial('COM4','Baudrate',1200,'Parity','none','Databits',8,'StopBits',1);

else
      fclose(obj1);
      obj1 = obj1(1);

end
      fopen(obj1);
% Communicating with instrument object, obj4.
      fprintf(obj1,'disp:enab on');

for i=75:1:110
      fprintf(obj1, ['sens:freq ' num2str(i)]);
      pause(0.5);
      data7 = query(obj1, 'syst2:sens:info?');

end

      fclose(obj1);
% Clean up all objects.
      delete(obj1);

end

function write_to_RS232_elva

out = instrfind('Type', 'serial', 'Port', 'COM3', 'Tag', '');
```

```
if isempty(out)
      out = serial('COM3','Baudrate',1200,'DataBits',8,'StopBits',1);
else
      fclose(out);
      out = out(1);
end

      fopen(out);
      fid = fopen('powerfreq.txt', 'wt');
      fprintf(out,'disp:enab on');

for i=79.9:0.1:81
      fprintf(out, ['sens:freq ' num2str(i)]);
      pause(0.5);
      fprintf(out, 'read?');
      pause(0.5);
      data = fscanf(out);
if(i>=80)
      fprintf(fid, '%3.3f\t%s',i,data);
end
      pause(0.5);
      display([num2str(i) 'GHz=' data]);
end
      fclose(fid);

      fid = fopen('powerfreq.txt', 'r');
      c = textscan(fid, '%f\t%f %s');
      fclose(fid);

      plot(c{1},c{2},'-r')
      xlabel('Freq. [GHz]')
      ylabel('Power [uW]')
      hold on

      fclose(out);
      delete (out);

end
```

APPENDIX C

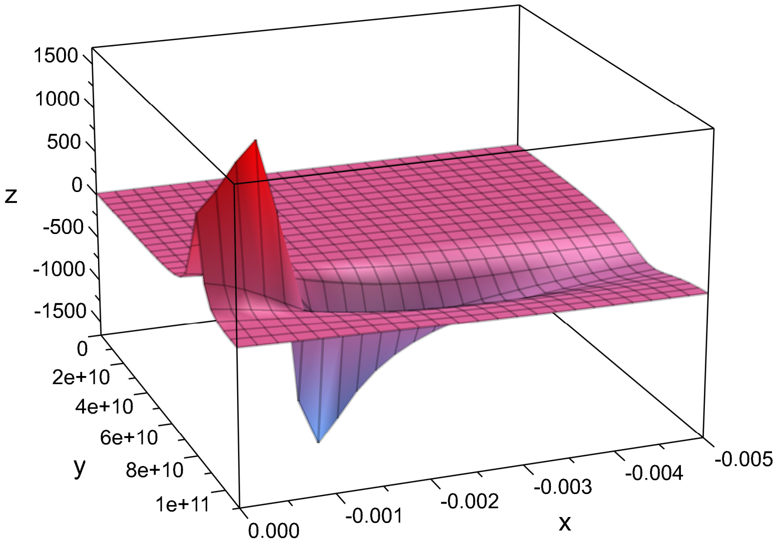
MATLAB Codes for One-Port De-embedding Core

```
%=========================================================================%
                  % One-Port De-embedding Calculation Core%
%=========================================================================%
      S = Sdaten{k};


        %De-embedding Procedure:
            S2P(:,1)=S(:,1).*1e9;
            SSP(:,1)=S(:,1).*1e9;
            SOP(:,1)=S(:,1).*1e9;

            S2P(:,2)=S(:,2)+S(:,3).*j;  %S11_meas   (Re+j*Im)
            S2P(:,3)=S(:,4)+S(:,5).*j;  %S12_meas   (Re+j*Im)
            S2P(:,4)=S(:,6)+S(:,7).*j;  %S21_meas   (Re+j*Im)
            S2P(:,5)=S(:,8)+S(:,9).*j;  %S22_meas   (Re+j*Im)
            SSP(:,2)=SS(:,8)+SS(:,9).*j;    %S11_short_meas (Re+j*Im)
            SOP(:,2)=SO(:,8)+SO(:,9).*j;    %S11_open_meas  (Re+j*Im)

 %            ZMP(:,1)=(S2P(:,2)+1)./(1-S2P(:,2)).*50;
 %            ZSP(:,1)=(SSP(:,2)+1)./(1-SSP(:,2)).*50;
 %            ZOP(:,1)=(SOP(:,2)+1)./(1-SOP(:,2)).*50;

 %            YMP(:,1)=1./ZMP(:,1);
 %            YSP(:,1)=1./ZSP(:,1);
 %            YOP(:,1)=1./ZOP(:,1);

        % %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Open-Short
        %
        % ZOS(:,1)=1./(YMP(:,1)-YOP(:,1))-1./(YSP(:,1)-YOP(:,1));
        % YOS(:,1)=1./ZOS(:,1);
        % SOS(:,2)=(ZOS(:,1)-50)./(ZOS(:,1)+50);
        %
        % %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Short-Open
        %
        % YSO(:,1)=1./(ZMP(:,1)-ZSP(:,1))-1./(ZOP(:,1)-ZSP(:,1));
        % ZSO(:,1)=1./YSO(:,1);
        % SSO(:,2)=(ZSO(:,1)-50)./(ZSO(:,1)+50);
        %
        % %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Xu’s Method
            A(:,1)=S(:,1).*1e9;
            B(:,1)=S(:,1).*1e9;
            SSOL(:,1)=S(:,1).*1e9;
            SSOL(:,4) = S(:,1);
```

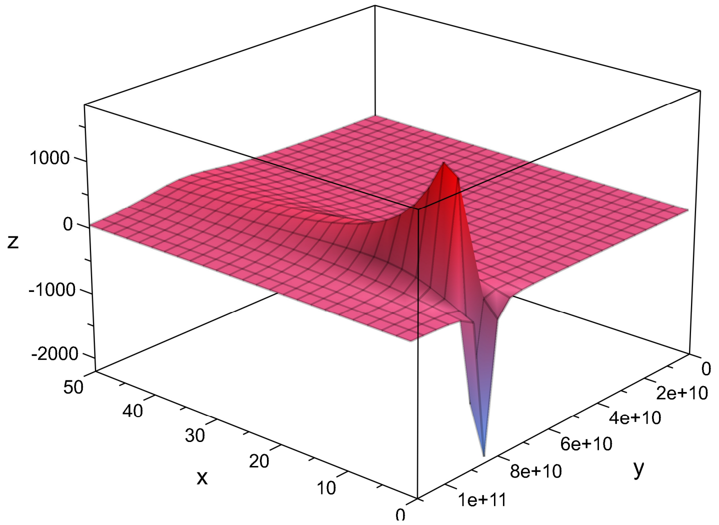
```
            A(:,2)=(SSP(:,2)+SOP(:,2))./(2-SSP(:,2)+SOP(:,2));  %
A=(S11_short_meas+S11_open_meas)/(2-S11_short_meas+S11_open_meas)
            B(:,2)=(SOP(:,2)-A(:,2)).*(1-A(:,2));                %
B=(S11_open_meas-A)*(1-A)

            SSOL(:,2)=(S2P(:,5)-A(:,2))./(A(:,2).*S2P(:,5)+B(:,2)-
A(:,2).*A(:,2)); % De-embedded file


     % De-embedding output in .s1p format
     DateiName = sprintf('%s_Deeb.s1p',char(strtok(dateiname, 's')));
     fid = fopen(DateiName,'w');   %fprintf(fid,'Freq. Real(Z)');
        fprintf(fid,'\n');
        fprintf(fid,'\n');
        fprintf(fid,'# Hz S RI R 50');        % R(eal) I(mag)
        fprintf(fid,'\n');
        fprintf(fid,'! data format:');
        fprintf(fid,'\n');
        fprintf(fid,'! Freq, GHz       Re (S11)      Im (S11)');
        fprintf(fid,'\n');

        freq(:,1) = S(:,1)*1e9;
        vektor=[freq(:,1) real(SSOL(:,2)) imag(SSOL(:,2)) ];
        for c=1:size(vektor,1)
            fprintf(fid,'%6.5e  ', vektor(c,:));
            fprintf(fid,'\n');
        end

end



 'De-embedding analysis finished!'
```

APPENDIX D

MATLAB Codes for Drawing 3-D Graphics in Subsection 3.4.3



```
a := plot::Function3d((6.6+((9+9^2*(x)+4*PI^2*(190*1e-12)^2*x*y^2)/((1+9*(x)-
(190*1e-12)*4*PI^2*(20*1e-15)*y^2)^2+(39.48*y^2*(9*20*1e-15+190*1e-
12*(x))^2)))), x=-0.5e-2..-1/100000000000000, y=0..110000000000);
```



```
b := plot::Function3d((6.6+((x+x^2*(1/-2500)+4*PI^2*(190*1e-12)^2*1/-
2500*y^2)/((1+x*(1/-2500)-(190*1e-12)*4*PI^2*(20*1e-
15)*y^2)^2+(39.48*y^2*(x*20*1e-15+190*1e-12*(1/-2500))^2)))), x=1..50,
y=0..110000000000);
```

VITA

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