Vertical Ge/SiGeSn-Based P-Channel Nano Field-Effect Transistors Integrated on Si

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Abbreviations

BTBT	Band-to-Band Tunneling
CB	Conduction Band
CMOS	Complementary Metal-Oxide-Semiconductor
CNL	Charge Neutrality Level
CV	Capacitance Voltage
DB	Dangling Bonds
DIBL	Drain-Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
FinFET	Fin-Field-Effect Transistor
GAA	Gate-All-Around
GIDL	Gate-Induced Drain Leakage
HL	Heterostructure Layer
high-κ	High Dielectric Constant
ICP-RIE	Inductive Coupled Plasma-Reactive Ion Etching
IHT	Institut für Halbleitertechnik
IL	Interfacial Layer
ITRS	International Technology Roadmap for Semiconductors
IV	Current-Voltage
MBE	Molecular Beam Epitaxy
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NW	Nanowire
RT	Room Temperature
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectrometry
SRH	Shockley-Read-Hall
PDB-diode	Planar-Doped Barrier Diode
PDBFET	Planar-Doped Barrier Field-Effect Transistor
PECVD	Plasma Enhanced Chemical Vapor Deposition
PE-ALD	Plasma-Enhanced Atomic Layer Deposition
PPO	Plasma Post Oxidation
O-rich	Oxygen Rich
SCEs	Short Channel Effects
s-Si	Strained Silicon
TAT	Trap Assisted Tunneling
VB	Valence Band
VS	Virtual Substrate

Symbols

A	Mesa Area
C	Load Capacitance
C_{acc}	Accumulation Capacitance
C_d	Depletion Capacitance
C_{ox}	Gate Oxide Capacitance
$C_{Parasitic}$	Parasitic Capacitance
D_{Mesa}	Circular Mesa Diameter
D_{it}	Interface State Density
d	Delta Doping Layer Thickness
E_A	Activation Energy
E_C	Conduction Band Edge
E_F	Fermi Level
E_G	Energy Band Gap
E_V	Valence Band Edge
f	Frequency
g_m	Transconductance
G_p	Parallel Conductance
I_D	Drain Current
I_{on}	On-State Current
I_{off}	Off-State Current
k_B	Boltzmann Constant
L_{CH}	Channel Length
L_{Mesa}	Square Mesa Width
N_A	Acceptor Doping Concentration
N_D	Donor Doping Concentration
n_i	Intrinsic Carrier Concentration
P	Power
q	Elementary Charge
Q	Doping Dose
Q_B	Bulk Trap Charge Density
Q_D	Ionized Donor Area Density
Q_{IF}	Interface Fixed Charge Density
Q_{IT}	Interface Trap Charge Density
R	Pillar/Mesa Radius
R_S	Series Resistance
SS	Subthreshold Swing
S	Segregation
T	Temperature
T_H	Heterostructure Layer Thickness
T_i	Intrinsic Layer Thickness
T_{OX}	Gate Oxide Thickness
T_{sub}	Substrate Temperature
V_{DS}	Drain Voltage
V_{FB}	Flat-Band Voltage
V_G	Gate Voltage
V_{DD}	Supply Voltage
V_{th}	Threshold Voltage
V_t	Thermal Voltage

W	Gate Width
W_d	Depletion Region Width
x	Silicon Content
y	Tin Content
ΔE_C	Conduction Band Offset
ΔE_G	Energy Band Gap Offset
ΔE_V	Valence Band Offset
ΔV_H	Voltage Hysteresis
δ-doped	Delta Doped
δ-layer	Delta Layer
ξ	Electric Field
ϵ	Vacuum Permittivity
ϵ_r	Relative Permittivity
Φ_{B0}	Built-in Potential Barrier
μ	Mobility
υ_{sat}	Saturation Velocity
ω	Angular Frequency
τ	Carrier Lifetime

Chemical Formula

Al	Aluminum
Al_2O_3	Aluminum Oxide
Ar	Argon
B	Boron
BHF	Buffered Hydrofluoric Acid
C	Carbon
Cl_2	Chlorine
CHF_3	Trifluoromethane
C_3H_6O	Acetone
C_3H_8O	Isopropanol
$C_6H_8O_7$	Citric Acid
Ge	Germanium
GeO_2	Germanium Dioxide
GeO_x	Germanium Oxide
GeO_xN_y	Germanium Oxynitride
HBr	Hydrogen Bromide
HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
H_2O_2	Hydrogen Peroxide
HP_3O_4	Phosphoric Acid
$(NH4)_2S$	Ammonium Sulfide
$(NH_4)_2SO_3$	Ammonium Sulfite
O_2	Oxygen
Sb	Antimony
SiO_2	Silicon Dioxide
SiGe	Silicon-Germanium
SiGeSn	Silicon-Germanium-Tin
Sn	Tin
TMA	Trimethylaluminum
TEOS	Tetraethyl Orthosilicate

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Summary

In this work, the fabrication and the electrical characterization of the germanium-based vertical p-channel planar-doped barrier field-effect transistor is investigated for the first time. Setting and adjusting the device design parameters and performing experimental iterations, the fabrication process was achieved successfully. Further enhancement of the device performance was accomplished through analysing the electrical characterization and introducing amendments to the fabrication process. Concurrently, a study of Ge/oxide interface was performed by introducing several surface treatments prior to gate oxide deposition and using capacitance voltage characterization to evaluate the resulting interface quality. The surface treatments were first applied to germanium-based metal-oxide-semiconductor capacitor structures that are integrated on silicon as well. Surface treatments included conventional and non-conventional treatment methods in addition to combinations of both. Subsequently, some of the best results were used in the transistor device fabrication to prove the validity of the results of this study. The results obtained for germanium-based planar-doped barrier field-effect transistor devices integrated on silicon are optimistic, using relatively large sized devices with a simple manufacturing process, which are competitive in electrostatic performance to more complicated and aggressively scaled devices from literature. Fabricated devices show the potential for energy efficient systems by achieving sufficiently low off currents. Furthermore, leakage current sources are studied through low temperature measurements and applying the studied surface treatment for additional possible progress. Low temperature measurements showed the potential of the superior device performance and competent subthreshold swing to literature, supported by simulation analysis of reduced effective oxide thickness. A comparison is demonstrated between this work and other similar channel length devices from literature that are defect free to elaborate the excellent possible performance of the devices in this work. Along with the fabrication and characterization of the devices, a simulation model based on extracted material data from the experimental work and literature is produced. Based on the model, a proposed design of a modified device using both planar doping and a heterostructure in the channel is then presented. The channel-engineered design uses a lattice-matched germanium/silicon-germanium-tin heterostructure within the channel that can be introduced at different positions. The results show improved performance by virtue of the larger energy band gap of the ternary alloy compared to germanium, leading to suppression of the leakage currents as well as a reduced subthreshold swing, making the heterostructure device promising for ultra-low power device applications.

Zusammenfassung

In dieser Arbeit wurde zum ersten Mal die Herstellung und die elektrische Charakterisierung von Ge-basierten vertikalen delta-dotierten p-Kanal-Feldeffekttransistoren (PDB-FET engl. planar-doped barrier field-effect transistor) untersucht. Durch Designparameterstudien und iterative Experimente wurde eine Prozessfolge zur Herstellung dieser Bauelemente entworfen. Die Bauteileigenschaften konnten durch die Analyse der elektrischen Charakteristika und Anpassungen des Herstellungsprozesses verbessert werden. Gleichzeitig wurde eine Untersuchung der Ge/Oxid-Grenzfläche durchgeführt. Dafür wurde die Grenzfläche vor der Gate oxid-Abscheidung verschiedenen Behandlungen unterzogen und durch Kapazitäts-Spannungsmessungen untersucht. Zum ersten Mal wurde dies an direkt auf Si-integrierten Ge-basierten Metall-Oxid-Halbleiter-Kondensatoren untersucht. Die Oberflächenbehandlungen umfassten sowohl konventionelle als auch neuartige Methoden sowie die Kombination aus beiden. Die besten Ergebnisse wurden herangezogen, um damit Transistoren herzustellen und die Ergebnisse zu validieren. Für die auf Si-integrierten Ge-basierten PDB-FETs wurden vielversprechende Ergebnisse erzielt. Diese relativ großen Bauelemente, basierend auf einem einfachen Herstellungsprozess, sind in ihren elektrostatischen Eigenschaften konkurrenzfähig zu deutlich komplizierteren und aggressiv skalierten Bauteilen. Mit diesen Bauteilen konnte ein besonders niedriger Sperrstrom erzielt werden, wodurch sie das Potenzial für energieeffiziente Systeme haben. Weiter wurde durch Niedertemperatur-Messungen die Ursache von Leckströmen untersucht. Unterstützt durch die simulative Analyse von reduzierten, effektiven Oxiddicken zeigen diese Messungen das Potenzial für überlegene Eigenschaften und mit dem Stand der Technik vergleichbare Unterschwellwertcharakteristik. Die Bauteile aus dieser Arbeit wurden mit defektfreien Bauteilen ähnlicher Kanallänge aus der Literatur verglichen, um eine Abschätzung für den bestmöglichen PDB-FET zu gewinnen. Mithilfe extrahierter Materialparameter aus Experimenten und der Literatur wurde ein Simulationsmodell erstellt. Basierend auf diesem Modell wurde ein modifiziertes Kanaldesign, welches eine Delta-Dotierung mit einer Heterostruktur kombiniert, entwickelt. Im Kanal wurde dazu eine gitterangepasste Ge/SiGeSn-Heterostruktur eingesetzt, deren Position frei wählbar ist. Die Ergebnisse zeigen eine verbesserte Unterschwellwertcharakteristik sowie geringere Sperrströme aufgrund der größeren Bandlücke des ternären Legierungshalbleiters verglichen mit Ge. Dies macht das Bauelement mit Heterostruktur zu einem vielversprechenden Kandidaten für ultra-hocheffiziente Anwendungen.

Chapter 1: Introduction

1.1 Objective and Motivation

Moore's law is approaching its limit due to complications encountering the scaling process including power, delay and area. New device engineering techniques are required to overcome the challenges facing advanced complementary metal-oxide-semiconductor (CMOS) technology forcing it to approach its scaling limits. Maintaining More Moore's platform, which aims at improving the performance guided by technology requirements through sustained horizontal and vertical dimension scaling of the device, these challenges are mainly addressed through two main approaches. First approach is to introduce new materials that have superior characteristics beyond silicon (Si) and strained-Si (s-Si) technology. Second approach is to present new structural designs that boost up the performance of the metal-oxide-semiconductor field-effect transistor (MOSFET). In regards to the first approach, high mobility materials are heavily investigated as a promising solution to replace Si. Germanium (Ge) and III–V semiconductor material channels have recently received a lot of attention, where the co-integration of III–V material channel for n-MOSFET and Ge channel for p-MOSFET integrated on Si substrate is considered as an optimum CMOS design. Concerning p-channel devices, Ge-based field-effect transistor (FET) is regarded as the most promising device to replace Si-based p-channel FET. Ge is investigated owing to its highest hole mobility among all the semiconductors which can be exploited for higher speed devices and low power applications. The second approach involving device design is concerned with the fact that beyond the 7 nm node, the fin-field-effect transistor (FinFET) structure will be no longer capable of sustaining Moore's law and new viable designs including vertical or horizontal nanowire (NW) with gate-all-around (GAA) structures are to be employed. GAA design proved its capability of enhancing the electrostatics of the device and increasing the driving current. The main challenges faced by Ge-based FET include the channel/gate interface quality that is significantly inferior to silicon/silicon dioxide (Si/SiO_2) system, higher dielectric constant that makes it more prone to short channel effects (SCEs). In addition, the smaller energy band gap (E_G) compared to Si, which leads to elevated band-to-band tunnelling (BTBT) leakage currents, setting limitations on the achievable off-state current (I_{off}).

Vertical GAA structures employing planar-doped barrier field-effect transistor (PDBFET) can be considered as promising candidates for tuning Ge-based FET performance:

their channel is almost undoped except for a very thin region perpendicular to the gate, creating the barrier necessary for device operation. This structure enables the carriers to spread to the bulk through almost the entire channel except for a small region, where the carriers are confined to the surface. This is important for a material such as Ge, for which controlling the properties of the interface with the gate oxide has proven to be challenging. By exploiting the advantages of the PDBFET, Ge-based FET behaviour can be better inspected with carriers spread away from the surface giving higher chance of experiencing the bulk mobility of Ge. The vertical GAA structure enables efficient control on the channel electrostatics and leads to reduced SCEs. The aim of this work is to investigate the implementation of the Ge-based p-channel PDBFET (p-PDBFET) and examine the feasibility of improving the Ge-based FET performance by employing the channel engineered device structure. The study includes the full manufacturing process in the institute of semiconductor engineering (IHT) labs as well as the simulation modelling of the device experimental results to be used as a means to fully understand the device behaviour and eventually improve it. Following these outcomes, the optimization of the device design and performance is to be pursued.

1.2 Thesis Organization Overview

The thesis shows the details of fabrication and characterization of vertical Ge-based p-PDBFETs. The focus is on the usage of planar doping technique for the Ge-FET and characterizing the performance through electrical measurements and subsequent analysis. The established p-PBDFET fabricated design was then studied through varying different parameters including the doping concentration, the planar or delta doping (δ-doping) thickness and position as well as the channel length. Simultaneously, experiments to investigate the influence of different surface treatment and passivation techniques were performed to help with the process of optimization of the Ge-based p-PDBFET device performance. A simulation model was then designed, used to analyse the results and speculate means to improve the device performance. Based on this model two approaches were proceeded, a modified growth recipe with optimized device parameters design were fabricated exhibiting enhanced experimental characterization results proving the impact of both design and fabrication modifications. The second approach was to create a new vertical heterostructure design that employs both the δ-doping and the usage of heterostructure structure germanium/silicon-germanium-tin (Ge/SiGeSn) alloy. The simulation results proved to boost the performance significantly. An overview of the thesis organization with a short description of the continuing chapters will be given below.

Chapter 2: Background on Ge as an Active Channel Material and PDBFET Principle and Operation

Ge is under dense study to be replacing Si as an active material in future, in Chapter 2, a brief about the Ge as a semiconductor material is presented discussing the advantages and the challenges of the material. Then, the history of progress of the Ge-based devices is discussed as well as the latest achievements accomplished by the state of the art devices employing Ge as an active channel material for FET devices. The second part of the chapter is dedicated to the discussion of the planar-doped barrier (PDB) concept and the devices based on it, followed by a summary of the history of the evolution of the PDBFET devices that were implemented using Si transistors and the advantages it provided as a new design structure. Finally, a review about the principle of operation of the PDBFET device with general design considerations for the FET-based structures is presented.

Chapter 3: Ge-Based P-Channel Vertical PDBFET Device Fabrication, Processing and Characterization

The chapter shows the details of the fabrication, processing and characterization of the first fabricated Ge-based GAA vertical p-PDBFETs. All the devices were fabricated in the cleanroom of IHT at University of Stuttgart. An overview is given about the layers growth of the devices using the molecular beam epitaxy (MBE) system followed by the detailed description of the fabrication steps of producing the devices structures. Then the electrical characterization of the Ge-based p-PDBFETs is then demonstrated through illustrating the influence of different design parameters of the device on the behaviour. The first parameters investigated are the δ-doping layer concentration and its thickness, that led in turn to the initial doping scheme, which was used for the subsequent experiments. Afterwards, the effect of the layer position on the device characteristics is then considered. To observe the SCEs, a comparison is made between short channel and long channel devices. This was followed by a study of the behaviour of different devices in the course of defining methods to improve the p-PDBFETs performance.

Chapter 4: Study on Surface Treatment of Ge-MOS-Capacitor on Ge-Virtual Substrate on Si

Ge/oxide is the basic building block of Ge-MOSFETs that has challenging interface quality properties. In this chapter, a general experimental study of some conventional surface treatment and passivation techniques were investigated through capacitance-voltage (CV) characterization of metal-oxide-semiconductor capacitor (MOSCAP) structures integrated on Si using virtual substrate (VS) method. The investigation includes the surface passivation effect

of plasma post oxidation (PPO) and sulfur passivation. It also includes different wet chemical surface treatments such as hydrofluoric acid (HF), hydrochloric acid (HCl) and recently proposed citric acid ($C_6H_8O_7$) solution as a competent method to produce a Ge oxide (GeO_x) free surface in preparation of gate stack formation. The combination of some of these methods is presented to show the possible progress that can influence the electrical characterization behaviour. An alternative surface treatment method is proposed at the end of this chapter, which uses a combination of the new $C_6H_8O_7$ treatment together with the typical HCl surface treatment, which proved to provide good performance and have great potential to produce high quality Ge surface for MOSFET fabrication.

Chapter 5: Simulation Model and Parameter Evaluation

At this point, a simulation model was created, based on the results from the previous experimental work together with literature. Simulations were performed on Silvaco device simulation tool (Atlas). The initial simulation results showed very good agreement with the experimental results. However, the created model is then modified and updated based on the successive experimental results for more accurate modelling. The model demonstrated a very good insight for the devices actual performance and inspired methods for further design improvements to be exploited in the fabrication of the successive devices that can improve the performance significantly. The model insights were followed by secondary ion mass spectroscopy (SIMS) measurements that supported the model outcomes. The next two chapters work was based on the outcomes from this model in conjunction with the previously obtained results.

Chapter 6: Fabrication of Optimized Ge-Based P-Channel PDBFET

Based on the previous experimental results and created simulation model, in this chapter the fabrication of Ge-based p-PDBFETs with modified MBE growth recipe is presented. The channel length (L_{CH}) parameter was varied with values of L_{CH} = 100 nm, 60 nm and 40 nm that is currently the state of the art value. The improved Ge-Based p-PDBFETs devices demonstrated remarkable performance. The electrical characterization of the p-PDBFETs results obtained are optimistic achieving off-currents of sub-nA/μm. The on-state current (I_{on}) to off-state current (I_{off}) ratio (I_{on}/I_{off}) reached value of I_{on}/I_{off} = 4 – 5 orders of magnitude and subthreshold swing (SS) of value SS = 220 mV/dec using relatively large sized devices and high equivalent-oxide-thickness (EOT) that is in the range of EOT = 7 nm. The devices achieved competitive electrostatic performance to much more complicated aggressively scaled

devices. Moreover, a new surface treatment experimental study, which was never applied before to Ge-FETs, is presented verifying the improvement in the device behaviour. Furthermore, simulation work was continued to present, based on the previously established model in Chapter 5 with modifications applied according to the new results, the expected improvements with further gate oxide thickness (T_{OX}) reduction. Further potential development of the performance of the devices is shown through low temperature measurements. At temperature (T) = 215 K, the p-PDBFETs demonstrated leakage current in the range of I_{off} = $3x10^{-11}$ – $1x10^{-12}$ A/μm, on-state to off-state current ratio I_{on}/I_{off} = 5 – 6 orders of magnitude and reduced subthreshold swing of SS = 123 – 153 mV/dec. Such promising results of fabricated devices show the potential of these devices to operate for high performance and low power applications.

Chapter 7: Ge/SiGeSn-Based Vertical Heterostructure P-PDBFET Model for Low Power Applications

A modified model is developed in this chapter, where a vertical Ge/SiGeSn-based p-PDBFET design model is presented. In this design, a barrier is introduced within the Ge channel by introducing a material of wider E_G, using SiGeSn heterostrucrure layer (HL). The calculations for Ge-based channel PDBFET model is based on the previously created model in Chapter 5. The Ge/SiGeSn heterostructure model calculations of the expected E_G of SiGeSn at different alloy compositions were designed using quadratic interpolation with given parameters from literature and the alignment calculation between Ge and the $Si_xGe_{1-x-y}Sn_y$ were approximated based on Jaros approach. This design aims at overcoming the concerns in Ge-FETs, where the introduced barrier of SiGeSn shows significant mitigation of the high tunnelling rates compared to pure Ge-based FETs, defying the inherent source of leakage currents in Ge-based short channel devices. The heterostructure composition and other parameters of the design are discussed in detail; showing their effects on the characteristics of the device and the influence on the performance. With the proper design of doping and heterostructure alloy composition, the normalized I_{off} achieved is reduced down to pico-ampere range. The design simulation results exhibited promising results that qualifies it to be employed in low power applications.

Chapter 2: Ge as an Active Channel Material and PDBFET Principle & Operation

2.1 New Technology Requirements and Reframed Roadmap

Electronic applications determine the future technology requirements. Following Moore's law, scaling down the transistor dimensions attempting to accomplish higher performance through increasing computation power and operation speed at lower cost is approaching the physical limits. As the electronic device dimensions approach few nanometre range, the devices performance depart drastically from the ideal switch, essentially due to substantial power dissipation [1]. This urged the reframing of the technology roadmap with several focuses [2], among which is a major platform: More Moore. This avenue embraces the extension of Moore's law through several equivalent scaling techniques with reference to power, area, performance and cost. Recent technology applications including big data, instant data and internet of things (IOT) require high performance, extremely low power consumption with reduced leakage, and variability. The mobile applications adds the restriction of the area to all of the above. Many challenges are encountered during the processes of scaling and integration in conjunction with accomplishing the expected performance. Some key encounters include preserving high drive currents while scaling the power supply and controlling the subthreshold current or leakage. In addition, superb electrostatic control is required to diminish SCEs and the production of excellent epitaxy quality while using lattice-mismatched active materials to retain the low cost and provide variability.

The rising emphasis on reducing the device power consumption has led to several possible solutions. The solutions are concerned with certain aspects, one of which is the improvement of the electrostatic control of the device and isolation. This approach is possible through the transition to new device architectures, which can help overcome obstacles faced by present structures. Sub 7 nm node device implementation is expected to be the end of downscaling of Si-based FinFETs: at this point employing alternative device geometries of Multi-Gate FETs such as GAA [3] structurers is essential. GAA transistor is a FET device that features a gate surrounding all the sides of the device channel, which is succeeding in overcoming the scaling performance limitations of FinFETs, specially the supply voltage (V_{DD}). GAA is considered as a good candidate for sub 7 nm technology node due to its stronger electrostatic control. IBM, in 2017, revealed 5 nm transistor employing horizontal GAA based

on stacked nano-sheets architecture replacing FinFET [4]. In 2018, Samsung latest researches demonstrated 3 nm node using as well horizontal GAA FET structures known as multi-bridge-channel FET (MBCFET) that improves the gate control [5]. Fig. 2.1 illustrates the evolution in the architecture of the MOSFET structures throughout the years, starting with the planar MOSFET technology that prevailed the microelectronic industry for decades (2.1(a)). The planar technology encountered severe scaling problems and was replaced by the Tri-gate transistor; FinFET structure (Fig. 2.1(b)) that was introduced by Intel at the 22 nm technology node, which is now again approaching its scaling capability limits and being substituted by the GAA design structure (Fig. 2.1(c)).

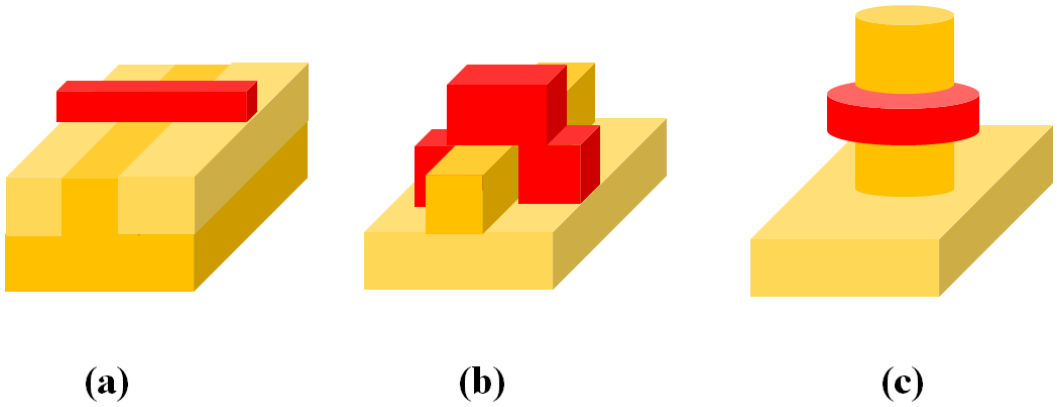


Fig. 2.1 MOSFET design structure development.

Augmented research is dedicated to substituting Si with high mobility materials as another major approach. The substitution of Si-based CMOS design with high mobility materials is expected to achieve significant power consumption reduction and upgraded speed while keeping the driving currents at the adequate values. Among new channel materials, III-V compound semiconductors are promising [6] [7] [8] especially for n-channel devices owing to possessing the highest electron mobility. For p-channel devices, Ge is regarded as the optimum choice for drive current boosting at lower V_{DD} [9] due to its superior hole mobility [10]. Intensive research is continuously conducted on Ge-based transistors [11] [12] [13] [14] [15]. Based on this fact, the co-integration of low power semiconductors as Ge p-channel FETs with III-V materials as n-channel FETs is considered as a promising solution that can substantially promote the performance of CMOS circuits [16].

2.2 Ge as an Active P-Channel Material

2.2.1 Ge Semiconductor Bulk Properties

Among all the semiconductors, Ge has the highest bulk hole mobility (μ_h), providing a factor of 4 times improvement compared to Si. In Fig. 2.2, intrinsic bulk electron and hole mobility for various semiconductor materials are plotted against E_G of the material. The E_G is a very important and effective parameter, where its value affects the performance concerning the voltage supplied for operation and the scalability of the device [10]. According to the technology requirements, devices that operate at low V_{DD}, which is interpreted as faster switching as well, involves the usage of small E_G materials. Nevertheless, as E_G value gets extremely small, the leakage of the device increases dramatically which is a main concern in the process of scaling down i.e. affects the I_{on}/I_{off}. Ge fits into the region of both possessing a relatively small E_G suitable for low power/fast operation however large enough to prevent huge leakage currents as compared to some of the III-V materials. Ge also shows the closest relation between its electron mobility (μ_e) and (μ_h) values (μ_e is about twice μ_h), which can result in a better size balance for the design of p-channel and n-channel transistor for a CMOS architecture.

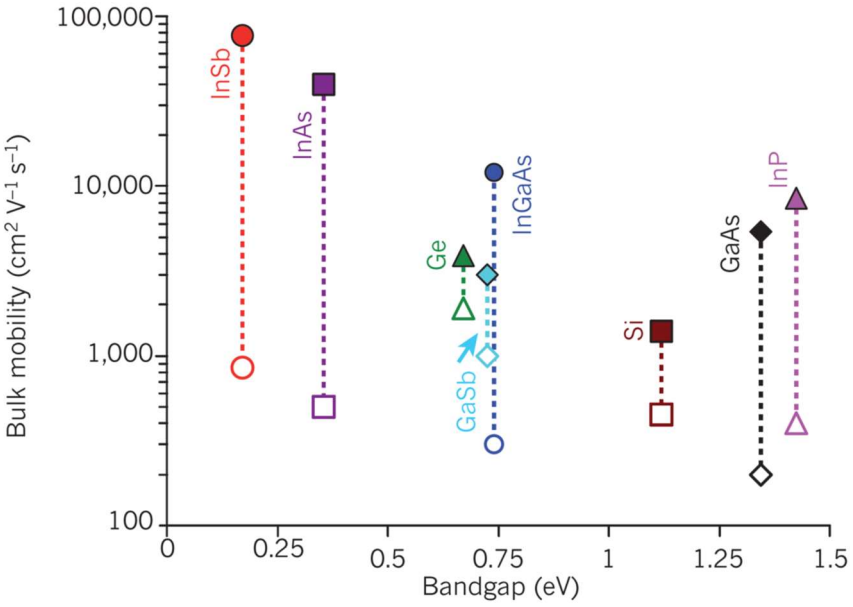


Fig. 2.2 Mobility landscape of semiconductors, after [10].

Table 2.1 illustrates the basic parameters of Si and Ge. Ge has larger lattice constant that constitutes mismatch when grown on Si substrate of ~ 4.2%. The E_G of Ge is much smaller compared to Si causing higher intrinsic carrier concentration (n_i). The electron and hole mobility are quite larger than those of Si as mentioned formerly. The relative permittivity (ϵ_r) is also higher indicating stronger response to applied fields.

Table 2.1 Properties of Ge in comparison to Si [17] [18].

Semiconductor	Lattice constant (Å)	Electric band gap (eV)	Mobility (cm^2/Vs)		Intrinsic carrier concentration (cm^{-3})	Relative permittivity ϵ_r
			μ_e	μ_h		
Si	5.431	1.12	1450	500	9.65×10^9	11.9
Ge	5.646	0.66	3900	1900	2.33×10^{13}	16.0

Ge has been advocated as a replacement for Si as active channel material in FETs, especially for p-channel, because of its superior transport properties, possessing the highest mobility of all semiconductors for p-channel devices. Ge channels also provide very interesting performance characteristics due to its smaller E_G, allowing for reduced power consumption due to requiring less V_{DD}, which in turn can provide faster switching speeds. The low processing temperatures used for Ge-based devices make the material compatible with advanced high-κ materials and metal gates [19] [20] [21]. An additional advantage is the possibility of alloying Ge with Sn [22] [23] that has been shown as an electric performance booster for Ge-based devices (with a possibility of higher electron and hole mobility). Ge can also be alloyed with Si and Sn enabling tunable E_G and strain engineering [24] [25]. All these tuning strategies have the additional advantage of being compatible to Si technology.

The main challenges for Ge-based FETs start from its smaller E_G as well, seen as a noticeable increase in leakage current that is introduced due to high rates of BTBT [26]. The higher ϵ_r of Ge makes it more prone to SCEs [27], where it becomes more difficult for the gate to switch off the channel due to the strong coupling between the source and the drain. Extraction and production of Ge bulk (Ge Czochralski) wafers has considerably high manufacturing costs. In fact, virtual substrates (VS) of epitaxially grown Ge on bulk Si offers major advantages over bulk Ge [28]. It is more convenient to integrate Ge channels on Si, for rather economic production in addition to better mechanical strength and improved compatibility with prevailing Si processing technology. Therefore, utilization of Ge for electronic devices is expected to be in the form of thin epitaxial layers on low-cost available Si-wafers. This is still a challenging

process for large-scale integration due to their thermal budget mismatch. The produced Ge layers need to be of a high crystalline quality with negligible threading dislocations and defects otherwise, this will substantially affect the performance if the devices are built on layers with flawed structure [29].

Concerning MOS devices, one of the most vital properties is the interface quality at the dielectric/Ge gate stack. The properties of germanium dioxide (GeO_2) are quite different from those of SiO_2 where it is not easy to grow oxide on Ge as easy as SiO_2/Si system. Due to the lack of thermodynamic stability (especially desorption of the sub-oxide GeO_x) [30] and its solubility in water, the interface quality deteriorates which hinders the development of Ge MOS devices. To overcome this challenge, several methods have been under study to find a suitable passivation method for Ge surface in addition to chemical treatment techniques to be applied prior to oxide deposition.

2.2.2 Ge-Based Field-Effect Transistor History

Ge is not new to the semiconductor industry; it was the material of choice for the first transistor in 1948 [26]. For more than a decade, Ge was almost exclusively the manufacturing material for solid-state devices [10] while being used as well for constructing many important physical theories. On the other hand, its progress in the field-effect devices was less successful, due to the critical surface properties of Ge and the lack of sufficiently stable oxide. Hence, with the absence of sufficient passivation for its surface, Ge was side-lined with the rise up of the CMOS technology at the beginning of the 1960's where Si took over and dominated the electronic device manufacturing. The discovery of the superior native oxide SiO_2 as interface passivation scheme for Si devices has led to the introduction of the planar technology which sustained microelectronics industry for decades.

In 1965, Gordon Moore observed that the number of transistors on an integrated circuit chip could be predicted to double annually for at least ten years [31]. The transistor count on chip sustained to increase while doubling at altered time points varying from 18 to 36 months [26]. While the size of the transistor decreased accordingly at remarkable rate, Gordon Moore's postulate became known as Moore's law with doubled transistor count approximately every two years. By doubling the number of devices per unit area, the fabrication cost per device was recurrently decreased, the density/functionality of the devices was increased and the semiconductor industry continued to advance. This law remained the main guidance for the microelectronics manufacturing process for decades where the best way of improving the

CMOS technology performance was established on scaling down the Si/SiO_2 system. As the size scaling continued, many obstacles were faced concerning the performance and power consumption. Ideal CMOS scaling seized beyond sub-100 nm range [32]. Up to 2002, the main technique for upgrading the performance was carried out through improving the operating frequency (doubling it every 18 months) [33]. The continuous scaling of threshold voltage (V_{th}) resulted in great leakage currents. To keep good control on the device, V_{DD} was kept relatively higher than the corresponding scaling scheme. Hence, the processing power density was increasing substantially and the pace of performance enhancement dropped significantly, mainly due to the increased leakage. In other words, transistor dimensions scaled-down quicker than its power consumption, and hence the power density scaled-up drastically throughout the years. Henceforth, necessity for further power scaling per transistor is inevitable. Generally, the power consumption per transistor (P) is given by [34]:

$$P = \alpha f C V_{DD}^{2} + I_{off} V_{DD} \qquad \text{eq. 2.1}$$

where α is the switching activity, f is the clock frequency and C is the load capacitance. The first term represents the switching or the dynamic power and the second term represents the stand-by or the static power. Power reduction can be achieved by several parameters, most effectively by reducing V_{DD}.

Various solutions were constantly introduced and developed, to keep Moore's law at pace. One powerful candidate solution is the search for a new material system to replace Si in order to sustain the growth of electronic devices functionality and performance through great V_{DD} scaling. Foreseeing the restriction of approaching the limits of the miniaturizing, attempts started to re-introduce Ge in the FET manufacturing process, owing to its higher carrier mobility, at a quite earlier stage at the late 1980's. Several successful results exhibited improved performance concerning mobility and driving current that outperformed Si-based devices [35] [36] [37] [38]. Compared to Si, Ge-based FET fabrication process was still immature and not feasible to replace the well-established Si-technology within this period due to the challenges related mainly to its oxide quality. Striving for better interface quality that boosts the MOSFET performance has also been continuously pursued and progress has been achieved throughout the last two decades [39] [40] [41] [42].

Meanwhile, the well-developed Si fabrication processes allowed the incorporation of Ge producing silicon germanium (SiGe) alloys using MBE that became an established technology, enabling high-quality strained materials of SiGe on Si [43] [44]. With the known

limitations accompanying further scaling, the main way to continue was to enhance the carrier mobility through applying strain to the channel via employing channel engineering. By exploiting the aspects of such advanced Si technology, SiGe could be used to produce substrate layers for growing s-Si channels [45] or using SiGe alloy itself as active channel material as well [46]. Only by the mid-1980s, SiGe and s-Si FETs were feasible, once low-temperature growth of Si epitaxy was possible [47]. Due to the difficulty of achieving high quality oxide at low temperatures, it was not until 1991 when first functional SiGe p-channel MOSFETs were presented [48]. Attention was also turned to s-Si MOSFETs on relaxed SiGe layers, with the aim of enhancing the mobility of both types of carriers and s-Si p-channel MOSFET was demonstrated in 1993 [49]. The strain engineering accomplished substantial enhancement in both n-channel FETs and p-channel FETs and proved to be successful for channel with length down to few nanonmeters [50]. The first introduction to commercial usage was at the 90 nm technology node, which came to be a mainstream for most companies, first demonstrated by Intel in 2002 [51]. The strained channel solution enabled sustaining the transistor feature size shrinking process for about two decades [52] [53] [54].

Within the process of scaling down the devices, dimensions including T_{OX} are being reduced accordingly. The scaling down of T_{OX} encountered problems of troublingly raised leakage current and stand-by power consumption. By the reduction of the thickness of the SiO_2 gate oxide beyond T_{OX} = 20 Å, huge gate leakage arouse due to quantum tunnelling through the gate oxide leading to deteriorated and unreliable performance. As the SiO_2 had to be replaced, the need for new dielectric materials became essential and eventually high dielectric constant (high-κ) materials were introduced [55] [56]. The higher ϵ_r of the material allows the usage of a thicker physical layer of dielectric material, compared to SiO_2 that can be exploited without compromising the gate capacitance, which is a major factor of improving the drive current of the device. In 2007, high-κ/metal gate stack was integrated into manufacturable 45 nm node technology [57]. High-κ/metal gate achieved higher performance and superior scalability. With the introduction high-κ materials instead of SiO_2, the binding to the Si-based electronic devices came to be less restraining. The replacement of Si with other higher mobility channel materials turned out to be more essential.

2.2.3 Recent Progress of Ge-Based FETs – State of the Art

Within the last two decades, the Ge-based FETs has been under heavy investigation in order to validate its capability to replace Si in the near future as predicted by more Moore platform. Ge is being incorporated as an active channel material for both p-channel and n-channel transistors. The focus will be mainly on the progress of Ge-based p-channel devices where a lot of attention has been paid to employing it in different FET designs [58] [59] [60]. As discussed above concerning the Ge challenges, the main aim is to improve the Ge/dielectric interface quality as the building block of the FET structure and integrating the channels on Si while keeping its superior mobility property that is the principle reason for its selection. The lower E_G leads to higher leakage, which directs the attention to the achieved I_{off} by the FETs under consideration. The SS value is a measurement for the interface quality and the I_{on}/I_{off} indicates the strength of the gate control of the device and hence an overall estimation of the device capabilities. In 2011, S. -H Hsu et al. [61] demonstrated a nearly defect free Ge-GAA based FET on Si substrates showing superior improvement of device performance by removing the dislocations resulting from integration on Si, the gate channel length achieved was L_{CH} = 183 nm with subthreshold swing of SS = 130 mV/dec and I_{on}/I_{off} = $1x10^5$. In 2014, M. J. H. van Dal et al. fabricated Ge p-FinFET by using aspect ratio trapping epitaxy [62], where for channel length of L_{CH} = 110 nm a subthreshold swing of SS = 108 mV/dec is obtained and with L_{CH} = 70nm exhibiting peak transconductance (g_m) = 1.05 mS/µm. Another mile stone of Ge-based FETs progress was demonstrated by Y. -J Lee et al. [63] in the fabrication of suspended diamond shaped Ge NW channel on Si by undercutting the dislocations near the Si/Ge interface. With L_{CH} =100 nm and SS = 167 mV/dec they achieved $I_{on}/I_{off} > 10^8$, the highest ever reported for Ge-based p-FETs. With the continued heavy research on Ge-based FETs, further studies by H. Wu et al. presented a hybrid Ge NW CMOS with accumulation mode n-MOSFET and inversion mode p-MOSFET for the first time on a Si substrate. In addition, they also showed a fully depleted Ge-CMOS devices and logic circuits fabricated on a Ge-on-insulator (GeOI) substrate, with a novel recessed channel and source/drain structures [64] [65]. The work showed high performance with symmetric behaviour CMOS structure employing short channel lengths with state of the art value of L_{CH} = 40 nm.

Recently in 2017, Imec demonstrated a strained Ge NW p-channel GAA-FETs on SiGe strain relaxed buffer. This work showed a significant improvement in Ge-based GAA devices. The Ge GAA devices confirmed excellent electrostatic control at the shortest gate lengths studied of L_{CH} = 40 nm with linear SS = 74 mV/dec [66] . In 2018 Imec continued their work

advances in Ge-based FETs, by introducing for the first time GAA vertically stacking of highly-strained Ge NW GAA p-FET with L_{CH} = 45 nm [67]. The work showed a great improvement in the driving current with values of I_{on} = 500 μA at I_{off} = 100 nA approaching the best FinFET reported values and achieving linear SS = 64 mV/dec. In general, the state of the art advances of Ge-based FETs has proven great potential and a solid viability of replacing Si-based FETs in the near future with Ge, especially in low power logic applications.

2.3 Planar-Doped Barrier FETs

2.3.1 History of Planar-Doped Barrier-Based Devices

The δ-doping profile is produced by growth-interrupted dopant deposition, was first reported by S. J. Bass in 1979, when he demonstrated that strong surface adsorption of Si to a non-growing GaAs surface produced sharp doping spikes [68]. In 1988, Schubert et al. [69] showed that high spatially confined Si-doping profiles to a layer with thickness comparable to the lattice constant in GaAs can be achieved at substrate temperature (T_{sub}) < 550°C during growth.

Studies showed that some mechanisms may interfere and affect the δ-doping distribution characteristics, including major broadening mechanisms such as diffusion [70] [71] (symmetric distribution), which is mainly dependent on growth temperature, or preferential impurity migration towards the growing surface (asymmetric distribution) that may occur due to classical segregation or solubility limit or Fermi-level pinning. Techniques used to evaluate the spatial localization are the CV profiling and SIMS measurements, where both techniques show agreement.

The δ-doping enables exceptional characteristics of decisive control of doping profile with large concentrations and great potential modulation within a miniature length scale. A variety of innovative structures in optoelectronic and electronic devices had been implemented within conventional designs showing great improvement in the performance. In III-V materials, the δ-doping technique was employed to optimize the performance of many device designs, as in optical modulators [72] where δ-doping was used to enhance electro-absorption in quantum wells by incorporating alternative n+ and p+ δ-doping forming square quantum wells, which produces significant enhancement in the modulator sensitivity . The δ-doping technique was applied as well in diode designs, called planar-doped barrier diode (PDB-diode) and was proposed as an alternative to Schottky diodes. PDB diode showed advantages qualifying it to

have a significant role in high frequency applications as mixers [73] [74] and detector diodes [73] showing higher sensitivity and low power requirements. The δ-profile technique was also used in avalanche photodiodes [75] by placing δ-doped layer in the multiplication region to add a degree of freedom for the thickness and doping limitations of the design requirements, enabling possible device improvements in gain bandwidth product and noise. In addition to improving device performance, δ-doping was also utilized in controlling the properties of interfaces of different materials, as in band offset tuning [76], and reduction of heterojunction band discontinuity [77]. Such interface engineering using δ-doping was exploited in HBTs as well [78] to enhance the device performance through reducing the hetero-structure potential spike at the emitter junction, while conserving the abruptness of the heterojunction, hence increasing the current gain. Moreover, the technique was also developed in other electronic devices such as metal semiconductor FETs (MESFETs) and High Electron Mobility Transistor (HEMT) where the δ-doped planar-FET structure achieved several improvements compared to the homogenously doped FET devices including higher trans-conductance and larger breakdown voltages while demonstrating reduced SCEs [79].

In Si, the first demonstration of δ-doping of Si as an accommodating material using Sb was accomplished by Zeindl et al. in 1987 [80]. For p-type doping, it is possible to produce sharp δ-profile using Boron (B) [81], at low temperatures due to its low segregation coefficient. The employment of δ-doping technique in Si-diodes resulted in significant improvement as in the design of triangular barrier diode (TBD) [82] and tunnel diodes [83]. In 1993 the first vertical MOSFET device employing the δ-doping layer was developed by Gossner et al. introduced as PDBFET [84]. The idea of the PDBFET arouse as a means to overcome the limitations in the planar devices within sub 100 nm range including hot carrier effects and avalanche breakdown [85]. Applying PDB concept as a channel engineering technique in Si-based FETs enabled precise control of the electric field inside the FET channel [86]. The electric field variation on a nanometre scale lead to freedom in the active field design, in other words, tailoring the electric field inside the channel. Such control demonstrated higher drive currents and enabled avalanche multiplication suppression hence higher operation voltages [87]. Further investigations on the new design performance in comparison to homogenously doped devices showed the superiority of the design regarding achieving lower I_{off} and V_{th} leading to reduced power consumption as well as improved subthreshold behaviour and increased g_m [88]. With the design facilitating the control of the electric field inside the channel by repositioning the delta layer (δ-layer) within the channel, the performance of the device can be boosted. According to the application requirements (analogue or digital design) the current saturation

behaviour, breakdown voltage and saturation current values can be optimized [88] [89] supported by simulation work [90], proving further speed capability [91] and reduced SCEs such as hot carrier degradation [92] can be accomplished by controlling the δ-layer location. Moreover, the experimental observations on low temperature measurements (between 4.2 K – 30 K) of PDBFET reported transfer characteristics with noticeable equidistant current oscillations, resembling the behaviour of Single Electron Transistors (SET) [93]. The unique doping profile demonstrated another phenomenal behaviour, where at relatively higher drain voltage (V_{DS}), Impact Ionization MOS (IMOS) behaviour was detected. The gate controlled impact ionization devices are fabricated using adequately high δ-doping PDBFET structure [94] [95] that could effectively reduce the SS using high fields created producing high impact ionization rates that achieve instant switching on of the device. IMOS based on PDBFET accomplished pronounced performance achieving SS < 20 mV/dec without reported degradation in performance.

The PDB principle realized in Si-based FETs (Si-PDBFET) demonstrated promising performance compared to homogenously doped MOSFETs concerning device characteristics such as current switching behaviour and SCEs. All these outcomes qualify the PDB concept to be an excellent candidate for high performance and high speed devices. Although all of the PDB work has been demonstrated mainly in III-V and Si materials, however it is applicable to all semiconductors in general. In fact, exploring new materials will lead to results that are even more interesting for such promising device structures.

2.3.2 PDBFET Theory of Operation

The PDB structure depends on the precise control of layer thickness and doping levels, which is enabled by the MBE technique. The flexibility in design permitted by MBE allows for structures that cannot be fabricated by planar processes, as controlling the thickness of the layers on atomic scale that is independent of lithography process. The δ- doping is constructed by a special control during MBE, unlike the growth process that is in general continuous and unaffected by the doping process. Meanwhile in δ-doping the process is altered by some means, using interrupted-growth. In this case, the epitaxial growth is first suspended, a pre-purge step is used and then the doping atoms are deposited on the accommodating semiconductor surface [96]. Then, the crystal growth is resumed, producing a very narrow doping distribution, typically of a few monolayers wide. Ideally, the doping distributions can be considered as δ-function as in equation 2.2 [97] .

$$n(z) = n_{2d}\,\delta\,(z - z_d) \qquad \text{eq. 2.2}$$

where, $n(z)$ is the dopant distribution in growth direction (z), z_d is the location of the plane of the doping atom and n_{2d} is the sheet dopant density assuming dopants are confined to the plane $z = z_d$. However, practically, diffusion, surface roughness and segregation effects makes the control on the sheet doping concentration more difficult. The dopant redistribution profile (if assumed symmetric) can be well described by Gaussian function as [71] [96]:

$$n(z) = \frac{n_{2d}}{\sigma\sqrt{2\pi}} exp\left[-\frac{1}{2}\left(\frac{z-z_d}{\sigma}\right)^2\right] \qquad \text{eq. 2.3}$$

where σ is the standard deviation of the Gaussian distribution. Hence, by fitting experimental measurement, the sheet density and the profile width can be extracted.

The PDB structure is formed in an p(n)+ / i / δ-n(p)+ / i / p(n)+ doping profile, in which a very thin highly doped layer is inserted between two undoped regions confined by two contact layers of opposite doping type. The resulting doping profile forms a triangular shaped barrier in the band structure that impedes the flow of carriers between the contact regions where the carrier transport is controlled by thermionic emission above the created barrier [98]. The produced potential barrier height and asymmetry in characteristics of carrier current are controlled by the δ-doping of acceptor doping concentration (N_A) or donor doping concentration (N_D), the thickness of the intrinsic layer (T_i) and the δ-doping layer thickness (d). A schematic cross-section of the layer arrangement of PDB-diode of p-i-n-i-p structure is shown in Fig. 2.3 with illustration of the energy band barrier generated for holes. Alternative diode of n-i-p-i-n layer structure can be built with a barrier produced for electrons.

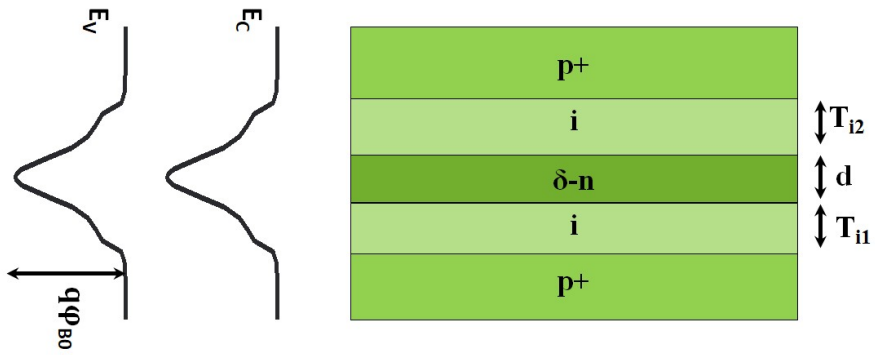


Fig. 2.3 Schematic view of layer sequence of PDB-diode with the corresponding formed energy barrier.

The zero-bias (built-in) potential barrier (φ_{B0}) height is calculated using eq. 2.4 [99]

$$\varphi_{B0} = \frac{(T_{i1}.T_{i2})}{T_{i1}+T_{i2}} \frac{Q_D}{\epsilon_s} \qquad \text{eq. 2.4}$$

where Q_D is the ionized donor area density.

For the δ-doping, the thin region at zero bias will be fully depleted forming a space charge sheet and narrow space charge region will be created in the contact regions. Solution of Poisson's equation will produce the electric field and potential barrier shown in Fig. 2.4 (b) in comparison to the homogenously doped MOSFET solution shown in Fig. 2.4(a) [86]. The resultant shape of electric field differs for both FETs. Within the homogeneously doped MOSFET, the electric field builds up linearly changing sign in a gradual manner, whereas within the channel of the PDBFET the electric field at the position of the δ-layer, varies in an abrupt step from a negative to positive value, demonstrating a constant field on both sides of the δ-layer. When the doping concentrations are chosen in both transistors such that the barrier height is equivalent leading to consistent V_{th}, the maximum of the electric field in the PDBFET is reduced to half of that of the MOSFET. The potential in the homogeneously doped MOSFET is a parabolic shaped barrier however in the δ-doped FET the potential barrier is triangular in shape. There are many advantages of a PDB structure compared to Schottky diode structure, which is mainly, the separate control of the zero bias barrier height and degree of symmetry of current-voltage (IV) characteristics. The zero bias barrier height can be varied almost from zero to slightly less than the value of E_G of the semiconductor material [100]. The capacitance of the devices using PDB structures are expected to be basically constant within the bias voltage of operation for equally doped contact regions. The PDB is a majority carrier semiconductor structure, where the carrier transport in these structures is controlled by thermionic emission over the barrier, enabling devices incorporating them to be operated at extremely high frequencies.

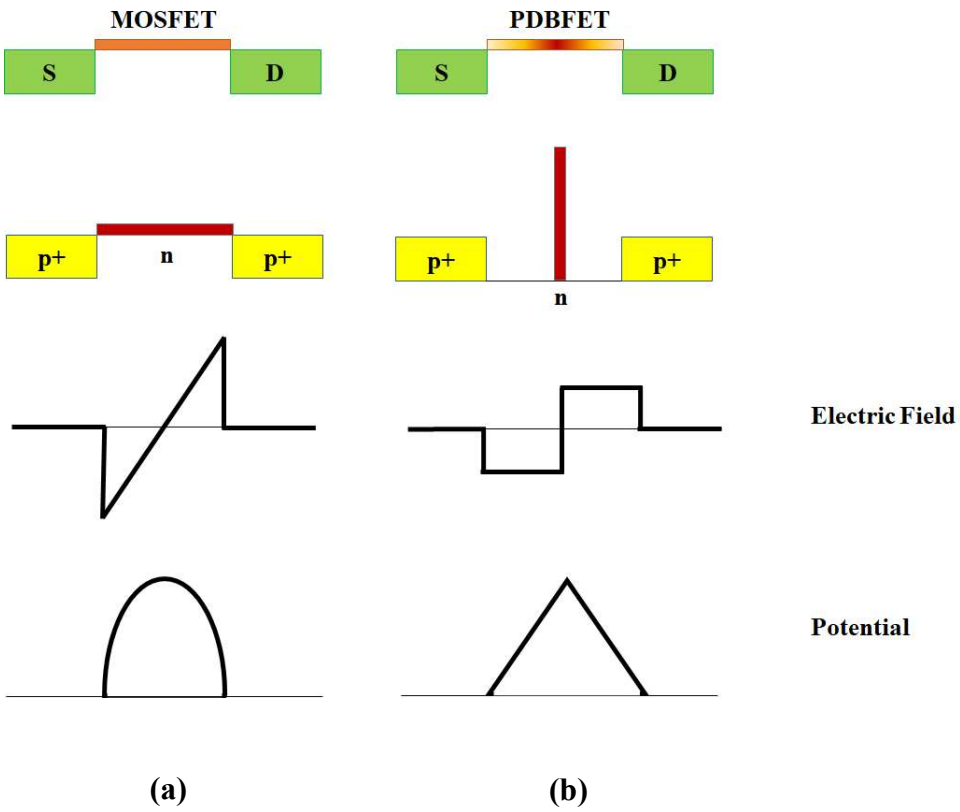


Fig. 2.4 Schematic view of geometric structure, doping profile, electric field and built-in potential of homogenously doped MOSFET versus PDBFET.

Since PDB structure enable precise control of the electric field inside the channel, it can be employed to optimize the performance in a vertical MOSFET structure. A significant improvement is achieved by the usage of vertical GAA transistor since the gate surrounds the circumference of the mesa sidewall, which increases the overall width of the gate (Fig. 2.5(a)). The vertical GAA transistor has several advantages over the planar devices including (i) higher packing density, since for the same drive current smaller GAA devices are needed (ii) better gate control due to surrounding gate, which in turn leads to improved subthreshold characteristics. In general, the depletion capacitance (C_d) in GAA structure is given as [101]:

$$C_d = \frac{\epsilon_S}{R \ln\left(\frac{R}{R-W_d}\right)} \qquad \text{for } R \geq W_d \qquad \text{eq. 2.5}$$

ϵ_S is the dielectric constant of the semiconductor, R is the radius of the semiconductor mesa or pillar and W_d is the depletion region width (Fig. 2.5(b)). This shows that C_d decreases as a function of the mesa radius, approaching zero as $R = W_d$.

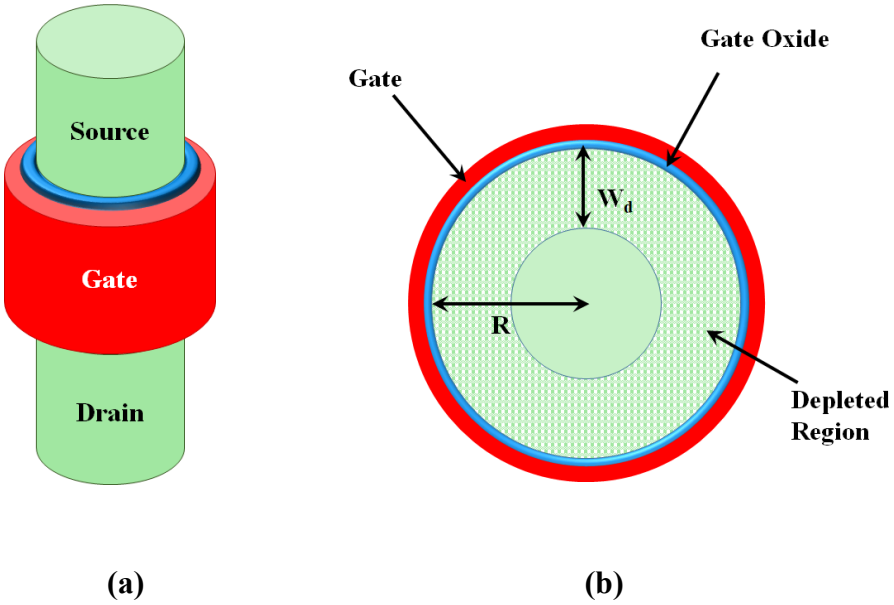


Fig. 2.5 (a) Schematic view of vertical GAA transistor, (b) cross-section of the GAA transistor.

For the subthreshold region behaviour, SS is given as :

$$SS = \ln(10)\,\frac{k_B T}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \qquad \text{eq. 2.6}$$

with C_{ox} is the gate oxide capacitance , T is the temperature, q is the elementary charge and k_B is Boltzmann constant. Here the relation shows that for an optimized SS, C_d is required to be minimum, therefore the smaller the size of the mesa, the better the SS performance. An important point is that CMOS technology is compatible with the vertical growth process (simply by the growing of opposite layers on top).

The merging of the advantages of PDB structure and the GAA vertical FET offers several advantages. While the δ-doping profile enables the precise design and control of the electric field inside the FET channel, moreover, the GAA structure itself further improves the gate control over the channel fields, which further strengthens this system. The PDB profile design is in such a way that the whole concentration is restricted in a sharp δ-doping profile surrounded by two intrinsic channel layers. This leaves the channel almost undoped except for a very thin region perpendicular to the gate, creating the barrier necessary for device operation. The structure of the GAA-PDBFET device is shown in Fig. 2.6.

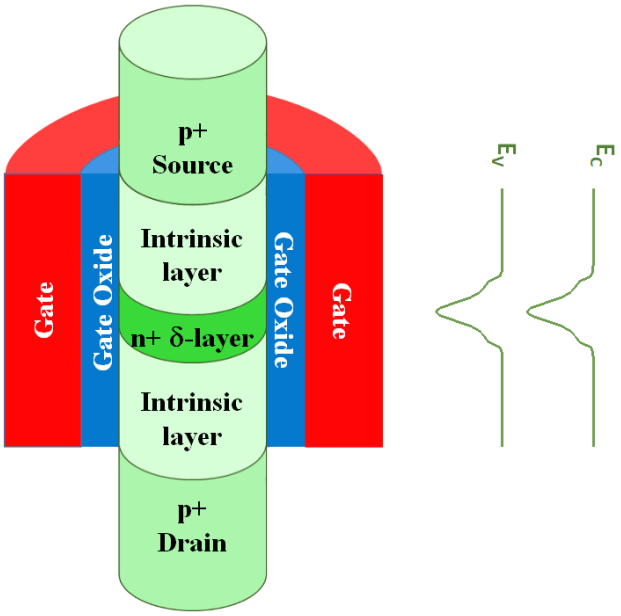


Fig. 2.6 Cross-sectional view of the layer sequence of the p-PDBFET transistor and the resulting barrier within the channel.

Since the intrinsic regions form most of the channel length, this guarantees the reduction of the impurity scattering of the channel carriers. Furthermore, the carriers within the intrinsic region of the channel are less confined to the surface forming deeper inversion channel and carriers are spread more into the bulk causing effective reduction in surface scattering of carriers allowing bulk transport behaviour to dominate the device performance. This in turn leads to the improvement of I_{on} and g_m, which was proven experimentally in literature. The intrinsic regions also reduce SCEs by reducing electric field near the drain leading to reduced hot carrier effect and higher breakdown voltages. The improved subthreshold behaviour as in the reduction of the leakage current is mainly due to the depressed direct tunneling at the drain-channel region. On the other hand, the existence of sharp thin doping barrier prevents punch through effects and gives a degree of freedom for controlling V_{th}.

2.3.4 MOSFET Design Considerations

Some important parameters that characterize the transistor performance and affects its reliability.

i) Drive current I_{on}:

The drive current or the on-state current I_{on} is defined as the drain current (I_D) at the gate voltage (V_G) equal to the drain supply voltage V_{DD}. Within the scaling process of devices, SCEs

lead to the reduction of the driving current due to factors such as saturation velocity (υ_{sat}) as a result of increased fields inside the channel and mobility degradation caused by interface quality problems due to using high-κ dielectrics. The drain current in the saturation region in short channel devices is calculated as [102] [103]:

$$I_{DSAT} = \upsilon_{sat}\, C_{ox}\, W\, (V_G - V_{th} - V_{DSAT}) \qquad \text{eq. 2.7}$$

$$\upsilon_{sat} = \frac{\mu_{eff}\, \xi_C}{2} \qquad \text{eq. 2.8}$$

where W is the gate width, V_{th} is the extrapolated threshold voltage, V_{DSAT} is drain saturation voltage at which carriers velocity is saturated, μ_{eff} is the effective carrier mobility and ξ_C is the critical electric field at which carrier velocity saturates. To reverse the short channel behaviour and increase the drive current, the effective mobility could be raised by using higher mobility channel material and enhancing gate oxide interface quality. Drive current is boosted by increasing C_{ox} value by reducing T_{OX} or essentially, by using high-κ dielectrics. Additionally, by improving the electrostatics inside the channel through increasing the overall W using GAA structures or by means of a design that reduces the effective electric field inside the channel.

ii) Subthreshold Swing (SS):

In the subthreshold region, where the semiconductor surface is in weak inversion or depletion, the subthreshold current flows determining how sharply the current reduces with gate bias V_G. It is a very important measure of the swiftness of the device to change between the on-state and the off-state, setting limitations on the device switching speed. The SS is essentially calculated as:

$$SS = \left(\frac{d(\log(I_D))}{dV_G}\right)^{-1} \qquad \text{eq. 2.9}$$

defined as the required change in V_G to reduce I_D by one decade. For a MOSFET, the theoretical limit for the minimum attainable SS at room temperature (RT) is 60 mV/dec. The limit comes from the thermal injection process of carriers over the energy barrier controlled by the gate. The equation can be rewritten as in eq. 2.6, with introducing the effect of interface trap capacitance (C_{IT}) in determining such parameter [17]:

$$SS = \ln(10)\, \frac{k_B T}{q} \left(\frac{C_{ox} + C_d + C_{IT}}{C_{ox}}\right) \qquad \text{eq. 2.10}$$

To keep the SS minimized, the main parameters include reducing the T_{OX}, improving the gate/oxide interface quality and optimizing the doping profile (minimize the doping). Moreover, as discussed in previous section, the device size have a great impact on improving the SS performance.

iii) Transconductance:

The g_m, is an important figure of merit for a transistor, defined as the change occurring in the output I_D corresponding to the change imposed on the input V_G. It is a key parameter that determines the gain of the transistor which translates into high speed performance. It can be considered within the two operational regions of the transistor; the linear or saturation modes according to the applied V_{DS}, as described in eq. 2.11.

$$g_m = \frac{dI_D}{dV_G}\Big|_{V_D=constant} \qquad \text{eq. 2.11}$$

where for a short channel MOSFET devices limited by the saturation velocity and high electric field performance, the transconductance calculation for saturation region ($V_D > V_{DSat}$) is dependent on three main parameters:

$$g_{m\_sat} \propto \upsilon_{sat} C_{ox} W \qquad \text{eq. 2.12}$$

Here the g_m is primarily determined by the saturation velocity, which means the channel material, C_{ox} which is mainly dependent on the material of the dielectric and T_{OX} and finally on W referring to the electrostatic control of the device. High I_{on} and hence g_m can be achieved by proper design of the above parameters besides achieving a high quality gate oxide/semiconductor interface.

iv) Leakage/off-state current

For low-voltage, low-power applications (digital logic and memory applications), this parameter is a crucial concern. In weak inversion and depletion, different causes can contribute to a current flow leading to high power dissipation of devices in the off-state (high static power consumption). Dominating leakage mechanisms include:

a) Shockley-Read-Hall :

Crystal imperfections in the bulk or at the surface and threading dislocations act as trap (generation/recombination) centers within E_G. Transitions described by electron and hole capture processes occurring within the junction depletion region contribute to the leakage current. The net transition rate can be described by the Shockley-Read-Hall (SRH) statistics U_{SRH} [17], which is maximized for trap levels near to the mid band gap. The total generation current density is given as:

$$J_{SRH} \approx q\, U_{SRH}\, W_d = \frac{q\, n_i\, W_d}{\tau} \qquad \text{eq. 2.13}$$

where W_d is the created depletion layer width and τ is the generation carrier lifetime . J_{SRH} is controlled by the temperature dependence of n_i . The activation energy (E_A) of the SRH leakage current is close to half of the E_G of the material [26].

b) Indirect Band Tunneling:

Carrier tunneling through the existing band gap trap-centers is another leakage mechanism, called Trap Assisted Tunneling (TAT). The TAT leakage current density is modeled as an extension of the SRH mechanism [29] as shown in eq. 2.14. When the crystalline layers contain defects producing traps within E_G, both SRH (involving mid band gap traps) and TAT processes take place. The combined leakage current due to these two mechanism can be described as:

$$J_{SRH+TAT} = \frac{q\, n_i\, W_d}{\tau}(1 + \Gamma) \qquad \text{eq. 2.14}$$

where Γ is the TAT enhancement factor [104] that is mainly dependent on the electric field inside the junction. In general, SRH mechanism has strong temperature dependence, while TAT mechanism is essentially controlled by the electric field. Short channels are governed by high fields and hence TAT leakage dominates. In this case, the leakage current can be controlled by manipulating the field inside the channel in addition to reducing the trap density inside the crystal and at the interface of the oxide that is the root cause accommodating such processes.

c) Direct Band Tunneling (BTBT):

BTBT is an important consideration for small E_G materials that gives rise to high off-state leakage. BTBT leakage current is intensely dependent on V_{DD} and therefore imposes limitation on the permissible V_{DD} for the anticipated low static power consumption. When a junction is under a large reverse bias, carriers can tunnel through a sufficiently thin potential barrier induced by large existing fields. In MOSFETs, the BTBT process occurs in the region where the gate and the drain overlap. The current flows due to the tunneling of carriers from conduction band (CB) to the valence band (VB) or vice versa. The process is dependent on the strength of the electric field at the semiconductor/oxide interface, and hence depends on the doping concentration and the difference between V_{DS} and V_G. The standard model of BTBT current [17] [105] is given by eq. 2.15, where a band bending of the E_G is the minimum necessary for BTBT to occur:

$$I_{BTBT} = A'\xi_s \exp\left[\frac{-B\,E_G^{\frac{3}{2}}}{\xi_s}\right] \qquad \text{eq. 2.15}$$

where A', B are constants, ξ_s is the vertical surface electric field at the tunneling point in the gate/drain overlap region, with minimum value required for tunneling occurring when band bending is larger than E_G, expressed as :

$$\xi_s = \frac{V_{DG} - \frac{E_G}{q}}{z\,T_{ox}} \qquad \text{eq. 2.16}$$

where z is the ratio of semiconductor permittivity to oxide permittivity. With the increase in V_{DD}, impact ionization further amplifies the BTBT current causing even larger leakage current until breakdown takes place. The voltage required to cause BTBT reduces with T_{OX}. Possible solutions lie in reducing ξ_s using lightly doped/undoped regions or enlarging the effective E_G through device scaling. The band-to-band tunneling current (I_{BTBT}) in Ge, InAs, GaAs and InSb can be decreased by over thousand times via scaling [106] where quantum confinement effects diminish BTBT leakage in ultra thin channels due to enlarged E_G by the quantization of sub-bands. Summary of the leakage processes is shown in Fig. 2.7.

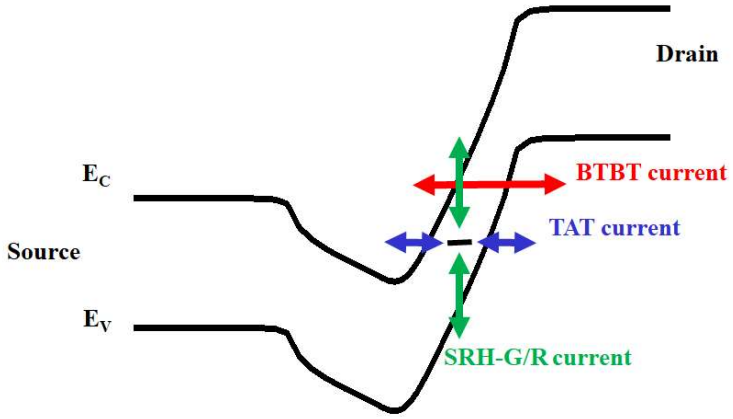


Fig. 2.7 Band diagram of main leakage current mechanisms. Traps in the forbidden band assist SRH and TAT processes. Based on the band bending barrier height and thickness, BTBT processes take place.

d) Parasitic Bipolar Effect :

In vertical GAA structures, this is a non-negligible leakage mechanism, due to lack of conduction path for electrons extraction between channel and substrate (floating body effect). Induced by the BTBT process occurring at the drain side, electron/hole pairs are generated. In the absence of substrate body contact, the electrons pile up and eventually cause the reduction of the energy band barrier, and in turn are injected to the source region where they recombine. At the same time, the holes are injected easier from the source to the drain amplifying the BTBT leakage current. The amplification factor β is calculated as the increase in the drain current ΔI_D with respect to the existing I_{BTBT}. This parasitic effect has been observed in Si [107] and III-V materials [108].

$$\beta = \frac{\Delta I_D}{I_{BTBT}} \qquad \text{eq. 2.17}$$

e) Gate leakage current (on and off state):

Low oxide thickness through aggressively scaled MOS systems accompanied by high electric fields causes quantum tunneling of carriers allowing free flow of carriers through gate oxide to the substrate and vice versa. The mechanism of tunneling can be either Fowler–Nordheim tunneling [17] or direct tunneling [34]. The tunneling probability depends on the barrier height, thickness, and structure. Gate leakage can be inhibited by using large T_{OX} which worsens the control of the gate on the channel by reducing the gate capacitance hence, the high-κ dielectrics were introduced as a solution as discussed previously. Gate oxide leakage affects

the reliability of the device performance and at extreme cases may lead to total loss of transistor operation.

2.4 Material Consideration for PDBFET

Boosting transistor performance can be achieved by enhancing carrier mobility through selecting a high mobility channel material as Ge or by reducing interface scattering and dopant scattering as well. In addition, the scaling process of transistors has already led to the usage of unintentionally doped channels in order to mitigate SCEs and the device variations. Concerning the reduction of scattering techniques, it is interesting to consider the modulated doping of the PDB utilized in PDBFET structure.

While the utilization of Ge material is considered relevant for attaining high I_{on} and low V_{DD} in MOSFETs, nevertheless the Ge-based FETs still have a large room for improvement. Ge has material challenging interface properties as a result of its weak unstable oxide, together with the possible material defects such as threading dislocations and crystal deficiencies owing to the integration on Si. Another challenge resides in the nature of material due to its smaller E_G giving a rise to higher BTBT leakage mechanism. The high dielectric constant making the material more susceptible to SCEs, which might limit device scalability .That is, the low effective mass brings high tunnelling current at relatively high V_{DD}, which may degrade performance in a short channel device. In such case, the increase of the I_{off} may lead to the need of V_{th} tuning/increasing in order to compensate for this degradation, thus negating the main advantage behind using Ge as a channel material. As the PDBFET structure enables the usage of mostly undoped channel, except for a very limited region within the channel introducing a necessary barrier for leakage currents, it is regarded as a good candidate for demonstrating the potential enhancement in performance using Ge as an active channel material. Essentially new materials with higher mobility or alternative device geometries with greater electrostatic control are vital alternatives for further extension of Moore's law. Combining these two techniques is becoming a vital ingredient for improving transistor operation beyond ultimately scaled Si devices.

In this work, I present the design, fabrication, simulation modelling, characterization and performance optimization the of Ge-based vertical p-channel FET integrated on Si using planar doping technique for the first time. The aim of implementation of this is design is to investigate the effect of applying the PDBFET concept to Ge-based FET structure and exploit the advances introduced by the planar doping design and the promising performance of the

PDBFET to the heavily investigated high mobility channel material Ge, which can further improve the Ge-based transistor performance. The main challenges introduced are the high leakage currents, the low interface quality and pronounced SCEs. By applying this design, improved performance for short channel Ge-based FETs is expected. This is the main aim of this thesis.

Chapter 3: Ge-Based P-Channel Vertical PDBFET Device Fabrication, Processing and Characterization

In this chapter, the realization of Ge-based GAA p-PDBFET is presented. An investigation on the fabrication process is demonstrated, where the devices were build up in two stages. The first step was the growth of the epitaxial layers using MBE, then the second step was the processing procedure of successive etching and deposition steps that pattern the layers to produce the final devices. The devices were then ready for characterization and performance evaluation. The results on the successful fabricated Ge-based PDBFET devices are shown and discussed in detail. Effects of several parameters are then introduced for further analysis and device subsequent improvement.

3.1 Layer Growth of Ge-Based P-PDBFET

The design of the Ge-based p-PDBFET structure is vertical, which eliminates dependence on lithography resolution complications for the L_{CH} dimension. However, it requires the grown layers to be of high doping profile precision and good crystalline quality to avoid high leakage currents and degraded performance. In this work, MBE epitaxial growth system was used to produce the semiconductor layers, which enabled the growth of high crystal quality with reproducible doping profiles. In addition, MBE technique is able to achieve sharp abrupt dopant concentrations varying orders of magnitude within few nanometres by allowing deposition at low T_{sub} with atomic monolayer growing precision using in-situ analysis.

Growth was performed with a 6-inch MBE system in which group-IV materials Si, Ge carbon (C) and tin (Sn) are used as matrix materials. In this work, Si as a substrate material on which Ge is integrated were used. Si, Ge and Sn were to be used within the structure design accordingly. As p-type and n-type dopants, B and antimony (Sb) are used, respectively, within the devices under consideration. For real time monitoring, residual gas analyser and pyrometer with 950 nm and 470 nm wavelengths are used. Low temperature measurements are made using infrared camera where T_{Sub} represents the most critical parameter. The p-PDBFET devices layers were grown on 4-inch Si (001) wafers, p-type doped with a sheet resistance R_{sh} = 10-20 Ω-cm.

Since these devices are integrated on Si, the fabrication process started with the thermal desorption of a Si wafer at 900 °C in order to remove the native oxide [109]. The growth process started with a Si buffer layer of 50 nm thickness to reduce the surface roughness, resulting from the thermal desorption step and get a smooth crystalline surface. Subsequently, a 400 nm p-type doped Si layer was grown with doping concentration $N_A = 1x10^{20}$ cm^{-3} as drain layer (bottom contact) at T_{Sub} of 600 °C. A germanium virtual substrate (Ge–VS) layer of p-type doping was then introduced for the subsequent growth of high quality relaxed Ge layers. Since Ge has around ~ 4.2 % lattice mismatch with Si, Ge experiences compressive strain when grown directly on Si. The pseudomorphic growth (epitaxial growth of strained Ge that is dislocation-free) is only limited to a certain critical thickness after which dislocations begins to form in order to release the strain. The relaxation continues until Ge layer reaches its lattice constant. The formed misfit dislocations represents defect density in the crystal. The Ge–VS used in this structure was with thickness of 100 nm, that was p-type doped with $N_A = 1x10^{20}$ cm^{-3} at T_{Sub} = 330 °C. The VS was then annealed at this point for 5 min at T_{Sub} = 850 °C in order to reduce the threading dislocation defects density that was estimated to be in the order of 10^8 cm^{-2} (from Transmission-Electron-Microscopy) for Ge integrated on Si wafers and achieve strain relaxation [110]. The actual Ge-based p-PDBFET structure was then grown at T = 330 °C on top of the Ge–VS with layer thickness of 100 nm of B-doped Ge (drain region) and doping concentration $N_A = 5x10^{19}$ cm^{-3}. The channel growth then started by depositing the first intrinsic Ge layer i-Ge with thickness = T_i at T_{Sub} = 330 °C. The subsequent layer, the δ-doped region, is the most crucial growth step in the fabrication of the p-PDBFET structure. In this step, before the growth of the Sb-doped Ge δ-layer, the growth process was stopped and temperature was ramped down to T_{Sub} = 160 °C. At this temperature the Sb segregation (S) was kept as low as possible at a ratio of S = 10 [111] [112]. The nominal Sb-doping of this layer N_D was varied accordingly in this work. Afterwards, the growth of the second intrinsic layer of the Ge channel with thickness T_i was carried out, while ramping the substrate temperature up back to T_{Sub} = 330 °C. Then a layer of 100 nm thickness of B-doped Ge heavily doped layer acting as the source layer was grown with $N_A = 5x10^{19}$ cm^{-3}. Finally, a highly B-doped Si layer of $N_A = 1x10^{20}$ cm^{-3} and thickness of 100 nm was deposited at temperature of T_{Sub} = 400 °C (to be used as top contact) to facilitate low-ohmic aluminum (Al) contacts. During the MBE process, growth were kept below 400 °C for all Ge layers except for the VS in order to obtain sharp doping profiles. Within this chapter, the nominal doping concentration N_D and the δ-layer thickness d were varied together with the intrinsic layer thickness of T_i in order to set a basis for the first working Ge-based p-PDBFET devices, discover the optimum doping scheme and

evaluate the device performance. The growth scheme is shown in Fig. 3.1(a) and the resulting grown layers are shown in Fig. 3.1(b).

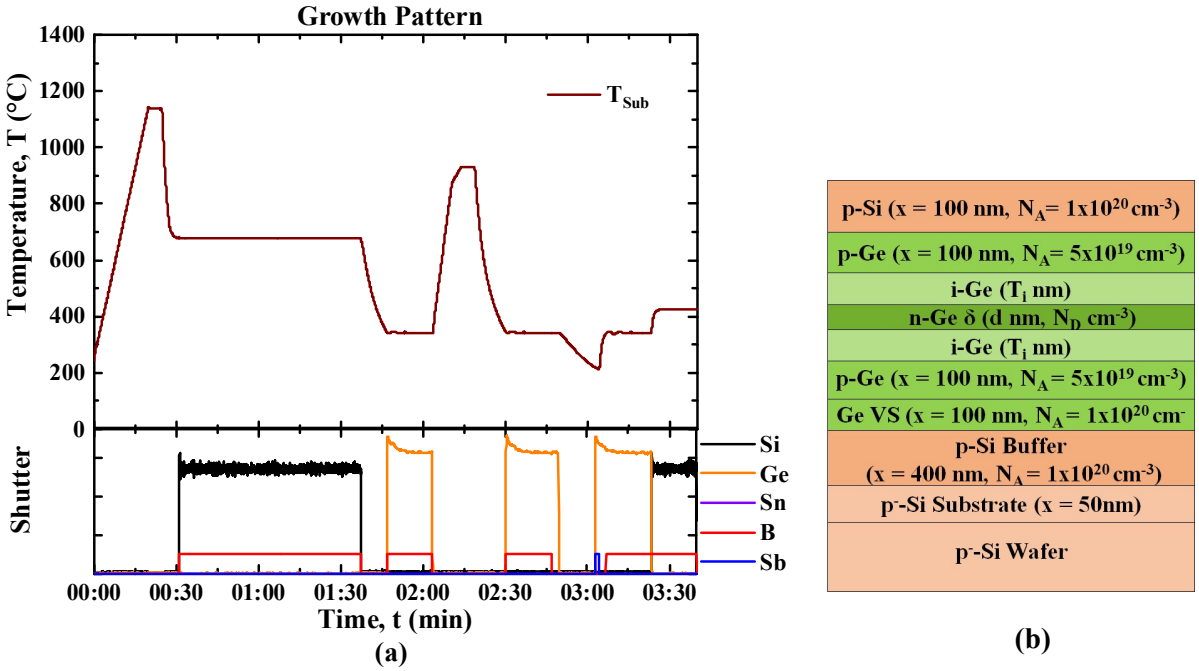


Fig. 3.1(a) Temperature growth scheme of the p-PDBFET layers, (b) the p-PDBFET created layer stack.

3.2 Gate-All-Around Ge-Based P-PDBFET Device Processing

After the fabrication of MBE layers of the p-PDBFET, the processing of the structures started. Samples of 35 mm x 35 mm were produced from the manufactured 4-inch wafers. Experiments were then applied to these samples accordingly. The basic process steps were developed at IHT of University of Stuttgart and was applied to tunnelling FET device structure. This work is involved with the design and the application of this process to produce GAA Ge-based p-PDBFETs for the first time and the development of this process to achieve highly performing novel designed Ge-based Nano-MOSFET devices. The processing masks produces GAA structures (with the gate fully wrapping around the mesa structures, nevertheless full depletion of the channel is not achieved due to relatively large device size). The mesa structures are symmetric of either square mesa with dimension width (L_{Mesa}) or circular mesa with diameter (D_{Mesa}) respectively ranging from L_{Mesa}, D_{Mesa} = 1µm up to L_{Mesa}, D_{Mesa} = 10 µm.

3.2.1 Mesa Structuring

The processing of the p-PDBFET devices started with the cleaning procedure of the samples to remove any organic contamination using ultrasonic acetone (C_3H_6O) and iso-propanol (C_3H_8O) baths for 11 min and 3 min respectively. The second step was to pattern the mesa structures using lithography process followed by anisotropic dry etching process using inductive coupled plasma-reactive ion etching (ICP-RIE). The etching process was done by using chlorine (Cl_2) and hydrogen bromide (HBr) gases. Fig. 3.2 shows the different fabrication stages, starting with the mesa structure formation step in Fig. 3.2(a). The mesa height ranged from 540 nm to 620 nm according to the respective L_{CH}. This height ensured that the mesa is etched down to the Si bottom layer. If the etching process ends at Ge surface, this results in a highly rough surface varying with 50 – 100 nm leading to poor isolation between the gate and the drain due to the gate-substrate overlap. That can cause high leakage current especially at smaller T_{OX} and at severe cases may lead to complete loss of the transistor operation.

3.2.2 Gate Formation

The next step, is one of the most crucial steps in the manufacturing of the FET, which is to prepare the surface of the mesa for gate oxide deposition by a suitable surface treatment. As mentioned previously, Ge has a very challenging interface quality with oxide and needs a lot of attention that is why it is heavily under study. In this process, mainly the surface treatment was done through two stages. First, a preparatory cleaning stage where the samples were immersed in ultrasonic bath containing C_3H_6O then C_3H_8O as previously mentioned to dissolve organics on the surface and then rinsed in deionized (DI) water removing native oxide GeO_2. This is followed by a 45 sec dip step in hydrogen peroxide (H_2O_2) of 30% concentration diluted in DI (of portion 50 to 50 %) to chemically oxidized the Ge surface with fresh oxide. Afterwards samples were dipped in DI water to dissolve the GeO_2 that is soluble in water. This removes approximately 20 – 30 nm of the Ge surfaces in order to obtain a clean surface for gate oxide deposition. This step is also useful because it is selective to Ge only, hence the Si layer serving as top contact is unaffected whereas the beneath Ge layer is slightly etched. This in turn acts as a recessed region that helps to protect the gate metal layer surrounding the mesa during further etching step to free the top of the mesa from the gate metal [113]. The final surface treatment step then involved using an HF dip of 1 min duration with concentration $HF:H_2O = 1:40$. Here the HF is employed for etching the surface for oxide removal and hydrogen termination (or passivation as reported by some studies) [114].

The samples were immediately placed in plasma-enhanced atomic layer deposition (PE-ALD) after surface treatment for gate oxide deposition. The gate oxide used in this work is aluminum oxide (Al_2O_3). The deposition process utilizes trimethylaluminum (TMA) and oxygen O_2 plasma as precursors. Thickness of T_{OX} ~ 13 nm – 16 nm corresponding to 100 deposition cycles were used in this work. A PPO step using O_2 plasma (discussed in details in Chapter 4) was used with duration t = 7 min after 15 ALD cycles then the rest of the cycles was resumed. In general, one cycle of ALD consists of several phases [115] including; TMA gas pulse during which interaction with the surface takes place in a self-limiting process followed by argon (Ar) gas pulse as a purging step to remove residues and gaseous by-products of the TMA interaction. Then O_2 plasma pulse is introduced where O_2 radicals react with the surface in a self-limiting reaction and finally initial conditions are re-established by evacuating and purging the chamber. The relative permittivity of Al_2O_3 extracted in IHT labs within the range of ϵ_r = 6 – 7.7. A high T_{OX} of 13 nm to 16 nm (EOT = 7 nm – 9 nm) was required because in this design it was used as the main basis of isolation between the gate contact region and the bottom contact region that is acting as the drain in this design. The overlap between the gate contact region and the drain region must be well isolated or it can induce high leakage currents or even can cause complete loss of device operation. The existence of non-negligible surface roughness due to the dry etching procedure limits the aggressive scaling of the T_{OX} possible to be achieved in our lab, which can reach T_{OX} = 3 – 5 nm. The succeeding step was to instantly deposit the gate metal which is done through sputtering process. The gate metal used is Al with layer thickness of 400 nm. A second lithography step was then used to pattern the gate geometry. The gate formation was then done by using ICP-RIE etcher (Fig. 3.2 (b)).

3.2.3 Planarization , Passivation and Contact Formation

A planarization step was then applied to free the top of the mesa from the deposited gate metal and allow top contact formation to the source region. This step was done by applying spin-on glass polymer (70-F) coating and baking it at 200 °C for 2 min, then performing a reactive ion etching (RIE) step to etch back the polymer to uncover the top of the mesa metal layer for around ~ 200 nm. O_2 gas was used for the etching process. Afterwards, dry etching of the exposed Al on top with ICP-RIE was carried out followed by a wet etching step using phosphoric acid (HP_3O_4) at 40 °C for thorough removal of any excess metal remaining. Fig. 3.2(c) shows the metal free top of the mesa. Hereafter, a passivation layer of silicon oxide was deposited at 250 °C, using tetraethyl orthosilicate (TEOS) liquid as a source of Si, forming 300

nm oxide thickness by means of plasma enhanced chemical vapour deposition (PECVD). A third lithography step was then used to pattern the oxide window opening necessary for contact formation. The oxide was then dry etched by means of RIE procedure using trifluoromethane (CHF_3) gas. The underlying gate oxide layer of Al_2O_3 acts as an etch stopper. Then a wet etching process using buffered hydrofluoric acid (BHF) dip was performed for 30 – 45 sec to remove the underlying Al_2O_3 layer from contact areas, controlled by microscopic examination (Fig. 3.2(d)). An Al sputtering step was then done to form the top and bottom contacts, with Al layer of 1.4 µm thickness. The deposition was preceded by a 10 sec dip in HF solution of 2.5% concentration to free the surface of the contact from any native oxide. A final fourth lithography step was then made to pattern the contacts geometry (Fig. 3.2(e)). Fig 3.2(f) show a complete view of the final fabricated devices.

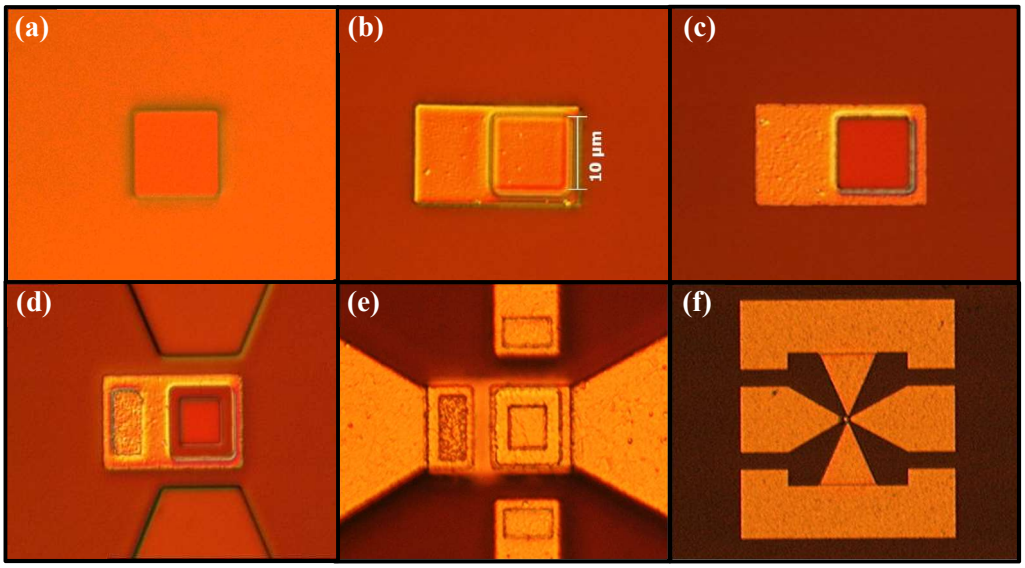


Fig. 3.2(a – f) The different stages of fabrication process of transistor with A = 10 μm^2 captured by microscopy with magnification x100 : (a) mesa structure etching, (b) gate geometry formation, (c) free mesa top of gate metal, (d) oxide window opening, (e) contact formation and (f) top view of the complete fabricated device with magnification x20.

For a closer look on the fabricated devices, an SEM (Scanning Electron Microscope) image is shown for the cross-section of a fully fabricated device (Fig. 3.3). The thicknesses of the different layers are highlighted for illustration, which might be slightly quantitatively different from the values mentioned in discussion, due to the tilting of the device while producing the images.

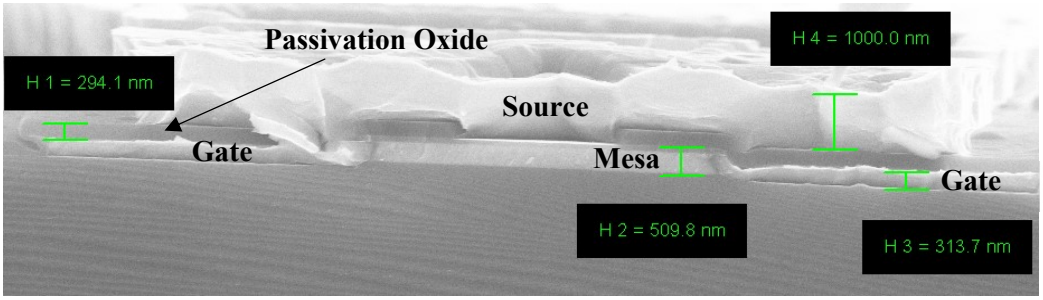


Fig. 3.3 SEM cross-section of the fabricated device layers.

A summary for the fabrication process is demonstrated in Fig. 3.4 highlighting the main stages of the manufacturing process. A schematic structure of the final device is illustrated in Fig. 3.5. Electrical measurements of IV characteristics were performed using Keithley 4200 characterization system. For the structures under consideration, to compare the devices performance, the quantities I_{on}, I_{off} and SS (defined at the steepest point of the transfer characteristics) will be mainly considered accordingly. Due to some design technology limitations discussed above, the scaling down of the T_{OX} of the p-PDBFET structures was restricted, and hence high gate bias was required to switch the transistors into the on-state compared to V_{DS} used. The on-gate bias was therefore chosen based the onset of device operation together with monitoring of the oxide leakage current. So according to the differences in oxide thickness obtained within different experiments, the on-gate bias varied consequently.

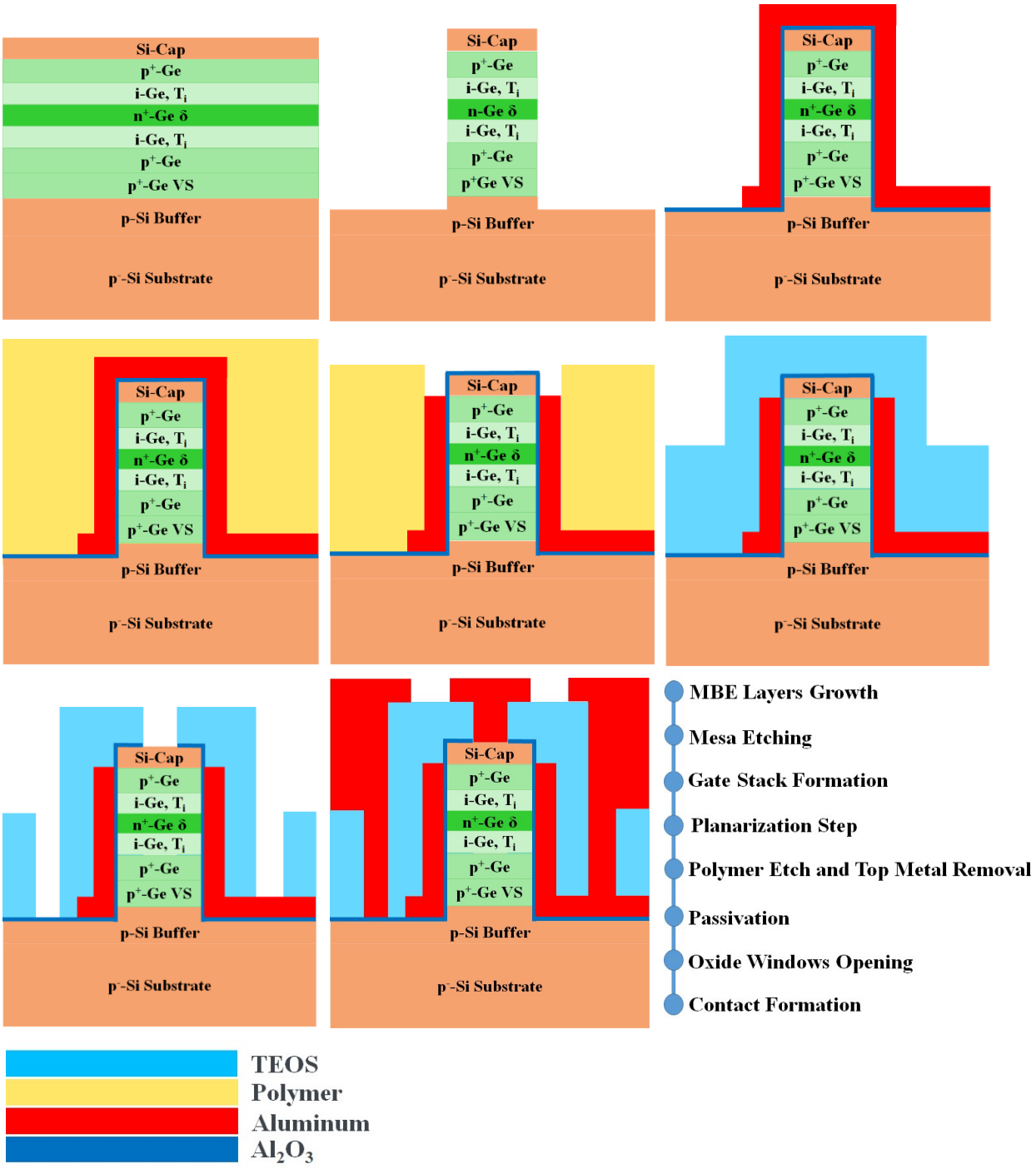


Fig. 3.4 Summary of the steps of the fabrication process of the devices.

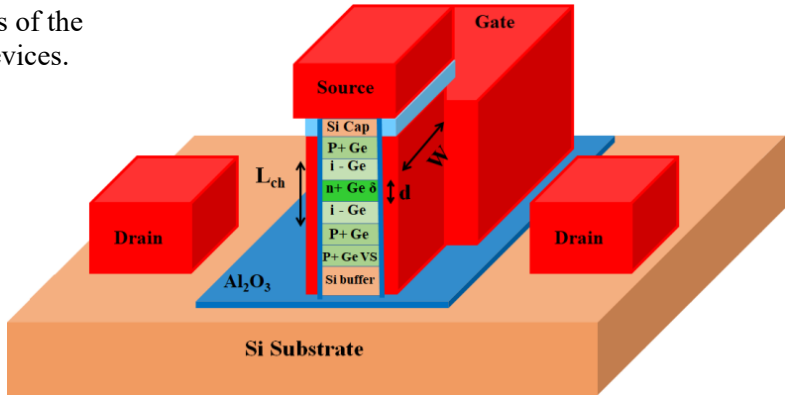


Fig. 3.5 Schematic view of the fully fabricated device.

3.3 Electrical Characterization of Fabricated Ge-Based Vertical P-PBDFETs

Results on the first successful fabrication of Ge-based p-PDBFET devices are shown in this section. Followed by experiments on design parameters variations to show the effect on the performance and how it is possible to further improve the device behaviour.

3.3.1 Effect of δ-Doping Profile

The main aim of this experiment is to set a basis for the design of most crucial layer in the p-PDBFET, which is the scheme of the δ-doping profile for the Ge-based p-PDBFET devices. The fabricated transistors were chosen to be of L_{CH} = 40 nm according to the state of the art of the Ge-based FETs. The aim was to design the optimum δ-layer doping concentration and thickness. So a set of samples with different N_D and fixed d according to Table 3.1 were fabricated. Another parameter is also investigated in addition, where the d was varied according to Table 3.2, while keeping N_D fixed i.e. the doping dose (Q) was varied. N_D chosen values were relatively higher than those used for Si-based PDBFETs in literature, due to the nature of Ge with its smaller E_G and higher I_{off}.

Table 3.1 MBE grown layer structure with different δ-doping concentration for Ge-Based p-PDBFET.

		Sample A	**Sample B**	**Sample C**		
Layer	Material	Doping cm^{-3}	Doping cm^{-3}	Doping cm^{-3}	Thickness nm	Growth Temperature °C
Source contact	Si	$N_A = 1x10^{20}$			100	400
Source	Ge	$N_A = 5x10^{19}$			100	330
Channel	Ge	-	-	-	16	330
Channel	Ge	$N_D = 5\ x10^{19}$	$N_D = 1\ x10^{20}$	$N_D = 2\ x10^{20}$	8	160
Channel	Ge	-	-	-	16	330
Drain	Ge	$N_A = 5x10^{19}$			100	330
Drain	Ge VS	$N_A = 1x10^{20}$			100	330
Drain Contact	Si	$N_A = 1x10^{20}$			100	600

Table 3.2 MBE grown layer structure with different δ-doping layer thickness for Ge-based p-PDBFET.

		Sample C	**Sample D**		
Layer	Material	Thickness nm	Thickness nm	Doping cm^{-3}	Growth Temperature °C
Source contact	Si	100		$N_A = 1x10^{20}$	400
Source	Ge	100		$N_A = 5x10^{19}$	330
Channel	Ge	16	18.5	-	330
Channel	Ge	8	3	$N_D = 2\ x10^{20}$	160
Channel	Ge	16	18.5	-	330
Drain	Ge	100		$N_A = 5x10^{19}$	330
Drain	Ge VS	100		$N_A = 1x10^{20}$	330
Drain Contact	Si	100		$N_A = 1x10^{20}$	600

Transfer characteristics measurements illustration from the different samples are shown in Fig. 3.6(a). A summary for comparing the parameters between the different samples behaviour is shown in Table 3.3. The sample with the lowest doping concentration N_D Sample A has the highest I_{on} and highest I_{off}, which is expected due to having relatively the lowest barrier height. This is also in accordance with having the lowest threshold value (roughly estimated) V_{th} ~ -0.35 V. Sample B with the intermediate barrier height had the best performance among all the samples with a barrier high enough to minimize I_{off} and yet low enough to allow for relatively high I_{on}. Consequently, this sample also has the best SS and V_{th} ~ -0.75 V. The highest doped Sample C had a very low I_{on}, with almost no actual turn on for the device. This indicates the exaggerated barrier height introduced to the carriers. At the same time, I_{off} is not the minimum current as expected, indicating the contribution of a high component of leakage current. This can be due to the dominance of tunnelling mechanisms of TAT and BTBT that were raised due to the extremely high doping concentration of the δ-layer and a poor interface quality with the oxide at the δ-layer region. Hence, an optimum intermediate doping concentration exists that maximizes the available I_{on}/I_{off} for the device.

Considering the effect of thickness of the δ-layer on the performance, the results show that the reduction of d improved the poor performance compared to highest doped Sample C, yet remains with inferior performance related to Sample B. In Fig. 3.6(b) the statistical measurement of all of the samples for the I_{on} for all the available devices' sizes (minimum achievable dimension L_{min} = 2 µm in this experiment) are shown. With Sample A having the highest I_{on} ~10^{-5} A/µm and Sample C the lowest with I_{on} ~10^{-7} A/µm, as discussed above. Normalized to the W, the I_{on} is expected to be independent of the device dimensions. However, the devices show a slight improvement in the I_{on} with reducing the mesa size in Sample A, similar effect in Sample B, but less pronounced, and further in Sample D and finally almost non existing in Sample C. The reason for this can be due to size reduction, the gate electrostatic control is improved and hence higher I_{on} is achieved. With higher N_D, a higher barrier exists and hence the improvement in I_{on} is tougher. For Sample C, with hardly any switching on behaviour the size has no effect.

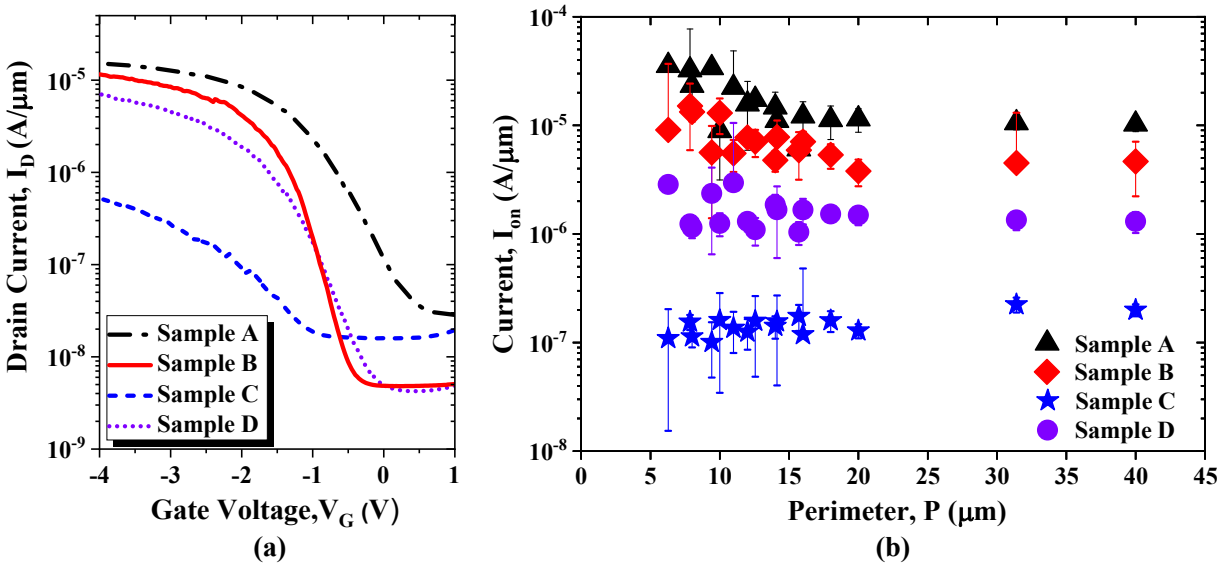


Fig. 3.6(a) Transfer characteristics of Samples A-D and (b) statistical measurements of the I_{on} for the different Samples A-D.

Table 3.3 Main parameter results for different Samples A-D.

Parameter	Sample A	Sample B	Sample C	Sample D
I_{on} (-3V)	1.3x10^{-5}	8.5x10^{-6}	2.7x10^{-7}	4.6x10^{-6}
V_{th} (V)	-0.35	-0.75	-1.5	-0.95
Best Point SS (mV/dec)	467	306	749	411
I_{off} (1V)	2.8 x10^{-8}	5 x10^{-9}	2 x10^{-8}	4.9 x10^{-9}

Statistical measurements of the I_{off} is shown in Fig. 3.7(a-d) as a function of the mesa area (A). Normalized to W, we see that the I_{off} scales efficiently with A. This shows that a considerable contribution to the leakage current comes from the bulk. This emphasizes that further scaling down of the device would be very effective to improve the device performance. Additionally, improvement of the grown crystal quality by upgrading the growth recipe, would similarly lead to reduced bulk trap density inclusion within the device and hence supressed leakage currents are also achieved.

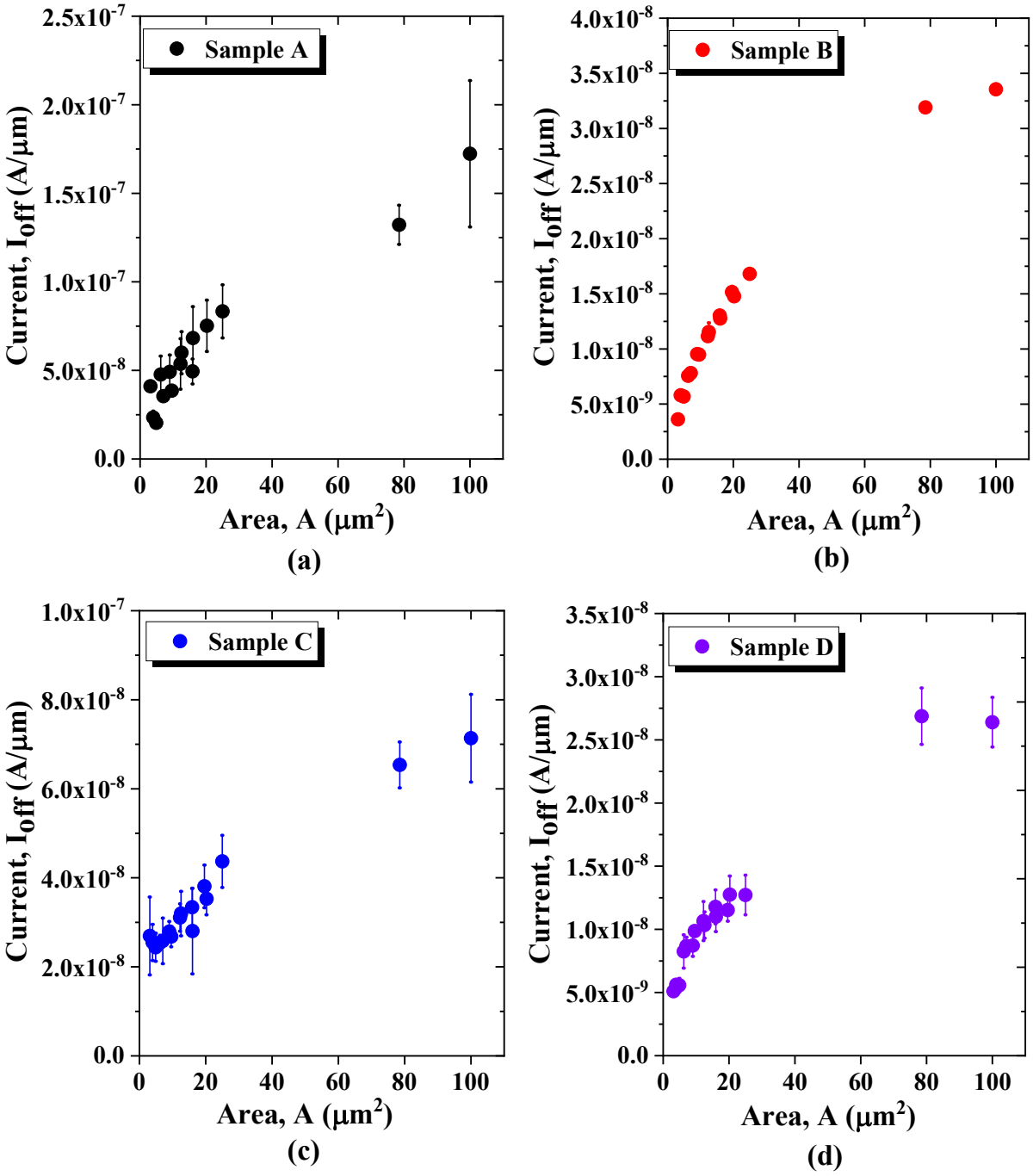


Fig. 3.7(a-d) I_{off} as a function of the device size for different Samples (A-D).

The output characteristics results in Fig. 3.8(a-d) supports that Sample B had the best performance, for all the ranges of V_{DS}. The results show two main encounters in the performance. First, it is obvious that the family of curves meet at relatively high V_{DS} indicating loss of gate control over the I_D at high V_{DS}. Also the non-saturating behaviour that appears clearly in the linear plot as shown in Fig. 3.9 (a-b). This might rise because of impact ionization behaviour due to high fields or tunnelling leakage currents that result from defects (TAT) or due to the small E_G (BTBT). Sample B shows a slightly better performance compared to sample D at low V_{DS}.

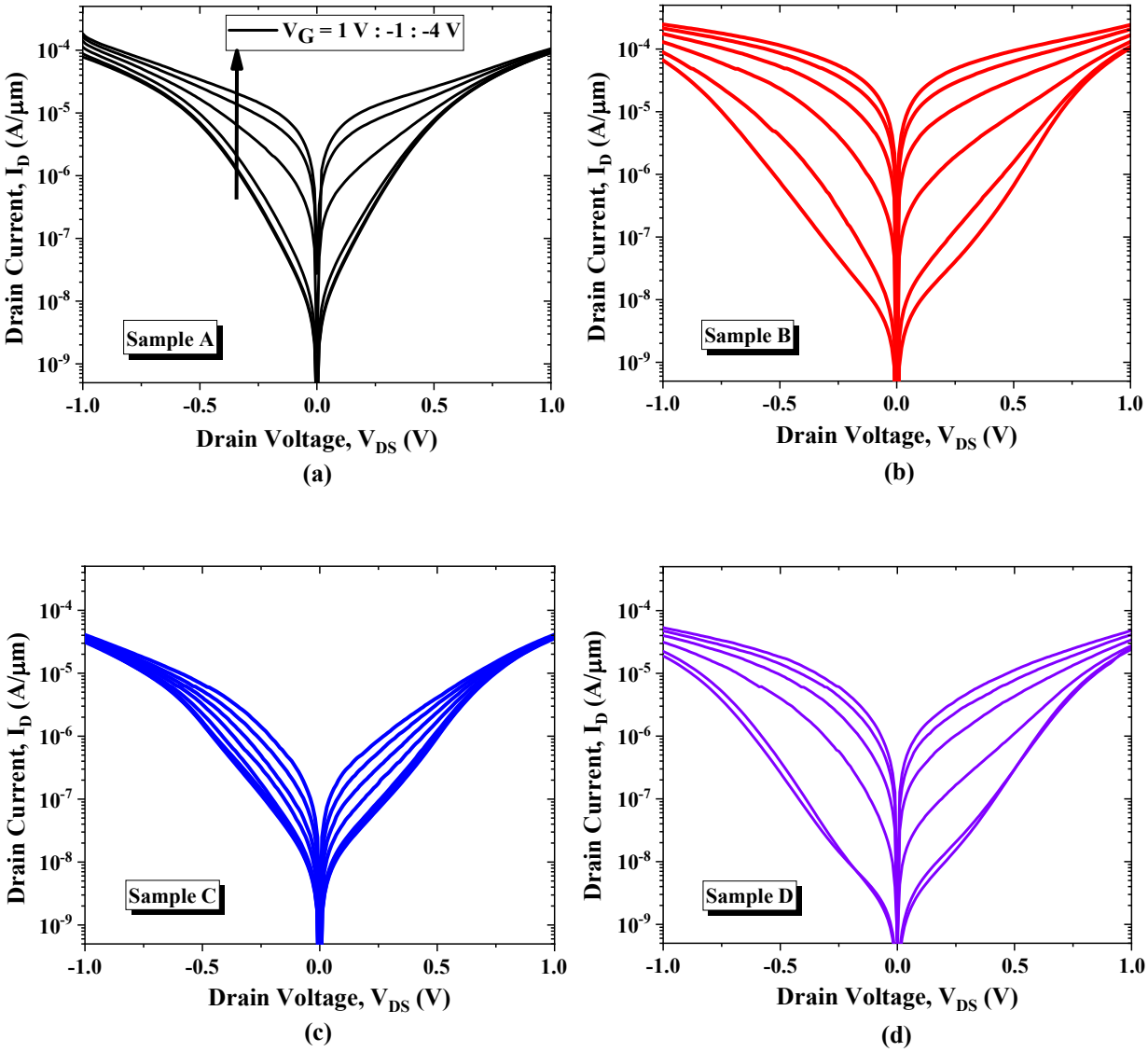


Fig. 3.8(a-d) Output characteristics for different Samples (A-D).

The influence of V_{DS} is an important indication for the SCEs behaviour on L_{CH} = 40 nm (Fig. 3.10). Sample A shows a reasonable I_{on}/I_{off} at V_{DS} = -50 mV and V_{DS} = -100 mV of three

orders of magnitude, but dramatically deteriorates when V_{DS} is elevated to -500 mV to only one order of magnitude which is not adequate for transistor operation.

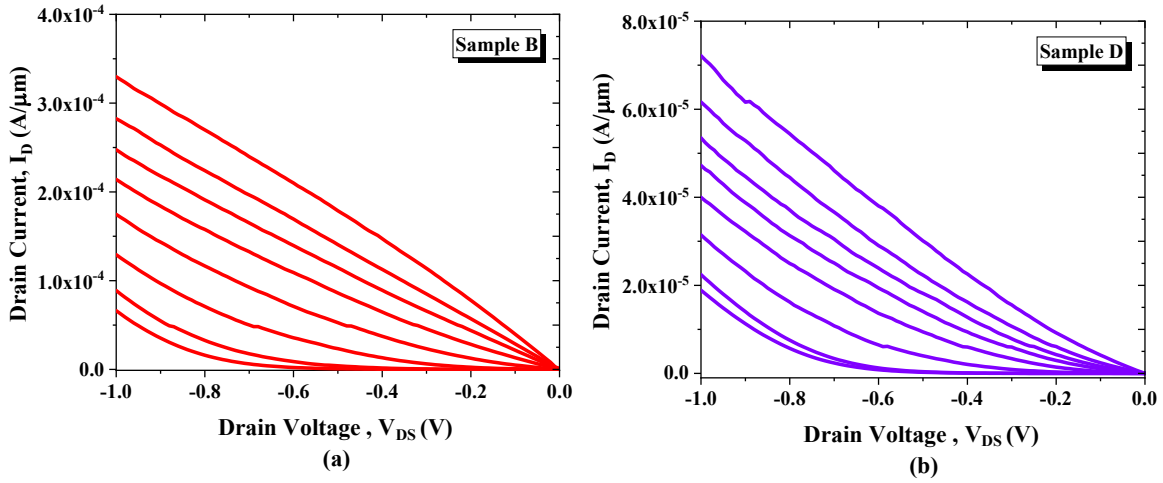


Fig. 3.9(a-b) Linear output characteristics for Samples B and D.

Sample B also shows similar behaviour at relatively low V_{DS}, but at V_{DS} = -500 mV, I_{on}/I_{off} is only reduced to two orders of magnitude indicating higher gate controlled barrier. Sample C is expected to have an inferior performance both at low and high V_{DS}. Sample D shows a lower I_{on}/I_{off} even compared to Sample A, that might result from its high barrier that inhibits high I_{on} to flow regardless how high V_G is, leading to an overall lower I_{on}/I_{off}.

The SS, defined as the steepest point in the transfer characteristics, is shown in Fig. 3.11. Devices of Sample B exhibited the lowest SS, ranging between SS = 300-350 mV/dec for EOT = 7 nm which is quite a good range for such relatively high T_{OX}. The state of the art for the oxide thickness is T_{OX} < 1.5 nm, which is expected to highly improve the SS performance. Due to limitation by the process, the T_{OX} was restricted to such high value.

3.3.2 δ-layer Position Influence on the Performance

Using the results of the previous experiment, as concluded, that the doping scheme of Sample B is the optimum doping with best performance among all the other samples, hence for the coming sections it was used as the standard profile scheme with δ-layer of d = 8nm and N_D = 1x10^{20} cm^{-3}.

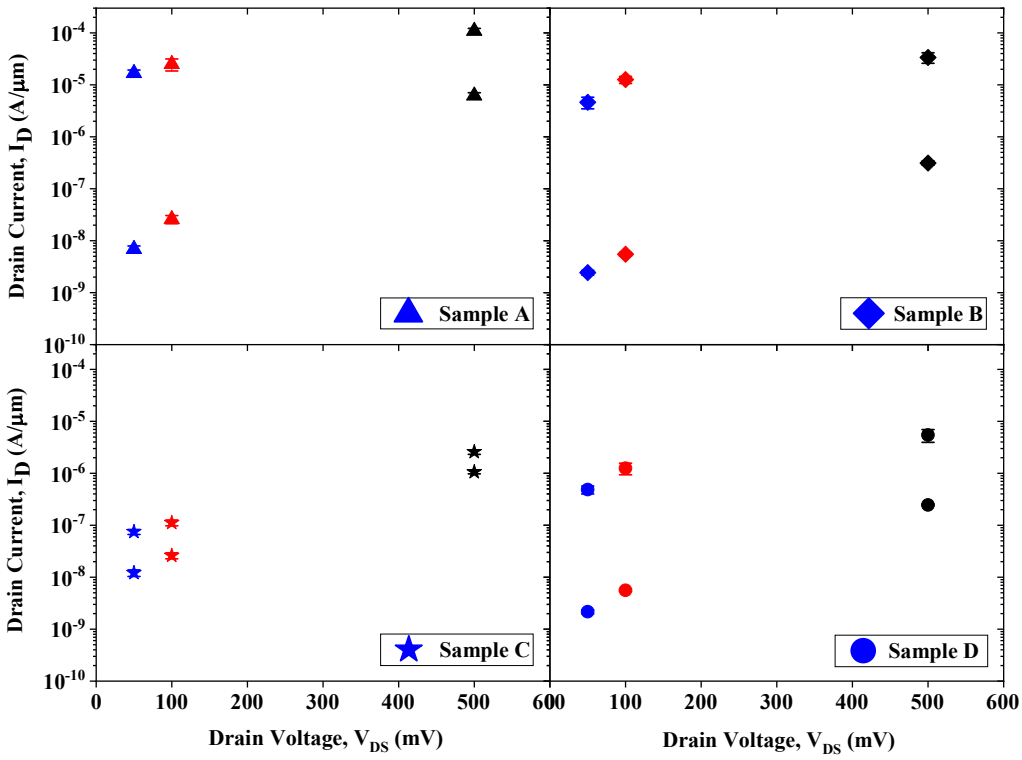


Fig. 3.10 Demonstration of the effect of the V_{DS} on the I_{on}/I_{off}.

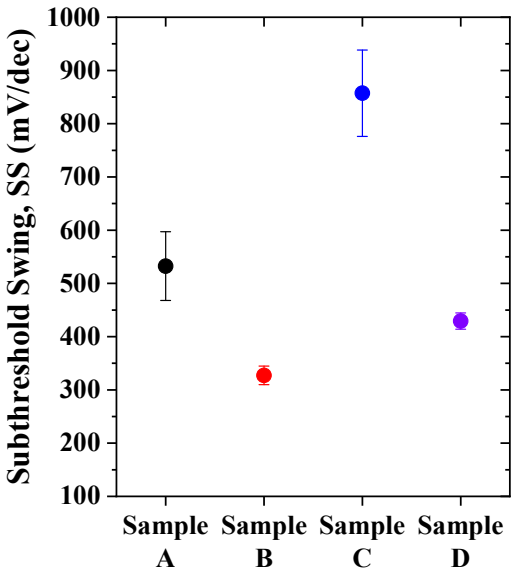


Fig. 3.11 SS mean values for different doping concentrations and doses.

For further investigation on the performance analysis, the next experiment performed was to study the efficiency of the barrier created within the channel. The design parameter was the position of the δ-layer, representing the barrier position, within the channel. The samples were designed as follows, Sample E with the centre of the δ-layer exactly in the middle of the channel (Fig. 3.12(a)). Sample F with centre of the δ-layer relocated at 14 nm from the edge of

the source region (Fig. 3.12(b)) and Sample G with centre of the δ-layer at 9 nm from the edge of the source region (Fig. 3.12(c)). Table 3.4 summarizes the MBE grown layers for the different samples highlighting the δ-layer positions. As in Si-PDBFETs, it is expected to see the influence in the output characteristics [88] where the δ-layer affects the saturation behaviour according to its position with respect to source and drain. When the δ-layer is placed near the source, better saturation behaviour and higher breakdown voltages are obtained whereas when placed near the drain, higher saturation currents are achieved. For this work, Ge-based p-PDBFETs output characteristics are shown in Fig. 3.13(a-f).

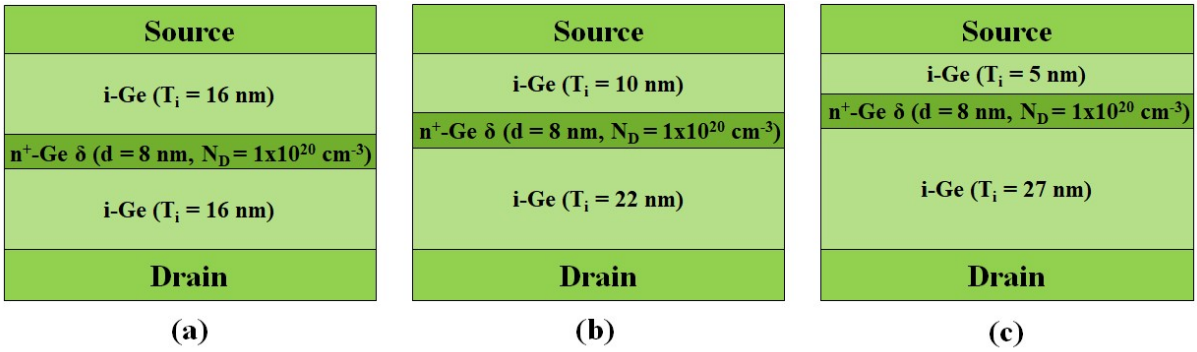


Fig. 3.12 Schematic of the MBE grown layers with different δ-layer positions w.r.t. source, (a) Sample E, (b) Sample F and (c) Sample G.

Table 3.4 MBE grown layers for different δ-layer positions within the p-PDBFET channel.

		Sample E	**Sample F**	**Sample G**		
Layer	Material	Thickness nm	Thickness nm	Thickness nm	Doping cm^{-3}	Growth Temperature °C
Source contact	Si	100			$N_A = 1x10^{20}$	400
Source	Ge	100			$N_A = 5x10^{19}$	330
Channel	Ge	16	10	5	-	330
Channel	Ge	8	8	8	$N_D = 1\ x10^{20}$	160
Channel	Ge	16	22	27	-	330
Drain	Ge	100			$N_A = 5x10^{19}$	330
Drain	Ge VS	100			$N_A = 5x10^{19}$	330
Drain Contact	Si	100			$N_A = 1x10^{20}$	600

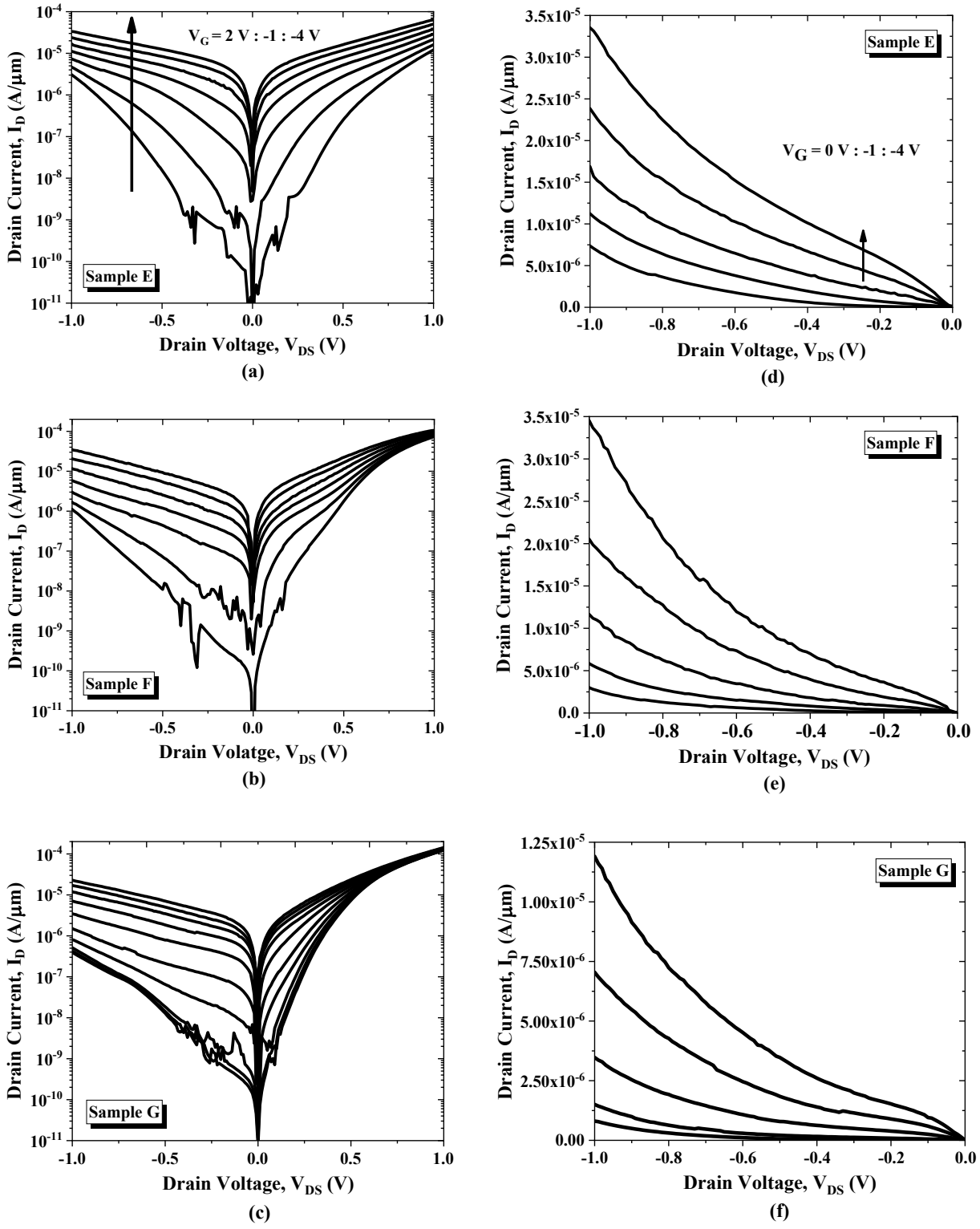


Fig. 3.13 Output characteristics for the different samples with varied δ-layer position, (a) middle position (log scale) , (b) 10 nm from the source (log scale), (c) 5 nm from the source (log scale) and (d-f) same as (a-c) with linear scale.

It is clear from the output characterization that the position of the δ-layer is insignificantly effective, in contradiction to the results of Si-PDBFET previous experiments. Minor variations can be detected concerning saturation behaviour or current values. This indicates the dominance of other parasitic effects that shield the observation of the fine-tuning of barrier position effect. This can be due to several reasons, the effect of highly defective Ge/Oxide interface, problematic MBE grown crystal layers quality with large trap density or SCEs as a result of the challenging L_{CH} of the design.

3.3.3 Study of the Effect of Short Channel Behaviour

Therefore, in order to study the effect of the short channel behaviour, devices with L_{CH} = 120 nm were also fabricated (Sample H) (Table 3.5). The comparison between the long and short channel devices performance is shown in Fig. 3.14(a-d). In this experiment, the achievable minimum feature dimension for the devices of both samples L_{min} = 1 μm, which is half the size of the devices of the previous experiment. By comparing the long and short channel devices behaviour (Fig. 3.14(a-d), the SCEs appeared in three points: (i) the relatively higher I_{off}, (ii) the deteriorated SS and finally (iii) the gate control problem that appears at relatively high V_{DS} in the output characteristics.

Table 3.5 MBE grown layers for 120 nm channel Ge-based p-PDBFET.

		Sample H	
Layer	Material	Doping cm^{-3}	Growth Temperature °C
Source contact	Si	100	400
Source	Ge	100	330
Channel	Ge	46	330
Channel	Ge	8	160
Channel	Ge	46	330
Drain	Ge	100	330
Drain	Ge VS	100	330
Drain Contact	Si	100	600

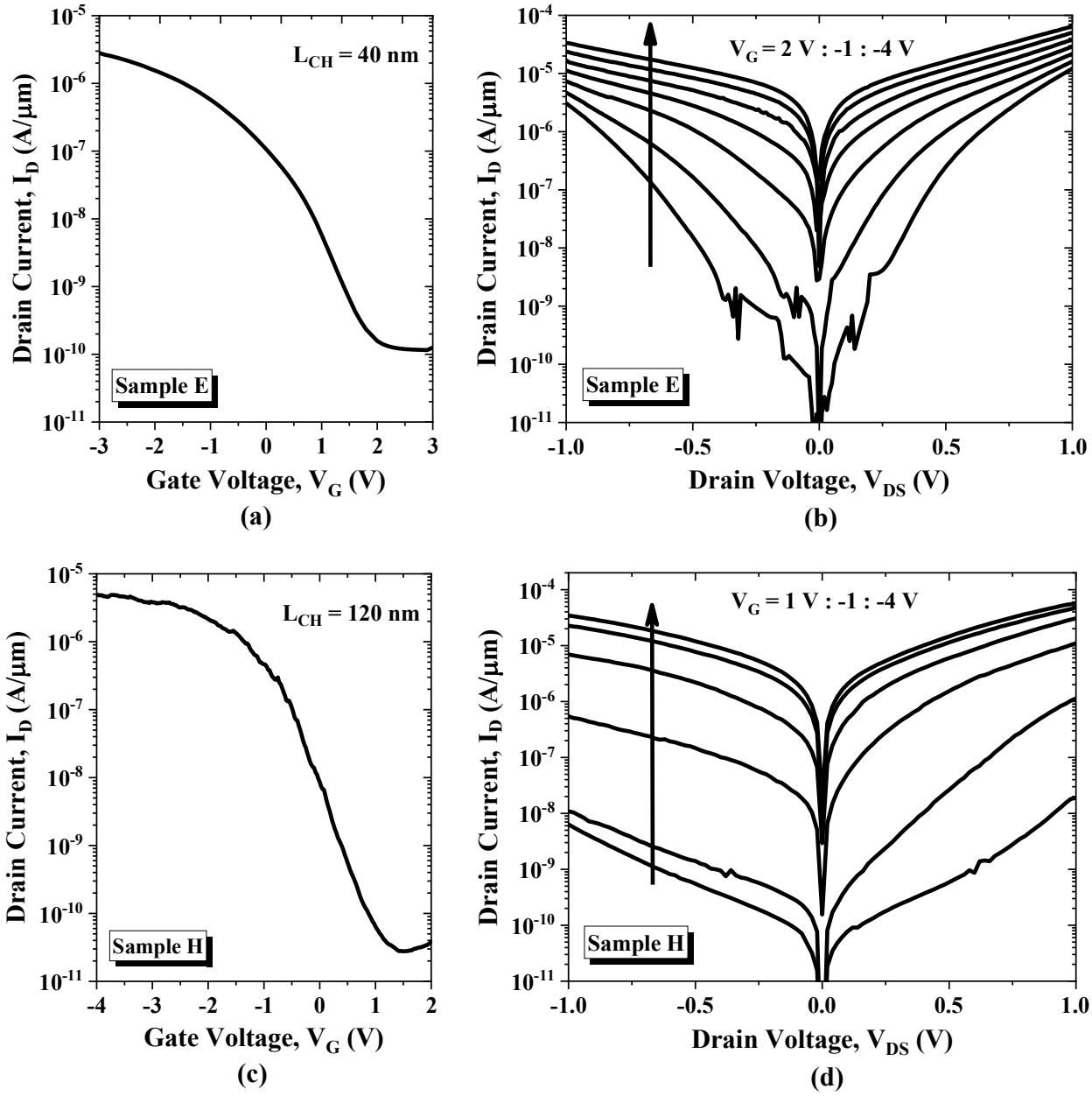


Fig. 3.14 Comparison between behaviour of (a) transfer characteristics of L_{CH} = 40 nm, (b) output characteristics of L_{CH} = 40 nm (c) transfer characteristics of L_{CH} = 120 nm and (d) output characteristics of L_{CH} = 120 nm Ge-based p-PDBFET.

As concluded from the previous experiment, the reduction in size will result in lower I_{off}. The results of the transfer characteristics measurements Fig. 3.14(a) show improvement in the I_{on}/I_{off} of L_{CH} = 40 nm approaching 4 orders of magnitude instead of 3 orders in the last experiment. However, another consequence was observed; the degradation in the SS reaching up to above 500 mV/dec compared to the previous experiment. This can be due to the increase of the influence of surface properties (dry etching surface roughness and prior gate oxide treatment) that in turn starts to limit the performance. Numerical comparison between L_{CH} =

40 nm and L_{CH} = 120 nm samples is shown in Table 3.6. Since the degradation of SS effect did not appear in the long channel L_{CH} = 120 nm, this raised the question whether the SS deterioration in performance can be due to surface tunnelling mechanisms that is highly triggered by shorter channel and higher fields. The results also show that a significant improvement in the gate control at relatively high V_{DS} is obtained in long channel p-PDBFET. This may point towards a contribution from drain-induced barrier lowering (DIBL) effect, however the outcomes from the previous experiment show that placing the barrier efficiently away from the drain is not improving the performance in the L_{CH} = 40 nm devices. Another interesting observation is that the non-saturation behaviour in the L_{CH} = 120 nm output characteristics also existed, urging the need to study the gate interface quality and analyse it.

Table 3.6 Comparison between the short channel and long channel Ge-based p-PDBFET performance.

Parameter	L_{CH} = 40 nm	L_{CH} = 120 nm
I_{on}/I_{off} (-2 to 2V)	$9.9x10^3$	$1.1x10^5$
V_{th} (V)	-0.2	-0.9
SS (mV/dec)	513	301

Before moving to the next experiment, to further investigate surface property influence on performance, inspection of the behaviour of individual devices of Sample E with different performances was made. A comparison between a single high performing (HP) device and average performing (AP) devices with D_{Mesa} = 1 µm was performed. Another device with D_{Mesa} = 3.5 µm of L_{CH} = 40 nm to perceive the size effect as well. Transfer characteristics of the three devices are shown in Fig. 3.15(a). The device with best performing SS (HP device) compared to the average behaviour (AP device) of D_{Mesa} = 1 µm indicates existence of a problem in the interface quality for the average performing device. In turn, a significant difference appears in the output characteristics (Fig. 3.15(b-d)) where gate control performance is improved at high V_{DS}. This proves that the gate control loss is related to surface tunnelling currents due to high trap densities existing at the interface. Comparing the performance of the D_{Mesa} = 1 µm and that of the D_{Mesa} = 3.5 µm , higher I_{off} is detected, showing higher bulk trap density as discussed in previous experiments, which affects the output characteristics behaviour as well at higher drain fields, showing a complete loss of gate control at high V_{DS}. That concludes that the main reason of gate loss control at high V_{DS} in the output characteristics lies in the existence of large concentration of bulk and interface trap densities that raises the TAT leakage current, overpowering the gate controlled I_D of the device.

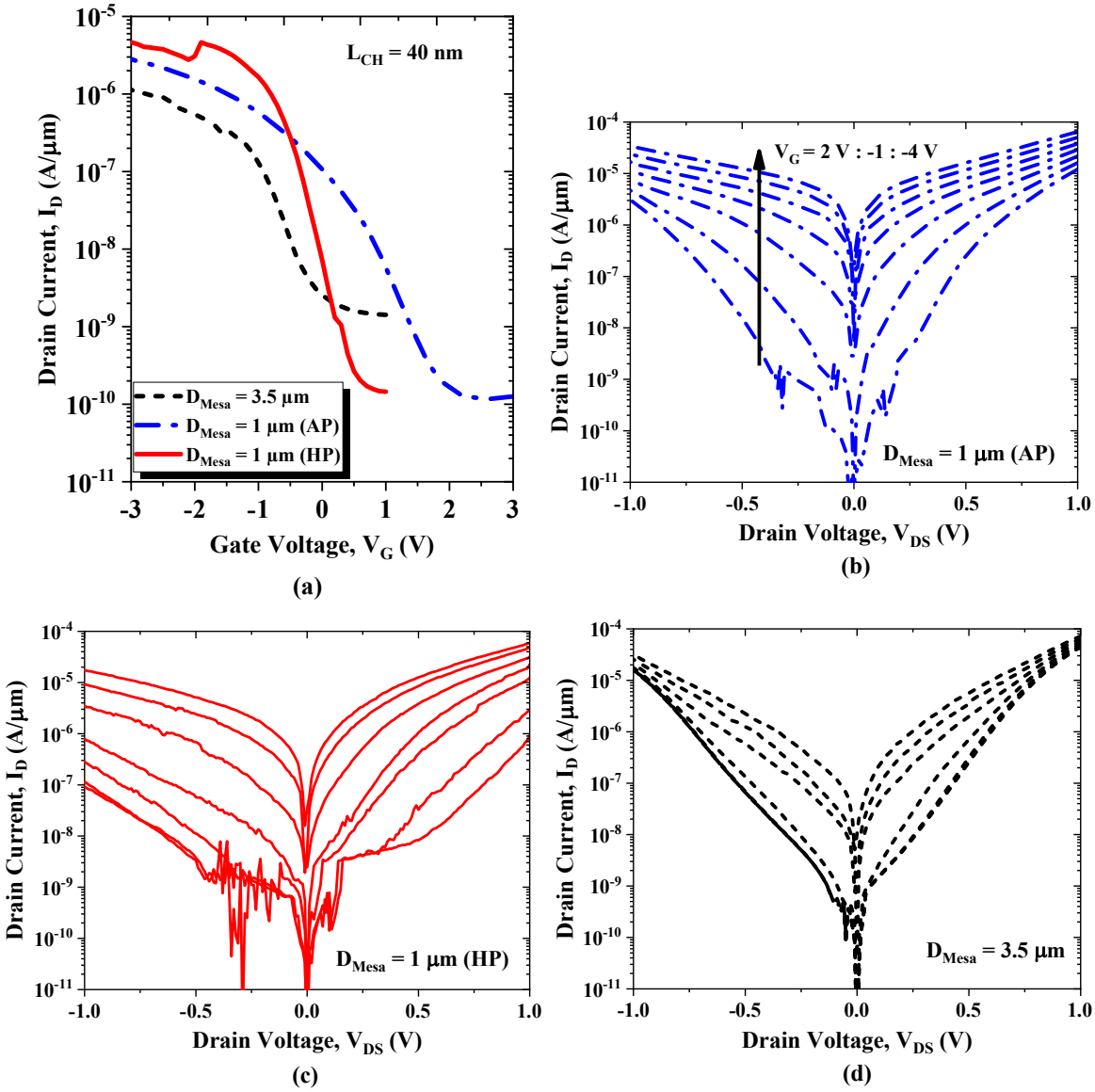


Fig. 3.15 Comparison of the transfer characteristics of the different devices. (a) Average performance device with D_{Mesa}= 1 µm , high performance device with D_{Mesa}= 1µm and larger device with D_{Mesa}= 3.5 µm and (b-d) the corresponding output characteristics respectively.

At this point, it is interesting to start the investigation of the interface quality of the device, by studying the effect of the pre-treatment of the mesa surface prior to the gate oxide deposition on the behaviour of the p-PDBFET.

3.3.2 Impact of Mesa Surface Treatment on Ge-Based P-PDBFET Performance

According to the former findings, an experiment was designed based on MOSCAP devices surface treatment experiments illustrated in Chapter 4. Here, devices with L_{CH} = 120

nm were used to avoid SCEs, with the exact fabrication procedure performed on both samples, except for the varying of the step of surface treatment of the etched mesa directly prior to gate-oxide deposition. In this experiment, two procedures were used; (i) same as explained in section 3.2.1 where the final surface treatment step included using an HF dip of 1 min duration with concentration HF:H_2O = 1:40 to etch the surface for oxide removal and hydrogen termination (Sample I). The second procedure (ii) the HF dip was replaced by surface cleaning using $C_6H_8O_7$ [116] at 90 °C for 30 min with 50 gm/300 ml of DI water, followed by a 10 min dip of HCl [117] with concentration of 32% (Sample J). The usage of high temperature $C_6H_8O_7$ compared to literature was to speed up the chemical reaction and ensure better interaction at the surface. Transfer characteristics are shown in Fig. 3.15(a-b) for comparison.

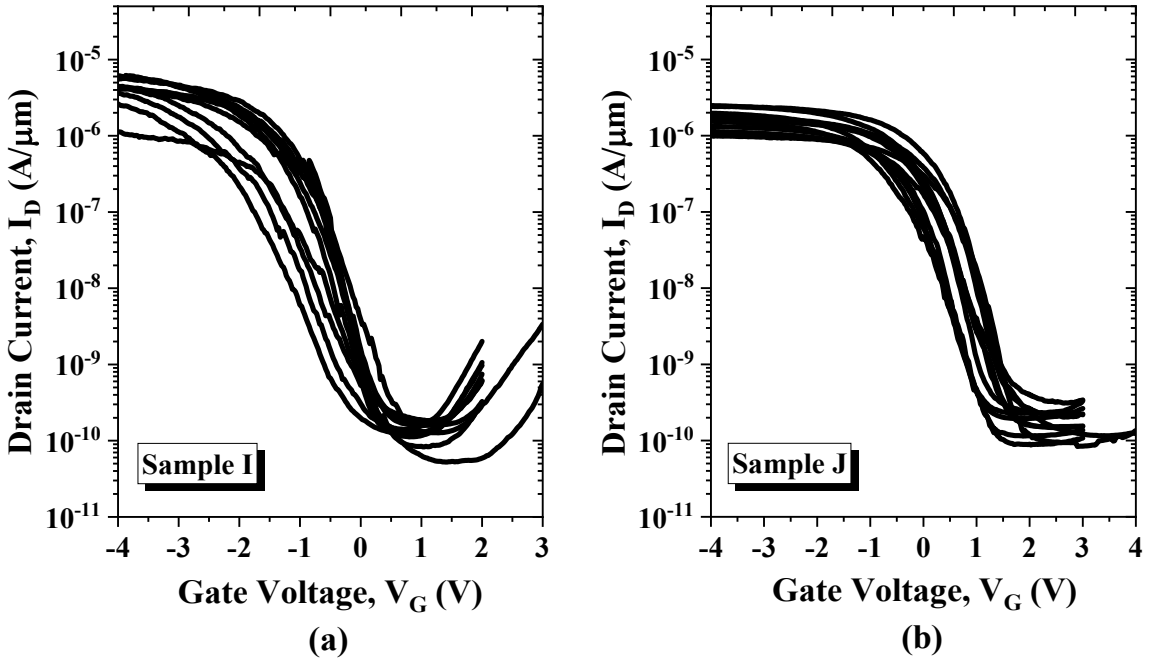


Fig. 3.16 Comparison between behaviour of L_{CH} = 40 nm and L_{CH} = 120 nm Ge-based p-PDBFET.

It is obvious that Sample I with standard HF surface treatment, shows clear gate-induced drain leakage (GIDL) behaviour [118], which is mainly caused by BTBT processes occurring near the drain region. The high field caused by the elevated V_G leads to strong band bending, aided by the depleted region of the drain surface, resulting from the large overlap between the gate and the drain regions in this vertical structure. In addition, the existence of high interface trap density can lead to increasing leakage current as V_G increases in the positive direction as seen in Fig. 3.15(a). On the other hand, Sample J with the modified treatment method shows good control on the leakage current that is independent of V_G, reaching up to V_G = 3 – 4 V, indicating improved surface properties. Meanwhile, Sample I shows on average higher I_{on} than

the average of Sample J, signifying improved surface roughness quality. This may be due to technological reasons resulting from the etching process, or reduced surface roughness quality of HF compared to HCl treatment, which is unlikely to be the reason based on literature results [119] [120]. In general, the modified treatment of the surface indicates a promising potential of performance improvement by further investigations to reduce interface trap density, which in general gives rise to surface leakage currents.

To summarize, in this chapter, the fabrication of GAA Ge-based p-PDBFETs for the first time was presented. The initial device design-parameters were determined, the study of the δ-layer position effect was discussed and the SCEs in those devices were studied. The results indicated that continued device-scaling leads to reduced bulk traps and hence reduced I_{off}. Which similarly can be achieved to some extent by the improvement of the grown crystal quality. Interface states led to inferior SS behaviour, which besides to the bulk trap existence, resulted in loss of gate control on I_D at higher V_{DS} due to TAT leakage current. A non-saturating behaviour in the output characteristics was observed as well, even in long channel devices. Additional examinations on the origins of the existing non-ideal characteristics is necessary.

Chapter 4: Study on Surface Treatment of Ge-MOS-Capacitor on Ge-Virtual Substrate on Si

The MOS-structure is the basic building block of the MOSFET and possessing high quality properties is crucial to construct a successful performing device. In this chapter, the study of the influence of treatment of Ge/Al_2O_3 interface is presented, through fabricating and characterizing Ge-MOSCAP as a method of improvement of the challenging interface properties of Ge/oxide. A quick overview of some of the various current surface treatment techniques used in literature is performed and compared. Then a proposed new surface treatment procedure using a combination of two of the presented techniques is demonstrated, which achieved good performance and proved its potential to produce high quality Ge surface for MOSFET fabrication.

4.1 Importance of Ge/Oxide Interface Study

A key challenge for Ge-based FET devices is the Ge/oxide material structure. The electrical properties of the GeO_2 interface are of inferior quality to that of Si/SiO_2 where GeO_2 is thermally unstable, decomposes into several sub-oxides (GeO_x); possessing high density of dangling bonds (DB), water-soluble and with growth process that is hard to control. This lead to the shelving of Ge with the rise up of the CMOS technology, where Si with its superior native oxide SiO_2 took over and maintained microelectronics industry for decades. By finding similar gate-dielectric interface quality, the advantageous high mobility performance of Ge can be accomplished.

The scaling down of T_{OX} encountered the problem of raised leakage currents due to tunnelling through the oxide. To avoid this problem a thicker physical layer of high-κ dielectric material, compared to SiO_2, can be applied without compromising the gate capacitance of the MOSCAP structure that is a major factor of improving the I_{on} of the device. In general, the gate oxide capacitance is given by:

$$C_{ox} = \frac{\epsilon_o \epsilon_r A}{T_{ox}} \qquad \text{eq. 4.1}$$

where ϵ_o is the vacuum permittivity. The fundamental concept of EOT is a favoured way to evaluate the gate capacitance, calculated by:

$$EOT = \frac{3.9}{\epsilon_{high-\kappa}} T_{ox\_high-\kappa} \qquad \text{eq. 4.2}$$

With the renewed interest for high mobility channel materials in replacement for Si, deposition of high-κ dielectrics on Ge is heavily investigated. The deposition of high-κ dielectrics on Ge is still a challenging process due to GeO_2 weak characteristics. The deposition of high-κ materials directly on Ge results in poor performance [121] due to formation of high density of defects, which is again a major encounter for Ge-based FET devices. The quality of the interface, and hence later the performance, is defined by the interface state density (D_{it}) which represents the number of trapped charges per cm^2 per eV. These defects, specifically the ones near the interface, have severe impact on the channel mobility. The trapped charges in the defect centers scatter the charge carriers leading to degraded mobility and consequently I_{on}. The trap-centers also elevate the leakage currents and causes loss of the gate control on the charge by screening the field leading to degraded performance of SS. Ge/high-κ direct interfaces have relatively much higher D_{it} compared to Si/SiO_2 interface. Typical SiO_2/Si gate stacks have a mid-gap interface state density with value of $D_{it} \sim 2 \times 10^{10}$ cm^{-2} [114], whereas most reported high-κ /Ge gate stacks show $D_{it} \sim 10^{11} - 10^{12}$ cm^{-2} and usually demonstrate significant flat-band voltage (V_{FB}) shift [122] [123]. Unlike SiO_2, high-κ dielectrics have high density of intrinsic defects due to their high coordination number. Such trapping of charges inside the dielectric causes hysteresis effects and the performance of the device becomes unreliable. To address this matter, an interfacial layer (IL) introduced to produce high quality interface with the oxide. This defect density reduction at the interface is usually called surface passivation and hence the layers are called passivating layers [121]. In general, it is essential to separate the channel from the high-κ material as it strongly affects its mobility. Hence, the passivation of the Ge/oxide interface is an essential task in paving the way for Ge-based FETs as a replacement for Si-FETs.

4.2 MOSCAP MBE Layer Growth

It is more convenient to integrate Ge channels on Si, for rather economic production. This integration of Ge on Si introduces an additional challenge, next to encountering Ge/oxide interface properties, which is the lower crystal quality of the grown Ge although a transition

layer of Ge–VS is incorporated. Due to the lattice mismatch - as discussed in Chapter 3 - threading dislocations, propagate from the surface of the Ge–VS to the active Ge device during MBE growth process. This in turn makes the fabrication of high quality devices more challenging.

In this work, Ge integrated on Si was used, where the growth was done using MBE technique. The MOSCAP device layers were grown on 6-inch Si (001) wafers, p+ doped with $R_{sh} < 0.05$ Ω.cm. To ensure a clean substrate surface the wafers were thermally annealed for 5 min at 900 °C as an initial process step. Ge–VS of p-type doping was introduced for consequent growth of improved quality relaxed Ge layers. The Ge–VS is of thickness of 100 nm that is B-doped with $N_A = 1x10^{20}$ cm^{-3} at $T_{Sub} = 330$ °C. The Ge–VS is then annealed at $T_{Sub} = 850$ °C to lower the threading dislocation defects density for Ge integrated on Si and achieve strain full relaxation. Finally, the active intrinsic Ge surface is grown at 160 °C on top of the Ge –VS with layer thickness of 300 nm. The produced wafer is then diced into 9 chips.

4.3 MOSCAP Device Fabrication.

Fabrication of planar Ge/Al_2O_3 – MOS – capacitor started with the surface cleaning and treatment (passivation). All samples were subjected to a cleaning step using ultrasonic C_3H_6O and C_3H_8O baths for 8 and 3 min respectively, to dissolve organics on the surface and then a rinsing step in deionized (DI) water removing native oxide GeO_2. A specific treatment step using wet chemical approach was then applied, varying according the experiment under consideration. That step was followed by the immediate loading of the samples into the PE-ALD chamber to deposit the gate oxide Al_2O_3. The deposition process took place at T = 300 °C. For all samples, deposition of 100 cycles (sequential pulses of TMA and O_2 plasma with intermediate Ar purging intervals) was used. Then instant gate metal formation was done by sputtering process of Al of thickness of 800 nm. To form the backside contact, a 10 sec dip in HF solution of 2.5% concentration was first done to free the surface of the contact from the native oxide SiO_2 prior to the second Al sputtering process on the backside with thickness of 1.4 μm. The patterning of the Al gate electrode was done through a lithography step followed by wet etching process using HP_3O_4 at 40 °C. The fabricated gate electrodes are of area $A = 6.4x10^{-7}$ m^2. The exact method of Ge-cleaning and passivation used for each experiment is discussed in the coming sections in detail. Electrical measurements of the MOSCAP were performed using Keithley 590 CV Analyzer. The backside contact was always at ground potential, while the alternating current (AC) applied signal was of 30 mV amplitude.

4.4 Ge Surface Treatment

Efficient electrical passivation of Ge surface is an essential concern for the prosperous integration of Ge devices. This is crucial because defects including DB at the Ge/dielectric interface are capable of trapping charges and hence affecting severely the performance. The principle of the formation of interfacial layer IL beneath the high-κ dielectric is to decrease the D_{it} through surface passivation. At the same time, the importance of the IL must be carefully balanced with the EOT cost as, in general, the IL material has lower dielectric constant. Therefore the IL thickness should be kept as low as possible (without degrading channel mobility) in order to provide an overall low EOT (0.5 nm as required by international technology roadmap for semiconductors (ITRS)). Therefore, different ILs production methods are currently being investigated, where the pretreatment of wet chemical cleaning influences the IL growth on Ge [124]. Ge surface preparation have a stronger impact on high-κ gate stack quality than on Si [125]. Thus, intensive investigations are needed to be able to understand and control its passivation techniques since its oxide is much less stable than Si, which makes the process very challenging to establish. Wet chemical treatment approach does not involve a lower- κ physical layer in the gate stack, which is desirable for EOT scaling. However, the absence of passivating GeO_2 barrier layer might cause undesirable interface reactions and may lead to direct interaction of the deposited dielectric with the Ge substrate [126]. So the principal aim of the studies of Ge gate stack in general is to achieve low EOT while keeping the high mobility and low leakage.

Numerous efforts have been demonstrated to passivate the interface defects in high-κ/Ge interface structures. First, the usage of wet chemical treatments, where the main objective is to remove completely the defective native oxide from the Ge surface. One of the classical methods to decrease the amount of Ge oxide prior to high-κ film deposition on the Ge substrate is using HF treatment, causing Ge surface hydride-termination [127] or hydrogen passivation (H-passivation) of Ge in analogy to Si surface treatment. The main criterion is to form the oxide (chemically grown) and then etch it through an HF dip step. This step is expected to both etch the oxide then H-passivation process takes place. Most studies agree that HF remove wet chemical oxides yet only few reported complete H-passivation [114]. This can be due to the fact that HF treatment does etch the GeO_2 but leaves the sub-oxides that prevents the full hydrogen termination of the surface [128]. The H-passivation also cannot effectively passivate DB defects [129] that in turn leads to high D_{it} values. Studies also showed that in Ge, H behaves

as an acceptor hence is negatively charged [130]. In turn, it is electrostatically repelled from the DB, and therefore will not be able to successfully passivate it [131]. Alternative passivation approaches are needed for Ge. Another chemical treatment for Ge surface is using HCl for chloride passivation (Cl-passivation) or Chloride-termination [127]. This is mainly done by simply dipping the Ge layer in diluted HCl solution. In contrast to HF, HCl etching results in a Cl terminated surface. HCl reported better results than the conventional HF, where whatever the concentration of the HF does not affect the sub-oxide removal whereas high concentration HCl (20%) removes most of the sub-oxide layer [117] [132] and leaves the surface mostly of mono and di-chloride bonds. In addition, HF treated-Ge-surface is rougher than that treated with HCl [119] [120] [132]. However, HCl treated surfaces passivation efficiency still needs more improvement since it re-oxidizes in the ambient air on the scale of hours [127]. Regarding the problem of remaining sub-oxide residues, concerning the above methods, as well as the re-oxidation of the surface (passivation inefficiency), a recent study has been presented that proposed the usage of $C_6H_8O_7$ solution as means of treatment of the Ge surface [116]. The $C_6H_8O_7$ solutions proved to be effective in the removal of GeO_x. The $C_6H_8O_7$ treated surfaces showed good stability with no oxide growth for 3 days of ambient exposure.

The passivation of the Ge surface through the formation of a physical IL between the Ge and the high-κ material is effective in reducing D_{it} and enhancing the interface properties, especially concerning the mobility performance. However, this comes on the expense of the EOT. Several techniques have been developed among the past two decades. Si passivation is a famous technique where an epitaxial silicon cap layer is used as a direct contact with the dielectric interface, protecting the Ge surface [133] [134] [135]. Nevertheless, this technique has limitations on the appropriate Si cap layer thickness due to the impact of the relatively higher thicknesses on the overall mobility [121]. Another technique is the Ge nitridation or oxynitridation where nitride layers are grown primarily by exposure either to ammonia gas or plasma [136] [137] [138] or using thermal growth of germanium oxynitride (GeO_xN_y) by means of ozone-oxidation and subsequent nitridation anneals [139] [140]. The nitride (or oxynitride) layer effectively prevents Ge oxidation and Ge diffusion into high-κ dielectrics. A third method to introduce passivation effect to the Ge surface is sulfur (S) passivation (S-passivation). The S-termination can be obtained using aqueous ammonium sulfide $(NH4)_2S$ [132] [141], or by S deposition through hydrogen sulfide (H_2S) adsorption. Recent studies also introduced the technique of solid-state reactions involving exposure to S-vapour at high substrate temperatures and near atmospheric pressure [142]. Experiments showed that S-termination well passivates the interface and is considered as a promising method [132] [141] [143]. In the previous

methods, absence of the GeO_2 on the Ge surface has been the main goal. Another interesting technique is, "GeO_2-passivation", where this method investigates the oxidation of the Ge surface to act as a passivation layer used as a very thin IL to improve the characteristics of the surface. "GeO_2-passivation" can be produced by a wide variety of oxidation methods including thermal oxidation [144] [145], high-pressure oxidation [146], ozone, molecular or atomic oxygen exposure [147] and different plasma techniques [148] [149] [150] [151] [152]. An interesting technique is the PPO [149] [153] [154] [155]. In this procedure, the Al_2O_3 is deposited prior to the plasma oxidation, then the GeO_x at the Al_2O_3/Ge interface is grown. Consequently, the GeO_x is confined from the beginning where Al_2O_3 acts as a diffusion barrier controlling the thickness of the GeO_x IL where the greatest challenge of the GeO_2 IL approach is controlling (i) the thickness of the oxide, and (ii) the diffusion of Ge into high-k material [121].

In this chapter, results of electrical characterizations of Ge/ Al_2O_3/Al MOSCAP of three different main experiments are presented. First, an experiment comparing the performance of the Ge-MOSCAP with/without PPO technique. The second experiment shows a comparison between different wet chemical etching/passivation treatments for the Ge-MOSCAP surface. Finally, an experiment introducing a proposal for a new surface treatment, combining one conventional and another nonconventional cleaning steps, that demonstrated a promising performance.

4.5 Ge-MOSCAP with/without Plasma Post Oxidation

In this investigation, the effect of PPO step is introduced. In this fabrication process, the treatment step prior to loading the samples to the PE-ALD machine is a 1 min HF dip of 2.5% followed by DI water cleaning to remove the chemical residues and remaining oxide. One sample S1 had regular growth using100 cycles of PE-ALD. The other sample S2 had 15 successive deposition cycles under the above mentioned conditions, allowing for the deposition of T_{OX} = 1.5-2 nm of Al_2O_3 that act as a protective layer for the consecutive step. Then the cycles are paused and plasma oxidation process takes place at RF power of 100 W at 300 °C. A flow of O_2 with 17 sccm and Ar with 10 sccm is applied within the same chamber, where the IL layer is kept protected. Then finally, the rest of the 100 cycles are performed to continue the deposition of the full gate oxide layer of Al_2O_3.

CV characteristics at f = 300 KHz with dual sweep measurement of the samples using a step bias of 25 mV are shown in Fig 4.1(a). The calculated C_{ox} corresponds to $\epsilon_r \sim 7.7$, and measured thickness of Al_2O_3, using ellipsometry measurement of Al_2O_3 deposited simultaneously on Si-reference sample, is T_{OX} = 8.3 nm for S1 and T_{OX} = 9.6 nm for S2 (T_{OX} of sample P is overestimated to some extent where the GeO_x IL is not accounted for). High frequency behaviour is detected in Fig. 4.1, with a hump appearing in the depletion/weak inversion region. This is a characteristic behaviour for interface trap response [156]. On the other hand, part of this behaviour can be also attributed to the minority carrier response [157] [158] as a result of the high n_i and the small E_G of Ge [159]. There is a slight improvement in the saturation behaviour at the accumulation region for S2, indicating improved gate control due to lower D_{it}. A clear shift in V_{FB}, reducing its absolute value is also observed; the CV curve shift is towards the positive V_G lowering the V_{FB} indicating lower effective positive charges (Q_{eff}) that can be at the interface or within the oxide. It can indicate a relatively oxygen rich (O-rich) Al_2O_3 oxide [160] that could be induced by the PPO treatment. In addition, the voltage hysteresis (ΔV_H) (calculated at (C_{max}+ C_{min})/2) is reduced from ΔV_H = 350 mV to ΔV_H = 200 mV, which demonstrates less contribution of trapped charges inside the oxide. The capacitance ratio C_{max}/C_{min} is a useful parameter that indicates the efficiency of the gate control and its ability to accumulate and deplete the charges. It is clear that the PPO treatment improved the performance with its higher C_{max}/C_{min}. In order to be able to demonstrate the effect on the interface traps, an estimation for D_{it} was calculated for both samples Fig. 4.1(b), where the conductance method was applied [161]. This might not be very accurate for high mobility materials since it cannot provide quantitative estimates of the D_{it} for interfaces with large D_{it} [156] where the used C_{ox} in this work is quite smaller than the qD_{it} product and hence C_{ox} dominates and D_{it} might be underestimated. Another concern is that the extracted D_{it} on Ge at RT would be over estimating D_{it} since the interaction of interface traps occurs with majority and minority carriers [159]. Hence, here it is applied only as a means for comparison between the two samples rather than reporting actual interface state density value. The evaluation of D_{it} according to equation 4.3 [161]:

$$D_{it} = \frac{2.5}{qA}\left(\frac{G_p}{\omega}\right)_{max} \qquad \text{eq. 4.3}$$

Where, G_p is the parallel conductance given by equation 4.4, and ω is the angular frequency.

$$G_p = \frac{\omega^2 C_{ox}{}^2 G_m}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \qquad \text{eq. 4.4}$$

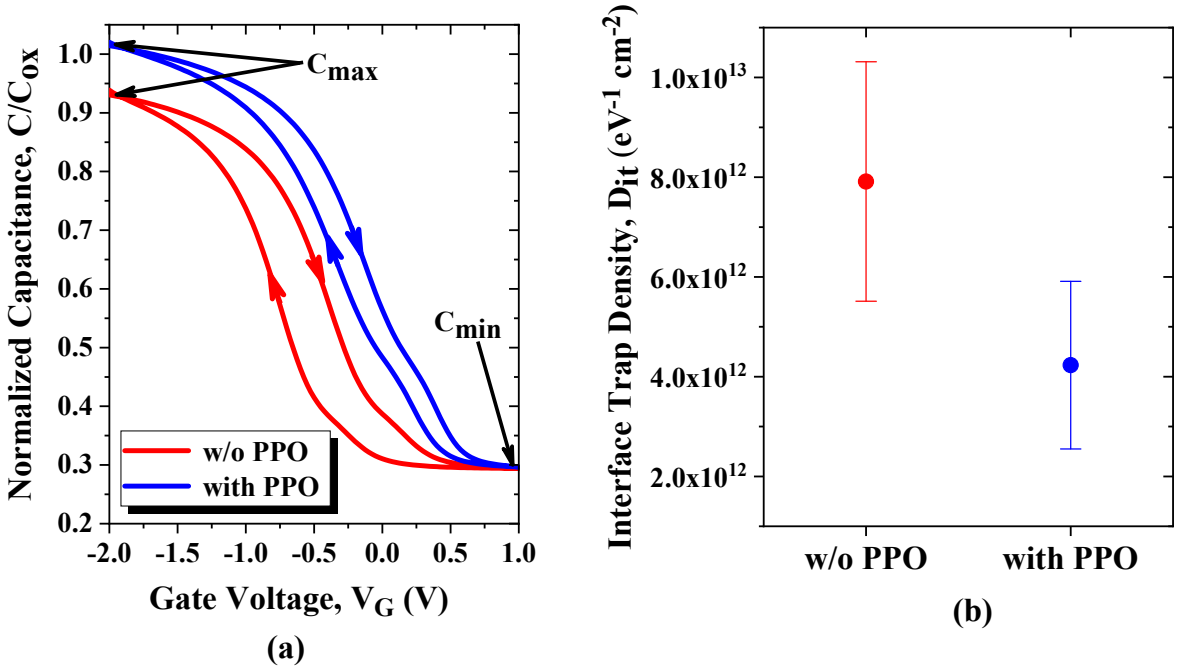


Fig. 4.1(a) Measured CV characteristics of Ge-based MOSCAPs for samples with and without applying PPO and (b) the average estimation of the corresponding D_{it} for each sample.

Clearly, the PPO has improved the CV characteristics of the Ge-MOSCAP where the O_2 plasma is expected to produce an IL layer of GeO_x that passivates the surface and reduces the interface traps enhancing the overall performance of the device. The conductance method is suitable for quantifying the D_{it} when the conductance (G) is governed by the majority carrier response [157] however the small E_G of Ge allows the interaction of both minority and majority carriers where carrier generation is a thermal activated process that can be suppressed by lowering the temperature [159]. Hence for further accurate estimation of D_{it} values, experiment can be performed at low temperature (~ 80 K) [162] to avoid overestimation of the D_{it}. Moreover, for more precise values, T_{OX} could be reduced to our facility limit at IHT of value ~ 3 nm, to maximize C_{ox} to be comparable to the qD_{it} product.

4.6 Chemical Surface Treatments Comparison: HF, HCl and $C_6H_8O_7$ with Sulfite Passivation

In general, a certain quantity of GeO_x ($x < 2$) remains even after the wet chemical treatment. In this context, solutions including an oxidizing agent, such as H_2O_2, are used to oxidize insoluble GeO_x into soluble GeO_2. It is used as a step to effectively etch the surface by the oxidation of Ge by H_2O_2, followed by dissolving the oxide product in the aqueous solution [163]. In this experiment, we include this step in the pretreatment process. This removes around 20-30 nm of the Ge surfaces in order to obtain a clean surface before further passivation steps. Three different samples were prepared combining different wet chemicals for etching and passivation purposes. Since the main aim is to explore alternative passivation strategies than H-termination for Ge, in the coming experiment, three different techniques are used for comparison. All three samples S3, S4 and S5 were all dipped in H_2O_2 (30%) solution (50% mixture with water) for 20 sec and then rinsed with pure DI. Afterwards, the first sample S3 was dipped in HCl solution of 32% for 10 min for passivation (Cl-termination). Meanwhile the second sample S4 was etched with HF (2.5%) dip for 1 min then it was placed in ammonium sulfite $(NH_4)_2SO_3$ of 35% for 5 min at 60 °C for passivation of the surface. It is worth mentioning that this is a different chemical solution composition than the frequently used $(NH_4)_2S$. This solution was used for its abundance compatibility within the cleanroom allowing for immediate successive oxide deposition. The final sample S5 was cleaned in $C_6H_8O_7$ with concentration of 50 gm per 300 ml solution at 90°C for 3 min then was dipped in $(NH_4)_2SO_3$ performing same passivation step as S4. All samples where scheduled for treatment simultaneously and then immediately placed in the PE-ALD chamber for Al_2O_3 deposition. Fig. 4.2(a) demonstrates the CV characteristics behaviour of the samples measured at f = 500 KHz. S4 and S5 have almost the same performance except for a slight difference in hysteresis performance, whereas for S6 with $C_6H_8O_7$ and $(NH_4)_2SO_3$ treatment has improved some characteristics. The calculated hysteresis for the different samples are $\Delta V_{H\text{-}S4}$ = 350 mV, $\Delta V_{H\text{-}S5}$ = 300 mV, $\Delta V_{H\text{-}S6}$ = 300 mV, indicating that the S-passivation causes slightly lower hysteresis. There is a clear enhancement in the saturation behaviour of "S6" and the C_{max}/C_{min} is relatively higher. The impact of the $C_6H_8O_7$ treatment in comparison of the classical HF treatment before S-passivation is clear in this case. On the other hand, the $C_6H_8O_7$ caused a shift in the V_{FB} causing it to have a positive value. This indicates that equivalent negative Q_{eff} exists at the interface. Further investigation is still required to study the effect of $(NH_4)_2SO_3$ rather than $(NH_4)_2S$ as a source of S-passivation of the Ge surface. The abnormal observation here is

that the measured accumulation capacitance (C_{acc}) is larger than the calculated C_{ox}, which is not possible. This may result from overestimation of T_{OX} or inaccurate refractive index of the oxide n_{ox}. Another explanation is the existence of parasitic capacitance $C_{Parasitic}$ that adds up to the measured capacitance. An estimation for D_{it} for the samples was done through calculating G_p then extracting the corresponding D_{it} only for comparison of the performance. Fig. 4.2(b-d) shows the equivalent G_p versus f plots for the three samples at different V_G. When plotted as $\frac{G_p}{\omega}$ versus f on a log scale, this contribution forms a function with a peak f that corresponds to the majority carrier capture time constant [164], and the integrated area is proportional to the interface state density. The local maximum of each curve indicates the magnitude of the corresponding D_{it} using eq. 7.3. S3 shows relatively higher but quite similar behaviour $\frac{G_p}{\omega}$ curves compared to S4. Comparing S4 and S5, the $C_6H_8O_7$ has slightly reduced the trap density compared to the HF treatment. An interesting observation is that the peak value occurrence frequency have been significantly shifted to higher frequencies, from around 2 $x10^4$ Hz up to$1x10^5$ Hz different trap levels are activated. For further investigation, CV characteristics at different frequencies were investigated as well (Fig. 4.3 (a-c). Two observations in behaviour are detected. First, for S4, it demonstrates minimum frequency dispersion in the depletion region compared to the other two samples, which contradicts the conductance method where the curves showed relatively higher D_{it}. Second, the low frequency response behaviour started considerably earlier in S5 (below 200 KHz) in comparison to S3 and S4 (below 50 KHz). This behaviour depends on minority carrier response (generation and recombination lifetime). Associated with the frequency dispersion in the depletion region, an unexpected frequency dispersion behaviour was detected in the accumulation. In general, frequency dispersion in the accumulation region, as a result of the effect of series resistance (R_S), leads to the decrease of the measured C_{acc} with the increase in the applied frequency [165] [166]. In these samples, the frequency dispersion detected was opposite, i.e. the measured C_{acc} increases with the increase in the applied frequency. This proves the existence of certain $C_{Parasitic}$ that adds up to the measured capacitance leading to such behaviour and also causing the C_{acc} to be higher than C_{ox} for those samples. A simplified model for this case is shown in Fig. 4.3(d). As a step for verification of the analysis, further comparison was made by performing CV measurements at a large range of frequencies for MOSCAP samples fabricated on Si and on Ge–VS substrate. The unusual behaviour appeared in the Ge–VS only, but not on the Si samples (Fig. 4.4(a-b)). This indicates that C_{ox} used in G_p calculations was overestimated in this experiment.

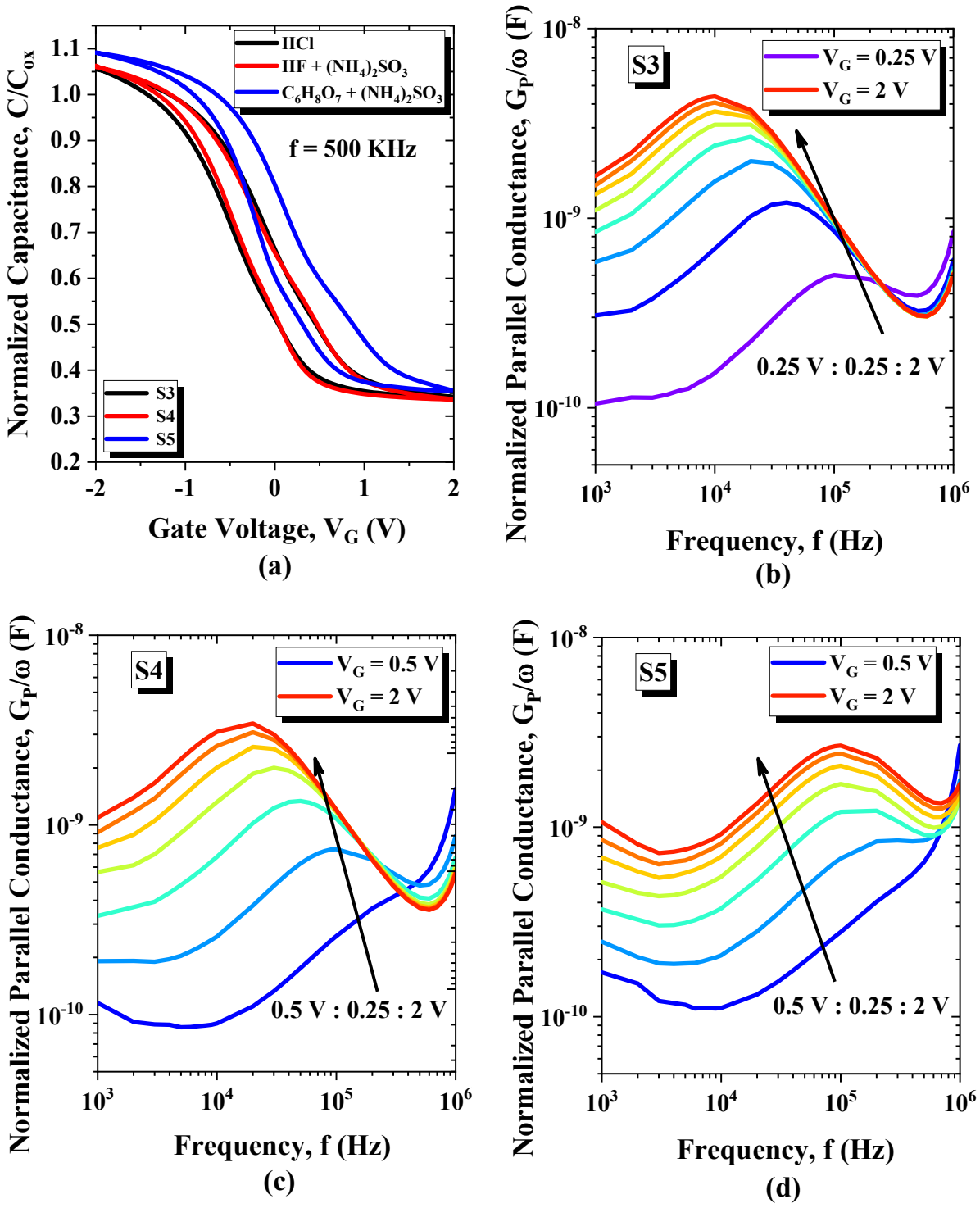


Fig. 4.2(a) CV characteristics of Ge-based MOSCAP at 500 KHz for samples S3, S4 and S5 and (b-d) frequency dependence of $\frac{G_p}{\omega}$ at different V_G for the three samples.

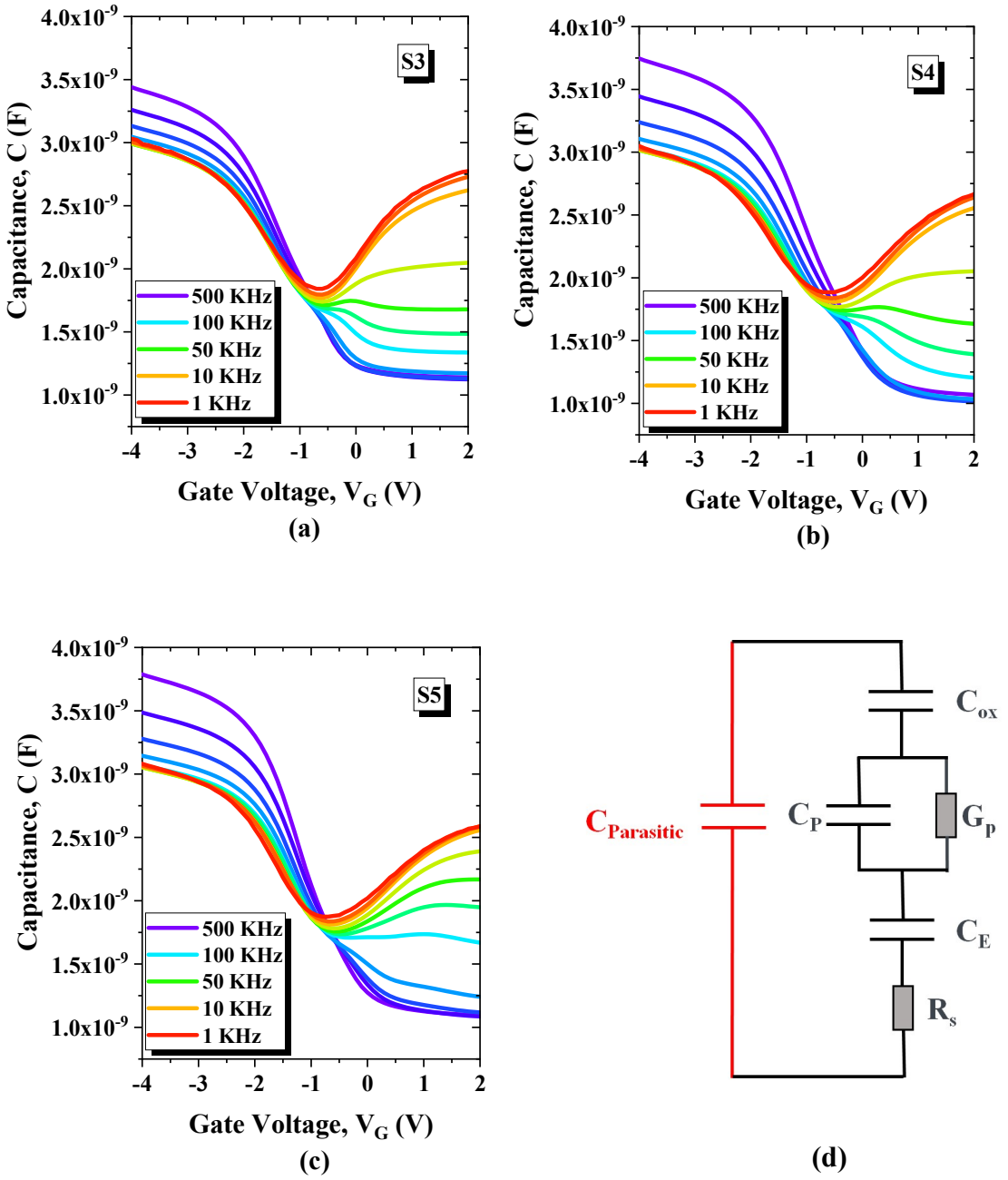


Fig. 4.3(a-c) Frequency dependent CV characteristics for S3, S4 and S5 and (d) simplified model for the frequency dispersion effect.

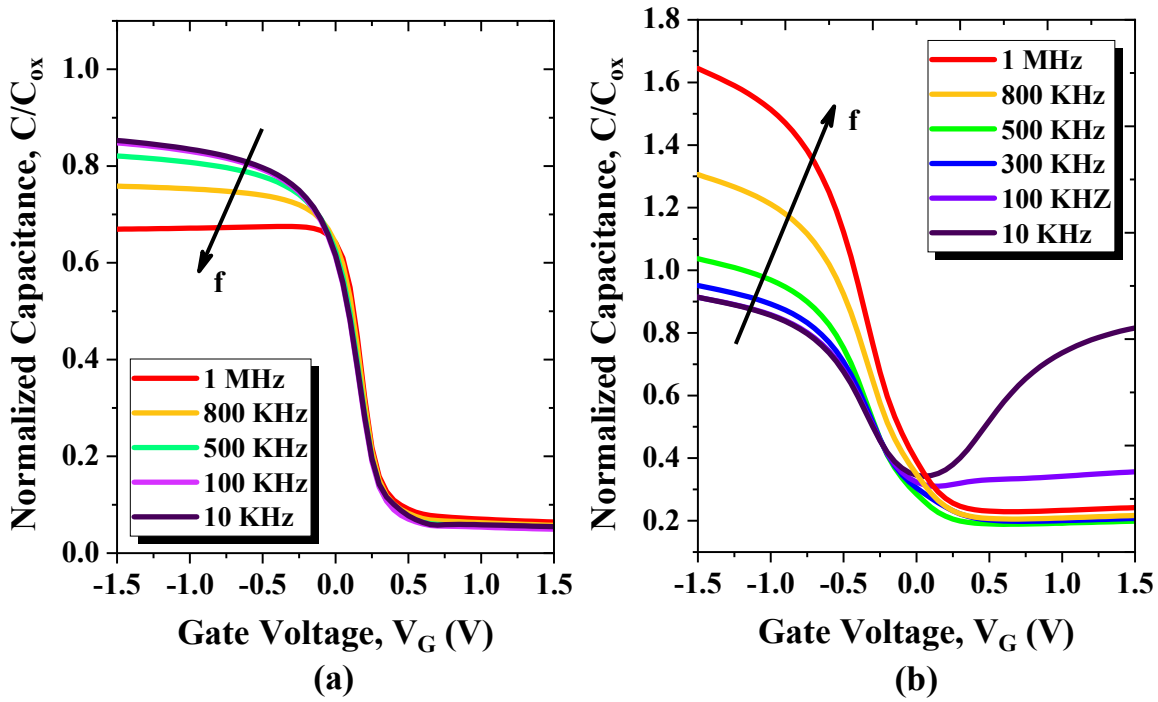


Fig. 4.4 Frequency dependent CV characteristics for (a) Si-based MOSCAP and (b) Ge-based MOSCAP.

This could be explained by the presented model, which was based on the model from literature [167] that is used to renovate the intrinsic gate capacitance from lossy MOSCAP characteristics. Here C_E represent the internal parasitic capacitance of the MOSCAP respectively. C_P is the parallel model capacitance [168]. In these devices, the backside contact used as the reference potential over a large thickness of substrate leads to existence of non-negligible R_S values. The MOSCAP structures used here are planar structures (with no mesa etched or sidewall isolation) leading to existence of current spreading and fringing effects. In the Ge-based MOSCAP, the VS leads to reduced crystal quality resulting in additional parasitic effects together with its inferior interface quality with the oxide compared to Si. This results in an immensely larger C_E in the Ge-based MOSCAP compared to Si-based ones. Hence, this leads to the coupling of the parasitic effects of the $C_{Parasitic}$ to the CV measurements, increasing with the applied frequency ($C_{Parasitic}$ is negligible below 400 KHz), in contrast to Si-based samples that have relatively lower C_E that can be considered negligible in this case. Based on these results, an improvement of the measurement setup design is studied, out of the scope of this work.

At this point, it is interesting to illustrate how does the $C_6H_8O_7$ itself affect the performance separately, so two additional samples were studied, S6 and S7. S6 was treated with H_2O_2 as previously discussed followed by $C_6H_8O_7$ treatment. S7 was treated similar to S6 with

an additional PPO step during gate oxide deposition. Fig. 4.5 shows the results of the CV measurement for the two samples. The $C_6H_8O_7$ demonstrates a better saturation behaviour within the accumulation region and has a sharper transition from depletion to accumulation than the previously investigated classical HF treatment as well as the HCl or the combined HF and sulfite treatment. However, the $C_6H_8O_7$ obviously causes a clear shift towards the positive voltage, indicating negative Q_{eff} charges on the interface. This may be caused by the existence of high density of DB that act as acceptor-type traps that is when activated result in earlier attraction of holes to the surface causing the surface to approach accumulation before gate voltage reaches $V_G = 0$. Hence, it can be deduced, that the $C_6H_8O_7$ effectively removes the oxides but the passivation of the surface is still questionable. On the other hand, the additional step of PPO established a minimized V_{FB} by shifting the CV characteristics around $V_G = 0$ again, where the created IL of GeO_2 efficiently passivated the surface while preserving the sharp transitional slope between depletion and accumulation indicating lower D_{it}. In addition, there is an obvious improvement in the C_{max}/C_{min} indicating enhanced gate control and overall lower trap density. The PPO did not show improvement on the hysteresis behaviour, opposing to the expectations the hysteresis was increased by 10%. Further studies of the impact of combining H_2O_2 and PPO may be useful, yet not within this scope since H_2O_2 is needed in the fabrication of this design for the PDBFET.

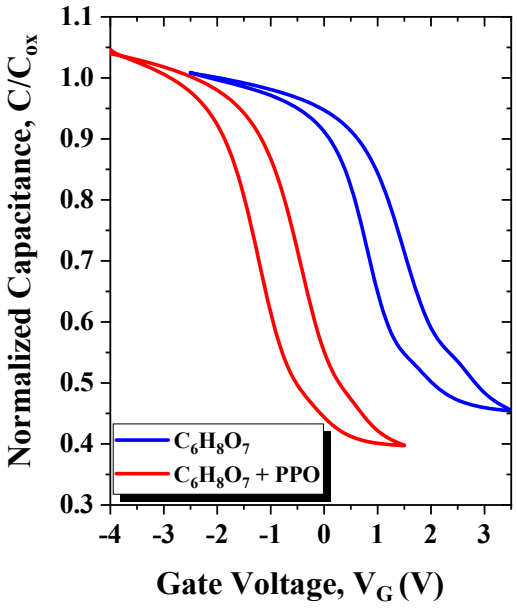


Fig. 4.5 Effect of $C_6H_8O_7$ treatment of Ge-based MOSCAP, with and without applying PPO.

4.7 A New Proposed Treatment Method of Combining $C_6H_8O_7$ Pre-treatment with HCl

The previous improvement caused by introducing $C_6H_8O_7$ treatment prior to S-passivation, and the effect of its treatment separately showed that there can be beneficial effects of introducing it with other chemical treatments. In this stage, it is interesting to show the combination of such oxide etchant with HCl passivation treatment as well. Hence, in this experiment, three samples are fabricated, S8 with simple HF treatment as a reference, S9 treated with HCl as both etching and passivating agent and finally S10 treated with $C_6H_8O_7$ followed by HCl passivation. All treatment methods are reproduced from the above experiments. Results are shown in Fig. 4.6(a-b). Fig. 4.6(a) shows the comparison between the common treatment by HF and its alternative HCl. It is clear that HCl has comparatively lower V_{FB} indicating lower effective Q_{IF} at the interface allowing better saturation behaviour (accumulation region). Another observation comes from its relatively sharper characteristics slope, as a sign of slightly reduced traps (D_{it}). This supports the results in literature showing that high concentrations of HCl (> 20%) can remove most of the sub-oxide layer [132] [117] and achieve relatively better Cl passivation leaving the surface mostly of mono and di-chloride bonds. Then moving to the next comparison, Fig. 4.6(b), the addition of the $C_6H_8O_7$ pre-treatment step to HCl passivation shows an improvement in different aspects. The C_{max}/C_{min} is increased, the saturation of the accumulation region as well as the slope are also further enhanced. On the other hand, $C_6H_8O_7$ still introduces an overall Q_{eff} of negative charge at the interface causing a shift towards positive V_G. The calculated hysteresis for the different samples are $\Delta V_{H\text{-}S8}$ = 295 mV, $\Delta V_{H\text{-}S9}$ = 275 mV, $\Delta V_{H\text{-}S10}$ = 280 mV, no distinctive difference in the hysteresis values. For further improvement of hysteresis, further PPO experiment application on samples S9 and S10 with and without the usage of H_2O_2 oxidizing agent can be investigated.

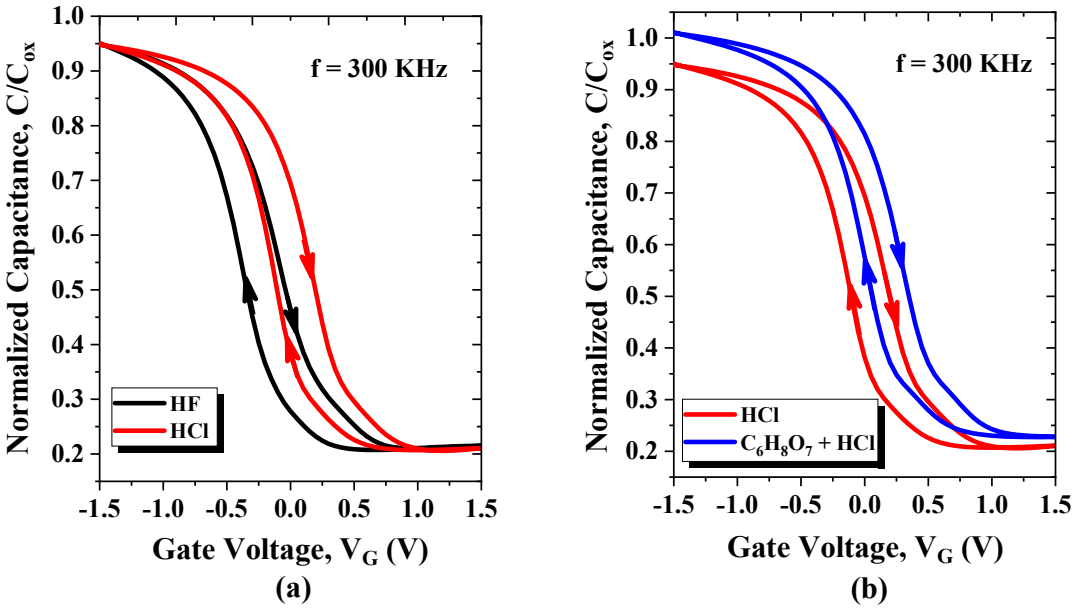


Fig. 4.6(a) Comparison between HF and HCl treatement on Ge-based MOSCAP and (b) comparison between HCl and $C_6H_8O_7$+HCl treatement on Ge-based MOSCAP.

The above results demonstrate that the best treatment methods introduced to samples are those of S2, S5 and S10. S2 was already applied to some of the fabricated transistors demonstrating good SS, but due to the problem in the initial MBE growth recipe (discussed in Chapter 6), fabricated design of the PDBFET might have limited the general performance. The best treatment so far with best results was the treatment of S10, which was applied to the Ge-based p-PDBFET devices of L_{CH} = 40nm (discussed in Chapter 6) and showed a clear improvement in the performance. More analysis can be used to optimize the overall performances by combining the best performing p-PDBFET design together with the best treatment recipe obtained from continued studies on MOSCAP CV-analysis.

In summary, Ge in contrast to Si with its standard recognized cleaning (RCA cleaning) procedure that produces high quality Si surfaces, has no existing cleaning procedure that can achieve comparable results. Current wet chemical treatments still lack the capability of producing such high quality Ge/oxide interfaces with similar values of D_{it} as Si. Enormous efforts are exerted to reach such standard cleaning and passivating technique. In general, HF incapable of removing the Ge sub-oxides. H_2O_2, used as an oxidizing agent to produce clean Ge surface, and can cause high percentage of sub-oxides that makes the cleaning step more challenging. HCl removes sub-oxides well but passivation efficiency is still questionable. $C_6H_8O_7$ is a new technique discussed lately in literature that might lead to better results, yet more studies are still needed for its binding mode to the Ge surfaces and its electrical

characterization results. Other techniques are utilized to form an IL layer that tends to preserve the surface mobility quality of Ge, but on the expense of the EOT of the MOS structure. An optimized combination of both good wet chemical treatment and an IL material would result in the best Ge interface with the deposited high-κ. In this chapter, the study of a number of combinations of basic conventional and unconventional treatments of Ge surface targeting improved results are performed using CV and frequency dependent analysis electrical characterizations. Improved outcomes are expected to enhance the performance of the Ge-based p-PDBFETs.

Chapter 5: Simulation Model and Parameters Evaluation

After the results obtained experimentally, a profounder insight is required into the operation of the manufactured devices and the physics behind this behaviour. In this chapter, a simulation model for the fabricated devices (in Chapter 3) is designed based on aspects including parameters calibrated for Ge material from literature and others extracted from characterisation of the devices in this work. The created model is then eventually updated and tuned based on the successive experimental results. The model showed very good agreement with the experimental results and established very good understanding for the devices actual performance.

5.1 Model Design

Simulation modelling of semiconductor devices is a vital tool that helps to comprehend and depict the physical processes in a device. In addition, it enables reliable predictions of the behaviour of the subsequent device generation based on current device structures performance, saving significant experimentation time and effort. The modelling of semiconductor devices is based on numerical solutions of complex mathematical equations that describe their fundamental physical properties. Two-dimensional device simulations with properly selected calibrated models and a well-defined suitable mesh structure are very suitable for applying predictive analysis of the device structure under consideration and enabling parameter extraction. This is performed by simulator mainly via solving the continuity and transport equations for electrons and holes after applying Poisson´s equation. These calculations in turn help to increase the development process pace and reduce uncertainties while providing improved reliability and scalability of the devices under test.

In this work, simulations were performed on Silvaco device simulator (Atlas) [169]. Modelling of Ge-based devices is still challenging compared to Si devices concerning the parameters used and the various model calibrations. The majority of the physical model parameters are standardized for Si, nevertheless for Ge, many parameters (interface and bulk traps or the carrier different types of masses like mobility, impact ionization and tunnelling) are known with less accuracy than for Si. The physical parameters used at this point for simulation were obtained either by using literature sources [170] [171] or extraction from the experimental data from measurements on MOS capacitors or transistors from this work. The models applied

for current calculations were concentration and mobility dependent SRH, field dependent mobility, Auger, Fermi-Dirac distribution, non-local TAT and BTBT, Impact ionization (selb) and band gap narrowing (BGN).

Since the leakage current is a main concern in this study, the choice of models concerned with the mechanisms involved in such current is very important. The first mechanism is the SRH model that describes the phonon transitions occurrence in presence of traps or defects as a two-step process within the E_G. The equation describing the rate is given by [169] :

$$R_{SRH} = \frac{pn - {n_{ie}}^2}{\tau au_{po}[n + n_{ie}\exp\left[\frac{E_{Trap}}{K T_L}\right] + \tau au_{no}[p + n_{ie}\exp\left[\frac{-E_{Trap}}{K T_L}\right]} \qquad \text{eq. 5.1}$$

where E_{Trap} is the energy difference between the trap and the intrinsic fermi level. T_L is the lattice temperature and $\tau au_{po,no}$ are the hole and electron life times respectively. In addition, main leakage sources are used including the non-local TAT model; which describes the trap to band phonon assisted tunneling effects. It is modeled by including the enhancement factors that modify lifetimes. The tunneling probability is evaluated using Wentzel-Kramer-Brillouin (WKB) approximation [172]. The BTBT is considered using the non-local BTBT model that calculates recombination/generation rate at each position based on the field value at that point. It provides modelling of the forward and reverse tunneling currents of degenerate pn-junctions using a specified mesh that calculates the rates based on interpolation from the basic device mesh. As to the mobility, the Lombardi inversion layer model (CVT) was chosen for this structure, which is more suitable for non-planar devices [169]. CVT model uses the transverse field, temperature and doping dependence set by three components combined using Matthiessen's rule.

$$\frac{1}{\mu_T} = \frac{1}{\mu_{AC}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_b} \qquad \text{eq. 5.2}$$

where μ_{AC} : is the scattering limited mobility due to acoustic phonons, μ_{sr} is the surface roughness factor and finally μ_b is the mobility limited by scattering with optical intervally phonons.

The calculation method used was newton numerical scheme (Newton iteration method) which is a fully coupled solution, in which the total system of equations is solved together. Parameters for Ge, provided in literature presenting good agreement to experimental measurements for Ge PMOS [170], were used to modify those of standard values of Si models

provided by the tool. During fitting process, for further SS matching accuracy, some parameters were further fine-tuned beyond the literature values. Knowing that the mesa sidewall roughness resulting from ICP-RIE etching was expected to be non-negligible, the surface roughness mobility factor μ_{sr} was further adjusted to give good match to the obtained experimental results. The varied values from literature to fit the obtained results are presented in Table 5.1.

Table 5.1 Parameters used for the model.

Parameter	Literature [170] (e,h)	This Model (e,h)
Tunneling mass (-)	0.12, 0.34	0.16, 0.38
Surface roughness (mobility model factor) (-)	1.5	1.67
Delta P (CVT model user defined parameter) (cm^2/Vs)	$1.705x10^{11}$	$1\ x10^{11}$
Saturation velocity (cm/s)	$6\ x10^6$	$9x10^6$

Other parameters necessary for modelling including the technology dependent parameters such as doping concentration N_D, bulk trap charge density Q_B, interface fixed charge density (Q_{IF}) and interface trap charge density (Q_{IT}), were used as adjustable parameters to improve curve fitting. The existence of impurities and lattice imperfections as vacancies and interstitial atoms leads to the introduction of defects inside the crystal identified in the Ge material model as Q_B. The determination of the types of surface states on semiconductor mesa sides is very complicated and essentially depends on its origin. In general, some of the states originate due to the sudden termination of the crystal lattice creating unsatisfied DB, which act as acceptor-like states, trapping electrons from fixed charges in the oxide or from the bulk of the device. Another source of such states is the physical defects on the mesa surface caused by dry plasma etching that can act as either acceptor-like or donor-like states on the surface [173] depending on several parameters including the RF power and the doping type of the bulk. The growth of Ge on top of Si substrate is challenging due to the large mismatch of the crystal lattice constant where misfit dislocations are inevitably generated at the interface between the two materials and typically propagate towards the surface as threading dislocations. In addition, 3D nucleation of Ge can take place and this can cause high surface roughness [174]. The acceptor-like surface states are neutral when empty and negatively charged when filled with an electron. The donor-like states are neutral when filled and positively charged when it loses an electron. The impact of the trap depends mainly on its type and its relative position to fermi level (E_F)

within the E_G. In the case of the p-PDBFET, most of the channel is intrinsic with unintentional doping of p-type doping (lightly doped) hence E_F is located close the mid band gap and considerably above the charge neutrality level (CNL) [171] which leads to the fact that more traps are expected to be filled . Within the very thin δ-doped layer, E_F is almost at the conduction band edge (E_C) indicating that almost all the traps are filled. Hence, as a result, most of the acceptor-trap charges are expected to be ionized, whereas the effect of donor traps is minimized. For this reason, in this modelling only acceptor-type traps are assumed (may be some donor-like traps do exist but their effect is negligible here and only the effective trap density existing is considered).

The interface states tend to pin E_F, where these interface traps have energy levels distributed in the E_G with density of D_{it} (number of states cm^{-2} eV^{-1}). The charge state (occupancy) of the traps depends on E_F. In this model, the interface trap charge density is used as acceptor type traps of value $Q_{IT} = 2.27 \times 10^{12}$ cm^{-2} at energy level positions ranging from 0.02 eV to 0.08 eV below E_C. The interface fixed charges shift the V_{FB} and thus V_{th}. In this model these charges are of negative type as explained above with value of $Q_{IF} = -1.32 \times 10^{13}$ cm^{-2}, as well as bulk traps of acceptor-type near the mid band gap of value $Q_B = 9 \times 10^{17}$ cm^{-3} were assumed as fitting parameters. The values estimated for interface trap charge density from planar MOS capacitors fabricated by using the IHT MBE layers using same oxide Al_2O_3 , by means of high–low CV technique and the conductance technique, were found to be $Q_{IT} \sim 4\text{-}5 \times 10^{12}$ cm^{-2}.

The 2-D model structure used for simulation is shown in Fig 5.1(a). In this simulation model, the Si layers were eliminated due to the alignment of E_G set by the simulation tool, causing no turn-on situation for the device. It is considered a valid assumption since Si layers are merely used for contact purpose. The model is created in two dimensional form for simplicity of calculations and convergence, yet precise enough to be used for modelling the physical structure since the mesa is symmetric. The doping profile used is shown in Fig. 5.1(b), a uniform p-type background unintentional doping resulting grown layers from the MBE of concentration of $N_A = 3 \times 10^{16}$ cm^{-3} was assumed within the whole Ge region of the structure. Starting from the top contact, a uniform doping of p-type with concentration of 1×10^{20} cm^{-3} was used and the lower layer is modelled as uniformly p-type doped layer with concentration $N_A = 5 \times 10^{19}$ cm^{-3}, to match the nominal values existing. As discussed in Chapter 2, the simple diffusion of the δ-layer results in symmetric Gaussian type broadening (neglecting other segregation and migration effects) [71]. In this model, a single Gaussian profile was used to implement the δ-doping with peak concentration N_D and standard deviation characteristic length (L_{charc}) (the doping drops off

laterally according to Gaussian distribution with standard deviation of $L_{charc}/\sqrt{2}$). These two parameters are varied corresponding to the provided Q. For this sample, effective doping concentration of $N_D = 3x10^{19}$ cm^{-3} was assumed and $L_{charc} = 6$ nm. There is a big difference between the nominal doping values used in experiment ($N_D = 1x10^{20}$ cm^{-3}) and the actual model fitting value. The Gaussian distribution parameter values were varied through this work among different samples accordingly.

While establishing the model, the results were fitted to the transfer characteristic behaviour for a group of transistors of different sizes simultaneously together with the output characteristics to ensure a reliable created model. The sample used for the fitting is Sample B discussed in Chapter 3. The obtained results from simulations for transfer characteristics are in very good agreement with the experimental measurements as shown in Fig. 5.2(a). We used the surface roughness factor to fit I_{on}, indicating that an increase of I_{on} is achievable by further treatment of the Ge surface either during mesa etching by improving the etching recipe or pre gate-oxide deposition by using advanced chemical surface treatment . The main contributor to the I_{off} at low V_{DS} = - 100 mV, is the TAT mechanism because of the crystal defects and surface traps introduced during growth due to integration on Si (lattice mismatch of 4.2%) and processing (interface quality and oxide deposition step). The output characteristics using this simulation model with the corresponding adjustable parameters for the sample show good agreement with measurements in Fig. 5.2(b). The p-PDBFET output characteristics showed the non-saturating behaviour for $V_{DS} < -0.7$ V. From simulation fitting results, BTBT model demonstrates a significant contribution to the non- saturating behaviour of the characteristics, which starts at around -0.66 V and becomes effective at around -0.7 V. Another mechanism that showed contribution, but at a relatively higher negative bias of V_{DS} (closer to -1 V) is the impact ionization mechanism.

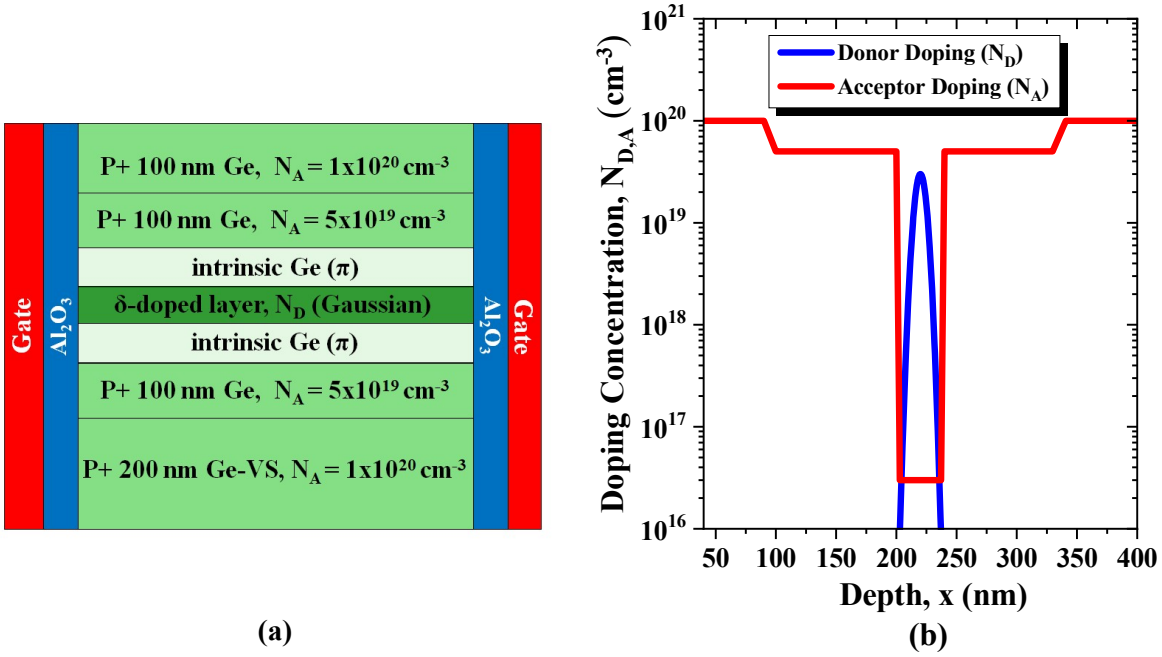


Fig. 5.1(a) 2-D model structure of the simulated Ge-based p-PDBFET and (b) doping profile used for simulation.

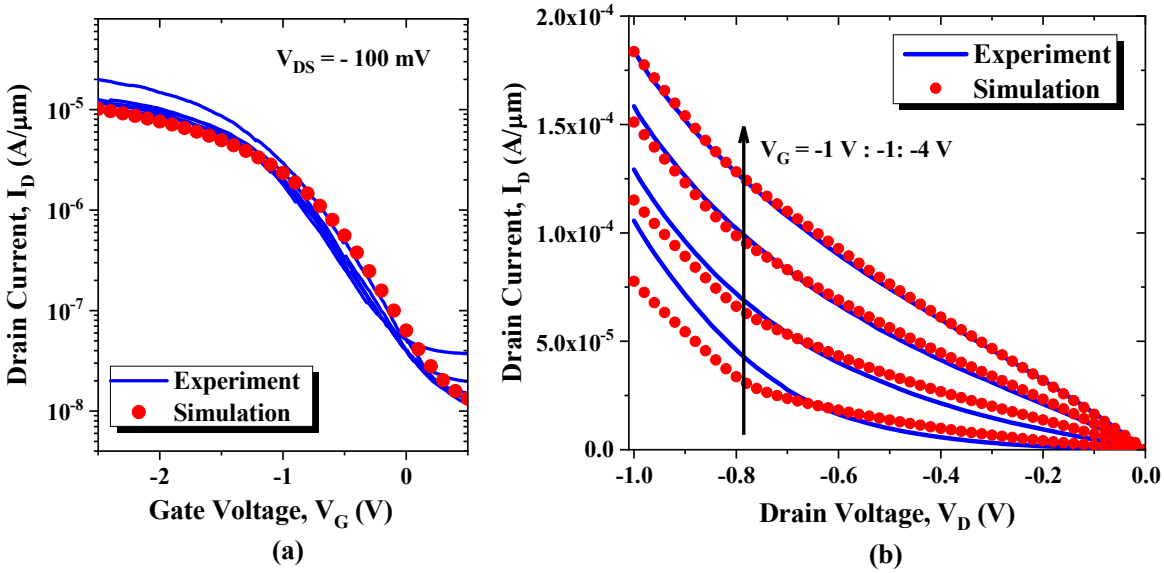


Fig. 5.2(a) Transfer characteristics of measured and simulated Ge-based p-PDBFET and (b) output characteristics of measured and simulated Ge-based p-PDBFET.

The fitting of the simulations results showed that the main contributor to I_{off} is TAT mechanism as a result of both crystal defects and surface traps. Fig. 5.3(a) demonstrates that the dark current measured for different mesa sizes of Sample B scaling with area indicating dependence on bulk traps density, and the extrapolation of data shows the expected improvement that can be achieved by size reduction (I_{off} ~ 4.6 x 10^{-9} A for mesa Area of A= 10^{-4} μm^2). In addition, the effect of the reduction in the temperature (in the range between T = 293 K to T = 241 K) on the transfer characteristics is shown in Fig. 5.3(b), demonstrating I_{off} reduction with decrease in temperature. Arrhenius plots (Fig 5.3(c)) of the average dark current at low gate bias (V_G) (from 0 to 1 V) support simulation speculation as well, where the slope of the plot shows E_A ~ 130 meV, which is lower than half of the E_G of Ge, confirming TAT contribution [104]. In subsequent experiments to Sample B in Chapter 3, even devices with mesa dimension of L_{mesa} =1µm achieved lower I_{off} than that linearly extrapolated from the larger sized transistors with L_{mesa} = 2-5 µm for sample B, indicating a superior effect of size reduction on device performance due to trap density elimination.

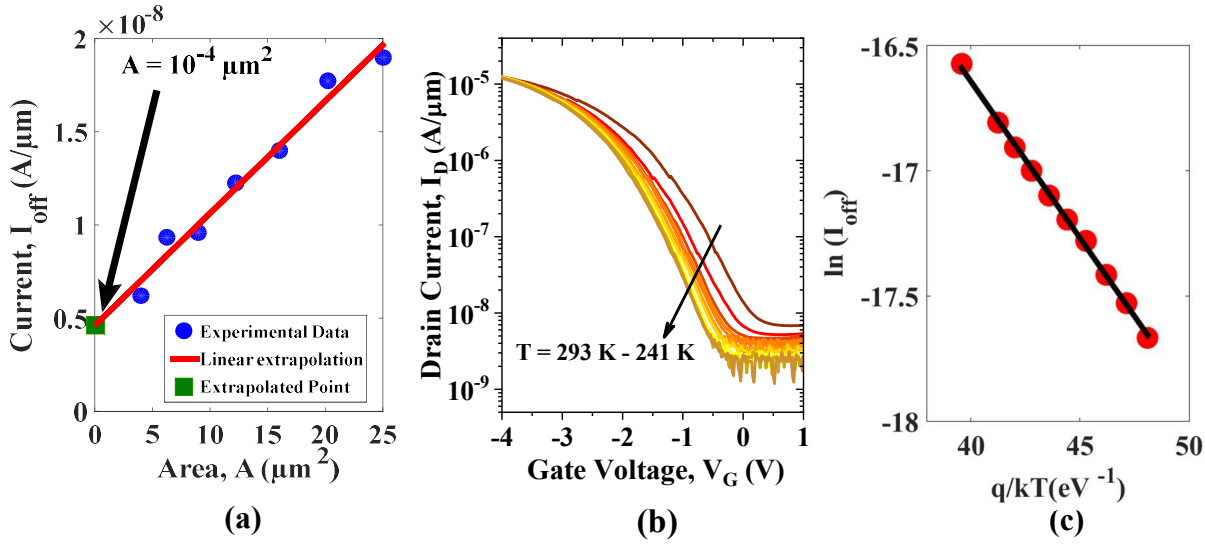


Fig. 5.3(a) Scaling of I_{off} with area. (b) Low temperature measurement effect on transfer characteristics of p-PDBFET. (c) Arrhenius plot of the fabricated devices.

Based on modelling of Ge-based p-PDBFETs as 2D-model shown in Fig. 5.1, simulation results for the transfer characteristics of a Ge-based transistor with a uniformly doped channel (p-MOSFET) with the exact same parameters and doping concentration N_D = 1.6 x 10^{19} cm^{-3} corresponding to the equivalent V_{th} and the p-PDBFET results are compared in Fig. 5.4. The p-PDBFET structure shows lower I_{off} with respect to uniformly doped p-MOSFET and relatively higher I_{on}. This can be explained by plotting the channel carrier distribution

demonstrated in Fig. 5.5 whilst increasing the gate voltage gradually from V_G = 0V (off-state) up to V_G = -2 V (start of the on state) at fixed drain voltage (V_{DS} = -100 mV). The main difference is in the inversion layer creation, where in the p-PDBFET the inversion layer is spreading into the bulk within the most of the channel length. However, in the p-MOSFET it is confined throughout the whole channel length to the interface. Hence, for the p-PDBFET the carrier distribution in the channel leads to reduced surface and impurity scattering that is considered as a major challenge in Ge-based p-MOSFET due to their channel/oxide interface properties. This is expected to enhance the I_{on} and in turn would lead to reduced surface tunnelling processes leading to lower I_{off} in addition to the tailored electric field leading to enhanced electrostatic control. In the real case, the equivalent interface traps experienced by carriers in each case should vary, where for undoped regions it is expected to be less, hence a larger effect is expected in experiment than revealed by simulation, where interface traps were assumed the same in both cases.

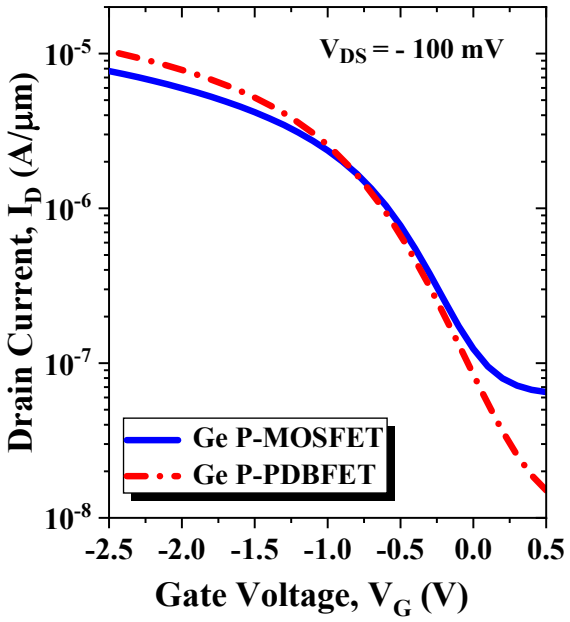


Fig. 5.4 Simulation comparison of the transfer characteristics of p-MOSFET and p-PDBFET with the same threshold voltage Vth.

An interesting observation here is the actual L_{CH} of the transistor, which is in general defined as the distance between the source and the drain. In fact, in the PDBFET structure, demonstrated by the simulation as in Fig. 5.5, the actual L_{CH} is the effective delta layer thickness [175], which is in this case around ~ 20 nm as estimated from the simulation results of holes

distribution contours. This result predicts that these devices are actually representing highly scaled channel length devices even beyond the state of the art.

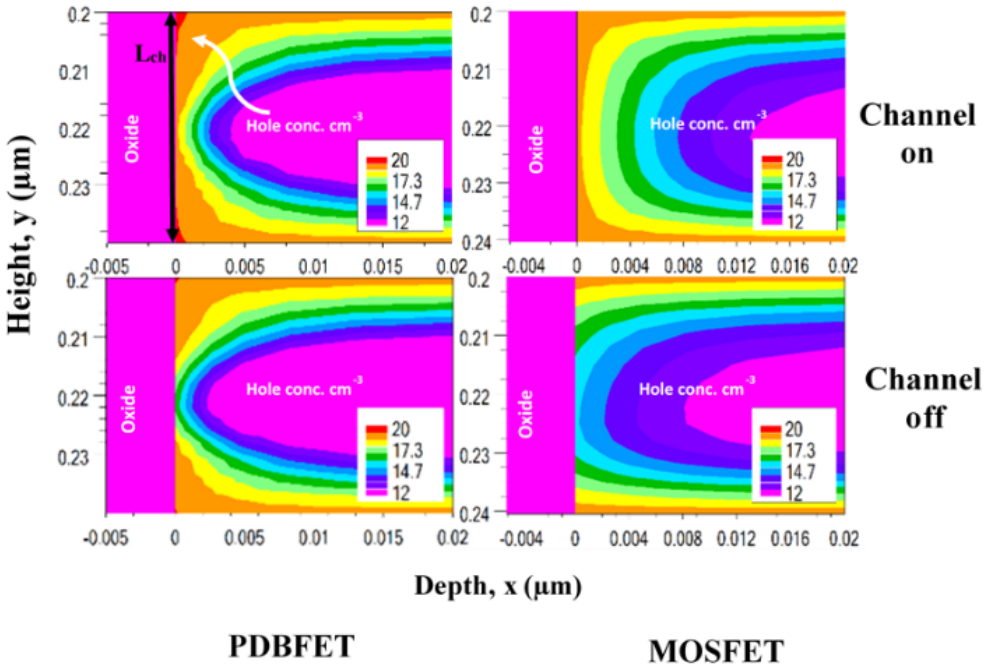


Fig. 5.5 Hole concentration distribution among the channel for both (a) p-PDBFET and (b) p-MOSFET at on-state and off-state.

5.2 Ge-Based P-PDBFET Model Development

The next step to develop the model, with respect to the experimental work was to reproduce the experimental results of the set of fabricated PDBFETs with different doping concentrations simultaneously. This means that all the parameters are fitted while being fixed to all samples except for the values of the effective doping concentration (peak value) and the standard deviation (ramping of the δ-doping is a function of the added Q and growth conditions) which correspond to the supplied dose during MBE growth (Fig. 5.6(a)). The technological parameters as interface traps or the fixed interface/oxide charges (dependent on surface treatment and oxide deposition conditions) and sometimes the bulk traps as well (dependent on the MBE growth conditions) were needed to be adjusted too (on a minimal scope). This is valid since these technological parameters are impossible to be fixated along the successive fabrication processes, from one sample to the other. The samples used for this fitting are Samples A, B and C from Chapter 3. To apply the fitting to these samples, additional modifications to the parameter values were essential to be applied. First, concerning the interface-trap level positions, it was redistributed on a wider range of energy levels, near to CB,

near to mid band gap and near to VB. The positions of the interface traps were placed at 0.2 eV, 0.4eV and 0.6 eV from E_C. The charge neutrality level (CNL) in Ge is located around 0.1eV above the valence band edge (E_V). The validity of the presence of acceptor traps near the VB below CNL is discussed in [176]. This modification resulted to a stronger impact of the interface traps on the SS and helped to improve the fitting results, mainly at the weak inversion region. It was clear that the levels nearest to E_V have the highest impact and produces the best matching with the experimental results behaviour.

The Q of active dopants required for fitting were less than that of the nominal values, where the model values mainly represent only the effective active dopants. The fitting of Sample B previously discussed was further modified, mainly by concerning a single device performance. Corresponding to this fitting, less negative Q_{IT} are assumed, necessary to obtain the same V_{th}. The tunnelling masses and saturation velocities were updated to be similar to the literature values [170]. Additional modification required updating, with $Q_B = 2.7 \times 10^{18}$ cm^{-3}, indicating a very high defect density inside the crystal. The surface roughness factor was further increased (higher roughness) to meet the measured current values, signifying a quite humble mobility performance behaviour. Table 5.2 shows a comparison between the previous and the updated values used. Then the model fitting was further extended to included the samples A and C. The fitting values corresponding to the doping concentration peak value, L_{charc} and the different technological parameters for each of the Samples A, B and C are shown in Table 5.3. All non-mentioned parameters are kept constant for all samples.

Table 5.2 Differences in values between the initial model and the updated model.

Parameter	Model I	Updated Model
Tunneling mass (-)(e,h)	0.16, 0.38	0.12, 0.34 [2]
Surface roughness (mobility model factor) (-)	1.67	1.8
Delta P (CVT model user defined parameter) (cm^2/Vs)	1×10^{11}	1×10^{11}
Saturation velocity (cm/s) (e,h)	9×10^6	6×10^6 [2]
Delta Doping of sample B (cm^{-3})	3×10^{19}	1.1×10^{19}
L_{charc} (nm)	6	4.1
Q_{IF} (cm^{-2})	-1.32×10^{13}	-2.3×10^{12}
Q_B (cm^{-3})	9×10^{17}	2.7×10^{18}
Q_{IT} (cm^{-2})	2.27×10^{12}	1×10^{12}

Table 5.3 Parameters used for the different Samples A, B and C.

Parameter	Sample A	Sample B	Sample C
δ-Doping (cm^{-3})	$8.3x10^{18}$	$1.1x10^{19}$	$1.9x10^{19}$
L_{charc} (nm)	3.6	4.1	4.2
Q_{IF} (cm^{-2})	$-2.3\ x10^{12}$	$-2.3\ x10^{12}$	$-2.3\ x10^{12}$
Q_B (cm^{-3})	$2.7\ x10^{18}$	$2.7\ x10^{18}$	$2.7\ x10^{18}$
Q_{IT} (cm^{-2})	$6.8x10^{12}$	$1x10^{12}$	$9x10^{12}$

Results from both experiment and simulation show excellent agreement (Fig. 5.6(b)). Comparing the experimentally determined device characteristics with simulation results gives the opportunity to gain insight into strategies for the optimization of the device. Both experimental and simulation results, revealed by BTBT model, show an optimum doping concentration that leads to the best I_{on}/I_{off} (dependent on growth technique, the interface and bulk trap concentrations produced during processing). This doping concentration would consequently lead to the best SS. An increase in the I_{on} can be achieved mainly by reducing the mesa surface roughness and minimizing the δ-doping concentration. I_{off} can be improved by optimizing the δ-doping concentration, reducing trap density and possibly by further improvement of the transistor channel design, which will be discussed in the Chapter 7.

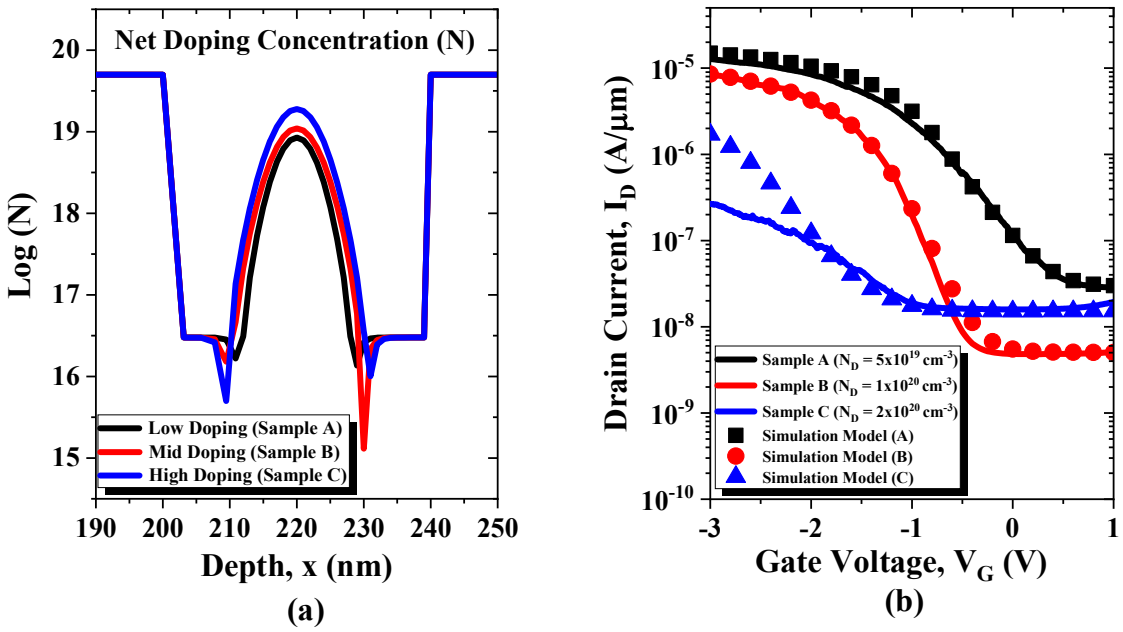


Fig. 5.6(a) The δ-layer doping profile fitted for different doped samples and (b) transfer characteristics of measured and simulated Samples A, B and C.

A very interesting point is comparing the simulation fitting values of δ-doping concentrations compared to experiment nominal values. Table 5.4 shows the difference between the nominal doping values and the simulation model fitting values representing the actual effective/activated dopant concentration. The Q values are calculated using eq. 5.3. A difference of one order of magnitude in the peak concentration was detected. For the assumption of Gaussian distribution, the dose can be approximated as:

$$Q = \sqrt{2\pi}\,\Delta R_p\, C_{peak} \qquad \text{eq. 5.3}$$

where ΔR_p is the straggle and C_{peak} is the peak concentration

Table 5.4 Difference between experimentally added doses and simulation calculated doses.

Parameter	Experiment (Nominal conc.)	Simulation (Activated conc.)
δ-doping sample A (cm^{-3}),	$5x10^{19}$	$8.3x10^{18}$
Dose Q (cm^{-2})	$4\ x10^{13}$	$6.2\ x10^{12}$
δ-doping sample B (cm^{-3}),	$1x10^{20}$	$1.1x10^{19}$
Dose Q (cm^{-2})	$8\ x10^{13}$	$8.25\ x10^{12}$
δ-doping sample C (cm^{-3}),	$2x10^{20}$	$1.9x10^{19}$
Dose Q (cm^{-2})	$1.6\ x10^{14}$	$1.43\ x\ 10^{13}$

Based on this consequence, SIMS measurement were performed on Sample B layer structure. The dopant concentration as a function of depth into the layer structure is shown in Fig. 5.7. The measurement result demonstrated that the Sb doping for the δ-layer within the channel is of much lower concentration than the Q designed. Only about 10% of the introduced value existed and the rest of the dopant atoms segregated towards the top, due to the usage of relatively higher growth temperatures for the upper layers than the δ-layer growth temperature. This, in turn, lead to the spreading of the biggest portion of the dopants into the intrinsic regions and finally residing in the source region. The existing barrier lead to a functioning transistor action but with weak blockage capability.

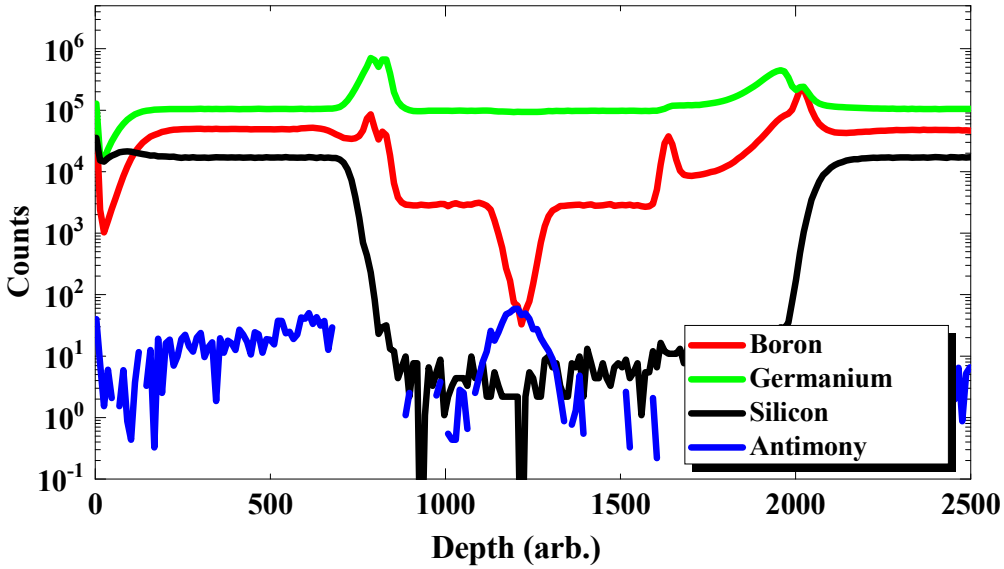


Fig. 5.7 SIMS measurement for Sample B.

Hence, the SIMS result came to support the simulation speculations, indicating a problem in the MBE δ-layer growth technique, leading to two main problems. First, a severely reduced peak concentration leading to lower barrier and loss of gate control increasing the leakage current I_{off} and SS. Second, the N_D atoms that were not activated still existed within the crystal, that can act as trap-centers contributing to further deteriorated behaviour for the I_{off} and I_{on} at higher V_{DS} as seen in the output characteristics. A careful study was performed concerning the growth recipe. An improved recipe was then designed. The results, showing significant improvement, will be discussed in Chapter 6.

As a summary, the performance of the Ge-based p-PDBFET device is mainly limited by three effects: first the interface quality between oxide and Ge which introduces a large amount of interface traps that is the main bottle neck for the deterioration of SS and a great contributor to the high I_{off} acting as trap-centers for TAT mechanism. In addition, the surface roughness factor is considerable due to dry etching of mesa and this in turn affects the achievable I_{on} that is one of the Ge pursued parameters. Second, the large bulk trap density present due to integration on Si and problematic growth of the δ-layer which causes threading dislocations and defects that lead to high leakage currents through TAT current. Finally, the third cause is the small E_G of Ge that leads to high BTBT, which is the main cause of degraded behaviour at high V_{DS} appearing as non-saturating behaviour and contributes to I_{off} leakage current. Addressing the above challenges can be done by several steps. High surface quality of the Ge mesa can be done by optimizing the etching process recipe. Concerning the D_{it}, attention has been drawn to reduce it by finding a suitable cleaning and passivation steps equivalent to

the Si standard cleaning processes prior to the oxide deposition step, which was discussed in Chapter 4. This would lead to improving I_{on}, SS and reducing surface leakage TAT current leading to lower I_{off} and better gate control. Concerning the crystal quality, bulk defects and traps is achievable by optimizing the MBE growth recipe for the δ-layer in Ge-based p-PDBFETs to achieve the required doping value and profile besides reducing the structure size. This would result in higher effective barriers against leakage currents mechanisms and lower TAT processes that leads to improved gate control at high V_{DS}. For the high BTBT rate concern, resulting from the small E_G, producing high leakage and the non-saturating behaviour in the output characteristics, further channel design improvements regarding the Ge-based p-PDBFET structure and simulation model results are introduced in Chapter 7.

Chapter 6: Fabrication of Optimized Ge-Based P-Channel PDBFET

In this chapter, Ge-based p-PDBFETs with modified MBE growth recipe and varied L_{CH} = 100 nm, 60 nm and 40 nm are fabricated, characterized and discussed. The new devices demonstrated significant improvement in performance. The electrical characterization of the PDBFETs results obtained are optimistic achieving low I_{off} reaching sub-nanoampere per micrometre using relatively large sized devices, which are competitive in electrostatic performance to even more complicated and extremely scaled devices in literature. Furthermore, leakage current sources are studied through surface treatment experimental study (discussed in Chapter 4) that has never been applied before this work to Ge-FETs, which proved to improve the device behaviour. Simulation work based on the previously established model in Chapter 5 was applied to the new results, illustrating possible improvements with further T_{OX} reduction. Additional possible enhancements of the performance of the devices is clearly demonstrated through low temperature measurements. Fabricated devices proved their potential for high performance applications and energy efficient systems.

6.1 New Growth Recipe

Simulation outcomes in conjunction with the characterization of the formerly fabricated devices established a basis for the new growth technique. Based on the fact that a large percentage of the δ-doping was aggressively outspread into the channel and over to the source region, attentions were made in particular towards the step of the Sb-atoms deposition, concerning the precise temperature control for this specific step and the subsequent layers as well. In the new recipe, the growth temperature of deposition was kept at 170 °C for both of Sb deposition and the subsequent intrinsic zone i-Ge to avoid the segregation of the Sb, in contrast to the previous recipe. The Sb has to be incorporated immediately in order to get the next layer as intrinsic as possible, which established the importance of growing the second intrinsic Ge region under such low temperature. The rest of the temperature scheme was retained the same as the previous recipe. Fig. 6.1 shows the former temperature growth scheme in Fig. 6.1(a) versus the new modified scheme in Fig. 6.1(b). The new p-PDBFETs processing steps were performed in a similar manner as Chapter 3 except for the mesa surface passivation prior to

gate oxide deposition which varied accordingly. In this chapter , only the characterization and the improvements in performance aspects are discussed.

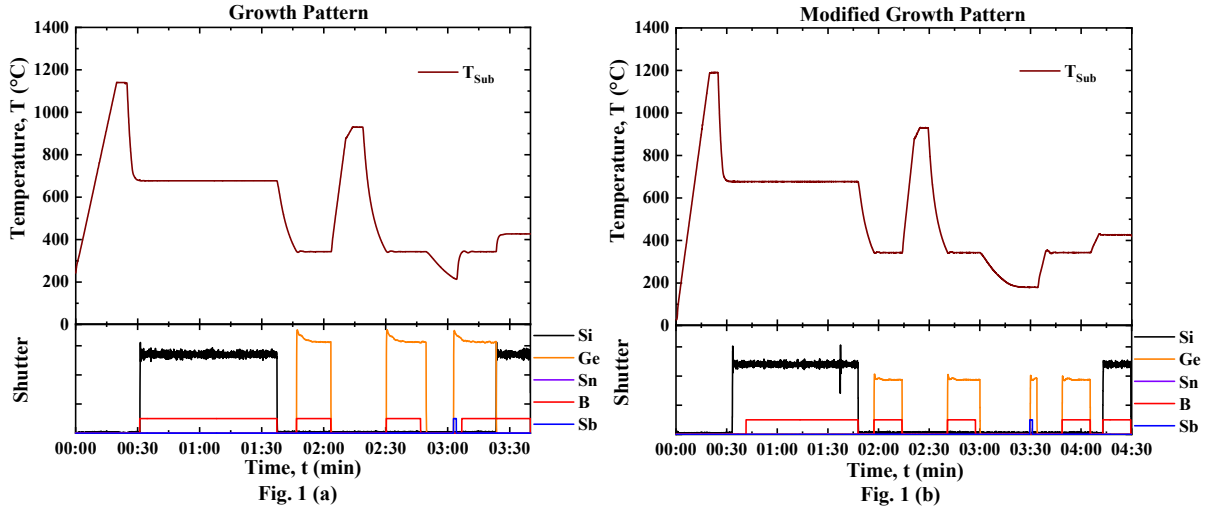


Fig. 6.1(a) The former temperature growth scheme of the PDBFET layers and (b) the modified growth temperature scheme.

6.2 Fabricated Ge-Based P-PDBEFT with Different Channel Lengths

Results on the second generation of fabricated Ge-based PDBFET devices are shown in this section. In this experiment, three different samples were fabricated, each with different channel length, Sample K with L_{CH} = 100 nm, Sample L with L_{CH} = 60 nm and Sample M with L_{CH} = 40 nm according to Table 6.1. Transfer characteristics for the fabricated p-PDBFETs are shown in Fig. 6.2(a) for different L_{CH} = 100 nm, 60 nm and 40 nm. I_{on} increases as L_{CH} is reduced, due to the stronger field from the drain that lowers the potential barrier more effectively. The subthreshold channel current is a combination of many components including DIBL and weak inversion currents described in eq. 6.1 [177] with μ_o as zero bias mobility, ϵ_{ox} as oxide permittivity, V_s as source voltage, V_t as thermal voltage, η as DIBL coefficient, m as subthreshold swing coefficient. The results show that I_{off} increases with L_{CH} reduction, this is due to subthreshold leakage current varying with inverse proportion to channel length.

$$I_{sub} \propto \mu_o \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L_{CH}} V_t^2 \left(e^{\frac{V_G - V_S - V_{th} + \eta V_{DS}}{m V_t}} \right) \left(1 - e^{\frac{-V_{DS}}{V_t}} \right) \qquad \text{eq. 6.1}$$

For all transistors, it can be seen that the threshold voltage is slightly shifted to $V_{th} > 0$. This is due to acceptor-like traps acting as effective negative charges that are either present inside the oxide or at the Ge/oxide interface. This can be due to two reasons, either the Al_2O_3 is O-rich forming oxygen DB [178], or due to the DB of Ge as a result of surface termination, which possess energy states below E_V of the Ge hence always acquiring negative charge [179] [131]. In addition, generally for lightly doped p-Ge (unintentional doping of intrinsic regions), E_F is located substantially above CNL [171] and hence more acceptor-like states are filled, building up negative charges at interface. These negative charges attract holes which helps the inversion of the channel and results in shifting V_{th}, leading to a conducting channel at $V_G = 0$. This can be remedied by further adjustment of δ-doping value, enhanced passivation of the Ge surface or fine-tuning of gate stack work function. The transfer characteristics results demonstrated $I_{on}/I_{off} = 4 – 4.5$ orders of magnitude. The SS = 220 mV/dec for L_{CH} = 100 nm and 60 nm and SS = 351 mV/dec for $L_{CH} = 40$ nm at $V_{DS} = -50$ mV which is considered as very good performance considering the relatively high T_{OX} used (EOT = 7 nm). Detailed results are shown in Table 6.2. The potential improvement in SS due to T_{OX} reduction is demonstrated in the next section based on the simulation model results. At relatively lower V_{DS}, the normalize leakage current is in the range of sub-nanoampere, which is comparable to state of the art devices. Fig. 6.3(a) to 6.3(c) show the transfer characteristics for the different L_{CH} at diverse V_{DS}. Fig. 6.3(d) represent a comparison of I_{on}/I_{off} of the different samples. For the Sample K with $L_{CH} = 100$ nm, the transfer characteristics shows the highest I_{on}/I_{off} among all V_{DS} range due to possessing the lowest leakage current, regardless its relatively smallest I_{on}. I_{on}/I_{off} increases as the V_{DS} is increased. For Sample L with $L_{CH} = 60$ nm, I_{on}/I_{off} has almost constant ratios for all values of V_{DS} whereas for Sample M with L_{CH} = 40 nm the I_{on}/I_{off} reduces drastically because of the SCEs. The results show that for each L_{CH} there is an optimum doping scheme concerning doping concentration and relative d that achieves the best performance, which is satisfied for $L_{CH} = 60$ nm in this case.

Table 6.1 MBE grown layer structure with different channel length for Ge-Based p-PDBFET.

		Sample K	**Sample L**	**Sample M**		
Layer	Material	Thickness nm	Thickness nm	Thickness nm	Doping cm^{-3}	Growth Temperature °C
Source contact	Si	100	100	100	$N_A = 1x10^{20}$	400
Source	Ge	100	100	100	$N_A = 5x10^{19}$	330
Channel	Ge	46	26	16	-	170
Channel	Ge	8	8	8	$N_D = 3\ x10^{19}$	170
Channel	Ge	46	26	16	-	330
Drain	Ge	100	100	100	$N_A = 5x10^{19}$	330
Drain	Ge VS	100	100	100	$N_A = 5x10^{19}$	330
Drain Contact	Si	100	100	100	$N_A = 1x10^{20}$	600

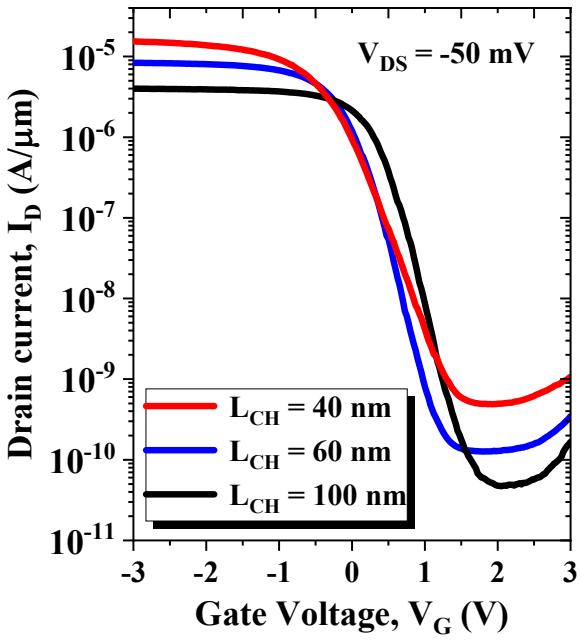


Fig. 6.2 Transfer characteristics for 100 nm, 60 nm and 40 nm channel p-PDBFETs at V_{DS} = -50 mV.

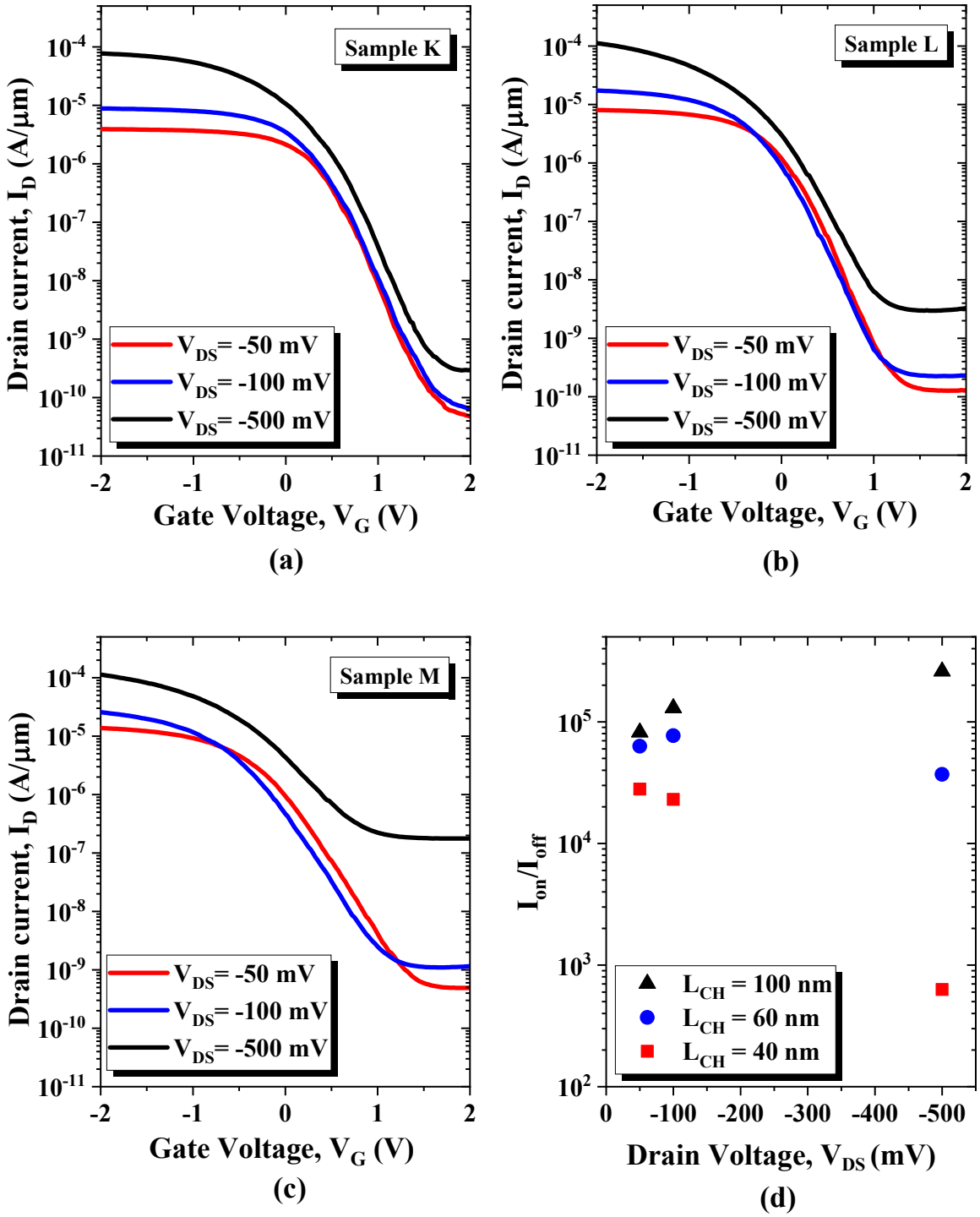


Fig. 6.3 Transfer characteristics for (a) 100 nm, (b) 60 nm (c) 40 nm channel p-PDBFETs at various V_{DS} and (d) comparison of the I_{on}/I_{off} ratio at different V_{DS}.

Table 6.2 Results on p-PDBFET with different channel lengths comparison.

Parameter	L_{CH} = 100 nm	L_{CH} = 60 nm	L_{CH} = 40 nm
SS mV/dec (V_{DS} = -50 mV)	219	220	351
SS mV/dec (V_{DS} = -100 mV)	230	239	366
SS mV/dec (V_{DS} = -500 mV)	234	304	511
I_{on}/I_{off} (V_{DS} = -50 mV)	$8.2x10^4$	$6.3x10^4$	$2.8x10^4$
I_{on}/I_{off} (V_{DS} = -100 mV)	$1.3x10^5$	$7.7x10^4$	$2.3x10^4$
I_{on}/I_{off} (V_{DS} = -500 mV)	$2.6x10^5$	$3.7x10^4$	$0.63x10^3$

The output characteristics of the L_{CH} = 100 nm and L_{CH} = 60 nm in Fig. 6.4(a-b) show onset of saturation behaviour whereas for the L_{CH} = 40 nm (Fig. 6.4(c)) the behaviour is relatively improved, but still shows non-saturating performance. That can be due to the inefficient barrier for this relatively short channel length leading to a stronger lateral field effect from the drain where an optimum doping profile (as discussed in Chapter 3) is still required specifically under the new temperature growth recipe. Another possibility would be due to the rise of the tunnelling currents (TAT and BTBT) that limits the Ge channel scaling (actual L_{CH} is expected to be much shorter than L_{CH} = 40 nm due to inverted intrinsic regions, leaving the effective L_{CH} ~ 20 nm, as discussed in Chapter 5). In addition, stronger field problems (SCEs) clearly appears within shorter channel lengths due to non-idealties such as non-sharp profiles of doping. This may be cured by modifying the barrier by using a thinner delta region with higher doping concentration peak while concerning the adequate Q hence elongating the intrinsic regions. Another solution that addresses both problems is the introduction of heterostructure barrier within the channel (Chapter 7).

The maximum g_m for the different samples are compared in Fig. 6.4(d). The values are relatively low (g_m = 50-70 μS/μm) compared to state of the art devices from literature, that recorded g_m values approaching 2 mS/μm [67]. The main reason of this low value is due to the relatively high EOT which reduces C_{ox} that is a main component of the g_m extracted values. Furthermore, high D_{it} is a factor that affects the FET device g_m value.

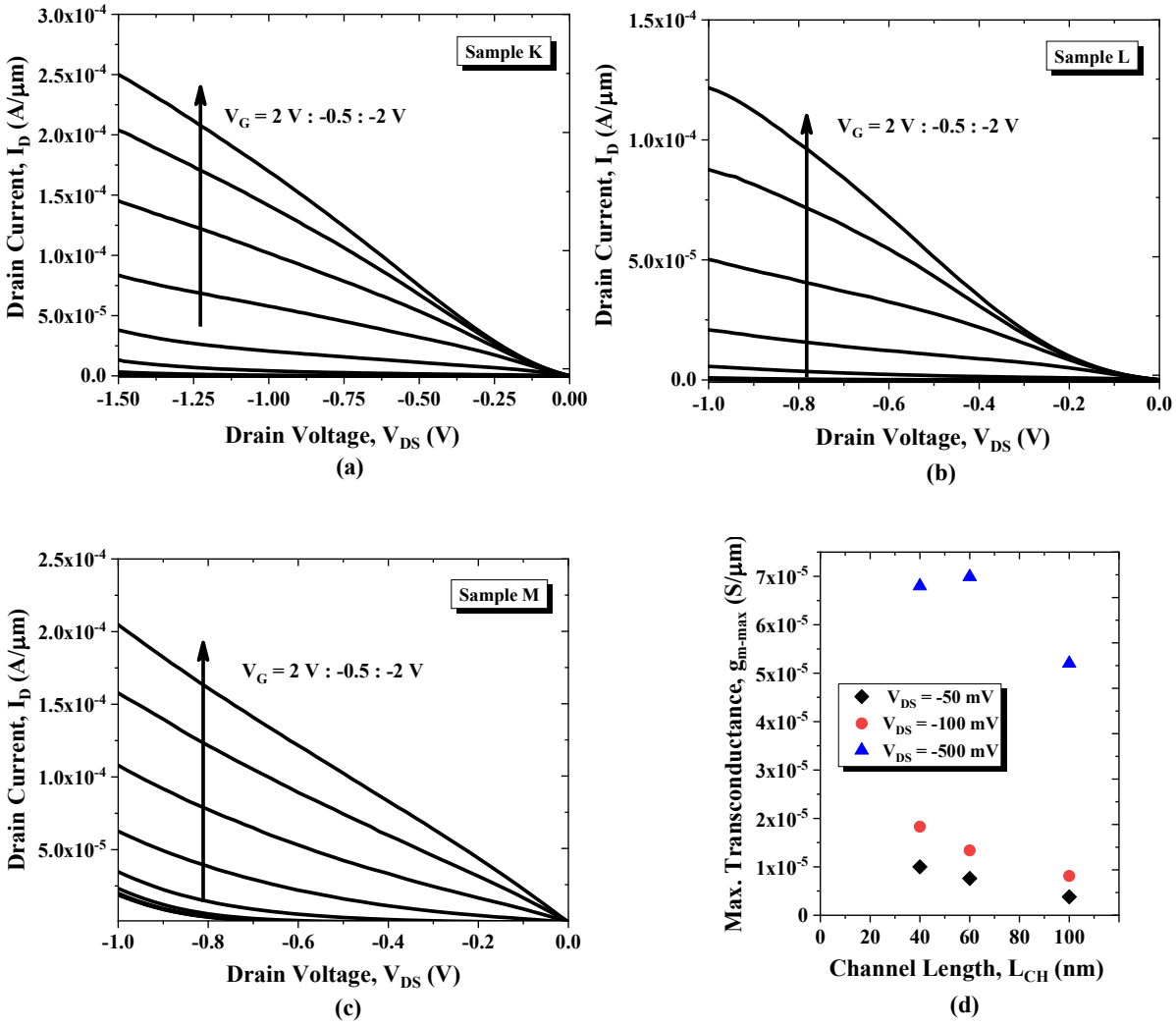


Fig. 6.4 Output characteristics of (a) 100 nm, (b) 60 nm, (c) 40 nm channel p-PDBFET and (d) maximum g_m at different V_{DS} values versus device channel length.

6.3 Discussion of Device Performance, Limitation and Potential Improvements

Based on the previous results, concerning these parameters: SS, I_{on} and I_{off}, improvements can be obtained by introducing modifications to the structure. This can be achieved by considering the following factors:

i) Interface quality (interface traps) effect on SS, I_{on} and I_{off}.

ii) T_{OX} reduction and its effect on SS.

iii) Bulk defects and traps (size reduction) effect on I_{off} and SS.

6.3.1 Surface Treatment Effect on Interface Quality and Performance

In attempt to improve the device performance through gate/oxide interface quality, the passivation step prior to gate oxide deposition is considered. This step is one of the primary factors responsible for the Ge/oxide interface properties. The passivation step of the mesa surface is done after chemically oxidizing it using H_2O_2 followed by dipping the samples in DI water for GeO_2 removal, as mentioned in Chapter 3 and 4. In this experiment, this stage was done using either of two methods for L_{CH} = 40 nm p-PDBFET. First method for Sample M, is to passivate the sample surface by simply using 1 min dip in HF solution with concentration HF:H_2O = 1:40. The sample is cleaned for 30 sec in DI water and blown dry using N_2. The second method for Sample N, is done by cleaning the surface using $C_6H_8O_7$ at RT with concentration of 2.4 mol/l for 1 min for thorough oxide removal similar to experiment in Chapter 3, but using exact parameters of literature [116]. Then the sample is dipped 10 min in HCl for passivation [117] [119] with HCl:H_2O = 37:100, where Cl passivation is employed for further confirmation of inhibiting the re-oxidation after the cleaning with $C_6H_8O_7$. Similar to the previous sample, Sample N is then placed for 30 sec in running DI water and blown dry with N_2. The effect of surface treatment on transfer characteristics is shown in Fig. 6.5(a). The samples treated with $C_6H_8O_7$+HCl show an enhanced average behaviour regarding both the average SS and the I_{on}/I_{off} ratio. A detailed comparison of performance of different parameters between sample M and sample N is shown in Table 6.3. This enhancement in sample N behaviour can be attributed to the fact that $C_6H_8O_7$ provides complete oxide removal and the HF increases the surface roughness compared to HCl. D_{it} is reduced, which can be detected by comparing the weak inversion region for both samples (Fig. 6.5(b)). Conversely, the HCl treated samples show vastly variable and higher negative Q_{IF} that is dependent of the position on the chip whereas the HF treated samples hardly show such dependence. Calculation of the SS at V_{DS} = -50 mV for several devices from sample M and sample N are shown in Fig. 6.5(c). The average SS of sample N is obviously better than that of sample M. Finally, as D_{it} is an effective parameter on g_m performance, a comparison between the two samples at V_{DS} = -500 mV is shown in Fig. 6(d). Sample N shows higher g_m values than sample M, indicating better surface quality, given structures are identical.

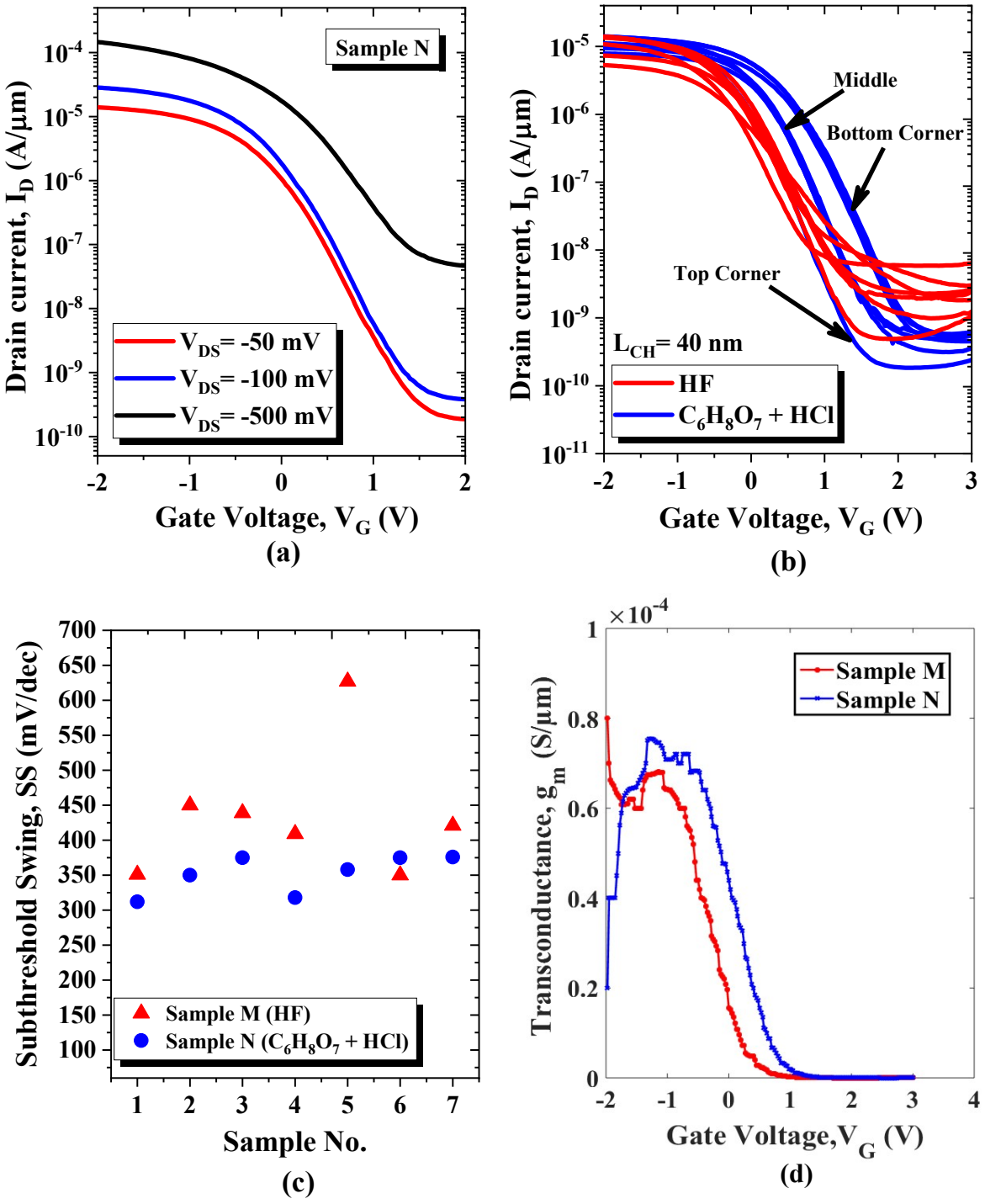


Fig. 6.5(a) Transfer characteristics of 40 nm channel p-PDBFET with $C_6H_8O_7$ and HCl surface treatment (Sample N), (b) transfer characteristics of 40 nm channel p-PDBFET with different treatment comparison (Sample M and Sample N), (c) SS comparison for devices from Sample N and M and (d) g_m comparison at V_{DS} = -500 mV.

Table 6.3 P-PDBFET of 40 nm channel length with different Ge surface treatment results comparison.

Parameter	Sample M	Sample N
SS (mV/dec) (V_{DS} = -50 mV)	351	318
SS (mV/dec) (V_{DS} = -100 mV)	366	327
SS (mV/dec) (V_{DS} = -500 mV)	511	473
I_{on}/I_{off} (V_{DS} = -50 mV)	$2.8x10^4$	$7.4x10^4$
I_{on}/I_{off} (V_{DS} = -100 mV)	$2.3x10^4$	$7.4x10^4$
I_{on}/I_{off} (V_{DS} = -500 mV)	$0.63x10^3$	$3.1x10^3$

6.3.2 Simulation Analysis: Effect of Reducing Al_2O_3 Gate Oxide Thickness

The aforementioned model (in Chapter 5) is adjusted in this study concerning doping concentration peak and the characteristic length of the Gaussian distribution L_{charc} assumed for the δ-layer, Q_F, Q_{IT} and Q_B that are technology dependent parameters to this set of samples. Simulations are focused on the L_{CH} = 40 nm and L_{CH} = 60 nm p-PDBEFT. In this work, the peak doping from simulation fitting is $N_D = 9x10^{18}$ cm^{-3} with characteristic length of L_{charc} = 5 nm. For the rest of the technological parameters above mentioned, the L_{CH} = 40 nm and L_{CH} = 60 nm p-PDBFET differed according to Table 6.4.

Table 6.4 Parameters used for simulating 40 nm and 60 nm p-PDBFETs.

Parameter	L_{CH} = 40 nm	L_{CH} = 60 nm
Q_{IF} (cm^{-2})	$-6.35x10^{12}$	$-7.18x10^{12}$
Q_{IT} (cm^{-2})	$5.45x10^{12}$	$3.18x10^{12}$
Q_B (cm^{-3})	$2x10^{17}$	$5.7x10^{16}$

Since the doping is assumed to be equal and the experimental results shows almost the same V_{th} although it is expected to be lower for L_{CH} = 40 nm, this indicates that the negative Q_{IF} are different. For Q_{IT}, the L_{CH} = 60 nm has longer length of intrinsic region with lower TAT rates hence the effective equivalent Q_{IT} is expected to be lower. Finally, for Q_B which is

considerably different, this can be due to higher crystal defects resulting from the MBE growth process. It could be also explained due to the higher TAT processes the L_{CH} = 40 nm suffers from due to stronger fields, that is modelled as higher effective bulk trap density experienced by carriers . Since L_{CH} = 40 nm has smaller intrinsic region, it is more affected by the residues of the doping profile tails of both δ-layer (n-type) and source and drain regions (p-type) behaving as defects or traps. The contribution of these defects is more effective in the L_{CH} = 40 nm p-PDBFET intrinsic regions with the higher fields existing. The simulated model shows excellent agreement with experimental work (see Fig. 6.6(a) and Fig. 6.6(b)).

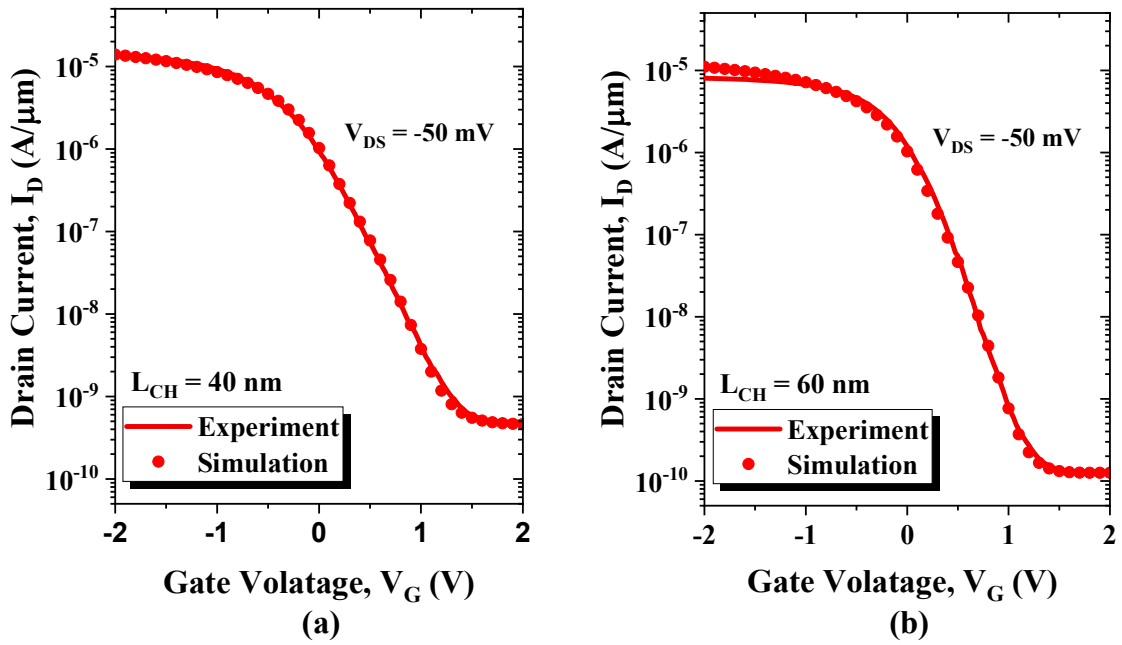


Fig. 6.6 Transfer characteristics of measured and simulated (a) 40 nm channel PDBFET and (b) 60 nm channel p-PDBFETs.

Based on the results obtained from these devices simulations, the gate oxide thickness is then reduced to T_{OX} = 3 nm of Al_2O_3 (equivalent oxide thickness EOT ~ 1.5 nm) and used for simulation. All other parameters remain unchanged. The attained results are demonstrated in Fig. 6.7. Further improvement mainly in the SS (predicted by eq. 2.6) and promising I_{on} increase is expected with the process of reducing T_{OX} due to improved gate control.

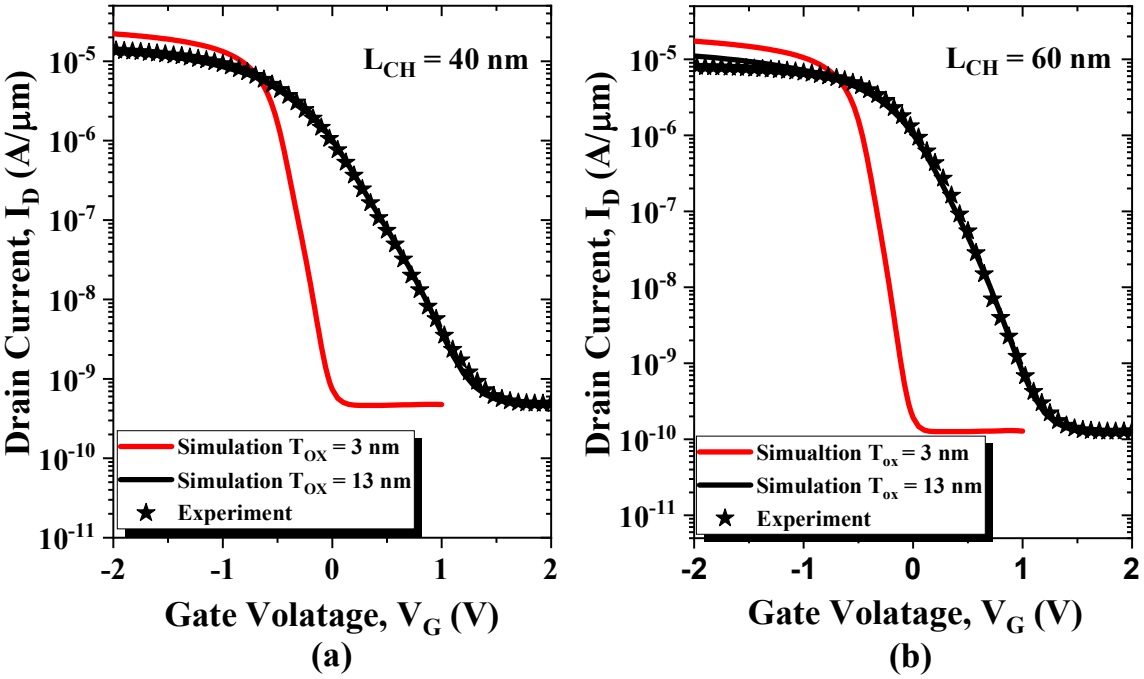


Fig. 6.7 Transfer characteristics of simulated p-PDBFET with Al_2O_3 gate oxide thickness T_{OX} = 3 nm for (a) 40 nm channel and (b) 60 nm channel.

The calculated SS values, at V_{DS} = - 50 mV, for the p-PDBFETs with L_{CH} = 40 nm and L_{CH} = 60 nm amount to SS = 126 mV/dec and SS = 103 mV/dec, respectively. (Fig. 6.7(a)), in spite of the relatively high $Q_{IT} \sim 10^{12}$ cm^{-2}. The reduction of T_{OX} can be done experimentally by adding a step of inserting a suitable isolation layer, to introduce a spacer [180]. In this material system, Hydrogen Silsesquioxane (HSQ) is an option to be introduced between the gate and the bottom region, hence the restriction on the oxide thickness T_{OX} for this design is released (Fig. 5.8(a-b))

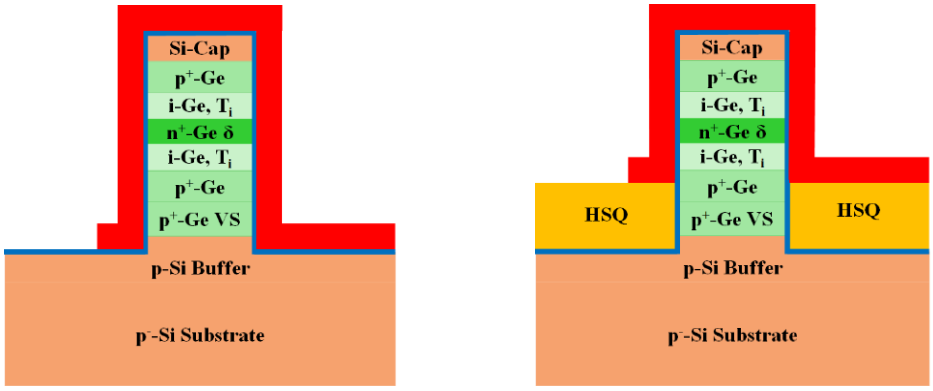


Fig. 6.8(a) The used design in this work and (b) the proposed modified design to release the restriction on the T_{OX} thickness.

In addition to improving SS, the addition of the isolation layer helps improve the high frequency performance of the device, where in vertical transistors, the absence of the self-aligned gate with source and drain introduces large overlap between the gate and the lower contact region (source or drain) that leads to severe loading of the device with $C_{Parasitic}$. If the bottom layer is used as drain, like in this case, also this layer helps to diminish GIDL effect as well.

Another interesting point is that the high I_{off} also limits the visibility of steeper SS. This could be achieved by reducing the size of the mesa by reducing A, hence reducing I_{off} as shown in Chapter 3 (Fig. 3.7). A method to imitate this size reduction effect and extrapolate it to ultimate scaling is to use low temperature measurements.

6.3.3 Low Temperature Measurement Performance

Leakage current is a concern because it increases power consumption and causes higher heat dissipation. Dark current can flow through the bulk or along the surface. The surface of Ge has high defect density and Fermi-level pinning, together with the fact that integration on Si results in imperfections in the crystal structure. Low temperature measurement can show the potential improvement in the devices by freezing out the traps and eliminating the parasitic effects. This in turn is analogous to the effect of ultimate scaling of the mesa size, reproducing a defect free device.

Fig. 6.9(a-c) show the effect of lowering the temperature on the transfer characteristics of the p-PDBFETs with different L_{CH} within the temperature range of T = 280 K down to T = 215 K. Figure 6.9(d) shows the increase of the I_{on}/I_{off} ratio with decreasing temperature. The improved parameter values reported in Table 6.5 are at T = 218 K – 215 K. The best-achieved ratio is for L_{CH} = 100 nm exceeds six orders of magnitude. The subthreshold values extracted achieved SS = 123-124 mV/dec for L_{CH} =100 nm and 60 nm respectively with EOT = 7 nm. The I_{on}/I_{off} ratio for L_{CH} = 60 nm and for L_{CH} =100 nm enhanced by almost 2 orders of magnitude. The enhancement in subthreshold behaviour is attributed to the frozen interface traps. I_{off} is decreased which can be explained as the effect of the freezing out of bulk and surface traps and subsequent reduction in TAT. Another factor that can be taken into consideration at relatively low temperatures, is the minor increase in the E_G [181] that can lead to a slightly reduced BTBT rates. It is worth mentioning that SS is also a function of temperature and the ideal subthreashold swing at such temperature is expected to reach SS ~ 43 mV/dec. For the L_{CH} = 40 nm p-PDBFET, I_{on}/I_{off} improved vastly reaching over 5 orders of magnitude

and the subthreshold swing substantially improved approaching SS = 153 mV/dec for EOT = 7 nm. The highest improvement in the I_{off} performance appears for L_{CH} = 40 nm p-PDBFET, where the equivalent Q_B predicted by simulations previously are significantly the highest. There is a V_{th} shift occurring with temperature reduction [182]. This could be explained by existence of DB at the Ge surface that act as trap-centers for charges of acceptor-type [131] [171] [176] and by decreasing the temperature, electrons lose their energy and are de-trapped from the acceptor centers leading to reduced equivalent negative charges resulting in this shift.

Table 6.5 Improvement of results on p-PDBFET under low temperature measurement.

Parameter	100 nm channel (218 K)	60 nm channel (218 K)	40 nm channel (215 K)
I_{on}/I_{off} (V_{DS} = -50 mV)	$1.5x10^6$	$5.6x10^5$	$1.6x10^5$
SS mV/dec (V_{DS} = -50 mV)	123	124	153

A comparison is demonstrated between the performance of the 100 nm channel p-PDBFET under low temperature measurement condition, where this represents a proposition to the expected free defect device behaviour, together with other fabricated trap free devices from literature in Table. 6.6. The obtained results represent very good performance for the relatively large sized devices. Table 6.7 shows a comparison between this work best devices performance and literature work devices that are ultimately scaled having more complicated designs and fabrication processes, including fully depleted channels with channel thickness of 10 nm and NW transistors of width of 20 nm.

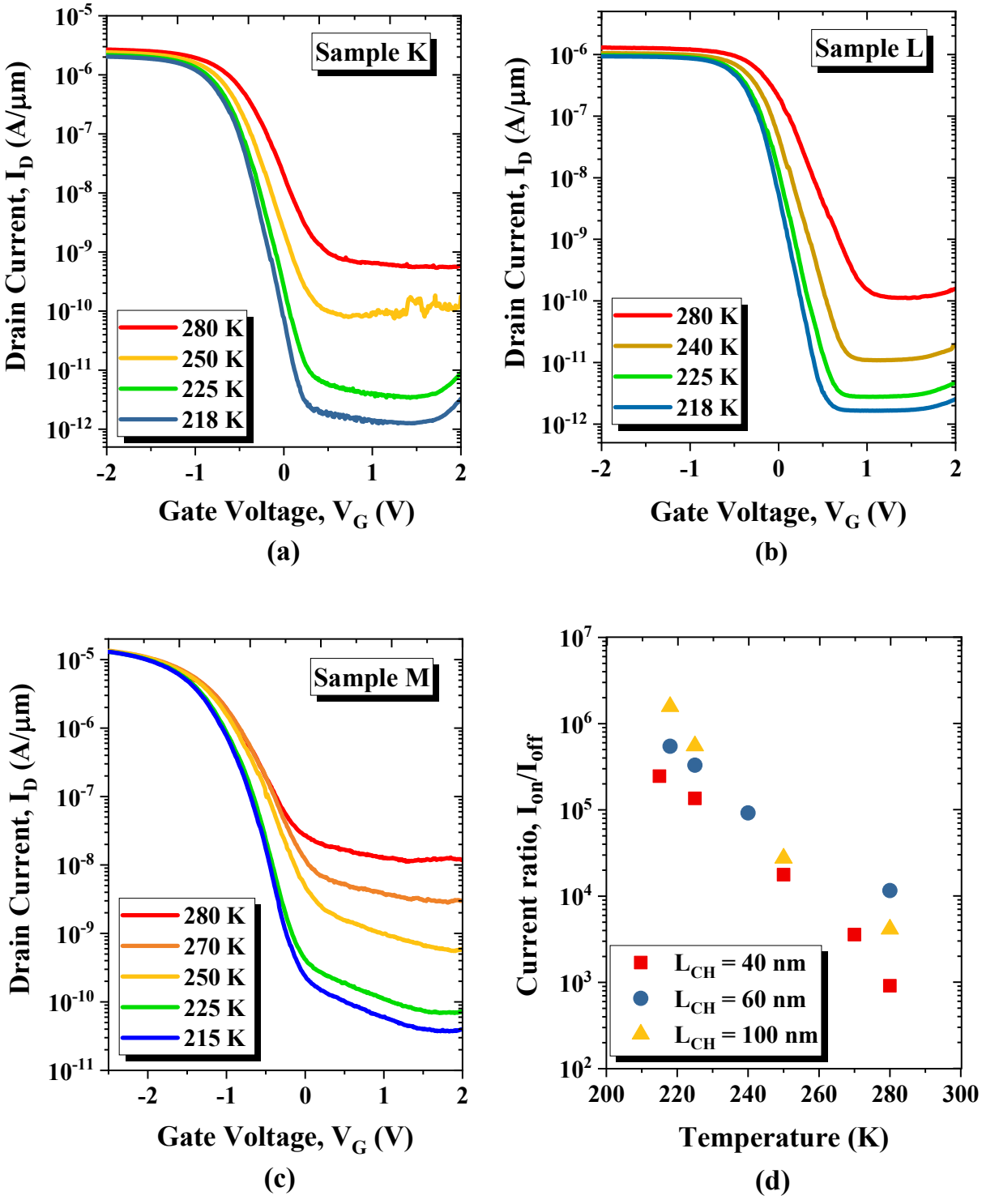


Fig. 6.9 Transfer characteristics of p-PDBFETs measured at different temperatures with (a) L_{CH} = 100 nm, (b) L_{CH} = 60 nm and (c) L_{CH} = 40 nm. (d) I_{on}/I_{off} versus temperature.

Table 6.6 Comparison between defect free Ge-based FETs from literature and low temperature measurement of this work for devices with L_{CH} = 100 nm.

Device	T_{OX}	L_{CH}	I_{on}/I_{off}	SS
Ref. [61] W_{FIN}= 52 nm	4 nm GeO_2 /3 nm Al_2O_3	183 nm	~10^5 (-500 mV)	130
Ref. [63] W_{NW}= 20 nm	GeO_2 /3 nm Al_2O_3	100 nm	>1x10^8 (-100 mV)	167
This work W_{mesa}= 1 µm	13.6 nm Al_2O_3	100 nm	>1x10^6 (-100 mV)	124

Table 6.7 Summary of comparison between results of Ge-based FETs from literature and this work.

	EOT nm	L_{CH} nm	I_{on}/I_{off} V_{DS} = -50 mV	I_{on}/I_{off} V_{DS} = -100 mV	I_{on}/I_{off} V_{DS} = -500 mV	SS mV/dec (V_{DS} = -50 mV)	I_{on} (V_{DS} = -50 mV)	I_{on} (V_{DS} = -500 mV)
Ref. [65] Tch=10 nm	4.5	50	2x10^4*	NA	6x10^4*	200	4*mA/mm	60*mA/mm
Ref. [64] W_{NW}= 20 nm	2	40	1x10^5*	NA	2.5x10^4*	107	135 µA/µm	135 µA/µm
Ref. [63] W_{NW}= 20 nm	GeO_2 /3 nm Al_2O_3	100	NA	>1x10^8	NA	167 (V_{DS} = -100 mV)	10*µA/µm	NA
Ref. [61] W_{NW}= 52 nm	5.5	183	NA	NA	~1x10^5	130 (V_{DS} = -500 mV)	NA	200*µA/µm
This Work W_{mesa}= 1 µm – 2 µm	7	40 60 100	7.4x10^4 6.3x10^4 8.2x10^4	7.4x10^4 7.5x10^4 1.3x10^5	3.1 x10^3 3.7x10^4 2.6x10^5	318 220 219	14 µA/µm 8.5 µA/µm 2.7 µA/µm	146 µA/µm 100 µA/µm 77 µA/µm
This Work Low Temp. Measurement	7	40 60 100	1.6x10^5 5.6x10^5 1.5x10^6	1.4x10^5 8x10^5 1.6 x10^6	NA NA NA	153 124 123	8 µA/µm 1 µA/µm 2 µA/µm	NA NA NA

*: values are estimated from literature.

Arrhenius plots for different transistors are shown in Fig. 6.10. The E_A extracted values are lower than the half of the energy band gap of Ge ($E_G/2$ = 330 meV). This indicates that this is TAT contribution having temperature dependence with $E_A < E_G/2$ [104] [183]. Hence, this result shows that device performance can be further improved by both reducing mesa size that

demolishes the bulk traps, together with further improved surface quality to reduce the surface traps.

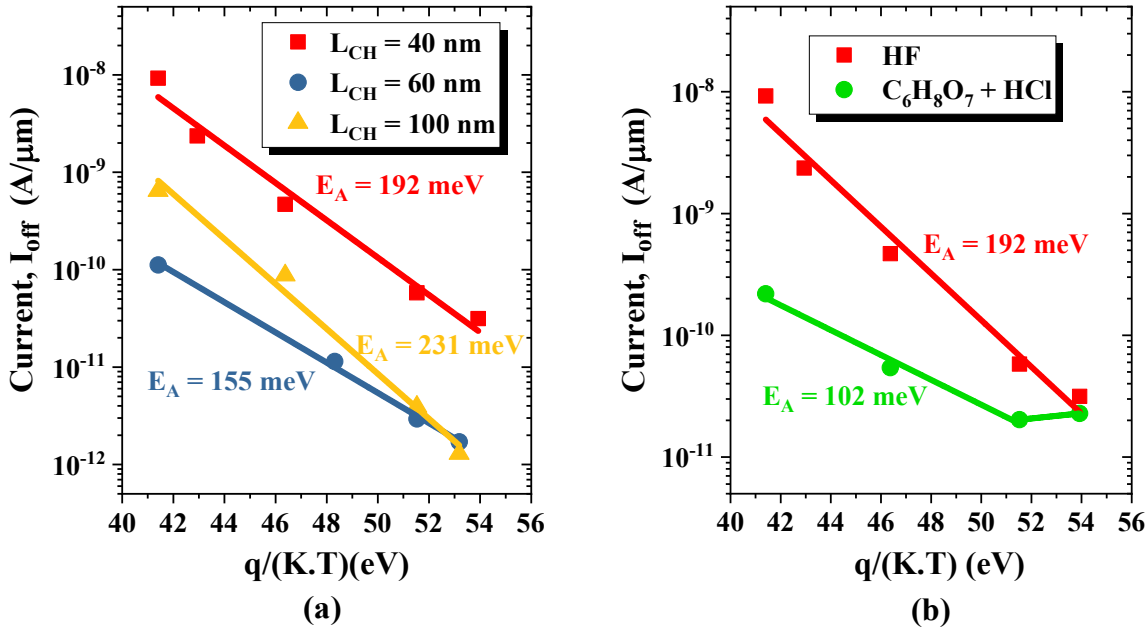


Fig. 6.10 Arrhenius plot for (a) L_{CH} = 100 nm, 60 nm and 40 nm and (b) L_{CH} = 40 nm with different surface treatment.

An interesting observation for sample N, with modified surface treatment, that improvement in the reduction of I_{off} saturated beyond 225 K, in fact a slight increase in the leakage current was observed. All other samples subjected to further lower temperatures experienced similar behaviour. After approaching temperature below 218 K (L_{CH} = 100 nm, L_{CH} = 60 nm) or 215 K (L_{CH} = 40 nm) according to the device L_{CH}, the improvement in performance did not continue on or even saturate referring to Si FET behaviour. In fact the performance started to degrade, demonstrating higher I_{off} and demonstrated poorer "strong inversion" performance especially in the L_{CH} = 100 nm leading eventually to a worsened SS (Fig. 6.11). This behaviour is usually due to trap density existence, which is clearly pronounced due to the specific distortion in the current curve in this region. A possible explanation is; as the temperature continues to decrease, alignment with different trap levels is enabled leading to further tunnelling processes to occur at the interface causing once more a higher leakage current.

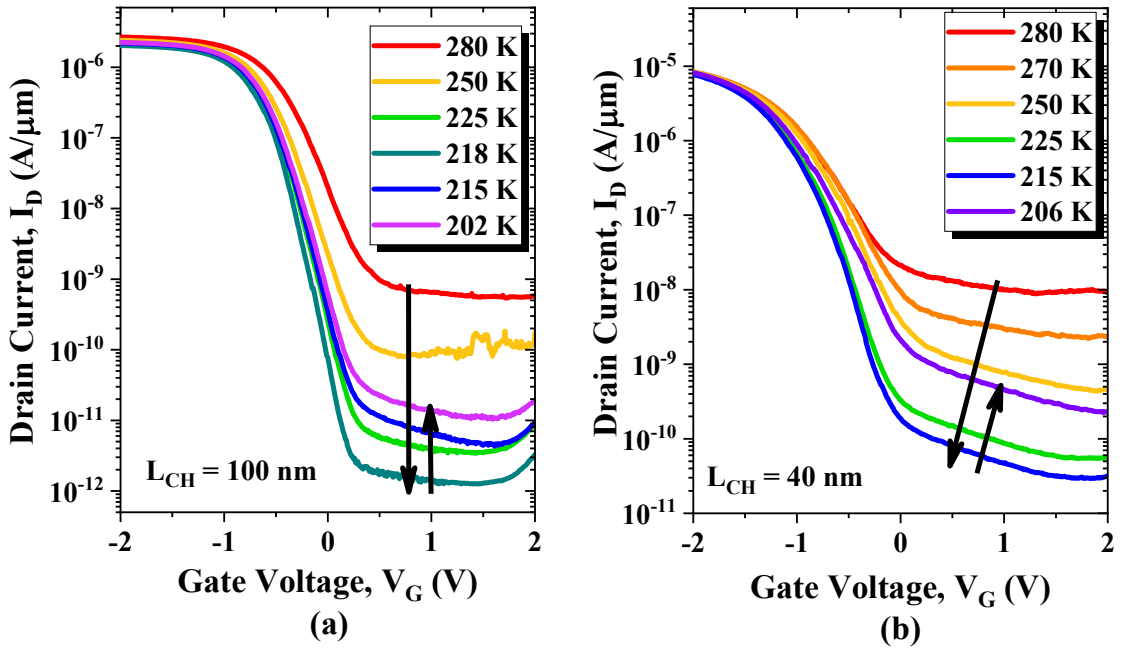


Fig. 6.11 Transfer characteristics development at lower temperatures for (a) L_{CH} = 100 nm and (b) L_{CH} = 40 nm.

In summary, results on high performance Ge-based p-PDBFETs were demonstrated and compared with literature Ge-based MOSFETs of comparable channel length and ultimate scaling designs. In spite of the large size of the fabricated devices and integration on Si, low leakage currents reaching sub-nanoampere were achieved for challenging channel lengths attributed to the usage of field tailoring concept realized by the planar doping of the channel. Influence of new surface treatment of Ge, T_{OX} reduction by simulation and low temperature measurements were investigated. All of these parameters proved to improve the behaviour, which illustrates the excellent potential performance of the fabricated devices in this work. As a conclusion, further improvement of the Ge-based PDBFET devices can be achieved in three directions. First, by improving the interface quality that is mainly dependent on the dry-etching process recipe and the treatment of the mesa surface. This includes the cleaning and the passivation processes prior to the gate-oxide deposition discussed in Chapter 4. Secondly, by improving the design using an insulating layer between the gate metal and the bottom contact allowing the scaling of the oxide thickness to reach the state of the art values resulting in substantial improvement in SS. Finally, ultimate size reduction of the mesa structure and improvement of crystal quality which can be performed by considering thicker VS layers.

Chapter 7: Ge/SiGeSn-Based Vertical Heterostructure P-PDBFET Model for Low Power Applications

The availability of high quality Ge/SiGeSn heterostructure epitaxial layers empowers the utilization of band gap engineering in Ge technology, enabling device design adjustments that can improve its performance. Based on the previously created model (using the experimental) work in Chapter 5, a modified design model was developed to overcome the complications causing high leakage currents in Ge-FET. In this chapter, a vertical heterostructure Ge/SiGeSn p-PDBFET design model is introduced for the first time. The inserted barrier using SiGeSn layer will in turn mitigate the high rates of BTBT that is an inherent property for Ge due to its relatively small E_G as well as TAT that occurs densely due to imperfections in crystal lattice and interface. The Ge/SiGeSn p-PDBFET model achieved low leakage current in the range of $I_{off} \sim$ pA/µm. The design is discussed in details; showing its effect on the characteristics of the device and the influence of the different parameters on the device performance. The design simulation results demonstrate the promising outcomes that qualifies this novel design to be employed in low power applications.

7.1 Effect of Introducing Heterostructure Layer into the P-PDBFET Channel

Ge FETs typically suffer from high I_{off} compared to Si, due to its relatively narrower E_G that results in elevated BTBT rates under the high electric field near the channel end. High TAT rates in Ge are still inevitable due to the challenging Ge/oxide interface quality together with the essential process of integration on Si producing threading dislocations and defects that act as trap-centers as well. These two factors contribute to the I_{off} of Ge, raising its static power consumption. Another existing mechanism that affects the V_{DS} performance is the impact ionization, leading to the deterioration of the device behaviour as seen in Chapter 5. An interesting solution for the Ge-based p-PDBFET high leakage current and SCEs, would be to manipulate the barrier of the charge carriers using channel engineering [182] [184] [185]. This can be done by introducing HL within the channel using a material of a larger E_G. In experiment, to implement a barrier structure within the Ge channel, $Ge/Si_xGe_{1-x-y}Sn_y$ heterostructures can be used [24] [25]. Figure 7.1 illustrates the p-PDBFET basic design (a) and the modification introduced in it (b).

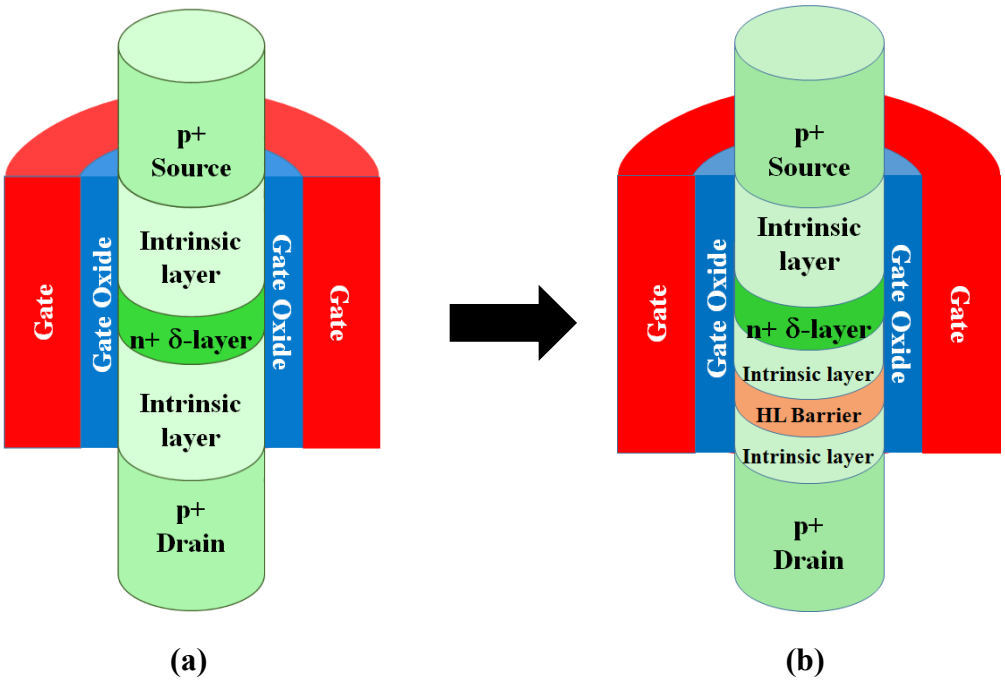


Fig. 7.1 (a) The basic design of the p-PDBFET and (b) the modified design by channel engineering through introducing a barrier structure within the p-PDBFET channel.

In principle, the introduction of HL may lead to added defects at the interface layers, which would contribute as well to the existing leakage current as result of added TAT processes. In order to avoid this problem, the $Si_xGe_{1-x-y}Sn_y$ alloy used is optimized to be lattice matched to Ge to avoid any additional interface concerns. The lattice constants for the three elements Si, Ge and Sn are $a_{Si} = 5.431$ A°, $a_{Ge} = 5.646$ A° and $a_{Sn} = 6.489$ A° respectively. To achieve lattice matching between Ge and the $Si_xGe_{1-x-y}Sn_y$ alloy, the ratio of the content of Si (x) to content of Sn (y) in the alloy should be $\frac{x}{y} \sim 3.67$. All the compositions of alloys satisfying this relation have the same lattice constant as Ge. Hence, throughout the calculation process, the layers are assumed to be unstrained.

Calculations for E_G of the ternary alloy $Si_xGe_{1-x-y}Sn_y$ and the expected band alignment with the E_G of Ge were done based on a quadratic interpolation of the E_G of the ternary alloy materials (eq. 7.1) [25], with parameters given in Table 6.1 and Jaros approach to approximate the band alignment between Ge and the $Si_xGe_{1-x-y}Sn_y$ ternary alloy. Furthermore, the validity of Vegard's law for the lattice constants of the $Si_xGe_{1-x-y}Sn_y$ alloys was assumed.

$$E_G(x,y) = E_G^{Ge}(1-x-y) + E_G^{Si}x + E_G^{Sn}y - b^{SiGe}x(1-x-y) - b^{GeSn}(1-x-y)y - b^{SiSn}xy \qquad \text{eq. 7.1}$$

Table 7.1 The used parameters for calculating the energy band gap of $Si_xGe_{1-x-y}Sn_y$ alloy.

	Si	Ge	α-Sn	b^{SiGe}	b^{GeSn}	b^{SiSn}
Γ (eV)	3.40 [186]	0.80 [186]	-0.413 [187]	0.21 [188]	2.46 [187]	13.2 [188]
L (eV)	2.00 [186]	0.66 [186]	0.006 [187]	0.169 [188]	1.03 [187]	0.925 [188]
X (eV)	1.12 [186]	0.85 [186]	0.910 [189]	0.108 [189]	0.1 [189]	0.772 [189]

In this work, we choose four diverse alloy compositions that have been experimentally grown and calibrated at IHT lab, using MBE technique, showing high quality layer results. These Si and Sn compositions sweep different content values of x and y in the alloy, keeping $\frac{x}{y}$ constant. The aim is to discover the effect of the resulting E_G values, which are relatively larger, as well as the band alignment type and alignment percentage on the performance. The band alignment is a very important factor here as it is responsible for forming the barrier type and heights for the different charge carriers inside the channel subsequently. Calculation results of the energy band alignment including conduction band offset (ΔE_C) and valence band offset (ΔE_V) and the resultant E_G for different combinations of the ternary alloy $Si_xGe_{1-x-y}Sn_y$ (according to Table 7.1) are shown in Table 7.2. The calculations demonstrate a type-I band alignment with an increasing portion of the energy band gap offset (ΔE_G) lying within ΔE_V as the concentration of Si and consequently Sn is increased.

A compromise should be made between the used concentration of Si and that of Sn in the ternary alloy according to these results. The Si concentration should be maximized such that the effective barrier height in CB and VB is the largest (in this case ΔE_G in total). However, Sn should be chosen to be low enough to avoid the transition of the Γ-band being the minimum E_C. In principle, the Sn concentration in the alloy affects the band gap alignment-type. The higher the content of Sn, the lower the Γ-band edge becomes. Beyond the concentration of Si of x = 0.49 (y = 0.13). The Γ-band edge becomes lower than the X-band edge and the overall E_G starts to decrease again leading to a lower ΔE_G. Furthermore, as the Sn content is increased to y = 0.15 and beyond, the E_C of the $Si_xGe_{1-x-y}Sn_y$ alloy falls below the L-band edge of Ge and the alignment type is expected to change to type- II, where a well is formed in the CB within the SiGeSn layer. As a result, the Sn concentration for this design should be kept below x = 0.13 to keep the ΔE_G maximized.

Table 7.2 Calculations of energy band alignment and resulting energy gap.

Alloy Composition $Si_xGe_{1-x-y}Sn_y$	Energy Band*	Substrate*	Layer*	Calculated E_G	ΔE_G	ΔE_C	Alginment in CB
$Si_{0.18}Ge_{0.77}Sn_{0.05}$	Γ	0.89670	1.00327	E_{Gmin} ~ 0.8 eV	140 meV	79 meV	~ 60%
	L	0.75670	0.83564				
	X001	0.94670	0.91438				
	X010	0.94670	0.91438				
	hh	0.09667	0.03851				
	lh	0.09667	0.03851				
	so	-0.19333	-0.23271				
Alloy Composition $Si_xGe_{1-x-y}Sn_y$	Energy Band*	Substrate*	Layer*	Calculated E_G	ΔE_G	ΔE_C	Alginment in CB
$Si_{0.73}Ge_{0.53}Sn_{0.10}$	Γ	0.89670	0.9555	E_{Gmin} ~ 0.9 eV	240 meV	119 meV	~ 50%
	L	0.75670	0.9432				
	X001	0.94670	0.87564				
	X010	0.94670	0.87564				
	hh	0.09667	-0.02527				
	lh	0.09667	-0.02527				
	so	-0.19333	-0.27525				
Alloy Composition $Si_xGe_{1-x-y}Sn_y$	Energy Band*	Substrate*	Layer*	Calculated E_G	ΔE_G	ΔE_C	Alginment in CB
$Si_{0.49}Ge_{0.38}Sn_{0.13}$	Γ	0.89670	0.84796	E_{Gmin} ~ 0.92 eV	255 meV	91 meV	~ 40%
	L	0.75670	1.02343				
	X001	0.94670	0.84902				
	X010	0.94670	0.84902				
	hh	0.09667	-0.06691				
	lh	0.09667	-0.06691				
	so	-0.19333	-0.30267				
Alloy Composition $Si_xGe_{1-x-y}Sn_y$	Energy Band*	Substrate*	Layer*	Calculated E_G	ΔE_G	ΔE_C	Alginment in CB
$Si_{0.55}Ge_{0.30}Sn_{0.15}$	Γ	0.89670	0.7303	E_{Gmin} ~ 0.81 eV	150 meV	-26 meV	---
	L	0.75670	1.06495				
	X001	0.94670	0.83812				
	X010	0.94670	0.83812				
	hh	0.09667	-0.08343				
	lh	0.09667	-0.08343				
	so	-0.19333	-0.31463				

* Energy band levels calculations were conducted by Torsten Wendav at Institute for Physics, Humboldt-Universität zu Berlin.

Beyond this stage, the CB barrier ΔE_C continues to decrease as well as the overall E_G of $Si_xGe_{1-x-y}Sn_y$ until reaching a point where a well is created in the CB instead. This is a crucial point because ΔE_C is a very effective parameter in this design for suppressing I_{off} (Fig. 7.2) and

is highly dependent on the bowing parameters. Another important point is the variation of the alloy composition effect on the I_{on}. As the Si percentage in the alloy is increased between x = 0.37 and x = 0.49 (and Sn correspondingly), the amount of the aligned ΔE_G inside CB starts to decrease and is compensated with an increase in the VB (ΔE_V increases). At a certain point this increase starts to affect the I_{on} significantly. This point depends mainly on the technological parameters. An optimum value of the alloy composition should be determined experimentally. Fig. 7.2 shows the effect of the energy gap difference and alignment on the barrier created for the two carrier types. Table 7.2 shows the chosen alloy compositions and the corresponding calculated minimum E_G.

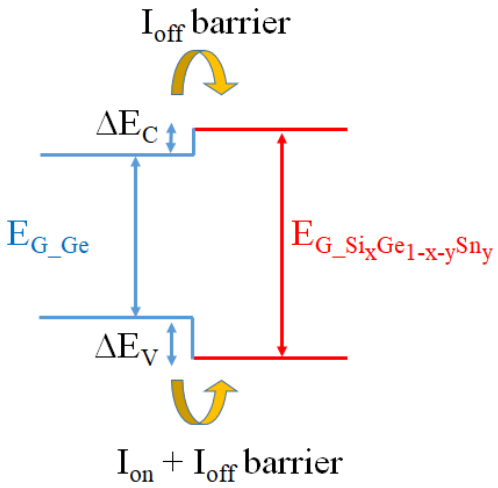


Fig. 7.2 Schematic for E_G alignment and barriers created in each band.

Based on the calculations in Table 7.2, the plotted results in Fig. 7.3 illustrate the resulting band alignment for each carrier type and its height. The first alloy concentration $Si_{0.18}Ge_{0.77}Sn_{0.05}$ gives $E_G \approx 0.8$ eV. with $\Delta E_C \approx 79$ meV. (Fig. 7.3 (a)). The second composition $Si_{0.37}Ge_{0.53}Sn_{0.10}$ gives $E_G \approx 0.9$ eV. with $\Delta E_C \approx 119$ meV. (Fig. 7.3 (b)). Here ΔE_C is having the highest value of all chosen alloy values. The third alloy $Si_{0.49}Ge_{0.38}Sn_{0.13}$ gives $E_G \approx 0.92$ eV. with $\Delta E_C \approx 91$ meV. (Fig. 7.3(c)). At this stage ΔE_G is almost maximized. The last composition $Si_{0.55}Ge_{0.3}Sn_{0.15}$ produces a quantum well in the CB of the alloy region rather than a barrier (Fig. 7.3(d)) with $\Delta E_C \approx -26$ meV. This alloy composition is not suitable for this design and should be avoided.

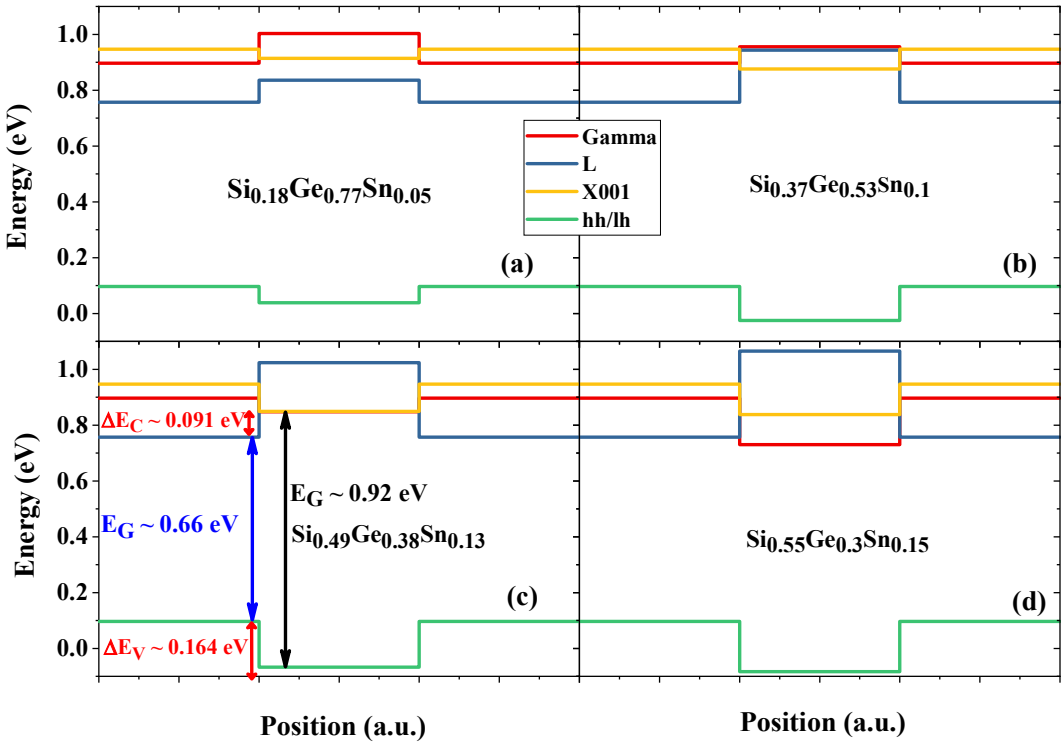
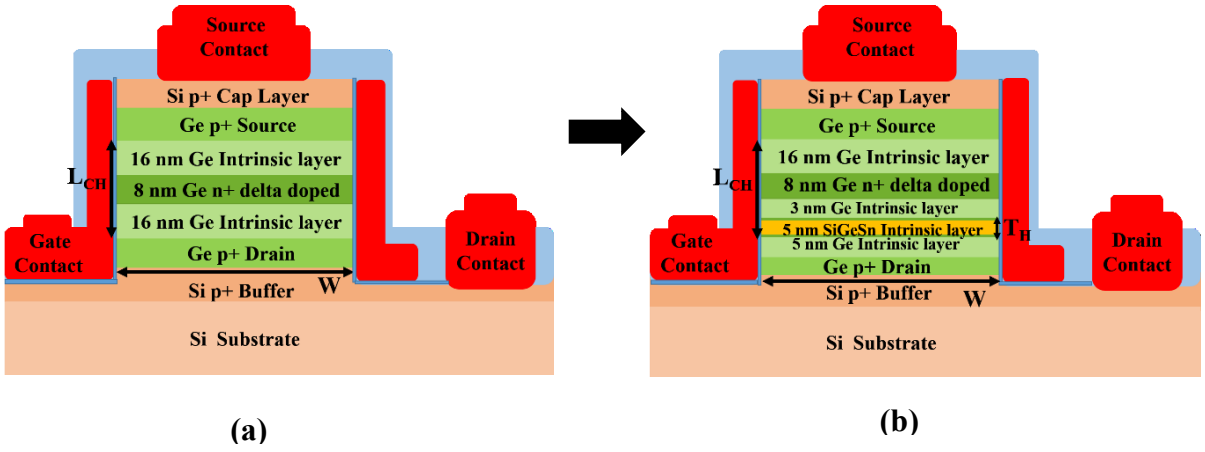


Fig. 7.3 Energy band alignment calculations for different $Si_xGe_{1-x-y}Sn_y$ alloy composition: (a) $Si_{0.18}Ge_{0.77}Sn_{0.05}$, (b) $Si_{0.37}Ge_{0.52}Sn_{0.10}$, (c) $Si_{0.49}Ge_{0.38}Sn_{0.13}$ and (d) $Si_{0.55}Ge_{0.3}Sn_{0.15}$.

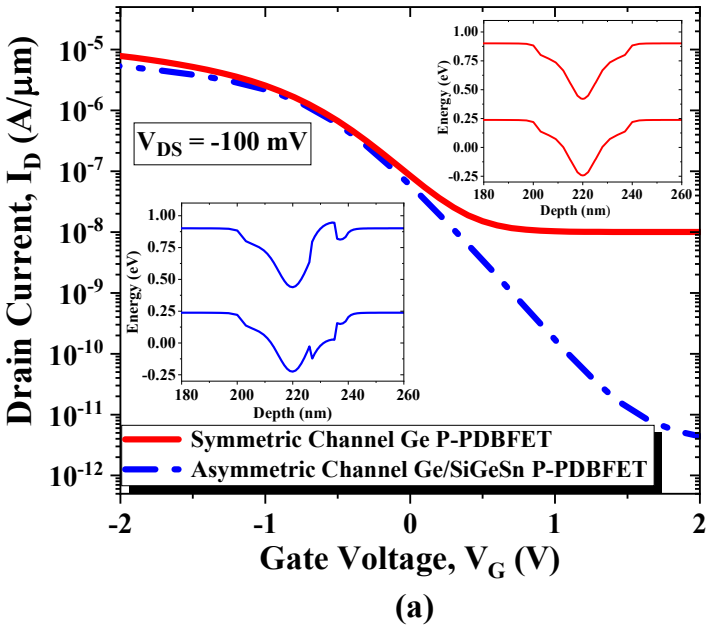
In this work, the alloy ratio of $Si_{0.49}Ge_{0.38}Sn_{0.13}$ is chosen, to maximize the ΔE_G while still maintaining considerable value for ΔE_C. The heterostructure thickness (T_H) chosen for the design is T_H = 8 nm. The heterosturcture interface is designed to be five nanometre away from the drain and the δ-doped layer is at the middle, resulting in an asymmetric Ge/$Si_xGe_{1-x-y}Sn_y$ p-PDBFET heterostructure channel. The study was started by applying the modification in the design to the initial basic model (in Chapter 5) with doping concentration of the δ-doped layer used $N_D = 3x10^{19}$ cm^{-3}. The heterostructure is added as a segment within the channel. Fig. 7.4 illustrates the proposed channel engineered design.



(a) **(b)**

Fig. 7.4(a) 2D-schematic of the Ge-based p-PDBFET structure used in experiment and simulation fitting and (b) 2D-schematic design of the proposed model structure of the asymmetric Ge/$Si_xGe_{1-x-y}Sn_y$ heterostructure channel p-PDBFET.

The transfer characteristics of simulated p-PDBFET with asymmetric Ge/ $Si_{0.49}Ge_{0.38}Sn_{0.13}$ heterostructure channel (Fig. 7.5(a)) predict a noticeable improvement in the I_{off} behaviour and subsequently a reduced subthreshold swing from SS = 625 mV/dec to SS = 445 mV/dec. Such low I_{off} enables power consumption reduction and opens the chances for energy efficient device applications. The output characteristics comparison (Fig. 7.5(b)) shows a significant development in the saturation behaviour with the presence of the asymmetric Ge/ $Si_{0.49}Ge_{0.38}Sn_{0.13}$ heterostructure channel. This improvement can be attributed to the effect of the heterostructure barrier on the BTBT processes occurring at relatively high V_{DS} at the reverse bias junction near the drain region. Calculations of BTBT rates for both channel designs (symmetric and asymmetric) at relatively high V_{DS} = -0.75 V for both on and off states are shown in Fig. 7.6. It is obvious that the rates of the BTBT of electrons and holes together with the region width within which the BTBT events take place are reduced significantly due to the modification in the design.



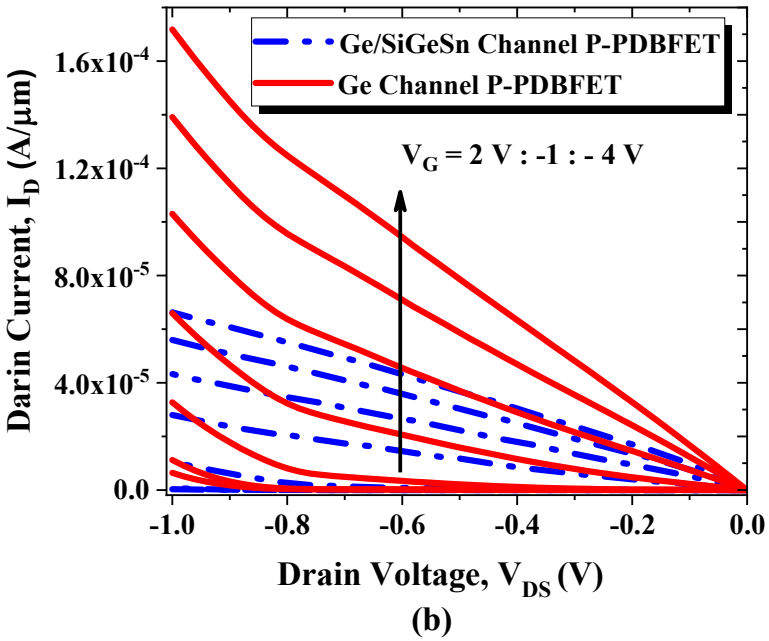


Fig. 7.5 Simulated characteristics of the p-PDBFET with symmetric Ge channel and asymmetric Ge/$_{SixGe1-x-y}Sn_y$ heterostructure channel (a) transfer characteristics and (b) output characteristics.

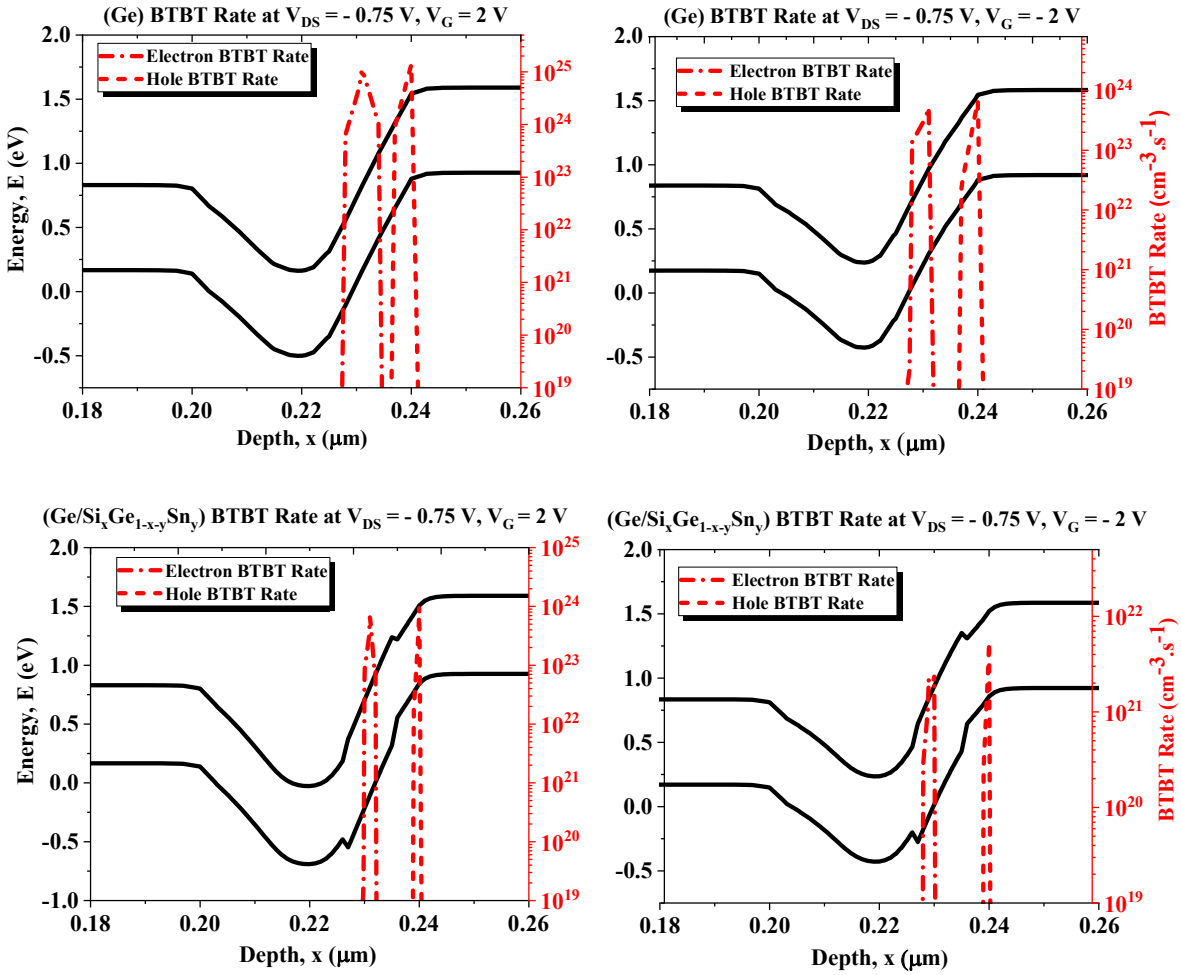


Fig. 7.6 BTBT rates for symmetric Ge channel and asymmetric $Ge/Si_xGe_{1-x-y}Sn_y$ heterostructure channel in on-state and off-states.

7.2 Effect of the Position of the Heterostructure Layer inside the Channel

To study the effect of the heterostructure position within the channel and determine its optimum position, four structures were designed and simulated (Figure 7.7 (a-d)). One with both the δ-doped layer and the HL being in the middle of the channel (a). The second with the HL in the middle and the δ-doped layer centerd at nine nanometre from source (top contact) (b), the third with the HL centerd at nine nanometre from source and the δ-doped layer centerd at the middle (c). Finally, with the HL centerd at nine nanometre from the drain (bottom contact) and the δ-doped layer centerd in the middle (d). Simulations demonstrate that the usage of the HL within the δ-doped layer in fact degrades the behaviour, i.e. I_{on} is slightly reduced and I_{off} remains unaffected (Fig. 7.8(a)). This is due to the fact that the barrier introduced by the heterostructure is affected by the energy bending resulting from the δ-doping layer (Fig. 7.8(b))

where the δ-doping can control the interface properties and tune the band offsets as discussed in Chapter 2 [76] [77].

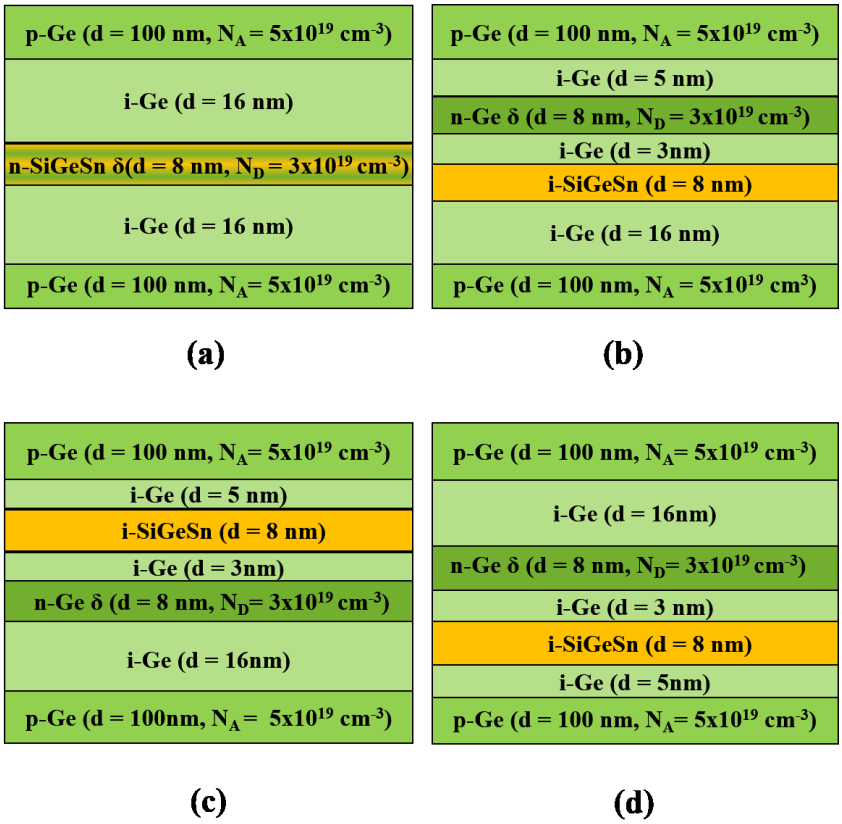


Fig. 7.7(a) to (d) Simulated layer structures with different relative positions of the heterostructure layer and the δ-doped layer.

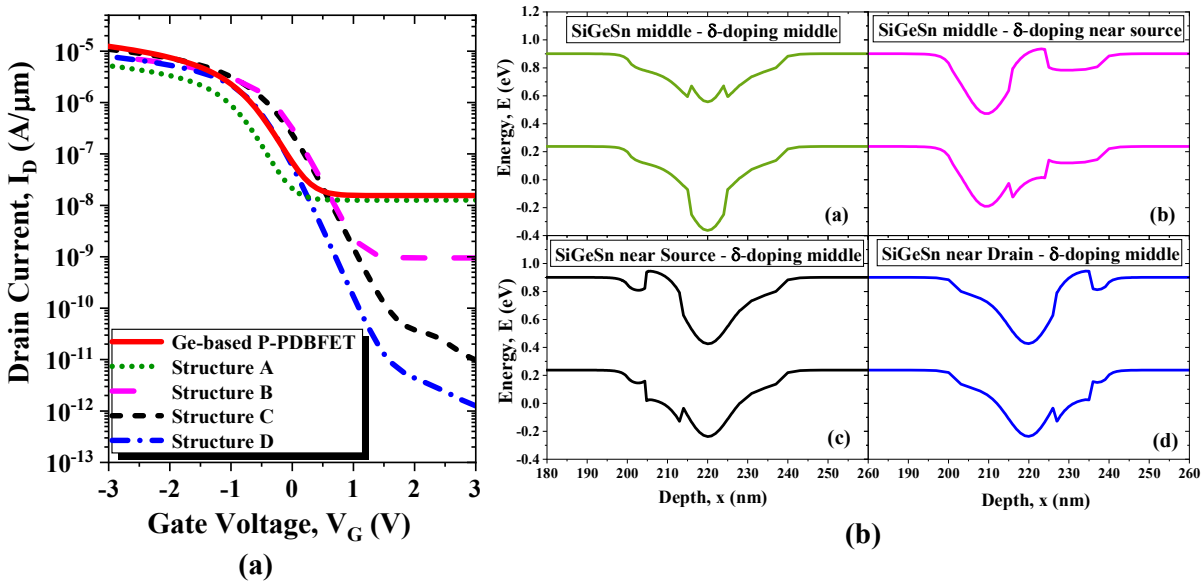


Fig. 7.8(a) Comparison of the simulated transfer characteristics of symmetric Ge channel and asymmetric Ge/ $Si_xGe_{1-x-y}Sn_y$ with the heterostructure at different positions within the channel (V_{DS} = -100 mV) and (b) the energy band diagram corresponding for each case at zero bias.

The second design shows a relatively decreased $I_{off.}$ The third structure provides an effectively reduced leakage current behaviour, where the heterostructure barrier near the source prevents collection of leaked carriers (Fig. 7.8(b)). The fourth structure demonstrates best suppression for I_{off}, which comes with placing the HL close to the drain region. Here this result clearly shows that BTBT, besides TAT, at the drain-end of the channel is a main cause of excessive off-state current.

7.3 Positional Dependence of the Heterostructure Layer between the Centre of the Channel and the Drain on the Off-Current

Based on the previous results, it can be deduced that there is an optimum position for the HL between the drain and the δ-doping position (structure d). A set of simulations were carried out while the heterostructure was shifted by an increment of one nanometre from the drain per each simulation (Fig. 7.9). The corresponding barrier created at different position stages is shown in Fig. 7.9(b). Simulation results confirm that, when the heterostructure is moved away from the drain the improvement in the I_{off} suppression progresses, where the effective barrier seen by carriers is maximized, until the heterostructure starts to approach the Gaussian doping curve of the doped layer. As it approaches a distance of less than three nanometre from the middle of the channel, the influence of the heterostructure starts to be ineffective due to the vanishing of the energy barrier created by the HL inside the δ-doped layer band bending and the behaviour starts to approach that of structure in Fig. 7.7 (a).

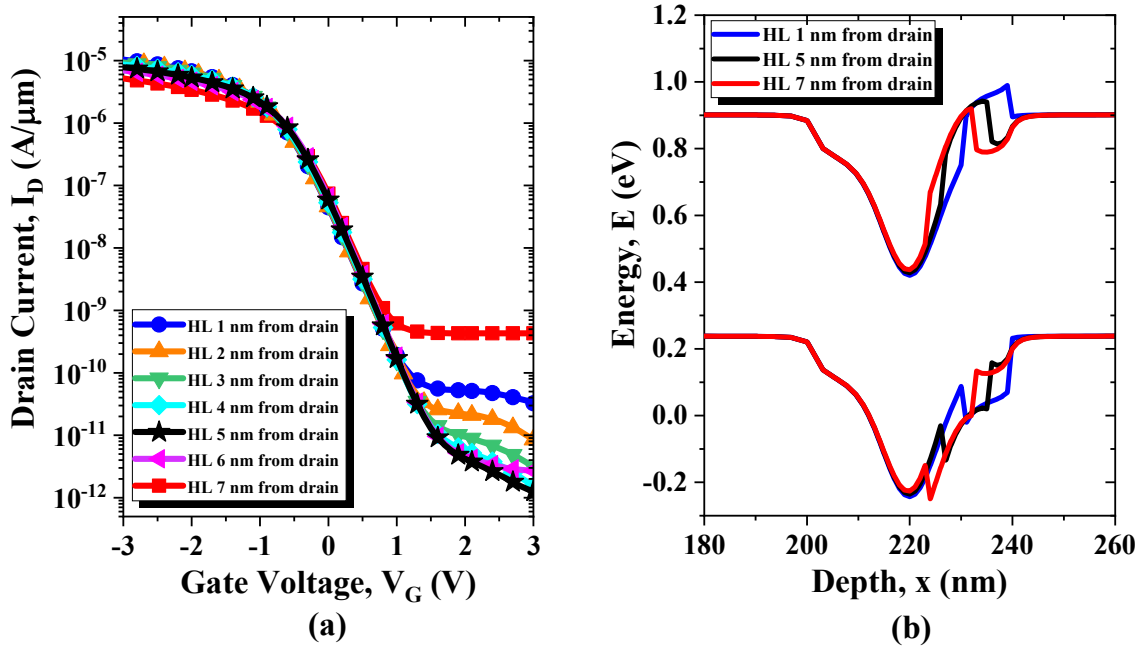


Fig. 7.9 (a) The dependence of the performance on the variation of the precise position of the HL from the drain and (b) the energy band diagram showing the effective barrier shape at different positions.

7.4 Effect of the δ-Doping Concentration in the Presence of the Heterostructure Layer

In this section, the investigation of the effect of changing the channel doping on the devices is applied, while keeping the alloy composition and position fixed as was introduced in Fig. 7.4 and varying the parameters of the δ-doping layer according to samples simulated in Chapter 5. In Fig. 7.10(a), results show that for the lowest doping concentration (Sample A) the improvement is almost negligible. This can be due to the insufficient barrier represented by the δ- doping layer that allows the carriers to freely pass thermionically and the band bending is weak (Fig. 7.10(b)), hence the tunnelling component is very small. For sample with middle doping concentration (Sample B), a significant improvement can be achieved in the I_{off} behaviour. For the highest doping sample (Sample C), the best improvement is accomplished since the fields and the band bending are maximized and the BTBT and TAT rates are highest (Fig. 7.10(b)). Hence, the effect of the heterostructure enhancement is dependent on the doping concentration as shown in Fig. 7.10. There would be an optimum doping concentration for such design (for a given $Si_xGe_{1-x-y}Sn_y$ alloy composition) that allows both best SS together with keeping I_{off} as low as possible. If the device trap density and interface quality are improved, lower doping concentrations are needed to obtain this optimum behaviour. In this case, the $Si_xGe_{1-x-y}Sn_y$ alloy composition would need to be optimized as well.

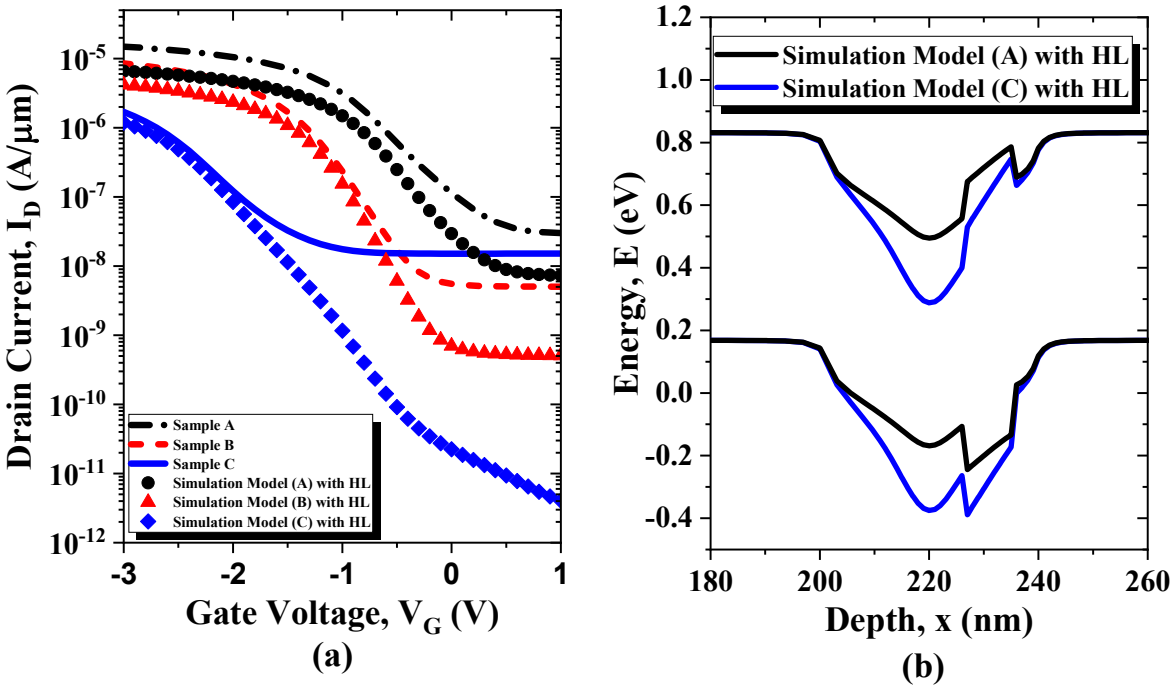


Fig. 7.10 The effect of the modified model design on the simulation fitted results of the fabricated devices (a) transfer characteristics and (b) the corresponding energy band diagram.

7.5 Effect of the Alloy Composition $Si_xGe_{1-x-y}Sn_y$

To stress more on the purpose of the choice of this alloy composition of $Si_{0.49}Ge_{0.38}Sn_{0.13}$ for the experimental results , a study about the effect of the alloy composition on the fabricated samples simulation results behaviour was performed. The calculated E_G values in Table 7.2 and alignments in the band structure resulting from the several compositions chosen for $Si_xGe_{1-x-y}Sn_y$ alloy ($Si_{0.18}Ge_{0.77}Sn_{0.05}$ (E_G = 0.8 eV), $Si_{0.37}Ge_{0.53}Sn_{0.1}$($E_G$ = 0.9 eV) and $Si_{0.49}Ge_{0.38}Sn_{0.13}$ (E_G = 0.92 eV)) were used (Fig. 7.11(a)). In Fig. 7.11(b) transfer characteristics are presented for the different alloy compositions, demonstrating that for larger ΔE_G, producing a higher barrier of ΔE_C and ΔE_V in total, the stronger the impact on the I_{off} reduction. It is worth noting that for improved interface quality and size scaled devices, the optimum alloy composition might differ depending on the technological parameters.

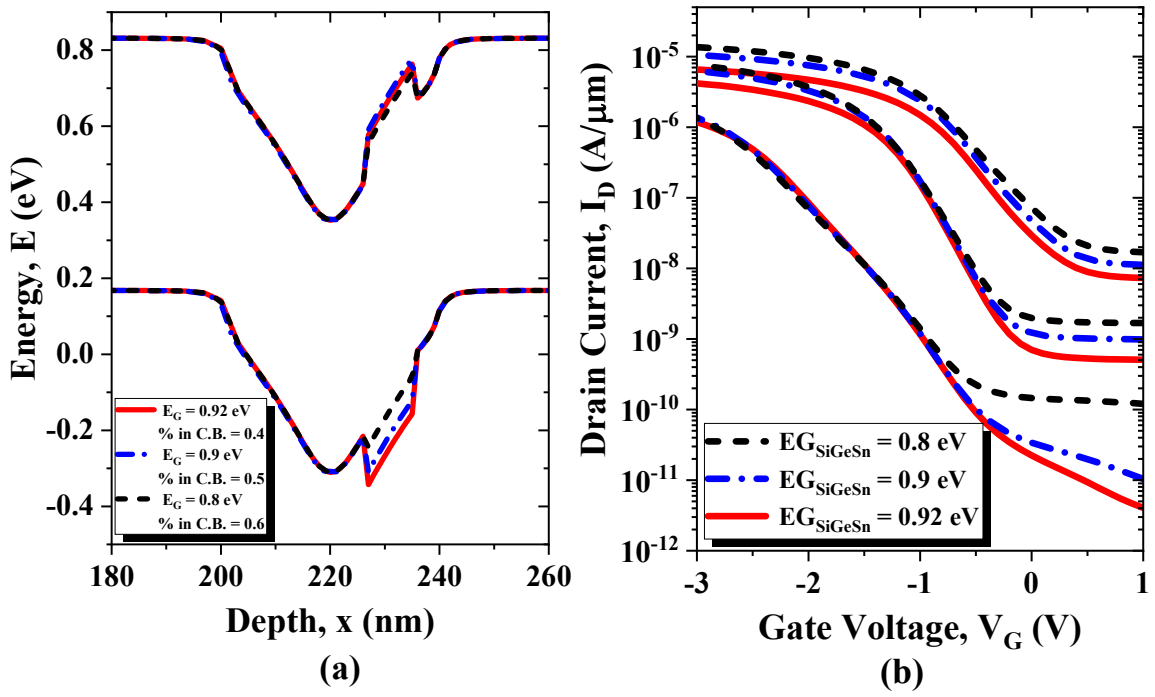


Fig. 7.11(a) Energy band structure for different $Si_xGe_{1-x-y}Sn_y$ alloy compositions. (b) Performance variation dependence on the δ-doping concentration with the usage of HL.

7.6 Effect of the Heterostructure Layer $Si_xGe_{1-x-y}Sn_y$ on High Performance Devices with Different Channel Lengths

In this section, we represent the effect of the heterostructure design on the p-PDBFET with enhanced growth recipe presented in Chapter 6, with reduced bulk and interface traps. Fig. 7.12(a) demonstrates results confirming that there is still a huge impact on the I_{off} of about 2

orders of magnitude reduction for L_{CH} = 40 nm using HL of thickness of T_H = 8 nm placed at five nanometre away from the drain (as in Fig. 7.4). For L_{CH} = 60 nm, the same HL thickness and position gives a limited effect but by increasing the HL thickness and relative position, the reduction in the I_{off} is vastly improved. In this case, the ratio of T_H to the intrinsic region is similar to the case of L_{CH} = 40 nm p-PDBEFT, i.e. For L_{CH} = 60 nm p-PDBEFT, T_H = 13 nm centerd at a position of ten nanometre from the drain. In addition, there is an effect on the I_{on} as well due to the usage of HL. This influence appears clearer in these set of samples because the effective doping is lower than the doping used before. It is expected that as the effective doping of the barrier (barrier height through built-in voltage) is increased, the effect of the heterostructure in turn have less impact on the I_{on}.

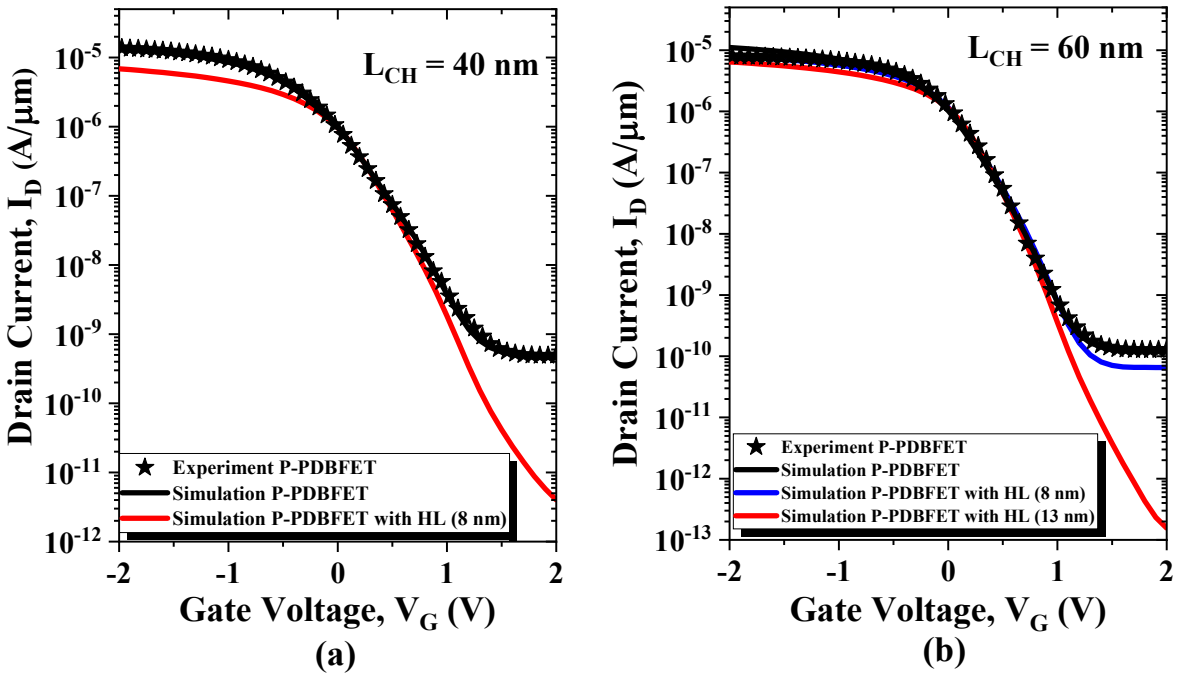


Fig. 7.12 Effect of the proposed model on the fitted simulation data of the fabricated Ge-based p-PDBFETof different channel lengths of (a) 40nm channel and (b) 60 nm channel.

Nevertheless, the loss in the I_{on} is small compared to the improvements achieved in lowering I_{off}, besides the improvement in the SS achieved. This design has proven that it has a quite optimistic performance for Ge based transistors, with different technological parameters and designs.

To sum up, the simulation model implemented for the Ge-based p-PDBFET experimental results was used to explore the effect of the proposed design modification using a HL of $Si_xGe_{1-x-y}Sn_y$ within Ge-based channel to improve the performance by combining both planar doping and heterostructure concept for the first time. In this modified design the origin of high leakage currents in Ge, BTBT and TAT currents, were mainly addressed. The results obtained demonstrated powerful diminishing of I_{off} of the diverse devices with different technology parameters, providing very promising performance for application in low power devices. The design relaxes the restriction of the necessity of existence of an ideal interface between Ge and the gate oxide as well as the restraint of perfect crystalline quality growth of Ge on Si.

For future work, by applying the proposed possible improvement on the current device quality to possess relatively lower bulk traps and better surface quality, the required alloy composition should be carefully tuned to optimize device performance. Such interdependency of the various parameters available to optimize the heterostructure device suggests the following for performance improvement: first, the reduction of the existing bulk traps density through size reduction. Second, the improvement of the quality of the Ge/oxide interface as possible by improving the mesa dry etching recipe to reduce surface roughness and then applying convenient cleaning and passivation steps to the Ge surface prior to oxide deposition (several methods shown in the coming chapter). Next, the optimization of δ-doping layer is set. At this stage, after reducing the trap density of different types, lower doping concentrations for the δ-layer would then be needed in order to boost the device performance, allowing for lower SS. In turn, the $Si_xGe_{1-x-y}Sn_y$ composition is then determined, where the optimum composition determination would be to maximize ΔE_C for achieving minimum I_{off}, rather than aiming at maximizing the E_G of the ternary alloy $Si_xGe_{1-x-y}Sn_y$ as was intended in this work due to existence of high trap density.

Conclusion and Future Work

Ge has the highest hole mobility among all semiconductors which makes it an excellent candidate for p-channel transistors, nevertheless its low E_G, high ϵ_r and poor interface with oxide makes Ge-FETs vulnerable to SCEs and high leakage currents. In this work, the aim is to study the suitability of applying the concept of the PDBFET device structure to Ge-based p-channel FET, with its mostly undoped channel structure in a vertical transistor scheme allowing for GAA design and enhanced electrostatic control. In Chapter 3, the application of the PDB concept was applied to Ge-based FET devices and the implementation of successful Ge-based p-PDBFET for the first time was accomplished. The design parameters (N_D, d, position of the barrier, surface treatment) were investigated showing presence of optimum doping scheme for the PDBFET design structure. Analysis of the electric characterization indicated the existence of primarily four observed complications in the performance of the initial design, the high leakage current, the loss of gate control at high V_{DS}, non-saturating behaviour of the output characteristics of the device and the relatively high SS with size reduction. Further examination lead to the fact that high leakage current is caused by high defect density that can be effectively reduced by size reduction and that the reason for the gate loss of control at high V_{DS} is due to the high TAT rates caused by defects in the crystalline structure and at oxide interface as well. Achieving high quality interface properties is important to construct a successful performing MOSFET device, especially for high frequency devices. Ge, unlike Si, has no existing standard cleaning procedure, with the current wet chemical treatments and passivation techniques still lacking the capability of producing high quality Ge/oxide interfaces. In Chapter 4, the study of several combinations of basic conventional and unconventional treatments of Ge surface aiming at obtaining improved results were performed using CV and frequency dependent analysis characterizations. The investigation included surface passivation techniques such as the effect of PPO and sulfite passivation. In addition, wet chemical surface treatments such as HF, HCl and recently proposed $C_6H_8O_7$ solution were compared using combination of some of these methods to show the influence on the MOSCAP electric characterization. Best results obtained were for PPO passivated devices as well as the combination of Sulfite passivated devices with $C_6H_8O_7$ combination. An alternative surface treatment method that was proposed at the end of this chapter, that uses a combination of the new $C_6H_8O_7$ treatment together with the typical HCl surface treatment, proved to provide good performance and have great potential to produce high quality Ge surface. This method was furthermore applied to complete p-PDBFET structures

during this work and proved its superiority as well. Prosperous development of a device simulation model that correlates the experimental device parameters to the performance was then demonstrated in Chapter 5. Comparing the experimentally determined device characteristics with simulation results provided the opportunity to gain insight into the device operation, revealing the non-ideal behaviour causes and consequently suggested strategies for device performance optimization. The existence of doping smearing out problem caused degradation in the crystal quality and hence high trap density leading to TAT rates. The leakage current is dominated by TAT mechanism and contributions from BTBT. The BTBT is the main mechanism responsible for the non-saturating behaviour of the output characteristics besides controlling the optimum δ-doping concentration value along with the trap density. Results from Chapter 3, 4 and 5 were exploited to optimize the performance in the following section of the work. In Chapter 6, the results on high performance Ge-based p-PDBFETs were demonstrated showing comparable performance to Ge-based MOSFETs from literature of comparable L_{CH} but of complex design and aggressive scaling schemes. It was possible to achieve low leakage current values, at relatively low V_{DS}, of sub-nanoampere down to picoampere at even relatively large structure sizes integrated on Si with challenging short channel lengths due to the virtue of the concept of field tailoring achieved by the planar doping of the channel. In addition, the influence of the new surface treatment method on Ge-based transistors that was investigated proved to further enhance the performance of the devices. The potential of the improved device performance and competent SS was proven thorough the updated simulation model and low temperature measurements, elaborating the excellent prospective performance of the devices and its efficiency. In order to relax the restriction of achieving a perfect Ge interface quality, and to combine the advantages of using Ge to boost the driving current while achieving low leakage current advantage of large E_G materials, a modified channel design is presented. A device improvement strategy was proposed, based on the developed simulation model in Chapter 5. The implementation of Ge/SiGeSn-based PDBFET model for the first time is presented using channel engineering, where a Ge-lattice matched $Si_xGe_{1-x-y}Sn_y$ heterostructure barrier placed within the Ge channel is implemented and investigated. The presented design verified to be a smart solution to overcome many of the Ge-based FET challenges recessing it from achieving the ultimate ideal conditions of Si/SiO_2 material system. Simulation results confirmed that introducing a larger E_G of the heterostructure into the channel is an interesting solution that is expected to highly decrease I_{off} and mitigated high rates of TAT and BTBT for different quality devices enabling its operation for energy efficient FET applications.

In future, continuation of work is recommended in the following directions based on the obtained results:

(i) GeO_2 is a very challenging interface and a great potential lies in improving its quality where harvesting Ge main advantages relies on this point. This includes optimizing etching recipe to reduce the mesa surface roughness, which would improve the obtained drive current, adjusting chemical treatment and passivation techniques by studying the effects of combination different conventional mechanisms.

(ii) Device Scaling is an essential procedure to be applied to Ge integrated on Si FET devices for bulk trap density reduction, which in turn would decrease leakage current and parasitics.

(iii) The study of high-speed performance of the Ge-PDBFET is of great importance, taking into consideration the advantage introduced by the Ge as a high mobility semiconductor and the PBD structure as a high speed diode structure. By introducing a spacer between the gate contact and the substrate, the large overlap between the gate and drain will be eliminated reducing GIDL effect and T_{OX} can be substantially reduced, leading to a major improvement in SS and enhancement of drive current values as well. This design would in turn decouple the substrate from the active device, and hence the large parasitic capacitive load is removed. This would make the mobility extraction possible and high frequency performance can be evaluated where the actual channel lengths of these devices, which is expected to be much shorter than defined, can then be abstracted and assessed.

(iv) With ultimate channel length scaling, the need for doping becomes less; hence, it is motivating to study the usage of the heterostructure Ge/SiGeSn as the main source of producing a barrier for aggressively scaled NW devices utilizing the optimized alloy composition.

Publications Based on this Work

[1] Y. Elogail, F. Berkmann, C. J. Clausen, I. A. Fischer, D. Schwarz and J. Schulze,“ Inverstigation of Ge Based P-Channel Planar-Doped Barrier FETs Integrated on Si“, To be submitted to Japanese Journal of Applied physics, IOPscience, 2020.

[2] Y. Elogail, I. A. Fischer, T. Wendav and J. Schulze, “Enhancement of Ge-Based P-Channel Vertical FET Performance by Channel Engineering Using Planar Doping and Ge/$Si_xGe_{1-x-y}Sn_y$ Heterostructure Model for Low Power FET Applications”, *Semiconductor Science and Technology*, IOPscience, vol. 33, no. 11, 2018.

[3] L. A. Hänel, Y. Elogail, D. Schwarz, I. A. Fischer and J. Schulze, “Performance of $C_6H_8O_7$-treated and H- and Cl passivated Ge-MOS-capacitances on Ge-Virtual Substrate on Si (001)”, *41st international convention on information and communication technology, electronics and microelectronics,* Opatija, Croatia, 2018.

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[5] Y. Elogail, K. Elkhouly, I. A. Fischer, K. Kostecki and J. Schulze , “Fabrication and Simulation of Vertical Ge-based P-Channel Planar-Doped Barrier FETs with 40 nm Channel Length”, *Fifth Berkeley Symposium on Energy Efficient Electronic Systems E3S, IEEE*, California, USA, 2017.

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