Frequency-Agile Bandpass Delta-Sigma Modulator for Microwave Transmitters

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Contents

Symbols

Latin Characters

Symbol	Description	Unit
A_{E0}	Emitter area	cm^2
A_{E1}	Emitter area	cm^2
A_V	Voltage gain	–
$\hat{A}_V$	Reduced voltage gain	–
$A_{\mathrm{V,sim}}$	Simulated voltage gain	–
Δf	Bandwidth	Hz
C_L	Load capacitance	F
$\hat{C}_L$	Scaled load capacitance	F
C_p	Equivalent parallel capacitance	F
C_s	Equivalent series capacitance	F
GBW	Gain bandwidth product	1/s
$G_{m,1}$	Transconductance of TCA in front of the quantizer	mS
$G_{m,2}$	Transconductance of TCA in front of the quantizer	mS
G_q	Transconductance of Q-enhancement TCA	mS
$I_{1\mathrm{a}}$	Tail current	mA
$I_{1\mathrm{b}}$	Tail current	mA
$I_{2\mathrm{a}}$	Tail current	mA
$I_{2\mathrm{b}}$	Tail current	mA
I_C	Collector current	mA
I_0	Collector current	mA
$I_{\mathrm{cap,tot}}$	Supply current for all switchable capacitors of one resonator	mA
I_1	Collector current	mA
$\hat{I}_1$	Modified collector current	mA
I_0	Tail current	mA
$\hat{I}_0$	Modified tail current	mA
I_S	Reverse saturation current of the base-emitter diode	mA
I_{S0}	Reverse saturation current	mA
I_{S1}	Reverse saturation current	mA

Symbol	Description	Unit
$\hat{I}_{S1}$	Modified reverse saturation current	mA
J_C	Collector current density	$\mathrm{mA/cm^2}$
J_S	Saturation current density	$\mathrm{mA/cm^2}$
L_p	Equivalent parallel inductance	H
L_s	Equivalent series inductance	H
P_{load}	Load power	W
P_{avg}	Average power	W
P_{Drain}	Drain power	W
P_{Driver}	Power of the driver	W
$P_{\mathrm{Modulator}}$	Power of the DSM	W
P_{peak}	Peak power	W
R_B	Base resistance	Ω
R_E	Emitter resistance	Ω
R_0	Resistance	Ω
R_1	Resistance	Ω
R_2	Resistance	Ω
R_{d}	Emitter degeneration resistance	Ω
R_L	Load resistance	Ω
$\hat{R}_L$	Scaled load resistance	Ω
R_0	Output resistance	Ω
R_p	Equivalent parallel resistance	Ω
R_s	Equivalent series resistance	Ω
R_{va}	Voltage-to-current converter resistance	Ω
R_{vb}	Voltage-to-current converter resistance	Ω
T_s	Sampling time	s
T	Absolute temperature	K
V_A	Early voltage	V
V_{BE}	Base-emitter voltage	V
V_{BE0}	Base-emitter voltage	V
V_{BE1}	Base-emitter voltage	V
$V_{\mathrm{BE,m}}$	Base-emitter voltage	V
$V_{\mathrm{BE,p}}$	Base-emitter voltage	V
V_{bi}	Bias voltage	V
V_{CE}	Collector-emitter voltage	V
V_f	Feedback voltage	V
Y_{LC}	LC-circuit admittance	$1/\Omega$
a	Scaling factor	–
C_{BE}	Base-emitter capacitance	F
C_{CB}	Collector-base capacitance	F
$\hat{C}_{\mathrm{CB}}$	Modified collector-base capacitance	F
C_{M}	Miller capacitance	F
C_d	Diffusion capacitance	F
C_{fix}	Fixed capacitance	F

Symbol	Description	Unit
C_{tot}	Effective total capacitance	F
C_{varac}	Varactor capacitance	F
ΔI	Deviation from the design current	mA
Δi	Differential current	mA
Δi_{max}	Maximum differential current	mA
DR	Dynamic range	dB
$D_{\alpha,\beta}(s)$	Laplace transform of the generalized DAC pulse	V
$D(s)$	Laplace transform of the DAC pulse	V
$D_{\text{HRZ}}(s)$	Laplace transform of the HRZ DAC pulse	V
$D_{\text{NRZ}}(s)$	Laplace transform of the NRZ DAC pulse	V
$D_{\text{RZ}}(s)$	Laplace transform of the RZ DAC pulse	V
$d_{\alpha,\beta}(t)$	Generalized DAC pulse in time domain	V
$d(t)$	DAC pulse in time domain	V
$d_{\text{HRZ}}(t)$	HRZ DAC pulse in time domain	V
$d_{\text{NRZ}}(t)$	NRZ DAC pulse in time domain	V
$d_{\text{RZ}}(t)$	RZ DAC pulse in time domain	V
Δv	Voltage change	V
$\overline{e^2}$	Quantization error	–
η_D	Drain efficiency	%
η_{tot}	Total efficiency	%
f_N	Nyquist frequency	Hz
f_0	Resonance frequency	Hz
f_s	Sampling frequency	Hz
f_T	Transit frequency	Hz
$f_{T,\text{differential}}$	Transit frequency of the differential pair	Hz
G_{q}	Q-enhancement transconductance	mS
g_m	Transconductance	mS
$\hat{g}_m$	Modified transconductance	mS
$h(n)$	Impulse response in discrete-time	–
$h(t)$	Impulse response in continuous-time	–
$H_{1\text{h,d}}(z)$	Discrete-time Transfer function for HRZ DAC pulse into the first resonator	–
$H_{1\text{r,d}}(z)$	Discrete-time Transfer function for RZ DAC pulse into the first resonator	–
$H_{2\text{h,d}}(z)$	Discrete-time Transfer function for HRZ DAC pulse into the second resonator	–
$H_{2\text{r,d}}(z)$	Discrete-time Transfer function for RZ DAC pulse into the second resonator	–
$h_{\text{bp,c}}(t)$	Continuous-time impulse-response	–
$h_{\text{bp,d}}(n)$	Discrete-time impulse-response	–
$H_{\text{LC,c}}(s)$	Continuous-time transfer function of the LC resonator	mS
$H_{\text{proto,c}}(s)$	Prototype transfer function of the resonator	–
$H_{\text{BP,c}}(s)$	Continuous-time loop filter	Ω

Symbol	Description	Unit
$H_{\mathrm{BP,d}}(z)$	Discrete-time bandpass loop filter	–
$H^*_{\mathrm{BP,d}}(z)$	Discrete-time bandpass loop filter without extra digital delay	–
$H_{\mathrm{LP,d}}(z)$	Discrete-time lowpass loop filter	–
$H_{\mathrm{LP,d}}(-z^2)$	Discrete-time bandpass loop filter	–
$i_{1\mathrm{a}}$	Differential current	mA
$i_{1\mathrm{b}}$	Differential current	mA
i_B	Base current	mA
$i_{2\mathrm{a}}$	Differential current	mA
$i_{2\mathrm{b}}$	Differential current	mA
i_C	Collector current	mA
$\overline{i_n^2}$	Noise current	mA^2
I_{ref}	Reference current	mA
k_{1h}	Feedback coefficient for the first HRZ DAC pulse	–
k^*_{1h}	Renormalized feedback coefficient for the first HRZ DAC pulse	mS
k_{1r}	Feedback coefficient for the first RZ DAC pulse	–
k^*_{1r}	Renormalized feedback coefficient for the first RZ DAC pulse	mS
k_{2h}	Feedback coefficient for the second HRZ DAC pulse	–
k^*_{2h}	Renormalized feedback coefficient for the second HRZ DAC pulse	mS
k_{2r}	Feedback coefficient for the second RZ DAC pulse	–
k^*_{2r}	Renormalized feedback coefficient for the second RZ DAC pulse	mS
λ	Scaling factor	–
n	Discrete-time	–
$\omega_{3\mathrm{dB}}$	Angular 3-dB frequency	1/s
ω_0	Angular resonance frequency	1/s
ω_T	Angular transit frequency	1/s
P_n	Noise power	W
P_{sig}	Signal power	W
$P_{Q,\mathrm{oversampling}}$	Quantization noise of an oversampling ADC	W
P_Q	Quantization noise	W
$P_{Q,\mathrm{Nyquist}}$	Quantization noise of a Nyquist ADC	W
Δ	Quantization step	V
r_0	Small-signal output resistance of a BJT	Ω
r_π	Input resistance of a BJT	Ω
t	Time	s
S_Q	Noise spectral density	W/Hz
$S_{Q,\mathrm{Nyquist}}$	Noise spectral density of a Nyquist ADC	W/Hz
τ_1	Time constant	s
τ_2	Time constant	s
τ_4	Time constant	s
$\hat{\tau}_4$	Modified time constant	s
τ_5	Time constant	s
$\hat{\tau}_5$	Modified time constant	s

Symbol	Description	Unit
v_{1a}	Small-signal voltage	V
v_{1b}	Small-signal voltage	V
v_{BE}	Small-signal base-emitter voltage	V
V_{cm}	Common-mode voltage	V
V_{dig}	Voltage swing of the differential amplifier	V
v_{in}	Input voltage	V
$\hat{v}_{in}$	Modified input voltage	V
$v_{in,max}$	Maximum input voltage	V
V_{max}	Maximum input voltage of the SMPA	V
$\overline{v_n^2(f)}$	Average squared noise voltage	V^2
V_{os}	Offset voltage	V
V_T	Thermal voltage	V
V_X	Voltage to node X	V
X_C	Impedance of the capacitance	Ω
X_L	Impedance of the inductance	Ω

Mathematical and Physical Constants

$e = 2.71828$	Euler's number
$\pi = 3.14159$	Archimedes' constant
$k_B = 1.38066 \cdot 10^{-23} J/K$	Boltzmann's constant

Zusammenfassung

Hochfrequenz-Leistungsverstärker sind für einen großen Teil des Leistungsverbrauchs im Mobilfunk verantwortlich. Klasse-S-Leistungsverstärker versprechen eine sehr hohe Leistungseffizienz, insbesondere für moderne Mobilfunkstandards. Ein wichtiger Teil eines Klasse-S-Leistungsverstärkers ist der Modulator, der aus dem Eingangssignal eine binäre Pulsfolge erzeugt. Ein Schaltverstärker kann diese Pulsfolge effizient verstärken.

Diese Arbeit behandelt die Implementierung eines solchen Modulators als Bandpass Delta-Sigma Modulator. Das Ziel ist eine standardkonforme Signalerzeugung für den Mobilfunkstandard UMTS (Universal Mobile Telecommunications System) in einem möglichst breiten Frequenzbereich.

Zu Beginn werden Grundlagen des Mobilfunks, Hochfrequenz-Leistungsverstärker und Voraussetzungen für Mobilfunksignale im Standard UMTS beschrieben. Ausgehend von einem zeitdiskreten Tiefpass Delta-Sigma Modulator wird ein zeitkontinuierlicher Bandpass Delta-Sigma Modulator hergeleitet.

Aus Projektgründen wird eine reine Bipolar-Technologie für die Implementierung ausgewählt. Verstärker und Auffangregister für den Digitalteil werden in Stromschalter-Technik umgesetzt. Verschiedene Schaltungen für einen Transkonduktanzverstärker werden hergeleitet und bewertet. Eine neue, schaltbare Kapazität wird vorgestellt. Diese ermöglicht einen großen Frequenzbereich für den Modulator.

Zwei Modulatoren werden entworfen. Der erste Modulator ist nicht abstimmbar und erfüllt die UMTS-Anforderungen für den Kanal von der Basis-Station zum Endgerät bei 2,2 GHz. Der zweite Modulator kann mit Hilfe der schaltbaren Kapazität einen Frequenzbereich zwischen 1,55 GHz und 2,45 GHz abdecken. Er ist im Bereich zwischen 1,83 GHz und 2,45 GHz standardkonform.

Abstract

A large part of the power consumption for mobile communications can be allotted to power amplifiers. Class-S power amplifiers promise a very high power efficiency, especially for modern communication standards. An important part of the Class-S power amplifier is the modulator that converts the input signal into a binary pulse sequence. A switching-mode power amplifier can amplify this sequence efficiently.

This work covers the implementation of such a modulator as a bandpass delta-sigma modulator. The goal is an output signal which fulfills the requirements of the mobile communication standard UMTS (Universal Mobile Telecommunications System) in a frequency range which is as large as possible.

The thesis starts with the basics of mobile communications, with power amplifiers and with the requirements for the transmit signals for UMTS. Based on a discrete-time lowpass delta-sigma modulator, a continuous-time bandpass delta-sigma modulator is derived.

Due to project constraints a bipolar technology is selected for the implementation. Current-mode logic is used for amplifiers and latches in the digital part. Different circuits for a transconductance amplifier are derived and evaluated. A novel, switchable capacitance is presented. With the switchable capacitance a large frequency range of the modulator becomes possible.

Two modulators are designed. The first modulator is not tunable and fulfills the UMTS requirements for the downlink channel from the base station to the user equipment at a signal frequency of 2.2 GHz. The second modulator uses the switchable capacitance and covers a frequency range between 1.55 GHz and 2.45 GHz. It fulfills the UMTS requirements within the frequency range between 1.8 GHz and 2.45 GHz.

1 Introduction

1.1 Goals of this work

The data rate in cellular nets grows exponentially since two decades. As a result, many mobile communication standards in various frequency bands coexist. If all mobile communication standards are integrated into the base station, the RF-transmitter becomes more complex.

Signals of modern mobile communication standards have a high ratio between the peak power and the average power. The peak-to-average power ratio (PAPR) is especially large for the channel from the base station to the user equipment (UE). A power amplifier must support the peak power level but is operated most of the time at a small power level. The power efficiency of conventional power amplifiers decreases significantly for signals with high PAPR.

The class-S amplifier addresses both challenges: it reduces complexity and offers higher power efficiency for signals with high PAPR.

It consists of a modulator, a switch-mode power amplifier (SMPA) and a filter. The modulator converts a mobile communications signal into a bit stream. The bit stream is amplified by the SMPA. Finally, a filter restores the signal waveform at a higher power.

Both, the modulator and the SMPA, can be designed as tunable circuits. That allows the class-S amplifier to replace several conventional transmit chains. The goal of this work is the design of such a modulator.

Two modulators are implemented as continuous-time bandpass delta-sigma modulators (CT-BPDSMs) in a bipolar technology with a transit frequency of 200 GHz. They convert bandpass radio-frequency (RF) signals for the channel from the base station to the UE into a digital pulse stream with a bit rate of 7.5 Gb/s. The first modulator is designed for a signal frequency of 2.2 GHz.

The signal frequency of the second modulator is tunable in a frequency range between 1.55 GHz and 2.45 GHz. The maximum signal-to-noise ratio (SNR) is at least 40.7 dB in a bandwidth of 20 MHz over the entire frequency range. The maximum SNR of 48 dB is achieved at a signal frequency of 2.1 GHz.

It is the first modulator for a class-S amplifier in a base station that fulfills the requirements of the mobile communications standard universal mobile telecommunications system (UMTS) in a frequency range between 1.8 GHz and 2.45 GHz.

The tunable modulator contains a transconductance amplifier with programmable transconductance. The linearity of several transconductance amplifiers [1] is simulated and compared.

The tunability of the modulator relies on switchable capacitances. The designed, switchable capacitance is based on an emitter follower and extends the state of the art.

Switchable emitter followers are already known from track-and-hold circuits [2].

Emitter followers generate replica voltages for both single-ended signal voltages (Chap. 4.5). A capacitance is connected between the positive signal node and the negative replica node. Another capacitance is connected between the negative signal node and the positive replica node. If the bias current sources of the emitter followers are switched on, the capacitances act as a differential capacitance. If the current sources are switched off, the replica nodes become floating and the effective capacitance is reduced to the parasitic capacitance.

1.2 Outline

Chap. 2 introduces the reader to mobile communication standards and especially to UMTS. Power amplifiers and the requirements on the transmit chain are discussed. The CT-BPDSM in this work can be interpreted as an analog-to-digital converter (ADC) followed by a single-bit digital-to-analog converter (DAC). Chap. 3 describes the basics of ADCs and concludes with the design choices for the implemented CT-BPDSM. Chap. 4 contains all circuit building blocks of the modulators. The system design, the simulation results for the modulator and the measurement results of the modulator implementations are summarized in Chap. 5. Chap. 6 concludes this work.

2 Transmitters for Mobile Communications

2.1 Mobile Communication Standards

This section gives an overview over the evolution of mobile communication standards and their properties. The transmit signal of early standards is a narrow band sinusoid with a low dynamic range (DR). A transmit chain for these signals is easy to implement. Later standards operate on several, different frequency bands. Their signals have a larger bandwidth. Their envelopes have zero crossings and very high peaks. The transmit chain must support a high SNR with a large bandwidth in different frequency bands. The large PAPR reduces power efficiency. Non-linearity at power peaks leads to intermodulation products outside of the signal band.

For each new standard, the requirements for the transmit chain become more stringent. But the fundamental problems for the transmit chain—frequency-agile operation, large bandwidths, high PAPR and non-linearity—remain the same for all mobile communication standards.

2.1.1 Historical overview

Mobile communications have a long history. In the early days only business men could afford mobile communications. Nowadays, mobile communications have become a commodity and are ubiquitious. In 2018, the number of mobile subscriptions reached 8.2 billion [3]. In 1979, it began with the first commercial wireless cellular net in Japan, followed quickly by another one in Scandinavia. This first generation (1G) of mobile communications still used analog transmission.

In 1983, the European conference of postal and telecommunications administrations (CEPT) decided to develop a standard for digital cellular voice telecommunications. The established committee came up with the first specification of global system for mobile communications (GSM) in 1987. To better support the development of the standard the European telecommunications standards institute (ETSI) was established in 1988. The countries of Scandinavia were among the first to benefit from the new technology: the first GSM call took place in Finland in 1991. Together with partners, the ETSI founded the 3rd generation partnership project (3GPP) to simplify and harmonize the future mobile communication standards. Today, standardization organizations from Japan, the USA, China, India and South Korea work together in the 3GPP.

GSM was developed to transmit voice. Data transmission was first done with modems using the voice channel. Later, circuit-switched data (CSD) used the underlying digital

Table 2.1: Data rates of deployed mobile communication standards

2G	Modem	CSD	GPRS	EDGE	
Data rate [kbit/s]	2.4	9.6	114	236	
3G	UMTS	HSDPA	HSDPA+	LTE Cat.3	LTE Cat.4
Data rate [Mbit/s]	0.384	21	42	100	150
4G	LTE Cat.6	LTE Cat.9	LTE Cat.11		
Data rate [Mbit/s]	300	450	600		

coding and quadrupled the data rates up to 9.6 kbit/s. With the advent of the first mobile web browsers and the wireless application protocol (WAP), the need for higher data rates lead to the development of general packet radio service (GPRS) in 2000 and later to the extension of GSM into enhanced data rates for GSM evolution (EDGE). EDGE extended the quadrature phase-shift keying (QPSK) constellation diagram into 8-phase shift keying (8-PSK) and doubled the data rate. That was the last modification to the second generation standard GSM. Nevertheless, GSM is still the standard with the best coverage worldwide.

The third generation 3G started in 2001 and already had a focus on data transmission. The commercial deployment of the high speed packet access (HSPA) and HSPA+ followed in 2007 and 2009, respectively. The first edition of the new standard long term evolution (LTE) from 2009 could not satisfy the requirements of the International Telecommunication Union (ITU) and is still considered a 3.95G product. Later versions of LTE, called LTE-Advanced (LTE-A), meet the 4G specifications and brought data rates of 300 Mbit/s and more.

Fig. 2.2 and Tab. 2.1 show the evolution of the data rates in mobile communications since the beginnings in the 90s. Unlike Moore's law, data rates still continue to grow exponentially. 5G is on the horizon with low latency and even higher data rates up to 10 Gbit/s. While the preceding standards always had a human user in mind, 5G promises to connect *everything*. The number of mobile subscriptions already outgrew the world population (cf. Fig. 2.1). Machine-to-machine (M2M) communication will enable new applications in the internet of things (IOT) and in autonomous driving. This will lead to another boost of the number of subscriptions.

2.1.2 Baseband processing

Signal-to-constellation mapping or modulation is the process where a stream of data bits is converted into a stream of m-dimensional symbols. Up to now, there are mainly two dimensions: phase and amplitude. These can be converted into the in-phase (I) and the quadrature (Q) components. Fig. 2.3 shows often used constellation maps.

2G uses only the phase of the symbol: standard GSM uses QPSK; the GSM revision EDGE doubles the data rate by using 8-PSK. The constellation map rotates after each symbol by $\frac{3\pi}{8}$ to avoid zero crossings during the transition from one symbol to the next.

Phase shift keying (PSK) is easy to implement. For modulation orders of 16 and higher,

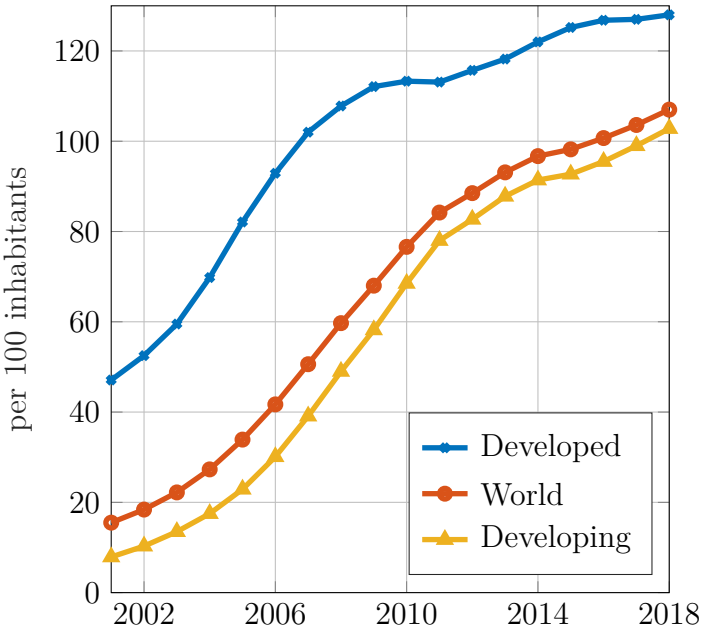


Figure 2.1: Mobile subscriptions. Reproduced with data from [3].

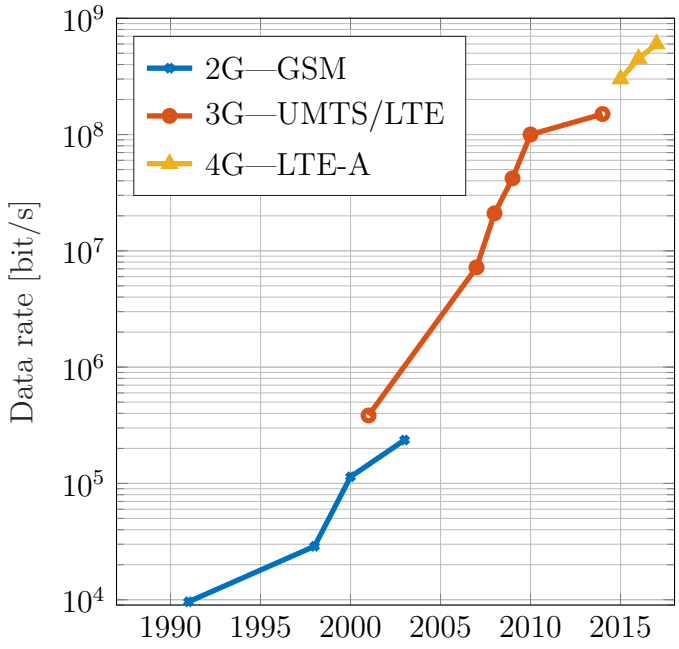


Figure 2.2: Data rate of deployed mobile communication standards vs. year of introduction.

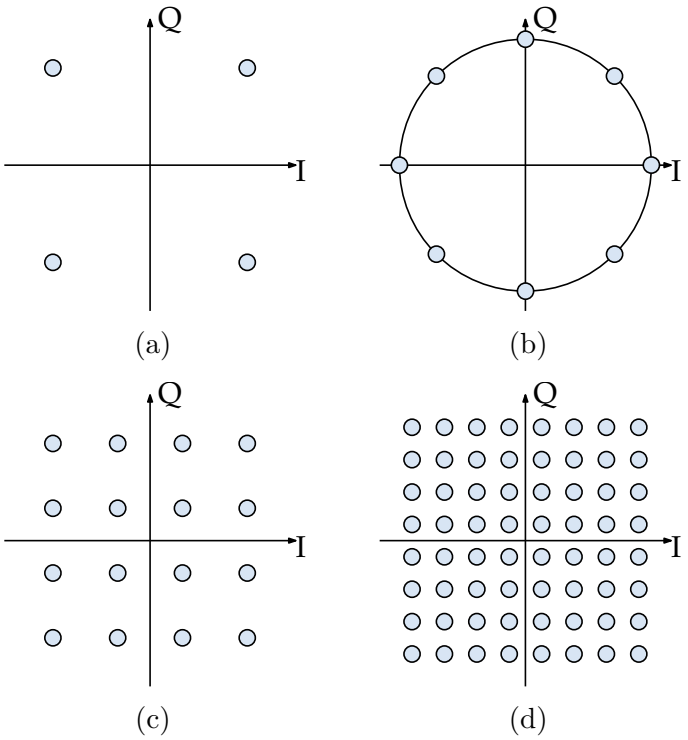


Figure 2.3: Constellation diagrams for (a) QPSK, (b) 8-PSK, (c) 16-QAM and (d) 64-QAM.

quadrature amplitude modulation (QAM) is preferred because it offers a lower bit error rate. 3G uses QPSK and 16-QAM. LTE and more recent standards use a modulation order of 64 and beyond.

The channel access method is the way how a transmission channel is partitioned between its users. If explicit partitioning is missing, collision can occur and lead to data loss. A good organization of resources avoids collision and increases the overall data rate. Wireless cellular nets are partitioned spatially into cells. Each cell has one base station (BTS) provided by an operator. The BTS provides access to the internet to many UEs. The channel from the UE to the BTS is called uplink; the channel from the BTS to the UE is called downlink. The BTS knows all UEs in the cell, estimates the properties of their channels to the BTS and allocates the resources accordingly. The only way collision can occur is when an additional UE enters the cell. In this case, the UE requests access on the special random-access channel (RACH). If a collision occurs during the request, the call is repeated.

Today, partitioning of the resources of a wireless channel is mainly done with five different methods:

1. Time-division multiple access (TDMA): used in GSM. The channel is partitioned into time slots and distributed to the UE. UEs only transmit in their allocated time slots.

2. Frequency division multiple access (FDMA): used in the analog nets in 1G and in

GSM.

3. Orthogonal frequency-division multiple access (OFDMA): used in the downlink of LTE, LTE-A and in 5G. It is a special case of FDMA where the partitioning is done within one frequency band. On the transmitter side, the data sequence is transformed into Fourier space and then mapped onto subcarriers. The tight spacing allows for a high spectral efficiency.

4. Single-carrier FDMA (SC-FDMA): used in the uplink of LTE. The main benefit is the low PAPR (cf. Chap. 2.3) because it is transmitted in time domain: On the transmitter side, the data sequence is transformed to Fourier space, mapped onto subcarriers and retransformed to time space.

5. Code-division multiple access (CDMA): used in UMTS. It distributes the information in space and time by multiplication with a pseudo-noise code. At the receiver, the information is recovered by multiplication with the same code. The partitioning is done in code domain.

6. Space division multiple access (SDMA): will be used in 5G. The channel to each UE depends strongly on its position in the cell. Several independent antennas in the UE increase the spatial diversity further.

2.2 UMTS Transmitter Specifications

The specifications for UMTS base stations are set by the ETSI [4]. The requirements for the transmitter are verified at the antenna connector.

The error vector magnitude (EVM) is a metric for the in-band signal quality. It is the normalized length of the vector from the measured signal point to the ideal signal point in the constellation map (cf. Fig. 2.4). UMTS allows for an EVM of 12.5 % for 16-QAM and an EVM of 17.5 % for QPSK.

The adjacent channel leakage power ratio (ACLR) is a metric for the out-of-band signal quality. It is the ratio between the (undesired) mean power in the adjacent channel and the mean power in the signal band[1]:

$$\mathrm{ACLR} = 10 \log \frac{P_{\text{adjacent channel}}}{P_{\text{signal}}}. \tag{2.1}$$

Fig. 2.5 visualizes the ACLR measurement. It shows the output spectrum of a bandpass delta-sigma modulator (BPDSM) with a UMTS-signal. The signal band is delimited by the two red vertical lines. The adjacent and the alternate signal channels are highlighted with the green hatched area. For UMTS base stations, ETSI specifies the minimum ACLR at ±5 MHz offset and ±10 MHz offset from the carrier (cf. Tab. 2.2).

[1] ETSI defines the ACLR as the inverse ratio. This work uses this wide-spread definition from many measurement equipment suppliers. Nokia (formerly Alcatel-Lucent), the cooperation partner in this project, also uses this definition.

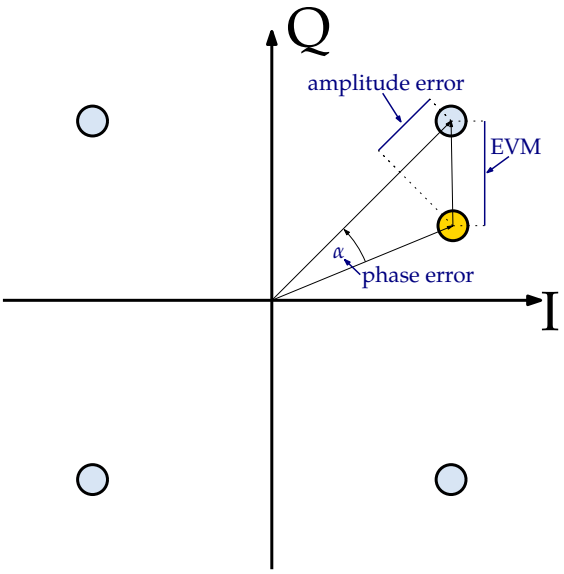


Figure 2.4: Error vector magnitude of a QPSK signal.

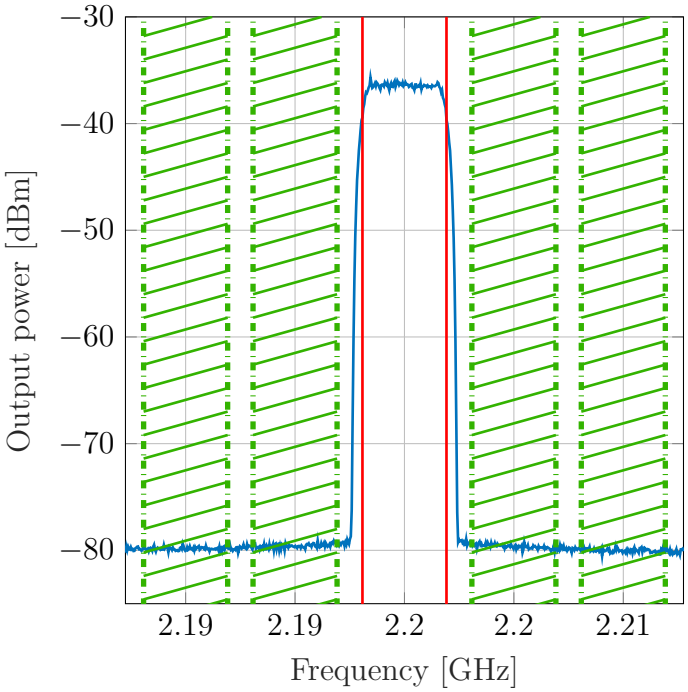


Figure 2.5: Measurement of the ACLR: signal band (delimited by the red lines) and adjacent / alternate signal channels (green hatched area).

Table 2.2: Minimum adjacent channel leakage ratio for UMTS base stations.

Offset to the carrier frequency	ACLR limit
±5 MHz	-45 dB
±10 MHz	-50 dB

2.3 Signal Statistics and Efficiency Metrics

The power efficiency is an important optimization goal for mobile communication systems. The drain efficiency η_D of an amplifier

$$\eta_D = \frac{P_{\text{load}}}{P_{\text{Drain}}} \tag{2.2}$$

is the ratio between the output power P_{load} and the power consumption P_{Drain} of the power amplifier. For the operator of a BTS, the total efficiency η_{tot} is more meaningful:

$$\eta_{\text{tot}} = \frac{P_{\text{load}}}{P_{\text{Modulator}} + P_{\text{Driver}} + P_{\text{Drain}}}. \tag{2.3}$$

It relates the output power to the total power consumption. The total power includes the power consumption of the modulator $P_{\text{Modulator}}$, of the driver in front of the amplifier P_{Driver} and of the power amplifier P_{Drain}.

The average power is much lower than the peak power in modern mobile communication standards. The PAPR quantifies these variations. It relates the maximum instantaneous power of the signal to its average:

$$\text{PAPR} = 10 \log \frac{P_{\text{peak}}}{P_{\text{avg}}}. \tag{2.4}$$

A large PAPR leads to bad efficiency in the power amplifier.

Clipping can reduce the PAPR at the expense of lower signal quality within the signal band (EVM) and outside the signal band (ACLR). If only very few peaks are clipped, the distortion is equivalent to white noise in the frequency domain. More clipping will lead to non-linearity and a higher ACLR. Filtering in frequency domain reduces the ACLR again. Clipping is done at a low intermediate frequency in the digital baseband processor where signal processing and filtering are cheap. In practice, the signal is clipped until the limit on the EVM from the mobile communication standard is reached. It is filtered until the power in the adjacent signal bands is below the specifications for the ACLR [5].

The main source for out-of-band power in the adjacent channels is the non-linearity in the power amplifier. The out-of-band power is significantly reduced for lower peak power (cf. Chap. 3.1.1). That makes clipping essential for good power efficiency *and* good ACLR. Therefore, the modulator in this work is characterized with an unclipped UMTS signal with a PAPR of 10.3 dB and a clipped UMTS signal with a PAPR of 5.4 dB.

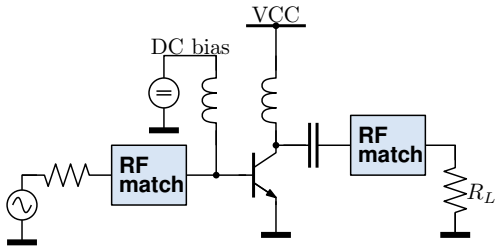


Figure 2.6: Schematic of a linear power amplifier. The power transistor is drawn as a bipolar junction transistor (BJT), but can be of any type.

2.4 Linear Power Amplifiers

Power amplifiers open up a broad topic [6]–[8] and only the three linear power amplifier classes are introduced here. All of these classes can be implemented based on the schematic in Fig. 2.6. A signal travels from the source through an RF-match to the input of the power transistor. The amplified output signal goes through a coupling capacitor and another RF-match to the load. The bias of the transistor is set by a voltage source and it is connected to the input by a DC feed.

The choice of the bias point determines the amplifier class. Fig. 2.7a shows the load line of the power transistor. The black curves represent the output current vs. the output voltage for different input voltages. The colored curves represent the linear response from the load.

The class-A amplifier uses the straightforward load line which connects the points of minimum current and maximum voltage with the point of maximum current and minimum voltage. The operating point is in the middle of this line. The full wave of a sinusoid at the input is amplified (cf. Fig. 2.7b). The conduction angle is 2π.

Both—the supply current and the supply voltage—are constant for the class-A amplifier. The amplifier delivers the power either to the load or consumes it itself. That makes the class-A amplifier very linear, but also very inefficient.

The class-B amplifier only amplifies one half wave of the input signal, that corresponds to a conduction angle of π. Only half of the usable voltage $\frac{V_{\max}+V_{\text{knee}}}{2}$ is used for amplification. Often, two class-B amplifiers are used together: one amplifies the positive, the other amplifies the negative half wave. The class-B amplifier is considerably better in efficiency than the class-A amplifier but suffers from non-linearities at the switching point. These non-linearities can be reduced with a larger conduction angle. An amplifier with a conduction angle between π and 2π is called class-AB amplifier.

The class-C amplifier has a low conduction angle of less than π. It is very efficient but also very non-linear.

The efficiency and the output power of linear amplifiers for full-scale sinusoids are shown in Fig. 2.8. The class-A amplifier offers the best linearity but the lowest power

efficiency. The best power efficiency is offered by the class-C amplifier, but it also suffers from large distortions. Today, linearization techniques improve the linearity of other amplifiers well enough and the class-A amplifier is rarely used. In mobile communications the class-B and the class-AB amplifiers offer the best mixture of power efficiency and linearity.

The efficiency and the output power for modulated signals with high PAPR are much lower. The output power of a class-C amplifier is not a linear function of the input which makes amplitude modulation difficult.

Class-A, class-B and class-AB amplifiers are truly linear and the modulated signal can serve as the input signal. The operating point must be chosen for the peak signal power; however, the drain efficiency depends on the average signal power.

The class-A amplifier draws the same power from the supply independently of the input signal. The drain efficiency is therefore proportional to the input power. The drain efficiencies of the class-AB and the class-B amplifier are slightly better than that but they are still very low.

Better power efficiency for modulated signals is a research topic since decades. The most promising solutions include [6], [9]:

- Adaptive biasing and envelope tracking: the input bias voltage and the supply voltage are varied during operation, following the envelope of the RF-signal.
- The Doherty principle: the signal range is split into a main range and a peak range. Both are amplified by dedicated amplifiers. The peak amplifier is only active when needed.
- Hybrid amplifiers: often an efficient but non-linear amplifier is used in conjunction with a highly linear amplifier. The non-linearities of the first are compensated by the second.
- Efficient SMPAs: class-F and class-E.
- The class-S amplifier: it consists of a signal modulator and a class-D SMPA.

2.5 Switching-Mode Power Amplifier (SMPA)

SMPAs use the transistor as a switch with only two modes: either it conducts or it blocks. The ideal switch does not consume power because the product of voltage and current is always zero. When it conducts, the voltage across the switch is zero. When it blocks, the current across the switch is zero. The theoretical efficiency of a SMPA is 100 %.

Class-D amplifiers are SMPA with two alternating operation modes. Each of the modes generates one half wave of the signal. There are two implementations of class-D amplifiers: the voltage-mode class-D amplifier (VMCD) and the current-mode class-D amplifier (CMCD).

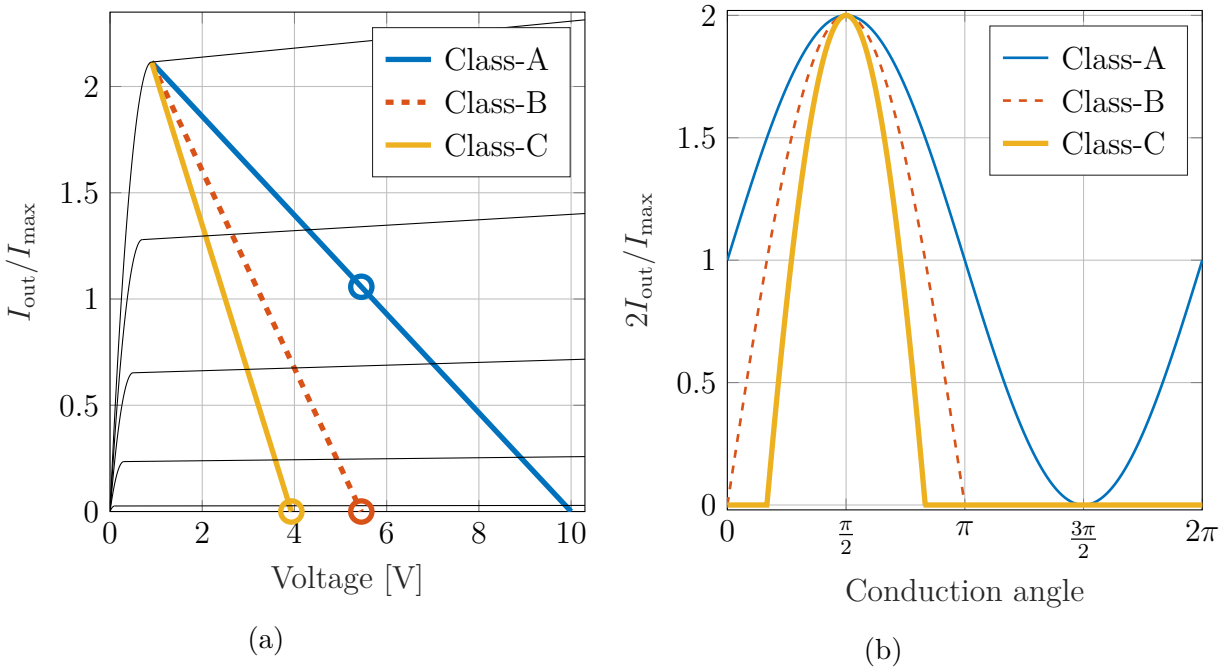


Figure 2.7: (a) Load lines of a class-A, a class-B and and a class-C power amplifier and (b) corresponding output currents.

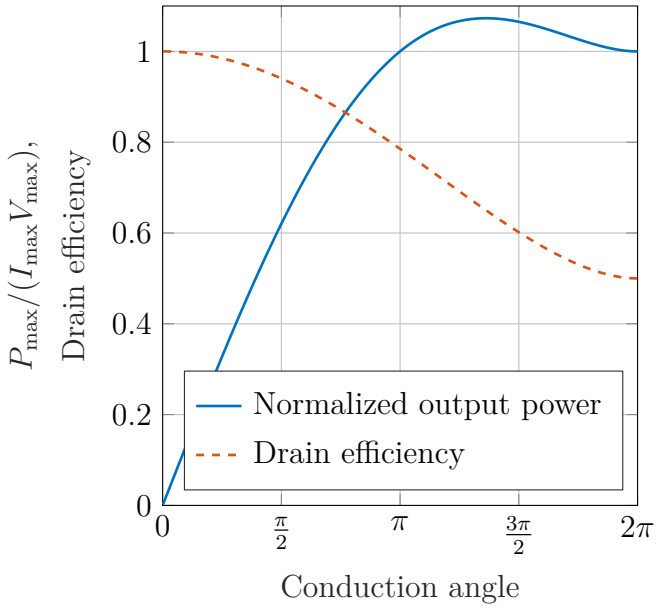


Figure 2.8: Output power and drain efficiency vs. conduction angle.

Fig. 2.9a shows a VMCD. The transistors are drawn as switches to emphasize the operation principle. Fig. 2.10 shows the corresponding output voltage and output current for one of the transistors. In the first step, the transistor conducts. The voltage across the transistor is zero, the current is the half wave of a sinusoid. In the second step, the transistor blocks and the output voltage is $V_{\max}$.

The other transistor is activated in antiphase. It blocks when the first transistor is conducting and vice versa. The output filter is drawn as a series LC circuit. In the ideal case, it is a high-Q series resonator and blocks all harmonics.

The CMCD in Fig. 2.9b is the dual circuit to the VMCD. The output filter is a parallel resonator and shorts all harmonics.

Real transistors differ from ideal switches in both modes. For high frequency operation, parasitic capacitors store energy in the electric field and parasitic inductances store energy in the magnetic field.

The stored energy in the electric field is lost when the switch is closed. The stored energy in the magnetic field is lost when the switch is opened. Therefore, a high power efficiency requires these two conditions:

- zero voltage switching and
- zero current switching.

Class-S amplifiers with conventional BPDSMs violate these conditions. That is the main limit for the power efficiency of a BPDSM-based class-S amplifier.

2.6 The Evolution of the Transmitter Architectures

Fig. 2.11 shows a heterodyne transmitter: the baseband processor maps the input bitstream onto a sequence of symbols. The I and Q components of the symbols are converted into analog domain and fed into a modulator. A local oscillator (LO) runs at an intermediate frequency (IF). It provides two sinusoids with 90° phase shift to each other. The in-phase component is mixed with the 0°-signal, the quadrature component with the 90°-signal. The summation of the products is the last step of the modulator. A second mixer moves the signal to the carrier frequency. The RF-signal is filtered amplified, filtered again and fed into the antenna.

Usually, the IF is much lower than the carrier frequency. In analog domain, mismatch of gain and phase in the I and Q paths are inevitable. This IQ-imbalance can severely impact linearity and SNR. The low IF of the heterodyne transmitter reduces the requirements on the technology and allows better postprocessing with less power.

The heterodyne principle dates back to 1920s when Lévy and Armstrong separately filed patents on it [10], [11]. Since then, it is popular for its many benefits. Today, technology has made lots of progress and a purely digital modulator and mixer is within reach. Fig. 2.12 shows a transmission chain, where the data stream is modulated, upsampled and mixed in digital domain. A digital BPDSM converts the multi-bit bandpass signal into a

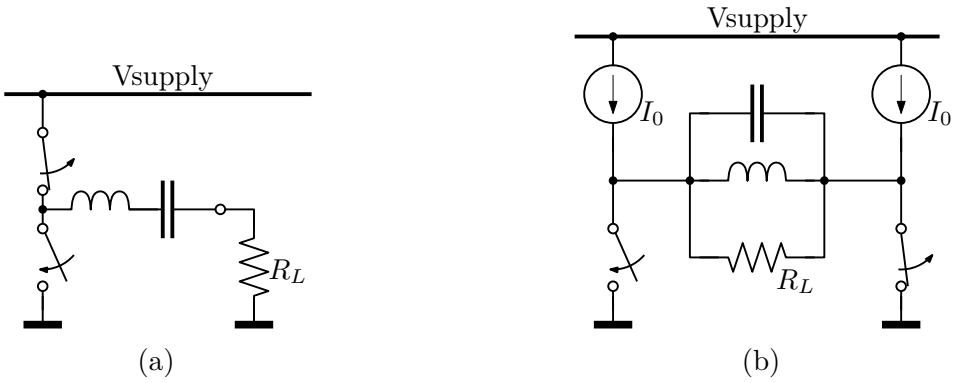


Figure 2.9: Two principles of switching-mode power amplifiers (SMPAs): (a) voltage-mode class-D (VMCD) power amplifier and (b) current-mode class-D (CMCD) power amplifier.

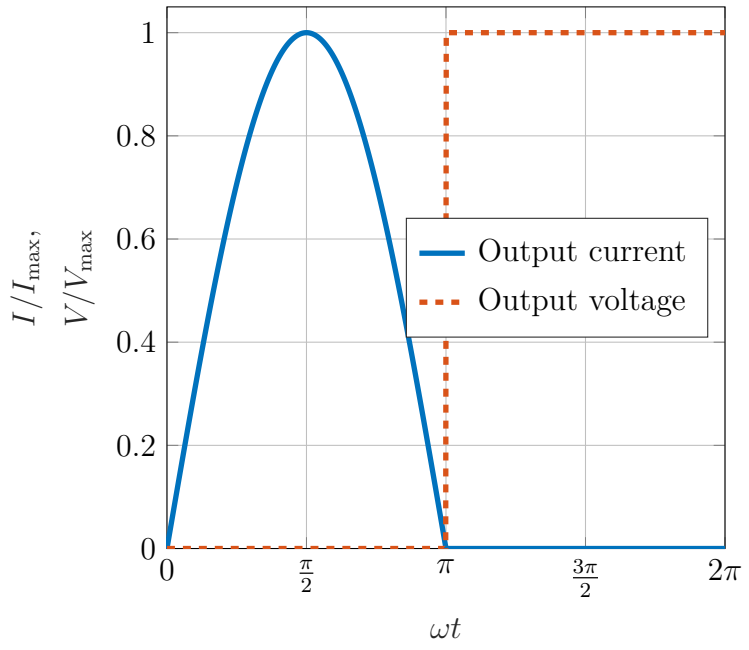


Figure 2.10: Output voltage and output current for a VMCD for a duty cycle of 50%.

single-bit bandpass signal. The remaining analog parts of the transmit chain consist of an efficient SMPA and the antenna.

This "digital transmit chain" has three main advantages:

1. The transmit chain has much less analog parts than the heterodyne transmit chain. The digital part can be migrated to other technology nodes with low design effort.

2. The digital part of the chain can run at any frequency below the maximum frequency.

3. The SMPA offers a high power efficiency when used with an appropriate filter. The combination of modulator, power amplifier and filter is called class-S amplifier.

The vision for direct digital synthesis of mobile communication signals already became true and evaluation kits for signal frequencies up to 3.7 GHz [12] and even up to 26.5 GHz [13] are commercially available. The main drawback of direct digital synthesis is the high power consumption. A digital transmit chain with a BPDSM as the last stage consumes less power, but it is still difficult to achieve high signal frequencies.

Fig. 2.13 shows an intermediate solution. A class-S amplifier replaces the filter and the power amplifier in the heterodyne transmit chain. The transmit chain can be designed with a tunable signal band. Digital control can adjust the frequency of the RF-mixer, of the CT-BPDSM and of the output filter.

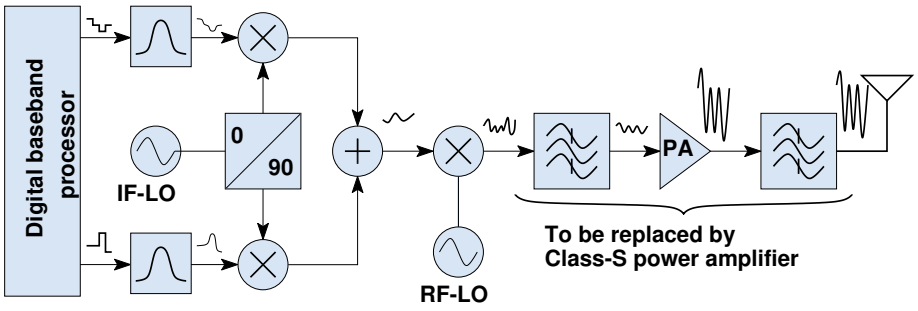


Figure 2.11: Conventional heterodyne transmit chain.

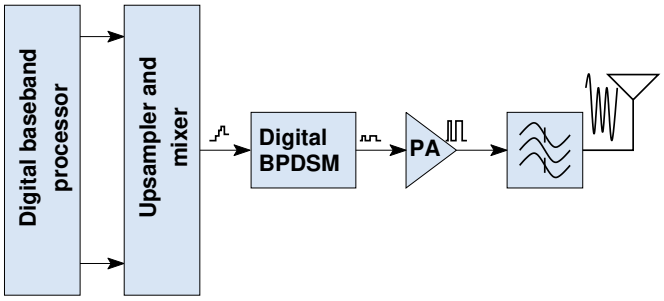


Figure 2.12: "Digital transmit chain": the bandpass signal is modulated as a digital pulse train and amplified by a switching-mode power amplifier SMPA.

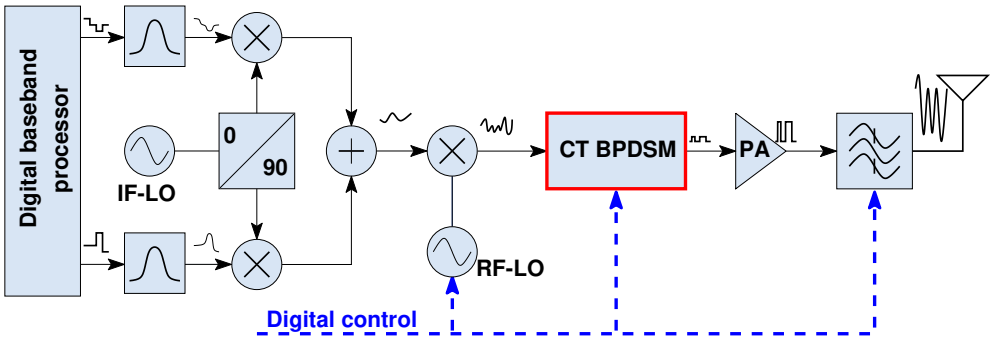


Figure 2.13: Transmit chain with class-S amplifier: the continuous-time bandpass delta-sigma modulator (CT-BPDSM) generates a noise-shaped 1-bit output signal. The inherent filter in the CT-BPDSM replaces the first bandpass filter in Fig. 2.11. A switching-mode power amplifier (SMPA) replaces the linear power amplifier. The CT-BPDSM for this setup is the main topic of this work.

3 Delta-Sigma Modulator

3.1 Signal Processing Basics

3.1.1 Introduction

In communications, a signal is a time varying variable that carries information from a sender to a receiver. A signal always has a purpose that limits its maximum amplitude and its bandwidth. An audio signal is a well-known example: the ultimate receiver of an audio signal is a human. Therefore, the human hearing range determines the bandwidth of technical systems for audio signals. The mp3 format exploits the limited bandwidth of the human ear and can compress audio signals with a high ratio.

A system is everything that processes an input signal $x(t)$ and generates an output signal $y(t)$. It can be artificial, such as an audio amplifier or a cable; it can be natural, such as the human ear or the propagation of speech in the air.

In electronics, a signal $s(t)$ is accompanied by random and deterministic noise $n(t)$ and by non-linearities or distortions $d(t)$ caused by the signal itself. Often, the sum of these parts

$$x(t) = s(t) + n(t) + d(t) \tag{3.1}$$

is called signal as well. This work follows that convention.

The power ratios between these components are important measures in electronics. The power ratios are easily determined with the power spectrum because the powers for signal P_{sig}, noise P_n and distortion P_d appear at different frequencies. The total output power

$$P_{\text{tot}} = P_{\text{sig}} + P_n + P_d + P_{\text{out-of-band}} \tag{3.2}$$

can be much higher than the sum of signal, noise and distortion because the out-of-band power $P_{\text{out-of-band}}$ makes up for a significant part of the total output power.

While the signal and the distortions are limited in bandwidth, noise is very broadband up to the THz range. In all practical systems, noise is filtered either implicitly or explicitly. The receiver can gather a significant part of the noise power from beyond the cut-off frequency of the filter if the filter response is flat. That dependency on the filter type hinders comparison of noise contributions.

The introduction of the equivalent noise bandwidth eliminates that dependency: the total noise power at the receiver is summed up. Within the signal band the noise power density is assumed to be flat. For calculation purposes, this noise power density is extended up to the cut-off frequency of a boxcar filter. The bandwidth of that filter is set such that

the noise power in that artificial system is identical to the previously calculated total noise power. This bandwidth is called equivalent noise bandwidth.

This work presents the design of a DSM and does not cover the necessary output filter. To allow for easy comparison to other DSMs, only the noise within the signal band is considered; the modulator output is filtered by a boxcar filter. In this case, the total noise is the summed up noise within the signal frequency band Δf. This simplification is used throughout the entire report.

IEEE standards describe the procedure on how to determine the power ratios for ADCs [14] and DACs [15]. For RF bandpass signals, only the power components in a certain band are considered.

The SNR is defined as

$$\mathrm{SNR} = 10 \log \frac{P_{\mathrm{sig}}}{P_{\mathrm{noise}}}. \tag{3.3}$$

In a similar manner, the signal-to-distortion ratio (SDR) and the signal-to-noise-and-distortion ratio (SNDR) are defined:

$$\mathrm{SDR} = 10 \log \frac{P_{\mathrm{sig}}}{P_d}, \tag{3.4}$$

$$\mathrm{SNDR} = 10 \log \frac{P_{\mathrm{sig}}}{P_{\mathrm{noise}} + P_d}. \tag{3.5}$$

3.1.2 Noise

Noise is ubiquitious in physical systems and is often dominated by thermal noise of resistors. At room temperature, the power spectral density of thermal noise is flat up to the THz-range. The power spectral density of a resistor with value R can be expressed by a mean square voltage

$$\overline{v_n^2(f)} = 4 k_B T R, \tag{3.6}$$

where k_B is the Boltzmann's constant and T is the absolute temperature. Using Norton's theorem, the voltage noise can be converted into a current noise

$$\overline{i_n^2} = \frac{4 k_B T}{R}. \tag{3.7}$$

The bandwidth of thermal noise is larger than the bandwidth of any practical system. The noise power within the signal band is therefore proportional to the bandwidth Δf of the signal band

$$P_n = \frac{\overline{v_n^2(f)}}{R} \Delta f = 4 k_B T \Delta f. \tag{3.8}$$

3.1.3 Non-linearity

Static and dynamic non-linearities can be distinguished. Dynamic non-linearities appear in systems with memory. The associated time constants depend on the technology. The

higher the signal frequency of the circuit with respect to the technology's oscillation frequency, the larger will be the effect of the memory on the total non-linearity. Thus, dynamic non-linearities play an important role in power amplifier (PA) design and circuits with a very high signal frequency. They can be modelled with the Volterra series [16]. Dynamic non-linearities can be neglected in this work because the ratio between signal frequency and oscillation frequency of the technology is low.

Static non-linearity leads to **saturation** of the signal power and to **distortion** within the signal band. Saturation can be observed in time domain, when the input value is beyond the limits of the system. It is quantified by the 1-dB compression point $P_{1\mathrm{dB}}$ in a plot of the output signal power vs. the input power. The 1-dB compression point is the input power where the signal power drops 1 dB below the extrapolated linear signal power.

Typically, a sinusoidal input signal saturates at a higher input power than a mixture of input frequencies. The mixture of input frequencies generates distortion; at the same signal output power, the total output power is higher than that for a sinusoidal input signal. This results in a higher peak amplitude and thus a lower 1-dB compression point.

Distortion is quantified by the SDR and the third-order intercept point (IIP3, OIP3), measured with the two-tone test [8], [17], [18]: the input voltage contains two sinusoids with amplitudes A at the center frequency ω_0 with the spacing $2h$

$$v = A\left[cos\left(\left(\omega_0 - h\right)t\right) + cos\left(\left(\omega_0 + h\right)t\right)\right]. \tag{3.9}$$

The non-linearity of the output current of a transconductance amplifier can be expressed with a power series of the input voltage

$$i\left(v\right) = c_0 + c_1 v + c_2 v^2 + c_3 v^3 + c_4 v^4 + c_5 v^5 + \ldots \tag{3.10}$$

where c_i are the coefficients of the non-linear system. In this work, higher-order terms have significant effect on the SNDR. For many other applications, it is sufficient to truncate the series after the cubic term.

The non-linearity mixes the two input sinusoids into a mixture of frequencies

$$\omega_{\mathrm{out}} = m\omega_0 + nh; \quad m, n \in \mathbb{Z}. \tag{3.11}$$

Mixing products occur

- at DC for $m = 0$,
- at the input signal frequencies for $m = 1$ and $|n| = 1$,
- at multiples of the input signal frequencies—the harmonics at $m = |n| \geq 2$,
- within the signal band—the intermodulation products (IMDs) at $m = 1$ and $n = 3, 5, 7, \ldots$ and
- elsewhere outside the signal band.

For bandpass systems, frequencies outside the signal band can be filtered out and are neglected. Within the signal band, the odd-order terms remain. The total distortion power is the sum over the IMDs

$$i_{\mathrm{IMD}} = i_{\mathrm{IMD3}} + i_{\mathrm{IMD5}} + i_{\mathrm{IMD7}} + \dots \tag{3.12}$$

SDRs can be defined relative to each of the IMD and are denoted analogously SDR3, SDR5, ...

The sum of the products IMD3 and IMD5 is given by

$$\begin{aligned} i_{\mathrm{IMD3+IMD5}} = &\left[\frac{3}{4}c_3A^3 + \frac{50}{16}c_5A^5\right]\left[\cos\left(\left(\omega_0 - 3h\right)t\right) + \cos\left(\left(\omega_0 + 3h\right)t\right)\right] \\ &+\frac{10}{16}c_5A^5\left[\cos\left(\left(\omega_0 - 5h\right)t\right) + \cos\left(\left(\omega_0 + 5h\right)t\right)\right]. \end{aligned} \tag{3.13}$$

The frequency spacing between two adjacent output tones—fundamental or IMD—is $2h$. Therefore, it is straightforward to determine the n^{th}-order distortion in the logarithmic output spectrum (cf. Fig. 3.1a). For a sufficiently small spacing $2h$ of the input tones, the powers of each IMDn-tone pair become equal. Then, the SDR$n = 10\log\frac{P_{\mathrm{sig}}}{P_{\mathrm{d,n}}}$ can be seen directly in the spectrum; it is the difference between one fundamental tone and one IMD tone.

Fig. 3.1b shows the fundamental, the IMD3 and the IMD5 vs. the input power. At small input power, IMD3 is much smaller than the signal power. But the slope is three times larger and the extrapolated curves intersect where the input power reaches the input-referred third-order intercept point (IIP3). This happens where the amplitudes of the fundamental and the IMD3 become equal [8]:

$$|c_1A| = \left|c_3\frac{3}{4}A^3\right|. \tag{3.14}$$

The IIP3 is given by the corresponding amplitude

$$A = \sqrt{\frac{4}{3}\left|\frac{c_1}{c_3}\right|}. \tag{3.15}$$

In a similar way, the amplitude for the input-referred fifth-order intercept point (IIP5) can be derived:

$$A = \left(\frac{16}{10}\left|\frac{c_1}{c_5}\right|\right)^{1/4}. \tag{3.16}$$

3.1.4 Signals and systems in the analog and in the digital domain

Analog signals are continuous in time and value. That means that they have a value at any arbitrary point in time and that they can take on any arbitrary value within the signal bounds.

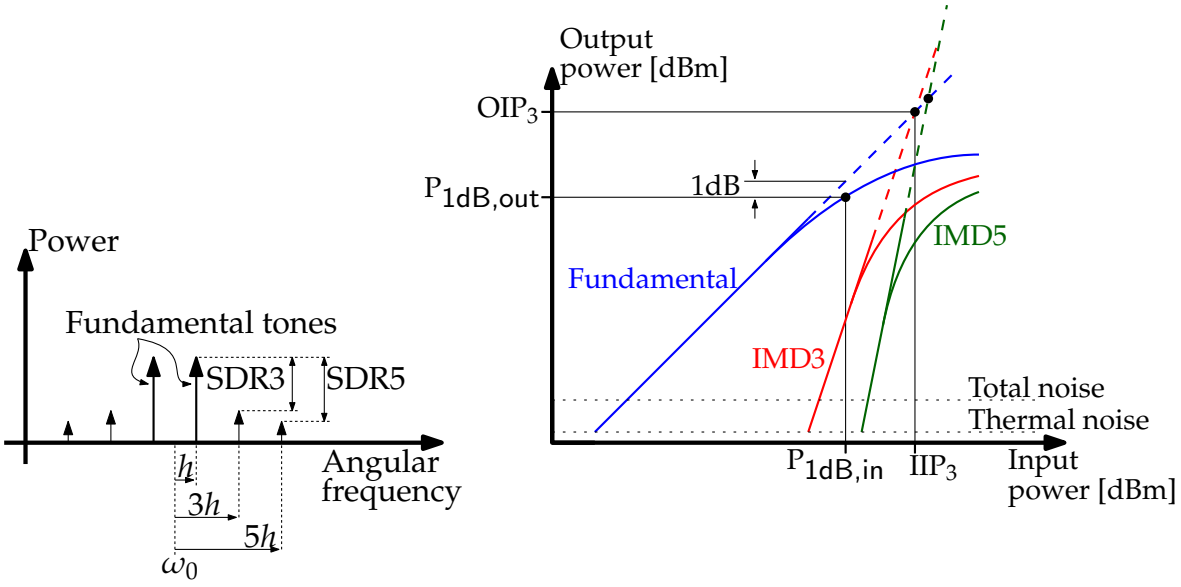


Figure 3.1: (a) Output spectrum of a two-tone test at low input power. (b) Fundamental (blue) and intermodulation products IMD3 (red) and IMD5 (green) vs. the input power. The 1-dB compression point and the third-order and fifth-order intercept points are marked with a dot.

Digital signals are discrete in time and value. These restrictions increase the noise margin and simplify requirements for timing. That makes them easier to store and to operate on.

Linear time-invariant (LTI) systems are used extensively in electronics because of their convenient properties. RLC networks are an example of an LTI system. Often, complex systems can be approximated by an LTI system—either by linearization (small signal analysis of circuits) or by limiting the considered time slice (channel in mobile communications).

A continuous-time LTI system is fully specified by its impulse response $h(t)$. The output signal $y(t)$ is the convolution of $h(t)$ with the input signal $x(t)$. The convolution is denoted with an asterisk:

$$y(t) = h(t) * x(t) = \int_{-\infty}^{\infty} h(\tau)x(t-\tau)\mathrm{d}\tau. \tag{3.17}$$

With this equation, the two key properties of LTI systems become clear immediately: The system is **linear**, that means scaling of the input signal with the scalar λ leads to scaling of the output signal with the same scalar λ

$$\begin{aligned} \tilde{x}(t) &= \lambda x(t), \\ \tilde{y}(t) &= h(t) * \lambda x(t) = \lambda y(t). \end{aligned} \tag{3.18}$$

And the system is **time-invariant**, that means that an input signal that is shifted in time by the delay Δt leads to an output signal that is shifted by the same time delay Δt

$$\begin{aligned} \tilde{x}(t) &= x(t - \Delta t), \\ \tilde{y}(t) &= h(t) * x(t - \Delta t) = y(t - \Delta t). \end{aligned} \tag{3.19}$$

The same arguments hold for discrete-time systems. There, the time variable t is replaced by the sequence index n.

The Laplace transform converts a signal $x(t)$ from time domain to (complex) frequency domain $X(s)$:

$$X(s) = \mathcal{L}\{x(t)\} = \int_0^\infty x(t)e^{-st}\mathrm{dt}. \tag{3.20}$$

The complex frequency domain is often named after the complex frequency s and simply called the s-domain. Variables in s-domain are upper-case throughout this work.

Many problem statements concerning LTI systems in the time domain can be solved in a more intuitive way in the s-domain. The impulse response $h(t)$ in the time domain becomes the transfer function $H(s)$ in the s-domain and the convolution in the time domain becomes a multiplication in the s-domain:

$$Y(s) = \mathcal{L}\{h(t) * x(t)\} = H(s)X(s). \tag{3.21}$$

The other direction holds true as well: a convolution in s-domain becomes a multiplication in time domain:

$$y(t) = \mathcal{L}^{-1}\{H(s) * X(s)\} = h(t)x(t). \tag{3.22}$$

The z-transform is similar to the Laplace transform and acts on discrete-time signals $x(n)$:

$$X(z) = \mathcal{Z}\{x[n]\} = \sum_{n=0}^{\infty} x[n]z^{-n}, \tag{3.23}$$

where z is a complex number and corresponds to the continuous-time complex frequency s. The variable $X(z)$ is said to be in the z-domain.

Convolution in discrete-time domain corresponds to multiplication in z-domain:

$$Y(z) = \mathcal{Z}\{h[n] * x[n]\} = H(z)X(z). \tag{3.24}$$

A time delay of k samples in discrete-time corresponds to a multiplication with z^{-k}:

$$Y(z) = \mathcal{Z}\{x[n - k]\} = z^{-k}X(z). \tag{3.25}$$

If z is evaluated on the unit circle ($|z| = 1$), it can be expressed as a function of the angular frequency ω and a sampling period T_s :

$$z \equiv e^{j\omega T_s}. \tag{3.26}$$

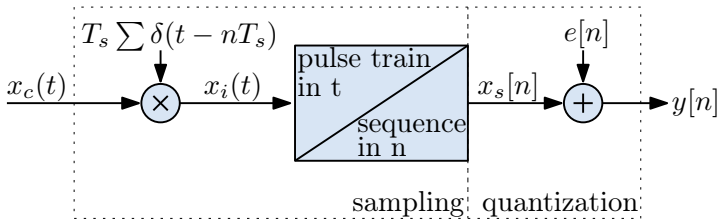


Figure 3.2: ADC blockdiagram: the analog input signal $x(t)$ is converted into the digital signal $y(n)$.

Then, the z-transform (3.23) is called the discrete-time Fourier transform (DTFT) of $x[n]$:

$$\begin{aligned} \mathrm{DTFT}(x[n]) &= \sum_{n=-\infty}^{\infty} x[n] e^{-j\omega n T_s} \\ &= \sum_{n=-\infty}^{\infty} x(nT_s) e^{-j2\pi f n T_s} \\ &= \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X\left(f - k f_s\right). \end{aligned} \tag{3.27}$$

where the equality between $x[n]$ and $x(nT_s)$ at the sampling instants is used. This equality and the repetition of the spectrum are anticipated and will be formally introduced in (3.28) and (3.31).

3.2 Analog-to-Digital Converters

Conversion from analog to digital domain consists of sampling and quantization [19], [20]. Fig. 3.2 shows a system model for the A/D conversion and Fig. 3.3 shows the signal waveforms for the involved steps. The input signal $x_c(t)$ is converted into the sampled signal $x_s[n]$ and then quantized into $y[n]$.

The order of these operations is arbitrary. Sampling usually comes first because of the large settling time during the quantization step. DSMs with a 1-bit quantizer amplify the signal before it is sampled. Then, a flip-flop does sampling and quantization in one step.

Sampling converts from continuous-time to discrete-time. The analog signal $x_c(t)$ is sampled at equidistant points in time with period T_s. The result $x_s[n]$ is no longer a function in time but a discrete-time sequence with index n:

$$x_s[n] = x_c(t)\Big|_{t=nT_s;n\in\mathbb{N}} = x_c(nT_s)\Big|_{n\in\mathbb{N}}. \tag{3.28}$$

For the analysis of the frequency behavior, the intermediate signal

$$x_i(t) = x_c(t)s(t) \tag{3.29}$$

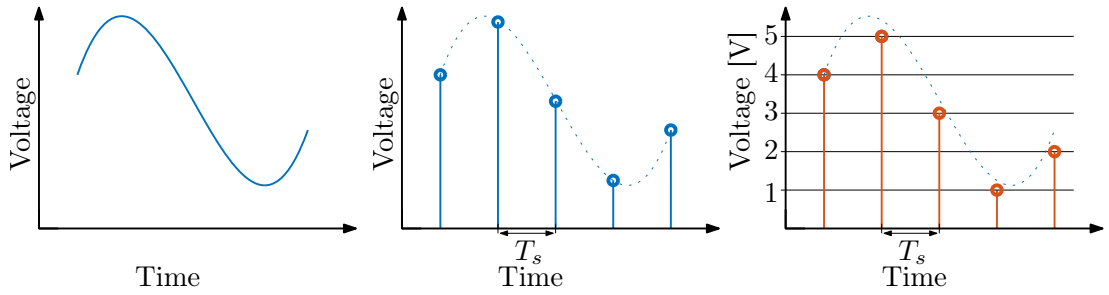


Figure 3.3: (a) Analog signal, (b) sampled signal in discrete-time but still with continuous values and (c) digital signal—the original values on the blue curve are rounded to the next quantization level and fall on the orange points.

is introduced. It is the multiplication of the input signal with the periodic Dirac impulse train

$$s(t) = T_s \sum_n \delta(t - nT_s). \tag{3.30}$$

In frequency domain, the Dirac impulse train converts into a Dirac impulse rake with a frequency spacing of $f_s = \frac{1}{T_s}$. Multiplication with the Dirac impulse train in time domain corresponds to convolution with the Dirac impulse rake in frequency domain. The spectrum of the input signal $X_c(f)$ repeats every f_s [21]:

$$X_i(f) = \sum_k X_c(f - kf_s). \tag{3.31}$$

Fig. 3.4 shows these repetitions for an input signal with bandwidth Δf. For small f_s, the images can overlap with each other and with the original input signal $X_c(f)$. This effect is called aliasing. In the frequency range where this overlap happens, the original signal can not be recovered from the sampled signal. However, sampling becomes completely reversible if the bandwidth of the input signal is smaller than the Nyquist frequency [22]

$$f_N = \frac{f_s}{2} \overset{!}{\geq} \Delta f. \tag{3.32}$$

Quantization converts from continuous values to discrete values. The chosen accuracy is a trade-off between effort and tolerable maximum error. The actual error in the final result is unknown but always less than the maximum error. The input range of an ADC is bounded and divided into equally large steps with step size Δ. The transfer curve of a quantization resembles a staircase (cf. Fig. 3.5). The quantizer rounds the input values to the nearest step. The maximum error is half the step size. Unlike sampling, quantization always involves errors and is not reversible even for ideal quantizers.

The number of steps is a power of two and relates the full-scale input range FS to the step size

$$\Delta = \frac{\mathrm{FS}}{2^B - 1}. \tag{3.33}$$

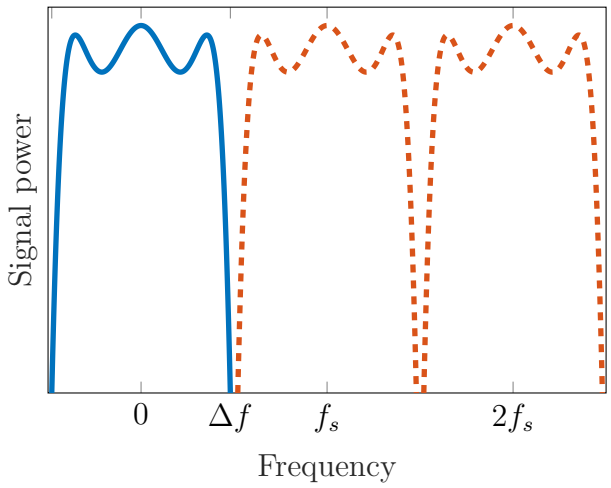


Figure 3.4: Spectrum of a sampled signal $x_i(t)$ with images at the multiples of the sampling frequency f_s.

where B is the resolution of the ADC in bit.

By definition, the difference between the output signal $y[n]$ and the sampled input signal $x_s[n]$ is called the quantization error (cf. Fig. 3.2):

$$e[n] = y[n] - x_s[n]. \tag{3.34}$$

The quantization error is a random variable and only its stochastic properties can be estimated [23], [24]. For well-behaved signals and ideal quantizers, $e[n]$ is independent of the input signal and is uniformly distributed in time and in frequency domain (cf. Fig. 3.6).

The average of the error is the systematic error. As expected with ideal quantizers, it is zero. The power of the error is the quantization noise P_Q. It can be calculated as the mean square of e:

$$\begin{aligned} P_{Q,\text{Nyquist}} = \overline{e^2} &= \int_{-\infty}^{\infty} e^2 \text{pdf}(e) \text{d}e \\ &= \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 \text{pdf}(e) \text{d}e = \frac{\Delta^2}{12}. \end{aligned} \tag{3.35}$$

where the probability density function (pdf) of e is given by

$$\text{pdf}(e) = \begin{cases} \frac{1}{\Delta} & \text{for } -\frac{\Delta}{2} < e \leq \frac{\Delta}{2} \\ \\ 0 & \text{otherwise} \end{cases}. \tag{3.36}$$

For practical signals, the spectrum of the quantization noise is flat [23] (some exceptions exist [25]). For a discrete-time signal, the quantization noise $P_{Q,\text{Nyquist}}$ is distributed onto the whole sampling frequency range from $-\frac{f_s}{2}$ to $\frac{f_s}{2}$. The power spectral density becomes

$$S_{Q,\text{Nyquist}}(f) = \frac{P_Q}{f_s} = \frac{\Delta}{12 f_s}. \tag{3.37}$$

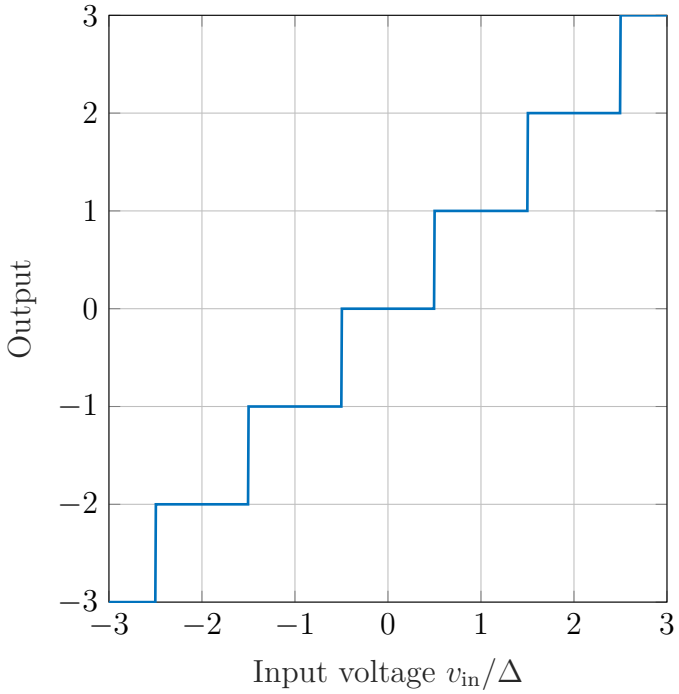


Figure 3.5: Transfer characteristic of a quantizer. A continuous input signal is mapped onto the nearest step of the "staircase".

3.2.1 Nyquist analog-to-digital converters

Nyquist ADCs use the whole available signal bandwidth between $-f_N$ and f_N. An anti-aliasing filter in front of the ADC removes out-of-band components above the Nyquist frequency. The maximum SNR for Nyquist ADCs is achieved with a full-scale sinusoidal input signal. The maximum SNR is also called the dynamic range (DR) of a circuit:

$$\text{DR} = \text{SNR}_{\text{max}}. \tag{3.38}$$

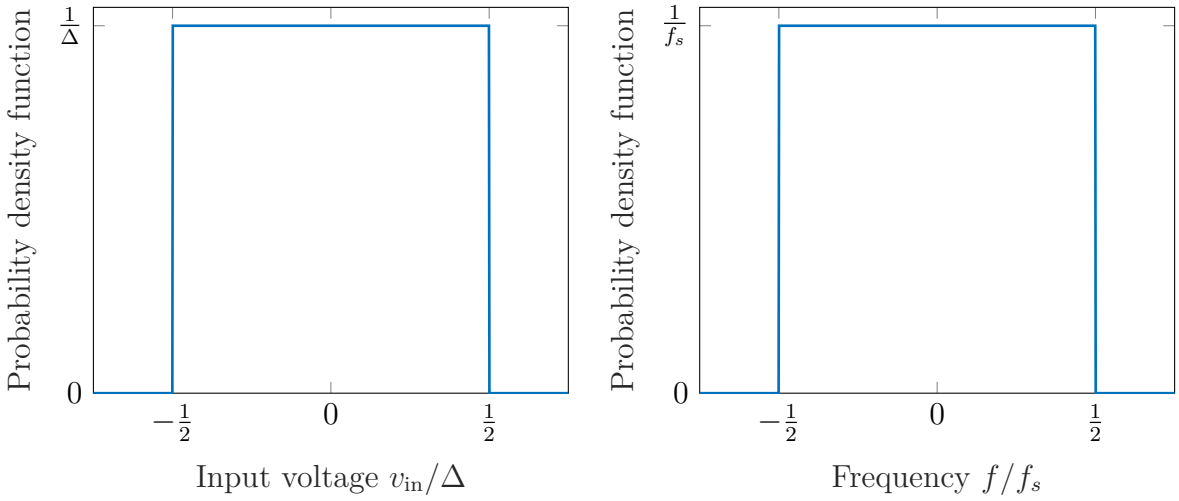
The DR can be interpreted as the useful signal range [26] between the smallest and the largest useful input power. The smallest useful input power is equal to the noise power. The largest useful input power is reached where the SNR peaks.

The signal power P_{sig} of the full-scale sinusoidal input signal can be expressed in terms of the resolution in nominal bits B:

$$P_{\text{sig}} = 0.5 \cdot \left(\frac{FS}{2}\right)^2 \approx 1.5 \cdot 2^{2B}\Delta^2. \tag{3.39}$$

Together with the quantization noise in (3.35) the DR becomes

$$\begin{aligned} \text{DR} &= 10\log\left(\frac{P_{\text{sig}}}{P_{Q,\text{Nyquist}}}\right) = 10\log\left(1.5 \cdot 2^{2B}\right) \\ &= (6.02B + 1.76)\,\text{dB}. \end{aligned} \tag{3.40}$$



(a) (b)

Figure 3.6: Quantization noise in time domain and in frequency domain: (a) probability density function of the quantization noise with the quantization step Δ vs. the amplitude and (b) power spectral density of the quantization noise vs. the frequency; the sampling frequency is f_s.

The DR has an affine relationship to the resolution. Each added bit increases the DR by approximately 6 dB.

Nyquist ADCs are used for many high-speed applications. The quantization step becomes very small for high resolutions. Above 10 bit, the quantization step is below 1 mV and most of the Nyquist ADCs need calibration [27]. For applications with high resolution, but low signal bandwidths, oversampling (cf. Chap. 3.2.2) and noise-shaping ADCs (cf. Chap. 3.2.3) are a better option.

To relate these architectures to Nyquist ADCs, the equation can be used in the other direction: from the peak SNR of an arbitrary ADC the effective number of bits (ENOB) for an ideal Nyquist ADC is estimated. The IEEE standard [14] includes non-linearity and defines the ENOB with the help of the SNDR:

$$\text{ENOB} = \log_2(\text{SNDR}) - 0.5 \cdot \log_2(1.5). \tag{3.41}$$

3.2.2 Oversampling data converters

For a single sample, the only way to reduce the quantization error is a higher ADC resolution. Samples of a discrete-time sequence are correlated if their bandwidth is limited. Like in channel coding, the information content of a sample is spread onto adjacent samples. The knowledge about the bandwidth and about previous samples reveals information about the next sample.

Another way to look at it is in the frequency domain. In the previous section, the distribution of the quantization noise in frequency domain is shown to be flat. The quantization error $\frac{\Delta}{12}$ is spread across the whole Nyquist band. But only the quantization

noise inside the signal band contributes to the noise power of the SNR. For a given signal bandwidth, the in-band noise can be reduced by oversampling, i.e. by increasing the sampling frequency. The effective quantization noise power becomes a fraction of the total quantization noise [28]

$$P_{Q,\text{oversampling}} = \frac{1}{\text{OSR}} P_{Q,\text{Nyquist}}, \tag{3.42}$$

where the scaling ratio is called the oversampling ratio (OSR)

$$\text{OSR} = \frac{f_N}{\Delta f} = \frac{f_s}{2\Delta f}. \tag{3.43}$$

Fig. 3.7 visualizes this effect: the input signal to the Nyquist ADC in (a) occupies the whole Nyquist bandwidth up to $\frac{f_s}{2}$. The oversampling ADC in (b) occupies the same bandwidth, but the sampling frequency is doubled. Scaling the sampling frequency does not affect the signal power. But the noise power density—and thus also the overall noise power—is only half as high as in (a). Doubling the OSR doubles the SNR. The DR improves by $10\log(\text{OSR})$:

$$\text{DR} = (1.76 + 6.02B + 0.5 \cdot 20\log(\text{OSR}))\,\text{dB}. \tag{3.44}$$

In contrast to the maximum resolution of 10 bit for Nyquist ADCs, higher resolutions are possible with oversampling ADCs. Doubling the sampling frequency improves the DR by 3 dB and the ENOB by 0.5 bits. The higher sampling frequencies come at the price of higher power consumption and more design constraints [27].

3.2.3 Noise-shaping with delta-sigma modulators (DSM)

Oversampling ADCs make use of the flat noise power spectrum and only sum up the noise inside the signal band. Thermal noise can be modelled by a random variable with a white noise spectrum. The quantization error differs from thermal noise because its exact value can be fed back to the unquantized part of the ADC.

Using this principle, DSMs minimize the quantization error inside the signal band. The analysis and the design of DSMs simplify in z-domain. Fig. 3.8 shows a first-order lowpass DSM: The quantized value is fed back to the input and runs through an integrator to the quantizer. The signal input runs through the same path to the quantizer. Signal and quantization noise are uncorrelated and are inserted at different points in the system. They have different transfer functions—the signal transfer function (STF) and the noise transfer function (NTF). The STF should not alter the signal inside the signal band. The magnitude of the NTF should be low inside the signal band and can be high elsewhere. The quantization noise in the output is no longer flat but shaped away from the signal band. Hence, DSMs are also called noise shaping ADCs. Fig. 3.7c shows the noise spectrum of a DSM. The quantization noise within the sampling bandwidth is the same for all ADCs. The quantization noise within the signal bandwidth for the DSM is significantly lower than for the other ADCs.

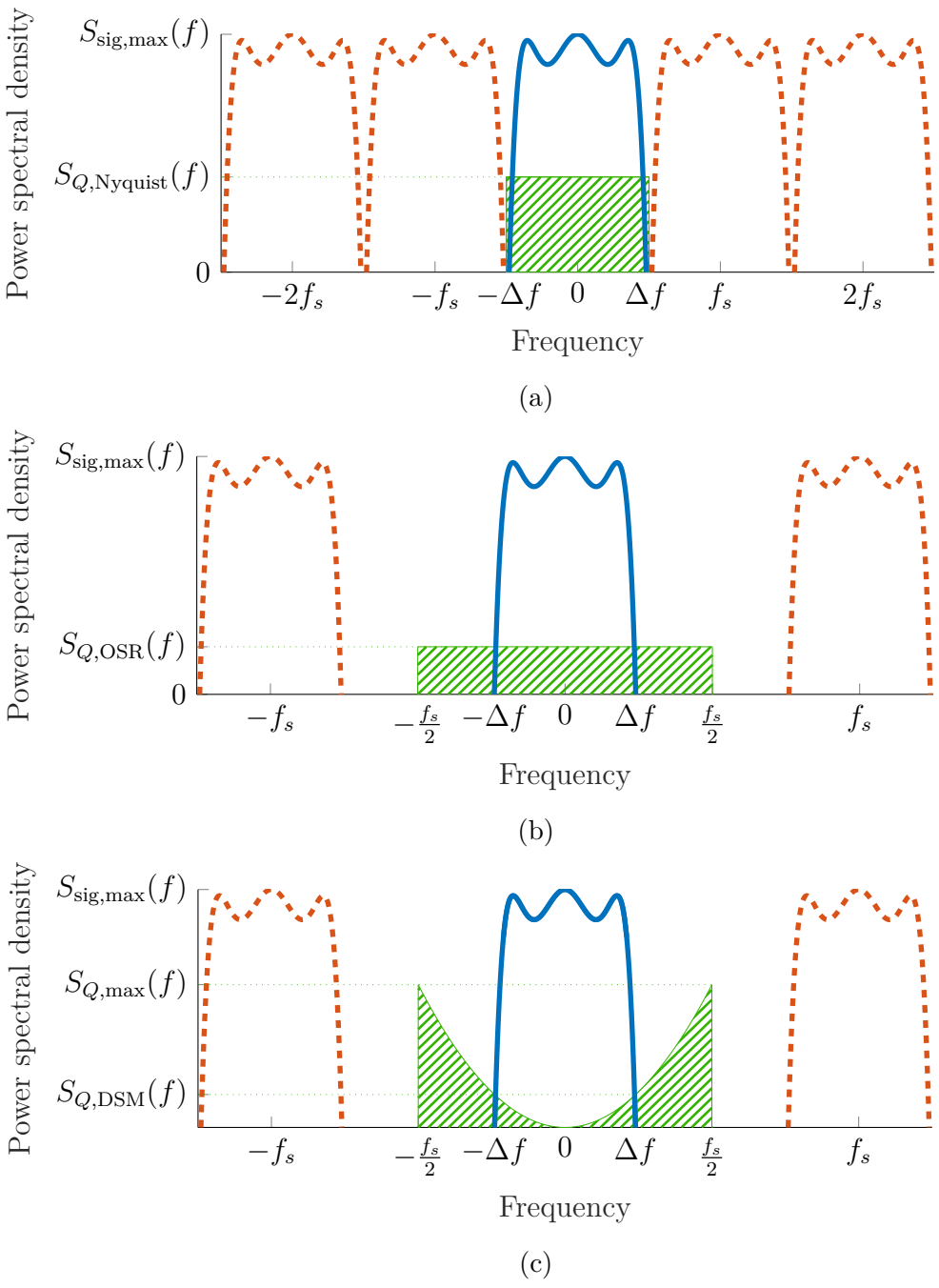


Figure 3.7: (a) Nyquist ADC, (b) oversampling ADC where $\frac{f_s}{2} \gg \Delta f$ and (c) DSM ADC with shaped quantization noise. The quantization noise power is represented by the green, hatched area. Note that the total noise power is the same for all three ADCs, the area has the same size. However, the effective noise power is the area within the bandwidth from $-\Delta f$ to Δf. The noise-shaping ADC in (c) has a significantly lower effective noise power than the Nyquist ADC in (a).

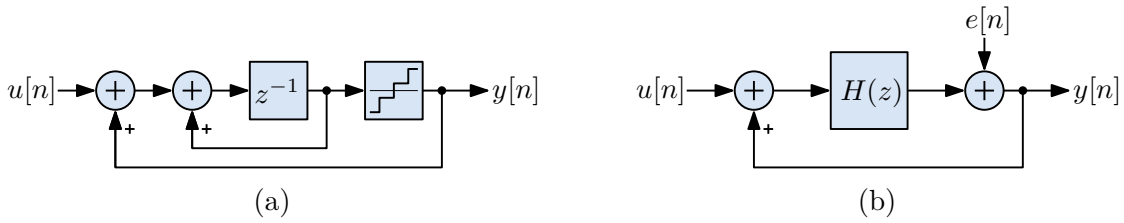


Figure 3.8: (a) First-order low-pass delta-sigma modulator and (b) corresponding simplified model with additive white Gaussian noise (AWGN) instead of the quantizer.

The STF and NTF of DSMs are defined implicitly by their contribution to the output signal $Y(z)$

$$Y(z) = \mathrm{STF}(z)U(z) + \mathrm{NTF}(z)E(z), \tag{3.45}$$

where $U(z)$ and $E(z)$ are the input signal and the quantization noise, respectively. The quantization noise is only an approximation and some real DSMs show non-idealities caused by correlation between the quantizer and the input or by a distorted amplitude probability density function of the quantizer. Nevertheless, the assumptions about the quantizer in (3.35), (3.36), (3.37) are sufficient for the analysis and the design of DSMs [28], [29].

For the DSM in Fig. 3.8, the STF and the NTF can be expressed with the transfer function $H(z)$:

$$\begin{aligned} \mathrm{STF}(z) &= \frac{H(z)}{1 - H(z)}, \\ \mathrm{NTF}(z) &= \frac{1}{1 - H(z)}. \end{aligned} \tag{3.46}$$

The DR of a DSM depends strongly on the loop filter $H(z)$ and especially on the order of the polynome in z. To estimate the large improvement of the DR, the first-order low-pass DSM in Fig. 3.8 is analyzed and then generalized to L^{th}-order:

With the implicit equation for the output $Y(z)$ of an integrator (cf. Fig. 3.9)

$$Y(z) = z^{-1}X(z) + z^{-1}Y(z), \tag{3.47}$$

the transfer function $H(z)$ can be derived to

$$H(z) = H_{\mathrm{integrator}}(z) = \frac{Y(z)}{X(z)} = \frac{z^{-1}}{1 - z^{-1}}. \tag{3.48}$$

With $H(z)$ and (3.46) the STF and the NTF can be expressed as:

$$\begin{aligned} \mathrm{STF}(z) &= z^{-1}, \\ \mathrm{NTF}(z) &= 1 - z^{-1}. \end{aligned} \tag{3.49}$$

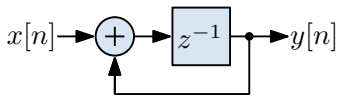


Figure 3.9: z-domain model of a delaying integrator.

The STF introduces a delay to the signal. That does not change the magnitude output spectrum. The NTF is a differentiator or—as desired for the noise—a high pass filter.

In continuous-time, z maps to $z = e^{j\omega T_s}$. With the DTFT, (3.27) the noise spectral density $S_Q(f)$ at the output of the modulator becomes [28]–[31]

$$\begin{aligned} S_Q(f) &= S_{Q,\text{Nyquist}}(f)\,|\text{NTF}(f)|^2 \\ &= S_{Q,\text{Nyquist}}(f)\left|1 - e^{-\omega T_s}\right|^2 \\ &= S_{Q,\text{Nyquist}}(f) 4\sin^2\left(\pi\frac{f}{f_s}\right). \end{aligned} \tag{3.50}$$

The total noise power P_Q at the output is the integral of the noise spectral density inside the signal band. The bandwidth is small in comparison to the sampling frequency, so the sine function can be linearly approximated with $\sin\left(\pi\frac{f}{f_s}\right) = \pi\frac{f}{f_s}$. The output noise power P_Q

$$\begin{aligned} P_Q = \int_{-\Delta f}^{\Delta f} S_Q(f)\mathrm{d}f &= P_{Q,\text{Nyquist}}\frac{\pi^2}{3}\left(\frac{1}{\text{OSR}}\right)^3 \\ &= \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{1}{\text{OSR}}\right)^3. \end{aligned} \tag{3.51}$$

depends on the OSR to the power of three. The first order noise shaping is three times more effective than oversampling alone in (3.42).

In the literature the DR of DSMs is calculated for a full-scale sinusoid like for other ADCs [29], [30].

$$\begin{aligned} \text{DR} &= 10\log\left(\frac{P_\text{sig}}{P_{Q,\text{Nyquist}}}\right) \\ &= \left(-3.41 + 6.02n + 1.5\cdot 20\log\left(\text{OSR}\right)\right)\text{dB}. \end{aligned} \tag{3.52}$$

Doubling the OSR improves the DR by 9 dB and the ENOB by 1.5 bit.

Real DSMs are only conditionally stable. The maximum signal amplitude is considerably lower than the full-scale sinusoid and the derived DR is too optimistic for real DSMs. For Nyquist and oversampling ADCs, the maximum output value of the quantizer defines the maximum output amplitude. If the input signal exceeds the corresponding maximum input signal, the output signal will be clipped. The associated distortions are temporary and disappear as soon as the input signal decreases below the maximum input signal.

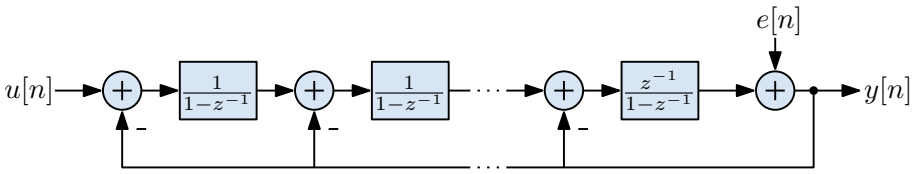


Figure 3.10: Generalized delta-sigma modulator with distributed feedback topology. The modulator consists of one delaying intgrator in front of the quantizer and $L-1$ delay-free integrators.

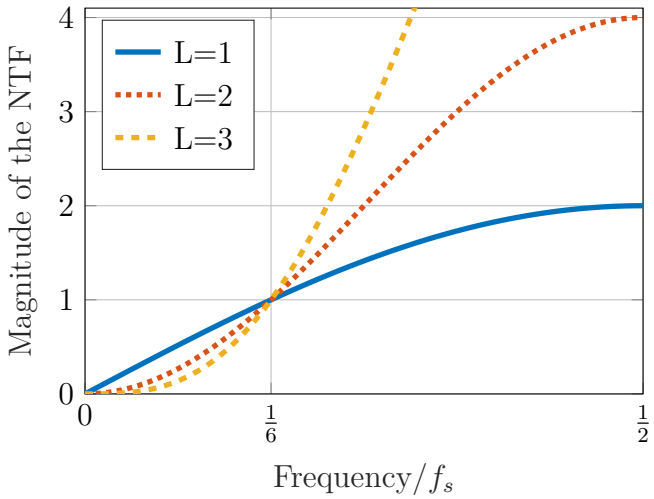


Figure 3.11: Magnitude of the NTF vs. the normalized frequency of the low-pass DSM in Fig. 3.10 with order $L = 1$, $L = 2$ and $L = 3$.

DSMs have a filter, internal states and a non-linear feedback loop. Typically, one of the internal states overloads well before the maximum quantizer output amplitude is reached. For linear systems with feedback, stability analysis accurately predicts the maximum input and output amplitudes. The non-linear quantizer impedes an analytical analysis. The approximation of the quantizer with AWGN yields good results for the design process and can indicate where the limit to instability may be. For a given DSM, a simulation sweep across the input amplitude is the best way to determine the maximum signal amplitude.

Higher order DSMs offer better noise shaping, especially near the poles of the NTF. Numerous ways for implementation exist where each has its own advantages and drawbacks [28], [29], [32], [33]. The single-loop distributed feedback topology is popular because of its robustness against process variation. Fig. 3.10 shows the straightforward form where all feedback coefficients are equal to 1. Its NTF is a general form of the discussed first-order NTF:

$$\mathrm{NTF}(z) = \left(1 - z^{-1}\right)^{L}. \tag{3.53}$$

Fig. 3.11 shows the magnitude of the NTF for different modulator orders.

The total noise power of the L^{th}-order modulator can be derived analogously to the

first-order modulator [30]:

$$S_Q(f) = S_{Q,\text{Nyquist}}(f)\left|1 - e^{-\omega n T_s}\right|^{2L} = \frac{\Delta^2}{12}\frac{\pi^{2L}}{2L+1}\left(\frac{1}{\text{OSR}}\right)^{2L+1}. \tag{3.54}$$

Again a full-scale sinusoid is assumed for the calculation of the DR

$$\begin{aligned}\text{DR} &= 10\log\left(1.5 \cdot \frac{2L+1}{\pi^{2L}}\text{OSR}^{2L+1}2^B\right)\\ &= 1.76 + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) + 6.02B + (2L+1)\cdot 10\log\left(\text{OSR}\right).\end{aligned} \tag{3.55}$$

For the cases $L = 1$ to $L = 3$, the DR becomes

$$\begin{aligned}\text{DR}\Big|_{L=1} &= \left(-3.41 + 6.02B + 1.5 \cdot 20\log\left(\text{OSR}\right)\right)\text{dB},\\ \text{DR}\Big|_{L=2} &= \left(-11.14 + 6.02B + 2.5 \cdot 20\log\left(\text{OSR}\right)\right)\text{dB},\\ \text{DR}\Big|_{L=3} &= \left(-19.62 + 6.02B + 3.5 \cdot 20\log\left(\text{OSR}\right)\right)\text{dB}.\end{aligned} \tag{3.56}$$

Doubling the OSR is equivalent to an increase of the ENOB by 1.5 bit, by 2.5 bit or even by 3.5 bit for a first-, a second- or a third-order modulator. The main drawback of higher modulator orders is not seen in this calculus: the higher the modulator order the higher becomes the tendency to instability. In addition, higher modulator orders increase design complexity, power consumption, non-idealities and the impact of parasitics because of the larger distances between the circuit components.

3.3 Continuous-Time Bandpass Delta-Sigma Modulator

This section describes the architecture of the implemented CT-BPDSM. It follows closely the state of the art of $f_s/4$-CT-BPDSMs in Ref. [34]–[37] and especially in Ref. [38], [39]. The architecture is based on a discrete-time lowpass prototype that is converted to a continuous-time highpass modulator.

3.3.1 Discrete-time loop filter

The second-order modulator with distributed feedback [40] is chosen for this work. With the definition of the NTF (3.46) and the NTF of the distributed feedback modulator in (3.53), the transfer function of the lowpass DSM becomes

$$\begin{aligned}H_{\text{LP,d}}(z) &= \frac{\text{NTF}(z) - 1}{\text{NTF}(z)}\\ &= \frac{-2z^{-1} + z^{-2}}{\left(1 - z^{-1}\right)^2}.\end{aligned} \tag{3.57}$$

A lowpass filter can be converted to a bandpass filter with any center frequency by suitable mapping of z [41]. For the especially simple mapping $z \to -z^2$, the center frequency f_0 becomes [35]

$$f_0 = \frac{f_s}{4}. \tag{3.58}$$

The bandpass transfer function is

$$H_{\mathrm{BP,d}}(z) = H_{\mathrm{LP,d}}(-z^2) = \frac{2z^{-2} + z^{-4}}{\left(1 + z^{-2}\right)^2}. \tag{3.59}$$

In Chap. 4.3.6 the metastability of sampling latches is analyzed. With (3.25), the term z^{-1} in z-domain is equivalent to one digital delay in discrete-time domain. The delay is separated from the transfer function $H_{\mathrm{BP,d}}(z)$ and implemented as an additional half latch stage [39]. The additional stage mitigates metastability. The transfer function that is implemented with the continuous-time loop filter is

$$H^*_{\mathrm{BP,d}}(z) = zH_{\mathrm{BP,d}}(z) = \frac{2z^{-1} + z^{-3}}{\left(1 + z^{-2}\right)^2}. \tag{3.60}$$

3.3.2 Impulse-invariant transformation

Several ways for conversion between discrete-time and continuous-time filters exist [19]. The best suited conversion for CT-BPDSM is the impulse-invariant transformation: the continuous-time modulator becomes equivalent to the discrete-time modulator if the inputs to the quantizers are equal at the sampling instant. This is identical to the sampling condition for ADCs (3.28).

The output of the quantizer stays constant for one clock period. The sampling condition is met if the impulse responses to the quantizer output are identical for both modulators. This impulse-invariant transformation is known from switched-capacitor design [42] and can be applied to CT-BPDSM design in frequency domain [35] or in time domain [34]:

$$\mathcal{Z}^{-1}\left\{H_{\mathrm{BP,d}}(z)\right\} = \mathcal{L}^{-1}\left\{D(s)H_{\mathrm{BP,c}}(s)\right\}\Big|_{t=nT_s}, \tag{3.61}$$

$$h_{\mathrm{bp,d}}(n) = d(t) * h_{\mathrm{bp,c}}(t)\Big|_{t=nT_s}. \tag{3.62}$$

$H_{\mathrm{BP,c}}(s)$, $D(s)$, $h_{\mathrm{bp,d}}(n)$, $d(t)$, $h_{\mathrm{bp,c}}(t)$ are the continuous-time loop filter, the Laplace transform of the DAC pulse, and the time domain variables for the discrete-time loop filter, the DAC pulse and the continuous-time loop filter, respectively.

Fig. 3.12 shows common feedback pulses. The straightforward feedback pulse—the non-return-to-zero (NRZ) pulse—is active for a full period. The loop filter of the CT-BPDSM has four coefficients, but only two resonators. To implement the desired loop filter, the transfer functions of the resonators could be adjusted. Mismatch and parasitics impede this effort. Instead, Ref. [43] proposes a multi-feedback architecture with modified DAC

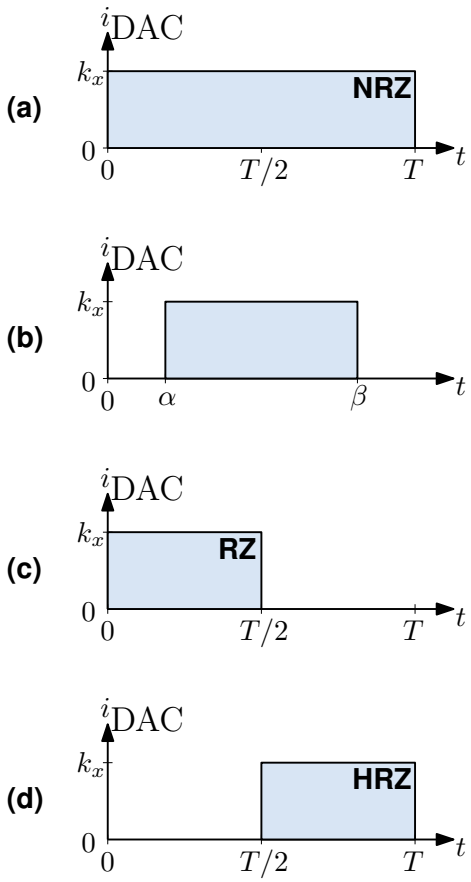


Figure 3.12: Rectangular DAC feedback pulses for a CT-BPDSM: (a) a non-return to zero (NRZ) pulse; (b) a generalized feedback pulse which begins at $t = \alpha$ and ends at $t = \beta$; (c) a return to zero (RZ) pulse and (d) a half return to zero (HRZ) pulse; this pulse is the same as a digital delay followed by the RZ pulse.

pulses: a return-to-zero (RZ) pulse and a half-return-to-zero (HRZ) pulse replace the NRZ pulse. Fig. 3.13 shows the corresponding DSM model. The model already includes the digital delay from (3.60).

In the following, a normalized sampling period of

$$T_s = 1 \tag{3.63}$$

renders the equations more concise for the calculations. In the end, the Laplace variable s must be replaced by sT_s. With that simplification the DAC pulses are defined in

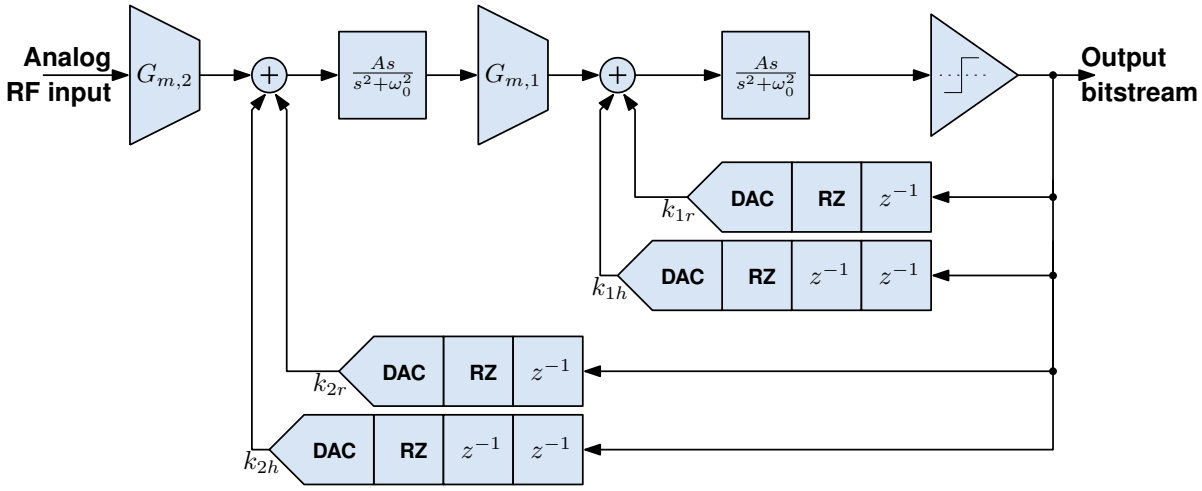


Figure 3.13: Model of the implemented CT-BPDSM with four feedback paths and RZ and HRZ DAC feedback pulses.

time-domain by

$$
\begin{aligned}
d_{\mathrm{NRZ}}(t) &= \begin{cases} 1 \text{ for } 0 \leq t < 1 \\ 0 \text{ otherwise} \end{cases}, \\
d_{\alpha,\beta}(t) &= \begin{cases} 1 \text{ for } \alpha \leq t < \beta \\ 0 \text{ otherwise} \end{cases}, \\
d_{\mathrm{RZ}}(t) &= \begin{cases} 1 \text{ for } 0 \leq t < 0.5 \\ 0 \text{ otherwise} \end{cases}, \\
d_{\mathrm{HRZ}}(t) &= \begin{cases} 1 \text{ for } 0.5 \leq t < 1 \\ 0 \text{ otherwise} \end{cases}.
\end{aligned} \tag{3.64}
$$

and in s-domain by

$$
\begin{aligned}
D_{\mathrm{NRZ}}(s) &= \frac{1 - e^{-s}}{s}, \\
D_{\mathrm{RZ}}(s) &= \frac{1 - e^{-0.5s}}{s}, \\
D_{\alpha,\beta}(s) &= \frac{e^{-\alpha s} - e^{-\beta s}}{s}, \\
D_{\mathrm{HRZ}}(s) &= e^{-0.5s} \frac{1 - e^{-0.5s}}{s}.
\end{aligned} \tag{3.65}
$$

The conversion between discrete-time and continuous-time is cumbersome if done manually. Fortunately, the problem is already solved for many cases. The z-transform and the Laplace transform are linear, so the transfer functions of practical systems can be expressed by a linear combination of previous solutions. The procedure is as follows: a

DAC pulse shape is selected. The discrete-time prototype is expanded into partial fractions and each of the fractions is converted to s-domain with the tables in [28], [39].

An alternative approach is the design in state-space. Conversions between transfer function and state-space, and between discrete-time and continuous-time are standard tasks in Matlab [44]. Design in state-space separates the transfer function and the DAC pulses, so both can be designed separately. The DAC pulses contribute only to the input matrix B of the state-space system. For rectangular pulses, the calculation of B can be found in Ref. [29], [45].

3.3.3 Feedback coefficients for the multi-feedback architecture

With this recipe, any discrete-time transfer function with any rectangular DAC pulse can be converted to continuous-time and vice versa. Following the approach in Ref. [43], the resonator transfer function in continuous-time is chosen first. The poles of the transfer function must match those of the discrete-time loop filter in (3.60). The LC-filter in Chap. 4.6 implements the $f_s/4$ resonance frequency and is chosen in this work. The transfer function

$$\begin{aligned} H_{\mathrm{LC,c}}(s) &= \frac{\text{Resonator output voltage}}{\text{Resonator input current}} \\ &= \frac{1}{Y_{\mathrm{LC}}} = \frac{s\frac{1}{C}}{s^2 + \frac{1}{LC}} = \frac{As}{s^2 + \omega_0^2} \end{aligned} \tag{3.66}$$

depends on the resonance frequency ω_0 and the amplification A. The normalization of the sampling period (3.63) also affects the resonance frequency $\omega_0 = 2\pi\frac{f_s}{4} = \frac{\pi}{2}$. The amplification A is a linear scaling factor. It is set to $\frac{\pi}{2}$ [43]. With these assumptions, the prototype for the continuous-time resonator is

$$H_{\mathrm{proto,c}}(s) = \frac{\frac{\pi}{2}s}{s^2 + \left(\frac{\pi}{2}\right)^2}. \tag{3.67}$$

The equivalent discrete-time transfer functions for the first resonator in front of the quantizer are calculated with Matlab [39], [43]. The transfer function for the RZ DAC pulse $H_{\mathrm{1r,d}}(z)$ is

$$H_{\mathrm{1r,d}}(z) = \frac{\left(1 - \frac{1}{\sqrt{2}}\right)z - \frac{1}{\sqrt{2}}}{z^2 + 1}. \tag{3.68}$$

The transfer function for the HRZ DAC pulse $H_{\mathrm{1h,d}}(z)$ is

$$H_{\mathrm{1h,d}}(z) = -\frac{\left(1 - \frac{1}{\sqrt{2}}\right) - \frac{1}{\sqrt{2}}z}{z^2 + 1}. \tag{3.69}$$

For the second resonator in front of the quantizer, the discrete-time transfer functions $H_{\mathrm{2r,d}}(z)$ and $H_{\mathrm{2h,d}}(z)$ are calculated analogously. The signal from the DAC crosses two

resonators, so the continuous-time transfer function is given by the squared resonator transfer function $H^2_{\mathrm{proto,c}}(s)$.

The sum of the scaled transfer functions is equated to the desired loop filter $H_{\mathrm{BP,d}}(z)$:

$$k_{1r}H_{\mathrm{1r,d}}(z) + k_{1h}H_{\mathrm{1h,d}}(z) + k_{2r}H_{\mathrm{2r,d}}(z) + k_{2h}H_{\mathrm{2h,d}}(z) \stackrel{!}{=} H_{\mathrm{BP,d}}(z) \tag{3.70}$$

The scaling factors k_{1r}, k_{1h}, k_{2r} and k_{2h} are the feedback coefficients of the DACs. They can be determined by comparison of the numerator polynomials in z.

The final step is renormalization of the feedback coefficients. The time period T_s is reintroduced and the renormalization factor $\left(\frac{\pi}{2}C\right)$ is absorbed into the feedback coefficients

$$\begin{aligned}
k^*_{1r} &= \frac{\pi C}{2T_s}k_{1r},\\
k^*_{1h} &= \frac{\pi C}{2T_s}k_{1h},\\
k^*_{2r} &= \frac{1}{G_{m,1}}\left(\frac{\pi C}{2T_s}\right)^2 k_{2r},\\
k^*_{2h} &= \frac{1}{G_{m,1}}\left(\frac{\pi C}{2T_s}\right)^2 k_{2h}.
\end{aligned} \tag{3.71}$$

The signal from the feedback DAC on the left hand side of Fig. 3.13 runs through both resonators and through the transconductance $G_{m,1}$; therefore, the coefficients k^*_{2r}, k^*_{2h} are scaled accordingly.

The feedback coefficients have the unit of a transconductance and can be converted into feedback currents by multiplication with an arbitrary voltage. The transconductance $G_{m,1}$ is scaled with the sum $k^*_{2r} + k^*_{2h}$:

$$G_{m,1} = \frac{1}{k^*_{2r} + k^*_{2h}}\frac{\pi}{2}\left(\frac{C}{T_s}\right)^2. \tag{3.72}$$

The resonator converts the input current and the feedback currents into a voltage. Fig. 3.14 shows the resonator voltages inside a CT-BPDSM. From the signal processing perspective, the absolute value of the currents and the resonator voltage is arbitrary: the transfer function remains the same if the input transconductance and all feedback coefficients through the resonator are scaled with the same factor.

From the circuit design perspective, a large resonator voltage means large signal power and large SNR. But a large resonator voltage also means high distortion. There is no analytical solution for the design optimum of the scaling factors. The best scaling can be found by stochastic estimation with formulas from Ref. [38], [39] or by experiment.

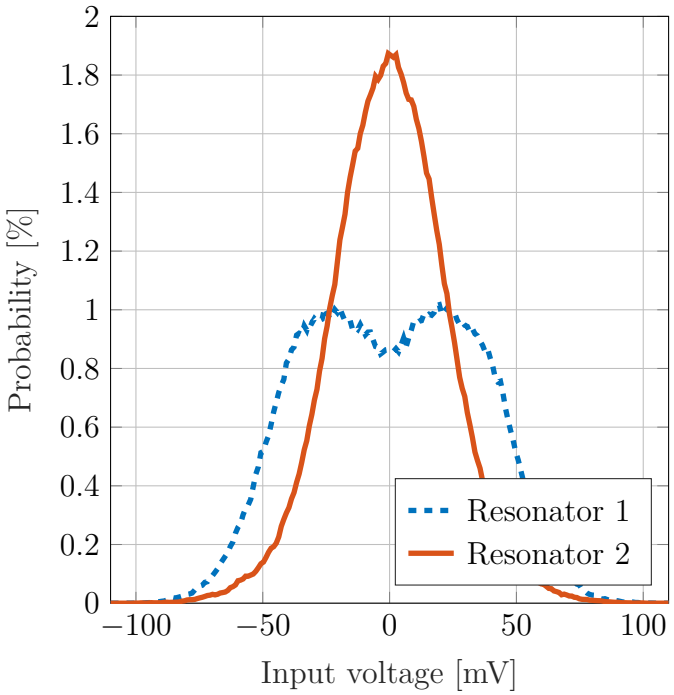


Figure 3.14: Histogram of the resonator voltages in the implemented CT-BPDSM. The bin size is 1 mV.

4 Circuit Design

This chapter gives an overview over the circuits used in the BPDSM. The reader is introduced to DC and RF characteristics of BJTs. Circuits like current sources, the emitter follower, the differential amplifier (DA) and the current-mode logic latch (CML latch) are sketched. The description touches several topics in high-speed analog circuit design in a bipolar process. But it is stripped down to the necessary details for the design of a BPDSM. The majority of the expressions in this part are state of the art and are well described in many text books [8], [31], [46]–[50].

This work extends the state of the art for tunable TCAs and switchable capacitors for configurable loop filters [51], [52]. Therefore, these circuits are explained in more detail.

All simulations use the transistor model (Gummel-Poon) from the process design kit of the bipolar technology B7HF200 from Infineon.

4.1 DC Operation of Bipolar Junction Transistors

Fig. 4.1 shows the structure and the circuit symbol of an npn BJT. The BJT has three terminals, called emitter (E), base (B) and collector (C). The emitter is the source of the charge carriers that are emitted into the base. It is heavily doped to increase the number of emitted carriers. The base is lightly doped and very thin. It is called base for historical reasons: in the first transistor a slab of Germanium was used as base or support for needles which served as emitter and collector [53], [54]. Most of the charge carriers from the emitter pass directly through the base to the collector without recombining. The collector is the sink of the carriers. Its doping level is in between the base doping level and the emitter doping level. In modern bipolar technologies, it is situated at the bottom of the stack and connected to the side.

The performance of a BJT depends on the dimensions of the base. A small base width—the distance between collector and emitter—is good for amplification and for speed. Lithography defines the minimum feature size in horizontal direction. In vertical direction the minimum size is the layer thickness which is determined by the epitaxy process. Epitaxy thickness can be controlled much better than horizontal structures. Therefore, the npn layer stack is oriented in vertical direction.

4.1.1 Regions of operation

The BJT can be seen as two pn-diodes connected together. Each of the diodes can be either forward or reverse biased. That results in four different operating regions for a BJT:

1. Forward-active: the base-emitter diode is forward biased and the base-collector diode is reverse biased. This is the normal amplification mode of the BJT.

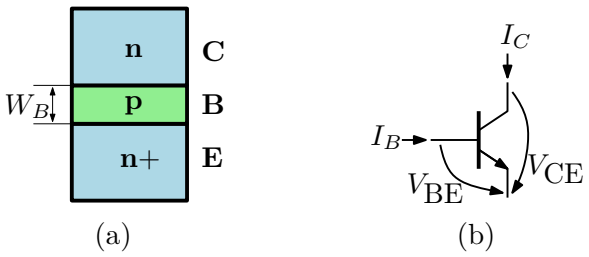


Figure 4.1: (a) An npn BJT in a bipolar process consists of a vertical stack of an n-doped collector (**C**), a thin p-doped base (**B**) and a highly n-doped emitter (**E**). The base width W is kept as small as possible to increase the collector current density and the maximum bandwidth. (b) Electrical symbol of an npn BJT.

2. Cut-off: both diodes are reverse biased. The BJT is switched off.

3. Saturation: both pn-junctions are forward biased. In this region of operation, the effective current gain is low; an increase in base current will no longer lead to an increase of collector current. As well, the base is flooded by carriers and switching off the BJT will need much longer than in forward-active mode.

4. Reverse-active: the base-collector diode is forward biased and the base-emitter diode is reverse-biased. This is similar to forward-active where emitter and collector change places. However, BJTs are asymmetrical devices and the current gain is much lower in reverse-active.

Most circuit designs use only the forward-active mode and the cut-off mode. It should be ensured that no BJT in the signal path goes into saturation. In the following, only the forward-active mode will be described.

4.1.2 Current amplification

Most circuit designes use BJTs as a current controlled current source with the current gain

$$\beta = \frac{I_C}{I_B}, \tag{4.1}$$

where I_C is the collector current and I_B is the base current (Fig. 4.1b). The circuit designer can scale the collector current I_C with the emitter area A_E of the BJT:

$$I_C \approx A_E J_C. \tag{4.2}$$

Lithography sets a lower bound for the emitter area. The upper bound is determined by heating and electromigration.

The relationship between collector current density J_C and the base-emitter voltage V_{BE} follows an exponential

$$J_C = J_S e^{\frac{v_{\mathrm{BE}}}{V_T}}, \tag{4.3}$$

where J_S is the saturation current density. The thermal voltage V_T is given by

$$V_T = \frac{kT}{q}, \tag{4.4}$$

where k is the Boltzmann constant and q is the elementary charge. V_T is proportional to the absolute temperature T. At room temperature, V_T is approximately 25 mV. However, practical values will be higher due to self-heating of the BJT. In this work, a junction voltage of 50 K above room temperature is used. The corresponding thermal voltage is $V_T = 30\,\text{mV}$. The technology parameter J_S depends on doping concentrations and is proportional to the inverse effective base width $J_S \propto W_{\text{B,eff}}$.

In a circuit, the emitter area is known and (4.3) is rewritten with currents instead of current densities:

$$I_C = I_S e^{\frac{v_{\text{BE}}}{V_T}}, \tag{4.5}$$

where I_S denotes the saturation current.

The Early effect describes the base width modulation in a BJT. The effective base is the neutral region between the depletion regions of the collector-base junction and the base-emitter junction. For a larger collector-emitter voltage V_{CE} the depletion region of the collector-base junction grows. Therefore, the effective base width becomes smaller than the drawn base width W_B and the collector current density rises.

The Early voltage V_A quantifies this effect. It can be determined directly from the BJT output characteristic (cf. Fig. 4.2): the tangent to any collector current curves intersects with the x-axis at the negative Early voltage $-V_A$. With the Early effect, the expression for the collector current density changes to

$$I_C \approx I_S e^{\frac{V_{\text{BE}}}{V_T}} \left(1 + \frac{V_{\text{CE}}}{V_A}\right). \tag{4.6}$$

Three high current effects stop the exponential growth of the collector current density J_C. The first is called the high-level injection effect. For large V_{BE}, the minority carrier density exceeds the base doping concentration. As a consequence, the slope of the collector current density is halved in log scale to $e^{\frac{V_{\text{BE}}}{2V_T}}$. The knee current density J_{KF} determines the current density where the slope changes (cf. Fig. 4.3).

The second reason for the decrease in the slope is the parasitic emitter resistor R_E. The exponential growth of J_C reduces to linear growth because the IR voltage drop across R_E is proportional to the collector current.

Thirdly, the heat distribution in an active BJT is not uniform. The temperature in the middle is larger than at the edges and the current density depends exponentially on the temperature. The result is a positive feedback between current density and heat. Therefore, the effective emitter area and the total current are reduced. Typically, the design rules of modern bipolar technologies prohibit emitter areas where non-uniform heating plays a role.

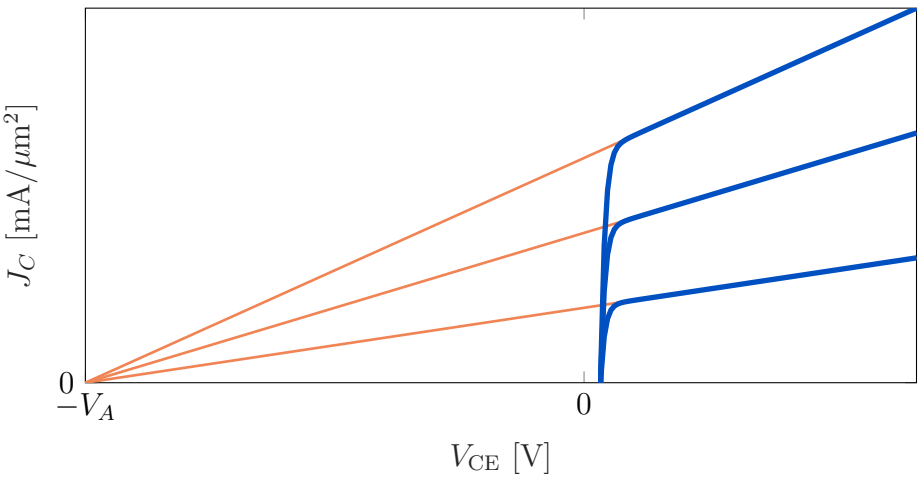


Figure 4.2: Collector current vs. the collector-emitter voltage V_{CE}. The tangents of the I_C curves intersect the x-axis at the negative Early voltage V_A.

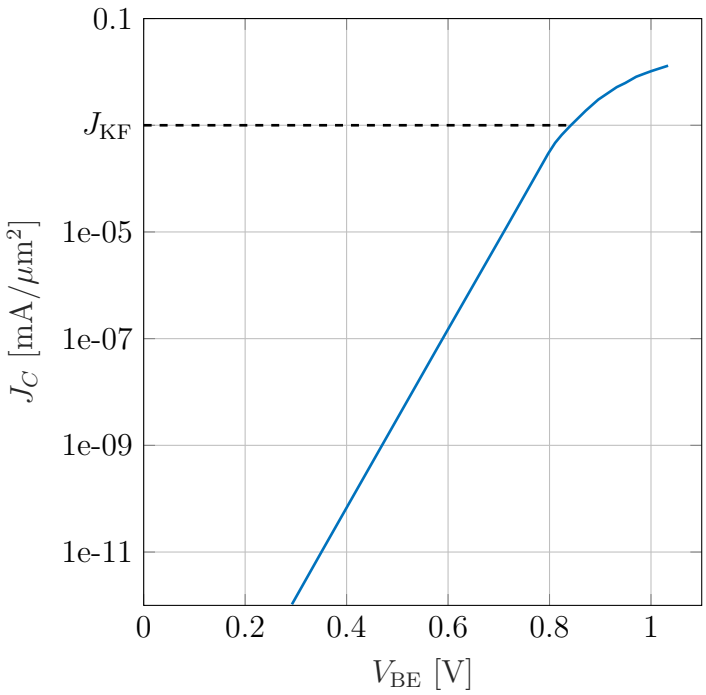


Figure 4.3: Collector current density J_C vs. the base-emitter voltage V_{BE}. Reproduced plot with data from [55]. The relationship of J_C vs. V_{BE} in the bipolar technology B7HF200 is similar but must not be disclosed.

4.2 High-Speed Analog Design with Bipolar Junction Transistors

4.2.1 Single-stage amplifier topologies for bipolar junction transistors

Six permutations exist to distribute an input, an output and a common node onto the three terminals of a BJT. Only three of them offer reasonable amplification in forward-active mode (the other three permutations are obtained by exchanging input and output of the three basic types). The amplifier topologies are named by the common node: common-emitter, common-collector and common-base amplifier. They form the basis for all analog circuits in this work. They are listed in Fig. 4.4. The circuits use a collector resistor R_C or an emitter resistor R_E or both. For some applications, a larger resistance is needed and a current source replaces the resistor.

The common-emitter circuit in Fig. 4.4a is the main amplifier circuit because of its high, negative gain. The gain depends strongly on temperature, process mismatch and bias current. For digital circuits, the high gain results in fast switching and gain variations are tolerable; for analog circuits, the gain must be known in the design phase. Fig. 4.4b shows the common-emitter circuit with an additional emitter resistor. The resistor mitigates the effect of temperature, mismatch and bias conditions but also reduces the voltage gain to about $A_v = -R_C/R_E$. The common-emitter circuit has a high input resistance and an output resistance determined by R_C.

The Miller effect limits the bandwidth of a common-emitter circuit: the capacitance C_{CB} between the collector and the base acts as feedback from the output back to the input. A voltage change of Δv at the input results in the (negative) voltage change of $A_V \Delta v$ at the output. That increases the effective input capacitance to the Miller capacitance $(1 - A_V)C_{\mathrm{CB}}$.

The common-collector circuit in Fig. 4.4c has a maximum current gain of β and a voltage gain of 1. The topology is better known as emitter follower because the emitter voltage is one junction voltage below the input voltage—the emitter voltage follows the input voltage. This work will use the naming "emitter follower" in the following. The circuit has a high input resistance and a low output resistance. That makes it a good voltage buffer.

The common-base circuit in Fig. 4.4d has a maximum voltage gain of $g_m R_C$ and a current gain of 1. It has a low input resistance and a high output resistance. That makes it a good current buffer. The common-base circuit is often used in conjunction with a common-emitter circuit with high negative voltage gain. The common-base circuit separates the amplifier from the load and reduces the effective input capacitance. That increases the bandwidth of the overall circuit.

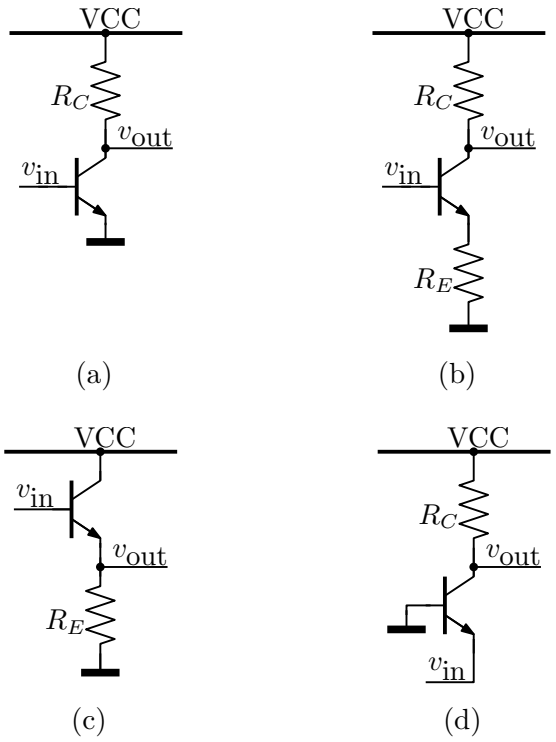


Figure 4.4: (a) Common-emitter circuit, (b) common-emitter circuit with resistive emitter degeneration, (c) common-collector circuit or emitter follower and (d) common-base circuit.

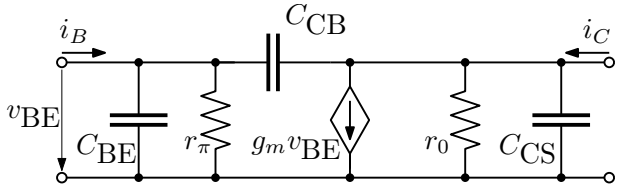


Figure 4.5: High-frequency hybrid-π model of a common-emitter circuit.

4.2.2 Small-signal model of the common-emitter circuit

The small-signal model in Fig. 4.5 shows the hybrid-π model of a BJT in common-emitter topology. The junctions at the collector-substrate, at the collector-base and at the base-emitter interfaces introduce depletion capacitances $C_{\text{CS}}, C_{\text{CB}}$ and $C_{\text{j,BE}}$. C_{CS} is the output capacitance. The junction capacitance is determined by the stored charge in the depletion region of the pn-junction. Its value depends on the doping level in the p and n regions and on the area of the junction. Despite the low doping level of the collector, the output capacitance C_{CS} is the largest of the three because of the large area of the junction.

A low C_{CB} is especially desirable for high-speed applications because it connects the output back to the input. The effective feedback capacitance—the so-called Miller capacitance C_{M} —is the junction capacitance C_{CB} amplified by the negative voltage gain

A_V:

$$C_{\mathrm{M}} = (1 - A_V)C_{\mathrm{CB}} \tag{4.7}$$

High voltage gain will inevitably lead to a large effective capacitance.

The input capacitance C_{BE} is determined by the junction capacitance and the diffusion capacitance C_d:

$$C_{\mathrm{BE}} = C_{\mathrm{j,BE}} + C_d. \tag{4.8}$$

The diffusion capacitance C_d depends on the current flow through the BJT: the collector current is dominated by diffusion of minority carriers in the base. These must be removed to turn off a BJT. The stored charge can be expressed by $Q_b = \tau_b I_C$ where τ_b is the base transit time. The small-signal capacitance C_d is the derivative with respect to the input voltage:

$$C_d = \frac{\mathrm{d}Q_b}{\mathrm{d}v_{\mathrm{BE}}} = \tau_B \frac{I_C}{V_T}. \tag{4.9}$$

In active mode, the diffusion capacitance is usually much larger than the junction capacitance.

The resistors and conductances in Fig. 4.5 are all small-signal values. The most important is the transconductance g_m which relates the change of the collector current i_C to the input voltage v_{BE}. Due to the exponential in (4.5) the equation can be simplified: the transconductance only depends on the collector current and the thermal voltage V_T:

$$\begin{aligned} g_m &= \frac{\mathrm{d}I_C}{\mathrm{d}V_{\mathrm{BE}}} = \frac{I_S}{V_T} e^{\frac{v_{\mathrm{BE}}}{V_T}} \\ &= \frac{I_C}{V_T}. \end{aligned} \tag{4.10}$$

The input resistance r_π models the non-zero base current. The base current is proportional to the collector current (4.1), so it has an exponential relationship to v_{BE} as well. The input resistor can be simplified to:

$$r_\pi = \frac{\mathrm{d}V_{\mathrm{BE}}}{\mathrm{d}I_B} = \frac{V_T}{I_B}. \tag{4.11}$$

Ideally, the output resistance should be as high as possible.

A low output resistance reduces the current gain because the current is split onto both—the load and the output resistance. The Early effect limits the output resistance r_0 to

$$r_0 = \frac{\mathrm{d}V_{\mathrm{CE}}}{\mathrm{d}I_C} = \frac{V_A}{I_C}. \tag{4.12}$$

4.2.3 Transit frequency of a bipolar junction transistor

The transit frequency or unity gain frequency f_T is an important metric to estimate the speed of a bipolar technology. It is reached when the small-signal current gain for a zero-impedance load drops to unity. For a BJT, the current gain is the ratio between collector current i_C and base current i_B. Both currents can be calculated directly from the equivalent circuit in Fig. 4.6 [31], [46], [55]:

$$\begin{aligned} i_C &= v_{\mathrm{BE}} g_m \\ i_B &= v_{\mathrm{BE}} \frac{1}{\frac{1}{r_\pi} + sC_{\mathrm{BE}} + sC_{\mathrm{CB}}} \\ \frac{i_C}{i_B} &= \frac{g_m r_\pi}{1 + s\left(C_{\mathrm{BE}} + C_{\mathrm{CB}}\right) r_\pi}. \end{aligned} \tag{4.13}$$

At low frequencies, the capacitances can be neglected and the current gain is equal to the DC current gain β or—with (4.11)—to $g_m r_\pi$. At very high frequencies, the denominator simplifies to $\omega\left(C_{\mathrm{BE}} + C_{\mathrm{CB}}\right)$. This leads to the transit frequency

$$f_T = \frac{g_m}{2\pi\left(C_{\mathrm{BE}} + C_{\mathrm{CB}}\right)}. \tag{4.14}$$

The diffusion capacitance within the base-emitter capacitance depends on the collector current as well. With (4.9) the equation can be rewritten into [31]

$$\left(2\pi f_T\right)^{-1} = \omega_T^{-1} = \left(C_{\mathrm{j,BE}} + C_{\mathrm{CB}}\right) \frac{V_T}{I_C} + \tau_b. \tag{4.15}$$

At low collector current, the junction capacitances at the base-emitter and the collector-base junctions limit the transit frequency. The maximum transit frequency is achieved at high collector current and approaches the inverse of the base transit time τ_b. Going to even higher collector currents will reduce the transit frequency again. At high collector current, the depletion layer at the collector-base junction moves into the collector and away from the base. The effective base width grows. The base transit time and thus the input capacitance increases. The base widening is also known as the Kirk effect.

In Fig. 4.7 the transit frequency vs. the collector current is depicted. In integrated circuits, BJTs for high-speed usage are sized for maximum transit frequency. The current density is in the range of several $\mathrm{mA}/\mu\mathrm{m}^2$. The knee current density is only a little larger. The currents in the signal path are large to increase the signal power. The dissipated power in the BJTs leads to local heating. Careful design is necessary to avoid signal degradation by thermal effects either by increased overall temperature or by mismatch due to asymmetric heating.

The currents in the DC circuitry, for example in the control logic, are much smaller to save power. The lithography poses a limit on the minimum emitter area. Otherwise these circuits could also be designed with a smaller area. As a result, the current densities in the control logic are much lower than in the signal path.

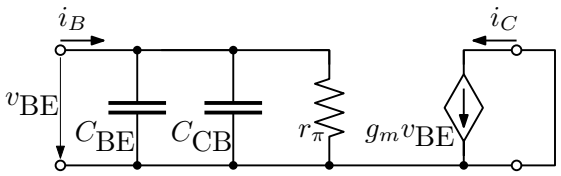


Figure 4.6: Simplified model for the calculation of the transit frequency f_T. The short circuit at the output removes r_0 and C_{CS}, the collector-base junction capacitance is in parallel to the base-emitter capacitance.

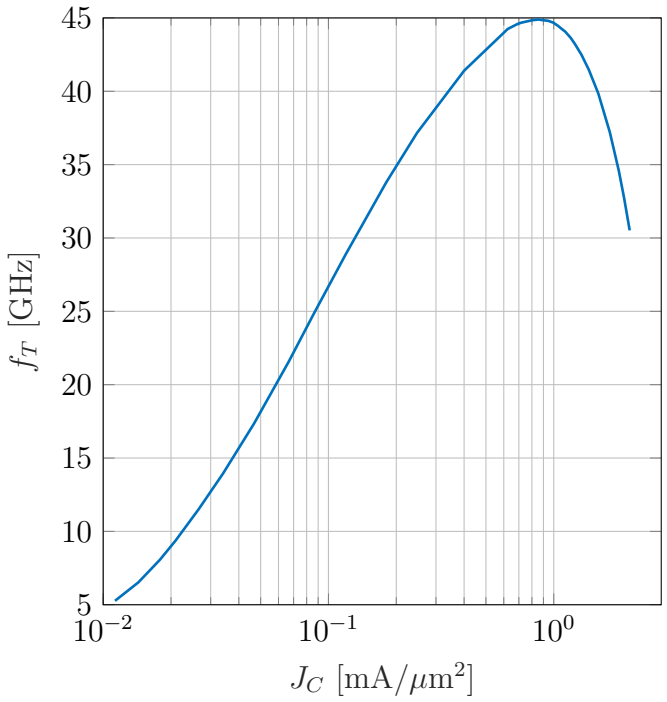


Figure 4.7: Unity gain frequency f_T vs. the collector current density J_C. Reproduced plot with data from [56]. The relationship of f_T vs. J_C in the bipolar technology B7HF200 is similar but must not be disclosed.

4.2.4 Differential circuits

Until here, only *single-ended* voltages have been discussed in this chapter. A single-ended voltage is defined relative to a reference node—the ground (GND) node. In analog RF circuits, most signals are differential voltages: these consist of two single-ended voltages v_p and v_m. The *differential* voltage is defined as the difference of the two:

$$\Delta v = v_p - v_m = \left(\frac{\Delta v}{2} + V_{\mathrm{cm}}\right) - \left(-\frac{\Delta v}{2} + V_{\mathrm{cm}}\right). \tag{4.16}$$

The average voltage is called the common-mode voltage V_{cm}. In comparison to single-ended circuits, differential circuits are larger in size and require more transistors, but they offer many benefits over single-ended circuits: they have a larger signal voltage range, are less susceptible to noise and non-linearity, and have a higher bandwidth.

The larger signal voltage range is understood immediately from the definition. The signal is the difference of two signals. If the two signals have the same voltage range as a single-ended signal, the differential signal has two times that voltage range.

The difference also helps against non-linearity, coupling noise and circuit noise. Even-order non-linearity leads to signal components which have the same sign in the single-ended output voltages. Coupling noise comes from other parts of the circuit, either from the power supply [57] or from large active nodes. A part of the circuit noise stems from bias generators. All of these power components go into the common-mode and not into the differential signal.

Another big advantage of differential circuits is the higher transit frequency they offer with respect to single-ended circuits. The equations for current gain (4.13) and transit frequency (4.14) hold as well for the differential amplifier. They relate the transit frequency to the transconductance of the amplifier and the input capacitances. Fig. 4.8 shows a differential amplifier, the input voltage and the output currents, and the input capacitances of one branch. Both transistors see only half of the differential input voltage v_{in} and produce half of the output current i_p and i_m. The differential output current takes into account both currents, therefore the differential transconductance of the amplifier is the same as in the single-ended case:

$$\Delta i = i_p - i_m = g_m v_{\mathrm{in}}. \tag{4.17}$$

The differential input capacitance is the series capacitance of the transistors' input capacitances. It has only half the size than that of the single-ended case. In the ideal case, the transit frequency is twice as high as that of the single-ended case [8]:

$$f_{T,\mathrm{differential}} = \frac{1}{2\pi}\frac{g_m}{0.5\,(C_{\mathrm{BE}} + C_{\mathrm{CB}})}. \tag{4.18}$$

If mismatch is neglected, a differential circuit is perfectly symmetrical. That simplifies the analysis: for DC analysis, one of the two differential branches is cut out and the common-mode voltage is fed into the input of the other branch. AC analysis becomes even more simple: the voltage of all nodes which are common to both branches are connected to the small-signal ground. It is sufficient to analyze the half circuit—i.e. only one differential branch.

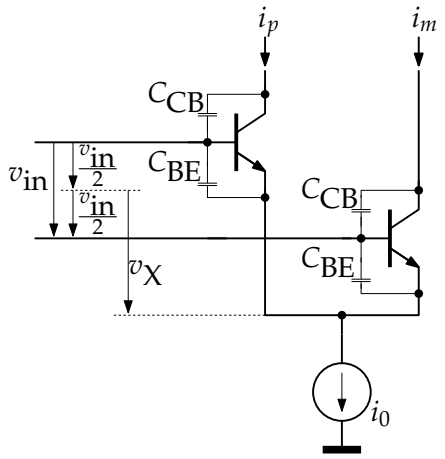


Figure 4.8: A differential pair acts as an f_T-doubler.

4.2.5 Recommendations for high-speed analog design

This section describes the high-frequency properties of BJTs, single-stage BJT amplifiers and differential circuits but lacks advice on how to do the actual design. A few guidelines for good high-speed analog design are presented here:

Where possible, circuits should use the differential topology. All BJTs should be biased in the forward-active operation region. Checks in the simulator can warn if a BJT leaves the forward-active region and enters the saturation region.

The bias point is set by the mirror current of the current source (cf. Chap. 4.3.1). The mirror ratio should ensure a current density where the maximum transit frequency of the BJT is achieved. The minimum (maximum) current of a BJT is limited by the minimum (maximum) emitter area which is given by the technology. In this work, the minimum (and the reference) current I_{ref} is chosen to be 1 mA. With (4.10), that results in a BJT transconductance of 33 mS at the junction temperature of 350 K.

LC-filters convert a current input signal into a voltage output signal and vice versa. The subsequent stage should not disturb the signal in the filter. An emitter follower is a voltage buffer and offers the desired separation.

4.3 Basic Building Blocks

4.3.1 Current mirror

Tail current sources in differential circuits set the bias current for the signal transistors independently of supply voltage and temperature. A reference current is generated on-chip or off-chip and is fed into a bias voltage generator. The bias voltage V_{bi} is distributed to the tail current sources where it is transformed into a current again.

The most simple BJT current source is depicted in Fig. 4.9a. It consists of only two BJTs—the reference transistor and the mirror transistor. The collector and the base of the reference transistor are connected together, so the transistor reduces to its base-emitter diode. The input current I_0 is fed into that diode and will generate the junction voltage

V_{BE0}. The bases of the reference transistor and the mirror transistor are connected together, so the base-emitter voltages V_{BE0} and V_{BE1} of both transistors are equal. With (4.5) that equivalence also holds for the current ratios between their collector currents I_0, I_1 and their saturation currents I_{S0}, I_{S1}:

$$V_{\mathrm{BE0}} = V_T \ln \frac{I_0}{I_{S0}} = V_{\mathrm{BE1}} = V_T \ln \frac{I_1}{I_{S1}}. \tag{4.19}$$

Using (4.2), the mirror current can be sized with the help of the emitter area ratio between mirror and reference transistor:

$$I_1 = I_0 \frac{I_{S1}}{I_{S0}} = I_0 \frac{A_{E1}}{A_{E0}}. \tag{4.20}$$

This equation lacks the dependency on the collector-emitter voltage of the current source. In the forward-active region, the mirror current will grow linearly with the collector-emitter voltage. The slope is equal to the output resistance r_0 and is already calculated in (4.12).

A current mirror with emitter degeneration (cf. Fig. 4.9b) improves the output resistance and mitigates the dependency on process, voltage and temperature (PVT) variations. The BJTs in the current mirror are used in common-emitter topology. A bias generator can supply many mirror current sources that are distributed on the chip. Process mismatch, the supply voltage and the temperature depend on the position on the chip. Conditions at the mirror current source can deviate significantly from the conditions at the bias generator and change the nominal collector current I_1 to $\hat{I}_1$:

$$\begin{aligned} I_1 &= I_{S1} e^{\frac{V_{\mathrm{BE1}}}{V_T}}, \\ \hat{I}_1 &= a I_1 = b I_{S1} e^{\frac{V_{\mathrm{BE1}} - c}{(1+d) V_T}}. \end{aligned} \tag{4.21}$$

a, b, c and d represent the deviations from the desired values. As proposed in (cf. Chap. 4.2.1), an emitter degeneration resistor introduces negative feedback and reduces the deviation from the design current. With the resistors in Fig. 4.9b, (4.19) transforms into an implicit equation for the mirror current $\hat{I}_1 = a I_1$:

$$V_T \ln \frac{I_0}{I_{S0}} + I_0 R_0 = V_{\mathrm{bi}} = c + (1+d)\, V_T \ln \frac{a I_1}{b I_{S1}} + \hat{I}_1 R_1. \tag{4.22}$$

With (4.20) the mirror current $\hat{I}_1$ can be estimated by

$$\begin{aligned} \hat{I}_1 &= \frac{R_0}{R_1} I_0 - \frac{1}{R_1} \left(c + (1+d)\, V_T \ln \frac{a}{b} + d V_T \ln \frac{I_0}{I_{S0}} \right) \\ \hat{I}_1 &= I_1 - \Delta I \approx \frac{R_0}{R_1} I_0. \end{aligned} \tag{4.23}$$

For distant current mirror sources, the supply voltage deviation c makes up for the largest error. The nominal feedback voltage $V_f = I_0 R_0 = I_1 R_1$ is the same for the reference

circuit and for all connected mirror current sources. The larger it is, the smaller is the relative deviation from the design current. The percentage of the deviation is given by

$$\frac{\Delta I}{I_1} = \frac{c/R_1}{V_f}. \tag{4.24}$$

A further advantage of the emitter degeneration is the higher output resistance. For a sufficiently large current gain β, the output resistance R_0 of the current mirror becomes [47]

$$R_0 \approx r_{0,1}\left(1 + g_{m,1}R_1\right), \tag{4.25}$$

where $r_{0,1}$ and $g_{m,1}$ are the output resistance and the transconductance of the mirror BJT, respectively.

The base currents of all current mirror sources draw current from the reference current and thus reduce the effective reference current. The case without emitter degeneration is analyzed here: If the BJT of the bias generator and the BJTs of the n mirror current sources are identical, the output current reduces to

$$I_1 = \frac{I_0}{1 + \frac{n+1}{\beta}}. \tag{4.26}$$

The deviation from the design current depends on β and on the number n of connected current mirror sources. The deviation becomes especially undesirable if this number changes during operation. A remedy is the beta helper circuit: The connection between collector and base of the reference circuit is replaced by an emitter follower. The emitter follower acts as voltage buffer with high current gain. It controls the bias voltage to that point where the reference BJT conducts the reference current. The beta helper improves the deviation from the design current to [47]:

$$I_1 = \frac{I_0}{1 + \frac{n+1}{\beta(\beta+1)}}. \tag{4.27}$$

Fig. 4.9c shows the beta helper with emitter degeneration resistors. This circuit is used to set the bias for all circuits in the signal path.

Distribution of DC signals across the chip is the same challenge as the distribution of the bias voltage for the current sources. The supply voltage deviation and coupling noise from aggressor nets can disturb a voltage signal. Fig. 4.9d shows a popular way to circumvent these problems [47]: an npn current mirror converts a positive reference current into a negative current. This current is routed on the chip to the destination circuit. There, a pnp current mirror converts it back into a positive current. Current routing has two advantages over voltage routing: first, only local current mirrors are used, so mismatch and temperature variations between mirror pairs are minimized. Secondly, in contrast to a single-ended voltage signal, the current signal does not suffer from noise on a reference node.

4.3.2 Emitter follower with tail current source

The emitter follower in Fig. 4.10 is a single-ended circuit and uses a BJT in common-collector topology (cf. Chap. 4.2.1). It can be used as a voltage buffer to separate a driver with high output resistance from the load. In conjunction with differential amplifiers it can increase the bandwidth significantly [58]. In this work, it separates the LC-filter from the subsequent circuit. A current source replaces the emitter resistor. The current source has two advantages: first, it allows to bias the signal transistor at the current density with the highest transit frequency. And secondly with (4.25), it offers a higher output resistance in comparison to a simple resistor.

The voltage gain of an emitter follower has a very high bandwidth [47] with both—a zero and a pole—only slightly below the transit frequency. If carefully designed [59], [60], the voltage gain behaves like an RLC circuit and peaks at $\omega_0 = \sqrt{\frac{\omega_T}{R_B C_L}}$.

4.3.3 Differential pair

The differential pair in Fig. 4.11a is a basic TCA and the basis for the differential amplifier (DA). It converts a differential input voltage into a differential output current. For the calculation of the output current, the input voltage v_{in} is distributed equally onto the base-emitter voltages of the differential pair:

$$\begin{aligned} V_{\text{BE,p}} &= V_{\text{X}} + \frac{v_{\text{in}}}{2}, \\ V_{\text{BE,m}} &= V_{\text{X}} - \frac{v_{\text{in}}}{2}. \end{aligned} \tag{4.28}$$

where V_{X} denotes the average voltage of the inputs relative to the collector node of the tail current source. The single-ended output currents follow directly from (4.5)

$$\begin{aligned} i_p &= I_S e^{\frac{V_{\text{BE,p}}}{V_T}}, \\ i_m &= I_S e^{\frac{V_{\text{BE,m}}}{V_T}}. \end{aligned} \tag{4.29}$$

With the trigonometric equivalence

$$\tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}}, \tag{4.30}$$

and the definition of the total current I_0 and the differential current Δi

$$\begin{aligned} I_0 &= i_p + i_m, \\ \Delta i &= i_p - i_m \end{aligned} \tag{4.31}$$

the differential output current and the transconductance can be derived:

$$\Delta i(v_{\text{in}}) = I_0 \tanh\left(\frac{v_{\text{in}}}{2V_T}\right), \tag{4.32}$$

$$g_m(v_{\text{in}}) = \frac{\mathrm{d}\Delta i}{\mathrm{d}v_{\text{in}}} = \frac{I_0}{2V_T}\operatorname{sech}^2\left(\frac{v_{\text{in}}}{2V_T}\right). \tag{4.33}$$

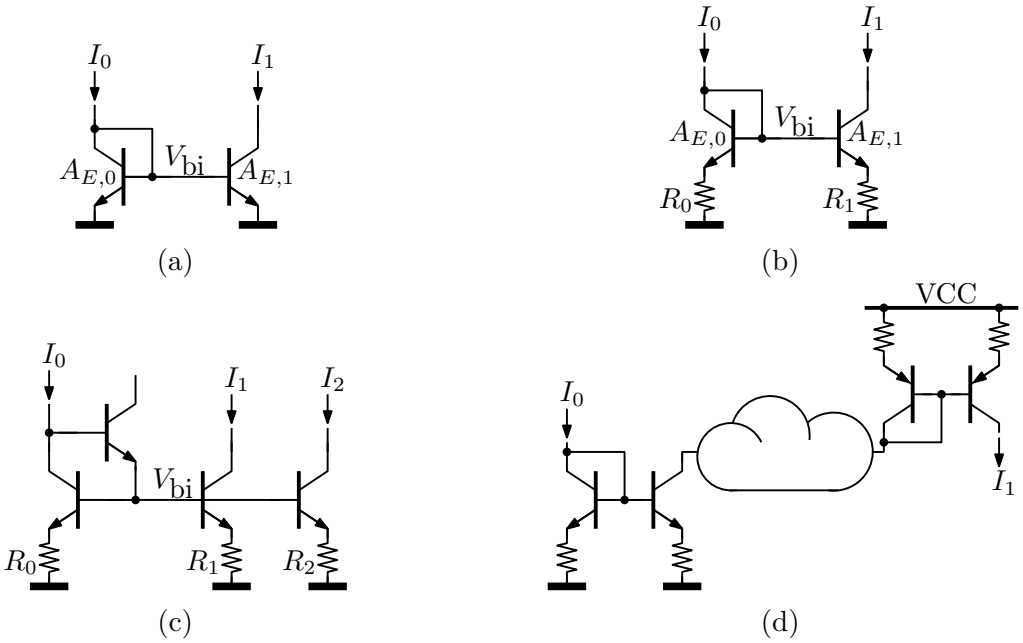


Figure 4.9: (a) Simple BJT current mirror, (b) current mirror with emitter degeneration, (c) current mirror with emitter degeneration and beta helper, (d) analog signal distribution across the chip with currents.

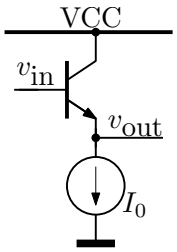


Figure 4.10: Emitter follower.

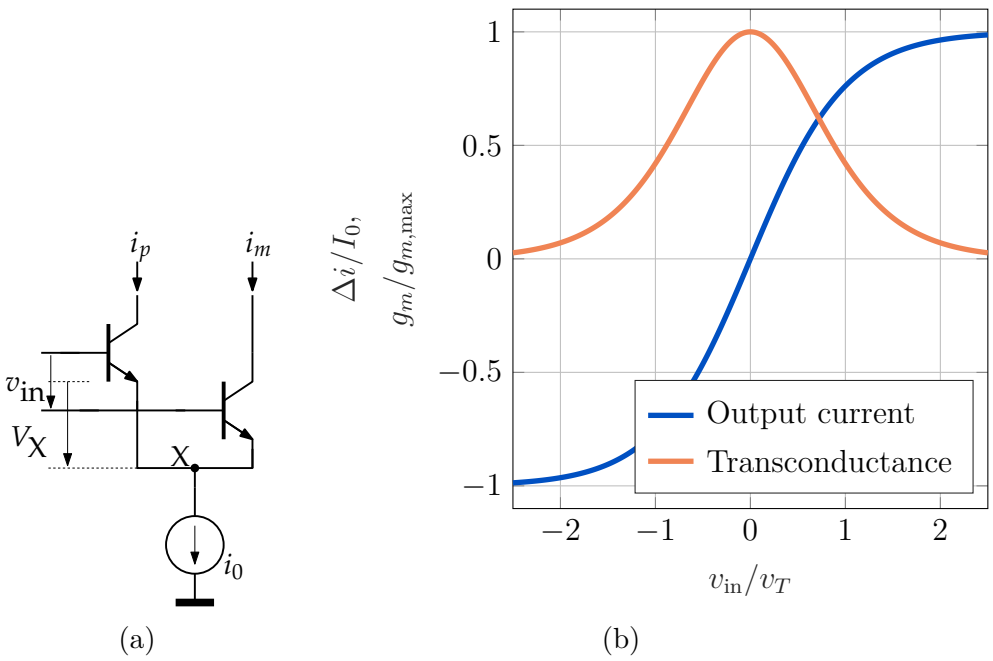


Figure 4.11: (a) Differential pair with current source and (b) differential output current Δi and transconductance g_m vs. the input voltage.

The transconductance is proportional to the bias current I_0, so it can be tuned during operation. In the vicinity of $v_{\text{in}} = 0$, the differential transconductance can be linearized to

$$g_m(v_{\text{in}})\big|_{v_{\text{in}}=0} \approx \frac{I_0}{2V_T}. \tag{4.34}$$

Compared to the transconductance of a single BJT (4.10), this is only half as large. This is reasonable because the tail current I_0 distributes equally onto both BJTs in the differential pair, so that each of the BJTs sees a collector current of $I_C = \frac{I_0}{2}$.

The approximation of the differential transconductance is only valid within a small input voltage range. At an input voltage of $v_{\text{in}} = \pm V_T$, the transconductance already reduces to 89% of the maximum value.

4.3.4 Differential amplifier with resistor load

The DA consists of a differential pair with load resistors R_L (cf. Fig. 4.12a). The resistors convert the output current to a voltage. The main design goals for the DA are high bandwidth and a sufficiently large voltage gain. If the DA is used as a digital circuit, it is also called CML-amplifier.

The small-signal voltage gain of the DA is the product of the small-signal transconductance and the load resistor R_L. The transconductance is already derived in (4.34) and depends on the tail current and the thermal voltage of the BJT. The junction temperature during operation is assumed to be 50 K above room temperature yielding a thermal voltage

of $V_T = 30\,\mathrm{mV}$. For the standard differential amplifier DA1, a load resistor $R_L = 300\,\Omega$ and a tail current of 1 mA is chosen. Later on, the versions DA2 and DA4 appear. These DAs have scaled tail currents of 2 mA and of 4 mA.

For DA1, the ideal differential voltage gain A_V becomes

$$A_V = g_m R_L = 5.0. \tag{4.35}$$

In a bipolar technology, BJTs show a parasitic resistance R_E in the range of several Ω in series with the emitter. In Fig. 4.4b the resulting negative feedback is intentional. In the DA, the negative feedback limits the transconductance to

$$\hat{g}_m = \frac{g_m}{1 + g_m R_E}. \tag{4.36}$$

With the parasitic resistance taken into account, the voltage gain is reduced to $\hat{A}_V = 4.29$. A DC simulation of a differential pair with the given properties yields a voltage gain of $A_{\mathrm{V,sim}} = 3.45$. The difference between the calculation and the simulation can be attributed to the high current effects.

The high-frequency analysis of the differential amplifier requires more calculation. The transit frequency of the differential pair with zero voltage gain is derived in (4.18). The relatively high voltage gain leads to an increased Miller capacitance and to a lower bandwidth. Fig. 4.12b shows the schematic of the differential amplifier with all parasitics. For the small-signal analysis the circuit reduces to its equivalent half-circuit (cf. Fig. 4.13). The base resistance R_B is absorbed into the source resistance R_s of the driving stage. R_L is the load resistance and C_L is the parasitic capacitance of the load resistor.

The transfer function is treated in full detail in the literature [31], [61]. The bandwidth

$$\omega_{3\mathrm{dB}} = \frac{1}{\tau_1 + \tau_2 |A_V|} \tag{4.37}$$

can be attributed to two time constants τ_1 and τ_2

$$\begin{aligned} \tau_1 &= (R_s \| r_\pi)\,(C_{\mathrm{BE}} + C_{\mathrm{CB}})\,, \\ \tau_2 &= R_s C_{\mathrm{CB}} + \frac{1}{g_m}\,(C_{\mathrm{CB}} + C_L)\,. \end{aligned} \tag{4.38}$$

For high voltage gain $A_V \gg \frac{\tau_1}{\tau_2}$, the second time constant τ_2 becomes dominant and the gain bandwidth product (GBW)

$$\mathrm{GBW} = |A_V| \omega_{3\mathrm{dB}} \tag{4.39}$$

must be optimized:

$$\begin{aligned} \mathrm{GBW}^{-1} &= R_s |A_V| C_{\mathrm{CB}} + R_L\,(C_{\mathrm{CB}} + C_L) \\ &= \tau_4 \qquad\qquad\quad + \tau_5 \end{aligned} \tag{4.40}$$

τ_4 represents the time constant at the input which is affected the most from high voltage gain. τ_5 is the time constant at the output which is limited by the parasitic capacitance of the load resistor.

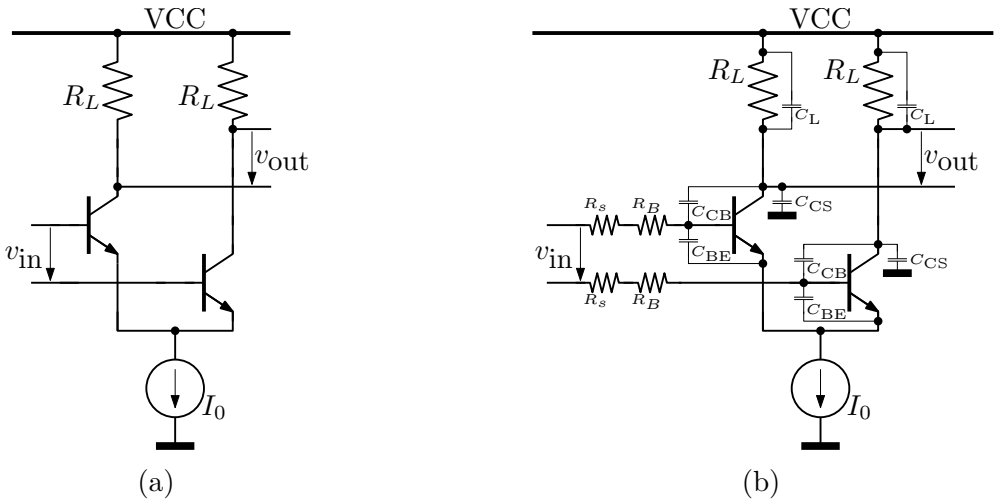


Figure 4.12: (a) Differential amplifier and (b) differential amplifier with parasitics.

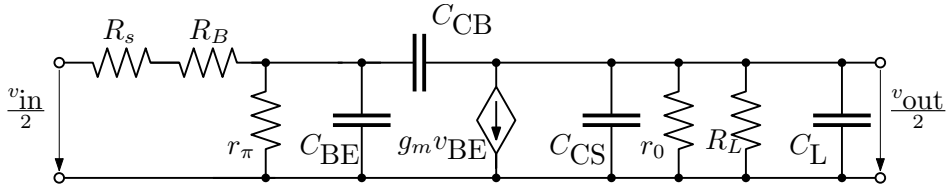


Figure 4.13: Equivalent half circuit of the differential amplifier.

The optimum design of an amplifier chain is derived in Ref. [8]. All DAs must have the same voltage gain and the same bandwidth. For maximum bandwidth, the voltage gain per stage in the chain is $A_V = \sqrt{e} = 1.65$. The voltage gain of 3.45 in this work is larger. It is a trade-off between noise immunity, power, layout constraints of the load resistor and predictability between simulation and experiment.

In a first order approximation, the system is invariant against geometry scaling. If the widths of all elements are stretched by a factor a, then the currents and the capacitors will scale likewise and the resistors will scale with the inverse:

$$\begin{aligned}
\hat{R}_L &= \frac{1}{a} R_L, \\
\hat{C}_L &= a C_L, \\
\hat{C}_{\text{CB}} &= a C_{\text{CB}}, \\
\hat{A}_V &= -\frac{a I_C}{V_T} \frac{1}{a} R_L = A_V, \\
\hat{\tau}_4 &= \tau_4, \\
\hat{\tau}_5 &= \tau_5.
\end{aligned} \tag{4.41}$$

Geometry scaling also means that the voltage drop

$$V_{\text{dig}} = R_L I_{\text{ref}} \tag{4.42}$$

at the load resistor R_L is fixed.

Table 4.1: Simulation results for differential amplifiers.

	DA1	DA2	DA4	DA1+EF1	cascDA1+EF1
Tail current [mA]	1.0	2.0	4.0	3.0	3.0
Load resistance [Ω]	300	150	75	300	300
DC voltage gain	3.5	3.3	3.3	4.6	4.6
Bandwidth [GHz]	14.5	18.0	18.0	27.8	36.4
Stage-to-stage delay [ps]	5.1	4.2	4.2	5.3	7.3

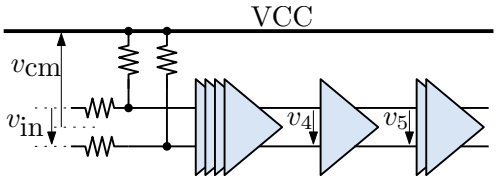


Figure 4.14: Test bench for a chain of differential amplifiers.

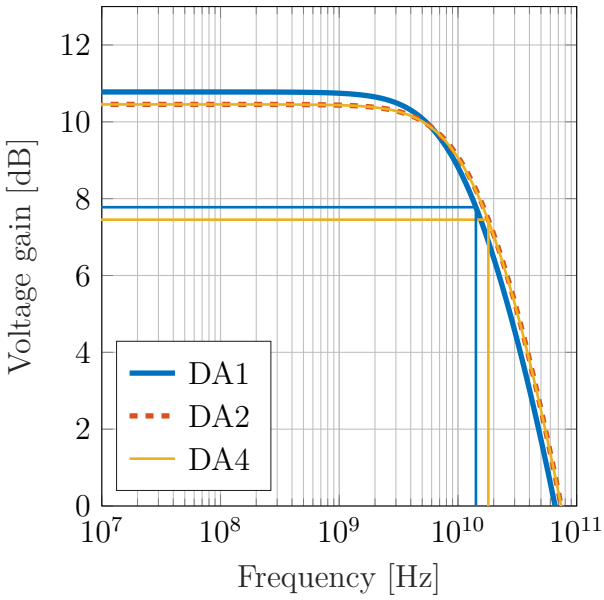
The design of the DAs is optimized by simulation. DAs with different tail currents (1 mA, 2 mA and 4 mA) are simulated on schematic level with an AC (cf. Fig. 4.15a) and a transient analysis (cf. Fig. 4.15b). For a realistic input and output behavior, an amplifier chain is simulated. Fig. 4.14 shows the test bench. The amplifier under test is surrounded by other amplifiers of the same type.

The DA2 and the DA4 are almost identical in their RF performance. The DA1 has a higher DC voltage gain but a slightly smaller bandwidth. The difference to the other DAs is the slightly different sizing of the differential pair. The BJTs of the other DAs are sized for the optimum current density (cf. Fig. 4.7). The BJTs of DA1 already have minimum size. The current density is lower which reduces the bandwidth. The gain is larger because the ratio between the collector current and the knee current is lower (cf. Fig. 4.3). The BJTs have less high-current effects and higher transconductance.

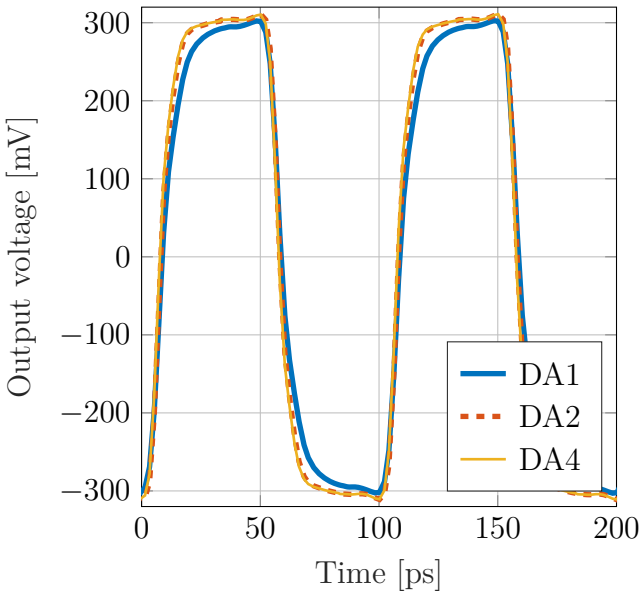
Tab. 4.1 summarizes the simulation results. The tables lists two additional amplifier types: first (DA1+EF1), a DA1 with an emitter follower at the output and secondly (cascDA1+EF1), a DA1 with cascode and an emitter follower at the output. An emitter follower consumes additional current but it can increase the bandwidth significantly [60].

4.3.5 Single-ended-to-differential converter

The perimeter of an integrated circuit limits the number of pads. While a differential signal requires two pads, a single-ended signal only needs one. The clock input, the signal input and the signal output are high-speed differential signals. The control currents are single-ended, but the digital control signals on the chip are differential. The control signals are written rarely and the speed requirements are low. That use case allows to replace the differential inputs by single-ended inputs. Fig. 4.16 shows the low-speed single-ended-to-differential converter for the interface. It is a modified version of the differential amplifier: the input signal drives one base. The complementary output signal drives the other base. The gain in the trip point is high. The delay until the output flips is reasonably slow so



(a)



(b)

Figure 4.15: Simulation results for the test bench in Fig. 4.14 for differential amplifiers with 1 mA (DA1), 2 mA (DA2) and 4 mA (DA4) tail current: (a) AC simulation results for the transfer function $\frac{v_5}{v_4}$ vs. the frequency with markers at the 3-dB bandwidth. (b) Transient simulation result for the output voltage v_4.

that bouncing is avoided.

4.3.6 Latch

Fig. 4.17 shows a CML-latch. It consists of two parts: a differential amplifier (Q_{1p} and Q_{1m}) and a cross-coupled amplifier (Q_{2p} and Q_{2m}). Both share the same load resistances R_L.

The latch operates in two phases. In the transparent phase the differential amplifier is active and delivers an amplified version of the input voltage to the output. The base-emitter capacitances of the cross-coupled amplifier track the output voltage.

In the hold phase the differential amplifier is switched off and the regenerative, cross-coupled amplifier is switched on. By positive feedback even small voltages are amplified until one of the BJTs (Q_{2p} and Q_{2m}) conducts the whole tail current.

Metastability of latches is a common concern in CT-BPDSM [39]. There, a latch is used as a regenerative decider. An ideal latch has three possible output values: positive, negative or—for zero input voltage—the *metastable* state. A real latch will always go into positive or negative direction due to thermal noise or coupling. But the delay until the output voltage is reached can become very large. An amplifier in front of the latch reduces the delay.

Fig. 4.18 shows the result of a transient simulation for a latch with and without preamplifier. The output of the latch is open, the input voltage is set to 1 mV. When the clock switches, both output voltages follow the collector voltage of the tail current source. The output voltages are slightly below the common-mode voltage, when the regenerative amplification starts.

The delay between the zero crossing of the differential clock voltage and the point where the latch output reaches 75 % of the differential voltage is determined for both latch types. The difference between these delays is 6 ps. The input voltage is small enough that small-signal approximation holds. The output voltage increases exponentially vs. the time. The time for an increase by a certain factor stays constant.

The transient simulation is repeated for different values of the input voltage. The simulated delays in Fig. 4.19 confirm the assumption about the constant delay. The delay remains below 100 ps for input voltages above 1 nV. The delay is smaller than the clock period and the input voltage is smaller than the typical voltage noise. That ensures that metastability will not degrade the BPDSM performance.

4.3.7 Return-to-zero latch

Fig. 4.20 shows an RZ-latch. The transparent phase is identical to the CML-latch. Instead of a hold phase, it has a return-to-zero phase, where the differential output voltage is zero.

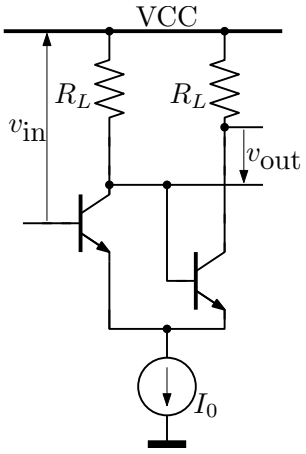


Figure 4.16: Single-ended-to-differential converter.

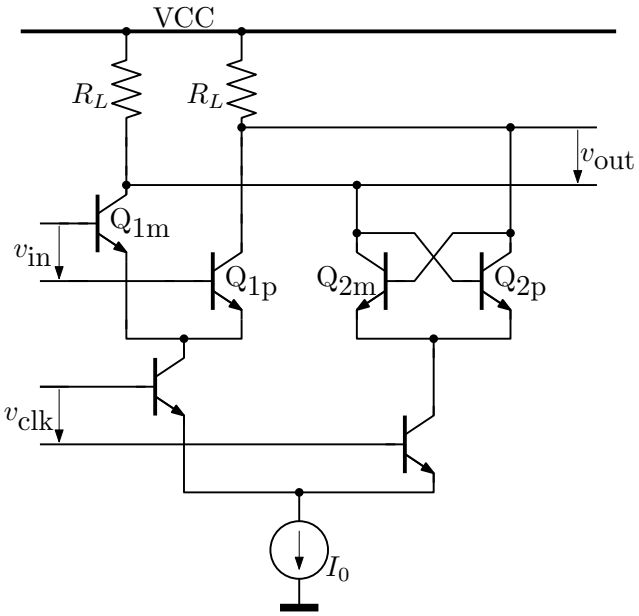
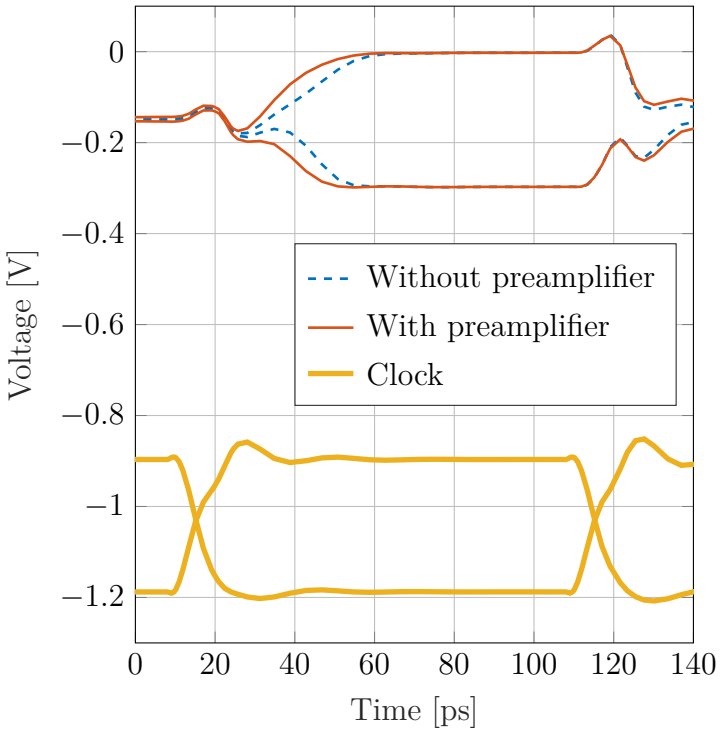
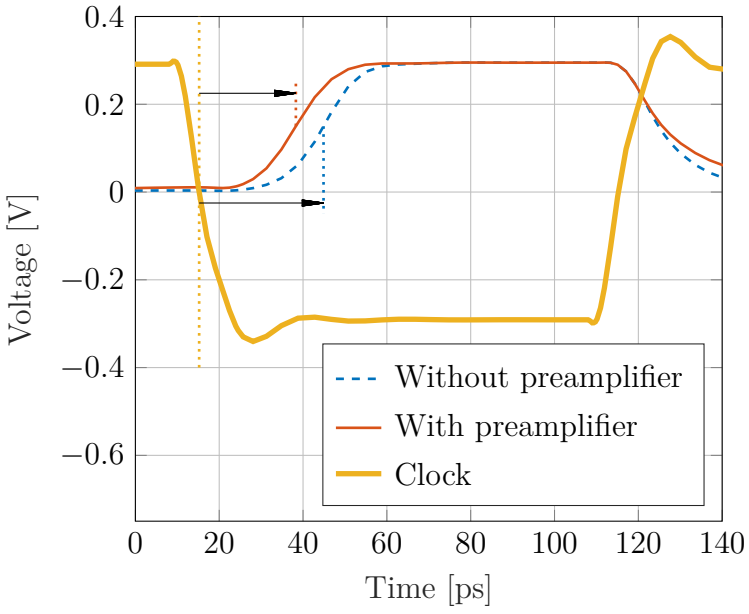


Figure 4.17: Latch.



(a)



(b)

Figure 4.18: Transient simulation results of a latch without and with a preamplifier with an input differential voltage of 1 mV: (a) single-ended voltages for latch outputs and for the clock at the latch inputs; (b) associated differential voltages and delays between 50% falling clock edge and 75% (corresponds to 150 mV) rising output edge.

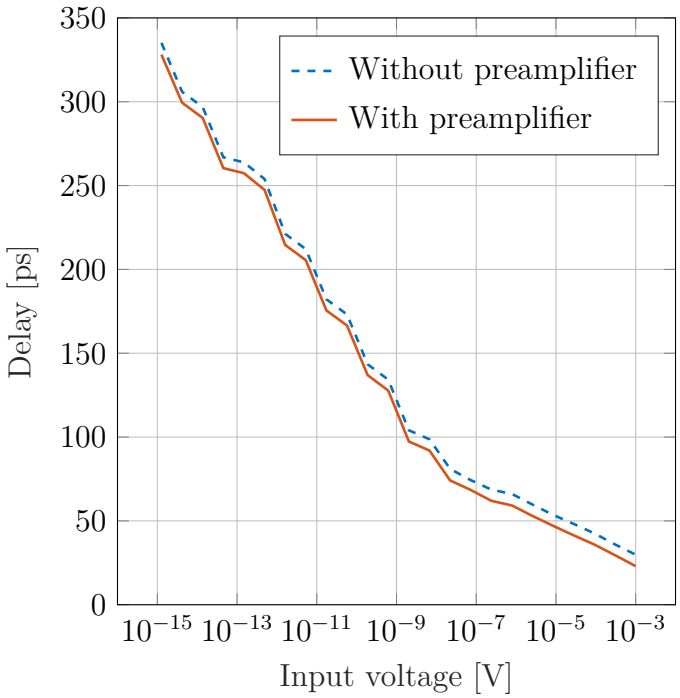


Figure 4.19: CML-latch delay vs. the input voltage.

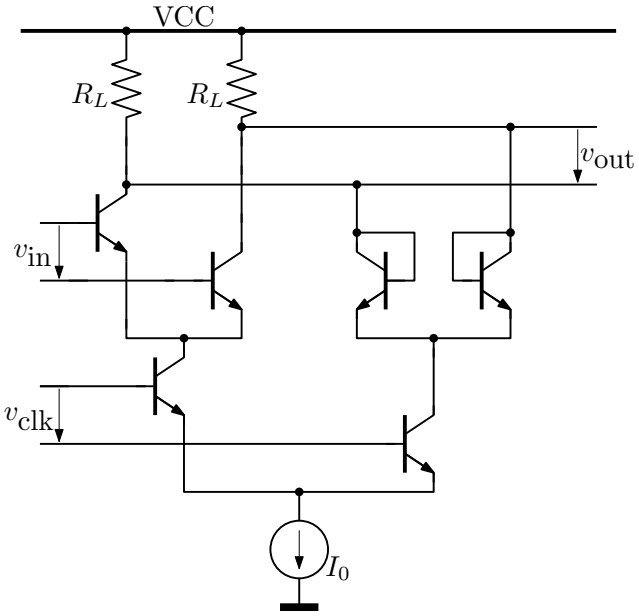


Figure 4.20: Return-to-zero (RZ) latch.

4.4 Transconductance Amplifier

An ideal TCA converts an input voltage into an output current. The input impedance is infinite and does not change the characteristic of the preceding stage. The output impedance is infinite as well. No matter what load resistor is connected, the output current will not change. The magnitude of the output current is a linear function of the input voltage.

For the design of a real TCA, a trade-off between non-linearity, bandwidth, noise, mismatch, tunability, area, supply current and supply voltage must be found. Most important for this work is linearity. Static and dynamic non-linearity can be distinguished. Dynamic non-linearity is caused by non-linear capacitances and time delays. The circuits in this work operate in the low GHz-range where static non-linearity is dominant. That allows for design optimization with DC simulations. For the analysis, dynamic non-linearities in the signal band must be taken into account as well. The combined non-linearity is estimated with periodic steady state (PSS) simulations.

This section starts with an ideal differential TCA. The straightforward implementation with a differential pair is already discussed in Chap. 4.3.3. The differential pair is the basis for all linearized TCAs. The most promising linearization techniques are presented. For the sake of brevity, the following TCAs implementations are excluded from the discussion:

- Caprio's cross-quad and its derivatives [62], [63] have an output path with an even number of base-emitter diodes connected in series. Half of the diodes have a positive, non-linear BJT transconductance. The non-linearity is cancelled by the other diodes which have negative, non-linear transconductance. The TCAs offer good linearity at medium input voltage range but require a large supply voltage.

- Quinn's cascode [64] uses a feed-forward error amplifier to cancel the non-linear BJT transconductance.

- Lim [65] proposes a variation of Quinn's cascode with a reduced input impedance.

4.4.1 Ideal differential transconductance amplifier

Fig. 4.21a shows an ideal differential TCA. The differential output current $\Delta i(v_{\text{in}}) = i_p - i_m = g_m v_{\text{in}}$ is a function of the differential input voltage v_{in} and the constant transconductance g_m. Like in (4.31), the tail current I_0 is the sum of the output currents. The single-ended output currents can not become negative, therefore I_0 is also the maximum differential output current $\Delta i_{\max}$. The input voltage must not exceed the corresponding maximum input voltage

$$v_{\text{in,max}} = \max\left[|v_{\text{in}}|\right] = \frac{\Delta i_{\max}}{g_m} = \frac{I_0}{g_m}. \tag{4.43}$$

For the ideal TCA, the output current saturates abruptly at the maximum input voltage (cf. Fig. 4.21b). For a real TCA, $v_{\text{in,max}}$ is an upper bound for the input voltage, but the TCA will become non-linear much earlier.

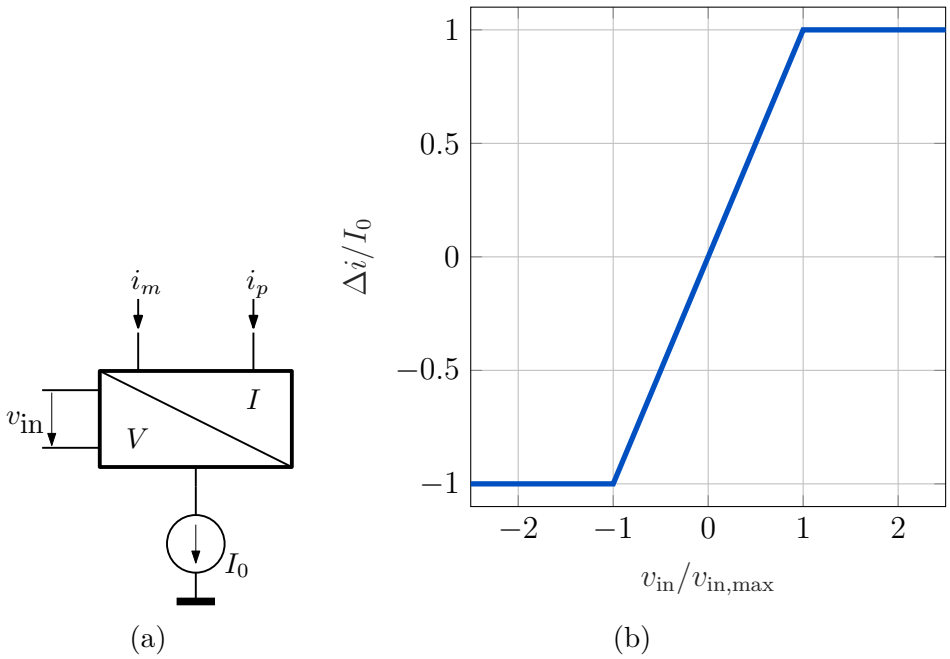


Figure 4.21: (a) Ideal TCA with current source. The tail current I_0 limits the maximum output current. (b) Output current Δi vs. the input voltage v_{in}.

4.4.2 Linearization by reduction of the input voltage

In Chap. 3.1.1 the basics for non-linear circuits are described. The power of the third-order non-linearity grows three times as fast as the fundamental. A straightforward way to increase the SDR is to attenuate the input power. Resistors are linear components and a resistive divider at the input can scale the input voltage of the TCA (cf. Fig. 4.22):

$$\hat{v}_{\text{in}} = \frac{R_1}{R_1 + R_2} v_{\text{in}}. \tag{4.44}$$

The overall transconductance remains the same if the tail current is scaled in the other direction:

$$\hat{I}_0 = \frac{R_1 + R_2}{R_1} I_0. \tag{4.45}$$

For 1 dB attenuation, 1 dB SNR will be lost, however the IMD3 will drop by 3 dB. In total, the SDR will increase by 2 dB. The attenuation of the signal also adds noise from the new circuit elements, so the increase in SNDR will be smaller.

If the whole signal path is under control of the designer, the voltage at each point in the circuit is a trade-off between non-linearity and noise. Attenuation should only be an option if the input voltage can not be changed easily. While this seems to be obvious here, this is not always the case—especially for multi-stage designs.

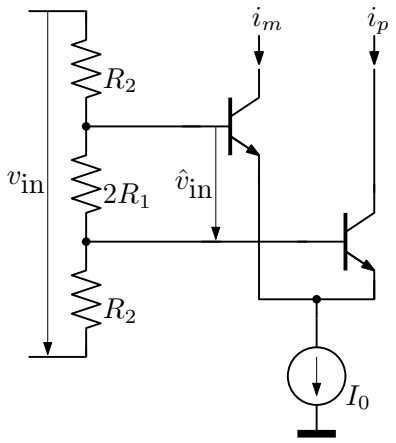


Figure 4.22: TCA with voltage divider at the input.

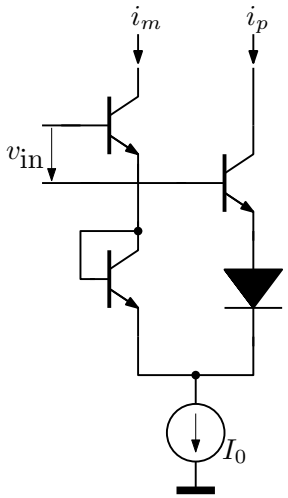


Figure 4.23: Differential pair with diode-degeneration.

4.4.3 Linearization by emitter degeneration with resistors and diodes

Attenuation scales the input voltage in front of the TCA. Emitter degeneration with diodes has a similar effect on the transfer characteristic in (4.33). The new output current

$$\Delta i(v_{\text{in}}) = I_0 \tanh\left(\frac{v_{\text{in}}}{2V_T\,(n+1)}\right) \tag{4.46}$$

depends on a scaled input voltage. The scaling factor $\frac{1}{n+1}$ is a discrete value determined by the number of diodes n. The transconductance is still continuously tunable with the tail current I_0.

Fig. 4.23 shows an implementation with one degeneration diode. In integrated circuits the base-emitter diode of a BJT is used.

Emitter degeneration with a resistor is a form of negative feedback (cf. Fig. 4.4b). The output current of the TCA can be expressed implicitly by

$$v_{\text{in}} = 2V_T \text{atanh}\left(\frac{\Delta i}{I_0}\right) + \Delta i R. \tag{4.47}$$

For a small ratio between the output current and the tail current, the arctangent can be neglected and the output current can be approximated with

$$v_{\text{in}} \approx \Delta i R \;\text{ for }\; \frac{\Delta i}{I_0} \ll 1. \tag{4.48}$$

In contrast to the degeneration with diodes, the tuning range becomes much smaller. For small $\frac{\Delta i}{I_0}$, the transconductance is almost constant and approaches the inverse of the degeneration resistor

$$g_m = \frac{1}{R}. \tag{4.49}$$

Two types of resistive degeneration can be distinguished: in Fig. 4.24a the feedback resistor is connected in series between the emitter and the tail current source. For zero input voltage, half of the tail current I_0 flows through each of the branches. The voltage drop across the resistors is $I_0 R$ and must be taken into account for the choice of the supply voltage. The current noise of the tail current source adds up to the tail current. If the degeneration resistor is large, its effect on the output current can be neglected.

In the TCA with shunt resistive degeneration (cf. Fig. 4.24b), the input transistors are connected directly to separate tail current sources. One feedback resistor connects both emitters. Only the differential output current flows through the resistor. That has two advantages: first, there is no additional voltage drop for the TCA. Secondly, the implemented resistor area can be made smaller because the rms current through the resistor is smaller.

Unlike the series degeneration, noise from the two separate current sources goes directly into the output current. In this work, the noise power of the TCA is 2.4 dB higher than that of the TCA with series degeneration. Mismatch of the current sources could cause other disadvantages.

4.4.4 Linearization by composition: the multi-tanh transconductance amplifier

For identical input transistors, the transconductance of a differential pair ressembles a narrow bell shape (cf. Fig. 4.11b) around $v_{\text{in}} = 0$. If the emitter area of the input transistors differ, the center of the bell shape will move by the offset voltage

$$V_{\text{os}} = V_T \ln A, \tag{4.50}$$

where A is the ratio of the emitter areas.

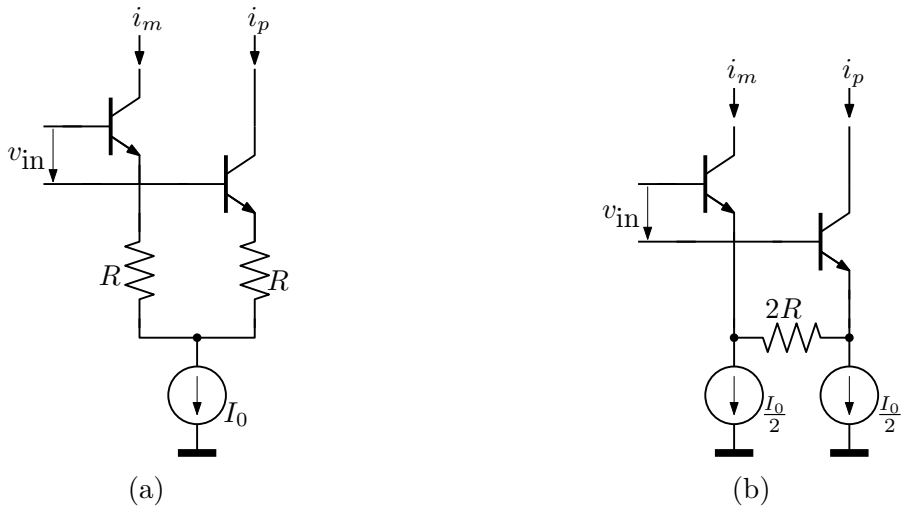


Figure 4.24: Differential pairs with resistive degeneration: (a) series emitter degeneration and (b) shunt emitter degeneration.

The input and the output impedance of an ideal TCA are infinite, therefore two TCAs can be connected in parallel without disturbing each other. The total transconductance is the sum of their separate transconductances.

These two properties are used in multi-tanh TCAs: several differential pairs with carefully designed offset voltages are connected together. Fig. 4.25a shows an implementation with two differential pairs—the multi-tanh doublet. The transconductance of the doublet is the sum of the single transconductances with the offset voltages $\pm V_{\text{os}}$:

$$g_m = \frac{I_0}{4V_T}\left(\operatorname{sech}^2\left(\frac{v_{\text{in}}+V_{\text{os}}}{2V_T}\right)+\operatorname{sech}^2\left(\frac{v_{\text{in}}-V_{\text{os}}}{2V_T}\right)\right). \tag{4.51}$$

Like the differential pair the transconductance is still tunable with the tail current I_0. The shape of the total transconductance depends on the offset voltage. The larger it is, the flatter becomes the total transconductance until two maxima form at $\pm V_{\text{os}}$. The optimum value of the offset voltage is just below that voltage and can be derived by minimizing the second derivative of the transconductance [66]. The corresponding value for the emitter ratio is $A = 3.73$. In comparison to the differential pair the input voltage range increases by $2V_{\text{os}}$. This amounts to $2.6V_T$ =78 mV at 350 K.

The large capacitive load of the multi-tanh circuit is its disadvantage. Compared to a conventional differential pair and for the same maximum transconductance, a single asymmetric differential pair has an emitter area which is $\frac{1+A}{2}$ larger. This ratio becomes worse for larger multi-tanh circuits: more stages mean larger offset voltages and larger emitter ratios.

4.4.5 Multi-tanh doublets with emitter degeneration

The degeneration with diodes works in a similar way than that for the differential pair (cf. Fig. 4.26a). The emitter area of the degeneration diode must match the emitter area

of the input transistor. The input voltage is split equally on both base-emitter diodes. That doubles the input voltage range to $2 \cdot 2.6 V_T = 156\,\mathrm{mV}$ at 350 K.

The transconductance remains tunable with the tail current. The large input voltage range and the tunability make this circuit a popular choice for a TCA [38], [67].

Emitter degeneration of the doublet with resistors is explored in Ref. [66]. The degeneration resistances are scaled with the inverse of the emitter area ratio of the input transistor. Small values of A increase the input voltage range only by a small extent. Large values of A lead to a high capacitive load and a wide spread of resistance values which is difficult to implement. A further disadvantage is the missing tunability.

4.4.6 Continuously tunable transconductance amplifier with large input voltage range

Fig. 4.27a shows an implementation of a continously tunable TCA with high linearity. Ref. [68] uses a similar circuit without input transistors for a variable-gain amplifier.

A common-collector circuit at the input provides high input impedance and separates the TCA from the preceding stage. The resistors R_{va} convert the input voltage into the differential current $i_{1\mathrm{a}}$. The translinear circuit [69] mirrors the current into a differential pair.

An alternative look on the circuit is this: The left side is a differential pair with **resistive degeneration** and **diode-degeneration**. Simulations verify that the output current can be approximated by

$$v_{\mathrm{in}} = i_{1\mathrm{a}} \mathbf{R_{va}} + \mathbf{2} \cdot 2 V_T \operatorname{atanh}\left(\frac{i_{1\mathrm{a}}}{I_{1\mathrm{a}}}\right). \tag{4.52}$$

Contrary to intuition, the application of both degeneration techniques at the same time mitigates the linearization effect. At low input voltages, the majority of the input voltage drop appears across the resistors. At high input voltages, the base-emitter diodes absorb more voltage. The additional diode moves the equilibrium to lower input voltages. The linearization comes from the resistive degeneration, therefore slightly higher non-linearity in comparison to a conventional resistive degeneration is expected.

Normally, the output current of the degenerated differential pair is the current through the collectors of the input transistors. Here, this current is absorbed by VCC. The same current flows through the degeneration diodes. The diodes convert the current to the voltage

$$v_{1\mathrm{a}} = 2 V_T \operatorname{atanh}\left(\frac{i_{1\mathrm{a}}}{I_{1\mathrm{a}}}\right) \tag{4.53}$$

and the differential pair on the right converts the voltage back to a differential current

$$i_{2\mathrm{a}} = I_{2\mathrm{a}} \tanh\left(\frac{v_{1\mathrm{a}}}{2 V_T}\right). \tag{4.54}$$

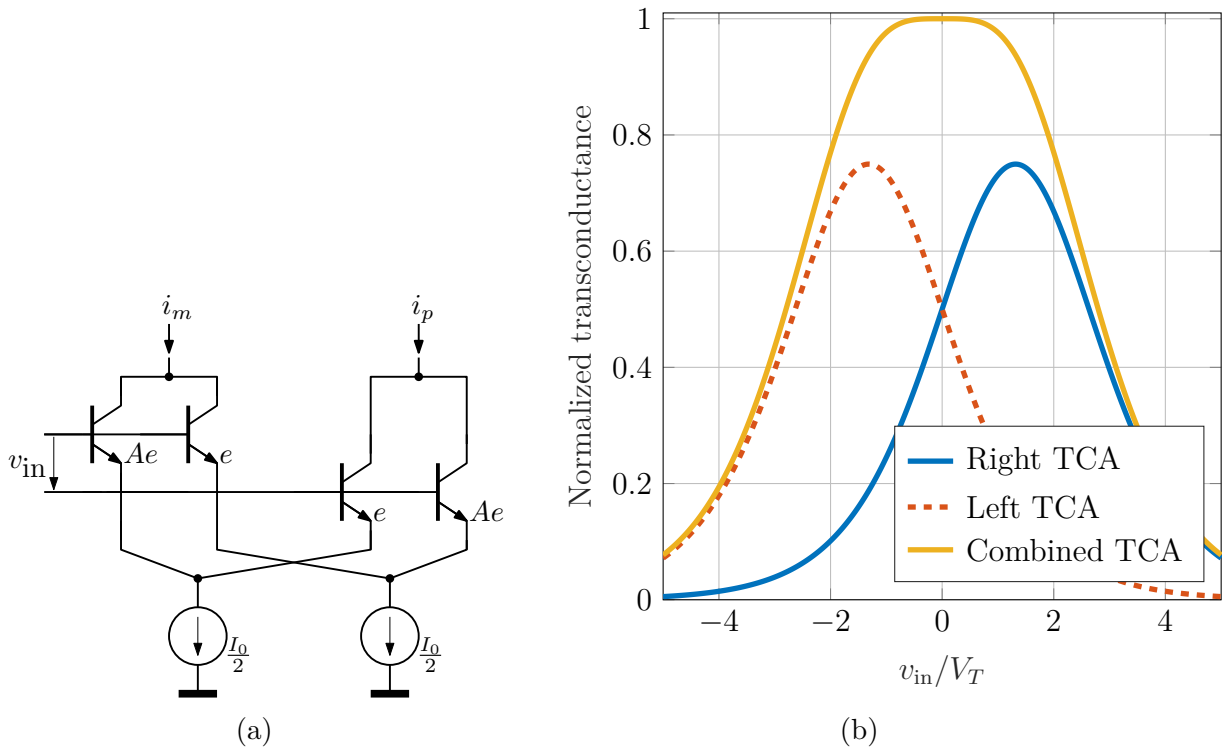


Figure 4.25: Multi-tanh doublet (a) schematic and (b) simulated transconductance vs. the input voltage for an emitter ratio of $A = 3.73$.

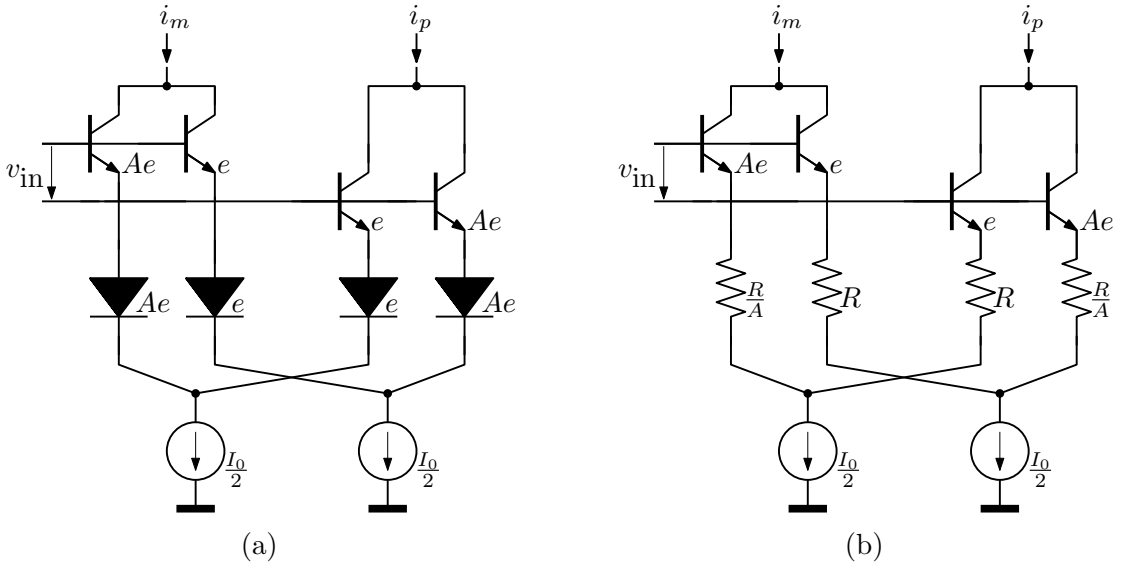


Figure 4.26: Hybrids of the multi-tanh doublet and emitter degeneration: (a) a doublet with diode-degeneration and (b) a doublet with resistive degeneration.

Combining (4.53) and (4.54) shows that the intermediate current i_{1a} is amplified by the ratio of the tail currents:

$$i_{2a} = \frac{I_{2a}}{I_{1a}} i_{1a}. \tag{4.55}$$

The total output current i_{2a} depends on the input voltage, the transconductance of the TCA on the left and the tail current ratio. The linearity is similar to that of a resistively degenerated differential pair, but in addition the new TCA is tunable!

4.4.7 Continuously tunable transconductance amplifier with feedforward linearization

The structure of the two-stage TCA opens up an interesting opportunity: the differential pair in Fig. 4.27a mirrors the current i_{1a} *linearly* to the output. In Fig. 4.27b the output differential pair is *resistively degenerated* with R_d. Here, the output current is

$$v_{1b} = 2V_T \text{atanh}\left(\frac{i_{2b}}{I_{2b}}\right) + i_{2b} R_d. \tag{4.56}$$

Similar to (4.48), the current depends linearly on the voltage v_{1b} for a small ratio $\frac{i_{2b}}{I_{2b}}$. The voltage-current $v_{1b}(i_{1b})$ relationship in the left part of the circuit is derived in (4.53). The output current implements an atanh function with respect to i_{1b}:

$$i_{2b} = \frac{v_{1b}}{R_d} = \frac{2V_T}{R_d} \text{atanh}\left(\frac{i_{1b}}{I_{1b}}\right). \tag{4.57}$$

Again—for a small ratio of $\frac{i_{1b}}{I_{1b}}$, the TCA on the left has a linear relationship between v_{in} and its output current i_{1b}:

$$i_{1b} = \frac{v_{in}}{R_{vb}}. \tag{4.58}$$

The transconductance from input to output is determined by

$$i_{2b} = \frac{2V_T}{R_d} \text{atanh}\left(\frac{v_{in}}{I_{1b} R_{vb}}\right). \tag{4.59}$$

The approximations only hold for ideal BJTs and if both TCAs in Fig. 4.27b operate in the linear region, that means for small ratios of $\frac{i_{1b}}{I_{1b}}$ and $\frac{i_{2b}}{I_{2b}}$. A rigorous theoretical analysis must include the knee current and parasitic emitter resistances of the BJTs. That is cumbersome and provides little design insight. Instead, the relationship between input voltage and output current is determined with DC simulations (cf. Fig. 4.28). The simulation results confirm the assumptions of the derivations qualitatively.

Fig. 4.29 shows the block diagram of the feedforward linearization with a combination of the two TCAs in Fig. 4.27. The negative curvature of the transconductance of the main TCA in Fig. 4.27a is cancelled by the positive curvature of the error correcting TCA in Fig. 4.27b. The search for the "best" tail currents becomes a software task:

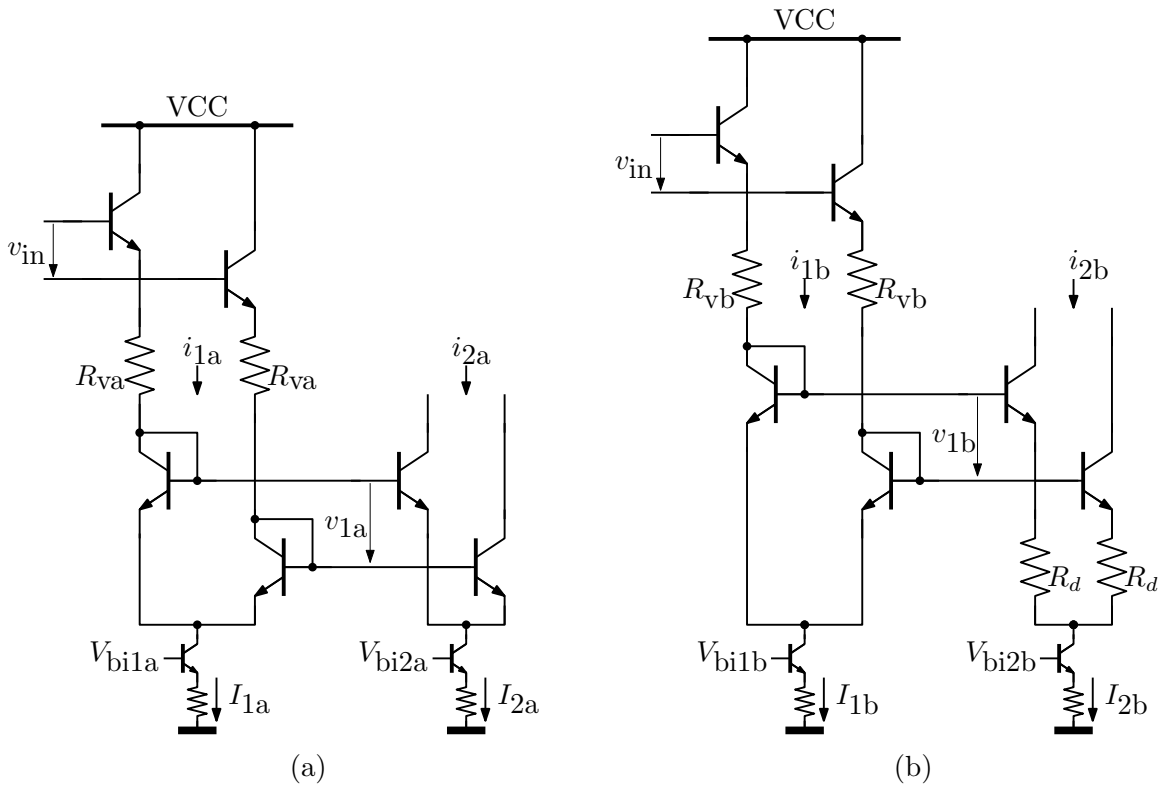


Figure 4.27: Continuously tunable TCA (a) without and (b) with resistive degeneration of the output differential pair.

Table 4.2: Comparison of different TCAs. The SDR3 is simulated with a two-tone test. Both input voltage amplitudes are 100 mV.

	Trans-conductance [mS]	Current consumption [mA]	SDR3 @100 mV [dB]	Tunable?
Differential pair	3.99	0.6	16	yes
Multi-tanh doublet	3.97	1.0	19	yes
Doublet with D-degeneration	3.99	2.6	57	yes
Doublet with R-degeneration	3.93	2.2	53	no
Diff. pair with R-degeneration	3.95	8.0	77	no
Feed forward linearized TCA	4.37	11.5	89	yes

For both circuits, the transconductance vs. the input voltage is simulated separately for a two-dimensional grid of tail currents. For each point in the grid, a polynomial which fits the transconductance is found. If the grid is defined sufficiently dense, the transconductance polynomial of arbitrary current pairs can be interpolated. The inverse holds as well: the current pair for a third-order—or any other order—polynomial coefficient can be interpolated. For each of the current pairs of the main TCA, the current pair of the error correcting TCA that minimizes non-linearity is determined.

The SNR of the TCA degrades due to the small ratios between the intermediate voltages v_{1a} and v_{1b} and the input voltage. The translinear loop between the input pair and the output pair is expected to show non-linear noise behavior [70].

4.4.8 Comparison of the transconductance amplifiers

The presented TCAs are implemented with a design transconductance of 4 mS. PSS-simulations on transistor-level determine the SDR3s vs. an input voltage between 10 mV and 200 mV. Fig. 4.30 and Tab. 4.2 show the simulation results.

For an input voltage amplitude of 100 mV the multi-tanh doublet with resistive degeneration and the multi-tanh doublet with diode degeneration yield acceptable results with an SDR3 of more than 53 dB. The feed-forward linearized TCA is tunable and has an excellent SDR3 of 89 dB but only a small SNR. The differential pair with series, resistive emitter degeneration offers the best trade-off between SDR3 and noise. Its transconductance can be made programmable with the techniques in Chap. 5.4.

4.5 Switchable Capacitance

The resonance frequency of an LC-circuit is

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{4.60}$$

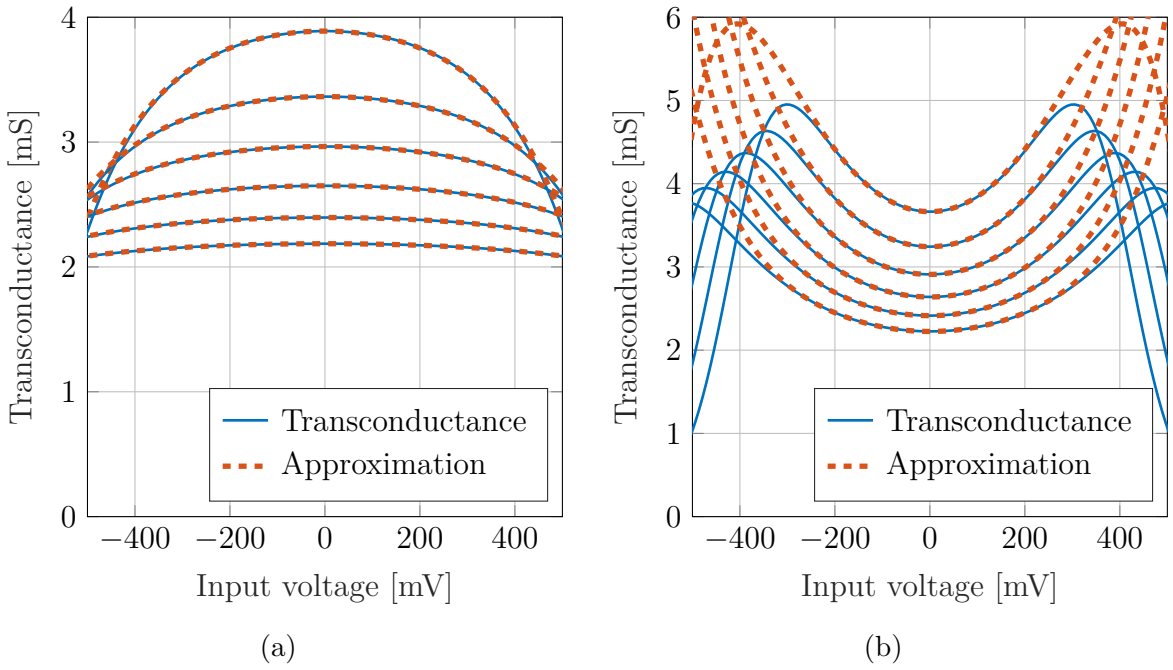


Figure 4.28: Simulated DC transconductance vs. the input voltage of the two-stage TCA (a) without (cf. Fig. 4.27a) and (b) with (cf. Fig. 4.27b) resistive degeneration of the output differential pair. Approximation denotes a fitted polynomial of the 4^{th}-degree. The resistances in Fig. 4.27 have the following values: $R_{\text{va}} = R_{\text{vb}} = 800\Omega$; $R_{\text{d}} = 20\Omega$.

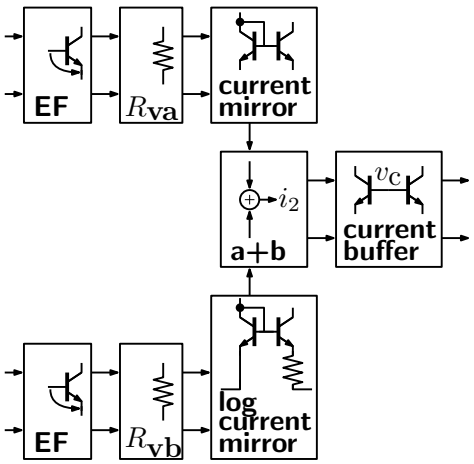


Figure 4.29: Feedforward linearized TCA consisting of the two-stage TCAs in Fig. 4.27. A common-base stage at the output can increase the output impedance.

A configurable resonance frequency requires a change in the inductance or in the capacitance. In integrated circuits, it is difficult to change the inductance. Analog bipolar technologies offer varactors. These have a junction capacitance with a strong dependency on the reverse bias voltage. The ratio between maximum capacitance and minimum capacitance is about two which translates into a maximum frequency ratio of $\frac{f_{\text{large}}}{f_{\text{small}}} = \sqrt{2}$.

In this work, switchable capacitances allow for higher frequency ratios. A MOSFET in a CMOS technology is a good voltage switch. A capacitance at the drain of a MOSFET can be connected to a signal at the transistor source with a high gate-source voltage. It is disconnected with a low gate-source voltage.

The technology in this work does not offer MOSFETs. A switchable capacitance in a bipolar technology is more involved because low on-resistance always means high bias current. Fig. 4.31 shows the implementation of a differential swichable capacitance with BJTs and the equivalent circuit. The circuit is similar to switched emitter followers in Ref. [2] (in the referenced paper the input voltage source is switched on and off, not the capacitance). The capacitance is symmetrical: emitter followers generate replica voltages of the signal voltages. Capacitances connect each signal node to the respective complementary replica node.

The capacitance is switched on if the current sources of the emitter followers are active. The Q-factor of the capacitance depends on the small-signal resistance through the BJT. It is determined by the transconductance

$$g_m = \frac{I_C}{V_T}. \tag{4.61}$$

The total differential admittance is

$$Y = \frac{2g_m sC}{g_m + sC}. \tag{4.62}$$

If the current sources of the emitter followers are switched off, the BJT transconductance becomes zero and the replica nodes become floating nodes. The differential admittance is zero and so is the effective differential capacitance.

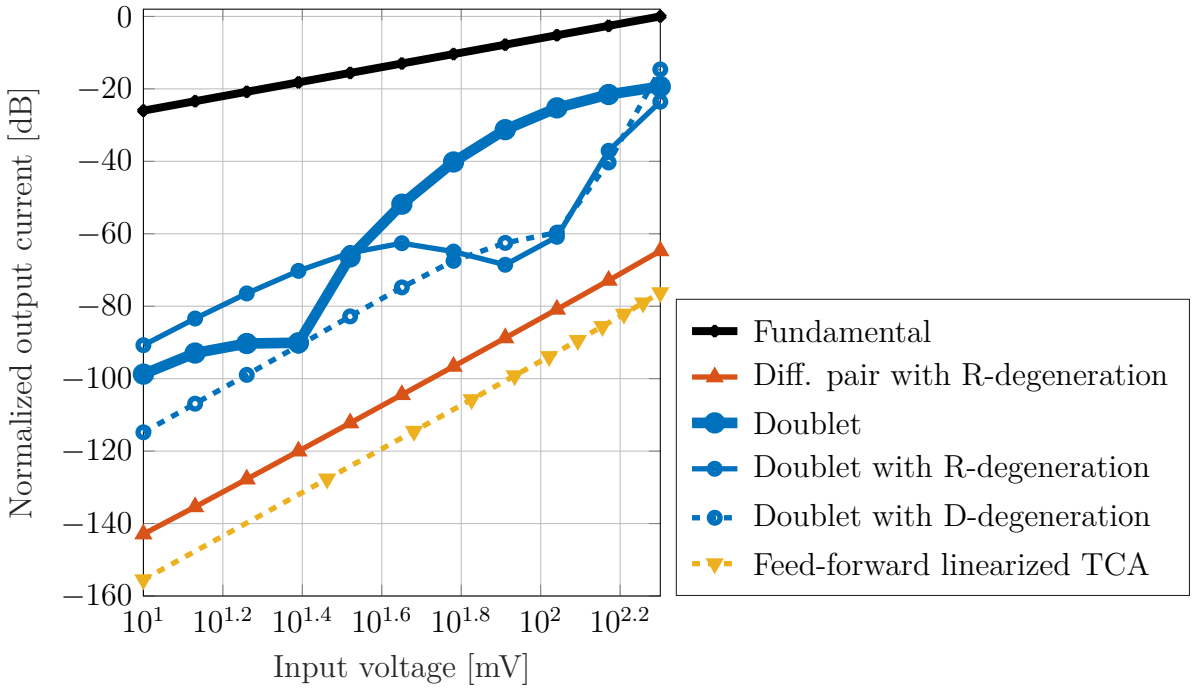


Figure 4.30: Power of the fundamental and the third-order intermodulation products (IMD3s) vs. the input voltage of one tone for different TCAs. R-degeneration denotes resistive degeneration, D-degeneration denotes degeneration with diodes.

4.6 Loop Filter

4.6.1 Resonance frequency

Fig. 4.32a shows the loop filter. It consists of an inductor, a capacitor and a Q-enhancement TCA. The integrated inductor in this work is provided by Infineon and has a Q-factor between 13 and 20. Its series resistance R_s can not be neglected. In a narrow frequency band around the resonance frequency, the series resistance can be converted into a parallel resistance: Fig. 4.32b shows the equivalent circuit. The Q-TCA acts as a negative resistance $-R_p$ and cancels the equivalent parallel resistance of the inductor. The input admittance of the resonator must become zero

$$\begin{aligned} Y_{\mathrm{LC}}(\omega_0) &= Y_C + Y_L + R_p - R_p \\ &= \omega_0 C - \frac{1}{\omega_0 L} \stackrel{!}{=} 0 \end{aligned} \tag{4.63}$$

at the resonance frequency

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{4.64}$$

4.6.2 Q-enhancement transconductance amplifier

For the computation of the transconductance $G_q = -\frac{1}{R_p}$ the circuit values in Fig. 4.32b must be derived at the resonance frequency [8]. The Q-factor of the inductor relates the series inductance L_s to the parasitic resistance

$$Q = \frac{\omega_0 L_s}{R_s}. \tag{4.65}$$

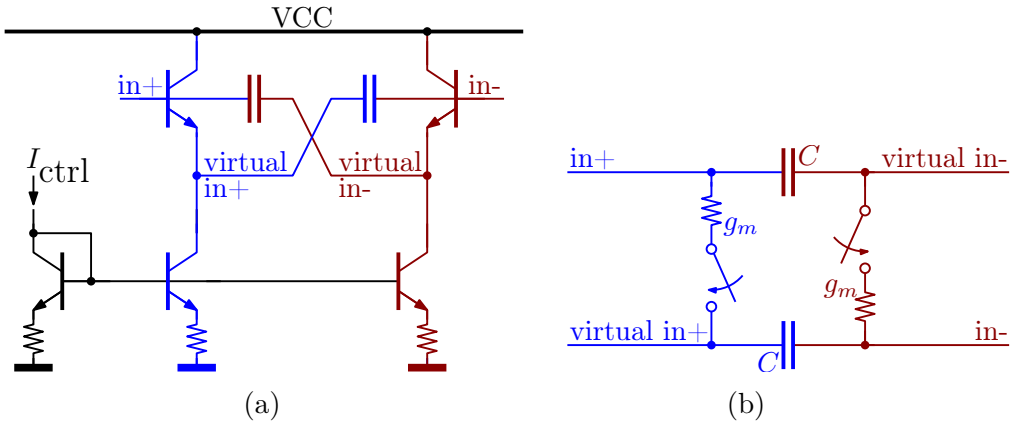


Figure 4.31: (a) Switchable capacitance and (b) equivalent circuit.

The parallel inductance and the parallel capacitance do not differ significantly from their series counterparts and their indices are dropped in the following:

$$\begin{aligned} L_p &= L_s \frac{Q^2+1}{Q^2} \approx L_s = L, \\ C_p &= C_s \frac{Q^2}{Q^2+1} \approx C_s = C. \end{aligned} \tag{4.66}$$

The parallel resistance R_p is much larger than R_s

$$R_p = R_s \left(Q^2+1\right) \approx R_s Q^2, \tag{4.67}$$

which intuitively makes sense: The small R_s is much smaller than the impedance of the series inductance. The parallel resistor R_p must be much bigger to have the same effect on the equivalent parallel circuit.

The Q-factor of the new circuit is the same as the Q-factor of the series circuit so R_p can be expressed in terms of the parallel inductance and the parallel capacitance:

$$\begin{aligned} R_p &= X_L Q = \omega_0 L \; Q \\ &= X_C Q = \frac{Q}{\omega_0 C}. \end{aligned} \tag{4.68}$$

With these equations the transconductance of the Q-enhancement TCA becomes

$$G_\mathrm{q} = -\frac{1}{R_p} = -\frac{1}{R_s Q^2} \tag{4.69}$$

$$= -R_s \frac{C}{L}. \tag{4.70}$$

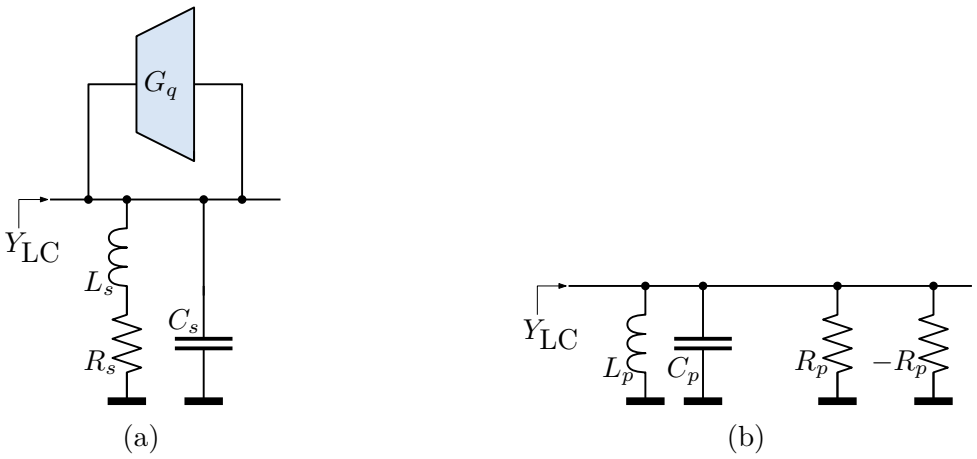


Figure 4.32: (a) LC-resonator with lossy inductor and Q-enhancement transconductance amplifier. (b) Equivalent circuit at the resonance frequency. The Q-enhancement transconductance provides the negative resistance which cancels the resistive losses of the inductor.

5 Bandpass Delta-Sigma Modulator Implementations

Two CT-BPDSMs are presented in this work: a non-tunable modulator with fixed transconductance and a fixed signal frequency of 2.2 GHz [71]. And a tunable modulator with configurable TCAs and configurable LC-resonator for a signal frequency between 1.55 GHz and 2.45 GHz [51].

The design, the architecture and the topology of the tunable modulator are derived from the non-tunable modulator. In the signal path, only the TCAs and the capacitances are replaced with a configurable version. The configuration is stored in an on-chip register. Both modulators have the same pad cage and occupy a chip area of 2.2 mm^2. They are fabricated in the bipolar technology B7HF200 from Infineon. The technology has a transit frequency of 200 GHz.

The design of both modulators is described in Chap. 5.1. Chap. 5.2 lists the nonlinearities of the modulators. The experimental results of the modulators are presented in the sections Chap. 5.3 and Chap. 5.4.

5.1 Modulator Design

Chap. 3 presents the choice for a CT-BPDSM architecture and the calculation of the feedback coefficients. The architecture is simulated and optimized with Matlab [44]. The optimized model is transferred into a behavioral model with Verilog-A components in the IC design environment from Cadence [72]. The model includes all components from the discrete-time DSM model in Fig. 3.13. A flip-flop with two latches realizes the comparator. The digital delays z^{-1} transform into latches as well. The resonator is an ideal LC-circuit.

Fig. 5.1 shows the block diagram of the next step with the modulator on transistor-level. The transistor-level schematic uses the components described in Chap. 4. The DAC is the only component that is not explicitly mentioned in Chap. 4; it is implemented with a differential pair. Infineon provides the layout of the coil in the resonator and the corresponding coil model.

For each component of the modulator, an ideal and a transistor-level model are available. Mixed-mode simulations allow the designer to optimize each component separately. Tab. 5.1 lists the values of the circuit elements in the analog building blocks.

Some early CT-BPDSM designs show common-mode oscillations. To damp the common-mode gain, the capacitance C_{fix} of the loop filter is implemented with two single-ended capacitors: one capacitance C_{fix} is connected between the positive signal node and GND; another capacitance C_{fix} is connected between the negative signal node and GND.

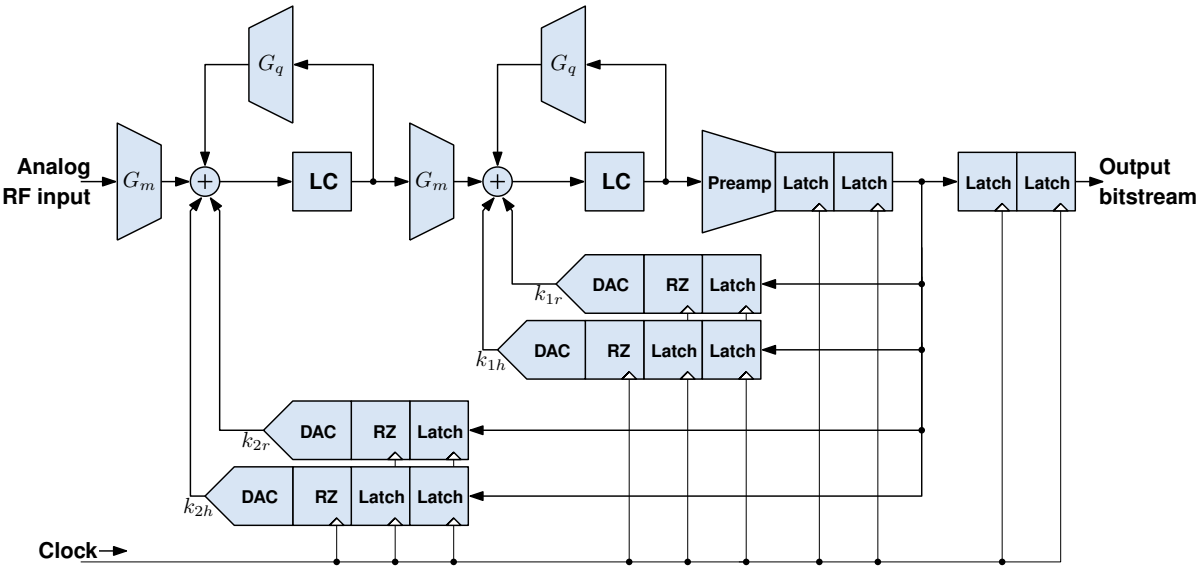


Figure 5.1: Block diagram of the non-tunable CT-BPDSM.

Table 5.1: Circuit properties of the non-tunable CT-BPDSM. The TCA is implemented as a resistively degenerated differential pair (cf. Fig. 4.24a).

Component	Variable	Value
Signal path TCA		
	G_m [mS]	8.1
	R_E [Ω]	115
	I_0 [mA]	8.0
Q-enhancement TCA		
	G_q [mS]	2.0
	R_E [Ω]	460
	I_0 [mA]	2.0
Loop filter		
	C_{varactor} [fF]	103 ... 234
	C_{fix} [pF]	2.6
	L [nH]	1.75
	C_L [fF]	22.1
	R_L [Ω]	1.44
	f_0 [GHz]	2.2

The output spectrum of the transient simulation of the transistor model is shown in Fig. 5.2a. The modulator output is sampled in the middle of the cycle. The analog samples are converted into a bit stream. A discrete time Fourier transform (DFT) is applied on 16384 of these digital samples. This yields an estimation of the CT-BPDSM output spectrum. The "real" output spectrum can only be calculated with an infinite sequence of samples. Taking only a finite number of samples is equivalent to the multiplication of the sequence with a rectangular window. The multiplication in time domain corresponds to convolution in frequency domain with a *sinc* function. Frequency components that do not fall directly in a DFT bin leak into several bins in the vicinity.

Explicit windowing allows for a trade-off between dynamic range and frequency resolution. The rectangular window has excellent frequency resolution but low dynamic range due to leakage. The Hann window is considered to be a good compromise [39], [73], [74] and is chosen in this work. For the Hann window, an input tone only leaks into the two adjacent bins.

The estimation of the SNR is done with the help of the Delta-Sigma Toolbox in Matlab [73]. In the resulting spectrum, the power sum of three bins—the bin of the signal frequency and the adjacent bins—is the signal power. The noise power is the sum of the other bins. The estimation neglects the 3 missing noise bins.

The number of simulated cycles is 100 cycles larger than the number of evaluated bins. These 100 cycles are skipped at the beginning to reduce the dependency on the simulated initial conditions. The input signal is a sinusoid with a signal frequency f_0 centered on the DFT bin 4379:

$$f_0 = \frac{4379}{16384} f_s \approx 2.14\,\text{GHz}. \tag{5.1}$$

To prevent leakage, the signal frequency must be specified with high accuracy to the simulator.

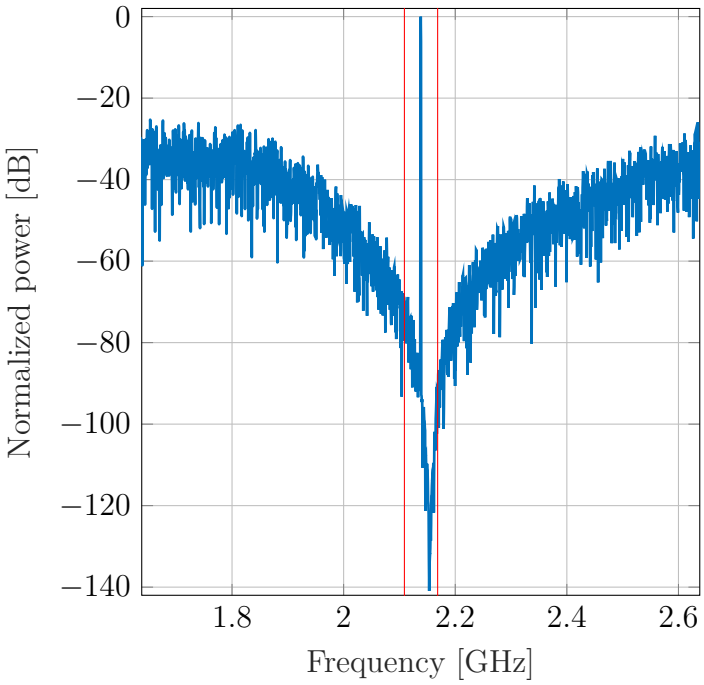
All simulations use a clock frequency of 8 GHz and the feedback coefficients from (3.71). Fig. 5.2b shows the SNR vs. the bandwidth of the signal band for the ideal model, for the transistor-level model and for the transistor-level model with electrostatic discharge (ESD) protection circuit (Chap. 5.2).

5.2 Non-Idealities and Performance Limitations

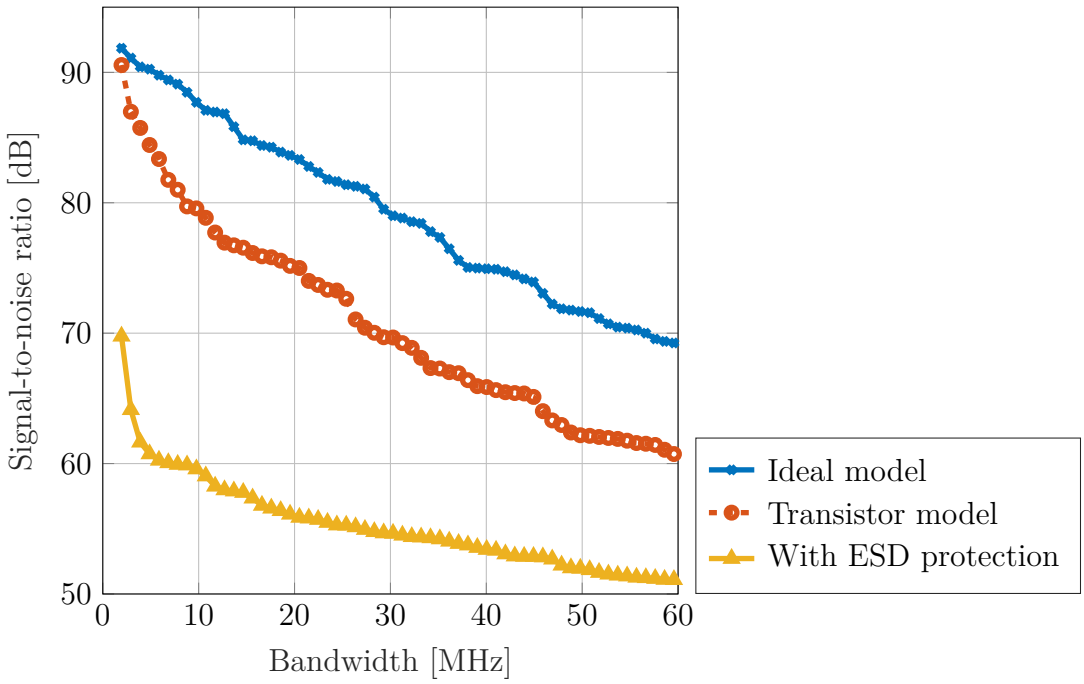
This section gives an overview over the performance limitations of the implemented modulators. They are listed in descending order of importance.

A reduced resonator Q-factor leads to less noise shaping and a smaller SNR. The modulators were not extracted and resimulated before tapeout. Three circuits feed the resonator with current: the signal TCA, the switched capacitance and the Q-enhancement TCA. The large size of these components and the large length of the interconnects introduce parasitic resistances that reduce the Q-factor of the resonator. These parasitics were not taken into account for the design of the Q-enhancement TCA.

The dependency of the SNR vs. the transconductance of the Q-enhancement TCA is investigated for the non-tunable modulator in Fig. 5.3. The optimum SNR is reached at a



(a)



(b)

Figure 5.2: Transient simulation results for the non-tunable CT-BPDSM: (a) output spectrum of the transistor-level model. The red bars highlight the signal band with 20 MHz bandwidth. (b) Signal-to-noise ratio vs. bandwidth.

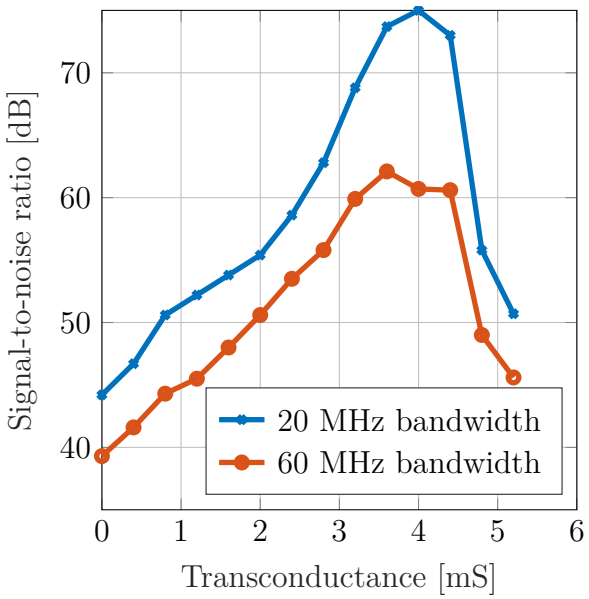


Figure 5.3: Signal-to-noise ratio of the modulator vs. the transconductance of the Q-enhancement transconductance amplifier.

transconductance that is about two times as large as the implemented transconductance on the test chip.

The maximum feedback DAC currents for the modulators are limited to small values. Each input pad for a control current is directly connected to an ESD protection diode. The distance from the pad to the current mirror is large. At the current mirror, a 1-kΩ-resistor is connected in series to the current sink to protect the control current from coupling noise. For large control currents, the voltage drop across the resistor will increase and the ESD protection diode will short the control current. The effect of the reduced feedback currents is simulated and depicted in Fig. 5.2b.

Excess loop delay is the delay between the quantizer and the feedback DAC [75]–[77]. The delay introduces a time shift to the feedback DAC pulses. Instead of RZ and HRZ pulses, the more complicated general DAC pulses from (3.65) must be used for analysis. A delay of the HRZ pulse leads to a DAC pulse in the *next* cycle. That increases the order of the loop filter.

Different strategies to compensate excess loop delay exist including the retuning of the feedback coefficients and the introduction of an additional feedback DAC [28], [77]. In this work, the excess loop delay is reduced with circuit techniques: the clock input of the sampling latch is delayed relative to the feedback DAC. The sampling latch still exhibits delay; however, the delay is compensated by a shorter digital delay to the feedback DAC.

Fig. 5.9 shows the full block diagram of the tunable CT-BPDSM including the clock tree. The clock tree follows the signal flow and has different feed points for the feedback DAC and for the quantizer. The delay from the quantizer through the feedback DAC and back to the quantizer is matched to the delay in the signal path.

Clock jitter affects mainly the feedback DACs. Bandpass modulators and modulators with many DAC edges are especially prone to jitter [39], [78]. The clock tree is designed for maximum bandwidth to reduce performance degradation due to jitter. The signal source for the measurements exhibits an rms jitter of less than 100 fs [79], so the impact of jitter is considered to be low.

Metastability is a concern for CT-BPDSM with very high sampling rate [39], [80]. The transit frequency of the bipolar technology in this work is very high in comparison to the sampling frequency. The simulations in Chap. 4.3.6 indicate that metastability can be neglected. Nevertheless, two latches are added to the output to prevent metastability at the output.

5.3 Measurement Results for the Non-Tunable Bandpass Delta-Sigma Modulator

Fig. 5.4 shows the measurement setup for the non-tunable CT-BPDSM (Fig. 5.1,Tab. 5.1). The clock input is driven by the signal generator SMF-100A with a clock frequency of 7.5 GHz. An SMU-200 signal generator provides sinusoidal and modulated RF-signals for the signal input. The modulator output is analyzed by the vector signal analyzer FSQ-8. 180°-hybrids convert between single-ended and differential voltages at the inputs and the output. The supply voltage and the control currents are generated by a programmable voltage supply and by the parameter analyzer HP 4155b. All measurement instruments offer a IEEE-488 / GPIB interface and are controlled by Matlab.

Fig. 5.5 shows a die photograph of the modulator. Only half of the chip area is occupied by the modulator. Nevertheless, the same pad cage as the tunable modulator must be used because the modulator is designed for on-chip measurements. A transmission line connects the modulator output with the pads.

The circuit draws 450 mW from a supply voltage of 3.6 V. Fig. 5.6 shows the output eye diagram. The single-ended voltage swing is 300 mV. For ideal BPDSMs, the probabilities for logic HIGH and for logic LOW at the output are equal. At very low input voltages, this is no longer the case. A small offset of the sampling latch is the probable reason.

Fig. 5.7a shows the output spectrum, Fig. 5.7b the output power and the noise power in a bandwidth of 20 MHz. At a certain frequency offset from the signal frequency, the noise power is measured. The total noise power is estimated by extrapolation from that point. This is legitimate because the notch in the spectrum is sufficiently flat within a bandwidth of 20 MHz.

The 1-dB-compression point is at an input power of −8 dBm. The modulator becomes instable 1 dB below the 1-dB-compression point. Instability becomes apparent immediately in the output spectrum: the noise floor drops and intermodulation products appear. In a bandwidth of 20 MHz, the maximum SNR is 45 dB, the maximum SNDR is 43 dB.

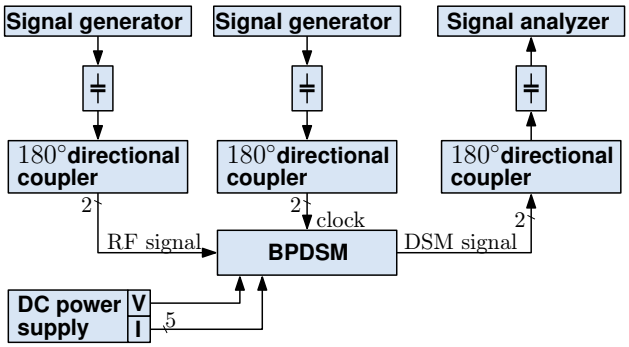


Figure 5.4: Measurement setup for the non-tunable CT-BPDSM.

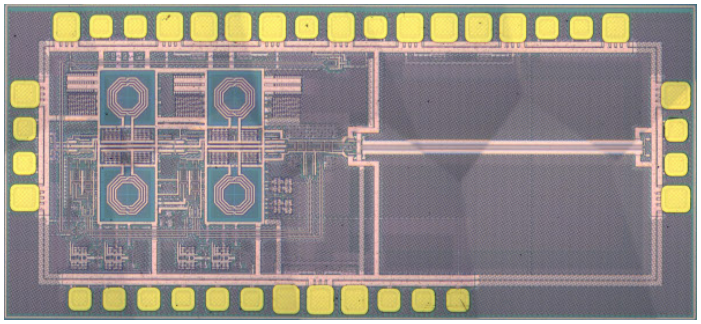


Figure 5.5: Die photograph of the non-tunable CT-BPDSM.

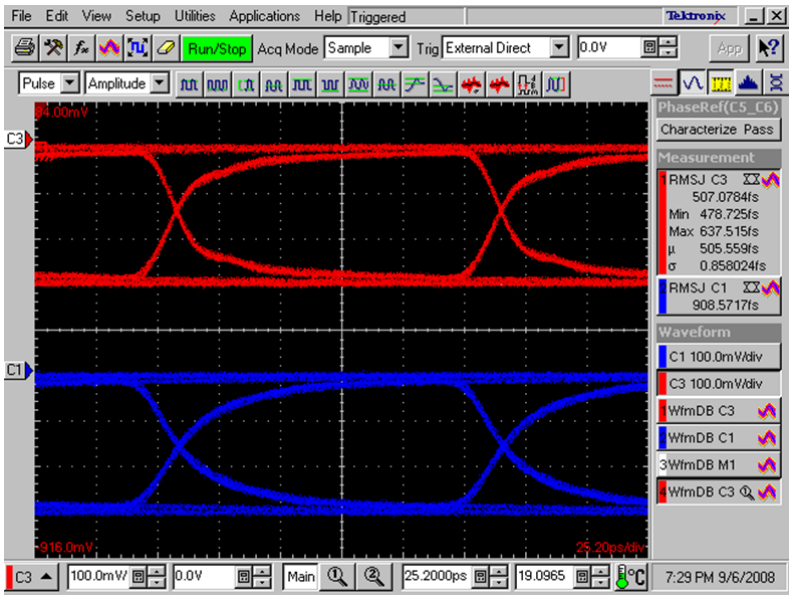
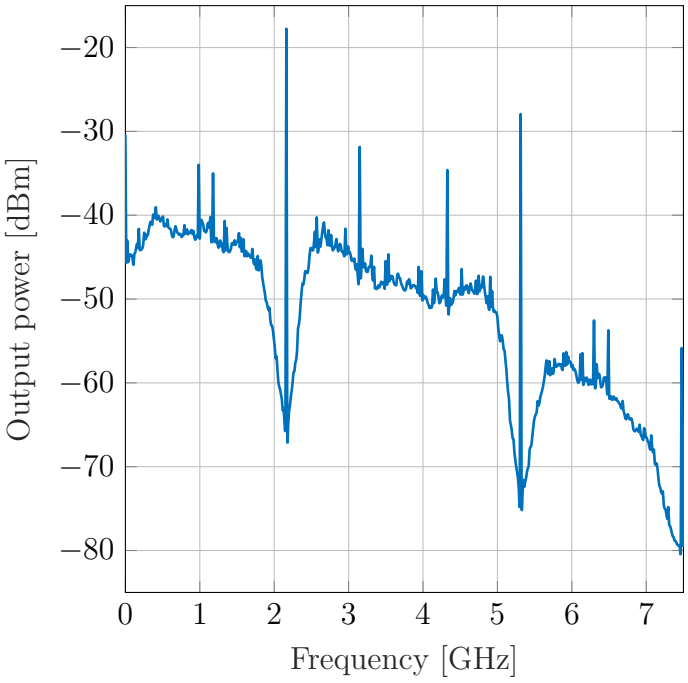
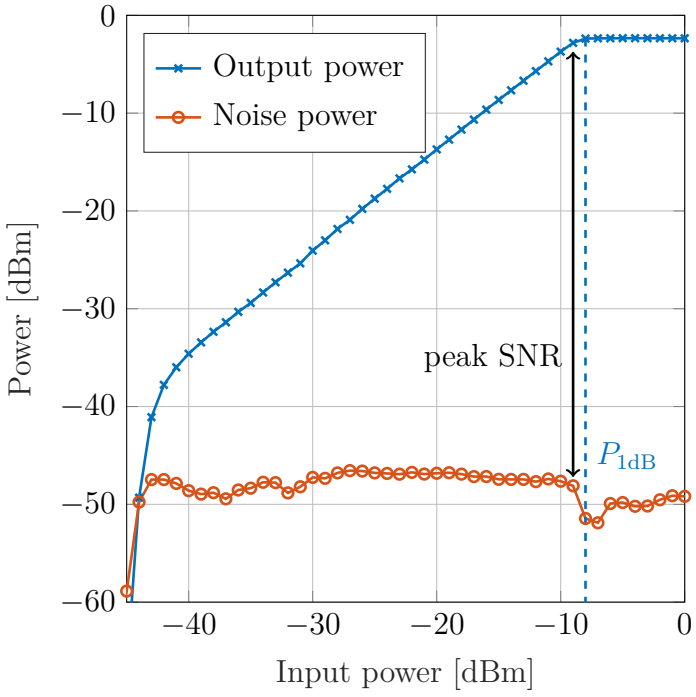


Figure 5.6: Measured eye diagram of both channels of the differential output. The small asymmetry is mainly caused by the off-chip RF components.



(a)



(b)

Figure 5.7: (a) Measured output power spectrum of the non-tunable CT-BPDSM and (b) corresponding output power and noise power within a signal bandwidth of 20 MHz vs. the input power.

5.4 Measurement Results for the Tunable Bandpass Delta-Sigma Modulator

Fig. 5.8 shows the block diagram of the tunable CT-BPDSM. The tunable modulator differs from the non-tunable modulator by a configuration register, by configurable TCAs and by configurable resonators. Each TCA and each resonator offer a programming range of 5 bits. The detailed block diagram in Fig. 5.9 includes additional information about the sizing of the building blocks.

Each configurable TCA consists of 5 binary weighted TCAs (cf. Fig. 5.10a). Each of these TCAs is a resistively degenerated differential pair from Chap. 4.4.3 because this implementation offers the best trade-off between linearity and noise. Each stage can be switched on or off with a control current coming from the configuration register.

The values of the circuit elements of the TCAs are listed in Tab. 5.2 and Tab. 5.3. The Q-enhancement TCAs use the same circuit design for the stages; however, the transconductance values are smaller. The signal path TCA stages 2, 1 and 0 are identical to the Q-enhancement-TCA stages 4, 3 and 2, respectively.

The configurable resonator is depicted in Fig. 5.11. It uses the same coil and the same varactor as the non-tunable modulator. A part of the capacitance is implemented as two single-ended, fixed capacitors $2C_{\text{fix}}$ against GND. The last part is implemented with the configurable capacitance in Fig. 5.10b. Similar to the TCA, the configurable capacitance has 5 binary weighted stages. Each stage can be switched on or off with a control current. The circuit of the switchable capacitance is introduced in Chap. 4.5.

The total capacitance is given by

$$C_{\text{tot}} = C_{\text{fix}} + C_{\text{varac}} + C_0 \sum_{k=0}^{4} a_k 2^k;\ a_k \in \{0,1\}, \tag{5.2}$$

where a_k are the control bits for the capacitance in the configuration register. The values for the capacitances are summarized in Tab. 5.4.

The control current for each stage is 1 mA. Each emitter follower in the smallest capacitor stage draws 1 mA from the voltage supply. The supply currents of the stages follow the binary scaling. If all stages are switched on, the total additional current per resonator is given by

$$I_{\text{cap,tot}} = 2\,\text{mA} \cdot \sum_{k=0}^{4} 2^k + 5\,\text{mA} = 67\,\text{mA}. \tag{5.3}$$

On chip level, the additional power consumption for all capacitances amounts to 415 mW for a supply voltage of 3.1 V.

5.4.1 Sinusoidal input signal and two-tone test

Fig. 5.12 shows the measurement setup for the tunable CT-BPDSM. The measurement setup for the non-tunable modulator is reused and an Agilent 34907A multi-I/O-module

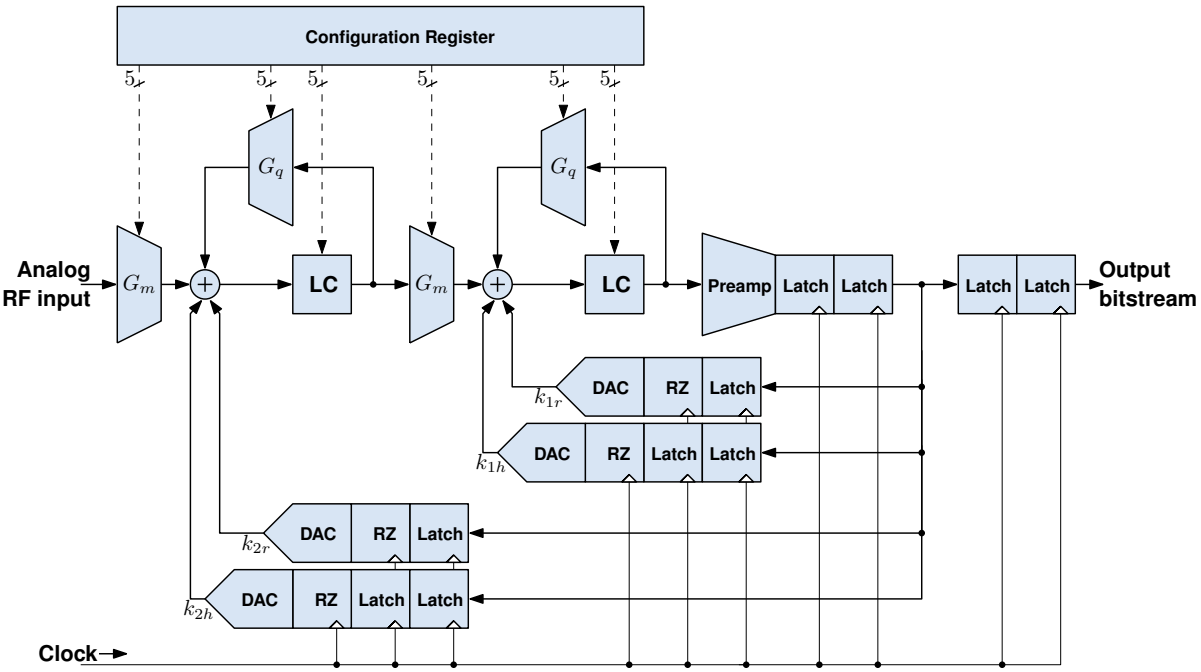


Figure 5.8: Block diagram of the tunable CT-BPDSM.

Table 5.2: Signal path transconductance amplifier (TCA) of the tunable CT-BPDSM. The TCA in Fig. 4.24a is used for the stages.

Binary index	4	3	2	1	0
G_m [mS]	8.1	3.95	2.0	1.0	0.5
R_E [Ω]	115	230	460	920	1840
I_0 [mA]	8.0	4.0	2.0	1.0	0.5

Table 5.3: Q-enhancement transconductance amplifier (TCA) of the tunable CT-BPDSM. The TCA in Fig. 4.24a is used for the stages.

Binary index	4	3	2	1	0
G_q [mS]	2.0	1.0	0.5	0.25	0.125
R_E [Ω]	460	920	1840	3680	2·3680
I_0 [mA]	2.0	1.0	0.5	0.25	0.125

Table 5.4: Loop filter capacitance of the tunable CT-BPDSM. The switchable capacitance in Fig. 4.31 is used for the stages.

Capacitance type	Schematic capacitance	Extracted capacitance
C_{fix} [fF]	885	928
C_{varac} [fF]	103...234	103...234
C_0 [fF]	32.8	62.1

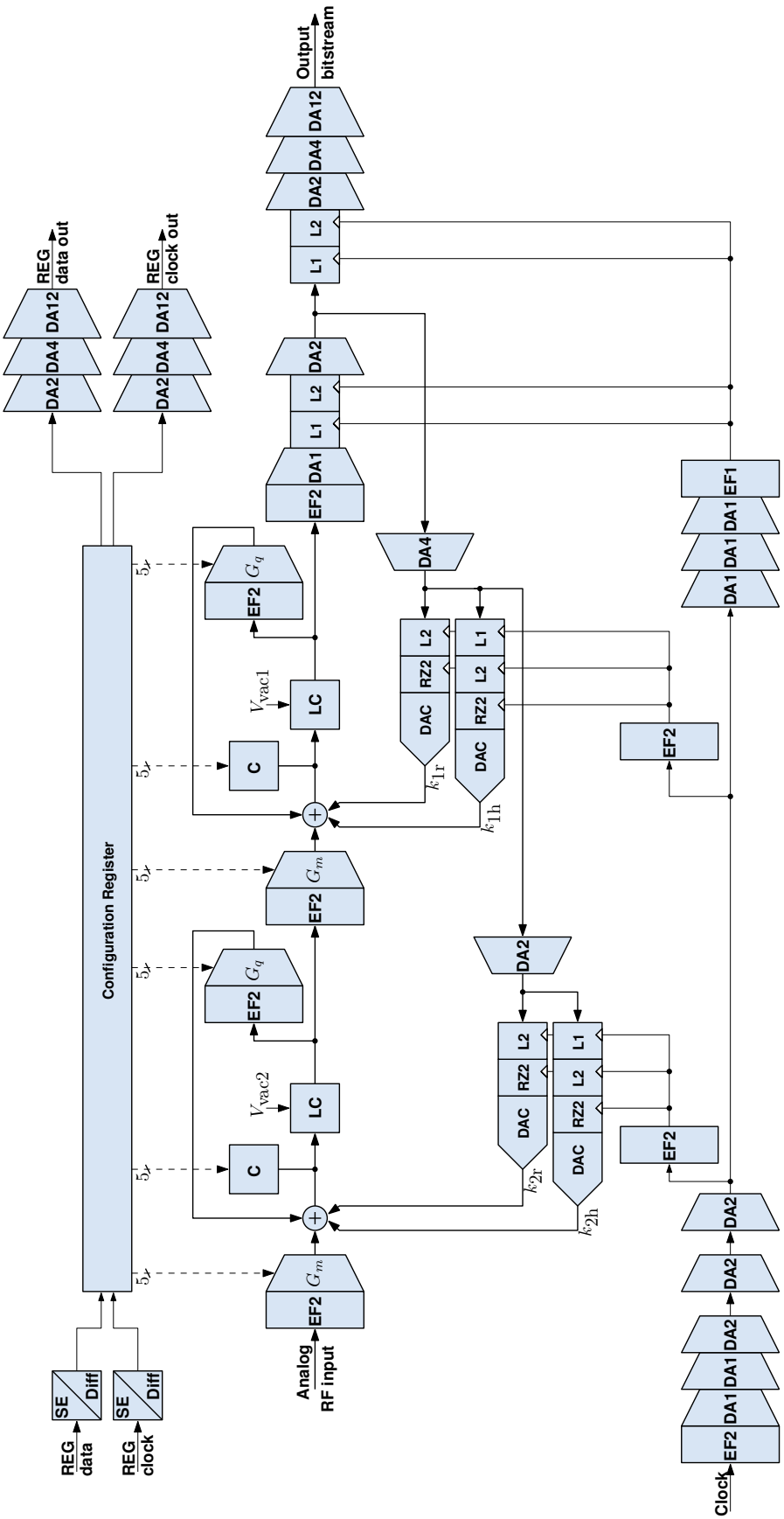
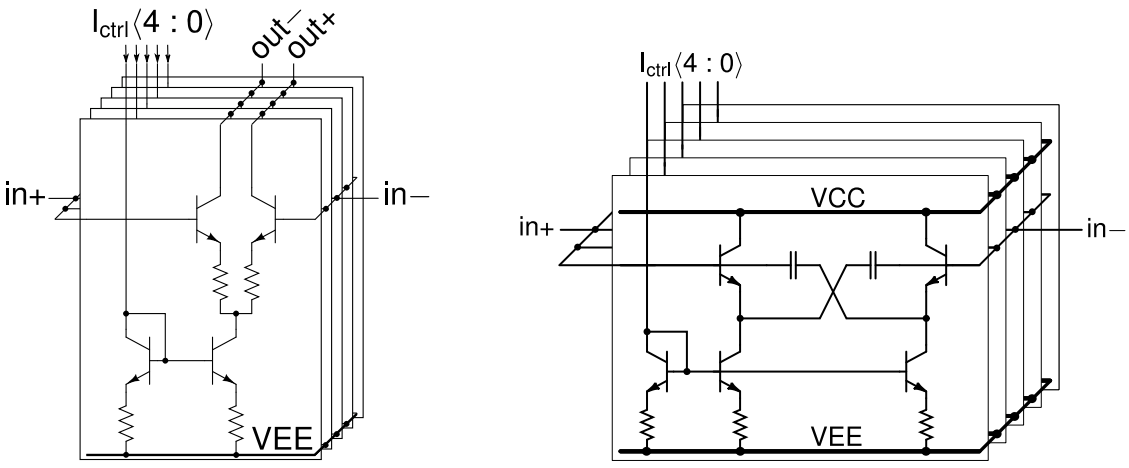


Figure 5.9: Complete block diagram of the tunable CT-BPDSM with sizing information: the number at the end of L1, L2, DA1, DA2, DA4, DA6, EF1, EF2, RZ2 denotes the tail current in mA.



(a) (b)

Figure 5.10: (a) Configurable transconductance amplifier (TCA) and (b) configurable capacitance.

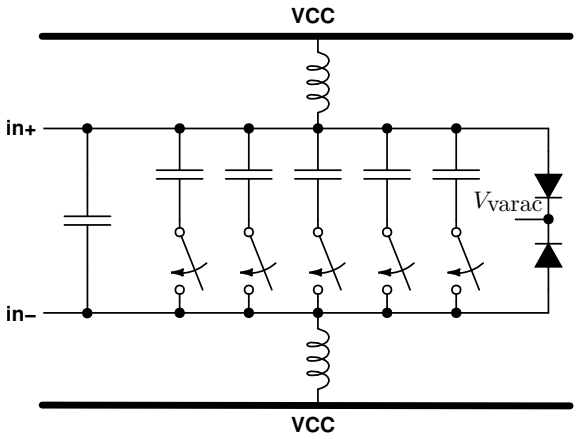


Figure 5.11: Behavioral circuit for the configurable resonator.

is added. The DAC outputs of the I/O-module write to the configuration register. The configuration register is implemented as a 2-wire shift register. The output of the configuration register is read in by the I/O module to verify the correctness of the written data.

For comparison with the non-tunable modulator, the configuration register is set to the same signal frequency as the non-tunable modulator. Fig. 5.14a shows the output spectrum, Fig. 5.14b shows the output power and the noise floor vs. the input power. At 2.2 GHz, the achieved peak SNR of 45.5 dB is comparable to that of the non-tunable modulator. This indicates a low performance impact of the more complex circuitry.

The input power sweep is repeated for every capacitance configuration from 1.55 GHz to 2.45 GHz. The clock frequency remains unchanged at 7.5 GHz. Fig. 5.15 shows the output power for maximum SNR and the corresponding noise power in a signal bandwidth of 20 MHz. The peak SNR is larger than 40.7 dB for all configurations.

At maximum signal frequency, the tunable CT-BPDSM consumes 992 mW from a 3.1 V voltage supply. Many capacitances are switched on for lower signal frequencies. The power consumption increases to 1.27 W if all switchable capacitances are active.

Fig. 5.16 shows the measurement results of a two-tone test at 2.2 GHz. Both tones have the same power. The 1-dB-compression point is already at −12 dBm input power of one tone. This corresponds to a combined input power of −9 dBm which is a little lower than the 1-dB-compression point for a sinusoid. Already at an input power slightly below the 1-dB-compression point, the modulator becomes instable and the non-linearities rise quickly.

5.4.2 Mobile communications signal for the universal mobile telecommunications system

Both modulators are developed by order of Alcatel-Lucent[1]. The measurements with sinusoids, the two-tone tests and measurements with simple UMTS signals are done at the Institute of Electrical and Optical Communications Engineering (INT).

The modulator is designed for the encoding of a mobile communication signal into a bit stream. The characterization results for UMTS signals are provided by Alcatel-Lucent [81]. Only a small subset of the measurement results with the tunable modulator is presented here. All of these measurements use one UMTS-carrier and a 16-QAM signal.

ACLR measurements verify the linearity of the modulator. Equation (2.1) defines the ACLR. The mean power in the adjacent channels must be 45 dB smaller than the power in the signal band. The mean power in the alternate channels must be 50 dB smaller than the power in the signal band.

Fig. 5.17 shows the ACLR measurements of an unclipped and a clipped UMTS signal at 2.3 GHz. Both pass the ACLR specifications of UMTS.

Fig. 5.18 and Fig. 5.19 show the ACLR measurements of clipped and unclipped UMTS signals at different signal frequencies. The modulator passes the specifications for signal

[1] now Nokia

frequencies above 1.81 GHz. Fig. 5.20 presents the same results vs. the input signal frequency.

EVM measurements are linked to the SNR of the modulator. The EVM for the unclipped signal is typically very low in comparison to the UMTS requirements. Clipping increases in-band noise to a level that is just below the EVM limit. Fig. 5.21 shows the EVM results for an input power sweep. Fig. 5.22 shows the minimum EVM vs. frequency.

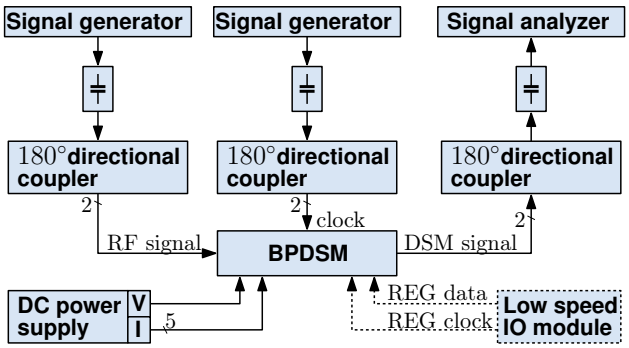


Figure 5.12: Measurement setup for the tunable CT-BPDSM.

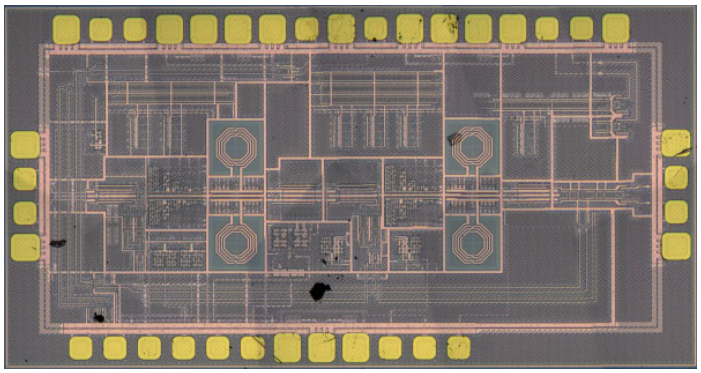
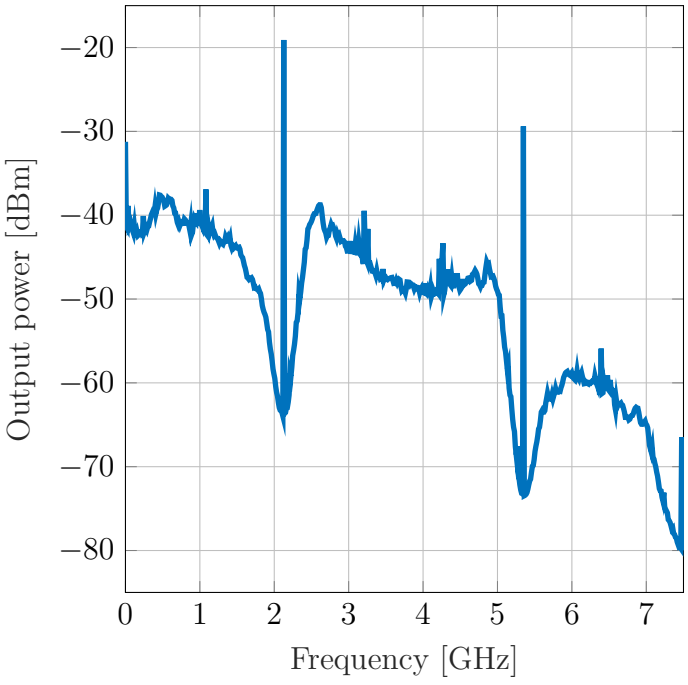
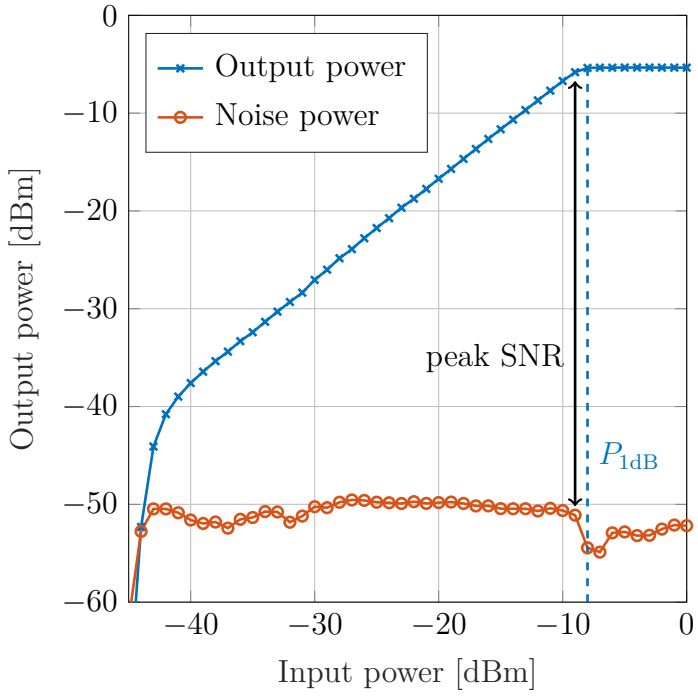


Figure 5.13: Die photograph of the tunable CT-BPDSM.



(a)



(b)

Figure 5.14: (a) Measured output power spectrum of the tunable CT-BPDSM for a signal frequency of 2.2 GHz and (b) corresponding output power and noise power within a signal bandwidth of 20 MHz vs. the input power.

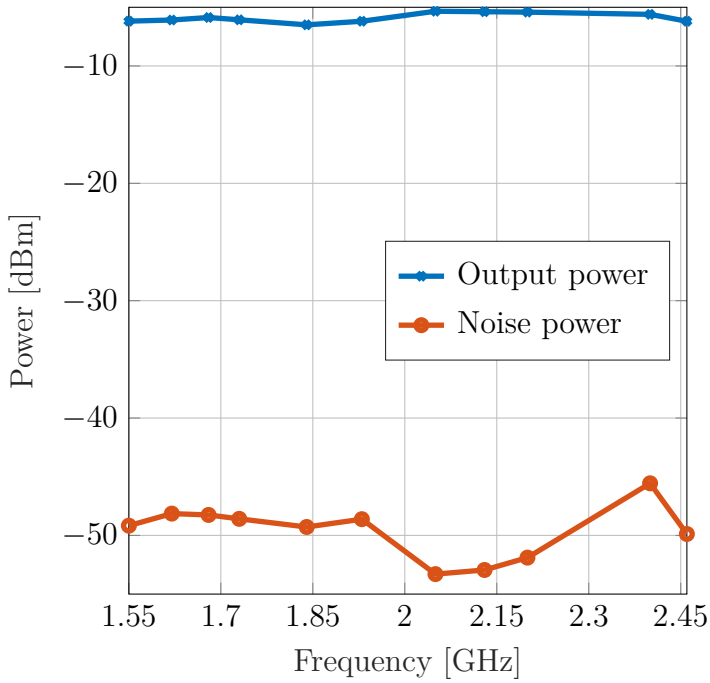


Figure 5.15: Measured output power and noise power in a bandwidth of 20 MHz vs. the signal frequency at the input power with the maximum SNR.

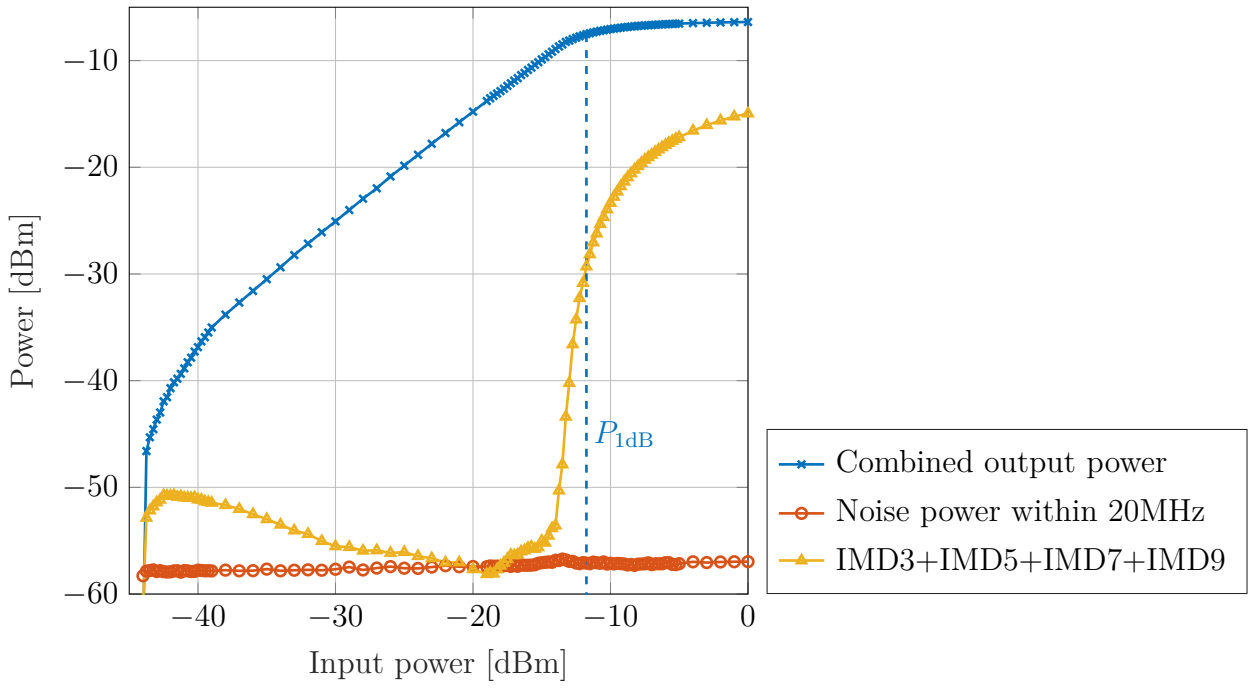


Figure 5.16: Two-tone measurement of the tunable modulator at a signal frequency of 2.2 GHz: output power, noise power and combined distortion power from the intermodulation products with orders 3, 5, 7 and 9 vs. the input power of one tone.

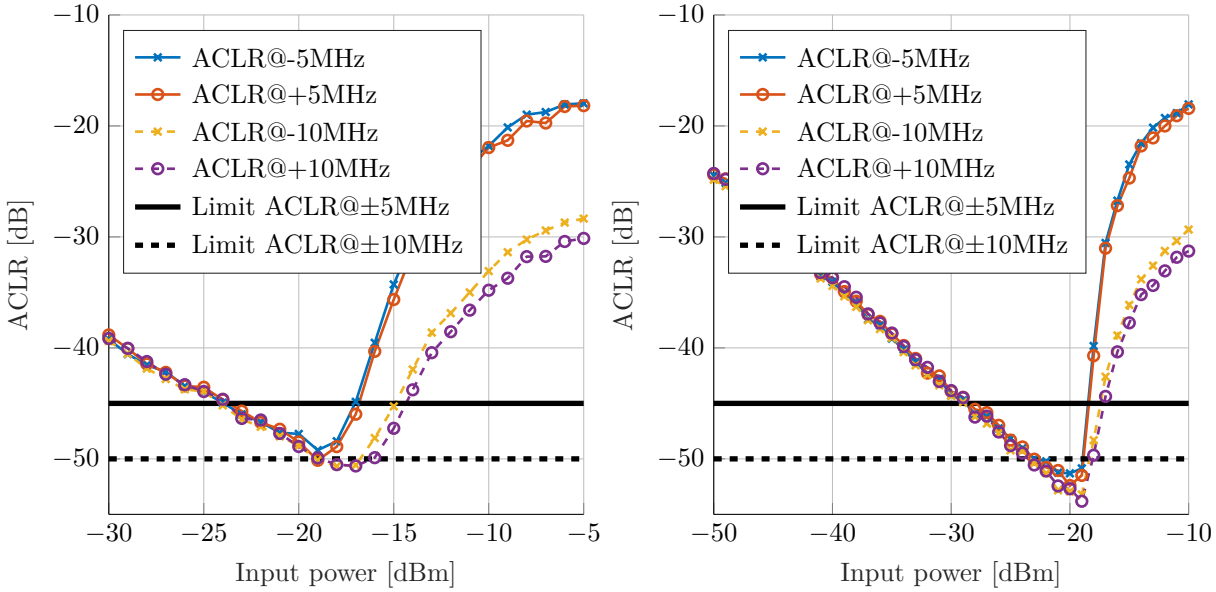


Figure 5.17: ACLR at f_{sig} =2.3 GHz vs. the input power for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].

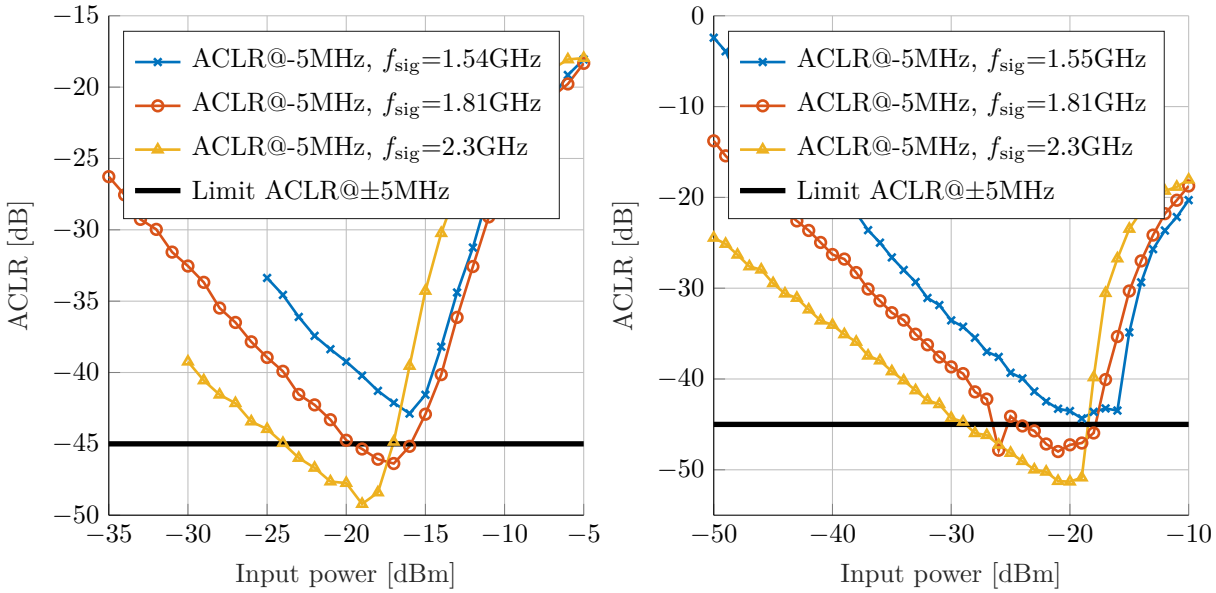
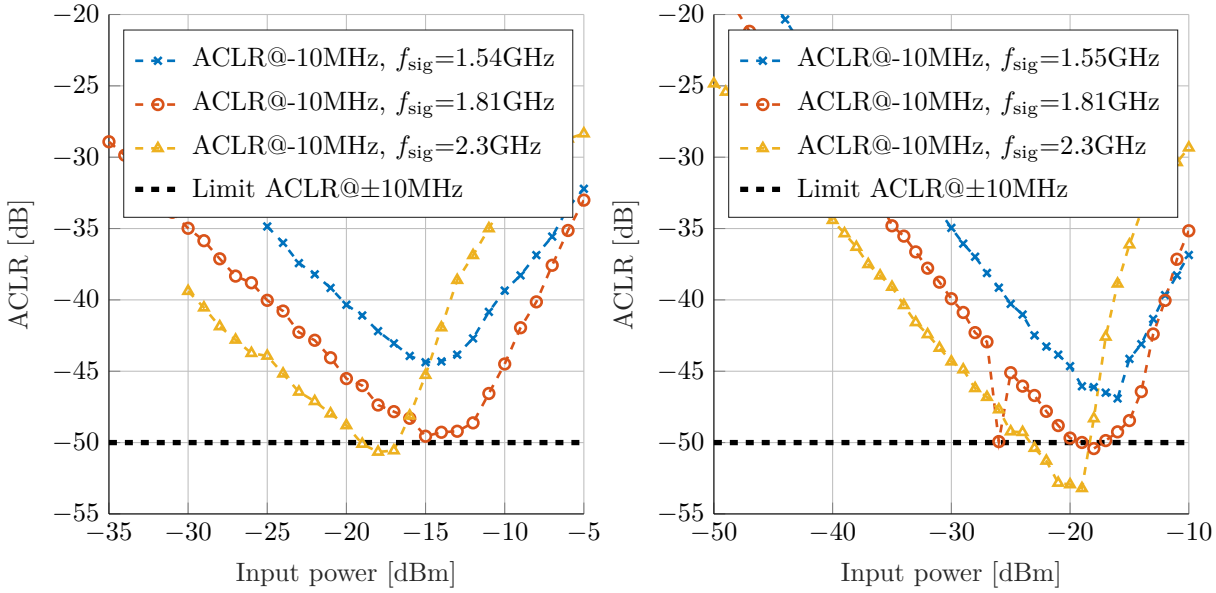
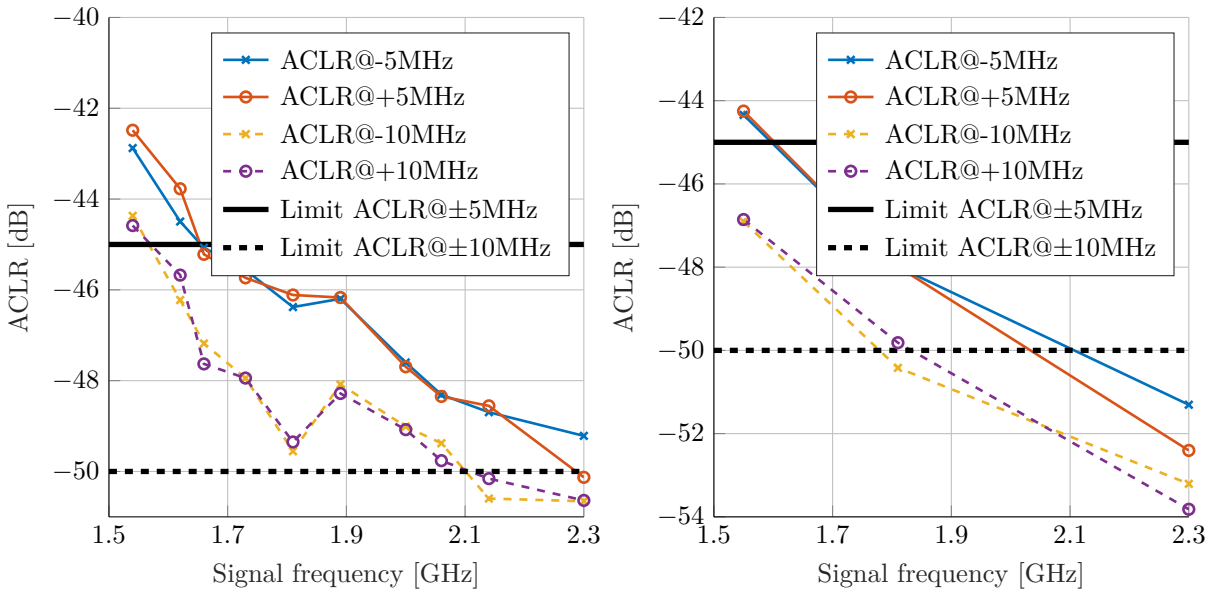


Figure 5.18: ACLR at −5 MHz vs. the input power for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].



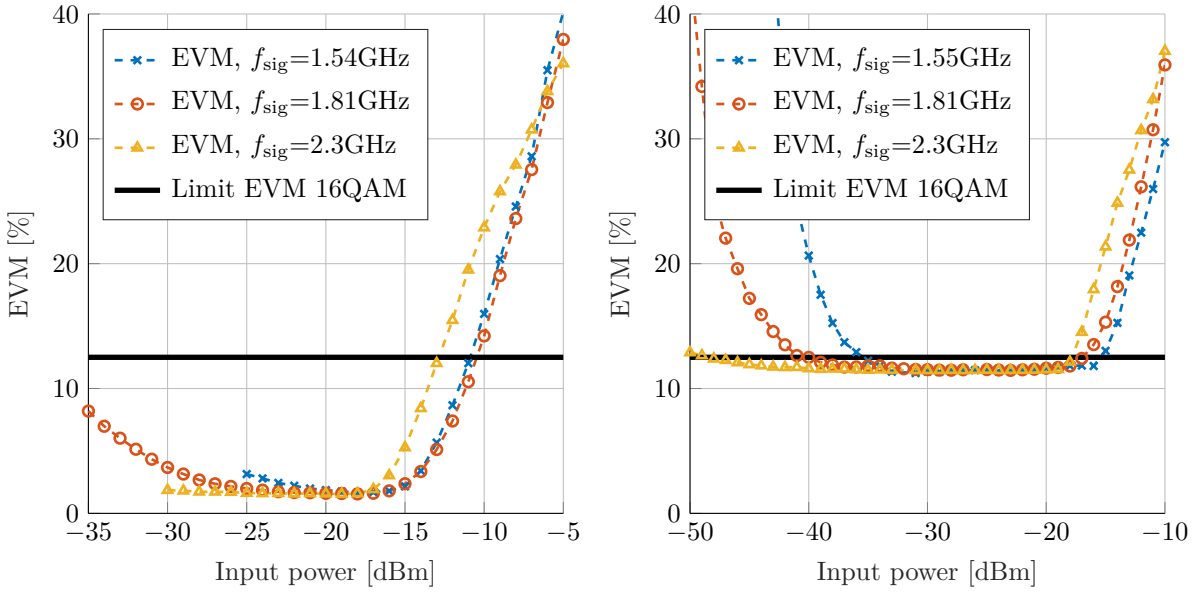
(a) (b)

Figure 5.19: ACLR at −10 MHz vs. the input power for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].



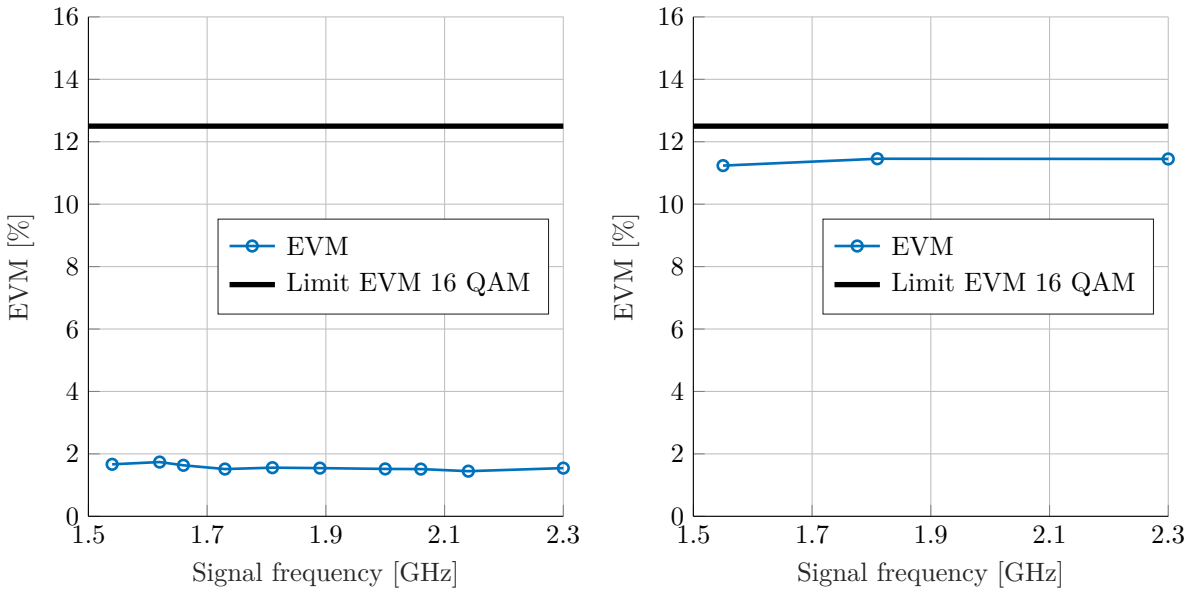
(a) (b)

Figure 5.20: Minimum ACLR vs. the signal frequency for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].



(a) (b)

Figure 5.21: Minimum EVM vs. the input power for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].



(a) (b)

Figure 5.22: Minimum EVM vs. the signal frequency for a UMTS signal with (a) PAPR=10.3 dB and (b) PAPR=5.4 dB. Courtesy of Alcatel-Lucent [81].

5.4.3 Summary and outlook

The aim of this work is to provide a modulator for switching-mode power amplifiers in RF transmitters for the downlink channel of UMTS base stations. Both modulators fulfill the requirements for the standard. The requirements are stringent and only one other CT-BPDSM [82] reports standard conform operation at a lower signal frequency.

Tab. 5.5 summarizes the state-of-the-art of CT-BPDSM. The modulators in this work achieve good SNR performance. The tunable modulator is the only modulator where the signal frequency is configurable within a range of 900 MHz.

A successor of the modulator should avoid the performance limitation by the ESD protection.

A stronger Q-enhancement TCA could improve noise shaping. The presented tunable TCA could reduce the occupied layout area and provide a continuously tunable transconductance.

Modern mobile communication standards require even more bandwidth. Recent publications [82], [83] use a 6^{th}-order design which promises higher bandwidth.

The presented modulators are not optimized for low power. Low design effort was spent on the configuration register and the associated interface. A redesign with low power techniques could reduce power consumption significantly.

If the redesign addresses higher sampling frequencies, the bandwidth of the amplifiers could be improved with emitter followers and cascode circuits.

Table 5.5: Comparison with the state-of-the-art.

	Ref.	Process	f_{sig} [GHz]	f_{clk} [GHz]	BW [MHz]	SNR [dB]	SNR* [dB]	Power [mW]
	[84]	BiCMOS	2	40	120	52	72.8	1600
	[85]	SiGe	2.2	9	10	43	53	270
	[86]	SiGe	2.2	5	10	46.6	56.6	330
	[87]	BiCMOS	0.9	2.2	10	43.8	53.8	-
	[38]	SiGe	1	4	20	37	50	450
	[88]	CMOS	2.4	6.1	80	41	80	53
	[83]	CMOS	2.4	3	60	40	57.8	40
	[89]	BiCMOS	0.95	3.8	1	59	59	75
	[82]	SiGe	0.78	3.13	35	56.7	72.1	1200
This work:								
Non-tunable	[71]	SiGe	2.2	7.5	20	47	60	450
Tunable	[51]	SiGe	2.2	7.5	20	45.5	58.5	1060
			1.55	7.5	20	40.7	53.7	1270

*normalized to 1 MHz

6 Conclusion

5G explores new frequency bands at 28 GHz and beyond. Higher frequency bands offer higher signal bandwidths and higher data rates up to 20 GBit/s. The high signal frequencies are difficult to attain for switching-mode power amplifiers (SMPAs) in the near future.

The range of the frequency band at 28 GHz is limited to less than 500 m. In contrast, the radius of a cell with a signal frequency of 450 MHz can extend to 50 km; at 2.5 GHz the cell radius is still 10 km [90]. Operators rely on the traditional signal bands in the frequency range between 450 MHz and 3.5 GHz to ensure good coverage.

The bandwidth in these frequency bands is limited and other ways to increase the data rate need to be found. Higher modulation orders of 256 and beyond are possible solutions to this problem. The drawback of higher modulation orders is the higher peak-to-average power ratio (PAPR). The power efficiency at high PAPR becomes even more important than today.

The class-S amplifier can cope well with high PAPR and it is an attractive way to incorporate many mobile communication standards and frequency bands into one transmit chain.

This work presents two continuous-time bandpass delta-sigma modulators (CT-BPDSM) for a class-S amplifier. One of the modulators supports broadband mobile communication signals in a frequency range between 1.55 GHz and 2.45 GHz.

Chap. 2 introduces the reader to mobile communication standards and transmit chains. It discusses RF-transmitters with linear power amplifiers and with class-D amplifiers.

The benefits of delta-sigma modulators are described in Chap. 3. The design of the modulator starts with a lowpass discrete-time prototype that is converted to a CT-BPDSM.

Chap. 4 introduces to circuit design in a bipolar technology with consideration of the relevant non-idealities. The chapter gives an overview over all building blocks of the modulator and over possible alternatives to the differential amplifier and to the transconductance amplifier (TCA). Simulations complement the theoretical analysis.

The CT-BPDSM architecture is implemented in Chap. 5. System simulations help to find the right design choices and help to analyze the measurement results. Two major improvements for future work are identified: first, a Q-enhancement TCA with higher transconductance could improve noise-shaping. Secondly, if the ESD protection diodes are connected behind the input RC-filter for the control current sinks, higher control currents and thus higher resonator voltages become available.

The tunable modulator is characterized with sinusoidal input signals, two-tone input signals and with UMTS-signals. It fulfills the requirements of UMTS in a frequency range from 1.8 GHz to 2.45 GHz and allows to gain experience with SMPAs.

Delta-sigma modulation continues to be an attractive solution for class-S amplifiers [91]. Instead of acting on the bandpass signal itself, it can be applied to the pulse width and the pulse position of a ternary RF-signal [92], [93]. Modern Complementary Metal Oxide

Semiconductor (CMOS)-SMPAs offer switching frequencies up to 4 GHz [94]–[96]. Together with a programmable output amplitude [97], [98], systems with even more resilience against high PAPR become possible.

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Acronyms

16-QAM 16-point quadrature amplitude modulation. 8, 9, 95

3GPP 3rd generation partnership project. 5

64-QAM 64-point quadrature amplitude modulation. 8

8-PSK 8-phase shift keying. 6, 8

ACLR adjacent/alternate channel leakage ratio. 9–11, 95, 100, 101

ADC analog-to-digital converter. x, 4, 20, 25–30, 33, 36

AWGN additive white Gaussian noise. 32, 34

BJT bipolar junction transistor. x, 12, 43–45, 47–50, 53–59, 61, 63, 67, 69, 74, 78

BPDSM bandpass delta-sigma modulator. 9, 15, 17, 43, 63, 88

BTS base station. 8, 11

CDMA code-division multiple access. 9

CEPT European conference of postal and telecommunications administrations. 5

CMCD current-mode class-D amplifier. 13, 15, 16

CML current-mode logic. 43, 58, 63, 66

CMOS complementary metal oxide semiconductor. 78, 105

CSD circuit-switched data. 5

CT-BPDSM continuous-time bandpass delta-sigma modulator. 3, 4, 17, 18, 35–38, 40, 41, 63, 83–93, 95, 97, 98, 103, 105

DA differential amplifier. 43, 56, 58–61

DA1 differential amplifier with 1 mA tail current. 59, 61

DA2 differential amplifier with 2 mA tail current. 59, 61

DA4 differential amplifier with 4 mA tail current. 59, 61

DAC digital-to-analog converter. 4, 20, 36–40, 83, 87, 88, 95

DFT discrete time Fourier transform. 85

DR dynamic range. 5, 28–30, 32, 33, 35

DSM delta-sigma modulator. viii, 20, 25, 30, 32–35, 37, 83

DTFT discrete-time Fourier transform. 25, 33

EDGE enhanced data rates for GSM evolution. 6

ENOB effective number of bits. 29, 30, 33, 35

ESD electrostatic discharge. 85, 87, 103, 105

ETSI European telecommunications standards institute. 5, 9

EVM error vector magnitude. 9, 11, 96, 102

FDMA frequency division multiple access. 8, 9

GBW gain bandwidth product. 59

GND ground. 52, 83, 91

GPRS general packet radio service. 6

GSM global system for mobile communications. 5, 6, 8, 9

HRZ half-return-to-zero. 37–39, 87

HSPA high speed packet access. 6

IF intermediate frequency. 15

IIP3 input-referred third-order intercept point. 22

IIP5 input-referred fifth-order intercept point. 22

IMD intermodulation product. 21, 22

IMD3 power of the third-order intermodulation product. 68, 79

INT Institute of Electrical and Optical Communications Engineering. 95

IOT internet of things. 6

ITU International Telecommunication Union. 6

LO local oscillator. 15

LTE long term evolution. 6, 8, 9

LTE-A LTE-Advanced. 6, 9

LTI Linear time-invariant. 23, 24

M2M machine-to-machine. 6

MOSFET metal oxide semiconductor field effect transistor. 78

NRZ non-return-to-zero. 36, 37

NTF noise transfer function. 30, 32–35

OFDMA orthogonal frequency-division multiple access. 9

OSR oversampling ratio. 30, 33, 35

PA power amplifier. 21

PAPR peak-to-average power ratio. 3, 5, 9, 11, 13, 100–102, 105, 106

pdf probability density function. 27

PSK phase shift keying. 6

PSS periodic steady state. 67, 76

PVT process, voltage and temperature. 54

QAM quadrature amplitude modulation. 8

QPSK quadrature phase-shift keying. 6, 8–10

RACH random-access channel. 8

RF radio-frequency. 3, 12, 13, 15, 17, 88, 105

RZ return-to-zero. 37–39, 63, 66, 87

SC-FDMA single-carrier FDMA. 9

SDMA space division multiple access. 9

SDR signal-to-distortion ratio. 20–22, 68

SDR3 signal-to-third-order-distortion ratio. 76

SMPA switch-mode power amplifier. xi, 3, 13, 16–18, 105, 106

SNDR signal-to-noise-and-distortion ratio. 20, 21, 29, 68, 88

SNR signal-to-noise ratio. 3, 5, 15, 20, 28–30, 40, 68, 76, 85, 88, 95, 96, 99, 103

STF signal transfer function. 30, 32, 33

TCA transconductance amplifier. vii, 43, 56, 67–72, 74–81, 83–85, 91, 92, 94, 103, 105

TDMA time-division multiple access. 8

UE user equipment. 3, 8, 9

UMTS universal mobile telecommunications system. 3, 4, 9, 11, 95, 96, 103, 105

VCC positive supply voltage. 72

VMCD voltage-mode class-D amplifier. 13, 15, 16

WAP wireless application protocol. 6

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