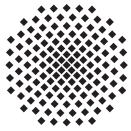

University of Stuttgart
Germany

Institute of
Robust Power
Semiconductor Systems

Master's Thesis

Evaluation and Characterization of a Reduced-Bandwidth Sampling System for Predistorting Broadband E-Band Communication Links

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Declaration

I hereby declare that this thesis is my own work and effort and follows the regulations related to good scientific practice of the University of Stuttgart in its latest form. All sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Stuttgart, 30.04.2021

Simon Bleickert

Executive Abstract

Today's communication link modulation formats, such as 5G New Radio or wideband Code Division Multiple Access (CDMA), require highly linear Radio Frequency (RF) front-ends to allow for sufficient bandwidth and efficient transmissions. Power Amplifiers (PAs) are the communication link's predominant nonlinear component. To avoid nonlinear behavior, PAs have to be operated in back-off in terms of PA input power. However, limiting the PA's input power reduces the available bandwidth and leads to PA inefficiency. If PA's linear amplification region would be higher, efficiency could be improved. One approach to compensate for PA nonlinearity is Digital Predistortion (DP). However, broadband DP puts high demands on the Analog-to-Digital Converters (ADCs) in terms of sampling rate. Therefore, costly broadband ADCs are required.

To address this issue, the Institute of Robust Power Semiconductor Systems (*Institut für Robuste Leistungshalbleitersysteme*, ILH) developed a low-cost Printed Circuit Board (PCB) that claims to be suitable for sampling 2.5 GHz baseband signals and therefore allowing for DP. This is achieved by downconverting and by sampling the broadband input signal in individual and narrowband frequency windows using a frequency mixer. In this study, it was investigated, whether the new PCB is capable of downconverting and sampling of 2.5 GHz bandwidths for a satellite communication link.

During testing, it was found that the hardware is not capable of sampling broadband signals due to a missing filter. Nevertheless, it was possible to sample a bandwidth of 700 MHz by adding filters manually. This implies, that the concept of sampling a broadband signal using low-cost components works.

However, in this thesis only the PCB and its sampling capabilities were examined and no DP was performed. Future studies might successfully develop and verify DP using low-cost, broadband downconverting and sampling PCBs. Such PCBs could be beneficial in predistorting broadband satellite communication links.

Zusammenfassung

Heutige Modulationen wie zum Beispiel 5G New Radio oder breitbandige Code Division Multiple Access (CDMA) benötigen hochlineare Übertragungsstrecken, um eine breitbandige und effiziente Signalübertragung zu ermöglichen. Hochfrequenzleistungsverstärker sind als nichtlineare Komponente ein ausschlaggebender Faktor für Linearität der Übertragungsstrecke. Um das nichtlineare Verhalten von Hochfrequenzleistungsverstärkern zu reduzieren, gibt es die Möglichkeit, die maximale Eingangsleitung zu reduzieren. Diese Reduzierung führt allerdings zu einer Limitierung der Signalbandbreite und auch zu einem ineffizienteren Betrieb des Hochfrequenzleistungsverstärkers.

Wenn der lineare Verstärkungsbereich von Hochfrequenzleistungsverstärkern erhöht werden könnte, könnte damit auch die Effizienz verbessert werden. Eine Möglichkeit, das nichtlineare Verhalten von Hochfrequenzleistungsverstärkern auszugleichen, ist die der digitalen Vorverzerrung. Allerdings werden zur digitalen breitbandigen Vorverzerrung ebenfalls breitbandige und damit teure Analog-Digital-Umsetzer benötigt.

Das Institut für robuste Leistungshalbleiter (ILH) hat eine kostengünstige Platine entworfen, die es ermöglichen soll, 2.5 GHz Basisbandsignale zur späteren Verwendung in einer digitalen Vorverzerrung abzutasten. Hierbei werden breitbandige Eingangssignale auf einzelne schmalbandige Frequenzfenster heruntergemischt und anschließend abgetastet.

In dieser Arbeit wurde untersucht, ob die Platine in der Lage ist, Signale mit einer Bandbreite von 2.5 GHz für eine Satellitenübertragungsstrecke herunterzumischen und abzutasten.

Während der Tests wurde festgestellt, dass die Platine aufgrund eines fehlenden Filters nicht in der Lage ist, breitbandige Signale abzutasten. Trotzdem war es möglich, eine kleinere Bandbreite von 700 MHz mithilfe von manuell hinzugefügten Filtern abzutasten. Daraus lässt sich schließen, dass das Konzept des Abtastens von breitbandigen Signalen mit kostengünstigen Bauteilen funktioniert.

In dieser Arbeit wurde nur die Platine und die Möglichkeiten der Abtretung von breitbandigen Signalen untersucht und keine digitale Vorverzerrung durchgeführt. Nachfolgende Arbeiten könnten die Platine weiterentwickeln und somit eine digitale Vorverzerrung ermöglichen. Eine solche Platine könnte für die digitale Vorverzerrung von breitbandigen Satellitenübertragungsstrecken hilfreich sein.

Contents

List of Abbreviations

ADC	Analog-to-Digital Converter
AP	Analog Predistortion
AWG	Arbitrary Waveform Generator
Balun	Balanced-unbalanced
BER	Bit Error Rate
CDMA	Code Division Multiple Access
COTS	Commercial off-the-shelf
CS	Chip Select
DC	Direct Current
DP	Digital Predistortion
EIVE	Exploratory In-Orbit Verification of an E/W-Band Satellite Communication Link
EVM	Error Vector Magnitude
GPIO	General Purpose Input/Output
I	In-Quadrature
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ILH	Institute of Robust Power Semiconductor Systems (*Institut für Robuste Leistungshalbleitersysteme)*
IMD	Intermodulation Distortion
IQTools	Keysight IQ Tools
LEO	Low Earth Orbit
LO	Local Oscillator
LUT	Lookup Table
MISO	Master Input, Slave Output
Modem	Modulator-demodulator
MOSI	Master Output, Slave Input
MTT-S	Engineers Microwave Theory & Techniques Society
MTT	Engineers Microwave Theory & Techniques
Nucleo	STM32 Nucleo Board by STMicroelectronics
OFDM	Orthogonal Frequency-Division Multiplexing
OR	Observation Receiver
PA	Power Amplifier
PAE	Power Added Efficiency

PAPR	Peak-to-average Power Ratio
PCB	Printed Circuit Board
Q	Quadrature
AM	Amplitude Modulation
RF	Radio Frequency
SNR	Signal-to-noise Ratio
SPI	Serial Peripheral Interface
SSH	Secure Shell
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier

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1. Motivation

High-data rates, reliable operation and efficient use of available bandwidth are crucial requirements for today's communication systems. Spectral efficiency is particular important as signal bandwidth is limited and leakage into other channels should be avoided.

Recent modulation formats such as 5G New Radio or wideband Code Division Multiple Access (CDMA) usually are characterized by high Peak-to-average Power Ratio (PAPR) [LP, Vye19]. In high PAPR communication links, signal linearity has to always be maintained and nonlinear effects have to be avoided.

Signal linearity in communication system's Radio Frequency (RF) front-ends is strongly influenced by Power Amplifiers (PAs). However, PAs amplify nonlinear above certain input power levels because of its semiconductor components [Cri06]. Operating PAs in their nonlinear region, leads to signal impairments such as spectral regrowth, Signal-to-noise Ratio (SNR) degeneration and amplification inefficiency. In frequency division multiplexing, spectral regrowth can cause PA signals to partially overlap with other channel's signals [FAA+15]. Degeneration of SNR increases Bit Error Rate (BER), thus limiting channel capacity. Inefficient PA operation increases heat dissipation and therefore may cause thermal issues [ZTT+99].

To compensate for these impairments, PAs have to be limited in their output power (backed-off), to avoid operation in nonlinear amplification regions. This results in loss of output power thus the PA's efficiency degrades.

High-power PAs, featuring linear amplification of broadband signals, as required for today's communication links, are expensive because complex hardware is required. Therefore, various linearization methods have been established in order to allow for implementation of regular PAs, compensating for their nonlinear characteristics.

Today's most promising linearization method is Digital Predistortion (DP) [MMK+06]. In DP, PA input and output signals are compared to each other and afterwards the input signal is predistorted based on the differences. The resulting, predistorted signal, results in a linear signal after having been amplified by the PA.

Analog-to-Digital Converters (ADCs) requires ADCs for sampling of both the PA's input and output signal. ADC sampling bandwidth can be a limiting factor in processing broadband signals because ADC sampling bandwidth typically scales with ADC cost.

In scope of Institute of Robust Power Semiconductor Systems (*Institut für Robuste Leistungshalbleitersysteme*, ILH)'s Exploratory In-Orbit Verification of an E/W-Band Satellite Communication Link (EIVE) project, ILH developed a Observation Receiver (OR) for sampling a 2.5 GHz band-

width based on Commercial off-the-shelf (COTS) components. The OR claims to mitigate the trade-off between broadband and low-cost DP: sampling of broadband input signals is achieved by downconverting the signal into multiple narrowband (reduced-bandwidth) frequency windows that are sampled individually by low-cost ADCs. This allows for broadband DP without expensive ADCs.

In this study, the fundamental OR functionality is examined and its suitability for implementation in satellite communication links is evaluated.

The thesis is structured as followed: The first chapter introduces PAs. Typical PA linearization methods and this works predistortion method are explained. Afterwards, the OR and its application within an E-Band satellite link in the scope of ILH's EIVE project is described. To understand the study experiments, the OR measurement setup is explained. The last two chapters discuss the measurement results and are completed by a short conclusion and outlook.

2. Radio Frequency Power Amplifier

This chapter introduces the fundamental concepts and principles of PAs. First, relevant figures of merit are introduced, followed by a detailed explanation of PA linearity, a major figure of merit in this work. Second, different predistortion techniques are presented and finally it is being focused on DP.

2.1. Power Amplifier Fundamentals

In general, a PA is an amplifying device right before the antenna in wireless communication systems. Its task is to amplify the RF signal in amplitude in such a way that it can be propagated by the antenna [Oxf]. In other words, the PA converts a low-power RF signal into a high-power RF signal to drive the antenna [Kal18]. On the receiving end, a low-noise amplifier amplifies the antenna's received signal. Afterwards, the signal is forwarded to the downconverting chain.

During transmission, a signal is subject to multiple impairments, for example attenuation, amplification or noise. However, in the following, it is being focused on impairments caused by the PA.

Important PA figures of merit are introduced, with focus on PA applications. There are also additional figures of merit such as third-order intermodulation intercept point, scattering parameters or intermodulation distortion, but these are not covered here. For a comprehensive overview of PA figures of merit see [Kal18, Cri06, NI].

2.1.1. Output Power and Gain

The fundamental task of a PA is to amplify power. This is achieved by increasing the input signal's amplitude by a certain ratio. The ratio between output power and input power is called power gain and usually represented as G. For better readability in the following the term power gain is abbreviated as gain. Gain is usually expressed in dB and power in dBm, respectively. The relationship between input power P_{in}, output power P_{out} and gain G can be seen in equation (2.1):

$$G|_{\text{dB}} = \frac{P_{\text{out}}|_{\text{dB}}}{P_{\text{in}}|_{\text{dB}}} \tag{2.1}$$

The required gain and resulting output power depends on the application. For instance, a cell phone tower's output power is approximately 20 W whereas in commercial wireless local area

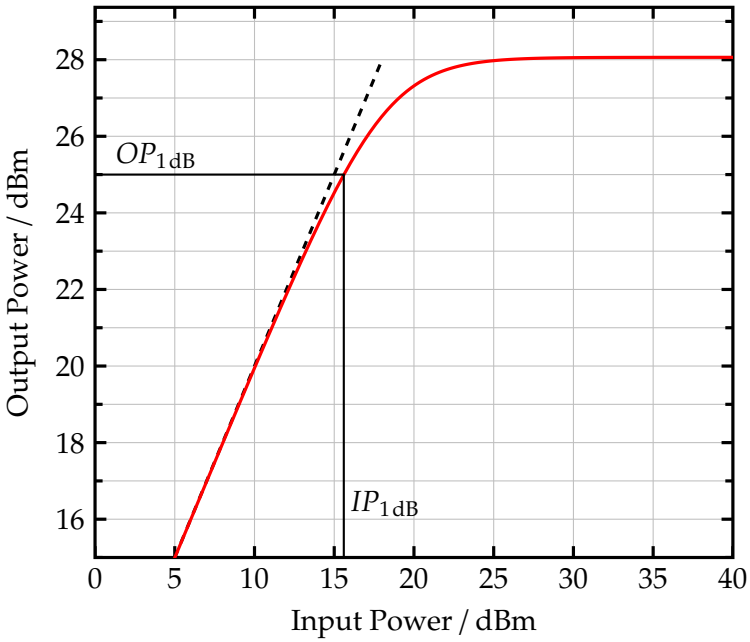


Figure 2.1.: This plot shows typical PA transfer characteristics. The dashed line describes ideal, linear power amplifier characteristics.

network applications output power is approximately 1 W [Kum07, ets07]. For each application, the PA has gain and output power requirements to fulfill. Figure 2.1 shows typical PA input and output power characteristics. $OP_{1\,dB}$ is the PA's input power level where the gain deviates by 1 dB from its ideal gain. $P_{1\,dB}$ is either referred to as input $IP_{1\,dB}$ or output related $OP_{1\,dB}$.

First, the PA's transfer characteristic is quasi linear. In the constant gain region, the PA acts as quasi linear device where an increase in input power is followed by a linear increase in output power [Cri02]. When reaching the PA's saturation region, the gain also saturates and gets nonlinear. The ideal, linear transfer curve is showed as dashed line.

2.1.2. Efficiency

Efficiency is not only for PAs implemented in battery powered devices a critical metric [Daw01]. Also, cell phone towers aim to operate as efficient as possible. One factor is PA power consumption but another factor is also to minimize cooling systems which take care of the PA's dissipated heat [YM08, Kal18]. An efficient PA dissipates less heat thus PA thermal management is improved. The latter also benefits PA's operating in harsh conditions for example aviation or military applications.

An ideal PA would translate the applied supply power directly into input signal amplification, that is output power. However, a real PA introduces energy losses such as power dissipated as heat or, in case of nonlinear operation, losses by creation of undesired frequencies. Therefore, PA efficiency could also be described as the ratio of Direct Current (DC) (supply) power to output power [NI]. The general PA efficiency can be divided into two more exact definitions: drain efficiency and

Power Added Efficiency (PAE). These two metrics are briefly outlined in the following.

Drain efficiency describes the ratio of input DC power to the output signal's RF power:

$$\eta_{\text{drain}} = \frac{P_{\text{RF, Output}}}{P_{\text{DC, Supply}}}. \tag{2.2}$$

Drain efficiency originated from field-effect transistors where DC power is applied to the drain [NI, Mic13]. Drain efficiency is a metric for calculating how much supply (that is DC) power is being translated to output RF power for a single PA. As it can be seen in equation (2.2), drain efficiency only considers RF output power and not RF input power. For PAs with low gain, the drain efficiency metric is therefore not useful. That is why PAE has been introduced.

Shown in equation (2.3), PAE, in contrast to drain efficiency, considers the PA's input RF power. Therefore, PAE is the typical figure of merit for classifying PAs.

$$\eta_{\text{PAE}} = \frac{P_{\text{RF, Output}} - P_{\text{RF, Input}}}{P_{\text{DC, Supply}}} \tag{2.3}$$

Typically, the highest PAE is near the PA's start of compression region [NI]. However, when using high PAPR signals such as Orthogonal Frequency-Division Multiplexing (OFDM), operation near the compression point is often not possible. That is because the PAPR signal's amplitude envelope fluctuates and therefore these signals are prone to drive the PA into nonlinear operation. Therefore, the input power must be limited to prevent any input signals from entering the PA's nonlinear operation region [MMK+06]. Limitation of PA input power is also called back-off and will be discussed in section 2.2.2.1 in more detail.

2.1.3. Classes

A brief overview of amplifiers classes will be given in the following section. For an extensive overview of amplifier classes, consider [Cri06].

In general, PAs can be divided up into four classes: A, AB, B and C [Kal18]. The are also additional classes such as D, E or F but these are mostly derivations of the previously mentioned classes and are not covered here.

Each class is characterized by different PA conduction angles η. η spans from $\eta = 2\pi$ (class A) up to $\eta < \pi$ (class C). Due to the different η, the individual PA classes differ in PA's linearity and efficiency characteristics.

For instance, class A amplifiers tend to exhibits the highest linearity but also show the lowest efficiency. This is in contrast to class C amplifiers. Class C amplifiers exhibit high efficiency but perform poorly in terms of linearity. Choosing between amplifier classes often results in a trade-off between efficiency and linearity [Cri06].

However, in most applications, linearity is a crucial requirement. Therefore, today's PA are often

class A PA as other classes would deteriorate the amplified signal.

2.2. Power Amplifier Linearity

This section introduces the PA linearity. First, PA linearity is defined and reasons for nonlinear PA behavior are addressed. Second, common methods to compensate for the PA nonlinearity are discussed.

2.2.1. Transfer Characteristics

As already mentioned, PAs add certain gain to an input signal applied to it. An ideal PA would always exhibit the same, linear gain over the entire input power range, similar as described in equation (2.1). Furthermore, the phase would be linear over the entire PA input power range. If the input power changes by a certain level, the output power should also change by the respective ratio.

However, a real PA's transfer characteristic exhibits at certain operation points, for example its saturation region, nonlinear behavior. The regions depend on PA class. For instance, class C PA transfer curves do have a cutoff region, class A PA transfer curves do not. For completeness, all PA class transfer characteristics regions are considered. The transfer characteristic can be divided up into four regions that are shown in Figure 2.2 and explained in the following.

First, a cutoff region in which the PA does not amplify the signal as the input signal's power is too low.

Second, a quasi-linear region in which the PA's input and output are in a linear relationship. A change in input power provokes an equal change in output power. In this case, the PA gain is independent of the input power.

Third, a nonlinear region in which the relation between input and output power is not linear anymore. PAs operating close to the saturation region cannot fulfill constant gain characteristics anymore as the output power level will only increase by a smaller percentage, in contrast to the quasi linear region. In this region, the PA exhibits nonlinear behavior and a change in input power does not provoke an equal change in output power and the gain depends on the input power. In other words, the PA output is not a proportional but nonlinear representation of the input signal due to gain compression [Kal18]. The input signal appears in a distorted form at the output. Distortion caused by PAs nonlinear transfer curve is also referred to as nonlinear signal distortion.

The fourth region can also be described as saturation region. In this region, the PA is unable to further amplify the signal. Furthermore, the signal is subject to clipping. Clipping means that higher amplitudes are being flattened out. In extreme cases, a sinusoidal input signal would appear as rectangular signal the output. Clipping significantly increases nonlinear signal distortion.

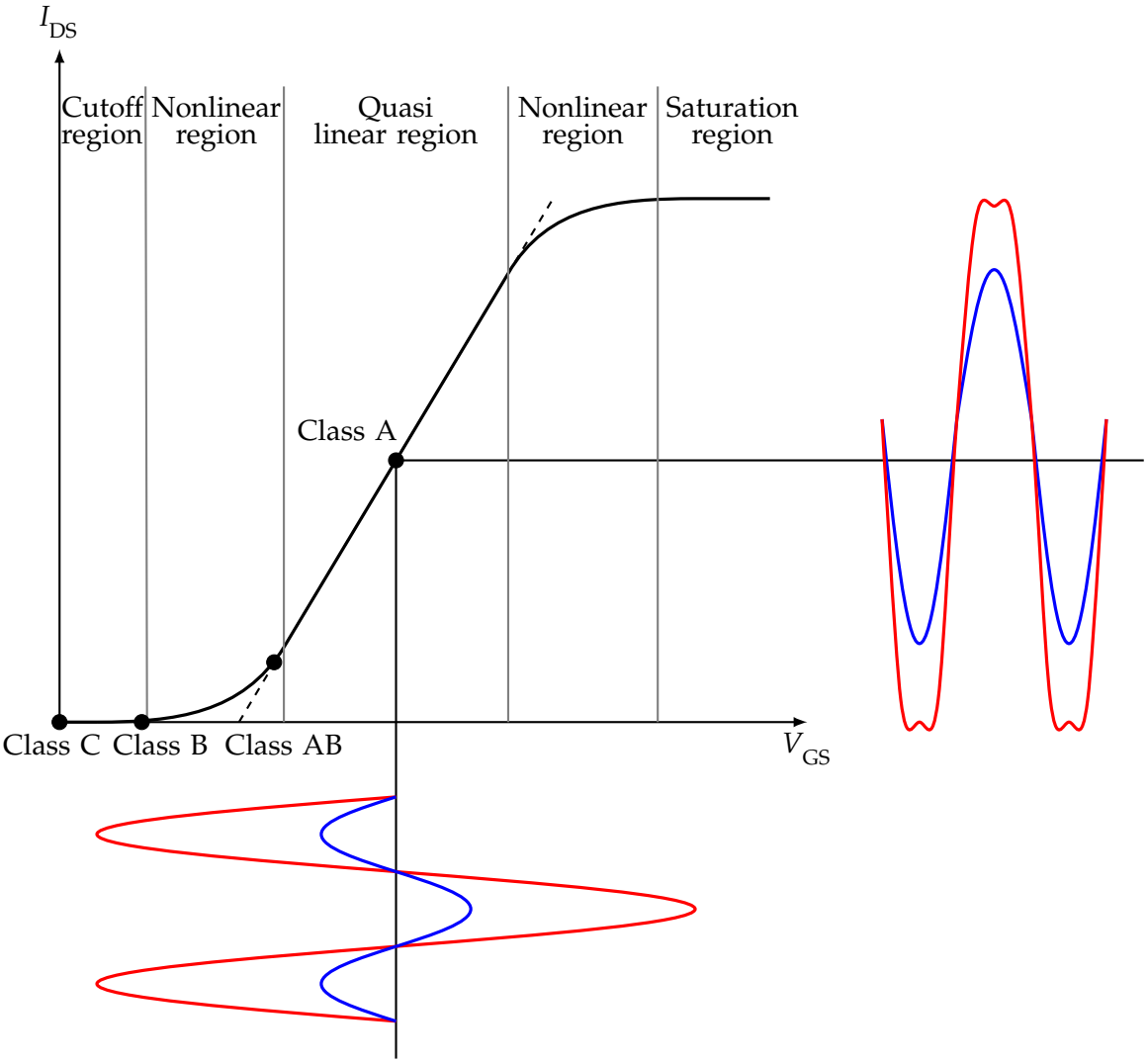


Figure 2.2.: This plot shows typical nonlinear PA transfer characteristics with focus on gain compression. The input signals are shown at the bottom whereas the amplified output signals are shown on the right. Adopted from [Kal18, Cri02].

The creation of undesired frequencies in the PA output spectrum can be described as nonlinear signal distortion [Kat01]. These undesired frequencies consume energy which is actually needed to amplify the desired signal. As already stated, nonlinear signal distortion is caused by PA's nonlinear transfer characteristic [Kat01]. Nonlinear signal distortion worsens a PA's noise floor. Intermodulation Distortion (IMD) products and harmonics appear in the output spectrum and loss in output power can be observed [Kal18].

Consider two tones fed into a PA operating near the previously mentioned 1 dB compression point. Besides the desired two-tone, the PA's frequency output spectrum also shows IMD products of different nonlinearity [Cri02]. Figure 2.3 illustrates the PA's output spectrum, only considering odd-order IMD products as these are close to the desired carrier signal and difficult to filter out.

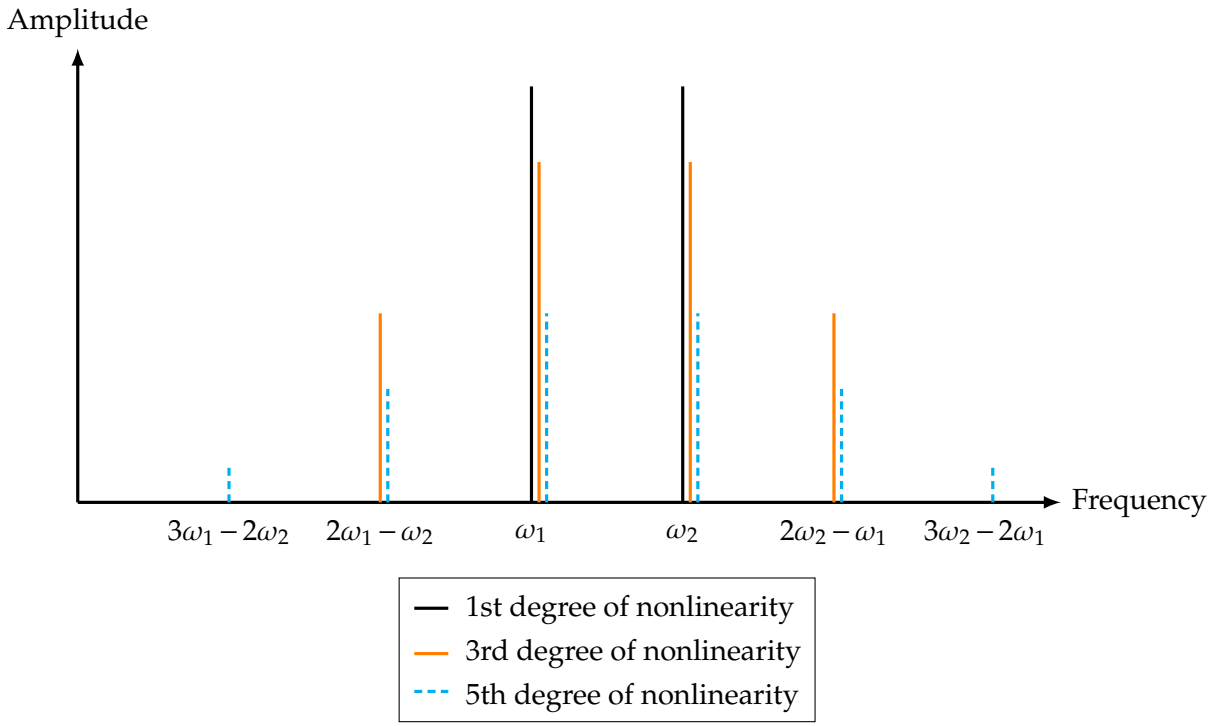


Figure 2.3.: This plot shows a typical power amplifier's output spectrum when applying two tones at the power amplifier's input. Adopted from [Cri02].

To further illustrate nonlinear signal distortion, a single sinusoidal frequency at the input of a generic PA is considered. First, a PA amplification in the linear region, see Figure 2.2, is considered. In Figure 2.4 a), it can be seen that the signal's amplitude is amplified by a certain amount. In the frequency spectrum of both PA input and output only this frequency will be present.

Second, PA amplification in the nonlinear region, see Figure 2.2, is considered. This can be achieved by driving the PA close to saturation. Again, the signal gets amplified but now is subject to distortion. To be more precise, the output signal is subject to clipping. As it can be seen in Figure 2.4 b), clipping causes the output signal's amplitude to be flatted out. Clipping also creates harmonics at the PA's output frequency spectrum [Cri06].

The IMD products are created because the original sine wave gets shaped (or distorted) into a square wave [Kat01]. When applying Fourier transform to an ideal square wave, odd-integer harmonics of the fundamental frequency appear in the spectrum. The detailed derivation of a square wave's Fourier series can be found in [Bog09].

In narrowband communication systems, these IMD products can be easily filtered out. However, when using advanced modulation schemes with multiple carriers such as OFDM, IMD products are near the desired frequencies and are therefore difficult to filter [tB17]. Furthermore, they may overlap with other desired frequencies and therefore distort them [Kat01]. The signal's IMD leaks into adjacent channels and this spectral leakage can violate channel requirements when disturbing other frequency bands. This is also referred to as adjacent channel interference or spectral regrowth [EURa, FAA+15].

When dealing with multiple carrier scenarios, nonlinear signal distortion can result in degrading of SNR, Error Vector Magnitude (EVM) or output power. In other words, the entire communication link gets deteriorated which results in loss of data rate or range. Especially modulation formats define PA linearity requirements [Kal19]. Today's modulation formats feature multiple carrier modulation and therefore strongly rely on a low EVM. Thus, PA linearity is crucial requirement [Vye19].

Besides multiple carrier modulation formats, also modulation bandwidth is a crucial requirement that needs to be considered by PAs. Higher bandwidth allows for the communication system to transfer more data as the signal's symbol rate can be increased. Furthermore, recent modulation formats such as 5G New Radio exhibit high PAPRs which also calls for higher bandwidth [Vye19].

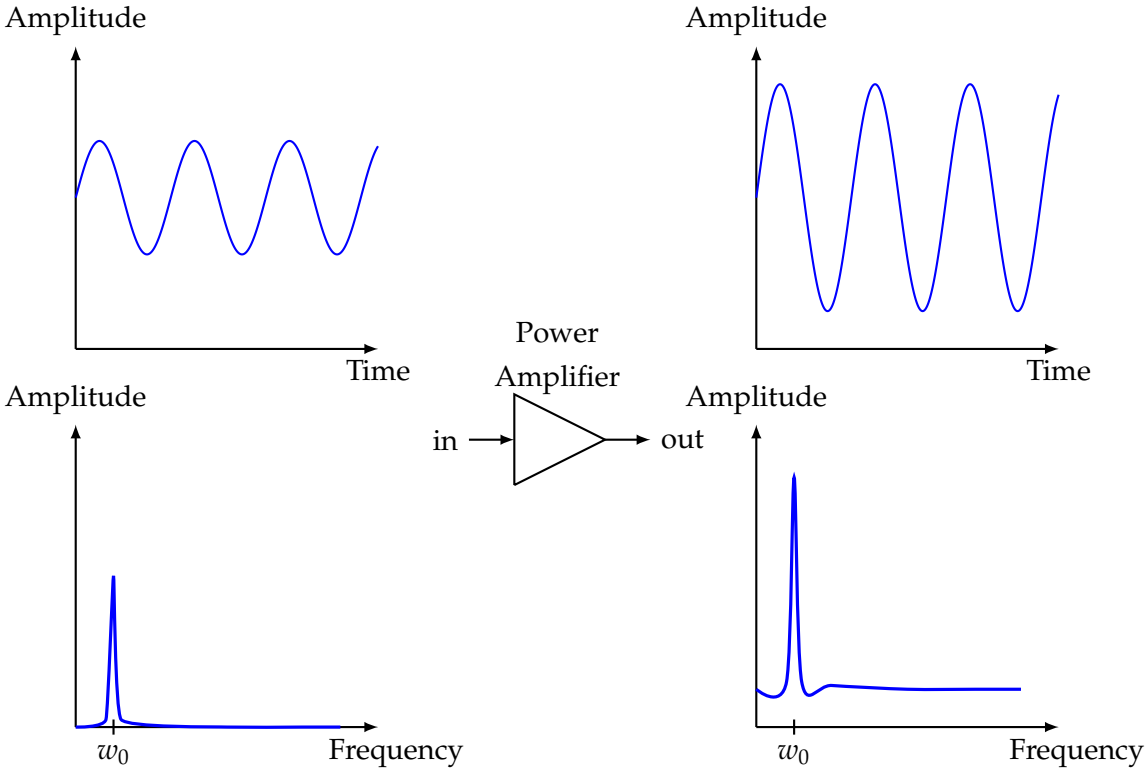
To conclude, for today's modulation formats, linear PA operation is crucial. Especially high bandwidth communication systems such as 5G New Radio rely on linear signal amplification [Cho16]. Nonlinear signal amplification introduces severe losses in terms of bit error rate or spectral regrowth.

Linear amplification is not only essential for the communication channel's capacity itself, but also for improving PA efficiency and output power. In typical base stations, PAs account for approximately 60 % of the total base station's power consumption [EURb]. Therefore, base station PA have to be operated as efficient as possible.

The fundamental goal of linearization methods is to compensate for PA nonlinearities. An ideal linearization method maximizes PA operating range without introducing input signal distortions. The PA operates more efficient and signal distortions are avoided.

The next section discusses multiple linearization methods that aim to ensure linear PA operation while at the same time maximizing channel capacity, PA efficiency and output power.

a) Power amplifier operating in linear region.



b) Power amplifier operating in nonlinear region.

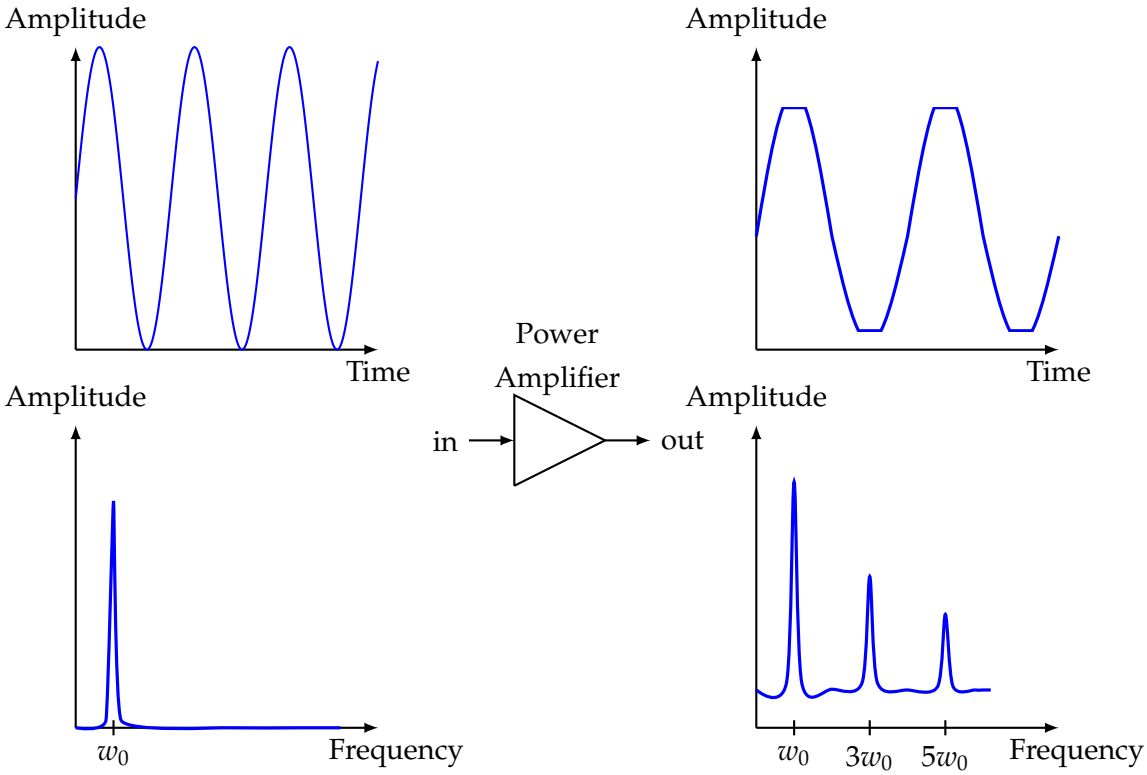


Figure 2.4.: This figure shows the effects of clipping. In a), the input signal's amplitude is still within the power amplifier's linear operation region. In b), the input signal's amplitude is too large and is subject to clipping. Adopted from [Kal18].

2.2.2. Linearization Methods

The following section presents typical and commonly applied PA linearization methods. The section concludes with a detailed explanation of linearization based on DP–this work's predistortion method.

However, the following section discussing linearization methods does not claim for completeness. Popular linearization methods are briefly introduced, but others such as feedback, crest-factor reduction, Cartesian feedback or linear amplification with nonlinear components are also possible but not discussed in this work. For more information on these linearization methods see [SB19, KC06, SE00, MLH+08, GGSC19, MMK+06].

2.2.2.1. Back-Off

Operating a PA in back-off in terms of input power is the most obvious way of ensuring linear PA operation [MMK+06]. Back-off is a passive linearization method that does not require additional or complex hardware and is usually defined as back-off in dB from $P_{1\,\mathrm{dB}}$. Therefore, back-off might not be classified as common linearization method, nevertheless it is considered here for completeness.

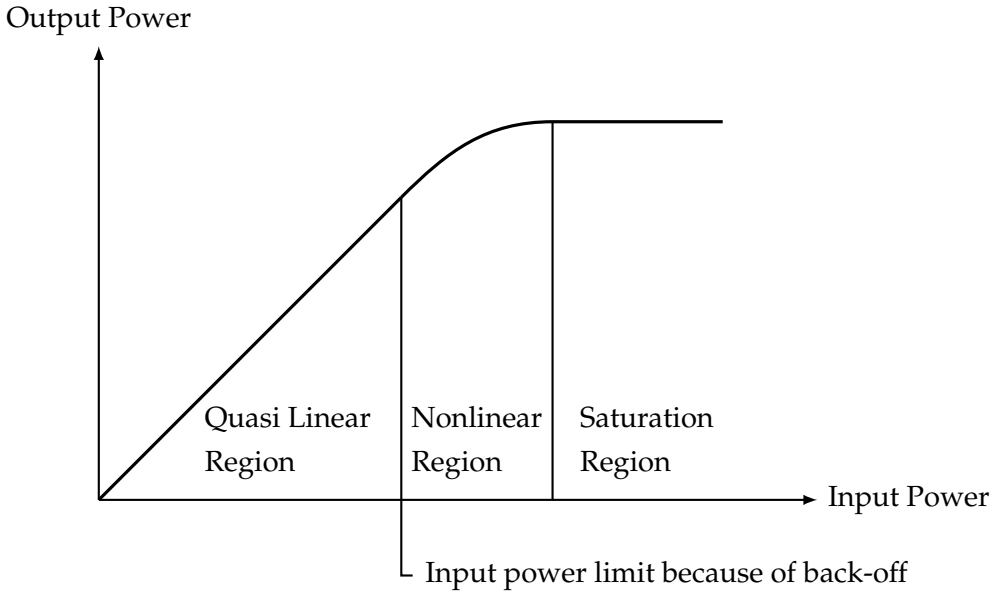


Figure 2.5.: This figure shows the concept of operating a power amplifier in back-off. The input power level is being limited to prevent operation in the power amplifier's nonlinear region.

When operating a PA in back-off, the input signal's power is limited to avoid driving the PA near the saturation region. Figure 2.5 shows the concept of back-off. It can be seen that the PA's operating region is limited to prevent operation in the nonlinear region.

Back-off does not fully utilize the PA's full dynamic range and therefore back-off degenerates the PA's efficiency and imposes range or PAPR limitations on the channel.

A typical a 16-Quadrature (Q)Amplitude Modulation (AM) signal has to be backed-off typically by 3 dB to 3.8 dB from a PA's $P_{1\,dB}$ [Tan18, HST+17].

2.2.2.2. Feedforward

Initially described by [Bla77], the concept of feedforward linearization is to negate distortions and is based on two loops: signal cancellation and error cancellation loop [Cri02]. The basic feedforward block diagram can be seen in Figure 2.6.

First, the nonlinear PA's output power is reduced to the PA's input power level. The difference between input and output signal is now the distortion caused by the PA's nonlinearity [Sta00].

Second, the isolated distortion is being amplified by an auxiliary amplifier, reversed in phase and added to the PA's output [Cey05]. The distortion is now being subtracted from the initial PA output signal resulting in a linear output signal.

Complex analog combining networks are necessary which increases hardware complexity, size and cost [MMK+06, Cri02, Cey05]. Also the two loops have to be matched and are prone to thermal drift. Therefore, feedforward efficiency might deteriorate over time [Key02].

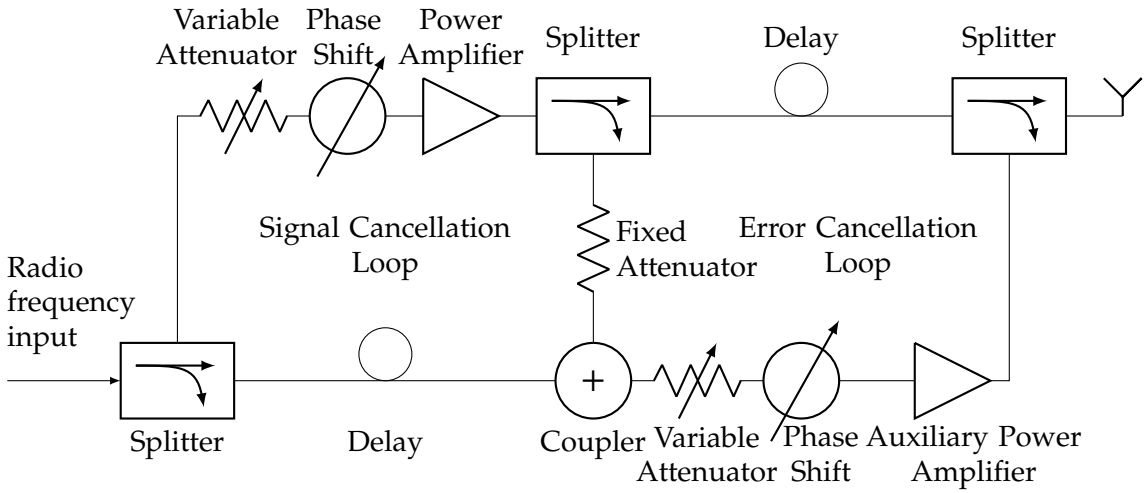


Figure 2.6.: This figure shows the concept of feedforward linearization. On the left, the circuit for signal cancellation can be seen. On the right, the circuit for error cancellation can be seen. Adopted from [Key02, Cey05].

2.2.2.3. Envelope Tracking

Envelope tracking tries to improve PA efficiency by constantly adjusting the PA supply voltage according to the instantaneous input signal's amplitude to ensure operation at maximum efficiency. The adjustment of PA supply voltage is carried out continuously during transmission and thereby at each amplitude level maximum efficiency is achieved. In other words, the PA's supply voltage is synchronous to the instantaneous input signal's envelope.

Envelope tracking can also be used to improve PA linearity and is often applied when using strong nonlinear PAs such as class E. For improving linearity, additional envelope elimination and restoration circuits are necessary [YHTB]. Besides adding additional circuits, envelope tracking can also be combined with other linearization methods such as predistortion [HRHR07].

Figure 2.7 illustrates the basic concept of envelope tracking. In Figure 2.7 a), the PA's supply level is constant. Therefore, at low amplitudes, the PA is in terms of efficiency not fully exploited and part of PA supply power is dissipated as heat.

In Figure 2.7 b), the PA's supply level is continuously adjusted to follow the instantaneous signal's envelope. At low input signal amplitudes, the PA is supplied with less power whereas at high amplitudes the PA is fed with more supply voltage. This results in an increase of PA efficiency and less power is dissipated as heat.

Envelope tracking requires complex hardware to allow for continuous adjustment of PA supply voltage. However, envelope tracking can significantly improve PA efficiency.

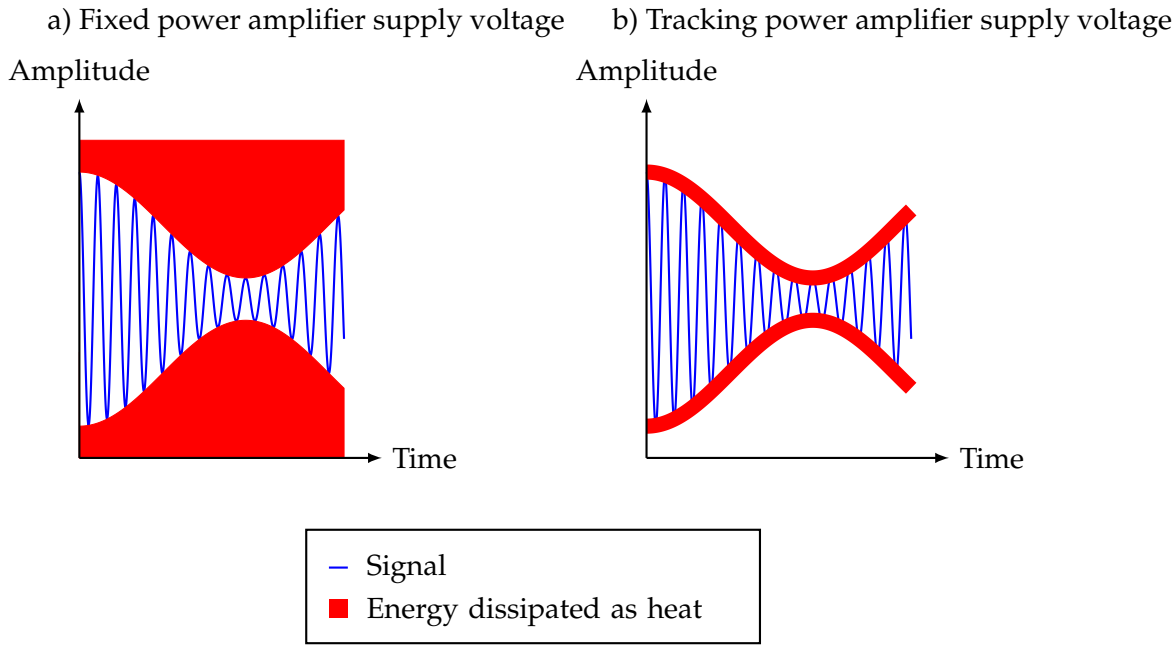


Figure 2.7.: This figure shows concept of power amplifier envelope tracking. In a), no envelope tracking is applied and power amplifier supply voltage is fixed. In b) envelope tracking is applied.

2.3. Distortion

In scope of distortion in general, two methods can be distinguished: post- and predistortion, see Figure 2.8. Both methods will be explained in the following.

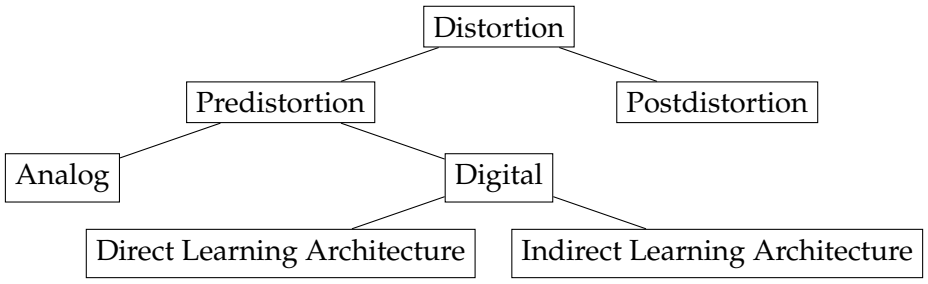


Figure 2.8.: This tree shows different distortion techniques.

2.3.1. Postdistortion

In contrast to predistortion, postdistortion is being applied at the receiver side [TY19]. IMD products are cancelled out by generating IMD products with opposite phase, similar to feedforward linearization [SQ92].

However, this concept requires costly hardware at the receiver side as the postdistortion circuit has to deal with high power signals. Furthermore, complex signal processing is necessary to calculate the postdistortion coefficients. Since receiver often differ in hardware, size and computational power, today postdistortion is mostly replaced by predistortion.

2.3.2. Predistortion

This section introduces the predistortion concept. First, the fundamental idea behind predistortion is presented. Second, the different predistortion types are explained, see Figure 2.8.

In the following it is being focused on predistorting PAs for RF applications. Other PA applications such as in cable distribution systems also apply predistortion techniques such as DP [PK17]. Since cable distribution systems are a closed environment, not all effects mentioned previously have to be taken into account. For example, out-of-band emissions are not as critical as in wireless applications [PK17]. However, it should be noted that besides this work's focus on RF PA applications, also other PA applications benefit from predistortion.

In general, predistortion means to predistort an input signal based on certain parameters such as amplitude difference between input and output signal, apply it to a distorting input and this way achieve an undistorted signal at the output [Key02]. Predistortion can also be described mathematically:

$$F(v_{\text{in}}) = v_{\text{out}} \tag{2.4}$$

where v_{in} is the distorted, nonlinear input signal which gets predistorted by a function F. This results in a linear output v_{out}. Figure 2.9 illustrates the predistortion concept. Predistortion is implemented in the transmitter chain before upconversion. The input signal gets predistorted in such a way that the PA's distortion is compensated for.

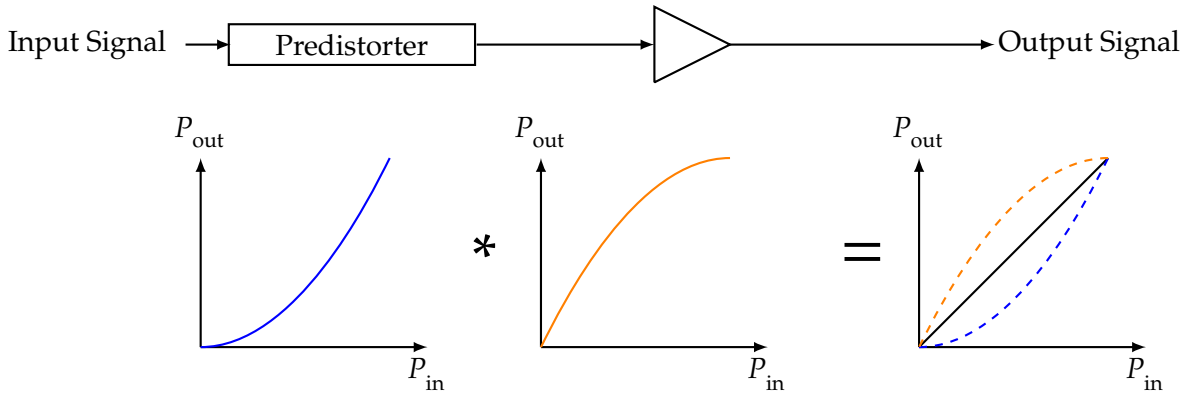


Figure 2.9.: This plot illustrates the predistortion principle. The $*$ describes the convolution of the predistorted signal with the power amplifier's nonlinear transfer characteristics which results (=) in a linearized output signal.

The concept of predistortion is widely used for a range of applications spanning from handheld devices up to satellite communication links [Ken02]. In general, predistortion compares the PA's input and output signal. After comparison, the input signal's required distortion is determined and the predistorted input signal is generated. The predistorted signal is fed into the PA resulting in a linear output signal.

Recently, new ideas for predistortion have emerged. For instance, neural networks can be used for predistortion coefficient calculation [RJ20, WZGY09, YGJ08]. Predistortion based on the neural network approach may be on higher computational cost and be more complex but also the predistortion coefficients can be calculated faster and more efficient.

Furthermore, research in adaptive predistortion using machine learning based on direct learning architectures was done [Bra06]. Another way is to combine the previously mentioned predistortion methods with conservative methods such as feedforward [FFDW15]. There are even predistortion methods for today's widely used multiple-input and multiple-output technology available [LZC+18].

Figure 2.10 illustrates the fundamental goal of predistortion: maximizing PA output power while maintaining low–or ideally no–signal distortion. Without predistortion, the PA's maximum linear output power is limited. Predistortion tries to compensate for PA nonlinearity and therefore allows to maximize the PA's dynamic range. This way, both increased efficiency and reduction of nonlinear effects such as IMD products are possible.

However, predistortion cannot compensate for signal levels which are beyond the PA's operating region, that is saturation region. Signal levels in the saturation region are subject to clipping and cannot be corrected by predistortion.

In the following subsections two kinds of predistortion, analog and digital predistortion, are introduced. As this work examines a reduced-bandwidth DP concept, the concept of DP will be discussed in more detail. For a detailed discussion of Analog Predistortion (AP) for linearization of satellite communication links the reader is encouraged to study [Ufs21].

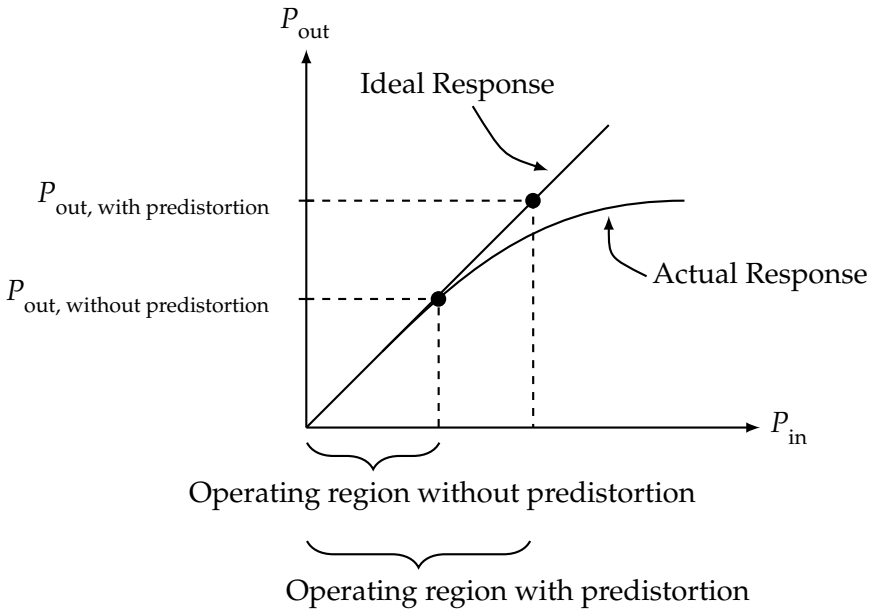


Figure 2.10.: This plot shows the idea of power amplifier predistortion. Adopted from [Fre13].

2.3.2.1. Analog Predistortion

AP relies on analog components to filter out undesired signals. The analog predistorter is designed in such a way that it exhibits the inverse nonlinear transfer curve of the actual PA [Key02]. Before entering the PA, the input signal travels through the analog predistorter. This way the input signal experiences an inverse distortion, with respect to PA distortion characteristics. After the input signal passed through the PA, the reciprocal distortions of the predistorter and the actual PA cancel out and the linear (amplified) signal remains.

AP is low cost, power efficient and does not require complex hardware for coefficient calculation. However, fabrication tolerances may affect the overall effectiveness of AP. Because of the passive approach, AP introduces insertion loss and has limited dynamic range [Cho16]. Therefore, AP cannot outperform DP. However, AP is a promising technique when simple, low-power and small-sized linearization methods are required, for example in satellite communication links [Ufs21].

2.4. Digital Predistortion

The fundamental idea of DP is similar to AP. Instead of analog components, DP manipulates the input signal by using a digital predistorter which acquires input signal and output signals from an ADC. In DP, necessary parameters for applying the predistortion are realized in digital domain. This allows for a more precise predistortion, also size and cost are reduced. Compared to AP, DP is more robust and flexible as fabrication tolerances or PA thermal drift can be easily compensated for, especially if DP is implemented in an adaptive manner. Furthermore, in contrast to AP, DP is unconditionally stable as no additional PAs are required [Cey05].

Figure 2.11 shows the fundamental principle of DP. The digital baseband signal travels through a digital predistorter and is amplified afterwards. At the PA's output stage, the signal is fed to the antenna but also downconverted and sampled by an ADC.

Now two parts of information for predistortion are available: first, the original input signal and second, the PA's output signal. The PA output signal is acquired in the feedback path by an ADC.

As both PA input signal and PA output signal have different propagation time, both signals need to be correctly aligned in time domain to allow for a precise predistortion [MKSK04]. This can be done by either measuring the delay or correlating the two signals.

DP compares the PA input and output signal. For successful DP it is crucial that not only the input signal's bandwidth is being sampled but also the remaining spectrum as this contains crucial information about the IMD products. Typically, the DP bandwidth should be 4 to 5 times higher than the signal bandwidth to obtain sufficient information (that are the IMD products) about the PA nonlinearity [LPST15, DMY13].

Figure 2.12 shows a typical frequency spectrum of an amplified, modulated signal. Moreover, the IMD3 and IMD5 products in frequency domain are shown.

The spectrum can be divided into three parts: signal bandwidth, influence of IMD3 products and influence of IMD5 products. As it can be seen in Figure 2.12, the difference between the original signal and amplified signal mostly depends on the spectral parts outside the signal bandwidth. If DP would only compare the signal bandwidth's and discard the remaining spectral portions of IMD products, DP efficiency would be degenerated.

Based on the acquired PA input and output samples, the DP coefficient estimator calculates predistortion coefficients which are then fed into the predistorter. Finally, the predistorter distorts the input signal based on the provided predistortion coefficients. Signal acquisition in digital domain requires fast ADCs. This is also the first challenge when designing a DP system. The baseband input signal has to be acquired by ADCs which have sufficient sampling rates to respect the Nyquist-Shannon sampling theorem. The second challenge is to process the sampled data, that is to calculate the predistortion coefficients. Especially as the demand for higher bandwidth grows,

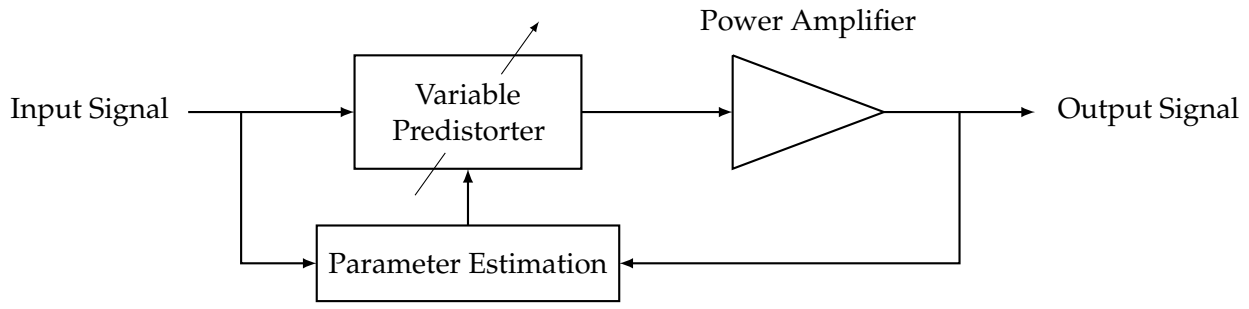


Figure 2.11.: This block diagram shows the fundamental principle of digital predistortion. The input signal is being fed into the variable predistorter unit and the parameter estimation unit. Via a feedback path, the output signal is fed into the parameter estimation unit. For simplicity, analog-to-digital-converters have been neglected.

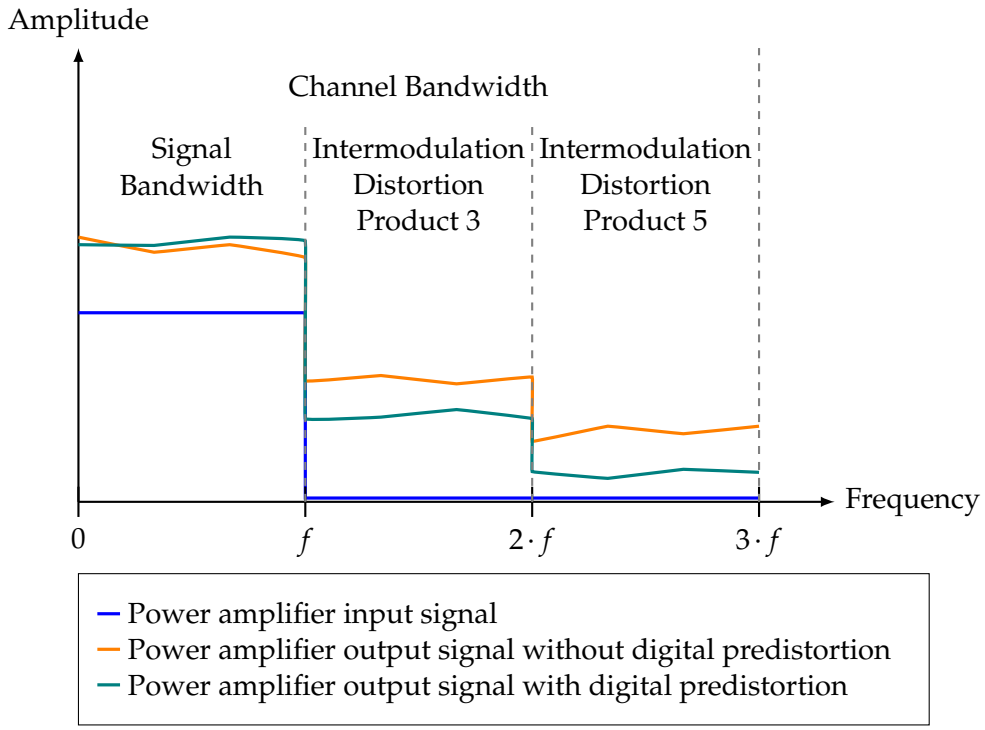


Figure 2.12.: This plot shows the typical frequency spectrum of a power amplifier's input and output baseband signal. The input signal's bandwidth is f. Furthermore, the power amplifier's output spectrum with and without digital predistortion is shown.

DP components have to adopt and ensure high sampling rates and clock speeds to successfully perform DP.

For instance, when performing adaptive DP, predistortion coefficients have to be calculated in real-time. Real-time signal processing poses strict requirements on the signal processing stage. Expensive hardware and computational power are required to process the obtained ADC data and to calculate the predistortion.

However, the previously mentioned challenges are often outweighing other linearization methods due to the DP's precise and efficient predistortion [Ken02]. In general, simple concepts of linearization often relied on feedforward and envelope tracking. Today, communication systems have widely adopted DP to compensate for PA nonlinearities [MMK+06]. Digital predistortion is one of the most promising methods for predistortion and provides a reasonable trade-off between cost and complexity. Therefore, in today's communication units such as cell phones or base stations, predistortion is often used to enhance the overall effectiveness of a communication system [ZTT+99, MMK+06].

As already shown in Figure 2.8, predistortion can be further distinguished into two DP training architectures which will be explained in the following [BMA21]. These training architectures are used to calculate the predistortion coefficients and–besides architecture–differ mainly on how adaptive the predistortion can be performed.

When using the direct learning architecture, the coefficients needed for predistortion are calculated

iteratively in a close-loop and the predistortion can be applied directly. In contrast to the indirect learning architecture, the predistortion can be calculated faster. Therefore, the predistortion unit can react immediately to PA drifts which may affect linearity, for example temperature drift. However, direct learning architecture is costly and complex due to the necessity of using real-time components for first sampling the signal and second for the calculation of the predistortion coefficients. Direct learning architectures are often used in base station PAs such as mobile stations whereas the indirect learning architecture is used in handsets where systems cost, complexity and power consumption are crucial [CMW05].

When using the indirect learning architecture, the DP is calculated in a static, less adaptive and indirect way. At the PA's input and output, a so-called postdistorter calculates coefficients for the predistorter. The predistorter is again connected to the signal source and adapts the signal source's signals according to the information provided by the postdistorter.

In both architectures, the predistortion coefficients can be recalculated for each iteration or Lookup Tables (LUTs) can be used to derive the proper predistortion coefficients [ZTT+99]. The latter reduces computational costs whereas iterative coefficient recalculation allows for a more precise predistortion [LLL13, LFWD12].

2.4.1. Mathematical Background of Predistortion Coefficients

An important factor determining the overall DP efficiency is coefficient calculation. Based on the coefficients, the input signal is being predistorted. The DP benefits from accurate and precise coefficients. The coefficients are based on mathematical PA models. In the following different PA behavior models are discussed.

Since PA behavior modeling is a comprehensive topic, it will be only given a brief overview of most popular PA behavior models. For a detailed outline of PA behavior modeling please consider [Cri02].

The DP coefficients are calculated based on a PA behavioral model. Choosing a suitable PA model greatly depends on the respective applications. There is always a trade-off between modeling accuracy and computational costs [LkY19]. Furthermore, PAs behavioral models are still being researched and different models or derivation of popular behavior models exist [AkYL, LkY19]. In general, two PA behavioral models can be differentiated: memoryless and memory models.

2.4.2. Memoryless Power Amplifier Behavioral Models

Memoryless means that the DP is an instantaneous response that tries to compensate for the PA nonlinearity [Keya]. Memoryless models assume that the current PA output only depends on the momentary PA input [Key02]. Any past input signals are neglected.

The most obvious way for modeling PAs is power series expansion which will be briefly explained in the following. For the following mathematical approach to quantify PA nonlinearity, it is focused

on the PA input v_{input} and output voltage v_{output}. Similar to equation (2.1), the PA's input and output voltage can be described as:

$$v_{\text{output}}(t) = a \cdot v_{\text{input}}(t) \tag{2.5}$$

where a is the PA's voltage gain [Koz19].

According to [Cri02], the PA's output spectrum operating around the 1 dB compression point can be described by a nonlinear behavior model. Each PA's fundamental output tone can be divided into three components: the (desired) linear term, the third-degree nonlinear component and the fifth-degree nonlinear component and can be represented by the following equation:

$$v_{\text{output}}(t) = a_1 v_{\text{input}}(t) + a_2 v_{\text{input}}(t)^2 + a_3 v_{\text{input}}(t)^3 + \dots \ . \tag{2.6}$$

The nonlinear transfer function in equation (2.6) shows a linear gain a_1 but also terms for higher order distortion. Equation (2.6) can also be represented by Figure 2.3.

Memoryless models are usually based on PA amplitude and phase measurements. Based on the acquired transfer curves, coefficients for correcting amplitude and phase are stored in a LUT [Cey05, Cri06].

Memoryless DP algorithms can be described in three steps [Cri06]. First, the input signal is sampled and information about input amplitude is acquired. Second, the necessary phase and amplitude corrections are obtained from the LUT based on the previously obtained input amplitude information. In the third step, phase and amplitude corrections are applied to the input signal.

Various memoryless PA behavioral models are available. Most popular models are Saleh, Taylor series or the Rapp model [Erm01, OML09, JS20].

For an improved DP, models considering PA memory effects would be beneficial because PAs' transfer characteristics can exhibit memory effects. The PA's instantaneous transfer characteristic may depend on signals previously travelled thorough the PA. Furthermore, it is important to consider memory effects if the PA requires linearization [Ale].

2.4.3. Memory Power Amplifier Behavioral Models

In general, memory models are useful for broadband input signal predistortion. For broadband signals, PAs start to introduce memory effects [Keya]. Memory effects are caused by thermal dependencies, frequency-dependent behavior of adjacent PA circuitry and transport delays [VR03, MMK+06]. Furthermore, baseband signal's peak amplitude may jump quasi instantaneous from maximum to zero or never reach zero which can affect PA output gain [Cri02].

In contrast to the previously mentioned power series, the Volterra series also considers the nonlinear system's output depending on the system's input at all time [Koz19]. The Volterra series considers the system's memory effects which can be caused by inductors or capacitors [Sch20].

For effective and precise predistortion all higher order distortion terms should be considered.

Because of the larger number of coefficients, the calculation of the Volterra series comes with high computational costs. Therefore, the Volterra series described above is unfavorable for practical DP implementations [Keya].

In today's broadband memory PA models often simpler Volterra series derivations such as Wiener or Hammerstein are used [MMK+06]. A popular PA model is the so-called memory polynomial behavioral model which is a simplified form of the Volterra series [MMK+06, CRG16]. The memory polynomial behavioral model is a combination of a generalized Hammerstein and Wiener model and was introduced in 2006 by Morgan [MMK+06]. The behavioral model has been successfully implemented in various DP systems [Sch20, JRW18, Mat21a]. However, various other behavioral models such as augmented complexity reduced generalized memory polynomial or Hammerstein based behavioral models are also available but not discussed here [LZCZ14, Ham10].

The memory polynomial behavioral model can be expressed as:

$$y_{\mathrm{MP}}(n) = \sum_{k=0}^{K-1} \sum_{m=0}^{M-1} a_{\mathrm{km}} x(n-m) \cdot |x(n-m)|^k \tag{2.7}$$

where

- n is the time index
- $y(n)$ is the PA's output
- $x(n)$ is the predistorter's output, thus $x(n)$ it can also be said to be the PA's input
- a_{km} are the memory polynomial predistortion coefficients
- M is the PA's memory depth
- K is the PA's degree of nonlinearity

A comprehensive derivation of equation (2.7) can be found in [MMK+06].

Usually, the memory polynomial coefficients are estimated using the least squares algorithm [Mat21c]. Alternative approaches such as a recursive least squares algorithm or an estimation based on separable function are also possible [JW10].

Linearity K and memory depth M parameter depend on the individual PA characteristics and are unique values for each PA. For effective predistortion, the designer should simulate the PA model in advance to determine K and M values which suit the practical PA behavior best. Mathematically, the memory polynomial coefficients can be described as an $K \times M$ matrix. The DP complexity scales with the number of memory polynomial coefficients. It can be seen that DP precision and computational cost results in a trade-off.

After memory polynomial coefficient's estimation, the resulting $K \times M$ matrix can be applied to the predistorter. Based on the memory polynomial coefficients, the predistorter is now able to predistort an arbitrary input signal.

In practice this can be accomplished as follows: First, a so-called training signal is used to characterize the PA transfer function. The training signal should be similar typical PA baseband signals

as based on this training signal the memory polynomial coefficients are estimated. The training signal is fed into the PA and PA input $x(n)$ and output $y(n)$ signals are obtained. Second, suitable K and M parameters are defined and the $K \times M$ matrix is calculated. In the third step, based on the information in $K \times M$, the predistorter predistorts the PA input signal. PA nonlinearity is reduced and quasi-linear PA output is achieved.

3. Predistorting an E-Band Satellite Communication Link

This chapter discusses broadband[1] satellite communication link predistortion. On the basis of the ILH's EIVE project, requirements and important DP parameters are presented.

Besides EIVE, ILH also participates in the Engineers Microwave Theory & Techniques (MTT)-Sat challenge, managed by Institute of Electrical and Electronics Engineers (IEEE) Engineers Microwave Theory & Techniques Society (MTT-S) [MTT21]. The MTT-Sat challenge aims to further advance both RF and microwave hardware for the next generation of satellites. However, the MTT-Sat challenge is not further discussed in this work's scope. For more information on the MTT-Sat challenge see [MGG20, MTT21]. Nevertheless, this work's proposed methods for predistortion satellite communication links could also benefit communication links of satellites developed during the MTT-Sat challenge.

3.1. Exploratory In-Orbit Verification of an E/W-Band Satellite Communication Link

ILH's EIVE project tries to establish a communication link at E-Band frequencies ranging from 71 GHz to 76 GHz between a Low Earth Orbit (LEO) satellite and a ground station [Sch21]. The satellite communication link's RF bandwidth is 5 GHz. The mission's goal is to observe various weather conditions and their impact on the communication link. Furthermore, a high-resolution video camera's real-time data should be transmitted to earth at data rates of 5 Gbit/s [SCM+20]. To satisfy this data rate, high order modulation schemes are required.

EIVE could benefit from DP in several ways which will be discussed in the following.

As already said, PAs often exhibit a trade-off between cost and linear amplification bandwidth. Therefore, DP would relax the requirement for a costly and highly linear broadband PA. Due to the bandwidth increase, EIVE's PA could be operated more efficient and therefore EIVE's total power consumption could be reduced.

[1] The terms 'broadband' and 'narrowband' are not coherently defined in literature. It strongly depends on the application if a bandwidth can be defined as broadband or narrowband. However, in this thesis the term broadband describes bandwidths that are higher than the usual bandwidths used in satellite communications. Usually, bandwidths up to approximately 500 MHz located in the S-Band are used for satellite communications [Con21]. In the following, bandwidths higher than 500 MHz are described as broadband. Bandwidths smaller than 500 MHz are referred to as narrowband.

The EIVE satellite is located in the LEO and therefore does not orbit at the same speed as earth. That means, EIVE is not stationary above a single station on earth's surface. Therefore, a single ground station on earth can communicate with EIVE only for a few minutes per day. That is because LEO satellites have a flyby duration of several minutes per day, depending on the satellite's height.

For instance, the International Space Station–a typical LEO space station–has an approximate height of 400 km above earth's surface and a flyby time of approximate four minutes, depending on what location on earth is considered [Pea21, Kee].

EIVE's telemetry and telecommand data is communicated between multiple ground stations around the world via a S-Band link [Sch21]. However, the E-Band downlink receiver, which allows for high-speed data transmission, is only available in Stuttgart [Sch21]. Therefore, E-Band links between the EIVE satellite and ILH's ground station in Stuttgart can only be established for few minutes a day. Due to the limited time window for E-Band downlink transmissions, efficient and high-data rate transmissions are crucial. The high-resolution video camera accumulates lots of data that has to be sent to earth, at best via a high-data rate communication link. DP would allow for an increase in data rate as usable PA bandwidth would be increased.

EIVE aims to fully utilize the frequency band from 71 GHz to 76 GHz. Operation only within the allocated frequency band is crucial and spectral leakage has to be reduced. DP improves PA linearity and therefore leakage in adjacent frequency bands is decreased.

The previous examples showed that DP could be a promising tool for improving the EIVE downlink to earth. In contrast to typical DP solutions implemented in cell phones or base stations, DP for satellite applications differs in requirements. These requirements are discussed in the following sections.

3.2. Requirements for E-Band Predistortion

This section introduces critical design parameters when considering DP for a satellite applications. The following enumeration does not claim for completeness, rather the most import design parameters are outlined.

3.2.1. Scattering Parameters

As already mentioned in section 2.4, DP is usually implemented into an already exiting transmission chain. Therefore, the DP has to be properly included into the transmission chain by means of matching, signaling and power limitations.

Similar to Figure 2.11, DP systems tap the PA input and output signal and therefore influence the baseband signal traveling through the PA. To reduce any signal degeneration, proper matching is required. Otherwise, the DP itself may disturb the original signal. Typical RF systems are matched to 50 Ω which is also the case in EIVE's transmission chain.

When considering signal paths, it is important to distinguish between differential and single

ended signaling. Differential signaling is impervious to electromagnetic interference but requires more hardware as the signal path is executed in two paths. Single-ended signaling is simpler to implement as less signal paths are required but it is more prone to outside interference. As EIVE relies on differential In-Quadrature (I)Q-modulation, the DP system needs to feature differential signalling, see Figure 3.1.

Another DP parameter are power constraints. The DP's ADCs sample PA input and output signals.

At the PA input signal path, power is often not a critical issue as the signal is not amplified yet. Nevertheless, the PA input signal should be strong enough to get acquired by the ADC but at the same time it should not exceed the ADC's input power.

At the PA output signal path, the amplified signal is forwarded to the antenna and also to the DP unit. The latter one might cause power limitation issues as PA output power can exceed the ADC's maximum ratings. Often attenuators inserted between PA output path and DP have to be used to prevent the ADC's input ports from being driven above their maximum ratings.

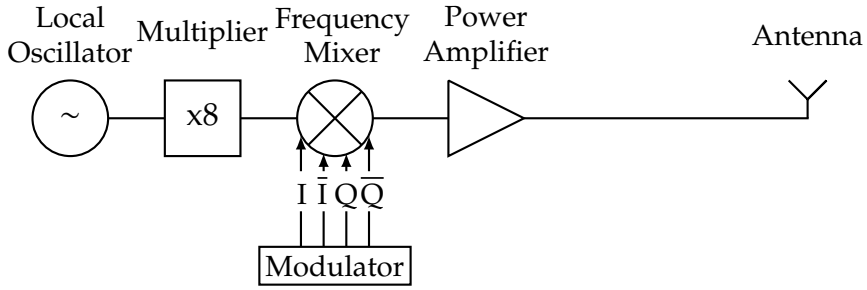


Figure 3.1.: This plot shows a simplified block diagram of EIVE's transmit chain. The source signal gets multiplied, frequency mixed and data is modulated. The modulated signal is then amplified and fed into the antenna. Adopted from [DSK19, HST+17].

3.2.2. Temperature

In space applications, environment and operating temperature are crucial parameters for satellite components. First, due to vacuum, heat dissipation can often only be realized through passive absorbers. Second, satellites are exposed to varying environment temperatures because of eclipse and sun phases.

EIVE features film heaters for heating critical components [Sch21]. EIVE's cooling is passive. Hence, the DP system must satisfy the operating temperature conditions and it should not require active cooling. Furthermore, the DP system should not dissipate too much heat as this may cause other components to overheat.

3.2.3. Cost

In hardware development, costs are often strongly depended on the chosen components. Therefore, designers often try to choose COTS hardware components. COTS components are cheap, tested

and available in large amounts.

Satellites are not attractive for mass markets and therefore cannot rely on typical COTS components. Furthermore, COTS components are primarily developed and tested for on-earth applications.

However, COTS components implemented in small satellites gained popularity over the last years [Col15, Nik19]. The primary reason for COTS components in space application are costs. For instance, when replacing proprietary space components by COTS, the designer can save up to 90 % in costs [FL20]. The secondary reason is that some proprietary space components are not yet developed or available and therefore the designer chooses COTS components. Using COTS components for a satellite applications may sound promising, but they need to be tested extensively beforehand to be approved for space applications.

Regarding the EIVE mission, the designer has to ensure that all implemented components are suitable for space applications in the scope of EIVE. Ideally, EIVE is based on low-cost COTS components for economic reasons, otherwise EIVE would obviously result in higher prices. Furthermore, specific, non-COTS components may be not always available.

Another issue might be the required DP sampling bandwidth. To sample a bandwidth of 2.5 GHz, advanced ADCs are required. Optimally, these ADCs are low-cost because in total four ADCs are necessary, see Figure 3.3 However, up to this work's date, no low-cost ADCs are available that facilitate sampling the previously mentioned 2.5 GHz bandwidth.

3.2.4. Power Consumption

Satellites require sophisticated power management because they solely rely on solar panels to receive power. The solar panels can only provide power during sun phases, during eclipse phases the satellite is fed by its battery. Furthermore, it must be ensured that the solar panels and the battery can deliver enough power for proper satellite operation.

EIVE features two solar panels and a lithium ion battery to provide power. A power management system allocates appropriate power levels to each subsystem. Furthermore, individual subsystems can be shut off to preserve power [Sch21].

A possible DP system for EIVE requires operation only for several minutes a day. Therefore, a standby or shut off mode would be beneficial to preserver power. Due to limited power resources, a DP system for EIVE has to operate as power efficient as possible.

3.2.5. Bandwidth

In this thesis, only EIVE's E-Band downlink's bandwidth is of interest. EIVE has a RF bandwidth of 5 GHz and a baseband bandwidth of 2.5 GHz. Predistortion usually takes place in the baseband, therefore only EIVE's baseband bandwidth is relevant for predistortion.

In contrast to conventional communication systems, 2.5 GHz is an exceptional broadband system. Especially predistortion of such a broadband system requires a sophisticated DP system. The DP

unit has to facilitate predistortion of a 2.5 GHz bandwidth, followed by processing the acquired data and thereafter computation of DP coefficients. Up to this work's date, no other study was found which considered predistorting a 2.5 GHz bandwidth.

3.2.6. Predistortion

Besides the previously mentioned linearization methods in section 2.2.2, Modulator-demodulators (Modems) could also be used to achieve channel linearization. Modems, placed on both ends of the communication link, could exchange information about link quality such as BER and settle on equalization parameters or modulation schemes [ZC93, Hra19]. Furthermore, Modems consider the complete up- and downconversion chain and are therefore able to effectively compensate for various channel impairments. This renders Modems to powerful tools for channel linearization. However, Modem's are complex and expensive. For EIVE, simple, low-cost but effective methods should be used to achieve channel linearization. Therefore, DP was the chosen for improving EIVE's downlink.

The motivation for predistorting EIVE's downlink is obvious: EIVE has only a limited flyby window, therefore EIVE's downlink to earth has to be as efficient as possible.

Figure 3.2 shows an idea of how DP could be implemented into EIVE's E-Band transmission link. After signal amplification, the signal is divided into two paths: one path to the antenna and the other path to the frequency mixer. The frequency mixer downconverts the output signal to lower frequencies to relieve the need for high sampling rate DP ADCs. The DP unit compares the acquired ADC signal with the one provided by the modulator and based on the differences calculates

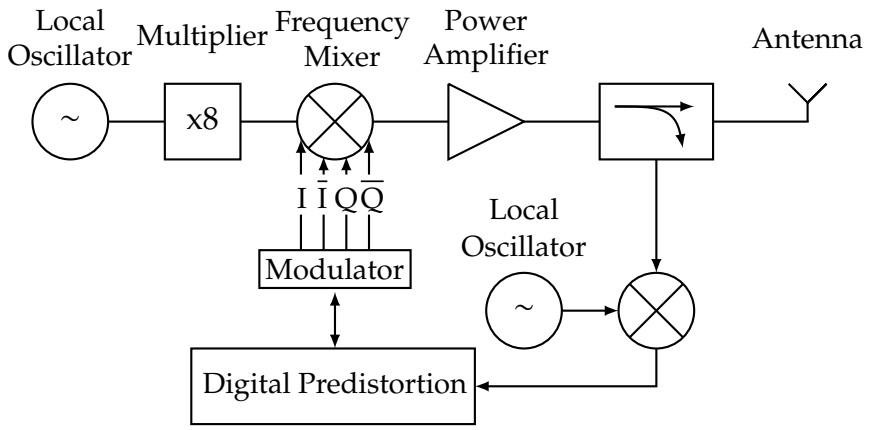


Figure 3.2.: This plot shows a simplified block diagram of EIVE's transmit chain. The source signal gets multiplied, frequency mixed and data is modulated. The actual data before amplification is also forwarded to the digital predistortion unit. The modulated signal is then amplified and a power splitter divides the signal into two paths. One path forwards the signal to the antenna and the other path forwards the signal to a frequency mixer. The frequency mixer downconverts the signal and afterwards the signal enters the digital predistortion unit.

predistortion coefficients. Based on the predistortion coefficients, the modulator predistorts the baseband signal entering the frequency mixer.

However, DP does not only require additional RF hardware on receiver side but also digital components.

DP is based on mathematical operations for obtaining the predistortion coefficients. But at the same time computational costs have to be kept low. Therefore, an effective DP algorithm is needed which does not require a complex processing unit. Complex algorithms would require powerful processing units that may consume lots of the satellite's scarce power resources.

Nevertheless, the DP unit should be capable to perform fast and iterative cycles of DP. A DP cycle describes the complete DP process, from obtaining signals to eventually predistorting the input signal. Iterative DP is useful when the PA's outside influences such as environmental temperature changes. A change in temperature may alter the PA's transfer characteristic and predistortion might be necessary several times during transmission to adapt to new operating conditions. However, iterative DP requires components which have sufficient sampling and processing speed.

It can be seen that there is a trade-off between computational speed and energy efficiency. The designer has to carefully select a suitable DP algorithm and hardware which benefits EIVE's downlink and at the same time satisfies all requirements.

Computation of predistortion coefficients could also be performed on earth, similar as proposed by [Str19]. This would relieve the requirement of high computational power on the satellite. A known signal, also called pilot signal, is exchanged between transmitter and receiver. Based on the received pilot signal, the receiver calculates predistortion coefficients for the transmitter which are then send back to the transmitter. This pilot signals could be transmitted via a simple modulation format so that the pilot signals are impervious to the channel's distortion effects.

3.3. Reduced-Bandwidth Sampling System

This chapter introduces a concept for predistortion of broadband satellite links. First, the sampling system, the OR, is introduced and specifications and characteristics are presented. Second, the fundamental concept of predistorting broadband E-Band signals is introduced.

3.3.1. 2.5 GHz Observation Receiver

The 2.5 GHz OR was developed by Heiko Strohmeier as part of a DP system for satellite communications [Str19].

The goal of the OR was to sample signals of up to 5 GHz bandwidth using low-cost COTS components. However, in this study only signal bandwidths up to 2.5 GHz were considered. As low-cost ADCs do not feature the required sample rates, a concept of sampling signal bandwidth in parts of individual, reduced-bandwidth frequency windows was introduced. This concept is also referred to DP with reduced observational bandwidth [dS14, Bra08]. The OR does not feature signal

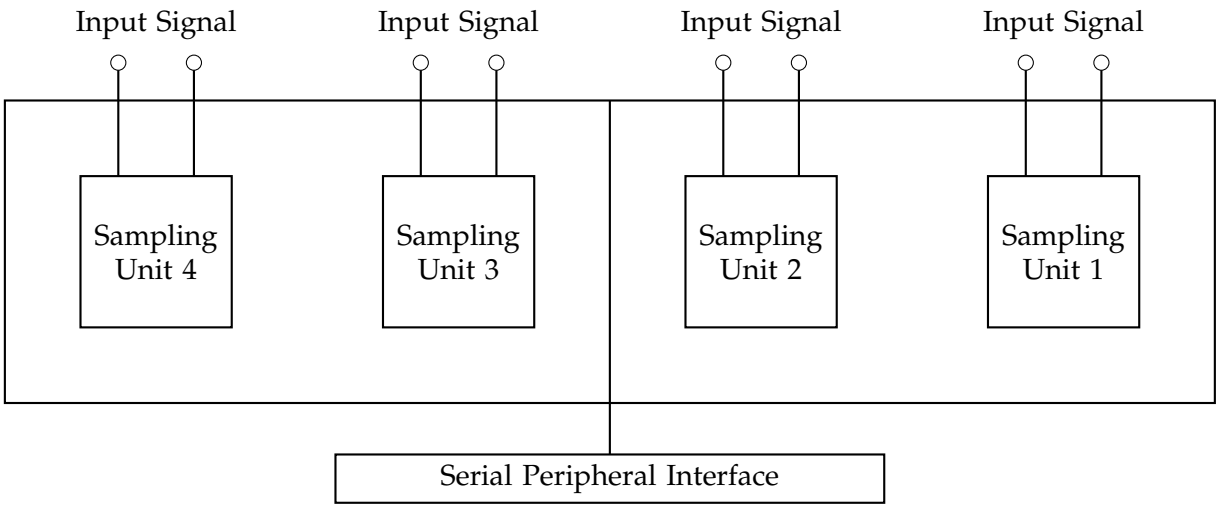


Figure 3.3.: Block diagram of the observation receiver. The observation receiver has four identical sampling units which feature differential ports.

processing components in order to perform predistortion. The obtained OR data has to be further processed by a computer.

Figure 3.3 shows the OR's block diagram. For a photo of the OR Printed Circuit Board (PCB), see appendix A.1.

As the OR was a special development for the ILH's satellite projects, all OR ports are differential and are implemented in form of SubMiniature version A connectors. Each OR components can be controlled individually by a computer as they feature the Serial Peripheral Interface (SPI) bus.

Whereas the ADCs only support 3-wire SPI–also called bidirectional SPI–the rest of the components such as Variable Gain Amplifier (VGA) or Voltage-Controlled Oscillator (VCO) feature the traditional 4-wire SPI mode. The OR requires 5 V DC supply voltage and the theoretically calculated power consumption is stated with 2617 mA [Str19].

The OR was developed for DP applications in particular and therefore features two main branches: one branch for sampling the PA's input and another branch for sampling the PA's output. The two identical main input branches are again split into respective I- and Q-paths.

When considering a single sampling unit like shown in Figure 3.4, the input signal can take two paths, depending on the state of the RF switches. The RF switches can be used to either downconvert the signal or to apply the signal directly to the ADC. Either way, the signal is filtered by a low-pass antialiasing filter and amplified by a VGA before entering the ADC.

When the input signal travels through the downconverting chain, a high-pass filter prevents low frequencies from entering the frequency mixer. The signal enters the frequency mixer and is mixed with the VCO signal. When considering typical frequency mixer terminology, the VCO could also be described as sweeping or tunable Local Oscillator (LO). The mixing product of VCO frequency and input signal leaves the downconverting chain and is low-pass filtered and amplified before entering the ADC.

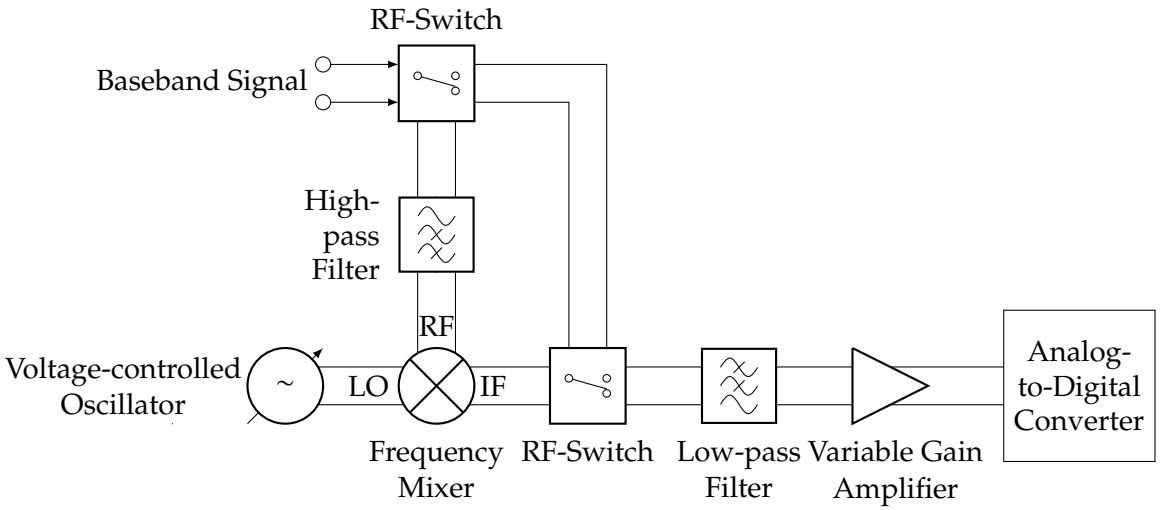


Figure 3.4.: Circuit of the observation receiver's sampling unit. The observation receiver features four identical sampling units. For simplicity, only one sampling unit is shown. RF, LO and IF annotate the typical frequency mixer's input and output ports.

3.3.2. Concept

The fundamental idea of sampling a broadband input signal in parts of individual, narrowband frequency windows will be explained in the following. The input signal is bandpass filtered and fed into a frequency mixer's RF port. The bandpass filter is required to reduce higher order harmonics which are generated by the frequency mixer.

The frequency mixer's LO port is driven by a VCO and thus the frequency mixer downconverts the input signal to an output signal Intermediate Frequency (IF). The VCO is tuned in such a way, that the resulting IF frequency complies the ADC's sampling bandwidth while also complying with the Nyquist-Shannon sampling theorem.

Before entering the ADC, the signal is filtered by an antialiasing filter to reduce frequencies above the Nyquist region.

The ADC samples the signal and afterwards the VCO is tuned again in such a way that the next input signal's spectral part (that is the next frequency window) can be obtained by the ADC. Depending on input signal and ADC bandwidth, this loop is performed several times until the entire input signal's spectrum is digitized.

The OR's ADCs feature sampling rates of 500 MS/s which, according to Nyquist, facilitates sampling of a 250 MHz bandwidth [AD11]. The ADC can acquire a maximum of 16384 samples. The first five frequency windows with their individual bandwidth and VCO frequency are shown in Table 3.1.

In case of the OR, 17 frequency windows have to be sampled to acquire a spectrum of 2.5 GHz. To abate any undesired effects at the ADC's lower and upper bandwidth limits, each frequency window overlaps the adjacent frequency window, see Figure 3.5. Furthermore, the low-pass filter

Frequency window	Frequency VCO	Frequency window start	Frequency window end
0	–	0 MHz	200 MHz
1	150 MHz	200 MHz	350 MHz
2	300 MHz	350 MHz	500 MHz
3	450 MHz	500 MHz	650 MHz
4	600 MHz	650 MHz	800 MHz
...	...	...	...

Table 3.1.: The table shows the first five frequency windows of the observation receiver. Adopted from [Str19].

in front of the ADC has a cutoff frequency of approximately 200 MHz. The filtering behavior of the low-pass filter is illustrated by the blue triangle at the end of every frequency window.

Because of the low-pass filter, each frequency window's nominal bandwidth is reduced to 200 MHz. The resulting overlap between adjacent frequency windows is therefore 50 MHz to compensate for any irregular frequencies at frequency window start and end. Overlapping frequency windows allow for smooth and continuous sampling.

Basically, the idea of sampling a broadband spectrum by dividing it in narrowband frequency windows is also applied in spectrum analyzers, see [Agi06]. Obviously, spectrum analyzers do not rely entirely on low-cost COTS components and have advanced circuitry that allows sampling a wider input signal bandwidth. Nevertheless, the fundamental principle of sampling an input signal in parts is the same.

This principle has already been implemented based on COTS components and was successfully tested with smaller bandwidths of 150 MHz in other studies, see [Bra08,dS14]. Sampling broadband bandwidths with low-cost components and performing predistortion is promising for broadband satellite communication links. Therefore, the ILH developed the OR.

For a first proof-of-concept, comprehensive simulations regarding matching, design and the sampling frequency windows in parts have been performed, see [Str19]. As the simulation results were promising, the OR was fabricated. However, comprehensive measurements with respect to a possible implementation in satellite applications have not been conducted.

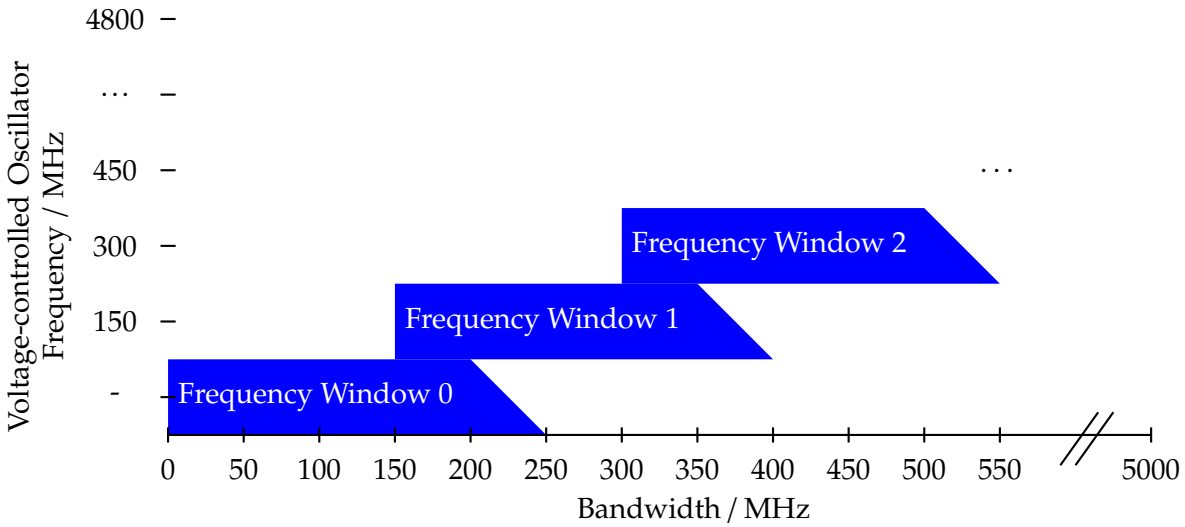


Figure 3.5.: The first three observation receiver's frequency windows are illustrated. The x-axis depicts the bandwidth to be sampled. The discrete-valued y-axis shows the required voltage-controlled oscillator frequency for the respective frequency window. Adopted from [Str19].

4. Measurements and Evaluation

This chapter introduces the performed measurements in order to evaluate a possible application of the OR in satellite communication systems. First, fundamental measurement design and setup are introduced. Based on the mentioned requirements of satellite communication systems, measurements were performed to allow for a first conclusion if the OR is suitable for satellite applications. Challenges and insights during measurements are outlined followed by a short evaluation and discussion of the results.

In general, the measurements can be described in a step-by-step process divided in three parts: First, the initial ramp up of the OR is described. Fundamental hardware setup, challenges and physical layer changes are introduced. Second, narrowband 250 MHz signal acquisition of only a single path, that is a single ADC, is performed. Finally, the OR's potential is fully exploited by acquiring broadband signals based on the concept of frequency windows.

The measurement setup differs between the three measurement parts. Therefore, in each section's beginning, the measurement setup and OR's operation point will be briefly explained.

As already mentioned, DP could not be achieved. Nevertheless, the DP measurement and possible causes for the failed DP will be outlined.

4.1. Initial Operation

During OR's first ramp up it was ensured that all parameters such as power consumption or individual component's voltage levels where within the expected range. The fundamental goal of the first measurements was to allow for reliable SPI communication with all OR components. Furthermore, typical component configuration such as reading out the ADC or configuring VGA gain should be possible.

When the OR was first developed, it was aimed to control the OR components using a Raspberry Pi. Hence, the OR features a 40 pin connector. OR's 40 pin connector was particularly designed for a direct connection to a Raspberry Pi's 40 pin connector. Later on, it was found out that the Raspberry Pi does not support mixed SPI modes within a single SPI environment. Both 3- and 4-wire SPI operations at the same time are not possible using a Raspberry Pi. Therefore, a STM32 Nucleo Board by STMicroelectronics (Nucleo) has been used as it supports simultaneous 3- and 4-wire SPI communication.

However, during this work it was decided to replace the Nucleo board by a Raspberry Pi. The

main reasons for the roll back to the Raspberry Pi are explained in the following.

The primary reason for replacing the Nucleo by a Raspberry Pi is debugging. The code for the Nucleo is written in a proprietary Nucleo integrated development environment in C/C++. The program code is then transferred via universal serial bus to the Nucleo. The transferred program code has to be compiled and afterwards the program can be executed on the Nucleo. It is important to note that once the program execution started, the user cannot easily interact with the Nucleo.

For example, interactive user input for controlling programming execution is difficult as the program is executed on the Nucleo. To observe and debug, especially line-by-line, the programmer has to use the universal asynchronous receiver transmitter protocol and debug output has to be implemented in the program code. Furthermore, it is difficult to connect peripheral devices such as a display or keyboard to the Nucleo.

Writing code on Raspberry Pi allows for advanced debugging and controlled program execution. The Raspberry Pi itself can be controlled by typical peripherals like keyboard and display. Moreover, Raspberry Pi also supports Secure Shell (SSH). SSH allows for headless operation via network. Furthermore, SSH can be used to interactively write, execute and debug code on the Raspberry Pi remotely on the user's local machine.

The second reason for replacing the Nucleo by a Raspberry Pi is portability. The Nucleo is not as portable as a Raspberry Pi. Future OR versions might require a change in hardware or more powerful hardware is needed to calculate DP coefficients. A Nucleo can only be upgraded to another, for example more powerful Nucleo board. Between different versions of Nucleo board, hardware and size can differ. Therefore, it has to be ensured that the replacement satisfies all hardware requirements.

The Raspberry Pi is a ready-to-use, low-cost product and does not require proprietary software. The latter is because the Raspberry Pi is founded on the open source approach. Therefore, almost all popular programming languages such as Java or Python can be used for programming the Raspberry Pi. Furthermore, the Raspberry Pi is portable because Linux machines are widely available and an upgrade to a more powerful Raspberry Pi or other Linux-based machine is possible.

Because of the advantages mentioned above, a Raspberry Pi was chosen to control the OR. However, even today's most recent Raspberry Pi's still do not support mixed SPI modes within a single SPI environment. Therefore, a circuit between OR and Raspberry Pi was developed which allows the Raspberry Pi to operate within a mixed SPI environment.

Basically, the circuit is made of pull-down resistors and commercial transistors. The transistors are controlled by the Raspberry Pi's General Purpose Input/Output (GPIO) pins. When 3-wire SPI communication is required, the transistors shorten the Master Input, Slave Output (MISO) and Master Output, Slave Input (MOSI) lines temporarily to allow for read-back of bits. The circuit to facilitate 3- and 4-wire SPI communication can be found in appendix B.2. Depending on which type of SPI operation–3-wire or 4-wire–the Raspberry Pi configures the respective transistors and therefore switches between different SPI environments during SPI communication. As it will be

seen later, this comes with a significant trade-off in SPI speed. However, for fundamental OR operation the speed was considered to be secondary.

For each component, Python classes were created. Python classes feature all relevant functions for typical OR operation. The OR's ADCs, VGAs and VCOs communicate via Raspberry Pi's SPI Interface. The RF switches can be controlled by using logic voltage levels. This was realized by using the Raspberry Pi's GPIO pins. After each SPI component was implemented in Python, a first communication test was done and all OR components could be reached and controlled successfully.

After several experiments, the Raspberry Pi's SPI clock was set to a frequency of 1953 kHz which was the maximum achievable SPI frequency. Higher frequencies lead to signal distortion. The reason for this limited SPI clock frequency are long SPI tracks on the PCB which cause, at higher SPI clock frequencies, crosstalk between the SPI clock and data line. Furthermore, the connection between Raspberry Pi and OR is realized in form of COTS jumper cables which also make higher SPI clock frequencies challenging. As already said, the primary goal was reliable communication with the OR's components and therefore SPI speed was considered secondary. However, in later sections SPI speed and ADC read-out duration will be discussed comprehensively.

It was noted that when powering the OR, the ADCs do not always power up being ready to sample. Especially if the OR was disconnected from power for longer time and is powered up, the ADCs go into fail mode and are not ready to sample. To get the ADCs ready to sample, the OR has to be power cycled. The reason for this might be that the OR's clock (that is the 500 MHz oscillator) provides an incorrect clock frequency for a short period of time after being powered up. As the ADCs require a correct clock right after booting this might cause the failure state. After power cycling the OR, the clock of the OR is already warmed up and therefore can now provide a precise clock frequency and the ADCs boot in ready state.

Throughout the measurements, the VGAs were set to a fixed gain of 3 dB to compensate for losses in the matching networks, RF switches and signal paths. The VGAs are beneficial when dealing with low-power and high-power signals. However, the performed measurements in this study took place in a controlled lab environment where input power is not an issue. Furthermore, as it can be seen in the next paragraph, the ADCs feature a wide dynamic range.

As there was no information about OR's maximum and minimum input power available, input power sweeps were performed. The measurements should give necessary input power level to obtain a low-noise and therefore high SNR spectrum. A signal source was set to 50 MHz and connected to the differential OR's port using a Balanced-unbalanced (Balun). For the Balun, an insertion loss of approximately 7 dB was measured.

The OR input power was swept from −57 dBm to 8 dBm. As the signal source could not output power smaller than −20 dBm, additional attenuators were used. The Balun also attenuated the signal source's signal by approximately 7 dB. To prevent the OR from being damaged, input powers higher than 8 dBm were not applied. Furthermore, at input signal levels of 8 dBm, the ADC was unable to sample and returned an 'overload error' implying operation above its maximum ratings.

In time domain, the cases of minimal and maximal applied input power can be seen in Figure 4.1.

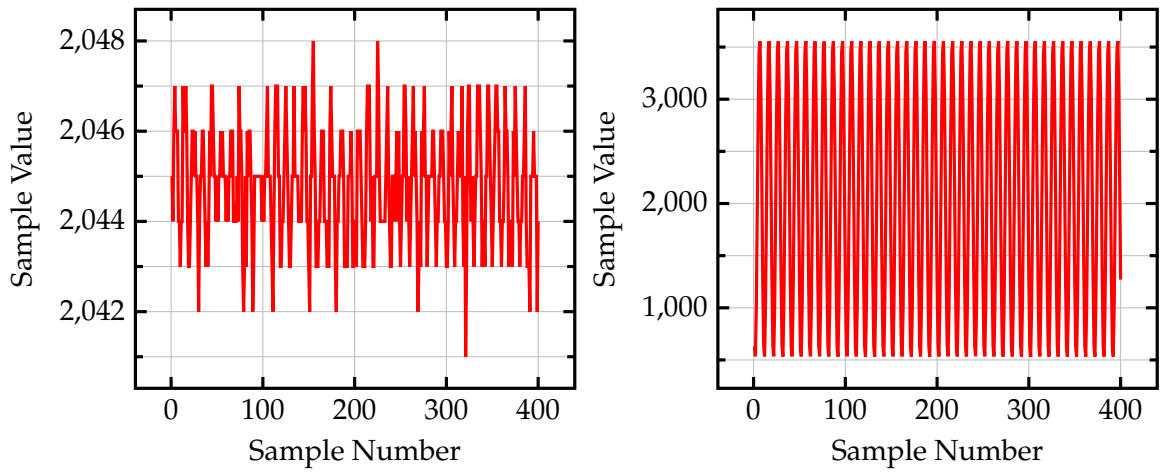


Figure 4.1.: This plot shows the analog-to-digital converter's samples in time domain at different input powers. On the left, the minimum input power of −57 dBm is present at the observation receiver's input ports. On the right, the maximum input power of 3 dBm is present at the observation receiver's input ports. For illustration purposes, only the first 400 samples are shown.

The low-power input signal of −57 dBm sampled by the ADCs exhibits lots of noise and does not properly represent a sine wave. The high-power signal of 3 dBm sampled by the ADCs is an accurate representation of the input signal. Amplitude values and the signal's period are constant and only marginal noise is present. Also notice the ADC's wide dynamic range. On the left, the sample's peak-to-peak value ist approximately 6 whereas on the right, the sample's peak-to-peak value is approximately 3000.

The samples acquired from the power sweep were also Fourier-transformed to obtain the respective SNR value. SNR allows for a more comprehensive comparison between different OR input powers. Figure 4.2 shows the OR's input power sweep versus SNR. It is important to mention that the Balun's insertion loss of approximately 7 dB has already been considered and the actual OR input power is shown. The ADC offers a wide dynamic input range and can detect signals from −57 dBm to 3 dBm input power. The ADC exhibits optimal performance from −4 dBm input power on and for input powers greater than −4 dBm the SNR does only improve marginal. For optimal measurements, an input power of −2 dBm was chosen in all following measurements.

The OR operation point is concluded in Table 4.1. All further measurements were based on this operation point.

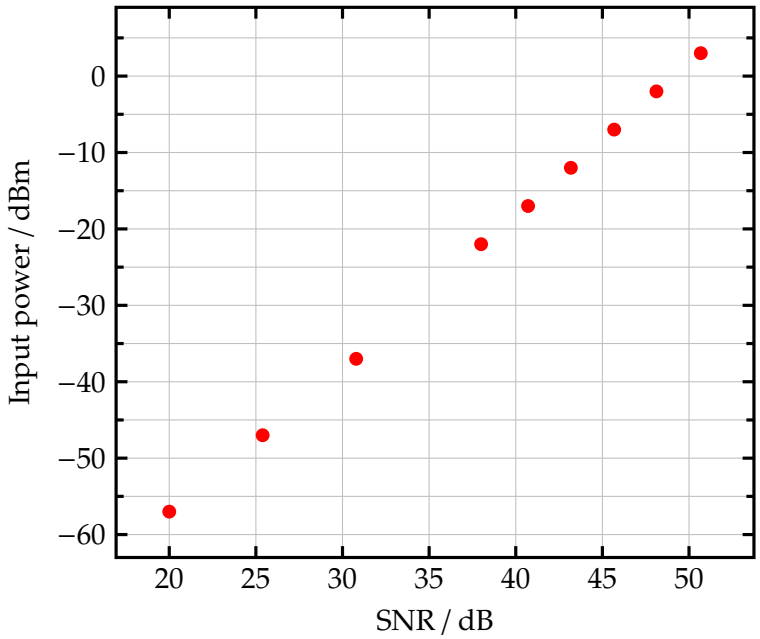


Figure 4.2.: This plot shows the digital predistortion observation receiver's signal-to-noise ratio when sweeping the observation receiver input power. Measured at sampling unit 4.

Parameter	Value
Supply Voltage	5 V
Input Power Range	−57 dBm to 3 dBm
Variable Gain Amplifier Gain	3 dB
Serial Peripheral Interface Clock	1953 kHz
Analog-to-Digital Converter Number of Samples	16384

Table 4.1.: This table shows the parameters of the observation receiver's operation point.

4.1.1. Scattering Parameters

The OR requires proper impedance matching so that adding the OR to a transmission chain does not disturb the signal before and after PA. An important parameter for determining if a component can be added to a transmission chain without disturbing the preexisting signal is the signal reflexion coefficient S_{11}. Input signal reflexions of the OR should be avoided as reflexions would disturb the transmission chain and lower the entire setup's SNR.

Figure 4.3 shows the OR S_{11} measurement. For input frequencies around 400 MHz and 1.4 GHz, the OR exhibits a high return loss of approximately −2.5 dB.

Expressed in linear scale and considering $10^{-2.5/20} = 0.75$, it can be seen that in the worst case scenario, approximately 75 % of input power is being reflected [Keyb]. Typically, signal reflexion values around −20 dB (10 %) across the entire relevant frequency range are considered acceptable.

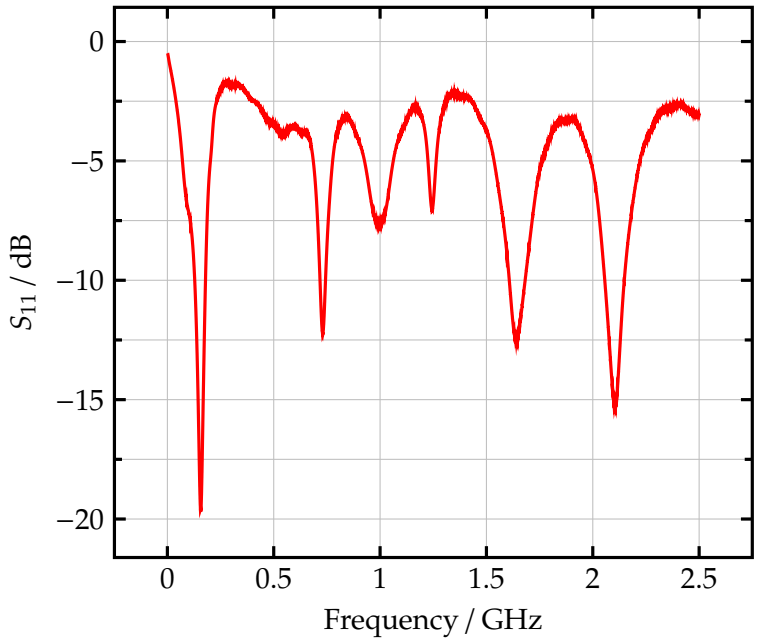


Figure 4.3.: This plot shows the observation receiver's return loss (S_{11}). Return loss measured at sampling unit 4.

Re-matching and re-simulating the OR's input path would be time-consuming. Therefore, it was decided to perform 'forced matching' by adding −10 dB attenuators at all OR input ports. The attenuators decreased the OR's return loss by −10 dB over the input frequency range and therefore reconsidering the OR's input path matching characteristics was not needed.

In case of forced matching, the ADC's wide dynamic range is beneficial. Even if the input signal is reduced by attenuators by 10 dB, the signal still can be sampled by the ADCs if the total input power level before the attenuators is kept greater than −20 dBm, see Table 4.1.

4.1.2. Temperature

In satellite applications, thermal management is crucial. Passive devices such as RF switches or filters usually do not heat up as much as active ones. The OR's active devices such as ADC or VGA's temperature was measured using a commercial infrared thermometer.

The active devices feature a standby mode that can be triggered via SPI. Standby is only supported by ADC and VGA. The VCOs do not explicitly support standby. But they can be powered off based on a logic level pin and therefore VCOs were also considered as being capable of standby.

Temperature was measured while powered on, in operation and standby. The temperature was measured for approximately 5 min to rule out measurement inaccuracies or fluctuations. The average obtained temperatures can be found in Table 4.2.

Table 4.2 shows, that the temperature of the states power on and operation do not differ significantly. However, ADC4 and VGA4 are in every state slightly cooler than their counterparts. A possible

	Temperature		
	Powered on	Operation	Standby
ADC 1	54 °C	54 °C	32 °C
ADC 2	56 °C	56 °C	33 °C
ADC 3	55 °C	55 °C	33 °C
ADC 4	49 °C	50 °C	32 °C
VGA 1	49 °C	48 °C	32 °C
VGA 2	48 °C	50 °C	33 °C
VGA 3	49 °C	50 °C	33 °C
VGA 4	45 °C	46 °C	33 °C
VCO 1	41 °C	48 °C	32 °C
VCO 2	40 °C	48 °C	33 °C

Table 4.2.: Temperatures of observation receiver's active components during operation and standby. The components are named with respect to the observation receiver's individual sampling units. VCO 1 represents the voltage-controlled oscillator for sampling unit 1 and 2. VCO 2 represents the voltage-controlled oscillator for sampling unit 3 and 4.

reason for the temperature difference could be that OR's ground pads for cooling are larger for sampling unit 4 than for the others. Another reason might be that sampling unit 4 has unused PCB space on the left which could benefit ADC4 and VGA4's heat dissipation, as it can be seen in photo A.1.

Up to this work's date, no detailed information about EIVE's temperature limits could be found. Therefore, it is difficult to asses measured OR temperatures. However, compared to other satellite applications, the OR's temperatures might be too hot. For example in [Zem96], the upper limit of data processing unit's operating temperature is 50 °C. If these limits also account for EIVE, additional heat sinks would be required.

However, the satellite designer has to take care of EIVE's thermal management. Each component's operating temperature range and its actual temperature have to be assessed and simulated. In a satellite, space is a scarce resource and therefore components often have to operate in tight spaces next to each other, optimally without causing thermal issues. Therefore, all satellite components should be considered together. This would allow for comprehensive insights about possible thermal issues and if additional heat sinks are required.

4.1.3. Power Consumption

As already said, OR requires 5 V DC supply voltage. Current consumption was measured in three different OR operation states: powered on, during operation and in standby. The measurements were performed using a Rohde & Schwarz HAMEG power supply.

In these measurements it was focused on the OR, therefore the Raspberry Pi was not included in power consumption measurements. It can be argued, that the Raspberry Pi may distort the

	Powered on	Operation	Standby
OR Current Consumption	2.063 A (10.314 W)	2.546 A (12.73 W)	0.480 A (2.40 W)

Table 4.3.: The observation receiver's current and power consumption is shown for three operation stages: powered on, during operation and in standby.

power consumption measurement because the Raspberry Pi's GPIOs feed a part of the passive components, for example the control pins of the RF switches. As the Raspberry Pi's GPIO maximum current draw is 16 mA, the influence of the GPIOs was considered negligible [Les].

Table 4.3 shows that the measured operation current consumption fits well with the theoretically calculated current consumption of 2.617 A by [Str19]. Due to standby capability, approximately 81 % of power can be saved in contrast to the operational state. In satellite operations, power consumption is a critical issue. Therefore, it is beneficial that the OR is able to put devices into standby. Regarding EIVE, during flyby phases the downlink and OR's components could be activated from standby. During eclipse, ADC, VGA and VCO can be put in standby to preserve energy.

ADC, VGA and VCO are synchronized by a 500 MHz reference clock. A clean and precise clock signal is crucial for OR operation. The OR features a 500 MHz temperature compensated crystal oscillator and its power supplied by the OR. The type of power supply is also important for reliable clock operations. Noisy or unstable power supplies could influence the clock signal and distort the clock signal. During this study's experiments, the OR was supplied by high-end lab power supplies. Future studies should consider switching to more real-world satellite power supplies such as solar panels or batteries. This would allow for a first estimation if power supplies may influence the OR's clock signal.

4.2. Narrowband Signal Acquisition

For first signal acquisition measurements, only one sampling unit was considered. A narrowband bandwidth of 250 MHz was sampled and evaluated.

OR's RF switches were set to bypass the input signal directly to the ADC, see Figure 3.4. No frequency mixing took place.

An Arbitrary Waveform Generator (AWG) was used to synthesize single tones for signal integrity measurements. Afterwards, the AWG signal was switched to a differential QAM-16 signal. The AWG's output signal was fed into a differential PA. The PA was operated in its linear region. To keep it simple and to reliably obtain PA output signals, no antenna was used but an oscilloscope was connected the PA output. Splitters were used to forward PA input and output signals to the OR. Attenuators connected to the PA's output ports prevent the subsequent stages (that is oscilloscope and OR) from being operated above their maximum ratings. The complete measurement setup can be seen in Figure 4.4. For a picture of the measurement setup see appendix D.4.

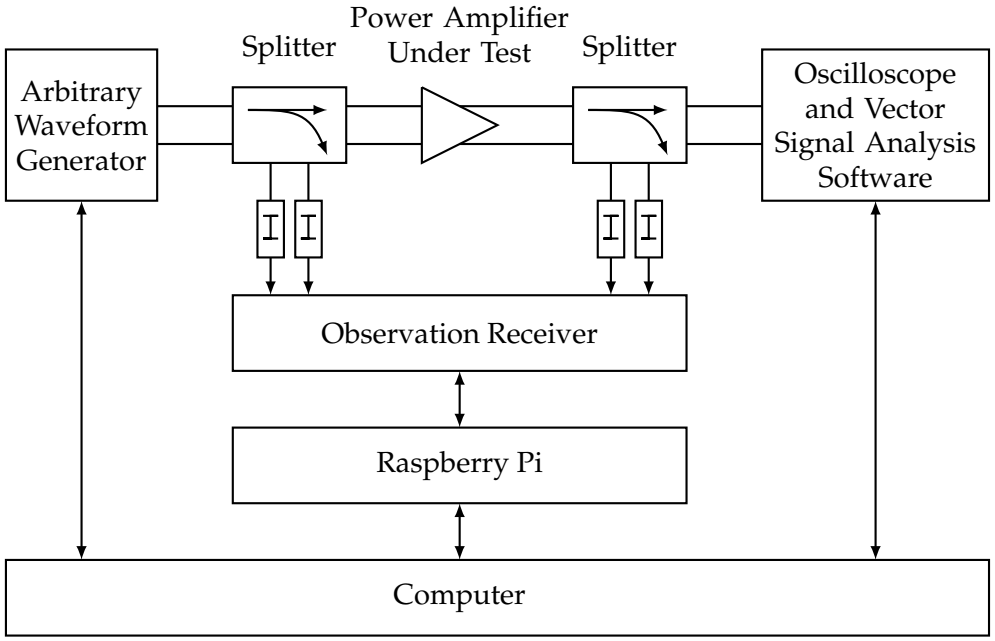


Figure 4.4.: Block diagram of the measurement setup. The power amplifier's input and output signals are sampled by the observation receiver and further post-processed by the Raspberry Pi and the computer. The computer is connected to the AWG and oscilloscope.

The ADC's command to start sampling data was not triggered via SPI. The Raspberry Pi only allows for sequential SPI commands, sending simultaneous SPI commands is not possible. When sending sequential SPI commands, the ADCs would receive the fill command one after another.

For implementation of predistortion, it is crucial that the acquired PA input and output signals are aligned in time domain. Any delay could corrupt predistortion coefficient calculation. Therefore, the ADCs' command to start sampling data was triggered using a special fill line. The fill line is connected to all four ADCs and allows for a simultaneous trigger to fill all ADCs at the same time. After the fill was issued, the Raspberry Pi obtained and processed the sampled data. The sampled data was copied to the computer and evaluated. The samples obtained from the ADCs were compared to the samples obtained by the oscilloscope. Comparison showed that the acquired ADC data is valid and the sample's integrity could be confirmed.

Besides sampling single tones, also the previously mentioned QAM-16 signal with a frequency offset of 100 MHz and a symbol rate of 50 MHz was sampled.

For more realistic results, the PA's gain was adjusted in a way that the PA operated in its nonlinear region. The PA was now in compression and OR's samples were obtained before and after PA. Figure 4.5 shows the frequency domain representation of the obtained samples before (left plot) and after (right plot) the PA. The right plot shows the obtained signal after the PA and shows the effects of compression. The 3rd and 5th IMD decrease PA linearity and increase noise floor. The PA's output spectrum is not linear anymore and SNR is decreased.

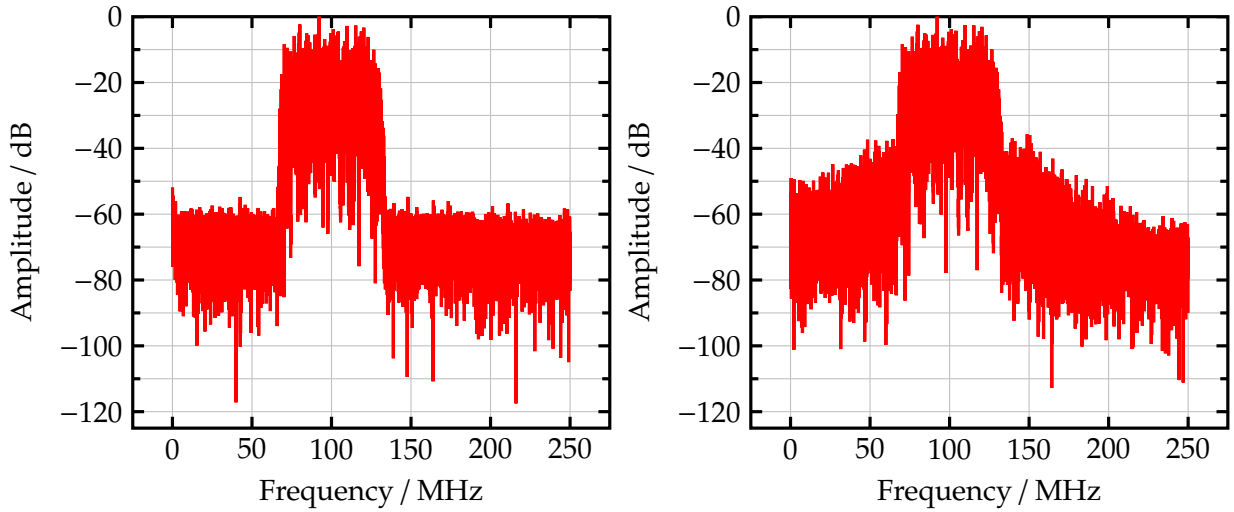


Figure 4.5.: The obtained samples of the PA output signals are shown in frequency domain. The left plot shows the frequency spectrum of the power amplifier's input port. The right plot shows the frequency spectrum of the power amplifier's output port. Amplitude is normalized to 0 dBm.

4.2.1. Delay

In simulations, the PA's group delay is often not taken into account. During simulation this should not raise an issue because the signal fed into the PA model should be instantly present at the output of the PA model because all components have ideal characteristics regarding the group delay.

However, in lab measurements the group delay needs to be considered to allow for proper predistortion. Otherwise, the predistortion coefficients may not be calculated correctly and the overall DP is not effective. If the delay is known, proper signal alignment in time domain can take place before passing PA input and output signals to the predistortion unit.

The AWG synthesized a single frequency which was sampled by the OR. MATLAB's *finddelay* function was used to calculate the delay between PA input and output. The *finddelay* function compares two signals and returns the delay in samples [Mat21d]. For multiple frequencies a delay of 1 sample was calculated. The delay of 1 sample (at the ADC's sampling speed of 500 MS/s) results in 2 ns of delay. In all future measurements, a delay of 2 ns was taken into account.

It can be argued that group delay depends on frequency and only considering single frequencies for calculating group delay may be insufficient. However, when using complex modulated baseband signals, the *finddelay* function often did not recognize start and end of the signal and therefore delivered invalid values. Furthermore, individual group delay measurements did not show a frequency-depended group delay, at least not in the baseband signal frequency bandwidth of 2.5 GHz.

4.2.2. Signal Acquisition Duration

Depending on communication link, environmental conditions or PA behavior, DP has to be repeated multiple times to ensure continuous linear signal amplification. A determining factor for repeated DP is the speed at which a signal can be obtained and processed. During signal acquisition, a limiting factor is the ADC. First, the ADC has to acquire the signal. Second, the signal has to be transferred to the processing unit, in this case the Raspberry Pi. For simplicity, the following measurements focus on the read-out duration of a single ADC which sampled a 250 MHz bandwidth with the maximum number of 16384 samples.

The OR's ADCs feature a resolution of 12-bit and a single sample is stored in two registers in two bytes. In order to obtain the two bytes, the Raspberry Pi first has to transmit two read-request bytes. The two read-request bytes address the registers that should be sent back by the ADC.

The process of requesting and receiving the ADC's samples is mainly limited by SPI speed and Raspberry Pi's GPIO toggling speed. The limitations of SPI speed was already discussed.

The GPIOs control the transistors used to switch between 3- and 4-wire SPI operation. Between sending and receiving data, the GPIOs initiate the transistor to switch the respective lines. This allows the Raspberry Pi to send and receive data also on 3-wire SPI busses.

The Raspberry Pi cannot toggle the GPIOs instantly. Measurements showed, that the Raspberry Pi requires on average 2 µs to change GPIO level from low to high or vice versa. Furthermore, the Raspberry Pi needs to switch internally between its SPI sending and SPI receiving mode. The process of GPIO toggling and mode switching has to be carried out 16384 times until all ADC's samples are obtained. The process is illustrated in detail in appendix C.3. Both GPIO toggling as well as SPI mode switching degenerate the Raspberry Pi's read-out speed.

Furthermore, the Raspberry Pi's dedicated Chip Select (CS) lines could not be used because the OR's CS is connected to all SPI components within one sampling unit. During 3-wire SPI communication, the ADC's output data is temporarily both on the MISO and MOSI line. When Raspberry Pi's dedicated CS lines are used, all components would receive the ADC's sent data on both MISO and MOSI pins and that may causes undesired SPI communication. To address the components individually, GPIO lines had to be used to realize CS functionality. However, using GPIO lines for CS operations also slows down the Raspberry Pi's read-out speed.

Figure 4.6 shows the ADC's duration when reading out 16384 ADC samples. ADC 1 and 2 differ in required read-out duration in contrast to ADC 3 and 4. On average, ADC 1 and 2 require 2.294 s and ADC 3 and 4 2.903 s read-out duration. The reason for this could be the different total length of the respective SPI tracks and the different Raspberry Pi bus lines.

The Raspberry Pi features two SPI busses, SPI0 and SPI1. SPI1 is responsible for SPI communication on sampling unit 1 and 2, whereas SPI0 is responsible for SPI communication on sampling unit 3 and 4. Further studies should investigate if a change of Raspberry Pi SPI busses may improve read-out performance.

The ADCs have an average read-out duration of approximately 2.6 s per ADC. The total ADC

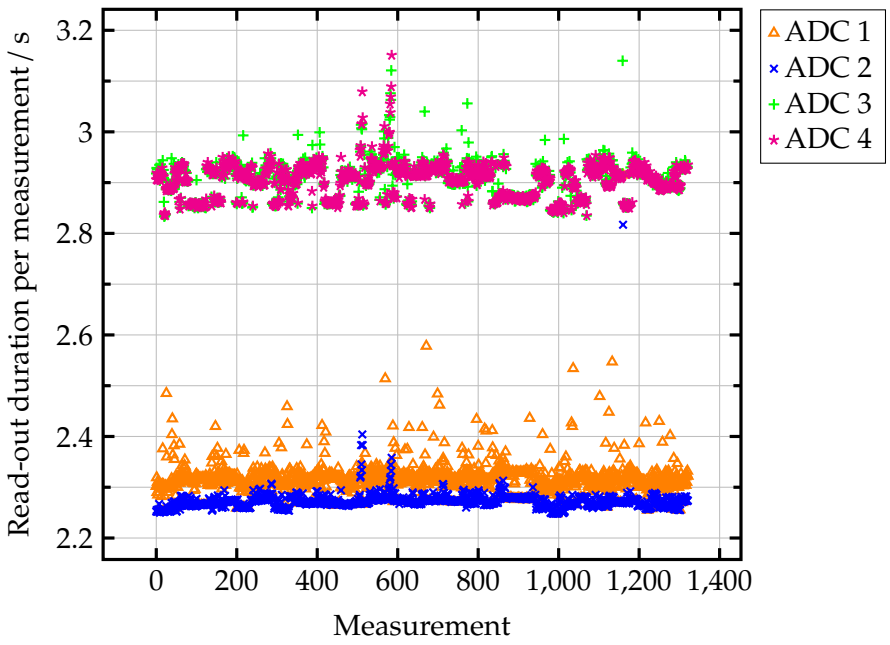


Figure 4.6.: This plot shows the analog-to-digital converter's read-out duration when obtaining 16384 12-bit samples. 1322 measurements were performed (x-axis) and the obtained read-out duration can be seen on the y-axis.

read-out duration t_{total} when considering all four ADCs and with respect to N frequency windows scales to:

$$t_{\text{total}} = N \cdot 4 \cdot 2.6\,\text{s}. \tag{4.1}$$

In a 2.5 GHz sampling bandwidth scenario, $N = 17$ windows are required which equals a total read-out duration of 2.95 min. Due to environmental factors such as weather conditions, PA's nonlinearity behavior or temperature can change significantly within 2.95 min. This could limit the DP's effectiveness as the PA input and output signal characteristic could have changed during signal acquisition. In a lab environment, it is expected that the previously mentioned factors do not influence the experimental communication link significantly. Nevertheless, this study's measurement setup using a Raspberry Pi and GPIOs for SPI communication is not ideal and should be improved in future studies by replacing the Raspberry Pi with an alternative SPI controller.

To estimate the maximum total read-out duration possible, an ideal OR setup is assumed: No GPIOs are used and in addition, an ideal SPI controller supports the ADC's maximum clock speed of 25 MHz.

For reading out one sample, four bytes are required (two read-request and two bytes containing the 12-bit sample value). Similar to the previous measurement, the maximum number of 16384

samples should be considered. This gives

$$4\,\text{Byte} \cdot 16384 = 65536\,\text{Byte} \tag{4.2}$$

$$= 524288\,\text{bit} \tag{4.3}$$

to be transferred for a complete ADC read-out.

SPI is a fully synchronous protocol and therefore the maximum SPI clock speed can be also expressed as:

$$25\,\text{MHz} = 25\,\text{Mbit/s}. \tag{4.4}$$

Considering equations (4.3) and (4.4), it can be concluded that a complete read-out based on ideal conditions would take 20.972 ms. This is a reduction of read-out duration t_{total} of approximately 87 % in contrast to the measurements shown in Figure 4.6. In conclusion, ADC read-out duration strongly depend on the measurement setup but improvements are possible. Improved read-out duration will benefit DP efficiency.

4.3. Broadband Signal Acquisition

Broadband signal acquisition describes the process of obtaining a bandwidth wider than the ADC's 250 MHz bandwidth using the concept of frequency windows.

OR's RF switches were set to forward the signal to the frequency mixer, see Figure 3.4.

For this measurement, a single tone higher than ADC bandwidth of 250 MHz was considered. The Raspberry Pi was configured to sample 2.5 GHz which is EIVE's usable bandwidth. The Raspberry Pi sets the OR's VCOs accordingly and acquires ADC samples of each frequency window up to 2.5 GHz (17 frequency windows in total).

During measurement it was found out, that the OR misses a bandpass filter in front of the frequency mixer. Because of the missing filter, undesired image frequencies are downconverted into the sampled frequency windows and therefore deteriorate broadband signal acquisition.

Before considering the actual measurement, first the mathematical background is highlighted. For instance, an OR input frequency of 275 MHz is assumed. The frequency of 275 MHz is right between frequency window 0 and frequency window 2 and should only be present in frequency window 1, see Figure 3.5. The OR's frequency mixer in the downconverting path (see 3.4) is assumed to be ideal and can be described by the following equations:

$$f_{\text{IF}\,1} = f_{\text{LO}} + f_{\text{RF}} \tag{4.5a}$$

$$f_{\text{IF}\,2} = |f_{\text{LO}} - f_{\text{RF}}|. \tag{4.5b}$$

The frequencies from above are explained in the following and they are also referred to in Figure 3.4.

- f_{IF} is the frequency mixer's IF frequency and in case of OR it is the frequency that travels to the ADC.
- f_{LO} is the frequency mixer's LO frequency and in case of the OR it is the VCO frequency.
- f_{RF} is the frequency mixer's RF frequency and in case of the OR it is the OR input frequency.

Table 4.4 shows the resulting frequencies of the first four frequency windows when applying a constant input frequency of 275 MHz and considers equation (4.5).

The obtained frequency peaks within the individual frequency windows are not as expected. Due to the missing bandpass filter in front of the frequency mixer, frequency windows 2 and 3 also exhibit frequencies within the ADC sampling bandwidth and therefore also get acquired by the ADC. This leads to an incorrect spectral representation of the 2.5 GHz bandwidth signal. The incorrect spectral representation can also be seen in the measurements. Figure 4.7 shows the obtained frequency spectrum when applying an input frequency of 275 MHz. For illustration purposes, only the first four frequency windows are considered.

Frequency window 0 shows a peak at approximately 225 MHz. The origin of this peak is not entirely clear. Most probably the peak is due to insufficient isolation at the OR's input chain.

Frequency window 1 shows a peak at 125 MHz. That is the expected frequency peak according to Table 4.4. As it can be seen in Figure 4.7 in spectral representation, this peak is correctly located in the spectrum at 275 MHz.

Frequency windows 2 shows a peak at approximately 25 MHz (Frequency in overlapping spectral representation: 325 MHz). This peak is present due to the mixing products according to Table 4.4. This peak is approximately 5 dB higher compared to the peak of frequency window 1. This implies that the OR's different sampling paths exhibit different losses. The VGAs could compensate for a power imbalance between different OR paths.

Frequency window 3 shows a peak at approximately 175 MHz (Frequency in overlapping spectral representation: 625 MHz). This peak is also present due to undesired mixing products as shown in Table 4.4.

In conclusion, Figure 4.7 shows an incorrect spectral representation due to undesired mixing

Frequency	Frequency Window 0	Frequency Window 1	Frequency Window 2	Frequency Window 3
OR in (f_{RF})		275 MHz		
VCO out (f_{LO})	-	150 MHz	300 MHz	450 MHz
Frequency mixer out (f_{IF})	-	125 MHz, 425 MHz	25 MHz, 575 MHz	175 MHz, 725 MHz
ADC in	-	125 MHz	25 MHz	175 MHz

Table 4.4.: This table gives an overview of the resulting frequencies in the first four frequency windows when applying 275 MHz at the observation receiver's input. Furthermore, the frequency present at the ADC's input after low-pass filtering is shown.

products caused by the OR's frequency mixer. The input signal is represented at incorrect locations in the total spectrum such as peaks at 325 MHz or 625 MHz.

Table 4.4 shows that the undesired frequencies are caused by the frequency mixer's downconversion which leads to the question if other frequency mixer types such as image-reject mixers could suppress the undesired frequencies.

An image-reject mixer is able to suppress one sideband. The output of either equation (4.5a) or equation (4.5b) could be suppressed. However, as it can be seen in Table 4.4, desired and undesired frequencies are within a single sideband (that is (4.5b)). Therefore, an image-reject mixer would not help.

Furthermore, when considering not only a single frequency but a wideband modulated signal, the frequency mixer would output various incorrect frequencies in each frequency window as frequency components get intermixed with each other. The resulting frequency spectrum would be incorrect and, furthermore, post-processing techniques could also not recover the desired signal.

The undesired mixing products could be reduced by a tunable bandpass filter implemented in front of the OR's frequency mixer, see Figure 4.8. This would reduce the undesired frequencies such as the peak of 25 MHz in frequency window 2.

While sampling a broadband signal, the tunable bandpass filter's passband should match each frequency window's range. In total, passband frequencies ranging from 200 MHz to 2600 MHz are required. As the required passband frequencies cover a high bandwidth, probably multiple

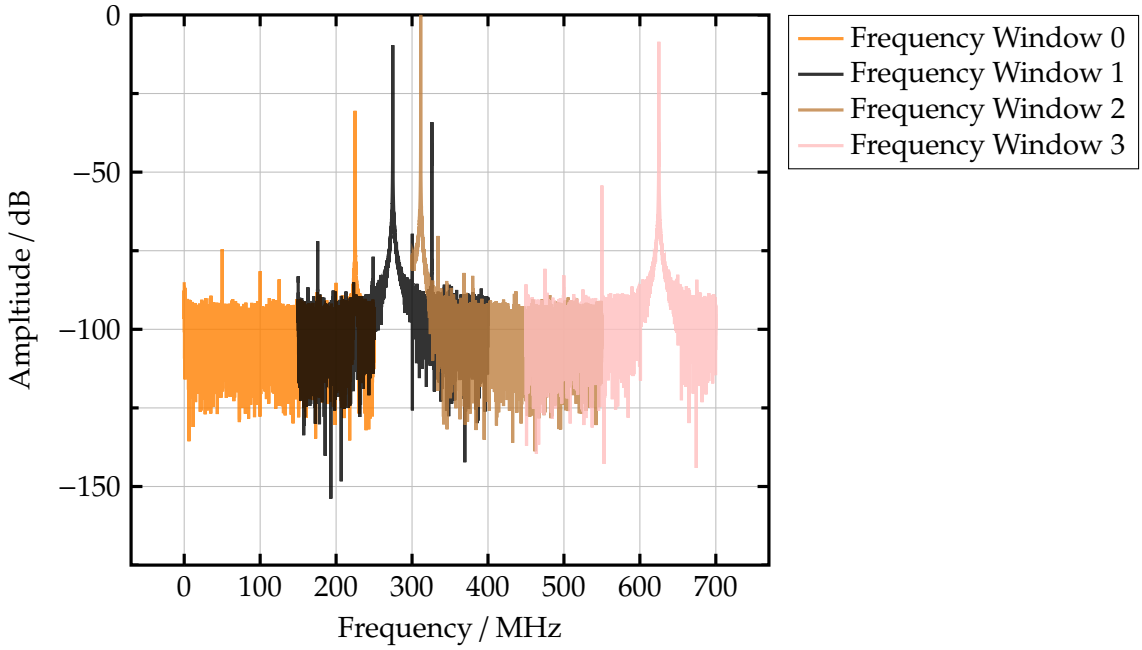


Figure 4.7.: The first four overlapping frequency windows in spectral representation are shown. Each frequency window was sampled by the observation receiver, Fourier-transformed and shifted in frequency to allow for a spectral representation from 0 MHz to 700 MHz. Amplitude levels were normalized to 0 dB.

bandpass filters have to be used. The tunable bandpass filters should be controllable by SPI. This would allow for the Raspberry Pi to set the respective passband for each frequency window.

In the following, the previous measurement is described if a tunable bandpass filter had been used.

For instance, the start and stop frequencies of frequency window 2 are 300 MHz and 550 MHz, respectively. A tunable bandpass filter's passband would be adjusted in such a way that only frequencies between 300 MHz and 550 MHz are forwarded to the frequency mixer's RF port. When considering Table 4.4, the input frequency of 275 MHz would be filtered. Therefore, the frequency mixer's output frequency would–ideally–be zero. The ADC would not sample any signal and the spectral representation would be correct.

When considering the tunable bandpass, the previous Table 4.4 can be updated to Table 4.5. In Table 4.5 it can be seen that due to bandpass filtering, only frequencies that are within the respective frequency window's bandwidth can enter the frequency mixer. When downconverting signals from other frequency windows, no undesired frequency mixing products are created by the frequency mixer and the spectral representation would be correct.

To verify the idea of using bandpass filters to reduce the creations of undesired harmonics, simple bandpass filters for the frequency windows 1, 2 and 3 have been designed. The filters were soldered on an already fabricated PCB developed by ILH. The PCB can be seen in appendix E.5. Based on the given PCB design, 3rd order Butterworth bandpass filters were designed using [RFT]. The bandpass filter's passband was designed according to the frequency windows start and stop frequencies.

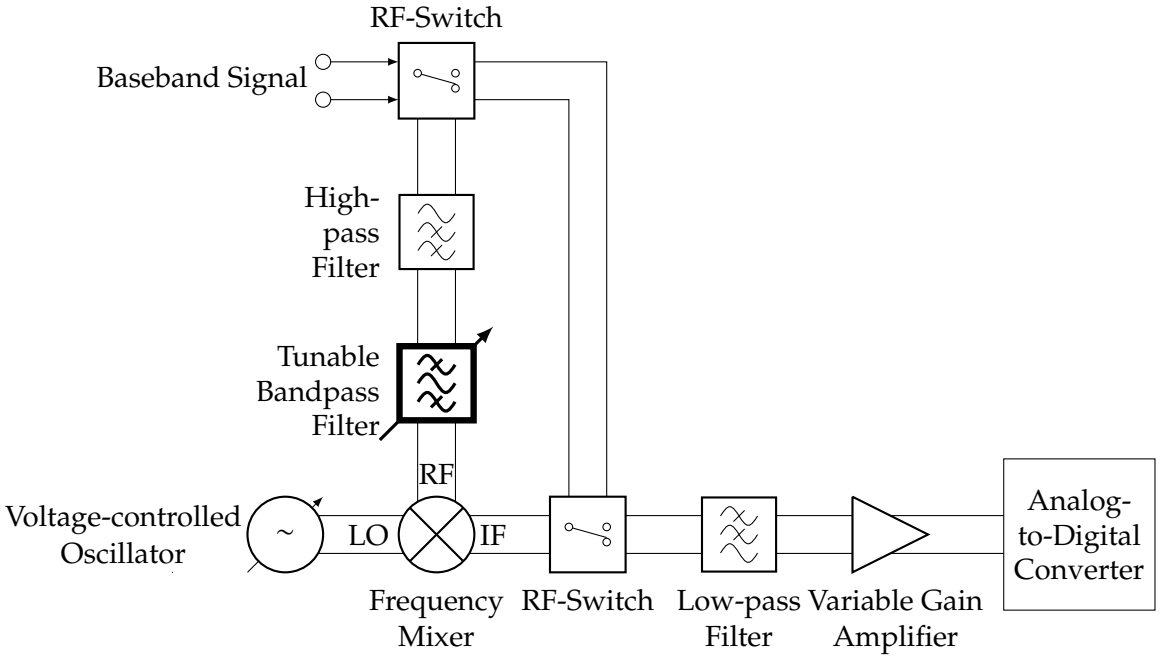


Figure 4.8.: This circuit shows a possible implementation of the tunable bandpass filter in the observation receiver's sampling unit.

Frequency	Frequency Window 0	Frequency Window 1	Frequency Window 2	Frequency Window 3
OR in (f_{RF})		275 MHz		
Tunable bandpass filter out	-	275 MHz	-	-
VCO out (f_{LO})	-	150 MHz	300 MHz	450 MHz
Frequency mixer out (f_{IF})	-	125 MHz, 425 MHz	-	-
ADC in	-	125 MHz	-	-

Table 4.5.: This table gives an overview of the resulting frequencies in the first four frequency windows when applying 275 MHz at the observation receiver's input. Furthermore, the tunable bandpass filter before the frequency mixer is considered. The frequency present at the ADC's input after low-pass filtering is also shown.

In total, three bandpass filters have been fabricated. For each frequency window, the respective bandpass filter was inserted between signal source and OR. After sampling frequency window 0, the OR was halted, the bandpass filter for frequency window 1 was placed between signal source and OR and sampling continued. This was done for the first four frequency windows and the obtained spectral representation is shown in Figure 4.9.

Due to the filters applied in the subsequent frequency windows, the amplitude levels changed and this also influenced frequency window 0 amplitude levels.

Frequency window 1 shows the expected peak at 125 MHz.

Frequency window 2 shows a peak at 25 MHz. The bandpass filter of frequency window 2 was apparently not effective enough to filter out the undesired mixing components. Therefore, the peak of the undesired mixing product is still present.

The undesired mixing product of frequency window 3 at 175 MHz was successfully reduced by approximately 40 dB and is therefore represented correctly in the spectral representation. This implies, that when using bandpass filters for the individual frequency windows, sampling of broadband input signal based on the concept of frequency windows does work. In this measurement, only bandwidth up to 700 MHz were sampled. However, it can be concluded that when using tunable bandpass filters for all frequency windows, sampling higher bandwidths up to the OR's maximum bandwidth of 2.5 GHz would be possible.

In this study, only simple and low-order bandpass filters were used. In futures studies, the frequency window's bandpass filters could be improved in terms of filter order and design. This would allow for more accurate bandpass filters which would lead to a more precise spectral representation of overlapping frequency windows.

The next step after obtaining a broadband bandwidth is to consider parts where frequency windows overlap. All frequency windows overlap by 50 MHz, see Figure 3.5. This overlap reduces artifacts

(for example peaks) at the borders of the ADC bandwidth and therefore allows for a continuous total spectrum. Therefore, in post-processing this overlap can be used to compensate for any incorrect frequencies at the start or end of frequency windows. To consider the overlap of the individual frequency windows, the Raspberry Pi Fourier-transforms the ADC's sampled time domain value of each frequency window. Afterwards, the individual spectral representation of each frequency window are divided into overlapping frequency parts and non-overlapping frequency parts.

For instance, in Figure 4.9, the overlapping frequency parts are 150 MHz to 250 MHz, 300 MHz to 400 MHz, 450 MHz to 550 MHz and so on. The non-overlapping frequency parts are 0 MHz to 150 MHz, 250 MHz to 300 MHz, 400 MHz to 450 MHz and so on.

The overlapping frequency parts are averaged. Afterwards, each frequency window part is combined in frequency domain to obtain a complete spectrum. The complete spectrum is then inverse Fourier-transformed to obtain the time domain values. The time domain values are then forwarded to the DP unit.

In the previous measurement seen in Figure 4.9, the individual frequency windows are only shifted in frequency and the overlapping frequency window parts were not averaged. In Figure 4.10, the overlapping frequency parts have been averaged. It can be seen that the amplitude of all peaks except the desired peak at 275 MHz decreased.

For instance, the undesired peak at 225 MHz is within an overlapping frequency window part. Without averaging, the peak's amplitude is approximately −26 dB, see Figure 4.9. With averaging,

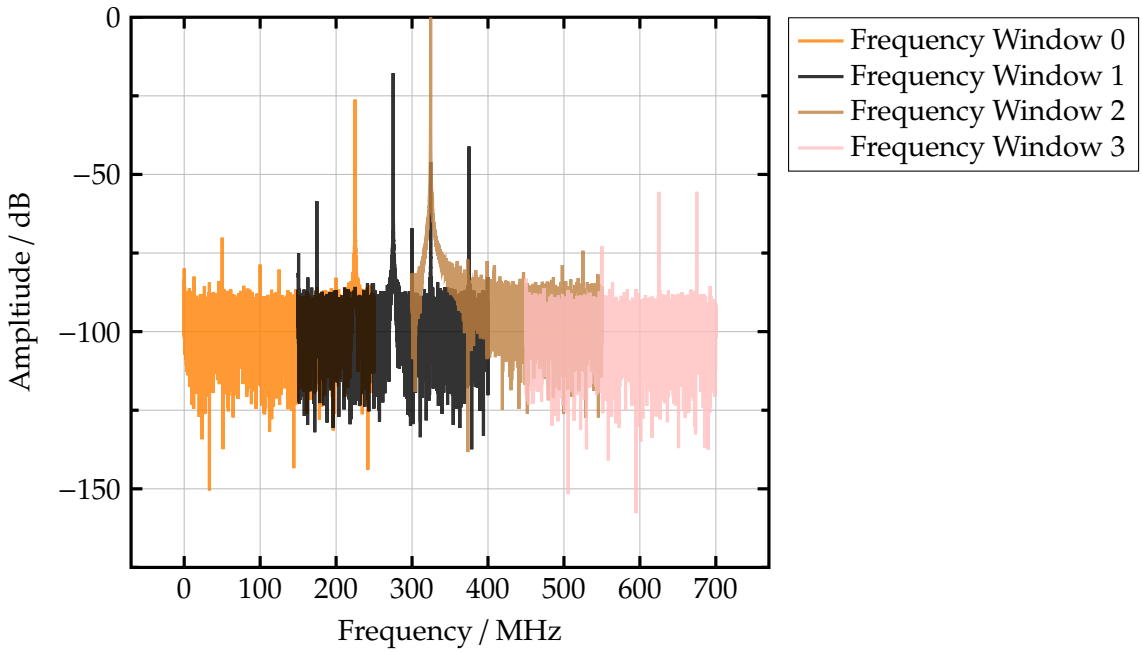


Figure 4.9.: The first four overlapping frequency windows in spectral representation are shown. Each frequency window was sampled by the observation receiver, Fourier-transformed and shifted in frequency to allow for a spectral representation from 0 MHz to 700 MHz. Amplitude levels were normalized to 0 dB.

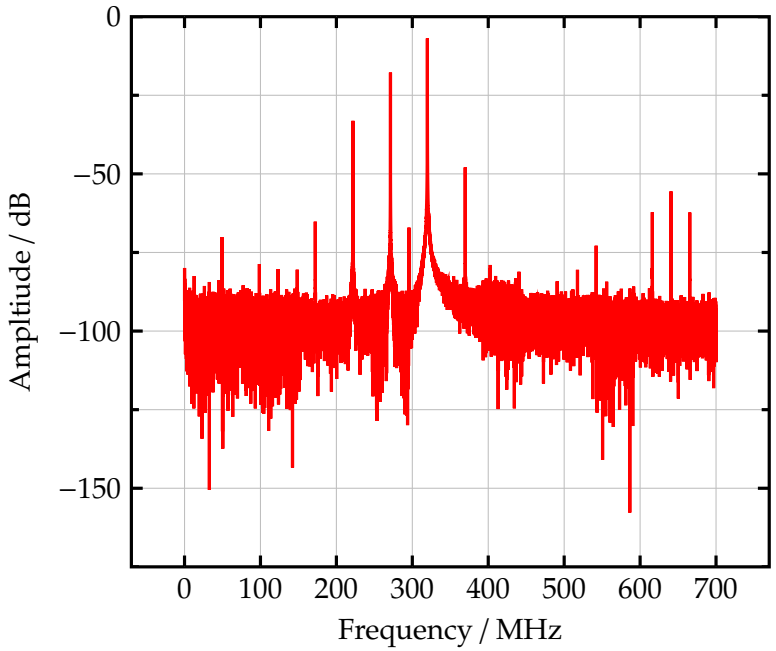


Figure 4.10.: The spectral representation of the first four frequency windows is shown. The frequency window's overlapping parts were averaged. All frequency window parts–overlapping and non-overlapping–were added sequentially in frequency domain. Amplitude levels were normalized to 0 dB.

the peak's amplitude is decreased to approximately −33 dB, see Figure 4.10.

However, a new frequency peak at 650 MHz can be seen. This frequency peak is caused by averaging the end of frequency window 3 with the start of the next frequency window 4. Frequency window 4 exhibits a peak at the respective frequency and therefore this peak at 650 MHz is present.

It can be seen that averaging the overlapping frequency window parts can reduce undesired frequency peaks of individual frequency windows. This smooths the overall spectrum and allows for a more precise sampling of broadband bandwidths which benefits the subsequent DP.

4.4. Digital Predistortion

After successfully obtaining samples with the OR, the next step was to process the obtained samples and to allow for DP. However, for DP a signal processing unit such as a computer is required as the OR is only capable of sampling data. It was aimed to facilitate a straight-forward DP which does not require comprehensive simulation or PA characterization.

Matlab Simulink offers two simple building blocks for DP: a DP block and a coefficient estimator block [Mat21a, Mat21c].

The DP coefficient estimator compares the PA input and output signal and provides a matrix of memory-polynomial coefficients. The DP coefficient estimator block is based on polynomial DP, similar to the approach mentioned in section 2.4.3 and also considers PA memory effects [Mat18].

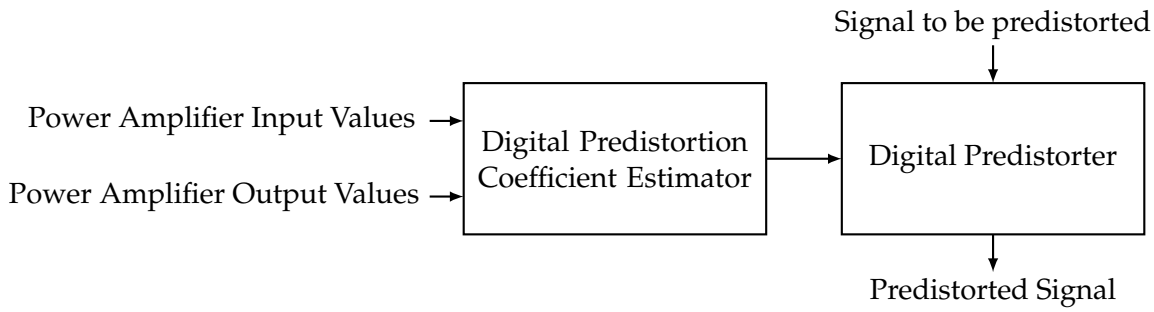


Figure 4.11.: This figure shows Matlab's digital predistortion building blocks that were used for this work's predistortion. Adopted from [Mat21c, Mat21a]

The DP block can also be referred to as the predistorter and it predistorts an input signal based on the coefficient matrix provided by the DP coefficient estimator block. Figure 4.11 shows the two building blocks. In the following, the three steps of obtaining a predistortet signal based on the measurement setup in Figure 4.4 are explained.

First, the AWG was set to output a modulated waveform. To obtain enough information for DP, it was ensured that the modulated signal's symbol rate was approximately $4-5$ times smaller than the available sampling bandwidth. The waveform was provided by Keysight IQ Tools (IQTools) and exported as MAT-File on the computer. Furthermore, the AWG's output power was set in a way that the PA operated in its nonlinear region.

Second, the Raspberry Pi retrieved the samples from the OR's sampling units. Afterwards, the samples of the individual ADCs were normalized and the sampling unit's I and Q data was combined into MAT-File per signal path. So after sampling, the Raspberry Pi provided a complex, normalized, time domain MAT-File of OR's sampled PA in and PA out data.

Third, the predistortion process started. Matlab's building blocks were realized in code and the Raspberry Pi MAT-Files were loaded into Matlab, along with the original AWG output waveform provided by IQTools. To ensure proper signal alignment, the PA input signal was delayed according to section 4.2.1. This way, all input parameters (PA input, PA output and the AWG signal) of the building blocks were satisfied and the generation of the predistorted waveform started.

Fourth, the predistorted waveform was exported from Matlab and loaded into the AWG. Keysight's Vector Signal Analysis software connected to an oscilloscope was used to observe the PA's output signal and to quantify the DP.

Unfortunately, it was not possible to achieve DP as the predistorted waveform did not improve PA linearity.

To rule out any OR impairments, the OR was replaced with an Oscilloscope. The delay was considered, followed by the mentioned steps of the predistortion process. Still, no DP could be achieved.

Due to time limitations, it was not possible to further investigate this issue. However, proper signal alignment is a crucial requirement for DP [Key02, Mat21b]. As an incorrect delay correction

might be the issue for the failing DP, future studies should therefore scrutinize the performed delay calculations.

Instead of comparing a single frequency in time domain, an oscilloscope could be used to determine the delay between PA input and output. The oscilloscope could be connected to PA input and output and based on trigger issued be the AWG the delay could be determined. Furthermore, as mentioned in [MKSK04], if the obtained delay does not match with the signal's discrete samples, interpolation could be beneficial. Additionally, comprehensive signal correlation could be used to determine the delay of the modulated signal.

Even though DP was not possible, the previous workflow showed a possible implementation of OR and DP into a communication link in general. The Raspberry Pi facilitates retrieving and pre-processing of data and provides the data to a computer which performs DP and controls the signal source. When replacing the Raspberry Pi with computationally more powerful processing units such as a field programmable gate array, SPI communication and DP could be done within a single unit and hardware complexity would be reduced.

5. Conclusion and Outlook

In this study, fundamental OR functionality has been examined and its suitability for implementation in satellite communication links has been evaluated.

Fundamental OR operation was possible to establish, although for sampling of broadband signals, bandpass filters had to be added.

Bandpass filters were required to filter out undesired mixing products caused by OR's frequency mixer. Bandpass filters for each frequency window were necessary.

Due to insufficient return loss on OR's input ports, the experimental setup suffered from sever loss of SNR. Attenuators helped with matching, although causing loss of signal power. Therefore, rematching the OR's input paths is proposed.

To the best of the author's knowledge, in former studies only bandwidths up to 150 MHz have been sampled based on the reduced-bandwidth approach. This study showed for the first time, that reduced-bandwidth sampling can also be applied for sampling of bandwidths as high as 2.5 GHz.

However, this study is object to several limitations. All measurements were performed in an experimental lab setup. Furthermore, no DP was achieved. Nevertheless, possible consequences can be derived from the study regarding implementation of OR into DP systems for satellite communication links.

Implemented into satellite communication links, OR could facilitate sampling of broadband satellite signals for subsequent DP. This way, higher data rates and efficient use of available bandwidth could be achieved, speeding up transmission of large data sets during the satellite's limited flyby time. Power is a sacred resource on satellites and has therefore be used as efficient as possible. PA efficiency could be improved by OR in combination with DP.

Future studies should consider implementing OR into DP system. This would allow for further insights into whether OR can facilitate low-cost and broadband sampling for DP in satellite communication link settings.

If bandpass filters would be implemented, OR would capable of sampling broadband signals. This way, OR, a low-cost sampling PCB, could relieve the trade-off between ADC costs and sampling bandwidth.

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A. Appendix

A.1. Photo of Observation Receiver

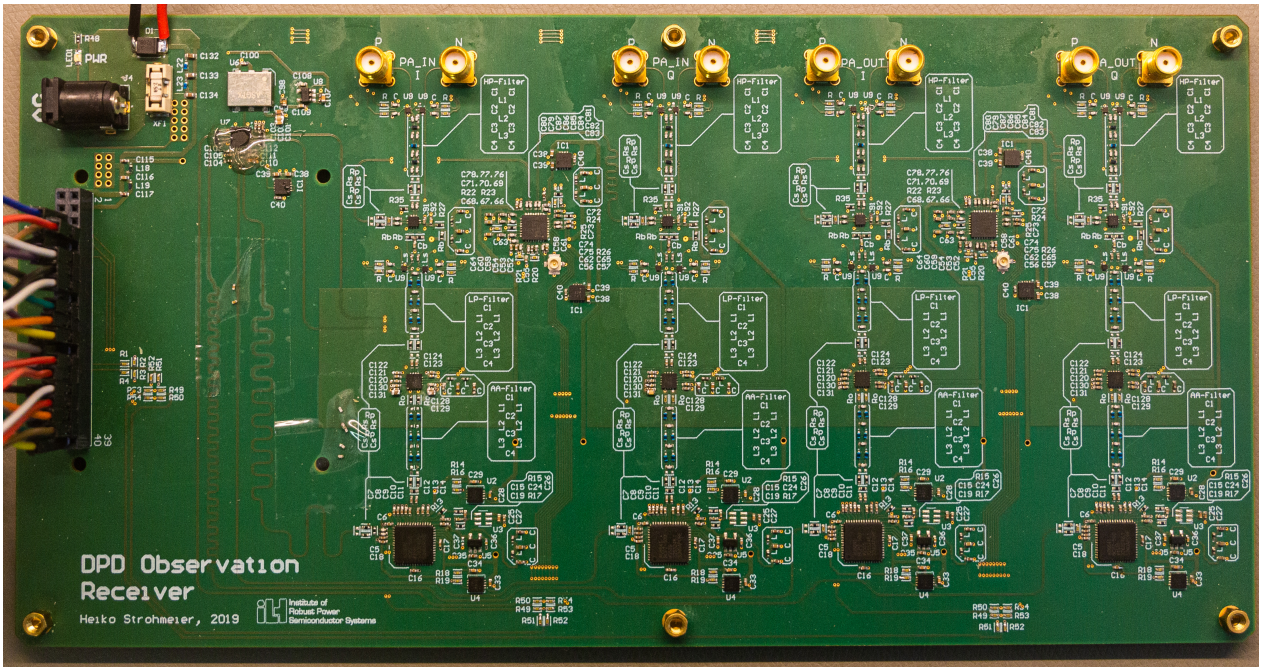

Figure A.1.: Photo of the observation receiver printed circuit board. Starting from the top left, the connector for power supply can be seen as well as the oscillator providing a clock of 500 MHz for the components. On the left, the 40 pin header for the controlling the components is shown. In the center, four vertical branches can be distinguished, each starting with two differential SMA connectors followed by matching networks, the frequency mixer, the variable gain amplifier and finally the analog-to-digital converter. Between the two input branches on the left and right the voltage-controlled oscillators can be seen.

A.2. Serial Peripheral Interface Circuit

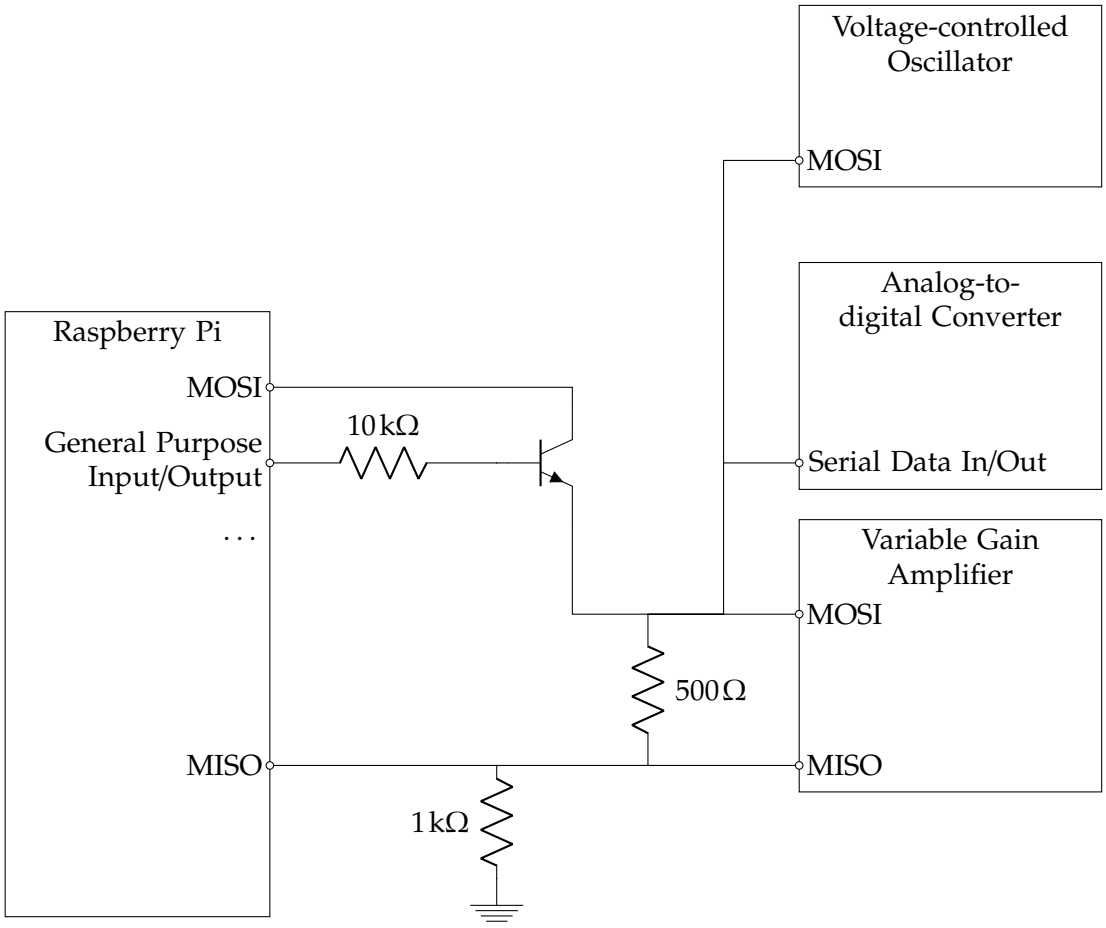

Figure B.2.: This schematic shows the circuit used to allow for a mixed SPI environment while using the Raspberry Pi. A transistor was used to switch between 3-wire and 4-wire SPI operation. For simplicity, lines such as clock or CS are neglected in this schematic. A typical transistor such as [CDI] can be used. The circuit was realized on a breadboard.

A.3. Raspberry Pi and Analog-to-digital Converter's Read-Out Flow Chart

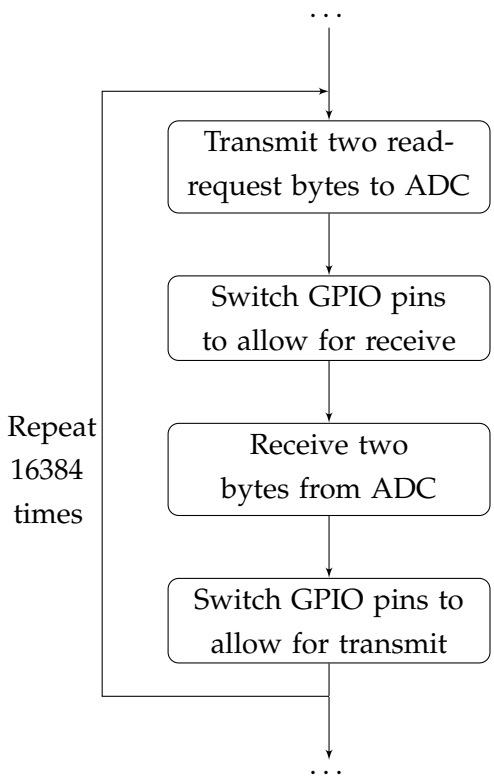

Figure C.3.: Extract of Raspberry Pi and ADC communication during readout of samples.

A.4. Photo of Measurement Setup

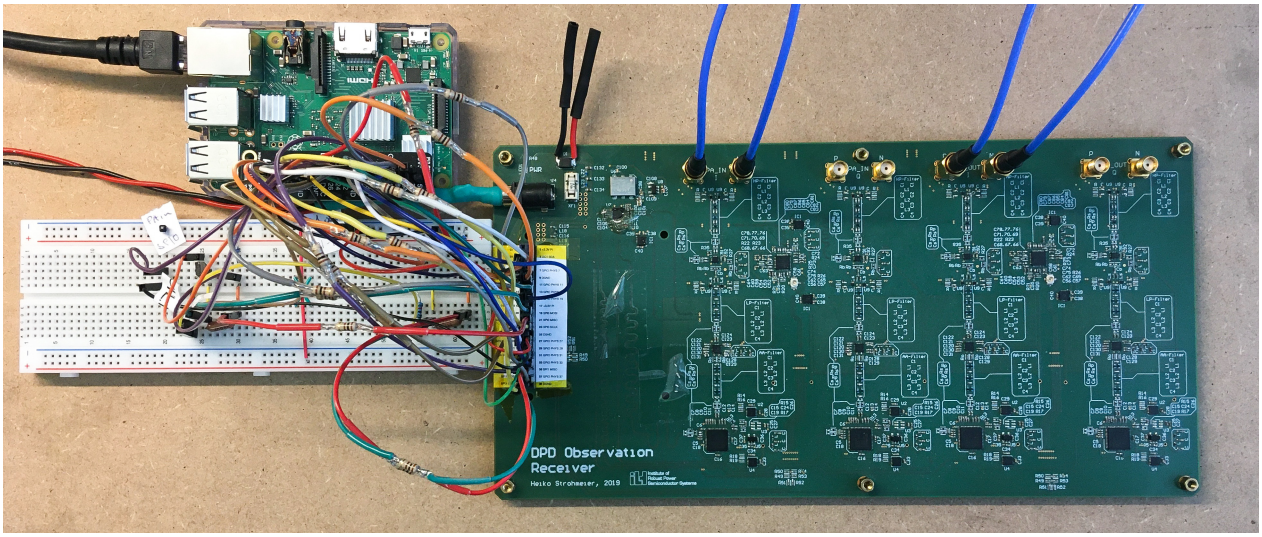

Figure D.4.: Photo of the observation receiver measurement setup. On the top, SMA cables connected to the splitters can be seen. On the left, the breadboard with the SPI 3- and 4-wire circuit is shown. On the upper left side, the Raspberry Pi for controlling the observation receiver via SPI can be seen. AWG, PA and splitters are not shown.

A.5. Photo of Bandpass Filter

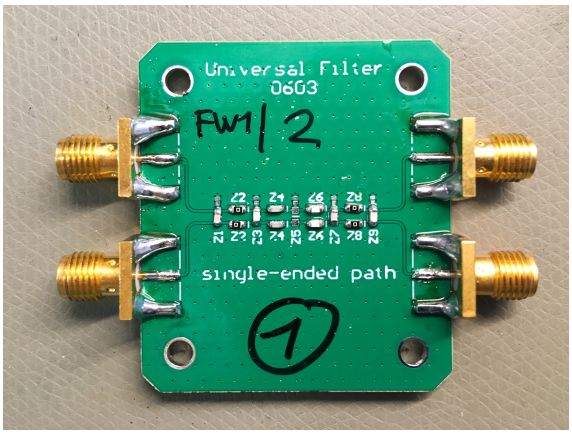

Figure E.5.: This photo shows the PCB used for bandpass filtering. The filters are realized as 0603 differential filters.