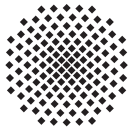

University of Stuttgart
Germany

Institute of
Robust Power
Semiconductor Systems

Student Research Project

Investigation of Flip-Chip Packaging for Monolithic Microwave Integrated Circuits

B. Sc. Martin Römhild

Supervisor: M. Sc. Moritz Vischer
Prof. Dr.-Ing. Ingmar Kallfass

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Postanschrift: Institut für Robuste Leistungshalbleitersysteme
Pfaffenwaldring 47

D-70569 Stuttgart

Tel.: +49 (0) 711 685 68700
Fax.: +49 (0) 711 685 58700
E-Mail: sekretariat@ilh.uni-stuttgart.de
Web: www.ilh.uni-stuttgart.de

Declaration

I hereby declare that this thesis is my own work and effort and follows the regulations related to good scientific practice of the University of Stuttgart in its latest form. All sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Stuttgart, 16.04.2021

B. Sc. Martin Römhild

Abstract

In this student research project flip chip is being investigated for its suitability as a packaging in the frequency range up to 100 GHz. The theoretical groundwork behind wave propagation in planar transmission lines is being discussed as well as the state of the art of flip chip processing. After a discussion of the simulated results of regular flip chip transitions and the so called hot via approach, in this work a novel mass-manufacturable packaging solution is proposed. The new packaging utilizes an intermediate substrate made of either fused silica or alumina and two subsequent flip chip bonding steps. In the frequency range of up to 100 GHz the new approach shows broadband matching and low insertion losses. It is possible to probe on-chip and use back end of line (BEOL) on-chip antennas with the new package. The proposed structure allows for connections between different chips on the same printed circuit board (PCB) as well as for connections to the PCB for the entire frequency range. According to the simulation the structure also shows resilience to manufacturing tolerances. The lowest achieved insertion loss at 100 GHz for a chip to chip connection at 2 mm distance between the chips is 0.77 dB which is lower and at much greater distance than the wire bonds presented by [1]. The transmission line connecting these two chips shows approximately 0.15 dB mm^{-1} line loss resulting in a loss of 0.24 dB per transition. This almost reaches the 0.2 dB insertion loss for a single flip chip transition achieved by [2]. For a connection from PCB to chip the minimum achieved insertion loss is 0.58 dB at 100 GHz.
Two process outlines to fabricate the novel packaging are proposed in this work. The processes use a combination of standard large area microelectronic fabrication and standard PCB manufacturing. Possible limitations of the different flip chip approaches are also discussed in this work.

Zusammenfassung

In dieser Forschungsarbeit wird Flip-Chip-Montage auf die Eignung für den Frequenzbereich bis 100 GHz untersucht. Zuerst erfolgt eine theoretische Diskussion über die Wellenausbreitung in planaren Wellenleitern und den Stand der Technik in der Flip-Chip-Montage. Es werden zunächst die Simulationsergebnisse von regulären Flip-Chip-Übergängen und dem so genannten Hot-Via-Ansatz diskutiert. Anschließend wird ein in dieser Arbeit neu entwickelter Ansatz vorgestellt. Der neue Ansatz nutzt ein Zwischensubstrat wahlweise aus Quarzglas oder Alumina und zwei nacheinander erfolgende Flip-Chip-Bond Schritte. Der neue Ansatz zeigt äußerst breitbandiges Verhalten bis einschließlich 100 GHz und geringe Einfügedämpfung. Außerdem werden on-Chip Messungen und die Nutzung von BEOL on-Chip Antennen durch die Struktur ermöglicht. Mit dem neuen Ansatz können Verbindungen von Leiterplatte zu Chip und zwischen verschiedenen Chips realisiert werden. Der neu entwickelte Ansatz zeigt sich robust gegenüber Fertigungstoleranzen in der Simulation. Die niedrigste Einfügedämpfung für eine Verbindung von Chip zu Chip beträgt 0.77 dB für eine Frequenz von 100 GHz bei einer Leitungslänge von 2 mm. Dies ist eine geringere Dämpfung als die Bonddrahtverbindung von [1]. Die Leitung, die diese Chips verbindet, hat eine Dämpfung von etwa 0.15 dB/mm, was zu einer Einfügedämpfung von 0.24 dB pro Übergang führt. Die Verbindung von Leiterplatte zu Chip zeigt eine minimale Einfügedämpfung von 0.58 dB bei 100 GHz.
Um den vorgeschlagenen Ansatz herstellen zu können werden in dieser Arbeit zwei Prozesse vorgestellt. Die Prozesse nutzen Standardherstellverfahren der großflächigen Mikroelektronik und der Herstellung von Leiterplatten.
Mögliche Limitierungen und Fehlerquellen der angesprochenen Flip-Chip Ansätze werden ebenfalls diskutiert.

Contents

List of Abbreviations and Symbols

Al_2O_3	alumina
Au	gold
b	spacing of the outer conductors in a Stripline
BEOL	back end of line
CMOS	complementary metal oxide semiconductor
CPW	coplanar waveguide
CST	CST Studio Suite 2020
Cu	copper
d	thickness
DC	direct current
ENEPIG	electroless nickel electroless palladium immersion gold
EPIG	electroless palladium immersion gold
ϵ_r	relative permittivity
f	frequency
FEM	finite element method
FIT	finite integration technique
GaAs	gallium arsenide
GCPW	grounded coplanar waveguide
IC	integrated circuit
IF	intermediate frequency
iGCPW	inverted grounded coplanar waveguide
ILH	Institute of Robust Power Semiconductor Systems
In	indium
IS	intermediate substrate
LAM	large area microelectronic processes
LCP	liquid crystal polymer
λ_d	smallest wavelength in the material
λ_0	vacuum wavelength
MMIC	monolithic microwave integrated circuit
mmWave	millimeter wave, 30-300 GHz
Mo	molybdenum
μ_r	relative permeability
μ_0	magnetic permeability of free space

Ni	nickel
ω	angular frequency
PCB	printed circuit board
PEC	perfect electrical conductor
QTEM	quasi transverse electromagnetic
RIE	reactive-ion etching
RF	radio frequency
RO3003	Rogers 3003
SEM	scanning electron microscopy
Si	silicon
SiO_2	fused silica
Sn	tin
σ	conductivity
TE	transverse electric
TEM	transverse electromagnetic
TM	transverse magnetic
W	width of the center conductor of a stripline
W_e	effective width
w_{micro}	width of a microstrip line
UBM	under bump metallurgy
Z_0	line impedance
3D	three dimensional

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1. Introduction

With emerging mass-market technologies such as automotive radar in W-band and the trend towards ever increasing bandwidths in high data rate communication the frequency range of up to 100 GHz is of interest to satisfy these requirements. Especially chips operating in the sub-THz regime require a broadband intermediate frequency (IF) source for large bandwidths. While this IF source can be placed on the same chip, this would increase chip size and it might be more practical to use different chips for analog frontend and baseband/IF generation. Careful design of compensated wire bonds is capable of achieving low insertion and return losses over a wide band [1]. However, this requires very short wires and thus makes connections mechanically challenging at these frequencies.
Flip chip offers a compact alternative to traditional wire bonds. Instead of using wires to connect the chip with a board, the chip is flipped and the connection to the board is achieved by bumps. These bumps have a shorter length than wire bonds and subsequently cause less inductance. P.V. Testa et al. (2019) [2] demonstrated very low insertion losses of direct chip to chip interconnections using flip chip techniques over a frequency range from DC up to 200 GHz and Khan et al. (2014) [3] demonstrated low loss flip chip interconnections up to 170 GHz from a liquid crystal polymer (LCP) substrate to a flipped chip, although LCP are mechanically soft materials which may make it challenging to fabricate. The intention of this thesis is to investigate the potential and limitations of flip chip connections for the frequency range of up to 100 GHz for connecting a chip to a PCB and for connecting different chips to each other within this frequency range. The investigation focuses on the following aspects:

- As power is scarce at high frequencies, losses should ideally be as low as possible. Hence, loss mechanisms and possible ways to reduce the losses are a main focus.
- On-chip antennas are an attractive alternative to connecting to an external antenna as the lossy connection to the antenna is omitted. The suitability of flip chip for on-chip antennas is another aspect of the investigation with a focus on BEOL on-chip antennas.
- Especially in prototyping and for yield analysis, verifying a structure is important to find out potential faults if the manufactured result is not in agreement with the simulation. Hence, the verifiability of a structure is also an important consideration.

Another consideration is in the manufacture, especially if and how flip chip based packaging can be implemented and possibly be used to partially or fully supplant wire bonds at ILH.

2. Theory

2.1. Selected Planar Transmission Line Geometries

The constraints of chip design and packaging necessitate the use of planar technologies to manufacture transmission lines. While technologies for planar manufacturing like photolithography can allow for excellent feature sizes, the constraint of being limited to 2 respectively 2.5 dimensions does introduce certain non-idealities that can lead to distortion. Particularly open or partially open structures also tend to radiate with increasing frequency and thus have to be evaluated for their suitability in the given frequency range.

2.1.1. Stripline

The first planar transmission line that was developed historically is called stripline. Similar to coaxial cable the center conductor is fully enclosed in a dielectric. Different to coaxial structures the center conductor has a rectangular cross section and while the center conductor is shielded by outer conductors at the top and bottom, the sides are open. Because of this configuration fringing fields are a significant part of the first mode of propagation. Similar to coaxial cable, the homogeneous distribution of the dielectric material and there being two conductors lead to the first mode of propagation being transverse electromagnetic (TEM) [4, pg. 141]. Due to the similarity of striplines to rectangular waveguides, higher order modes can propagate. The cutoff frequency of these higher order modes can be increased by reducing the spacing of the outer conductors. According to [4, pg. 141] the higher order modes can be avoided entirely by choosing the spacing of the outer conductors b to be less than half of the smallest wavelength in the material $\frac{\lambda_d}{2}$.
Losses in striplines are mainly caused by a non-zero loss tangent of the dielectric and a finite conductivity and surface roughness of the center and outer conductors. Due to the enclosed nature of striplines, radiation loss is almost zero and mainly occurs at the interfaces to other structures.

Figure 2.1 shows an example stripline topology with the electric and magnetic field of the fundamental mode.

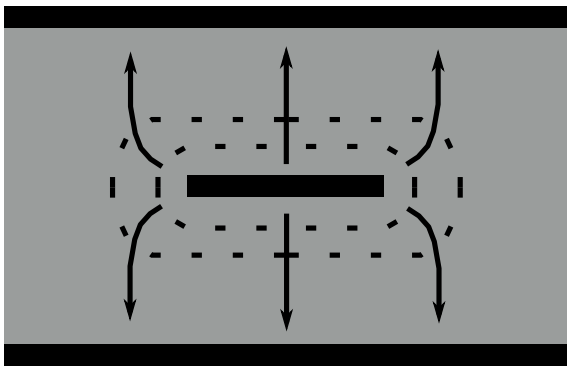


Figure 2.1.: Fundamental TEM mode of a stripline, the electric field is indicated by the solid lines and the magnetic field by the dashed lines (adapted from [4, pg. 141])

To achieve good matching, the line impedance of two subsequent structures should ideally be the same. Assuming a thin center conductor the line impedance Z_0 of a symmetric stripline depends on the outer conductor spacing b, the relative permittivity ϵ_r and the width W of the center conductor as follows [4, pg. 142]:

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_r}} \frac{b}{W_e + 0.441b}$$

With the effective width [4, pg. 143]:

$$W_e = \begin{cases} 0 & for \frac{W}{b} > 0.35 \\ (0.35 - \frac{W}{b})^2 & for \frac{W}{b} < 0.35 \end{cases}$$

This leads for a target impedance of 50 Ohm with a dielectric constant of 3 and a conductor spacing of 250 μm to a width:

$$W = b * (\frac{30\pi * [\Omega]}{\sqrt{\epsilon_r} Z_0} - 0.441) \approx 162 \mu m$$

Low conductor widths increase the influence of production tolerances as the relative change of the width increases for smaller widths for the same absolute tolerance. In addition to that striplines require three conducting layers. As the center conductor is shielded from the outside, probing the center conductor also proves challenging if not impossible. In PCBs the layer thickness also varies with the fabrication which would make striplines asymmetrical. These limitations cause striplines to be uncommon for use in PCBs. Their property of providing a TEM mode with very good wave confinement while suppressing higher order modes makes striplines interesting for the highest of frequencies, an example for a transition in the range of 500 GHz is detailed in [5]. However as this work deals with base band and intermediate frequencies with a frequency range of up to 100 GHz, the practical and economical limititations of striplines take precedence and thus striplines are not further discussed in chapter 3.

2.1.2. Microstrip Line

Microstrip line is one of the most popular choices to realize a transmission line with planar manufacturing technologies. Contrary to stripline, there is only one outer conductor layer with the other side instead being open to another dielectric, often air. This reduces the capacitance per length, in turn allowing for and requiring larger conductor widths compared to striplines for the same line impedance. Figure 2.2 shows an example microstrip layout with the electric and magnetic field components of the fundamental QTEM mode.

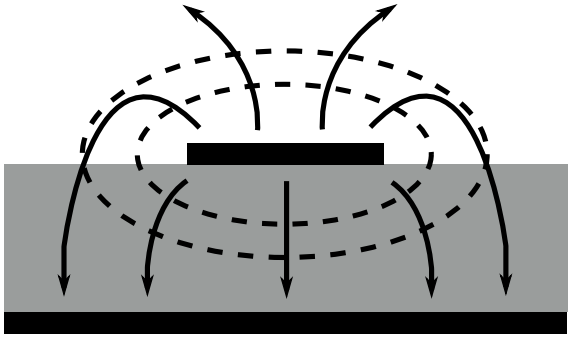


Figure 2.2.: Fundamental QTEM mode of a microstrip line, the electric field is indicated by the solid lines and the magnetic field by the dashed lines (adapted from [4, pg. 147])

This non-homogeneity for the dielectric materials leads to the fundamental mode having longitudinal components in both electric and magnetic field. For low frequencies their contribution to the total energy in the travelling wave is negligible [4, pg. 147], hence the fundamental mode of a microstrip is called quasi TEM (QTEM). According to [4, pg. 147], the actual fields constitute a TM-TE hybrid wave and describing it as QTEM only holds if the electrical thickness of the dielectric d is much smaller than the wavelength $d \ll \frac{\lambda_0}{\sqrt{\epsilon_r}}$ with λ_0 being the vacuum wavelength of the wave that is propagating. Another problem that arises when using microstrip is its tendency to radiate at higher frequencies. Research by P.B. Katehi and N.G. Alexopoulos (1985) [6] suggests discontinuities to be major contributors to microstrip radiation loss and according to G. Pan and J. Tan (1993) [7] this radiation loss has a maximum where the thickness of the dielectric is equal to $\frac{\lambda_0}{4\sqrt{4\epsilon_r}}$. Hence it can be expected that radiation loss increases up to that point. For a 250 μm thick substrate with ϵ_r of 3 this amounts to a frequency of approximately 173 GHz which is far beyond the considered frequency range of this work. Still, it can be expected for radiation losses to be a particular problem at transitions. Similar to striplines dielectric losses and metal losses also occur due to non-ideal materials with microstrip lines. Due to the generally larger dimensions these losses can however be expected to be smaller. Additionally the dielectric losses in particular are also smaller as part of the field is in the air which has a loss tangent that is virtually zero.

Comparing the required widths of microstrip lines to striplines can be done by taking a look at the line impedance of microstrip lines. According to [4] under the assumption of the width of the microstrip line w_{micro} being more than twice as large as the thickness of the dielectric d the width for a given characteristic impendance is:

$$w_{micro} = d \cdot \frac{2}{\pi}[B - 1 - ln(2B-1) + \frac{\epsilon_r - 1}{2\epsilon_r}\{ln(B-1) + 0.39 - \frac{0.61}{\epsilon_r}\}]$$

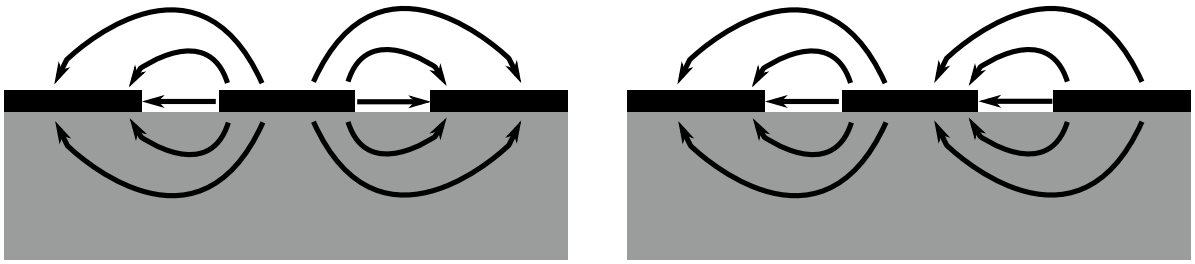
with

$$B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}}$$

For a 250 µm thick dielectric with ϵ_r of 3 and Z_0 of 50 Ω this amounts to a width of the transmission line $w_{micro} \approx 630\,\mu m$ which is much wider than that of a stripline of the same impedance. It is easier to probe microstrip lines than striplines as the conducting strip is exposed, however accurate probing still requires a connection to the conducting plane. A transition to a geometry such as coplanar waveguide is used in practice for on-wafer probing [8].To reduce reflections and obtain a more accurate measurement result, probing should be done only in the parts of the circuit where the line impedance approaches close to 50 Ω as most probes are manufactured with a line impedance of 50 Ω [8]. Another issue that can arise with microstrip lines is the coupling of unwanted signals originating from other parts of the circuit. Of particular importance with regards to this phenomenom are the modes found in grounded dielectric slabs [4, pg. 135 ff] that have a cutoff frequency and become increasingly important at higher frequencies or for larger thicknesses of the dielectric. However, the straightforward accessibility of microstrip lines on PCBs, ease of manufacturing, as well as resilience to production tolerances makes microstrip transmission lines interesting for consideration in the mmWave frequency range and they are the first structure that is investigated in chapter 3.

2.1.3. Coplanar Waveguide

As mentioned in the previous section another common planar transmission line geometry is the so called coplanar waveguide (CPW). While pure CPW is rare in PCBs, it is a common topology in chips. Additionally, there are numerous topologies that can be derived from CPW [9] and some of those like grounded CPW are commonly used in PCB.
In CPW the center conductor is flanked by two outer conductors on the same layer. An example layout with corresponding field components is shown in figure 2.3.



(a) Even mode **(b)** Odd mode

Figure 2.3.: Even and odd QTEM modes of a CPW, the electric field is indicated by the solid lines (adapted from [10])

The description of coplanarity stems from all conductors being on the same layer. All three conducting strips are placed on a dielectric and when realized in PCBs the upper dielectric above the conducting layer and between the conductors is usually air. Apart from the desired even mode, the CPW also supports a parasitic odd mode [10]. Exciting the odd mode from the even mode can induce additional losses which can happen at unequal discontinuities such as bends [10]. When the distance is smaller than the height of the conducting layer, the overall field has a large component that is homogeneous which in turn would simplify calculating the associated line impedance. However due to manufacturing tolerances in PCBs this is generally not the case and the distance between the conductors is larger than the height of the metal layer [11]. Hence a large part of the energy of the even mode is in the fringing fields which necessitates numerical methods to obtain accurate results. Similar to microstrip lines the obtained even and odd modes of propagation are QTEM due to the difference in electric permittivity of the different dielectrics. The pure CPW also has no other conducting structures apart from the three conducting strips. This makes CPW straightforward to use for creating vertical connections without changing the mode significantly as the outer strips can be routed in parallel to the center strip. Similar to microstrip lines, the modes found in grounded dielectric slabs are important parasitics in CPW.

2.1.4. Grounded Coplanar Waveguide

Combining the geometries of microstrip and CPW leads to a CPW with a grounded plane on the other side of the substrate dielectric. The result is called grounded CPW (GCPW). Due to the lower metal plane being tangential to the electrical field of the corresponding odd mode in a pure CPW without the lower metal plane, the odd mode is suppressed in GCPW. Figure 2.4 shows the fundamental mode of an example GCPW with vias.

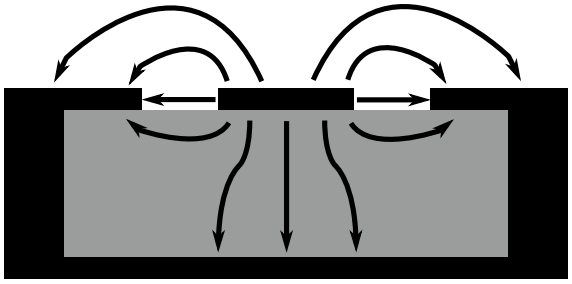


Figure 2.4.: QTEM mode of a GCPW, the electric field is indicated by the solid lines (adapted from [12])

Parallel plate modes [4, pg. 102 ff] can propagate as parasitics. The use of vias connecting the outer conductors on the upper plane with the lower plane allows the suppression of these parallel plate modes. Another parasitic mode that can propagate at higher frequencies is a parasitic rectangular waveguide mode and the conductor width and dielectric thickness should be chosen to keep it in the cutoff region [9, pg. 107 ff]. Due to the partially enclosed structure, GCPW has better wave confinement and thus lower radiation losses than both microstrip and CPW. Similar

to microstrip and CPW, the fundamental mode is QTEM and similar to CPW requires numerical computation to obtain an accurate result for the line impedance. The resilience of GCPW to parasitic signals originating from other parts of the circuit makes it interesting for RF applications and most structures investigated in chapter 3 are based on GCPW geometries.

2.2. Flip Chip Processing

To evaluate the suitability of flip chip bonding techniques for the bonding in the frequency range of up to 100 GHz, a look at the state of the art of flip chip processing is required. In this section an overview of flip chip process flow, requirements and differences to wire bonding is given.

2.2.1. Process Description

While there are many different ways to achieve a flip-chip bond, in most cases for bonding chips that are operating above 1 GHz the basic process involves the use of conductive bumps. The first step is to create the bumps. Depending on the material this can be a wafer-level process or an assembly-level process. After depositing the bumps on the chip, next follows the actual bonding of the chip to the substrate, often a PCB. The bonding step is dependent on the bump material and can for example be achieved by first aligning and putting the chip on the bond pads of the substrate and then reflow soldering if a solder is used as the bump material. Other bonding techniques include thermosonic bonding and thermocompression bonding. As the chip often has a different thermal expansion coefficient than the substrate material, for large chips this puts mechanical stress on the bumps if the system experiences a change in temperature, affecting the lifetime of the system. To alleviate some of the stress acting on the bumps, a filler material called underfill is commonly used. According to [13] this underfill provides no significant additional mechanical benefit if more than 25% of the distance from the edge of the chip to its center is coated. If an underfill is used then it is commonly applied after the bonding process through the use of capillary action and then an additional heating step for curing it. Figure 2.5 shows an example flip chip process utilizing bumps made of solder.

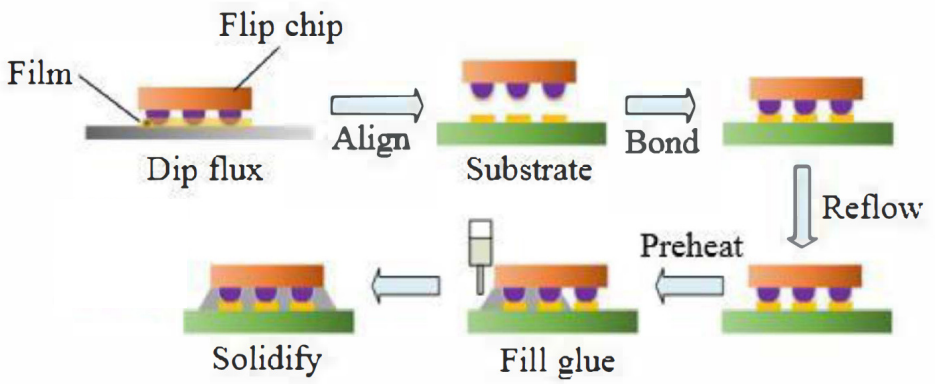


Figure 2.5.: Process flow of an example flip chip process using solder bumps (adapted from [14])

Underfill materials are commonly epoxy resins. An example epoxy resin given in [15] has a loss tangent at 1 GHz in the order of 0.03 which is an order of magnitude larger than that of Rogers 3003 as given in [16]. Hence to keep dielectric loss low, large lengths of transmission lines in underfill materials should be avoided.

Other flip chip techniques include the use of anisotropic conductive film where small spheres coated in gold are suspended in a non-conducting resin. This technique allows the underfill to be applied before the bonding step. However due to the aforementioned high loss tangent of epoxy resins this technique may not be preferred for applications in the mmWave range. Another flip chip technique using non conductive films encounters a similar issue with the use of epoxy resins for the full area. Hence only techniques utilizing conductive bumps are further investigated in this work. As the specifics of the bonding step are dependent on the type and material of the bump, a further look at the manufacturing of the bumps is necessary and is given in the next section.

2.2.2. Bumping Techniques

As mentioned in the previous section, bumps can be manufactured in a wafer-level process or an assembly-level process. Wafer-level processes typically add the bump at the end of the back end of line. Current state of the art wafer-level bumping processes include screen printing, evaporation and electroplating. Screen printing is cheap and allows for straightforward prototyping, but suffers from large process variations, low yield and is limited in resolution. Evaporation uses a metal mask to first evaporate an under bump metallurgy (UBM) on the bond pad and then evaporates a lead-rich solder on the UBM. Next the metal mask gets removed and a reflow step to form the bump follows. While yield is good for evaporation based bumps, the minimum pitch is limited by the metal mask. Additionally, using lead-rich solder makes them not compliant with regulations limiting the use of lead in electronics which may limit their widespread use. An additional constraint is the need to clean the metal masks of evaporation residue. Finer pitches that are theoretically only limited by the lithographic process are possible by using electroplated bumps. Here a photoresist is applied and structured after depositing the UBM. Subsequently, the solder is electroplated onto the UBM. The photoresist is then removed and the now exposed UBM etched to prevent to the solder from flowing laterally during reflow. After this comes the reflow soldering step to achieve a uniform bump. Figure 2.6 shows the major process steps of an electroplated bumping. (adapted from [17])

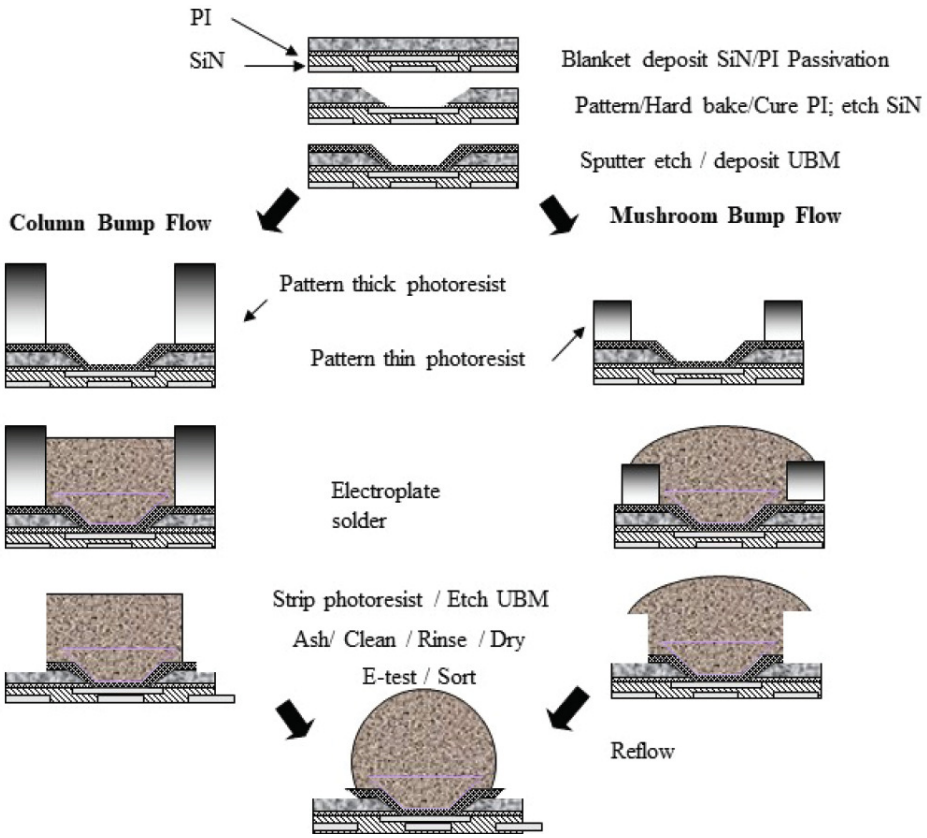


Figure 2.6.: Process flow of electroplated solder bumps (reproduced from [17])

Another wafer-level process utilizing electroplating can be achieved by first electroplating copper to the UBM and then a thin layer of solder on top to achieve the bond. The resulting structure is called copper pillar. Figure 2.7 shows the changed process steps. (adapted from [17])

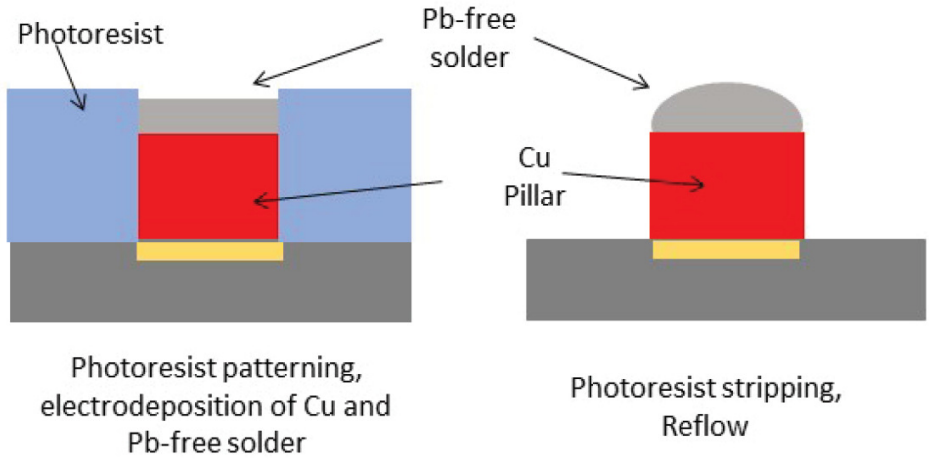


Figure 2.7.: Changed process steps of electroplated copper bumps (reproduced from [17])

[18] demonstrated copper pillars of up to 170 µm height with an aspect ratio of at least 4:1. One issue that can arise with copper pillars is that they might corrode if exposed for extended periods

of time which is similar to the corrosion in PCBs.
Assembly level processes function similar to wire bonding. The use of gold bumps is common which are made with wire bonding machines by cutting off the wire after placing the initial bump. To improve bump uniformity the gold bumps can be coined during which the bumps get flattened by the wire bonder. To increase the total bump height it is possible to stack gold bumps on top of each other. [19]
Achievable minimum bump diameters for gold bumps are in the range of 50 µm [20].

2.2.3. Comparison to Wire Bonding

Wire bonding is an assembly-level process. Particularly for many bond pads, flip chip can achieve finer pitches and be more robust as the distance between neighboring bonds depends only on the pitch and not the shape of the wire of a wire bond. Chip-on-board packages may require more tightly controlled production tolerances in PCBs and a resolution in the order of the pitch for flip chip compared to wire bonds. An interposing package can be used to achieve a wider pitch to allow for less tightly controlled PCB production tolerances, an example using through silicon vias was reported by X. Ren et al. (2013) [21]. Thermal expansion and subsequently device reliability is an additional challenge in flip chip over wire bonds.
Particularly of interest for RF-applications, flip chip bonds have a much reduced bond length compared to wire bonds and subsequently less inductance caused by the bond. An estimate for the inductance of a 25 µm thick bond wire is 1 nH per mm length [22].
For chips with many bond pads wafer-level processes may allow for larger throughput than assembly-level processes as the bonding process can be parallelized more easily, for example by the use of a reflow process for bonding.

2.3. Materials

In this section an overview of the different materials that are used in the simulations in chapter 3 is given. A particular focus is on the non-idealities and how they are approximated in the simulation program CST Studio Suite 2020.

2.3.1. Metals

Metals are approximated with the so called Lossy Metal model [23]. The Lossy Metal model approximates the material characteristics of the metal by forgoing a volumetric simulation in favor of assuming an equivalent surface impedance. This is done to reduce simulation times as the mesh does not have to be refined inside the metal and is accurate as long as the metal thickness is much higher than the skin depth. The documentation for the simulation program [23] offers an estimate for the range of validity with the lower end of the frequencies:

$$\omega \gg \frac{2}{\mu_0 \mu_r \sigma (Factor \cdot d)^2}$$

In the documentation the factor is chosen as 0.2. For a thickness of a metal $d = 4\,\mu m$ and a conductivity $\sigma = 3 \cdot 10^7 \frac{S}{m}$, this results in an estimate of the lower end of the range of validity of $f \gg 13.2\,GHz$ and for a thickness $d = 10\,\mu m$ this results in $f \gg 2.1\,GHz$. In table 2.1 the relevant physical characteristics of the metals used in the electrical simulation in chapter 3, namely gold, tin and copper, and the broader materials considered for fabrication. The data is taken from [23] except for the thermal expansion coefficient of molybdenum, all data for indium and the melting points for all materials which are taken from [24] instead.

	Au	Sn	Cu	Mo	Ni	In
Electrical conductivity in $10^6 \frac{S}{m}$	45.61	8.6957	58	18.2	14.4	12
Relative permeability	1	1	1	1	600	1
Thermal conductivity in $\frac{W}{K \cdot m}$	314	66.6	401	142	91	82
Thermal expansion in $10^{-6} K^{-1}$	14	20	17	4.8	13.1	32.1
Melting point in °C at 1 bar	1064	232	1084	2623	1455	156.6

Table 2.1.: Electrical and thermal material parameters for the metals

Previous experience at ILH suggests a value of $3 \cdot 10^7 \frac{S}{m}$ for the conductivity of gold to obtain more accurate results [8].

2.3.2. Dielectrics

Dielectric losses are modelled with the respective loss tangent. A non-zero loss tangent also causes a frequency dependence of the relative permittivity which is modelled in the simulation program [23]. This dispersive property can be neglected for sufficiently small loss tangents however. The loss tangent and dielectric constant are assumed to be constant over the entire frequency range. In table 2.2 the electrical and thermal material parameters for the dielectrics used in the simulation, namely fused silica (SiO_2), also called fused quartz, alumina (Al_2O_3), Rogers 3003 (RO3003), gallium arsenide (GaAs) and air, as well as high-resistance silicon (Si) for a broader consideration. Unless noted otherwise the data is taken from [23].

	SiO_2	Al_2O_3	RO3003	GaAs	Air	Si
Relative permittivity	3.75	9.9	3	12.94	1	11.9
Relative permeability	1	1	1	1	1	1
Loss tangent	$4 \cdot 10^{-4}$	$1 \cdot 10^{-4}$	$1 \cdot 10^{-3}$	$6 \cdot 10^{-3}$	0	n/a**
Thermal conductivity in $\frac{W}{K \cdot m}$	5	30	0.5	54	0.026	148
Thermal expansion in $10^{-6} K^{-1}$	0.5	7.9	17*[16]	5.8	n/a	5.1

Table 2.2.: Electrical and thermal material parameters for the dielectrics
*Expansion in one direction, overall expansion is anisotropic, but stays in the same order
**Losses in Silicon are modelled with a conductivity, an example for a high-resistance silicon is 0.0014 $\frac{S}{m}$ [25]

3. Simulation

The cost of manufacturing even small runs of contemporary integrated circuits (IC) is significant. The fabrication also takes significant time. Packages typically have a lower complexity than the most advanced ICs. However, accurately measuring the overall system of a given package and a given IC and comparing the impact of different packages requires putting both IC and package together. For this reason simulations are powerful tool not only for the design of chips, but also for the design of the package as they allow gauging how a system would behave prior to fabricating it. In this work several approaches to flip chip packaging were investigated and the simulation results are presented in this chapter. CST Studio Suite 2020 was used as the simulation software. The frequency domain solver [23], which uses finite element method (FEM) approach, was used for most simulations due to the faster simulation time, the possibility of using a tetrahedral mesh and optimisation for resonant structures. Some simulated structures were further verified by using the time domain solver [23], which implements a finite integration technique (FIT) and uses a hexahedral mesh. However, due to the time domain solver being constrained to the use of a hexahedral mesh, if both large and small structures are present in a simulation, the meshing becomes challenging. Both solvers allow for 3D full-wave calculation. Unless noted otherwise for all simulations presented in this chapter

- the material of the lateral metal layers is gold as detailed in section 2.3.1 with the approximation for the conductivity $\sigma = 30 \cdot 10^6 \frac{S}{m}$,
- the material for the bumps is tin as detailed in section 2.3.1 and the material for the PCB dielectric is RO3003 as detailed in section 2.3.2 and is 250 µm thick,
- the bumps are cylindrical in shape, the planar metal layers consist of cuboids
- and the boundary below the backside metallization of the PCB, is a perfect electrical conductor (PEC).

Additionally, the associated tolerances in PCB manufacturing depend on the process, but generally prevent distances below 60 µm between conductors. Hence, for the PCB pad to have a similar dimension to the bumps and the pad on the chip side near the transition the line impedance deviates from 50 Ω. As a consequence to achieve 50 Ω a taper is required to keep return loss low. Tapers on the PCB side can be simulated with 2.5D simulators and do not require a 3D simulator for accurate results [8]. Taper dimensions are in the order of the wavelength and are thus much larger than the transitions that are discussed in this chapter if they are also to include the lower end of frequencies. So a taper would increase simulation size significantly while not being required to be simulated with 3D methods. For this reason the author of this work chose to omit the taper on

the PCB side. Consequently the feeding port on the PCB side deviates from 50 Ω line impedance in some of the simulations shown in this chapter.

As simulations always assume simplifications over reality, some limitations of the simulations shown in this chapter are discussed in section 3.4. All simulations that are presented in this chapter were developed and simulated during this thesis.

3.1. Regular Flip Chip

The first structure that was investigated within the framework of this thesis is a regular flip chip transition. The chip is flipped and so faces upside down compared to wire bonding techniques. This approach is widespread in contemporary packaging for low-frequency applications with many bondpads. Its most basic form was first developed by General Electric in 1963 [26]. The regular flip chip transition with microstrip lines on both the chip side and the PCB side is shown in figure 3.1. The material used for the dielectric on the chip side is GaAs with the material parameters according to section 2.3.2. As mentioned in section 2.2 for mechanical stability an underfill is required. According to the discussion in section 2.2 it is reasonable to assume that the material at the transition is air, as according to [13] only 25% of the length from the edge of the chip to its center is required to be covered by the underfill to achieve the full benefit for mechanical stability. Choosing air at the transition has the benefit of simplifying the simulation and reducing losses.

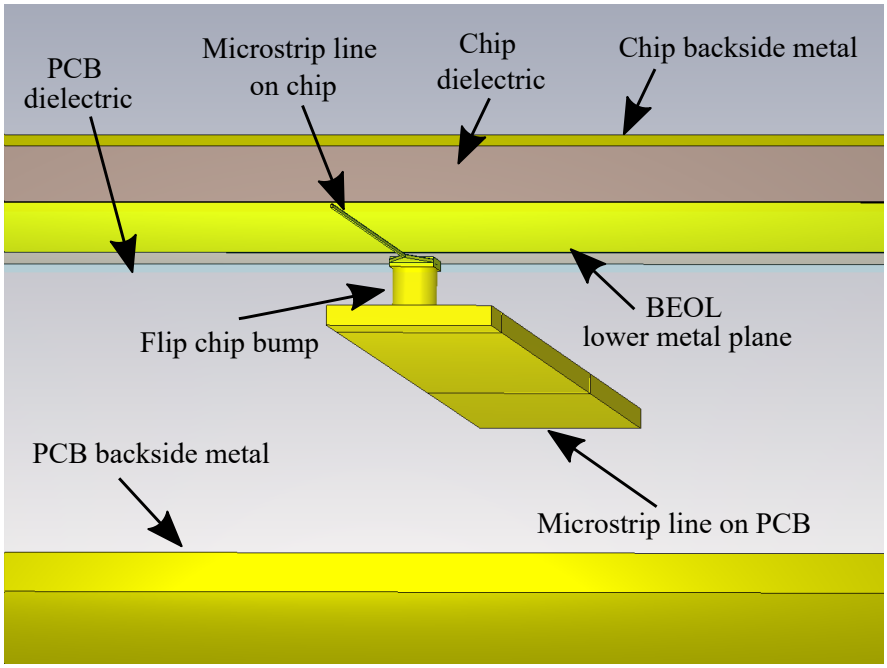
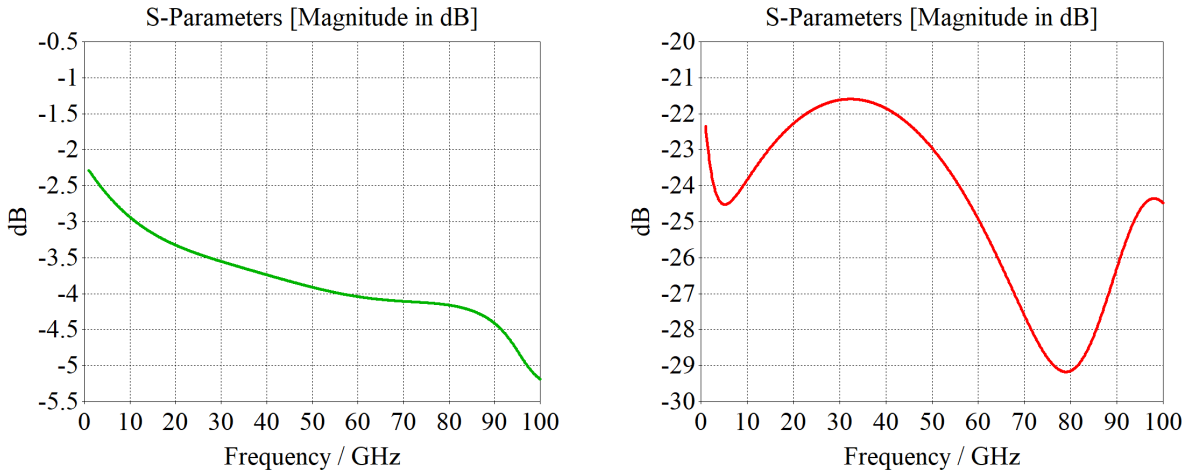


Figure 3.1.: Model of the regular flip chip transition in CST.
View is from below, to improve visibility dielectrics on the PCB and on the BEOL of the chip are transparent.

The results for the S-Parameters of the simulation of the structure shown in figure 3.1 can be seen in figure 3.2.



(a) S21 **(b)** S11

Figure 3.2.: Simulation results of the regular transition with microstrip line on the PCB.

While the return loss is lower than -21 dB for the range of up to 100 GHz, the insertion loss of this regular flip chip transition using microstrip on the PCB side is significant. The insertion loss at 1 GHz is about 2.25 dB, while this increases up to 5.2 dB at 100 GHz. The main contributor of the insertion loss is radiation. Figure 3.3 shows the overall power of the part of the excitation lost to radiation. Power accepted (blue) is the sum of power lost to metal losses (green), dielectric losses (red) and radiation.

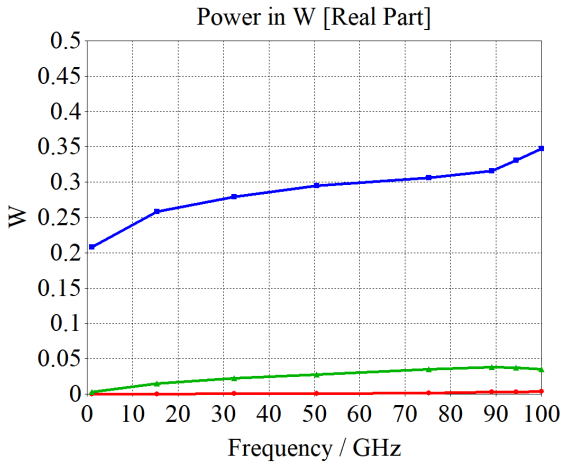


Figure 3.3.: Power accepted by the structure resulting in radiative losses. Excitation is with 0.5 W.

Radiation occurs particularly strongly at the transition to the chip. There the QTEM mode of the microstrip line spreads along the transition and excites modes between the PCB substrate and the chip. This behavior can be explained by the energy of the wave in a microstrip mode being

concentrated in the dielectric. This explanation is also in line with the finding of discontinuities being major contributors of radiation loss in microstrip that was discussed in section 2.1.2 with the flip chip transition being one such discontinuity. Figure 3.4 shows the power flow at 50.5 GHz of a cutting plane normal to the z-axis cutting the upper conductor of the PCB exemplifying this radiative behaviour.

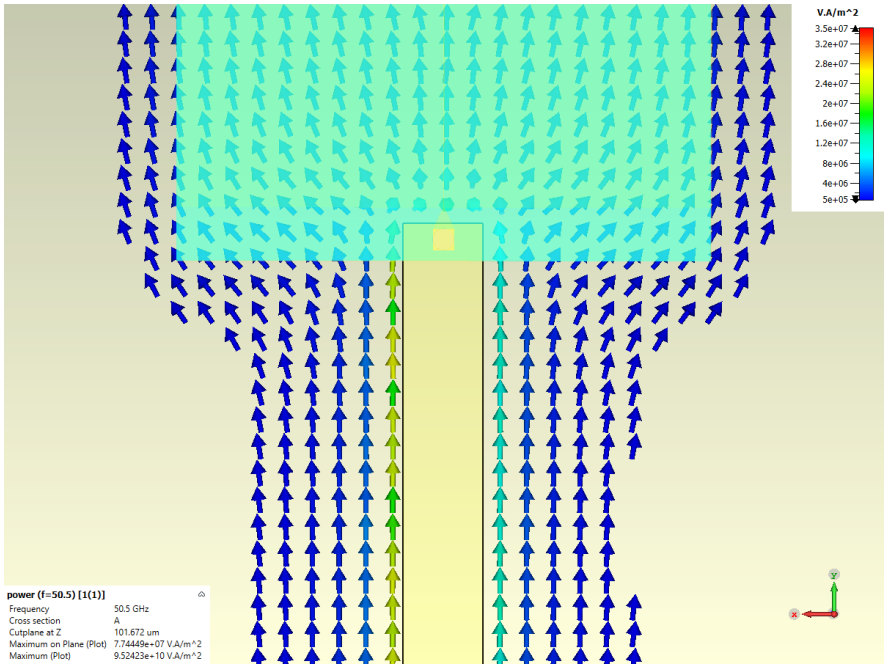


Figure 3.4.: Power flow at 50.5 GHz showing the radiative behaviour of the microstrip line at the flip chip transition.

The high insertion loss of the microstrip line structure shown in figure 3.1 at microwave and mmWave frequencies makes it unattractive as a packaging solution for the given frequency range. The excitation of substrate modes is also unwanted as in addition to causing loss, they could also interfere with the operation of the chip. However, instead of microstrip line, GCPW can be used as the transmission line on the PCB side. Different to the microstrip line transition, there are three bumps to account for both the center conductor and the two outer conductors. Additionally the outer conductors on the chip side are connected to the lower metal plane of the microstrip line on the chip side and a small taper is realized between the bondpad and the microstrip. Figure 3.5 shows the adjusted transition with a GCPW on the PCB side.

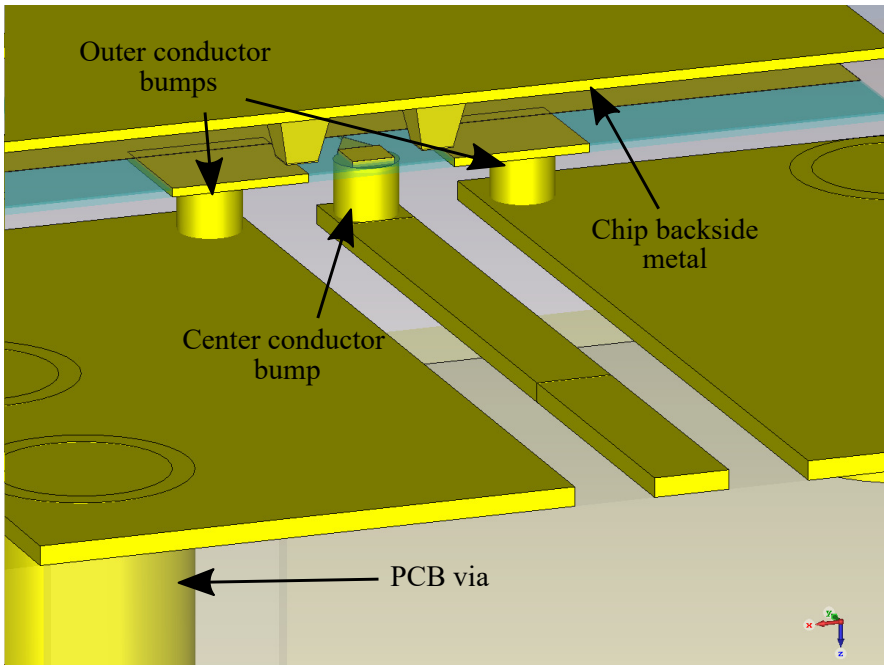
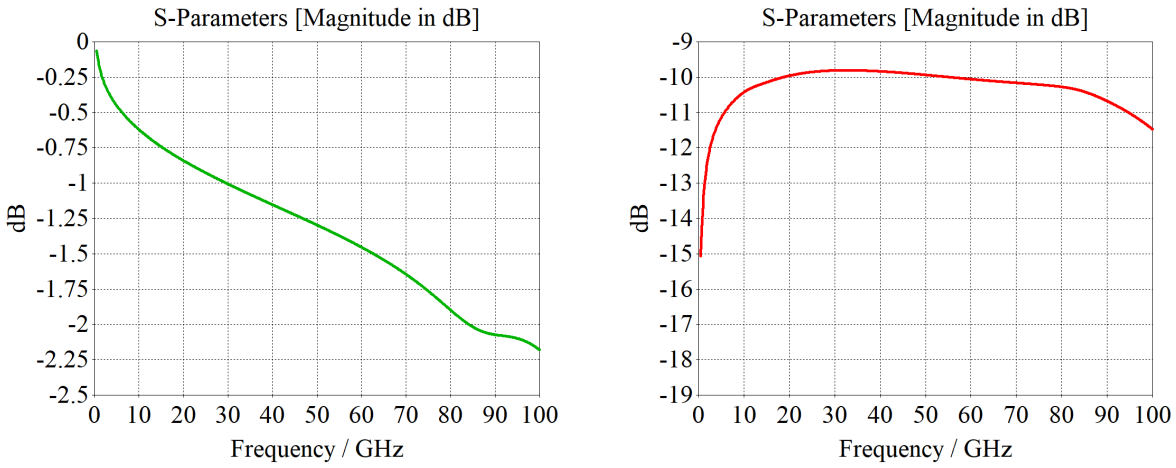


Figure 3.5.: Regular flip chip transition with GCPW on the PCB side

The resulting S-parameters of the regular flip chip transition with GCPW on the PCB side are shown in figure 3.6.



(a) S21 **(b)** S11

Figure 3.6.: S-parameters of the regular flip chip transition with GCPW on the PCB side.

The transition using GCPW on the PCB side has much lower insertion loss than the microstrip line transition with 2.2 dB at 100 GHz. Return loss peaks at -9.8 dB at 32.5 GHz. The reason for the lower insertion loss is the lower radiation of the structure which results from the CPW-part of the mode on the GCPW being continued throughout the transition. A simulation result showing the power flow analogous to the microstrip line transition is shown in appendix A.1. Radiation loss is two orders of magnitude lower than in the microstrip transition. However, the flip chip transition

is not the only cause of subtrate modes that are in danger of interfering with the chip. Parasitic signals can also originate from other parts of the PCB, such as from DC lines acting as antennas parasitically. One way to combat the issue of parasitic substrate modes was proposed by M. Ito and T. Marumoto (2019) [27] by introducing vias below the flipped chip. Another problem with a flipped chip is that it is challenging if not impossible to probe on-chip after the flip chip process as the gap between the PCB and chip is too small for a probe. It is also challenging to realize functioning BEOL on-chip antennas on a flipped chip is the radiated signal has to travel through the PCB first. While Beer et al. [28] propose putting the antenna on the substrate, this would require a flip chip transition for the frequency range that is radiated from the antenna, which could be beyond the frequency range of this work. Instead two approaches that use the same orientation as a wire-bonded chip - allowing for similar realization of BEOL on-chip antennas and on-chip probing - are discussed in the following sections.

3.2. Hot Via

F.J. Schmueckle et al. (2001) [29] proposed a different way to orient a chip using flip chip techniques: By transmitting the signal over vias drilled from the back side of the chip through to the upper side, the chip can be oriented in a similar way to a wire bonded chip. The interconnect using flip chip techniques is on the back side of the chip and requires a structuring of the back side metal layer. Both the transition from the PCB to the chip and the transmission over the so called hot vias is realized in CPW. On the upper side of the chip the CPW mode transitions similarly to the GCPW approach in section 3.1 to a microstrip line mode. Figure 3.7 shows the hot via transition.

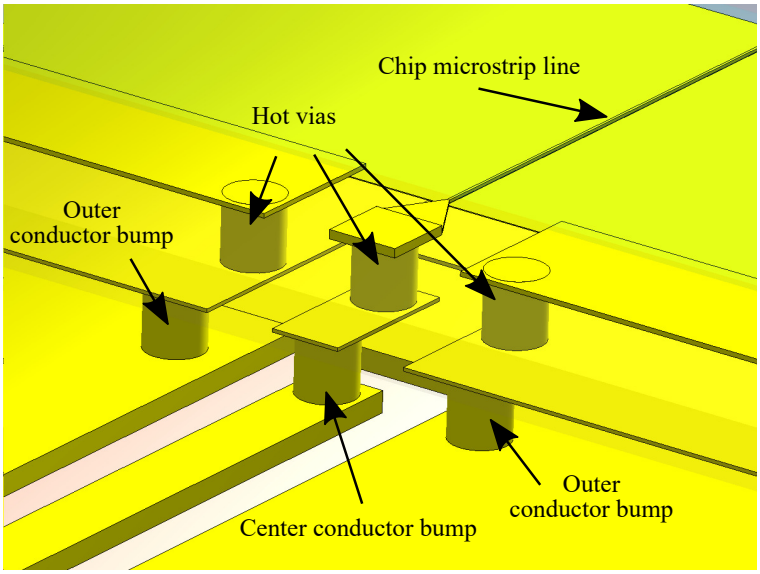
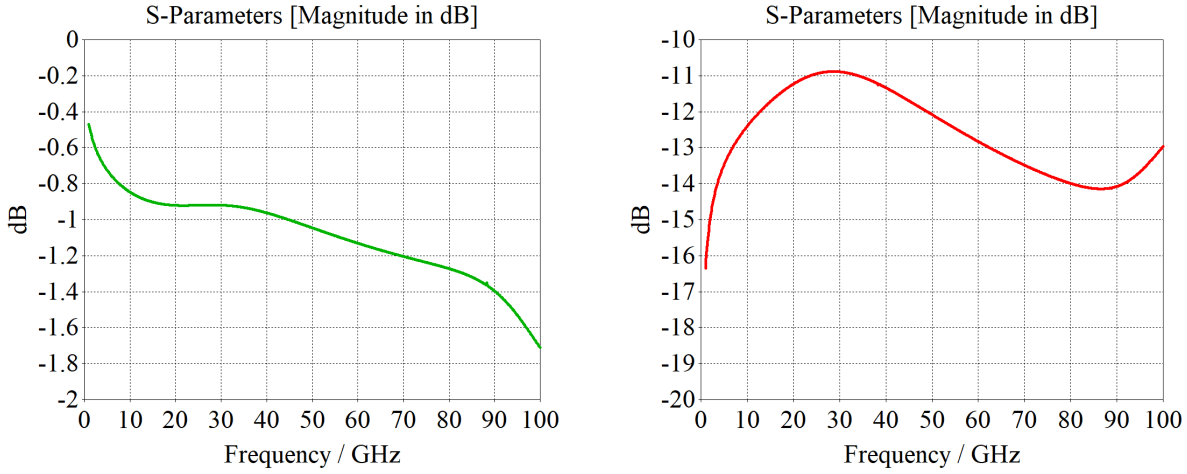


Figure 3.7.: View of the metal connections in the hot via approach, notably the vias are buried inside the chip substrate material

The simulated S-parameters can be seen in figure 3.8.



(a) S21 **(b)** S11

Figure 3.8.: S-parameters of the hot via approach with a PCB center conductor width of 80 µm and a distance between center and outer conductors of 60 µm.

Insertion loss is lower than for the regular GCPW flip chip transition discussed in the previous section with 1.7 dB at 100 GHz. The return loss for the parameters depicted is also below -10 dB in the frequency range of 1 GHz to 100 GHz. A detailed parametric analysis of changing center conductor widths and distance between center and outer conductors is shown in the appendix A.2. As the active components of the chip are shielded by the backside metallization of the chip, substrate modes of the PCB are less of an issue. Additionally the upward orientation allows for BEOL on-chip antennas and on-chip probing.

Similar to the regular flip chip transitions discussed in the previous section for mechanical stability an underfill is beneficial. The underfill could be an epoxy resin as is common in regular flip chip technology or as proposed by A. Bessemoulin et al. (2016) [30] using solder. A challenge that occurs with the hot via approach is that the structure itself is difficult to verify. As the vias are surrounded by, at optical frequencies, opaque semiconducting material, regular optical microscopy can not be used to verify the shape of the vias. Similarly, scanning electron microscopy (SEM) is also not suitable for verification as it can only verify a surface. While it is feasible to etch the semiconducting material to reveal the vias, doing so would destroy the chip. Another constraint with the hot via approach is that it requires a lithographic step for structuring the backside metallization of the chip which might not be available for a given chip technology. The fabricated structure of A. Bessemoulin et al. (2016) [30] showed significant return loss of over -3 dB during measurement that was not indicated by the simulation. While A. Bessemoulin et al. (2016) [30] used active structures on their chip which could partly explain such a high return loss, the vias or the underfill could also be the cause of this reflection. Indeed, the actual shape of the hot vias might differ significantly from the cylindrical shape used in the simulation of this work and the simulations of [30]. The challenge of verification combined with possible process variations, particularly of the vias on the chip, and the requirement of a back side lithography constitute the main problems of the hot via approach. Another approach, designed to allow for straightforward verification and

not requiring a back side lithography step of the chip, is discussed in the following section.

3.3. Inverted GCPW on Intermediate Substrate

To allow for a chip orientation in the same direction as wire-bonding Y. Shi et al. (2019) [31] proposed the use of a high resistance silicon interposing substrate. Their process consists of two flip chip steps: First a gold ball flip chip bonding of the MMIC to the silicon interposing substrate and secondly a solder ball flip chip bonding of the silicon interposing substrate to the PCB. The frequency range of Y. Shi et al. (2019) [31] with a maximum simulated frequency of 24 GHz and a measurement at 2.4 GHz is far below the upper end of the frequency range investigated in this work at 100 GHz. However, the idea of using two subsequent flip chip bonding steps to achieve a similar orientation to wire bonded chips avoids the challenge of verifying vias inside the chip that the hot via approach has.
As indicated by the simulation of the regular flip chip transition using microstrip line on the PCB side as seen in figure 3.1, the strong radiation makes microstrip transitions at mmWave frequencies lossier when compared to a CPW-based transition. Additionally silicon is opaque at optical frequencies and prone to contamination by gold and copper. Furthermore the backside metallization of the silicon interposer proposed by Y. Shi et al. (2019) [31] would prevent straightforward observation after bonding.

Thus, the process proposed by Y. Shi et al. (2019) [31] can not be applied directly to the frequency range investigated in this work. However, to make the idea of using two flip chip steps and an intermediate substrate (IS) viable for the frequency range of up to 100 GHz, the author of this thesis proposes several changes:

Firstly, to achieve lower radiation losses, GCPW is chosen as the mode on the PCB side. The mode on the IS is proposed to use the PCB top metal layer as the lower plane in a mode resembling GCPW, but with the lower dielectric and air being exchanged with each other. Flip chip bumps are placed a steady distance apart from the center conductor to resemble the vias in a GCPW. Thus, the mode on the IS is referred to as inverted GCPW (iGCPW) in the following.

Secondly, as no semiconducting structures are necessary on the IS, the author of this work proposes to forgo the use of high-resistance silicon for the IS over a material with better electrical characteristics, lower cost and that is transparent or semi-transparent at optical frequencies. The main materials that were considered in this work for the substrate material are alumina and fused silica.

Thirdly, the deviation from silicon as the substrate material allows using different and cheaper processes than those used in the fabrication of silicon semiconductor devices. The author of this work particularly proposes the use of large area microelectronic processes (LAM) for the manufacture of the IS such as those used in display manufacturing. LAM are specialised in the processing, including the deposition and structuring of metal and isolating layers, on glass and other transparent solid materials over large areas and still allow for tolerances in the order of 1 µm [32]. Due to the possibility of manufacturing over areas in the range between 10 cm^2 to 1 m^2 [32]

LAM are also well suited for mass fabrication. To keep costs low in the structures that are proposed in this thesis there is only one metal layer requiring one to two photolithographic masks. Details on the possible fabrication, including two processes for manufacturing the IS proposed by the author of this work and a summation of critical tolerances derived from the simulations in the following sub sections, is given in chapter 4.

The IS in this work is called intermediate and not interposing, as the chip is first bonded to the IS before the IS is bonded itself to the PCB and so acts as an intermediate substrate for bonding. In the following the simulated electrical characteristics of the proposed structure are detailed.

3.3.1. Intermediate Substrate to Chip Transition

The structure introduced in this section consists of two main transitions. The first of these transitions is between the iGCPW on the IS and the CPW on the chip. This transition bears some similarities to the one demonstrated by P.V. Testa et al. (2019) [2], particularly the approximation of cylindrical shape of the bumps, using a CPW transition and the arrangement of a short height of the bumps. Differences include the use of the PCB as part of the main mode of propagation and the IS having larger dimensions than a chip.

Different to the hot via structure simulated in section 3.2 the chip for this chipset is approximated by a bondpad used for wire bonds and on-wafer probing in the sub-THz frequency range at ILH. The reason for this substitution is that this bondpad and especially the vias would have to be adjusted for the hot via structure, which was not possible within the framework of this thesis due to its proprietary nature and the process to fabricate that specific bondpad not being open to adjustment [8]. So while this bondpad could not be used for the hot via structure, it is used here to give a better approximation of the chips that were already fabricated at ILH [8]. The transition is shown in figure 3.9.

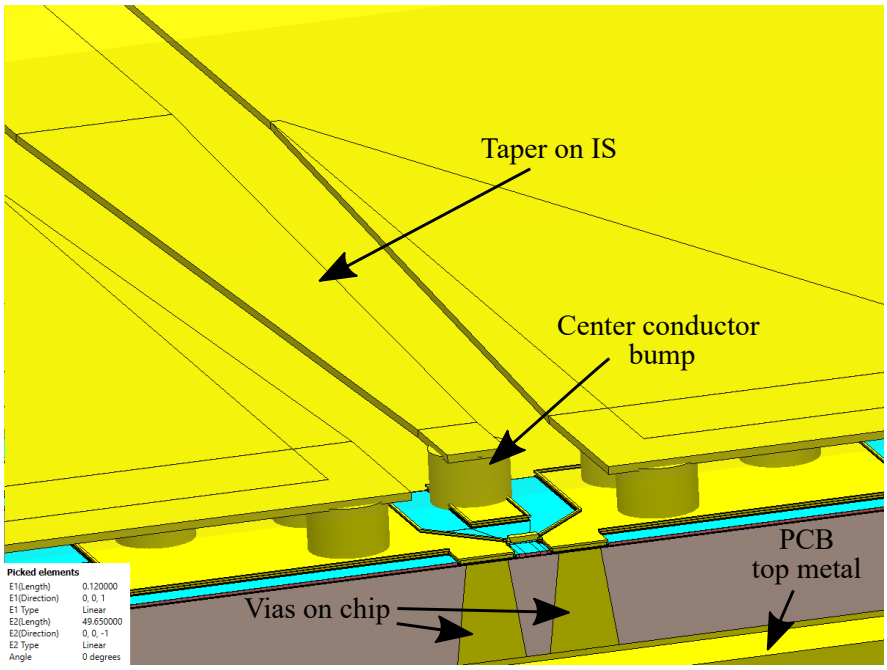
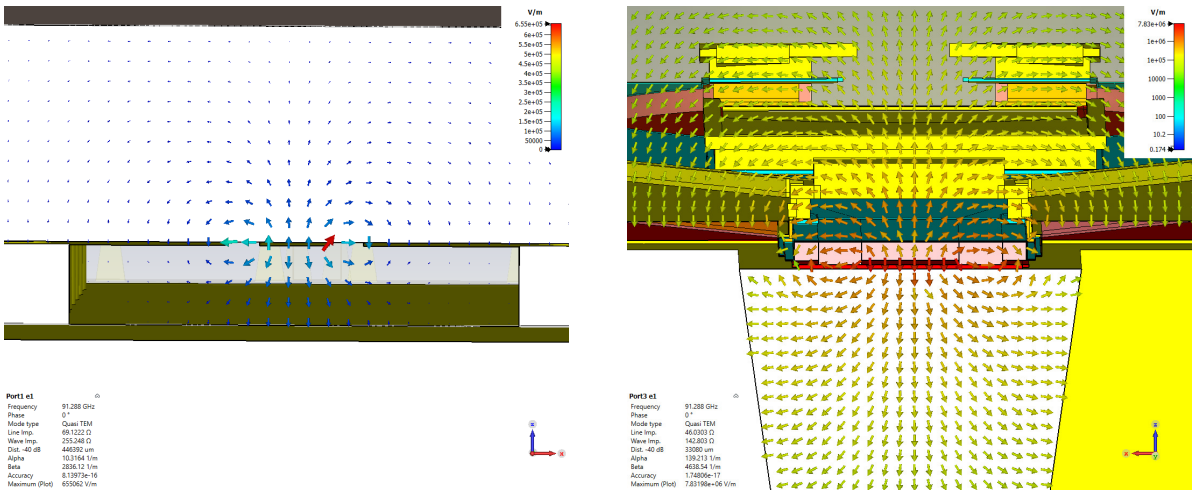


Figure 3.9.: View of the intermediate substrate to chip transition, the distance between chip and intermediate substrate is 20 µm. To approximate a single bump for the transition with a radius of 20 µm the IS dielectric material is transparent to improve visibility.

Field pictures of the port modes can be seen in figure 3.10.

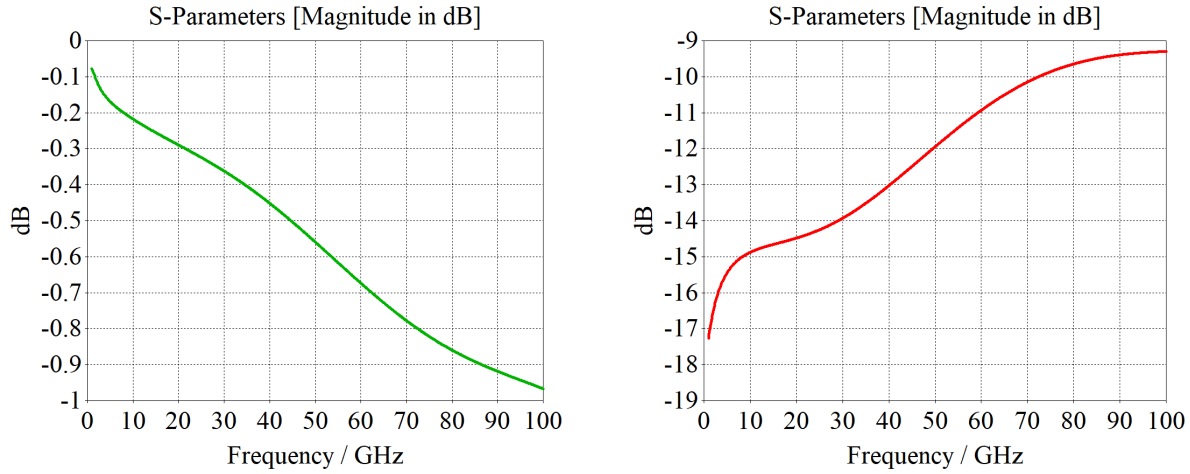


(a) **(b)**

Figure 3.10.: Pictures of the E-field of the QTEM mode on the intermediate substrate (a) and the CPW mode on the Chip (b) at 91 GHz.

The line impedance at the port of the chip is approximately 46 Ω. At the feeding port the line impedance is approximately 69 Ω. The IS is made of fused silica and is 250 µm thick. The distance between the center and outer conductors on the IS at the feeding port is 40 µm. This is reduced to 35 µm at the transition to the chip. The width of the center conductor at the feeding port is 80 µm

and this is tapered to 30 µm at the bondpad of the IS at the chip transition. The distance of the IS to the PCB surface corresponding to the height of the bumps connecting the two surfaces is 92 µm. The simulated S21 and S11 parameters of the structure in figure 3.9 are shown in figure 3.11.

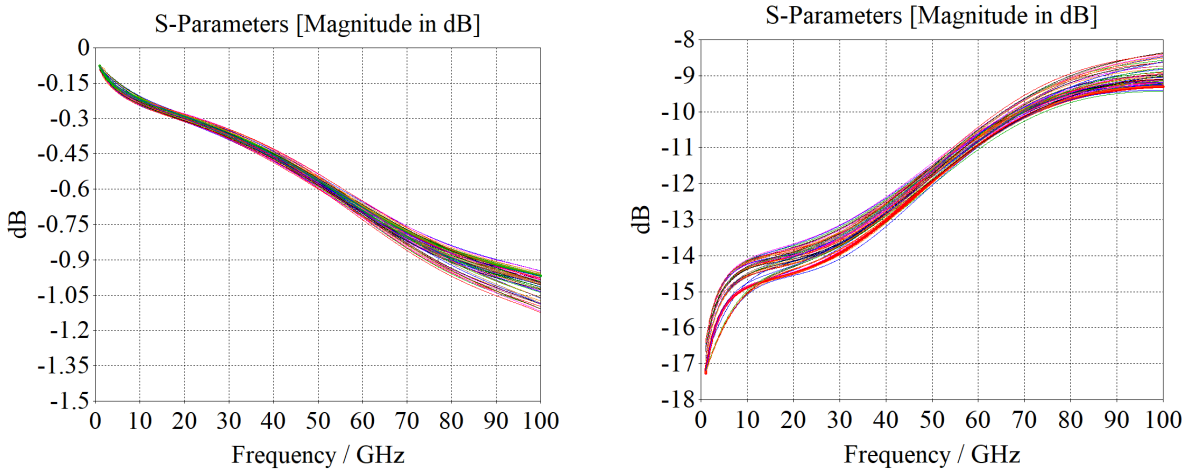


(a) S21 **(b)** S11

Figure 3.11.: S-parameters of the IS to chip transition shown in figure 3.9.

S11 remains below -10 dB until 72 GHz and reaches -9.3 dB at 100GHz. S21 has an approximately linear slope with respect to the representation in dB and indicates an insertion loss of 0.45 dB at 40 GHz and 0.96 dB at 100 GHz. The main contributors of insertion loss in this structure are reflection and metal loss, with radiation coming in third and dielectric loss being an order of magnitude lower. The graphs showing the different loss contributions in terms of power are shown in appendix A.3.

A parametric evaluation of the chip bump radii between 10 µm and 25 µm, the gap between PCB and IS with a 10 µm step size between 92 µm and 122 µm and the gap between the chip and the IS with a 10 µm step size between 10 µm and 40 µm is shown in figure 3.12.

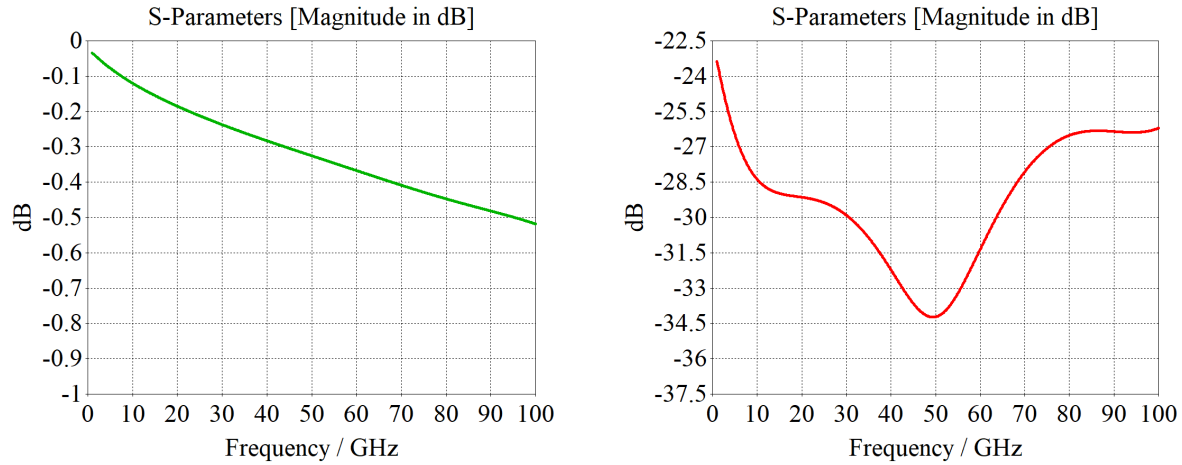


(a) S21 **(b)** S11

Figure 3.12.: S-Parameters of the parametric evaluation.

The spread for S21 is approximately 0.16 dB wide around a center at -1.03 dB at 100 GHz. The most significant contribution to return loss and consequently insertion loss is from the bump radii, particularly the bump radius of 25 µm. At this radius, the bumps connecting chip and IS are far wider than the bondpad on the chip. This leads to an increase in capacitance at the bondpad and thus a local change of line impedance, causing higher return loss. It can be expected that choosing the bondpad to be wider than the maximum expected bump width plus an additional width accounting for tolerances in the placement of the bump would limit such a local impedance variation. Without the contribution from the bump radius of 25 µm, the spread decreases to 0.1 dB around -1 dB. Increasing the distance of IS and PCB leads to higher insertion loss due to increased radiation. Apart from the distance between PCB and IS of 92 µm, increasing the distance between IS and chip reduces insertion loss due to lower radiation loss. This is not the case for the bump radius of 25 µm however where increasing the height of the bumps causes higher capacitance at the transition and subsequently higher return loss. Overall there is a very good agreement between different chip bump radii and heights and variations of the distance between PCB and IS. This indicates a resilience of this transition to process variations of the bumping process both for the chip bumps as well as the bumps connecting PCB and IS.
In the previous simulation there is a taper with a length of 600 µm before the transition. A taper is necessary as the bond pad on the chip has fixed dimensions in this work and the bumping process of the bumps connecting PCB and IS may have some tolerances in placement or bump width. This is an important consideration for the second transition discussed in section 3.3.3 where a larger distance between the center and outer conductors may be necessary. Forgoing a taper yields lower insertion loss due to lower reflection for some combinations of center conductor width and distance between center and outer conductors. The simulation result for the lowest return loss of this analysis with a height of the bumps connecting PCB and IS of 92 µm and a height of the bumps connecting chip and IS of 30 µm can be seen in figure 3.13. The center conductor width is 80 µm

and the distance between center and outer conductors is 10 µm. The full simulation result of the parametric evaluation without a taper is shown in appendix A.3.

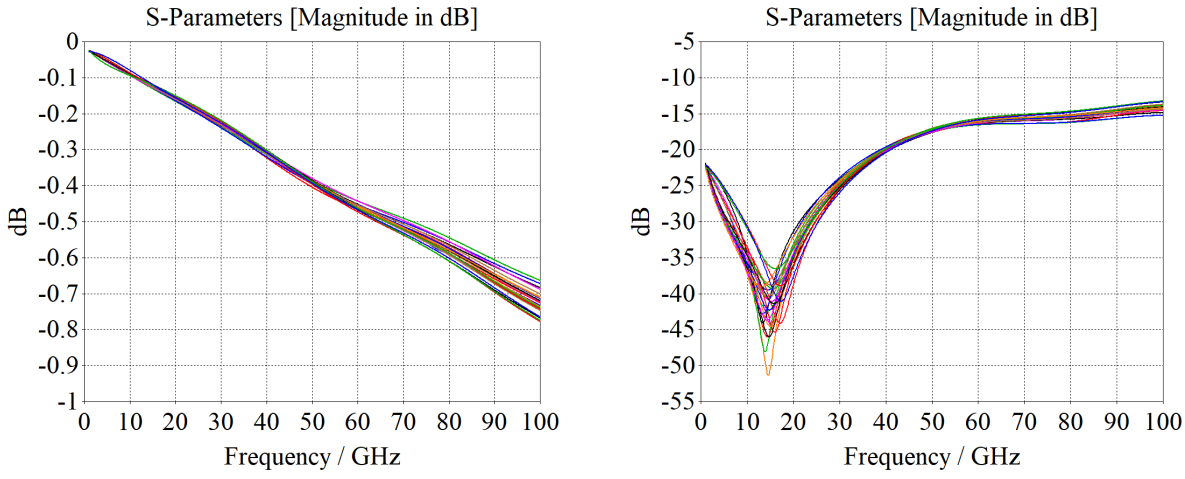


(a) S21 **(b)** S11

Figure 3.13.: S-Parameters of the parameter combination for lowest return loss without a taper.

The insertion loss without a taper for the given parameter combination is 0.52 dB at 100 GHz and return loss remains below -25 dB for the frequency range of 3 to 100 GHz and below -23 dB for the range of 1 to 3 GHz. A taper on the IS may not be necessary for chips either with larger bond pads than the one used in this work or especially for a larger spacing of the center and outer conductors at the bond pad.

Apart from fused silica it is also possible to use alumina as a substrate material. Figure 3.14 shows the same parametric analysis as figure 3.12, but with alumina as a material for the IS.



(a) S21 **(b)** S11

Figure 3.14.: Parametric spread of simulated S21 (left) and S11 (right) parameters.

This spread is very similar to the one using fused silica, but shows higher insertion losses. The

increase in insertion loss is due to higher radiation loss. Particularly, as the proposed structure is not shielded at the top of the IS, radiation can occur in this direction. Alumina having a higher ϵ_r than fused silica causes a larger part of the energy of the main mode of propagation on the iGCPW to be within the IS. Additionally, according to the discussion in section 2.1.3, if the substrate thickness is too high, surface waves may propagate. A simulation result showing the S-parameters resulting from a substrate thickness of 500 µm, instead of 250 µm, and choosing alumina resulting in a higher electrical length of the intermediate substrate is shown in the appendix A.3. These surface waves are unwanted as they would increase loss to radiation and might couple signals originating from other parts of the structure similar to the problem of PCB substrate modes with a regular flip chip approach discussed in section 3.1. For substrates made of either fused silica or alumina of a thickness of 250 µm such surface waves were not indicated in the given frequency range however. Due to these parasitics fused silica may be preferred as a material for higher thicknesses of the IS or for higher frequencies than were simulated in this work as it has a lower ϵ_r. Placing additional bumps near the transition can help alleviate some strain acting on the bumps due to thermally-caused material expansion. The compensating bumps are included in figure 3.9 shown at the beginning of this section. In the appendix A.3 the power flow near the transition and S-parameters without the compensating bumps can be seen. Adding the compensating bumps has little effect on the overall electrical performance of the transition.

Another source of radiation loss is caused by the gap between the grounded metal plane on the PCB and the backside metal plane of the chip. A view of the power flow in this gap compared to the overall power flow near the transition is shown in appendix A.3. Depending on the bumping process for the bumps connecting IS and PCB, lower heights might be preferred. One way to achieve that is to remove the top metal layer of the PCB under the chip and some tolerance for placement around it. Figure 3.15 shows the power flow if the PCB top metal layer beneath the chip is removed.

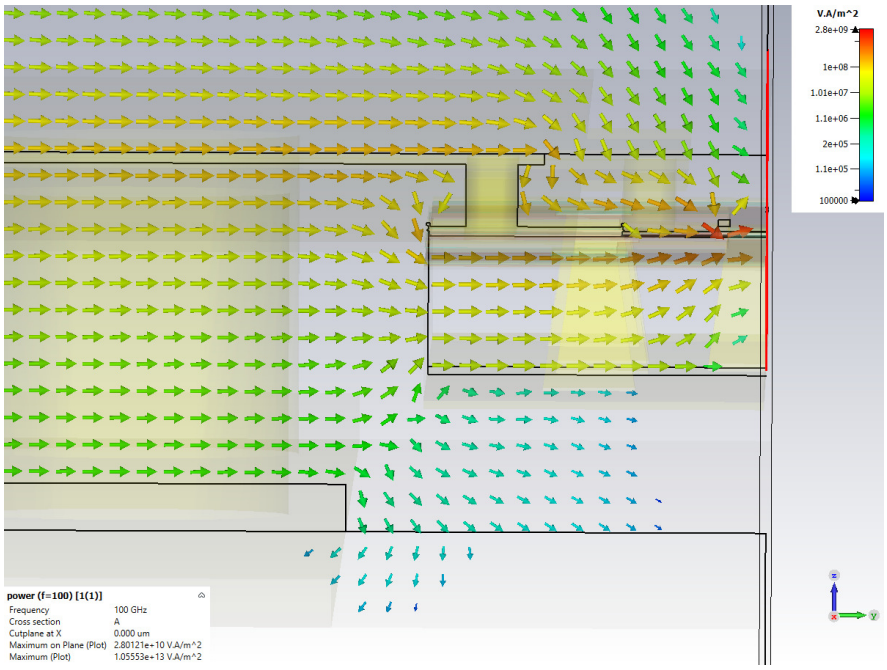


Figure 3.15.: Power flow of the gap between PCB and chip.

The S-parameters of this simulation can be seen in appendix A.3. However the overall impact on the insertion loss of this change is very small. It should be noted that removing the PCB metal below the chip could cause PCB substrate modes to interfere with the signal inside the structure unless vias inside the PCB are placed around the placement point of the chip. Additionally the metal on the PCB has a higher thermal conductivity than the PCB dielectric and not removing the top metal layer under the chip may thus be preferred for thermal performance. Still, despite the removal of the top metal layer below the chip showing little increase in overall radiation loss, radiation loss, in addition to return loss and metal losses remain the major loss mechanisms in this structure. Thus, in the next section the losses on the iGCPW transmission line are analysed qualitatively and quantitatively, especially with regards to the impact on losses of variations of the structural parameters.

3.3.2. Transmission Line Loss on Intermediate Substrate

A challenge in the design of chip sets and packaging is the limited degree of freedom of placing the chip on the PCB. Achieving a long-lasting and mechanically stable interconnection requires not only precise manufacturing and placement on the PCB, but also either a sophisticated wire bond which should be as short as possible to reduce insertion and return losses, connecting both chips with a direct flip chip interconnection or routing the signal over the PCB. The approach proposed in this work allows the designer more freedom in the placement and connection between different chips of a chipset without requiring lossy and narrowband wire bonds or as precise manufacturing on the PCB side. In this section the losses of the iGCPW transmission line are evaluated to estimate the contribution of the transmission line to total loss. This can also give an estimate how long the

iGCPW transmission line on the IS can be made for a given maximum acceptable insertion loss. Figure 3.16 shows a model of the transmission line.

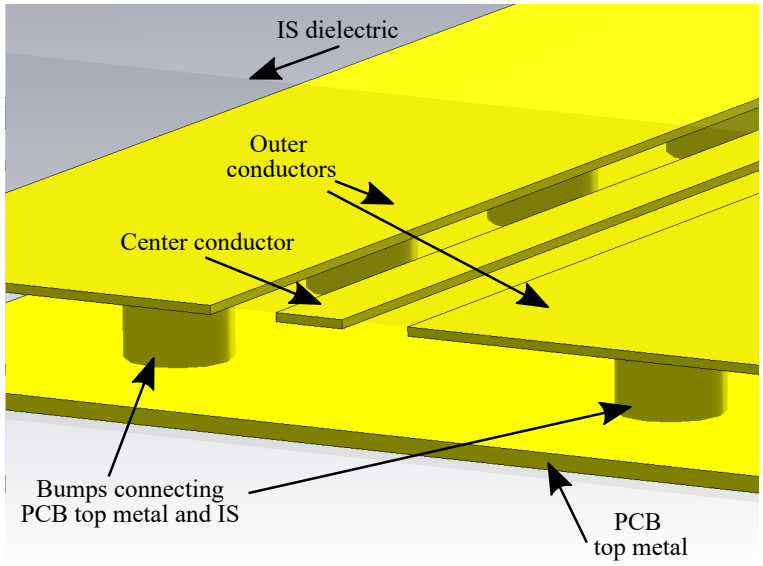
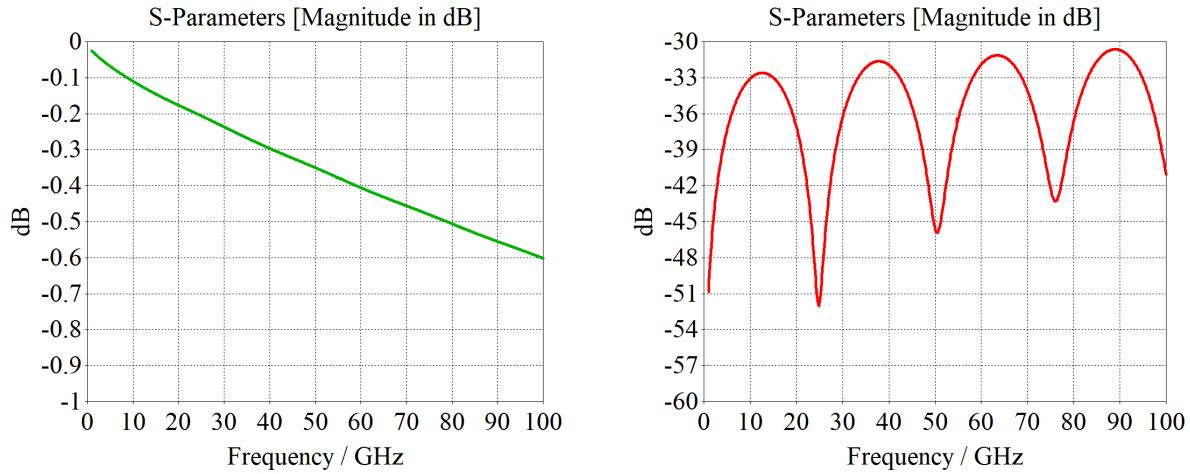


Figure 3.16.: Model of the iGCPW transmission line simulated in this section.

S21 and S11 of a transmission line of 4 mm length with a height of the bumps connecting IS and PCB of 110 µm, a distance between the center conductor and the outer conductors of 40 µm, a thickness of the metal on the IS of 4 µm and a width of the transmission line of 80 µm is shown in figure 3.17. The material is fused silica and the bumps are placed at a distance of 300 µm from the center of the transmission line. The bumps are placed every 400 µm along the transmission line.



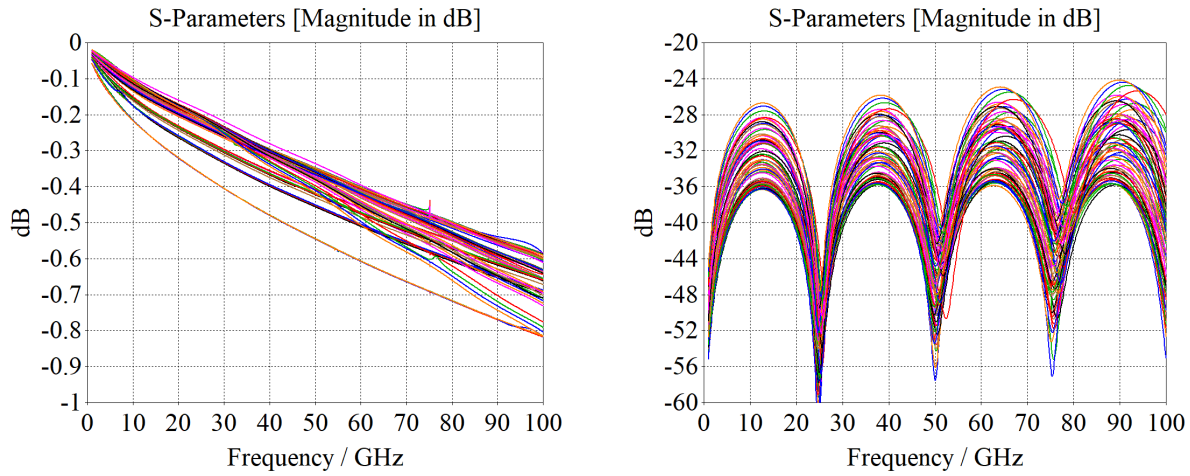
(a) S21 **(b)** S11

Figure 3.17.: S21 (left) and S11 (right) of the 4 mm long iGCPW.

S11 stays below -30 dB for the entire frequency range from 1 GHz to 100 GHz. Insertion loss increases monotonically with frequency and has a value of 0.6 dB at 100 GHz. This indicates a

simulated attenuation of 0.15 dB/mm at 100 GHz as the simulated transmission line is 4 mm long. The main contributors of loss are metal losses and radiation, with dielectric loss and return loss both being one order of magnitude lower than the first two loss mechanisms.

A parametric evaluation of varying the center conductor width from 20 µm to 100 µm in 20 µm steps, the height of the bumps connecting PCB and IS from 70 µm to 130 µm in 20 µm steps and the distance between the center and outer conductors at 20 µm, 40 µm and 60 µm is shown in figure 3.18. The length of the structure is 4 mm and the bumps have a distance of 300 µm from the center of the center conductor. It should be noted that this parametric evaluation only considers the losses and the impedance may vary from 50 Ω.



(a) S21 **(b)** S11

Figure 3.18.: Parametric evaluation for the transmission line loss.

For all parameter combinations S11 corresponding to return loss is below -25 dB except for a width of the center conductor of 100 µm combined with a distance of center and outer conductors of 60 µm where it peaks slightly below -24.1 dB. Insertion loss shows little variation with regards to changes in the bump height. The spread if center conductor width and distance between center and outer conductor stays below 0.01 dB for most parameter combinations. A distance between center and outer conductor of 60 µm combined with transmission line widths of 80 µm and 100 µm are exceptions where the spread stays below 0.02 dB instead.

This little impact of the bump height on loss can be explained by looking at the loss mechanisms. Decreasing the height of the bumps increases metal loss as the electrical field has a larger amplitude at the metal-air boundaries to achieve the same total energy of the wave. However, decreasing the bump height also leads to a smaller part of the energy of the wave being in the IS dielectric where most radiation losses occur. Increasing the bump height reverses the two effects. As these two effects appear to be of the same order of magnitude for the given parameter combinations, the iGCPW transmission line's total loss changes little with changing bump height. In appendix A.4 a comparison of the losses of bump heights of 70 µm and 130 µm is shown.

Increasing the transmission line width decreases metal losses, but also increases radiation losses.

This can be explained by the field being less concentrated on the metal surfaces while also extending further into the IS dielectric for larger widths where it is more likely to radiate away. Changing the distance between center and outer conductors has a similar effect as changing the transmission line width. The sweet spot for lowest total losses depends on both width and distance. For transmission line widths of 40 µm and 20 µm, the total losses decrease with increasing distance between center and outer conductor. For the transmission line widths of 60 µm, 80 µm and 100 µm the trend is reversed and lowest total losses for the given parameter combinations occur with the distance at 20 µm.
Of all parameter combinations the lowest insertion loss is achieved with a transmission line width of 60 µm, a distance of 20 µm and a height of 90 µm at 0.585 dB. Changing the transmission line width to 80 µm and leaving the other parameters at the same values increases the insertion loss to 0.602 dB. Changing the parameters also changes the line impedance of the transmission line and can be varied to improve matching to the connecting transitions. The lowest line impedance within the given parameter range is achieved by maximizing center conductor width and minimizing distance between center and outer conductors and bump height at approximately 69 Ω. The highest line impedance, conversely, is achieved by maximizing distance and bump height and minimizing center conductor width at approximately 123 Ω.

While for the IS to chip transition in section 3.3.1 the most important loss contributors are return loss, metal losses and radiation, the pure transmission line without any transitions has significantly lower return loss than the transition. Additionally, in the simulation model for the transition discussed in section 3.3.1, there is a 1 mm transmission line preceding the actual transition with the bumps. So the simulation results regarding the losses obtained in this section can be used to more accurately estimate which part of the losses obtained for the IS to chip transition corresponds to the preceding 1 mm transmission line and which corresponds to the transition. It can be estimated that the contribution of return loss to total loss is caused almost entirely by the transition itself, whereas the majority of metal losses are caused by the preceding line. Using the estimate of 0.15 dB/mm attenuation of the transmission line for the parameters of the structure in figure 3.16 and the 1 mm long transmission line preceding the transition in the simulations in section 3.3.1, the actual transition causes an insertion loss of 0.8-0.9 dB at 100 GHz, depending on bump parameters. Compared to wire bonds this structure shows lower loss per length which allows for greater distances to achieve comparable losses. However the confinement would still be a perpendicular orientation of the different chips of a chipset to each other. Achieving bends of the transmission line outside of the chip would allow for greater flexibility in the chip design as different signals, especially of higher frequency, would not need to be routed to the sides of the chips facing each other and at the same distance on both chips. For this reason 45° bends of the iGCPW transmission line were also investigated in this work and are shown as a model of a 90° bend consisting of two subsequent 45 ° bends in figure 3.19.

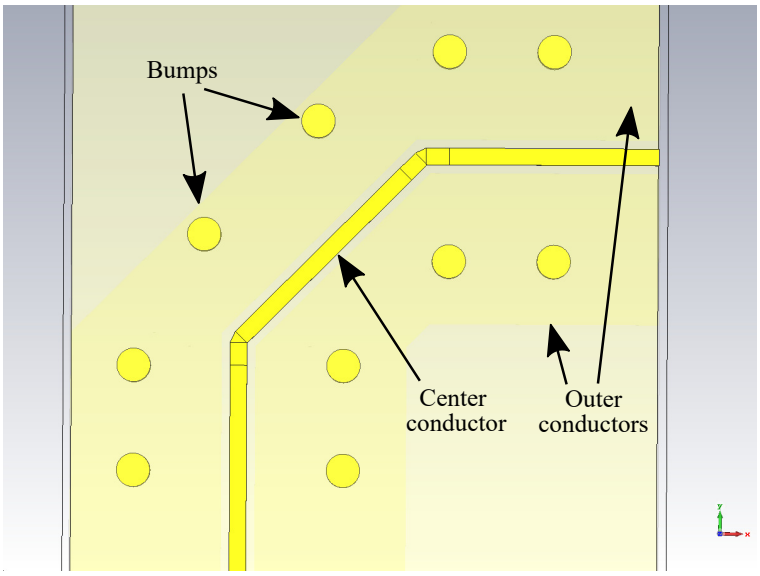
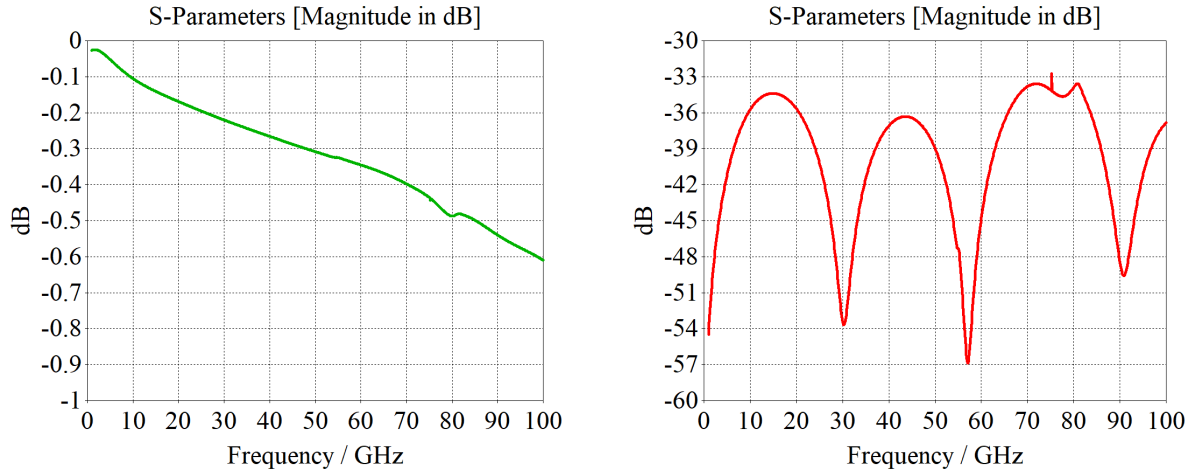


Figure 3.19.: Model of a 90° bend consisting of two 45° bends.

The corresponding S-parameters are shown in figure 3.20. The port dimensions are the same as in figure 3.16. The entire length of the bend structure is approximately 3 mm. The length consists of 1 mm from the feeding port to the first 45 ° bend, 1 mm straight between the bends and another 1 mm as the distance from the second bend to the receiving port.



(a) S21 **(b)** S11

Figure 3.20.: Simulation result of the 90° bend.

Compared to the results from the straight transmission line in figure 3.17, the difference adjusted for length is insignificant. This shows a good wave confinement even at 45 ° bends. Another simulation result where the bumps are removed is shown in appendix A.4. Removing bumps, particularly the bumps on the outer side of the bend structure, causes additional radiation to occur between PCB and IS at the location of the bends. A simulation result showing the resulting power flow is also shown in appendix A.4. Apart from this electrical influence, distributing mechanical

stresses caused for example by thermal expansion, better distribution of heat and maintaining an even distance between PCB and IS are other reasons for the rigorous placement of bumps connecting the PCB top metal layer and the IS metal layer. In the next section the simulated results for the transition between PCB and IS are presented.

3.3.3. Printed Circuit Board to Intermediate Substrate Transition

The second transition of the structure introduced in this work concerns the transmission of signals between a PCB and the IS. The feeding port is on the PCB and feeds into a GCPW. For a width of the center conductor of 100 µm and a distance of 100 µm between the center and outer conductor this results in a line impedance of approximately 87 Ω. A taper on the PCB would be required for this structure to be fed by 50 Ω cables or for probing. The distance between the feeding port and the transition is 3 mm. After the transition, the distance to the receiving port on the IS is 1.5 mm. In figure 3.21 the simulation model of the transition is shown with a bump height of 100 µm.

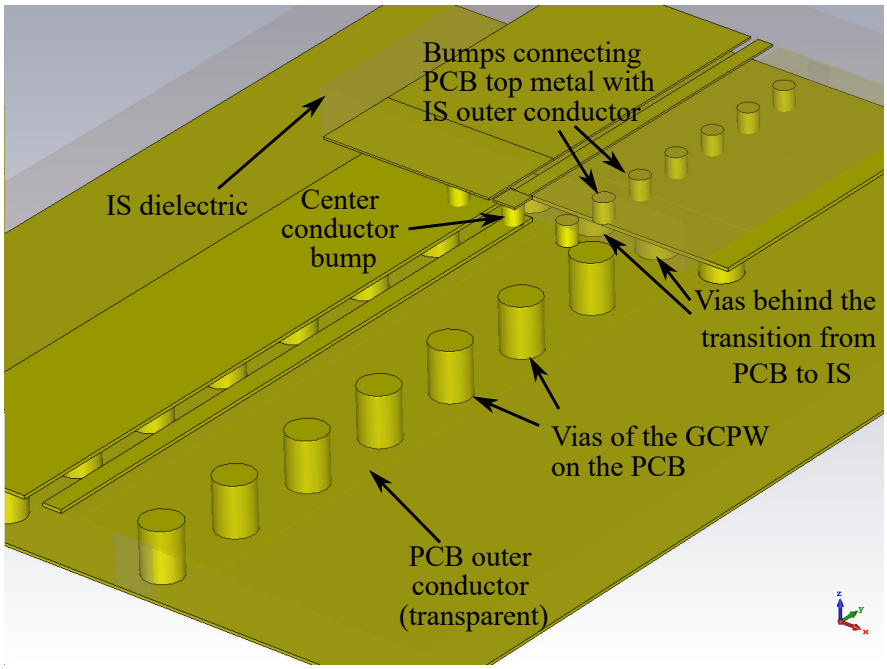
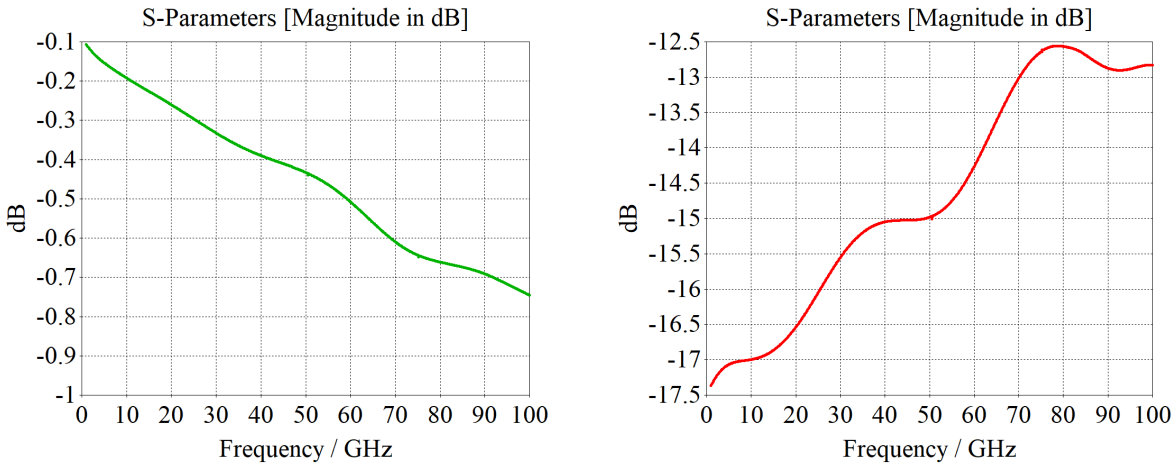


Figure 3.21.: Model of the PCB to IS transition; the IS and PCB dielectrics, part of the top metal on the PCB and part of the IS outer conductor metal are transparent to show the bump and via placement.

The corresponding S11 and S21 are shown in figure 3.22.



(a) S21 **(b)** S11

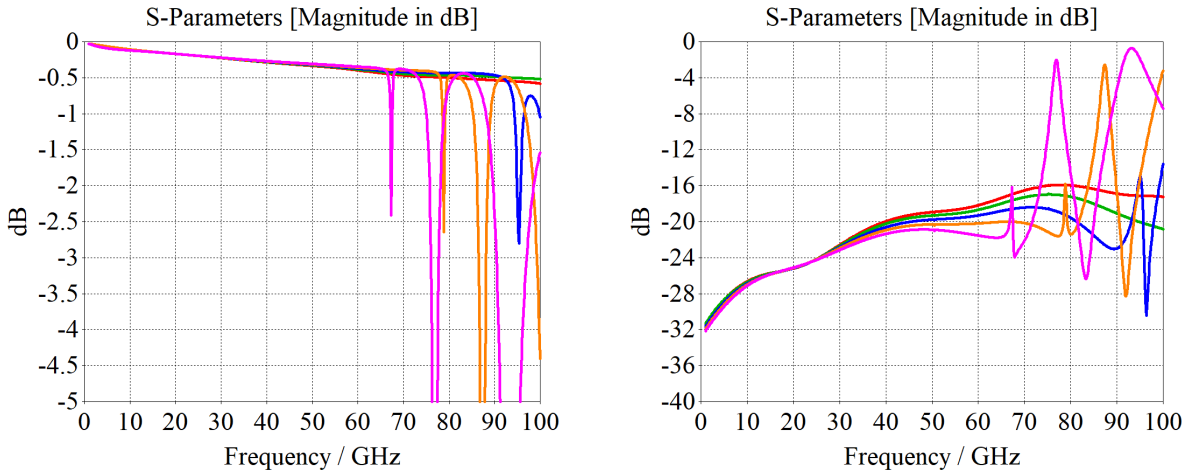
Figure 3.22.: Simulation result of the PCB to IS transition.

S11 remains below -12.5 dB for the entire frequency range of 1 GHz to 100 GHz. S21 decreases monotonically and reaches approximately -0.745 dB at 100 GHz. With the approximation for the loss of the QTEM mode on the iGCPW of 0.15 dB/mm at 100 GHz and 1.5 mm length, the resulting insertion loss from the transition and preceding 3 mm GCPW transmission line on the PCB can be approximated as 0.52 dB at 100 GHz.
In the structure shown in figure 3.21 there are vias placed behind the transition. The vias have a planar surface made of conducting metal on the top layer. Such vias are called filled-and-capped vias and can be fabricated at PCB manufacturers [33] although they do incur some additional costs. It is also possible to use regular vias that are not filled and capped and thus have a hole in the center. A simulation result with such vias and additionally adding a slight lateral misalignment to investigate potential resonances or mode conversion due to disruption of the planar metal top layer of the PCB for the iGCPW structure are shown in appendix A.5. The difference is negligible. Although, because a non-planar surface could interfere with the manufacturing of the bumps connecting PCB and IS, it may be beneficial to ensure a planar surface and forgo the use of regular vias near the iGCPW structure. This is particularly impactful if a reflow step with bumps made of solder is used.

A planar surface can also be achieved by forgoing the use of vias behind the transition entirely. A simulation result where vias behind the transition are omitted is shown in appendix A.5. S21 reaches -0.94 dB at 100 GHz corresponding to an insertion loss of 0.79 dB of the sum of transition and preceding GCPW on the PCB. Omitting the vias increases radiation loss. An explanation for this is that while the CPW component of the QTEM mode on the GCPW passes the transition with low losses, the non-CPW component of the QTEM mode on the GCPW behaves in a similar way to the microstrip line transition in section 3.1. The structure also approximates the end of a rectangular waveguide, showing similar radiation as can be observed in a horn antenna. To reduce this effect while still achieving a planar surface on the top layer for the iGCPW mode it is possible to use blind vias drilled from the backside. A simulation result using blind vias extending up to

approximately 100 µm below the top metal layer can be found in appendix A.5. S21 reaches -0.83 dB corresponding to an insertion loss of 0.68 dB of the transition and preceding GCPW transmission line. The structure with blind vias has lower radiation loss than the structure without vias, but shows higher losses than the structures with filled and capped and regular vias. Blind vias are more expensive to fabricate than regular vias, but cheaper than filled and capped vias [8]. The achievable minimum distance of the blind vias from the top metal layer depends on the PCB composition and requires a metallization. Minimum layer thicknesses are in the range of 60 µm to 100 µm [34].

A critical component of this structure are the vias connecting the outer conductors of the GCPW mode to the lower metal plane on the PCB. A simulation result of the parametric evaluation of the placement of these vias is shown in figure 3.23. The vias are placed between 100 µm to 500 µm away from the edge of the outer conductor near the center conductor with a 100 µm step size. The center conductor width on the PCB is 200 µm.



(a) S21 **(b)** S11

Figure 3.23.: Simulation result of the parametric evaluation of the via placement.

For the distances of 100 µm (red) and 200 µm (green) S21 for the transition shows a monotonic behaviour. Insertion loss at 200 µm is slightly lower than for 100 µm. The reason for this difference is slightly improved matching near the upper end of the frequencies for the larger distance. For distances of 300 µm (blue), 400 µm (orange) and 500 µm (magenta) the structure shows significant return loss with the behaviour being similar to a notch filter. Increasing the distance further beyond 300 µm shifts the center frequencies of this notch filter characteristic to lower frequencies. A parametric evaluation with a center conductor width of 100 µm can be found in appendix A.5 and shows similar results, however the filtering characteristic is shifted to slightly higher frequencies and losses other than return loss are slightly higher.

A possible heuristic explanation for this phenomenom can be given by looking at the GCPW near the transition in detail: If the distance between center and outer conductors would become sufficiently small the structure would transition into a structure resembling a rectangular waveguide which is in line with the discussion in section 2.1.4. By conducting a thought experiment the vias

behind the transition can be approximated as a conducting wall and the resulting structure would strongly resemble a rectangular cavity showing resonant behaviour and resulting in reflections. Additionally the structure shows much increased radiation and metal losses near the resonances which can be attributed to the vias not forming continuous conducting walls. As the vias are placed farther from the edge of the outer conductor, the similarity to a rectangular waveguide increases.
In addition to the vias not forming continuous walls, the real structure is not a perfect rectangular waveguide as the CPW part of the GCPW has the upper conducting wall of a rectangular waveguide broken apart. Still, the shown resonance strongly indicates a parasitic behaviour that resembles that of rectangular waveguide. To avoid this parasitic behaviour the sufficiently near placement of the side vias of the GCPW mode on the PCB can be derived as a design rule.
Reflections at this transition are also influenced by the height of the bumps. For a distance of center and outer conductors of 40 µm, a width of the center conductor of 80 µm and a material of the IS of fused silica the resulting line impedance of the port on the IS varies between 62 Ω and 68 Ω for a variance of the height of the bumps between 70 µm and 130 µm. A graph comparing the impedance variation for different bump heights can be seen in appendix A.5.
While the two transitions and the losses of the iGCPW on the IS offer important indications of the behavior of a full system combining these three elements, the actual behavior of the full system might differ due to unforeseen simplifications in the single models or interdependencies of the different structures. Hence, in the next section an analysis of the behavior of the full system consisting of a connection from a GCPW on a PCB to the chip and a connection between different chips is given.

3.3.4. Full System

The first of the two connections in a full system is the one concerning PCB to chip connections. The signal is fed on the feeding port of the PCB, then travels to and passes the transition from PCB to IS. It then travels on the iGCPW transmission line before passing the transition from IS to chip and is received by the port on the chip. In figure 3.24 a model of the full system is shown. The height of the bumps is 100 µm, the distance between chip and the PCB to IS transition is 1.3 mm, the width of the center conductor on the PCB is 200 µm and the distance between the center and outer conductors on the PCB is 60 µm. On the IS the center conductor is 80 µm wide and the distance between the conductors is 20 µm.

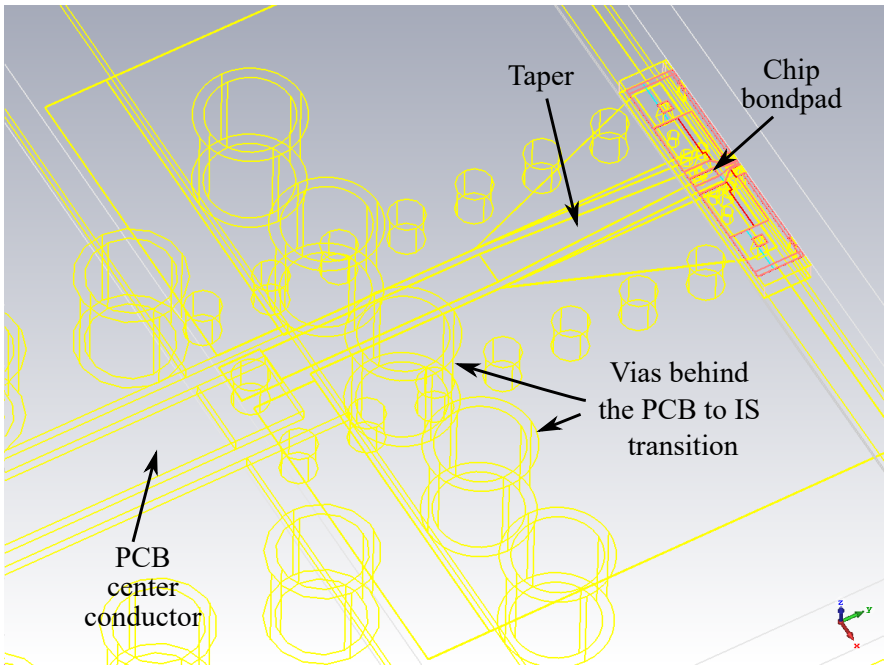
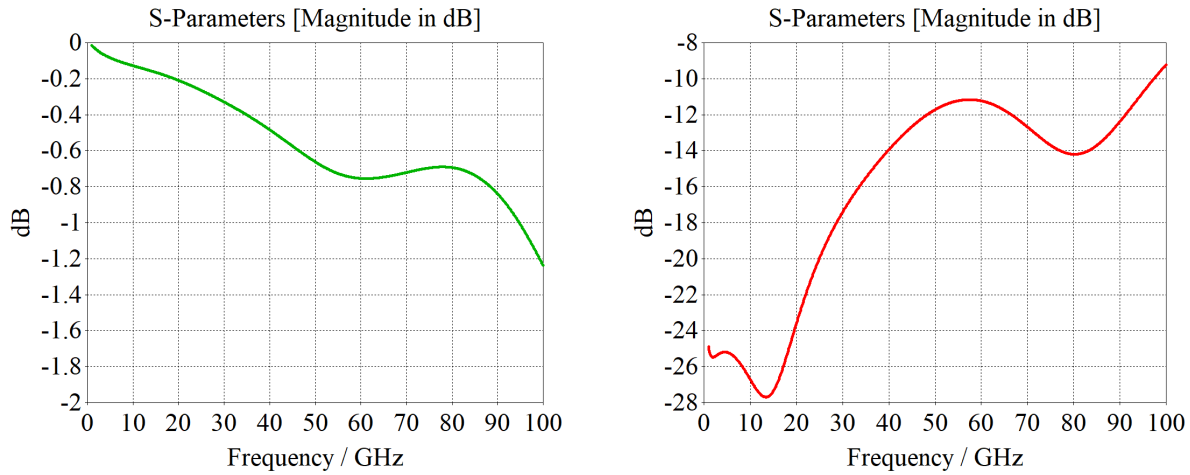


Figure 3.24.: Model of the full transition from PCB to chip over the IS.

The corresponding S-parameters are shown in 3.25.

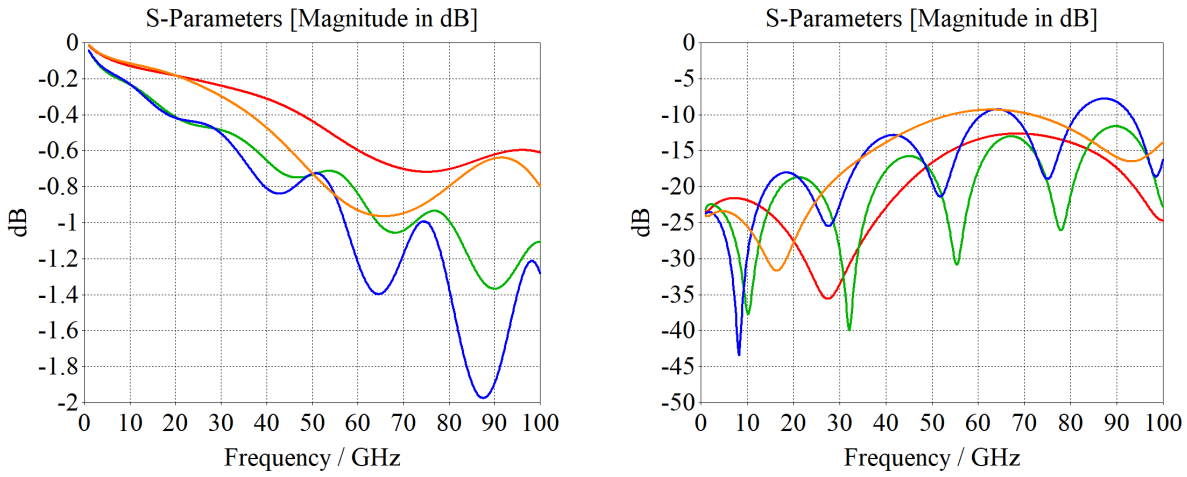


(a) S21 **(b)** S11

Figure 3.25.: Simulation result of the full transition shown in figure 3.24.

S21 reaches a local minimum of -0.75 dB at 61 GHz, has a local maximum of -0.69 dB at 78 GHz and reaches -1.24 dB at 100 GHz. This non-monotonic behavior of the insertion loss can be explained by looking at the return loss. S11 reaches a local maximum of -11.2 dB at 57 GHz strongly aligning with the increased insertion loss. This return loss is higher than the combined return losses of the two single transitions. The reason for this discrepancy is that there are two transitions in a row leading to resonances from standing waves. This can be seen in the profile of S11 in that there are

minima where destructive interference occurs and maxima where the positive interference leads to greater return loss. One cause of reflection is the taper before the IS to chip transition. In the simulation result shown in figure 3.25 the taper is 600 µm long. Changing the distance should also change the resonance frequency of the two subsequent transitions while also increasing losses due to the loss mechanisms discussed in section 3.3.2. A parametric evaluation of distances of 1.1 mm and 4.1 mm and taper lengths of 600 µm and 25 µm and unchanged other parameters is shown in figure 3.26.

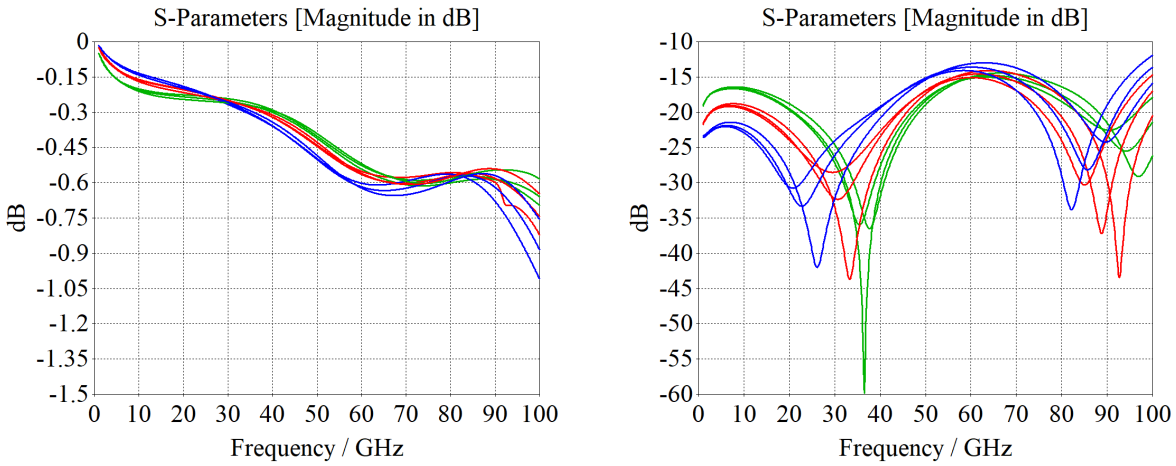


(a) S21 **(b)** S11

Figure 3.26.: Simulation result of the length and taper variation for the full system.

The lower distance (red and orange) has reduced losses due to lower losses on the iGCPW and fewer ripples as the resonance frequency and its harmonics are shifted to higher frequencies. The lower taper length (red and green) has a significantly reduced return loss compared to the longer taper (orange and blue). Careful design of the taper can thus help reduce return loss.
Another influence on the return loss is the quality of the matching. The main parameters affecting the line impedance of the GCPW on the PCB are the thickness of the PCB, the distance between center and outer conductors and the width of the center conductor. Decreasing the thickness of the PCB would lead to both increased dielectric losses and metal losses as the electric field is more concentrated in the dielectric and the metal surfaces on the dielectric. For the IS the relevant parameters affecting line impedance are the height of the bumps connecting PCB to IS, the width of the center conductor and the distance between center and outer conductors. To achieve a better matching for the full system a parametric evaluation is shown in figure 3.27 with center conductor widths on the PCB of 200 µm, 250 µm and 300 µm, distances between center and outer conductors on the PCB of 60 µm, 80 µm and 100 µm and heights of the bumps connecting PCB and IS of 90 µm, 110 µm and 130 µm. The distance of the center and outer conductors on the IS is 40 µm and the width of the center conductor on the IS is 80 µm. The line impedances for the variations of center conductor widths and distances on the PCB correspond to line impedances in the range of 49 Ω to 66 Ω. The taper is 25 µm long and the distance between chip and the transition from PCB to IS is

1.3 mm.



(a) S21 **(b)** S11

Figure 3.27.: Simulation result for the bump height and PCB transmission line variation for a distance between center and outer conductors of 100 µm

S11 remains below -10 dB for all parameter combinations in the frequency range between 1 GHz and 100 GHz. The degree of influence of the bump height on overall insertion loss depends on the center conductor width of the PCB. The spread is below 0.15 dB at 100 GHz for the center conductor width of 200 µm (green) a fixed distance of the center and outer conductors and a variation of the bump height. This increases to 0.2 dB for a width of 250 µm (red) and to 0.3 dB for a width of 300 µm (blue). Overall losses also increase with increasing center conductor width which can be explained by the poorer match for this choice of parameters on the IS. The lowest insertion loss at 100 GHz of this parametric evaluation was achieved with a center conductor width of 200 µm, a bump height of 90 µm and a distance between center and outer conductors of 100 µm at 0.58 dB. The full parametric result is shown in appendix A.6.

Significant coupling to different port modes was not observed in the given frequency range in the simulations shown in this chapter. It should be noted, however, that this could constitute a problem which is not indicated by the CST simulation software and might limit the upper frequency range of signals propagating particularly on the GCPW on the PCB.

The second structure, that is of interest, concerns the connection between different chips. This structure uses the IS to chip transition twice. For this transition the taper introduced in chapter 3.3.1 causes significant return loss as it is applied twice and a simulation result showing this behavior is shown in appendix A.6. However, as the connection between different chips does not involve a connection of the center conductor to the PCB, a taper is not needed for this connection. Figure 3.28 shows the model of the chip to chip connection. To achieve a good match, the distance between center conductor and outer conductor is 10 µm and the center conductor width is 80 µm.

The distance between the two chips is 2 mm.

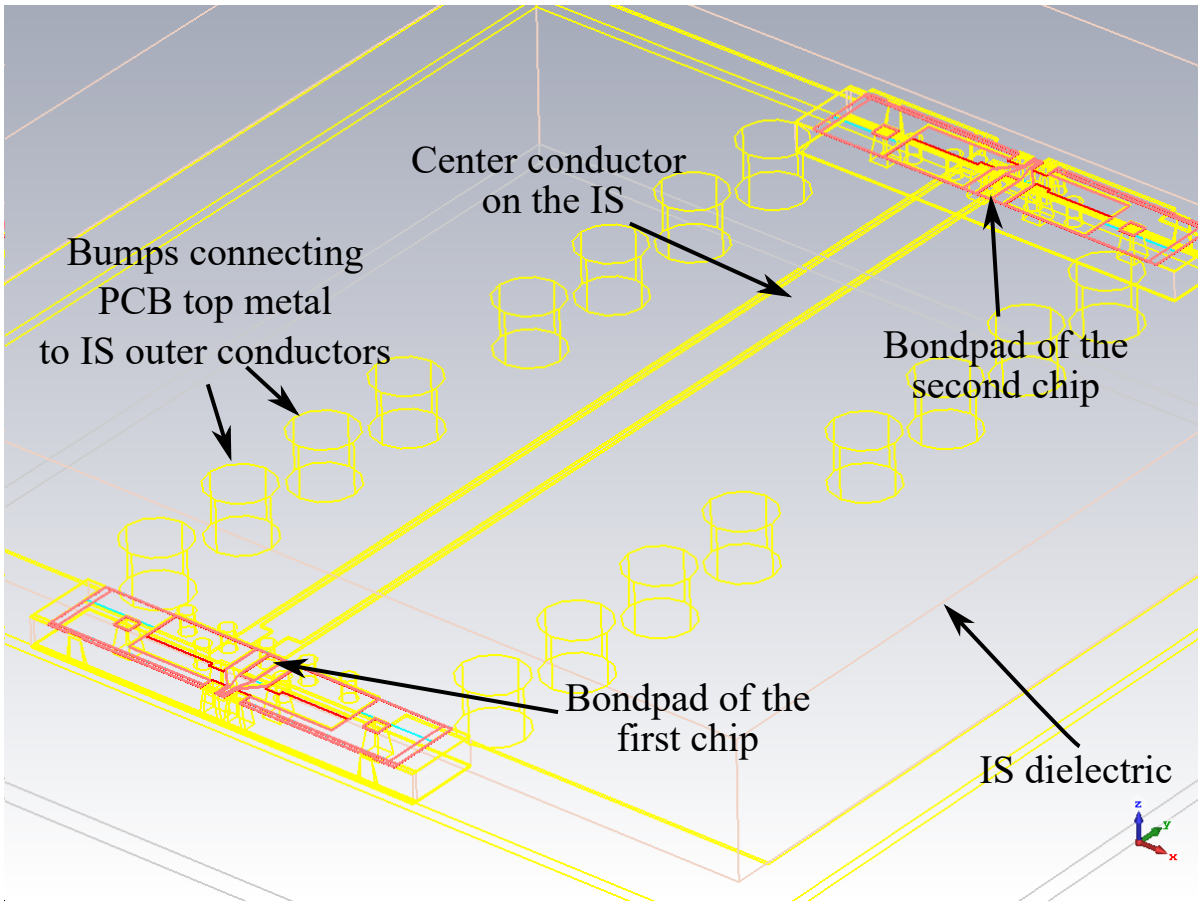
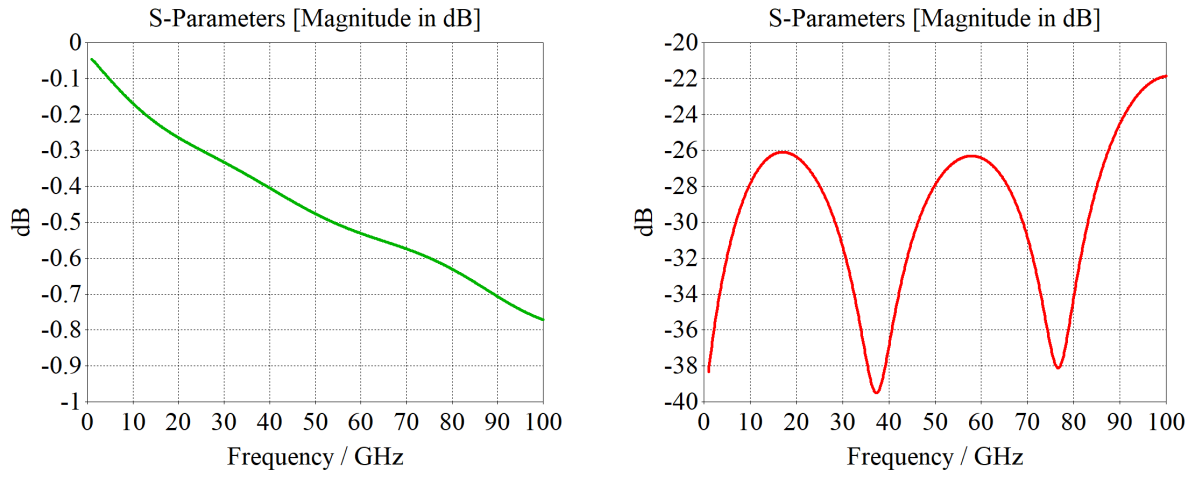


Figure 3.28.: Model of the chip to chip connection.

The corresponding S-parameters are shown in figure 3.29.



(a) S21 **(b)** S11

Figure 3.29.: Simulated results of the chip to chip connection.

The insertion loss rises monotonically and reaches 0.77 dB at 100 GHz. Increasing the distance would increase losses with the increasing loss coming from the iGCPW transmission line being in the order of 0.15 dB per millimeter added. Return loss remains below -21 dB for the entire frequency range between 1 GHz and 100 GHz indicating a very good broadband match. This means the structure is well suited to connecting different chips of a given chipset in this frequency range. This structure has also been verified with the time domain solver. A simulation result of this structure with the time domain solver is shown in appendix A.6. For the time domain simulation return loss is higher, but stays below -15 dB for the entire frequency range. The simulated insertion loss at 100 GHz is 0.69 dB. Changing bump height changes the line impedance of the iGCPW transmission line. A parametric evaluation can be found in appendix A.6. Insertion loss slightly increases with increasing height with 0.77 dB insertion loss for a bump height of 92 µm and 0.84 dB for a bump height of 132 µm at 100 GHz. The increase in losses is mainly due to increased loss to radiation.

3.4. Simulation Limitations

As mentioned in the beginning of this chapter simulations are a powerful tool to gauge how structures behave prior to fabricating them. However, due to the finite processing power and storage capacity of computers every simulation assumes certain abstractions from the real world. If these abstractions turn out to omit important parts of the real structure, the results of the simulation might differ significantly from the result obtained from measuring a real circuit. This section is dedicated to the discussion of the limitations of the simulation software and possible solutions.

A first limitation stems from the usage of a mesh. The resolution of the structure is limited by the size of the mesh cells. In FEM a finer mesh can be expected to provide a more accurate representation of the model, but also takes longer to simulate for the same computation power. To optimize the two competing interests in accurate simulation results and a reasonable time to simulate, CST uses an algorithm to refine the mesh in iterations. The exact algorithm is proprietary, however the algorithm optimizes by reducing the difference of S-parameters between consecutive iterations for a given frequency sample. The simulations in the frequency domain solver shown in this chapter all used this adaptational mesh refinement prior to a broader frequency sweep targeting a minimum difference of the S-parameters of 0.01 in absolute terms at a given frequency sample. The broader frequency sweep also uses an algorithm to automatically select the next frequency sample and works similarly by aborting the sweep once a selected accuracy for the broadband convergence is achieved. Due to difficulties in simulation stability the mesh for all simulations using the time domain solver had to be adjusted manually.

A possible error stems from the accuracy of the modelling. Actual shapes of the fabricated structures might differ from the simulation model. Particularly the assumption of the bumps being cylindrical in shape and the surface metal layer of the PCB being composed of perfect cuboids could differ in reality.

Another possible inaccuracy of the simulation is from the accuracy of the lossy metal model. According to the discussion in section 2.3.1, the lower end of the range of validity is proportional to the inverse square of the thickness of the metal. In the simulations there was little difference in the results of simulating a 10 μm and 4 μm thick metal layers on the IS. However, in a fabricated structure with lower thicknesses metal losses or wave confinement could be worse corresponding to higher radiation losses. However, this discrepancy can be expected to be more of an issue especially at lower frequencies.

Hence, to evaluate the accuracy of the simulation and to find potential problems that could arise during fabrication, a fabrication of the proposed structure is necessary.

4. Manufacturing Considerations and Outlook

While a fabrication of the structures proposed in section 3.3 is not within the scope of this work due to time constraints, preliminary ideas regarding the manufacturing and its associated constraints were developed in this work and are presented in this chapter. This is done through a description of the outline of a process to manufacture the IS and the steps involved in bonding chips to the IS and the IS to a PCB. This chapter also includes an overview over possible future avenues of research making use of the proposed structures.

4.1. Intermediate Substrate Process Description

The proposed process begins by coating one side of the substrate, made of either fused silica or alumina, with a thin layer in the range of 100 nm of a metal such as gold through sputter deposition. Other possible materials for the sputtered metal are copper and molybdenum. This metal serves as an electrode for a subsequent electroplating step. While it is possible to achieve thicknesses in the range of micrometers by pure sputter deposition [35, pg. 6], doing so would require significant time in the vacuum chamber of the sputter deposition machine [32].
Hence, the next step is to electroplate a layer of copper on the sputtered layer. The thickness of the electroplated layer dictates the main part of the final thickness of total metal layer. The thickness of the copper layer is in the range of micrometers. Next follows the structuring of the metal layers. For this a photoresist is applied for example by spin coating, exposed through the use of a single mask and subsequently developed. After this the copper can be etched via reactive ion etching (RIE) to achieve sharp edges without significant under etching and the underlying metal can be etched either in the same RIE step or with a subsequent wet etching step. Copper can be etched by chlorine chemistry RIE [36], gold by wet etching [37] or chlorine chemistry RIE [37] and molybdenum can be etched by flourine chemistry RIE [32]. After the etching comes the stripping of the photoresist. Next follows the surface finish to allow for more straightforward bonding which can use a standard PCB process like electroless palladium immersion gold (EPIG) or electroless nickel EPIG (ENEPIG). Both of these, especially ENEPIG, introduce additional metal thickness vertically and laterally which must be accounted for when designing the mask for the metal layer. To allow for probing and the use of on-chip antennas the part of the IS where the chip is to be placed has to be removed. As both alumina and fused silica are brittle materials, mechanical drilling would prove challenging. Instead, a laser drilling process such as the one demonstrated by [38] should be considered, allowing for lateral tolerances in the range of 50 µm. Another alternative would be the use of RIE, although this would require an additional mask and take considerable time. With

this the wafer-level processing is finished and the wafer can be cut into the intermediate subtrates for bonding.
With the fabrication of the substrate finished, the next step is the bonding. First, the chip is bonded to the IS. Assuming gold bumps are deposited on the bondpads of the chip, this can be done by thermocompression or thermosonic bonding. Next an underfill can be applied to the chip, for example by capillary underfill and subsequent thermal curing. As mentioned in section 2.2, applying the underfill to 25% of the distance from the edge to the center is sufficient to achieve the maximum benefit. Alternatively to prevent the underfill being near the RF signals only the corners of the chip can be underfilled or the underfill could also be forgone entirely, although this would worsen thermal performance and increase thermal stresses on the bumps.
If the chip uses solder or indium bumps then the bonding to the IS can be achieved by reflow soldering. However, because a second bonding step follows after the bonding of the chip, it may be preferred to use gold bumps over solder and especially over indium on the chip as the gold bumps would be more resilient to another increase in temperature due to the much higher melting point of gold compared to tin and indium.
After bonding the chip to the IS, for the second bonding step gold bumps are placed at their respective positions on the IS. To achieve the necessary height of the bumps in the range of 100 µm, double-stacked or triple-stacked gold bumps should be considered. After finishing the placement of the gold bumps on the IS the IS is bonded to the PCB. This can be done by thermocompression or alternatively thermosonic bonding.
Depending on the achieved height of the bumps, it may be considered to place a small drop of thermally conducting paste on the backside of the chip before bonding the IS to the PCB to improve thermal conduction of the chip to the PCB during operation. Finally a capillary underfill can be applied and subsequently thermal cured. However the quantity of the underfill should be chosen small enough so that it does not leak into the iGCPW transmission lines where it would lead to increased dielectric losses and a change of the line impedance. Figure 4.1 shows the major processing steps of the process involving stacked gold bumps to connect IS to PCB.

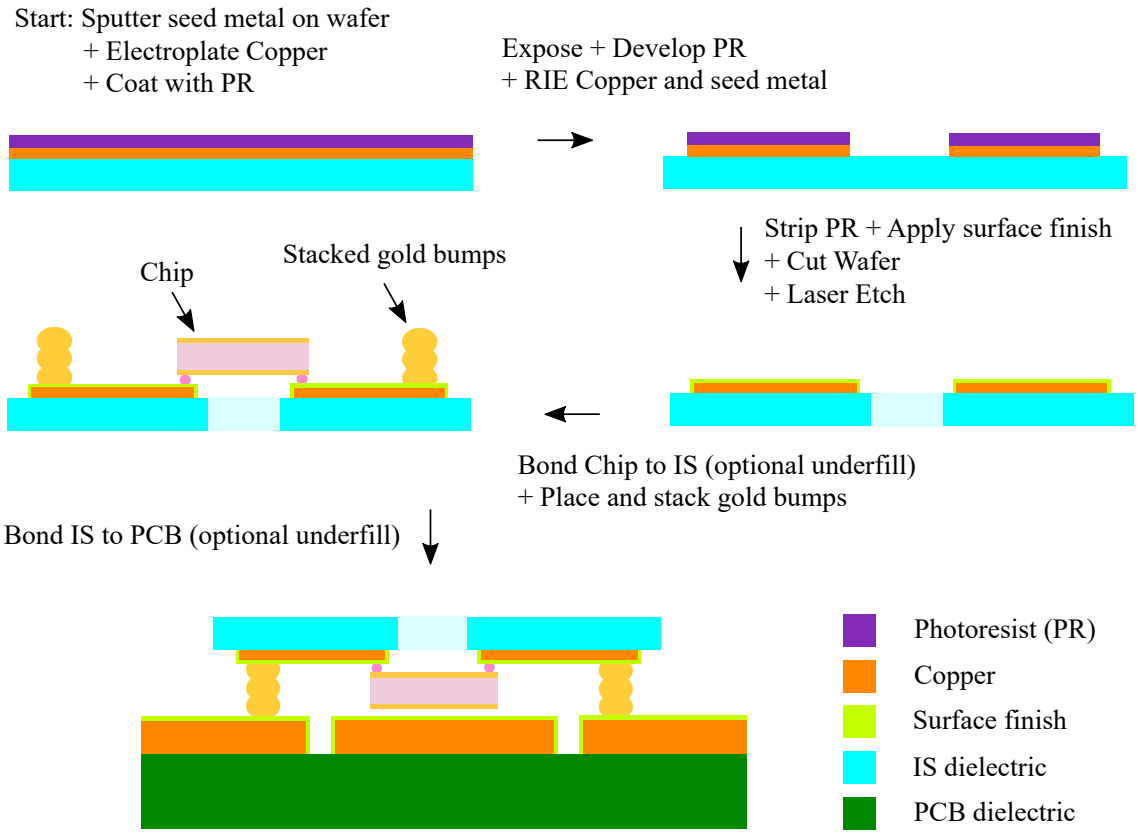


Figure 4.1.: Major processing steps of the proposed process utilizing stacked gold bumps on the IS (not to scale).

As mentioned in section 2.2, due to the potentially improved parallelizability, wafer-level processes, compared to assembly-level processes, may be more suitable for mass fabrication. Analog frontend chips for RF-applications typically have much fewer bond pads than highly integrated CMOS logic chips. The more critical component for manufacturing time of the structures proposed in section 3.3 is the IS. To achieve a uniform height, the IS requires many flip chip bonds. Particularly if stacked gold bumps are used, such as in the process proposed in the beginning of this section, the bumping process may take considerable time occupying a wire bonding machine. While this is acceptable for prototype runs, it could be too costly if used in an assembly line. Instead, in the following a variation of the aforementioned process to fabricate the bumps in a wafer-level process is proposed.

The process using wafer-level produced bumps is the same as the process described in figure 4.1 up until after the application of the surface finish. While it is feasible to use solder for the bumps, doing so would require additional preparation of the bondpads and may require additional consideration such as a solder stop mask for the reflow soldering step. Instead it is proposed to utilize copper pillars. For this a photoresist with a thickness above the required bump height is applied and subsequently structured. In line with the discussion in section 2.2.2 an electroplating step of first nickel to provide a diffusion barrier for the gold surface, then copper, then nickel to form a diffusion barrier between copper and solder and then the lead-free solder follows. The next steps are similar

to the first process in this section. It follows the optional laser drilling to allow for on-chip probing and straightforward BEOL on-chip antennas, cutting the wafer into individual IS and then bonding the chip or chips to each individual IS. Subsequently bonding an IS to a corresponding PCB can be achieved by reflow soldering. An underfill may be applied and the major process steps of the process with wafer-level bumps are shown in figure 4.2.

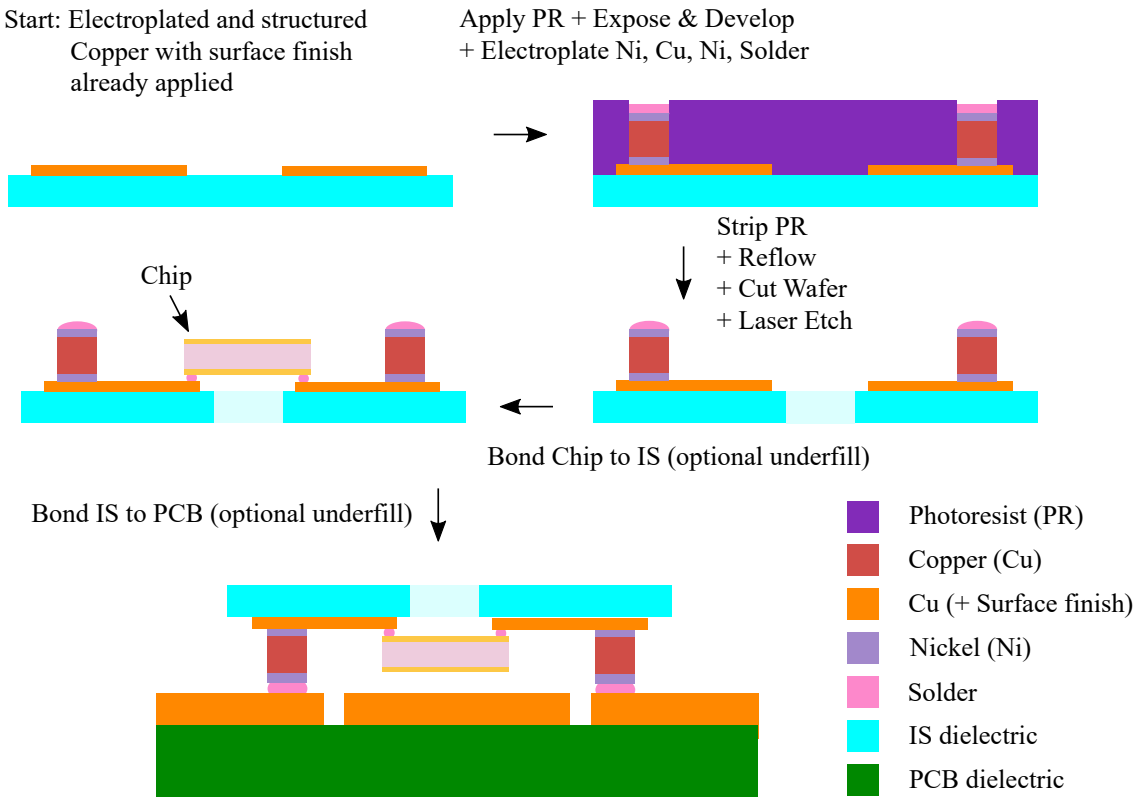


Figure 4.2.: Additional processing steps of the proposed process utilizing wafer-level processed bumps on the IS (not to scale)

As mentioned in section 2.2.2, a potential issue in copper pillars is corrosion. A possible remedy for this is electroplating a corrosion resistant cupronickel alloy instead of the copper layers, one way to achieve such an electroplating is patented by [39], although it has to be investigated how uniform the plating is over an entire wafer. Another potential limitation of this process stems from the use of a very thick photoresist in the order of 120 µm. While Swarbrink et al. (2017) [18] achieved layer thicknesses of their photoresists up to 120 µm for a single coating and up to 250 µm for a double coating, the uniformity of the photoresist thickness may be a critical tolerance for the copper pillar process.

4.2. Critical Tolerances and Thermal Considerations

It was mentioned in section 3.3 that the height of the bumps affects the line impedance of the iGCPW transmission line. Process tolerances in the bump height thus directly affect how good the matching is. Another important tolerance is the shape and placement of the bump connecting the center conductor of the PCB with the center conductor of the IS. To accomodate for a possible variance the outer conductors on the IS are placed further apart from the center conductor near the PCB to IS transition. If the distance near the transition is too small, this could lead to an increase in local capacitance or in the worst case a short. Similarly depending on the size of the bondpad on the chip, the bump connecting the center conductor of the chip and the IS must have a diameter small enough to not exceed the dimensions of the bondpad as this would also induce a local change in capacitance or in the worst case a short. The bumps connecting PCB to IS also have to be chosen high enough so that the chip including the bonds to the IS fit in the space between IS and PCB.

Thermal expansion is an important consideration for the stability of flip chip bonds. For the structure in this work, fused silica has a lower thermal expansion coefficient than alumina, but also a lower thermal conductivity. It can be expected that if a thermal paste is applied on the bottom side of the chip prior to bonding the IS to the PCB, then the thermal performance should be similar or exceed that of a wire bonded chip as the IS has many bumps connecting it to the PCB and both the bumps connecting IS and PCB and those connecting chip to IS are much shorter than a bond wire. However a thermal analysis of the structure is necessary to confirm or deny this estimate. The thermal aspects of the structure could especially become important if no thermal paste is applied on the bottom side of the chip.

4.3. Outlook

Due to the promising results of the simulation, the next step would be to fabricate the proposed structures and subsequently measure them to evaluate how accurate the simulation represents the fabricated structure and how much the tolerances affect the performance of the fabricated devices. The fabrication can use the outline of the processes given in this chapter. The process using stacked gold bumps may be less expensive for a prototype run as it is less complex and requires one less mask. However, it may have to be further refined if unforeseen problems appear during fabrication as the processes are new.

Evaluating the structure for higher frequencies, particularly for the chip-to-chip connection, could be another avenue of research. However, it can be expected that metal losses and radiation increase at higher frequencies and new parasitic modes, particularly of surface waves might appear on the IS. Depending on the results of the fabrication, the approach of using the IS-PCB-structure can be expanded to realize on-IS antennas. This is similar to an approach by Beer et al. [28] where an antenna is placed inside the package and connected to the chip via flip chip techniques. Another possible improvement could be achieved by coating the back side of the IS with a metal to achieve a structure resembling inhomogenous stripline. This could potentially reduce radiation losses, but

would require another mask to remove parts of the back side metal on the IS if the chip or chips of a chipset have on-chip antennas, require probing after bonding or for optical inspection of the structure. M. Ito and T. Marumoto (2018) [40] demonstrate laser-drilled vias in fused silica. The use of vias could also be investigated as a possible remedy against parasitic modes such as surface waves. Figure 4.3 shows a sketch of the cross section of a combination of stripline and IS-vias as a possible structure for future investigation.

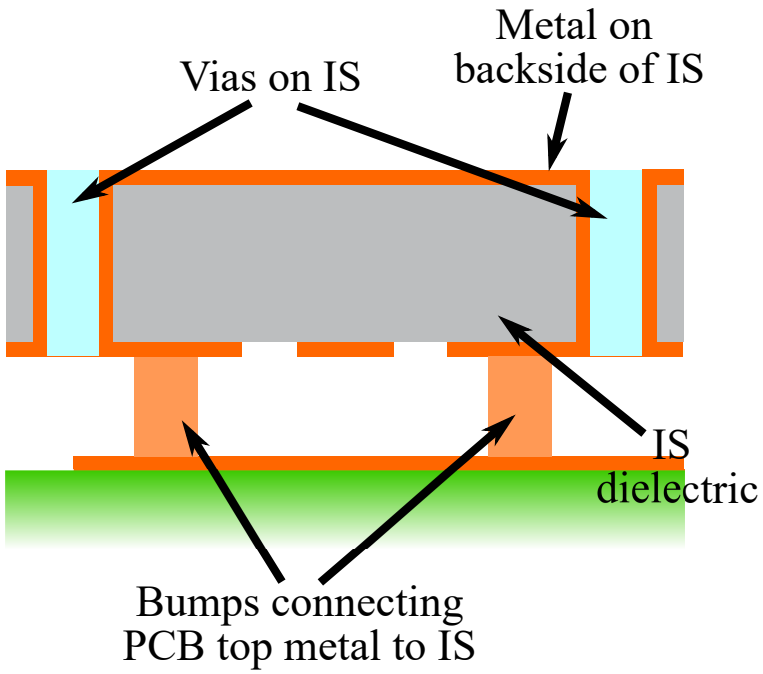


Figure 4.3.: Proposed stripline structure using vias on the IS

Other potential topics for investigation are the influence of the IS on chip operation and especially antenna characteristics of BEOL on-chip antennas if the IS is not removed over parts of a chip as well as a thermal analysis of the system for a given chip.

5. Conclusion

In this work flip chip transitions were investigated for their suitability for connecting chips with each other and with a PCB in the frequency range of up to 100 GHz. It was found that microstrip line transitions show high radiation losses at the transition and CPW based transitions are more straightforward to use. While regularly flip-chipped devices can be prone to coupling from substrate modes and pose great challenge to realize functioning BEOL on-chip antennas, the hot via approach is one way to solve these issues. The flip chip bonds of chips bonded with the hot via approach, however, are difficult to verify and require a back side lithographic step for the chip.
The new approach proposed in this work, using an IS with two bonding steps and using the PCB as part of the fundamental mode of propagation on that IS, is designed to solve these challenges. Both for connections between a chip and a PCB and between two chips the simulated results indicate very good broadband matching with a resilience to production tolerances, particularly the bump dimensions. A potential limitation of the new approach is the appearance of parasitic resonances at the transition from the PCB to the IS if the vias in the PCB GCPW are placed too far from the center of the transmission line. Another limitation corresponding to a maximum usable frequency limit was the simulated excitation of surface waves in the form of dielectric slab modes if the IS is chosen as too electrically large. For this reason fused silica may be preferred over alumina substrates if the structure is considered for larger IS thicknesses or frequencies higher than 100 GHz.
For the new approach the minimum achieved insertion loss at 100 GHz is 0.58 dB for a connection between PCB and chip over a 1 mm long iGCPW on the IS. For a connection between two chips placed 2 mm apart, the minimum simulated insertion loss at 100 GHz is 0.77 dB leading to approximately 0.24 dB insertion loss for each of the two transitions between the IS and the chips. The system thus allows for much larger distances between chips than contemporary wire bonds and direct chip to chip interconnects. A comparison of the proposed approach to contemporary technologies for broadband connections at 100 GHz of chips to each other and to PCBs is shown in table 5.1. S21 is for a single transition without line loss (*) or from a chip to a substrate at 100 GHz including all losses (**).
The approach in this work shows lower losses than the wire bonds in [1] and a single transition shows slightly higher insertion loss at 100 GHz for one transition than [2] and [3]. However, as the IS in the approach of this work is made of fused silica, it can be expected that the bonding step and manufacture is more straightforward than for a LCP as in [3]. Due to the larger dimensions of the IS compared to a chip it can be expected for the bonding to be more straightforward in the approach of this work than the direct chip to chip interconnections in [2].

	[1]	[2]	[3]	This work
Technology used	Wire bonds	Chip interconnects	Flip chip	Flip chip with IS
S21 (transition)	−0.8 dB*	−0.2 dB*	−0.15 dB**	−0.24 dB*/−0.58 dB**
Line loss in $dB\,mm^{-1}$	n/a	n/a	0.153	0.15
BEOL on-chip antennas	yes	n/a	difficult	yes
Carrier	glass	silicon	LCP	fused silica + PCB

Table 5.1.: Comparison between other contemporary works and this work
*For connections between chips, the approach of this work needs two transitions to connect chips
**For connections between a chip and a PCB or substrate

It is concluded that flip chip techniques show great promise to deliver a robust, broadband and low loss connection between PCB and chip and between different chips. Flip chip can thus be considered to supplant wire bonds in the frequency range of up to 100 GHz, for example by fabricating the approach proposed in this work with the process outlines provided in chapter 4.

6. Acknowledgments

I would like to thank Prof. Dr.-Ing. Ingmar Kallfass for giving me the opportunity to work on this research project at the Institute of Robust Power Semiconductor Systems. I would like to thank my supervisor M.Sc. Moritz Vischer for his continuous guidance, the very many insightful discussions and for providing help whenever I had questions. I would also like to thank Dipl.-Ing. Holger Baur from the Institute of Large Area Microelectronics for providing feedback with regards to the manufacturability of the proposed processes. I would like to thank the entire staff at ILH and my colleagues in the student room for the great working environment. In addition to that I would like to thank my family and friends and especially my parents and my friend Daniel Tandler for the great mental support they gave me while I was working on this research project during the global pandemic.

A. Additional Simulation Results

In this appendix additional simulation results regarding the structures discussed in chapter 3 are shown.

A.1. Regular Flip Chip

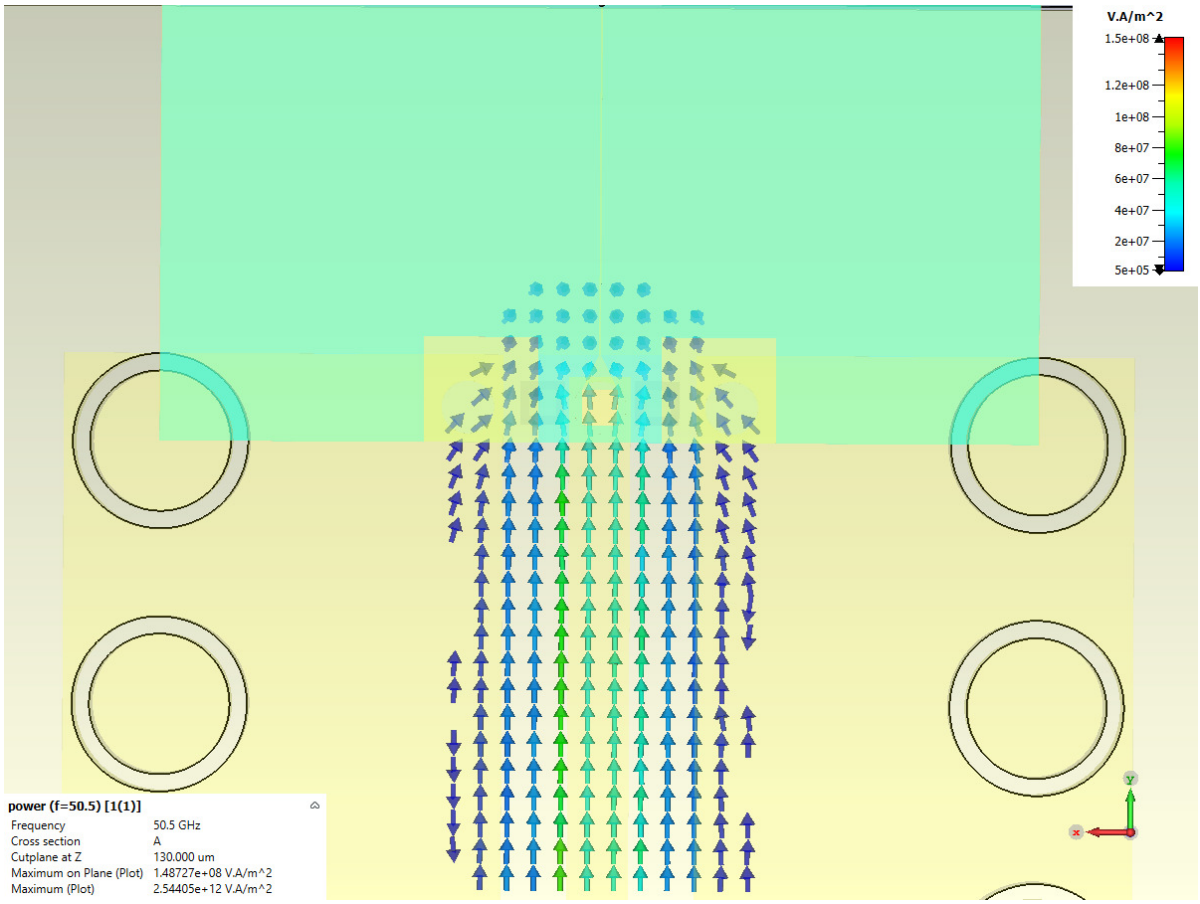
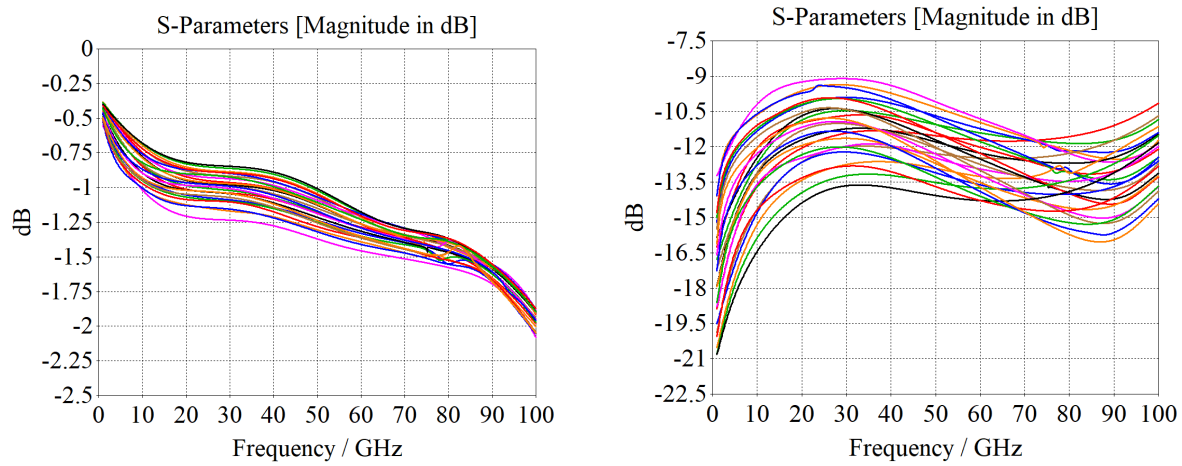


Figure A.1.: Power Flow of the regular flip chip transition using GCPW, the lower scale is the same as for the microstrip line transition.

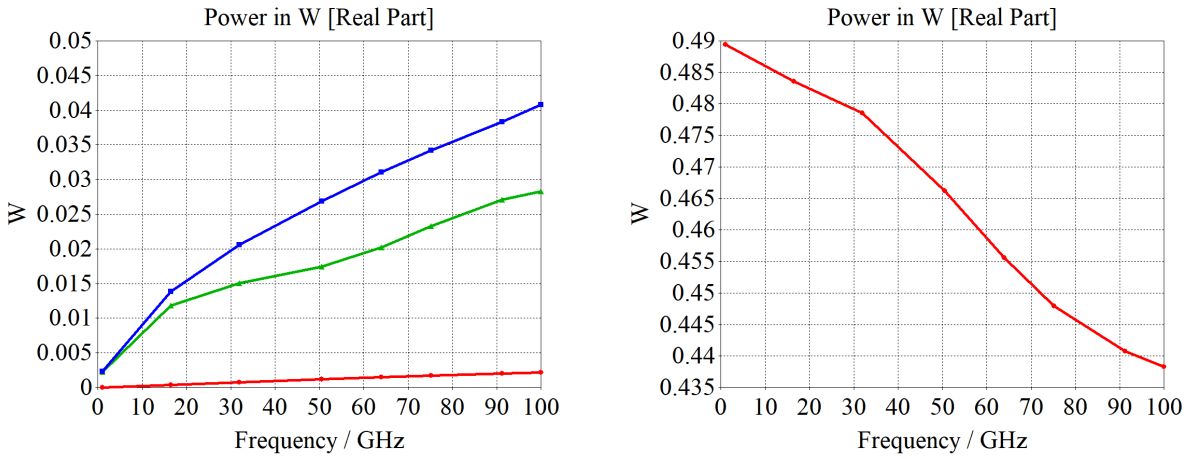
A.2. Hot Via



(a) S21 **(b)** S11

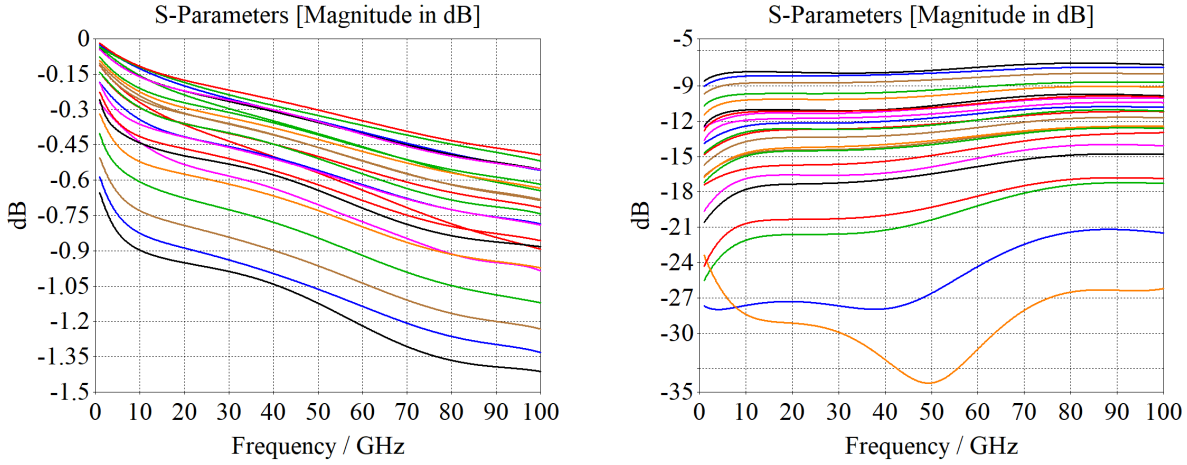
Figure A.2.: Parametric evaluation for changing center conductor widths and distances between center and outer conductor of the hot via approach.

A.3. IS to Chip



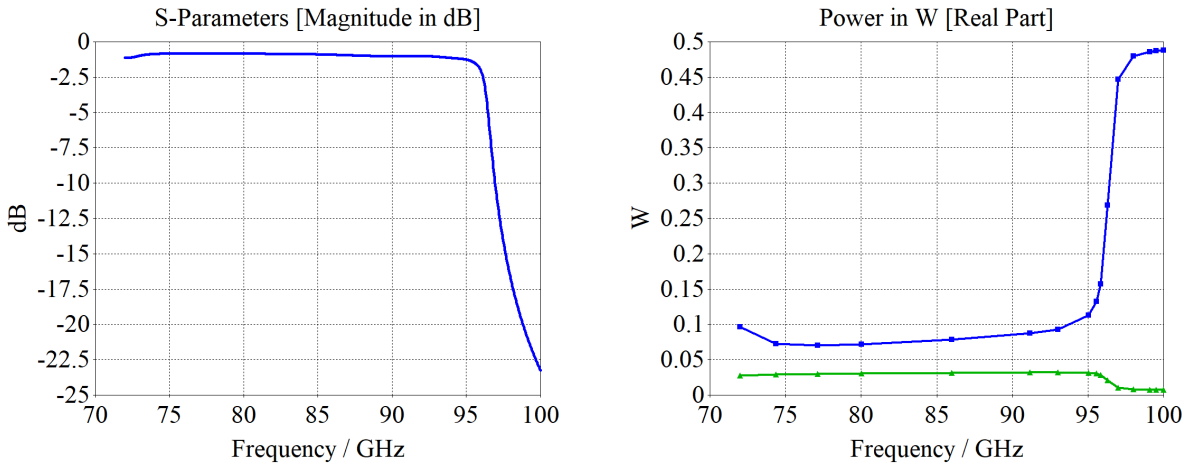
(a) **(b)**

Figure A.3.: Different loss contributions for the IS to chip transition.
(a) shows power accepted (blue), consisting of metal losses (green), dielectric losses (red) and radiation (not shown).
(b) shows power accepted by the feeding port, 0.5 W would mean no return loss, 0 W would mean 100% return loss.



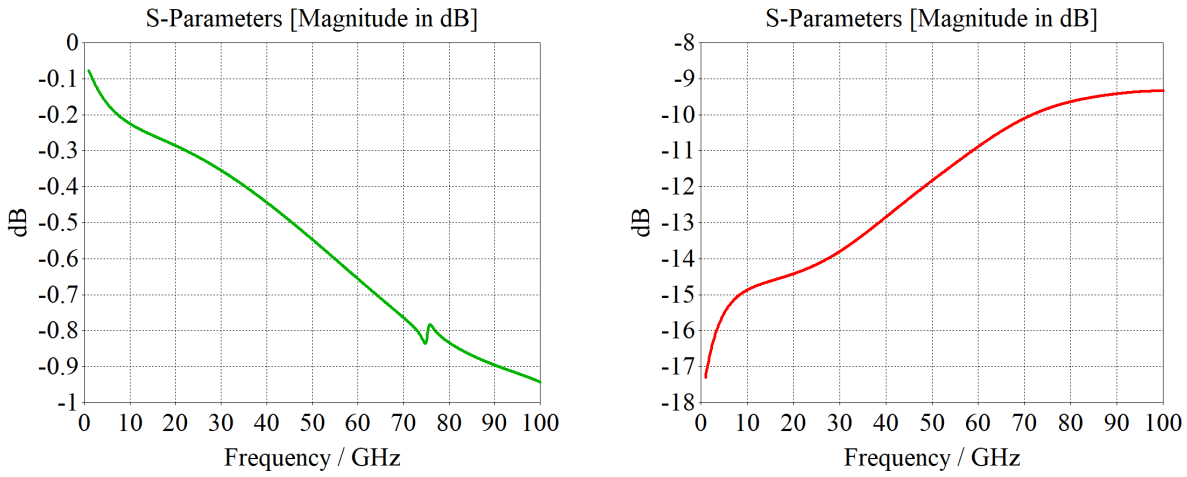
(a) S21 **(b)** S11

Figure A.4.: Full parametric evaluation of changing center conductor width and distance between center and outer conductors without a taper.



(a) S21 **(b)** Power accepted

Figure A.5.: Surface waves in a 500 µm thick alumina IS.
(b) shows the increase in radiation (difference of blue and green curves) due to the dielectric slab mode being out of the cutoff region above approximately 95 GHz.



(a) S21 **(b)** S11

Figure A.6.: S-parameters of the transition without the compensating bumps near the transition.

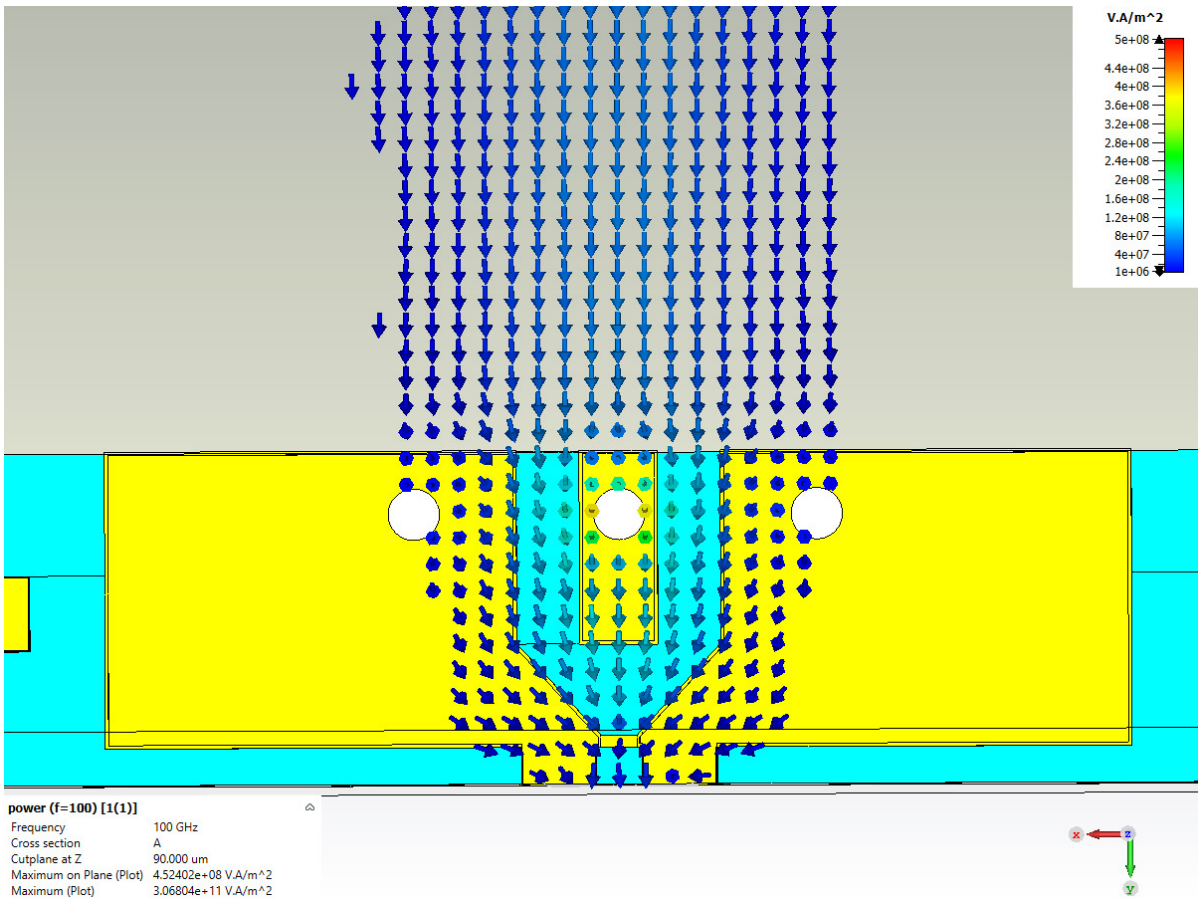
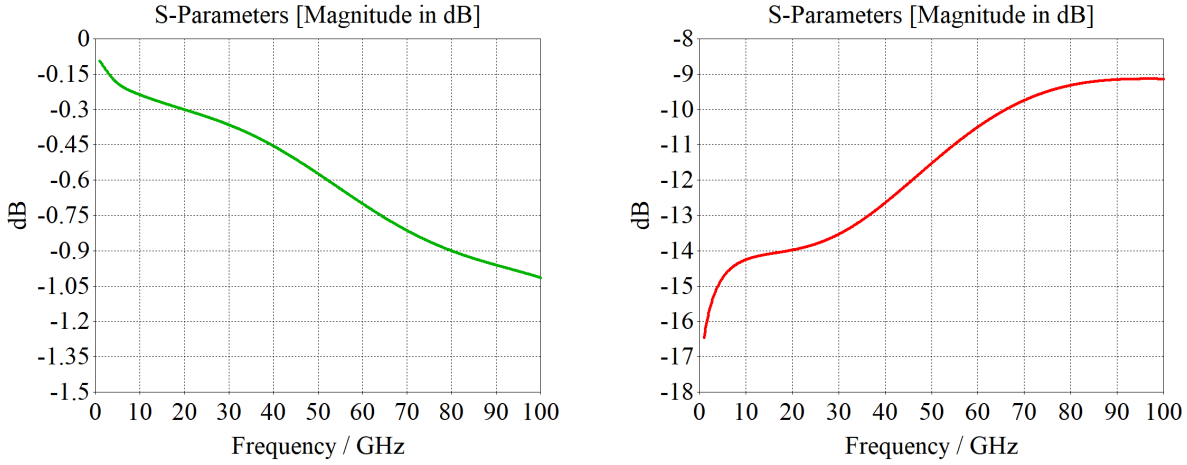


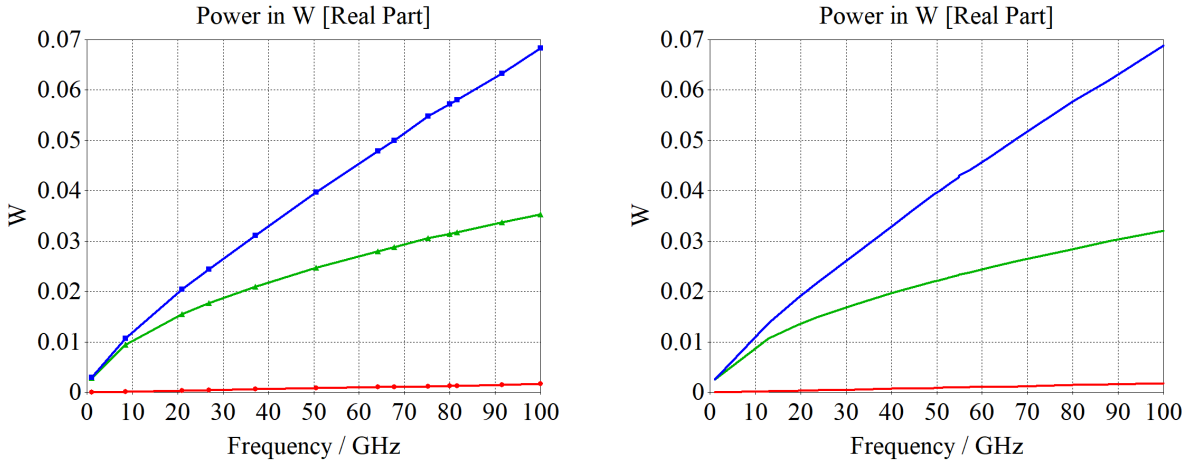
Figure A.7.: Power Flow without the compensating bumps near the transition.



(a) S21 **(b)** S11

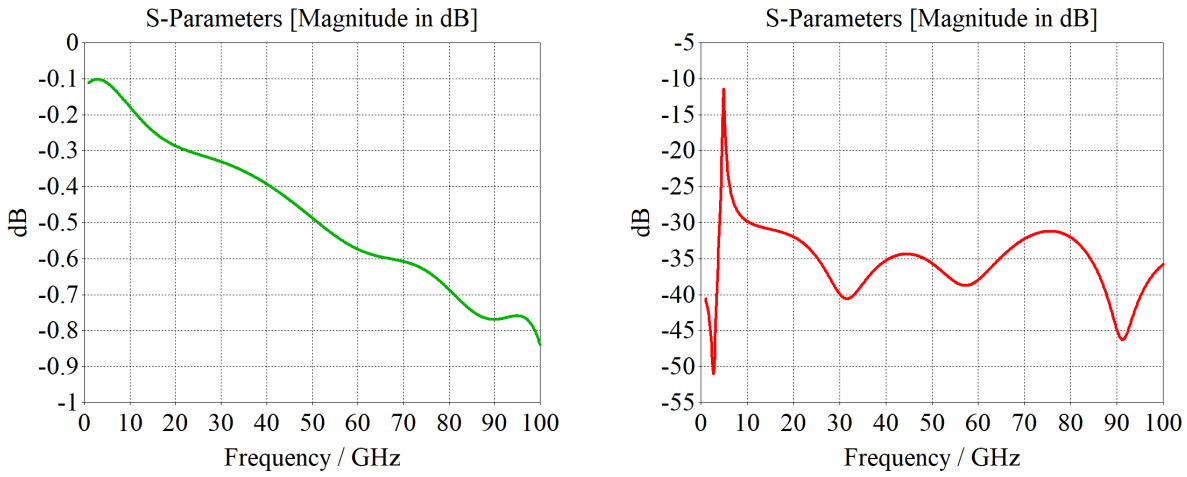
Figure A.8.: S-parameters of the transition without a PCB top metal beneath the chip.

A.4. Transmission Line Loss



(a) 70 µm height **(b)** 130 µm height

Figure A.9.: Comparison of different loss mechanisms of the iGCPW for a center conductor width of 80 µm, a distance between center and outer conductors of 40 µm and bump heights of 70 µm and 130 µm.
While metal losses (green) are lower for the height of 130 µm radiation losses increase, leading to a very similar total power accepted (blue). Dielectric losses (red) are an order of magnitude lower.



(a) S21 **(b)** S11

Figure A.10.: S-parameters for the two subsequent 45° bends without bumps connecting PCB to IS.

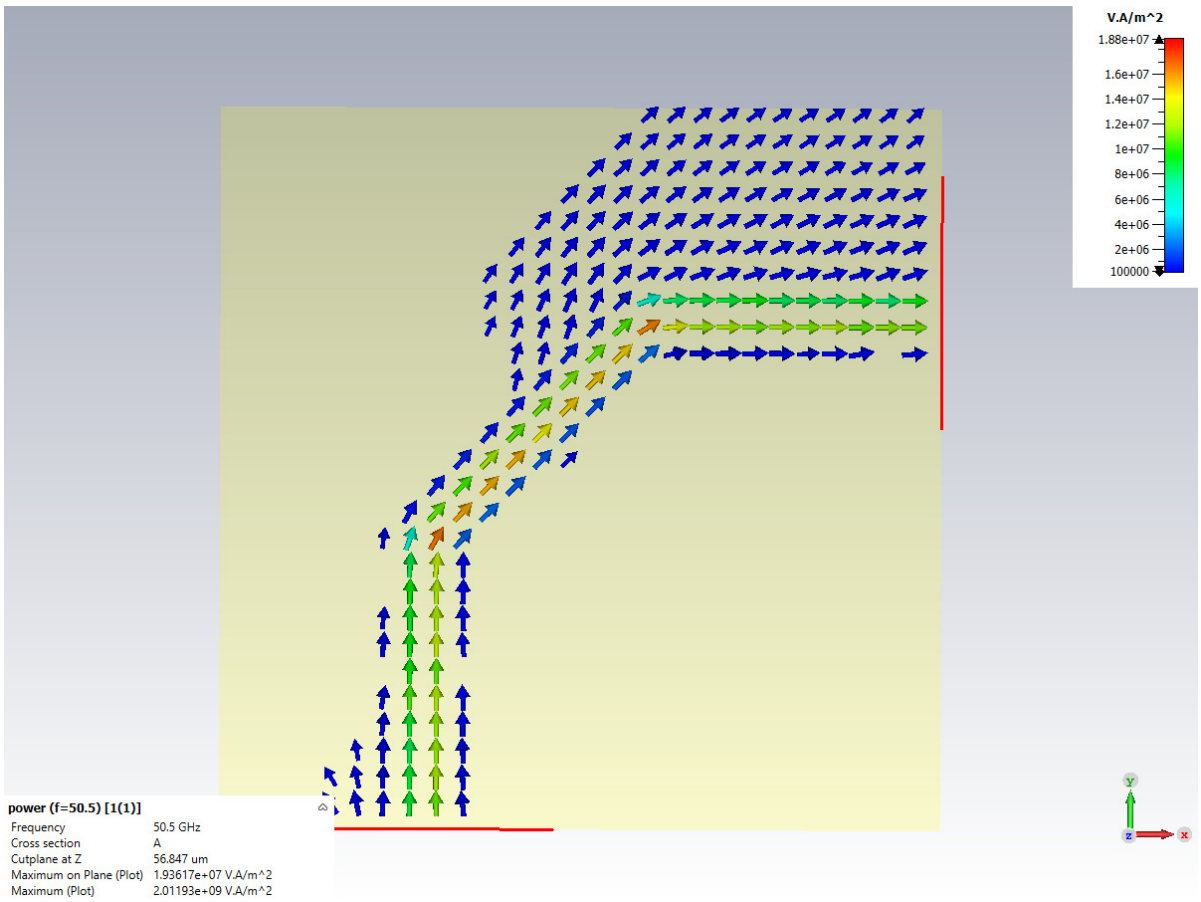
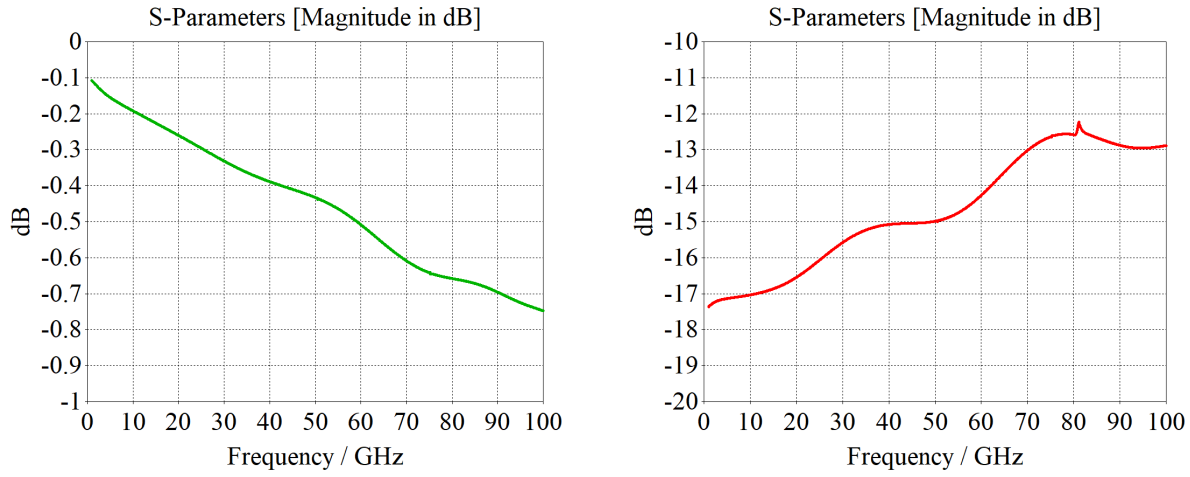


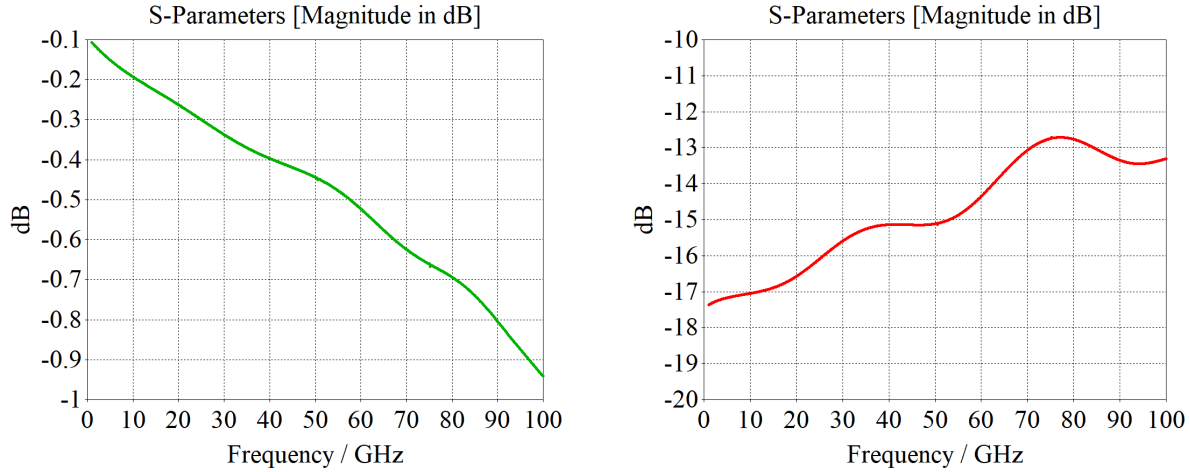
Figure A.11.: Power flow at the two subsequent 45° bends without bumps connecting PCB to IS, the cutting plane is between the IS and the PCB.
Some radiation occurs particularly at the second bend.

A.5. PCB to IS



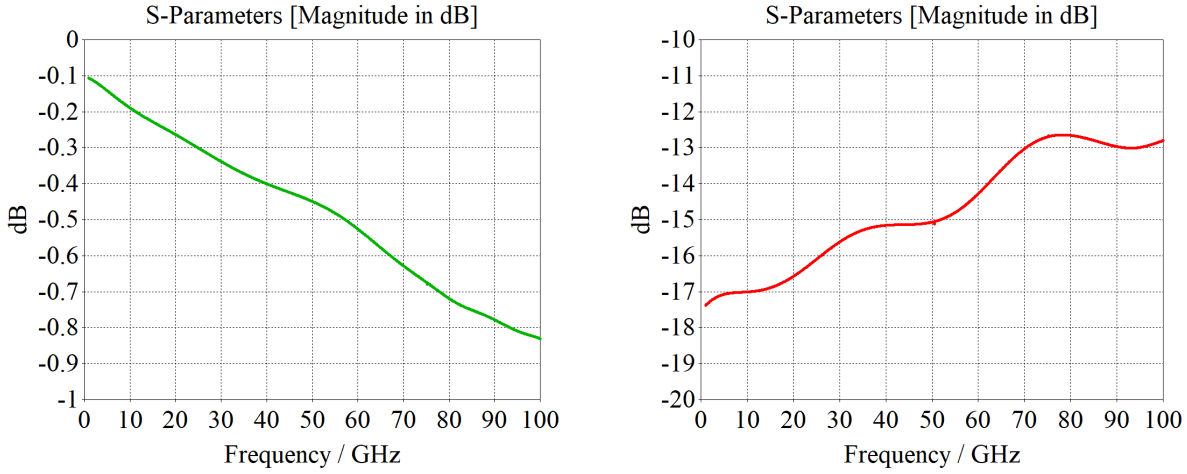
(a) S21 **(b)** S11

Figure A.12.: S-parameters of the PCB to IS transition using regular vias.



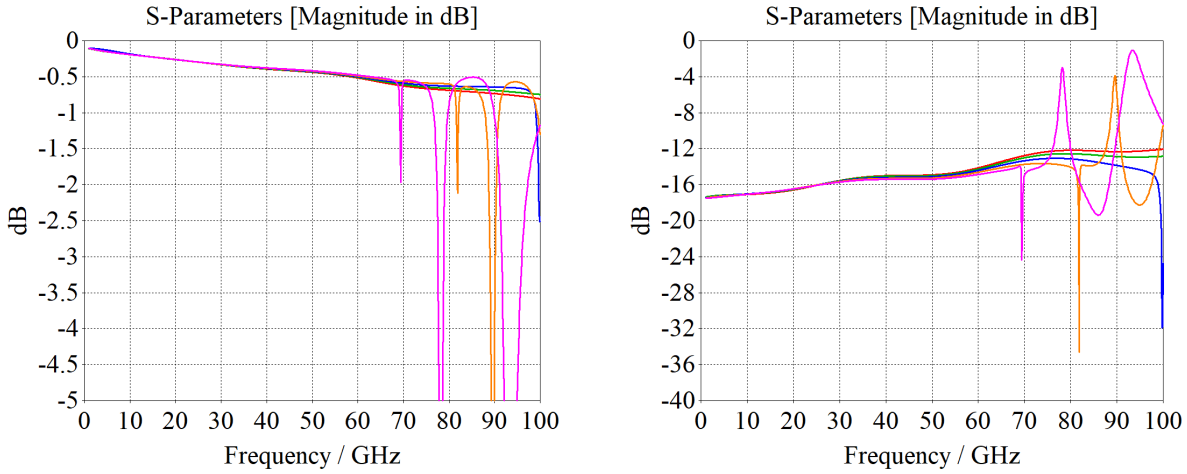
(a) S21 **(b)** S11

Figure A.13.: S-parameters of the PCB to IS transition using no vias.



(a) S21 **(b)** S11

Figure A.14.: S-parameters of the PCB to IS transition using blind vias.



(a) S21 **(b)** S11

Figure A.15.: Parametric evaluation of the notch filter characteristic for a center conductor width of 100 µm.

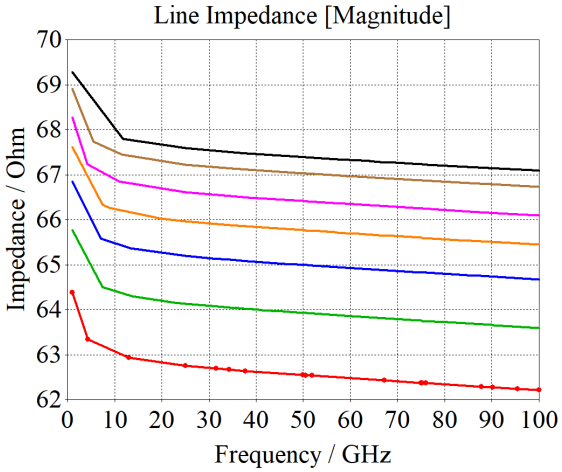
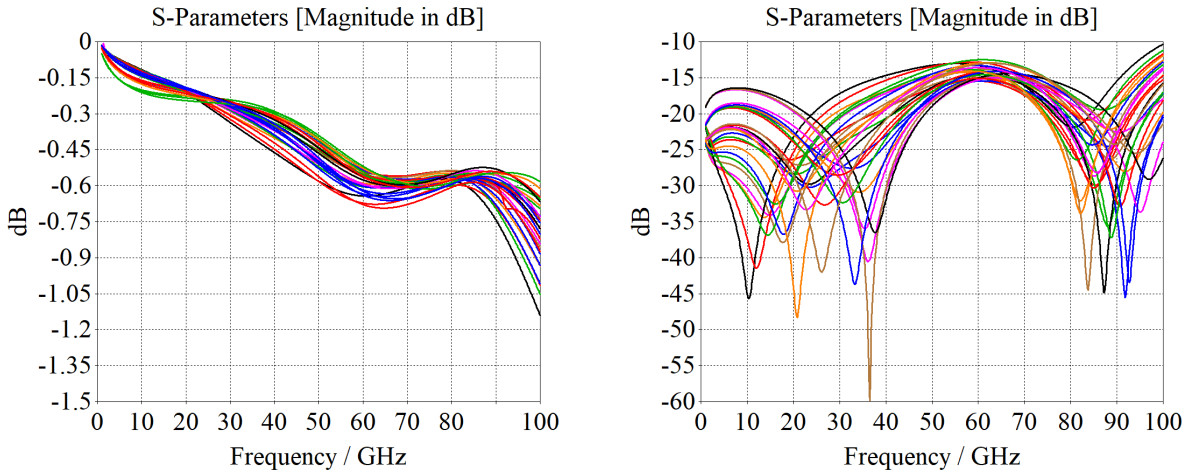


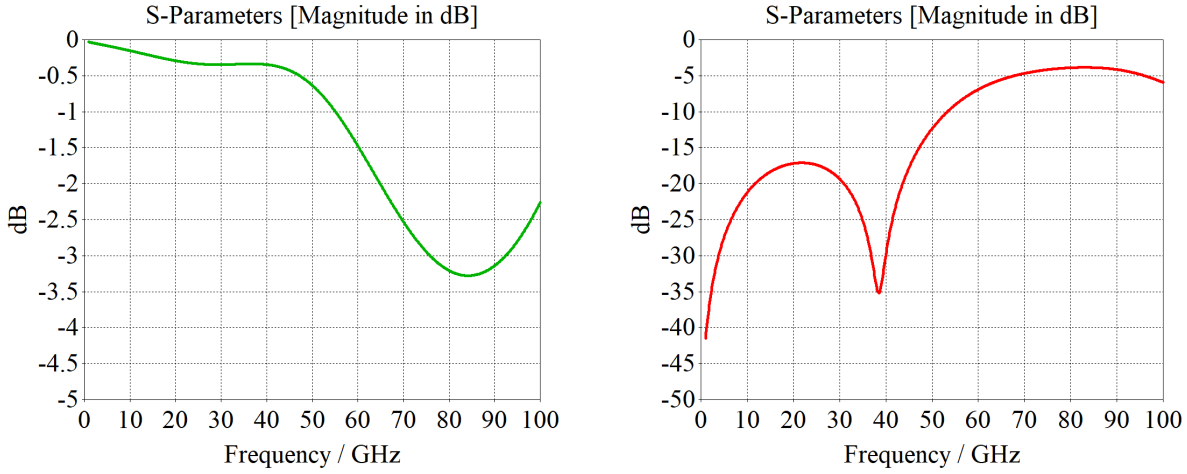
Figure A.16.: Influence of changing bump height on line impedance of the iGCPW fundamental mode.
The red curve is for a bump height of 70 µm, the black curve for a bump height of 130 µm and the lines inbetween show an increment of 10 µm between adjacent lines

A.6. full system



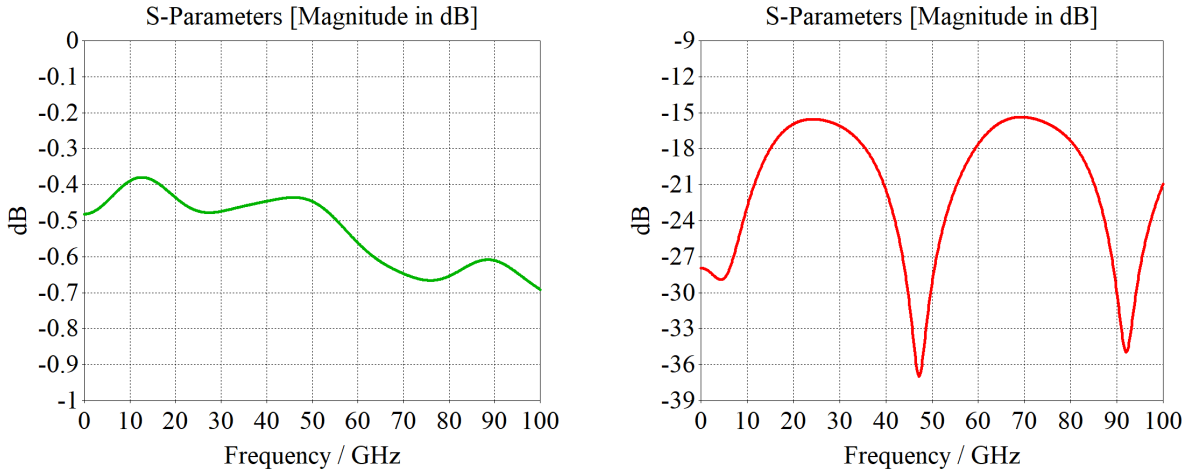
(a) S21 **(b)** S11

Figure A.17.: Full parametric simulation result for the bump height and PCB transmission line variation.



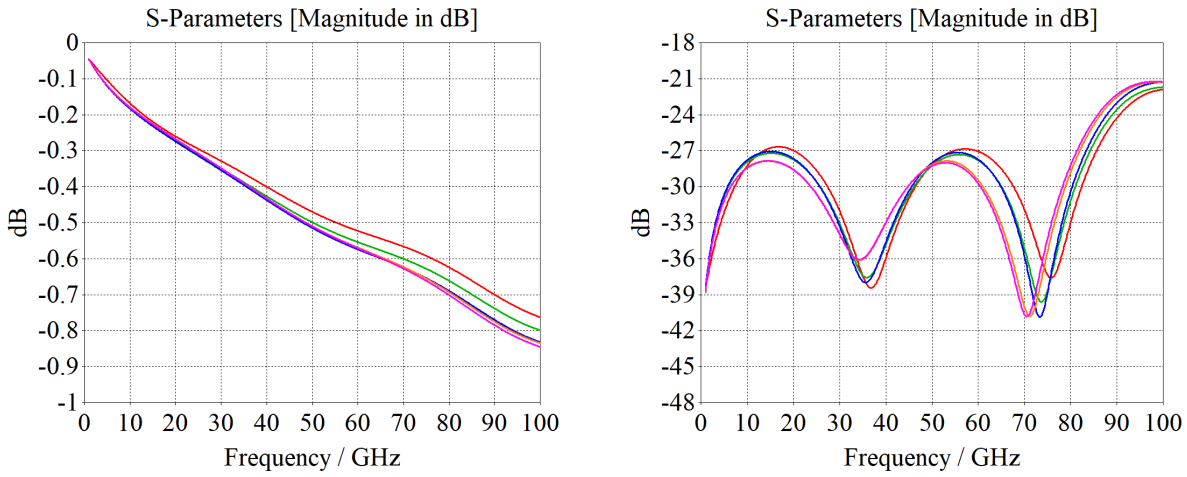
(a) S21 **(b)** S11

Figure A.18.: Simulated results of the chip to chip connection with tapers.



(a) S21 **(b)** S11

Figure A.19.: Simulated results of the chip to chip connection with the time domain solver.



(a) S21 **(b)** S11

Figure A.20.: Parametric evaluation of the height variation for the chip to chip connection.

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