Switching Characteristics of Integrated GaN-on-Si Half-Bridge and Driver Circuits

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Executive Summary

This work examines particularities in the switching characteristics of gallium nitride (GaN) half-bridge and driver circuits, which arise from the integration on a common conductive silicon (Si) substrate, or from the operation of discrete devices on an electrically coupled Si substrate. The supposed advantages of monolithic integrated half-bridges and drivers are promising: The reduced parasitic interconnect inductance improves voltage-switching transitions. The Si carrier allows low-cost and large-scale fabrication. A single integrated IC simplifies the assembly compared to conventional multi-chip power modules.

However, the operation of such monolithic GaN-on-Si power circuits also evokes substrate-related effects, especially at elevated operation voltages, which were previously not relevant for single low-side GaN HEMTs.

On the one hand, deteriorating effects such as on-resistance increase by negative substrate biasing (back-gating) have to be considered. On the other hand, beneficial effects such as the possibility of decoupling of substrate capacitances can be exploited for reduction of switching energies and consequently increased efficiencies compared to conventional discrete GaN power transistors. Furthermore, even though the monolithic integration of a gate driver with a power transistor reduces the interconnect parasitics between the driver and the transistor, still external interconnects to decoupling capacitors are required. The monolithic integration of half-bridges and drivers thus does not fully eliminate parasitic gate-loop and power-loop inductance. Therefore, advanced assembly technologies such as PCB-embedding of GaN-based power integrated circuits should also be considered in combination with the monolithic circuit integration.

First, this work provides a theoretical framework to calculate and compare the effect of substrate-capacitances on application-oriented half-bridge capacitances for different feasible substrate terminations of discrete and monolithic GaN-on-Si half-bridges. It is explained and verified how floating substrate terminations reduce the effective output capacitances. To harness the benefits of this reduced effective capacitances, an improved passive substrate biasing network for monolithic half-bridges is proposed and experimentally verified: The proposed operation scheme for monolithic half-bridges avoids negative back-gating in all operation points of a dc-dc converter and at the same time has reduced effective output capacitance compared to a discrete half-bridge. Experimental operation of a monolithic half-bridge with the proposed substrate biasing network shows increased efficiency compared to a discrete half-bridge and verifies the effectiveness of the proposed duty-cycle independent floating substrate biasing. Compared to a conventional discrete half-bridge with two substrate-to-source terminated transistors, this work's operation scheme for a monolithic half-bridge in a dc-dc converter with 200 V input voltage, 100 V output voltage, 1.5 A load current and 100 kHz switching frequency, reduced the switching energies by over 20%, and the total power loss in a dc-dc converter by over 10%. This efficiency improvement is the results of this work's beneficial combination of a (semi-)floating substrate which reduces the effective output capacitance, and the novel

substrate biasing network which avoids negative back-gating during conduction phases by shifting the average substrate voltage towards higher values.

Then, this work work analyzes high slew-rate voltage switching transitions and the effect of parasitic inductance in the power-loop on switch-node overshoot voltage. An equivalent circuit analysis is carried out, which takes the limited voltage slew-rate of a power transistor into account. In contrast to a simplified RLC-circuit analysis with a infinitely fast voltage excitation pulse, this work analytically provides insight into the dependency of switch-node overshoot voltage on the voltage transition time. Even though the power-loop is almost undamped due to the low on-resistance of the transistors, the analysis shows that local minima of overshoot as a function of switching time exist, and by selection of optimal switching times it is possible to minimize the overshoot without a significant reduction of switching speed. Furthermore, an advanced PCB-embedded packaging technology is combined with on-package gate and dc-link capacitors, which further reduces parasitic inductance of GaN half-bridges with integrated drivers.

Finally, this work exposes that the substrate-to-source termination of a lateral GaN power transistor, which is typically realized on the packaging level, forms a third parasitic loop. In addition to the well-known parasitic gate-loop and power-loop inductance, this work analyzes the effects of this substrate-loop inductance. An analytical and experimental stability analysis is carried out. Countermeasures are proposed to avoid instabilities from the parasitic-substrate loop. A substrate damping circuit is proposed, which avoids instabilities by damping of the substrate-loop, without slowing down of the switching transition.

The experimental and theoretical investigation and results of this work on the switching characteristic of GaN-on-Si half-bridges with drivers on conductive Si substrates contributes to unlock the benefits of GaN HEMTs and monolithic power circuit integration for compact, clean switching and highly efficient power electronics.

Zusammenfassung

Diese Arbeit untersucht Besonderheiten im Schaltverhalten von Galliumnitrid-basierten (GaN) Halbbrücken und Treiberschaltungen, die durch die Integration auf einem gemeinsamen leitfähigen Silizium (Si) Substrat verursacht werden. Die angenommenen Vorteile von monolithisch integrierten Halbbrücken und Treibern sind vielversprechend: Die reduzierte parasitäre Verdrahtungsinduktivität verbessert Spannungs-Schaltvorgänge. Der Si-Träger erlaubt eine kostengünstige Herstellung im großen Maßstab. Eine einzige integrierte Schaltung (IC) vereinfacht die Aufbautechnik im Vergleich zu konventionellen Multi-Chip Modulen.

Allerdings verursacht der Betrieb von solchen monolithischen GaN-on-Si Leistungsschaltungen auch substratbezogene Effekte, besonders bei erhöhten Betriebsspannungen, die bisher für den Betrieb von Einzeltransistoren nicht relevant waren.

Einerseits müssen Degradationseffekte wie die Erhöhung des Leitwiderstandes durch negative Substratspannung (back-gating) berücksichtigt werden. Andererseits können aber auch vorteilhafte Effekte, wie etwa die Möglichkeit Substratkapazitäten zu entkoppeln, ausgenutzt werden um Schaltenergien zu reduzieren, und folglich den Wirkungsgrad im Vergleich zu konventionellen GaN Einzeltransistoren zu erhöhen. Obwohl die monolithische Integration von Treiber und Leistungstransistor die Verdrahtungsparasiten zwischen Treiber und Transistor reduziert, so sind doch weiterhin noch externe Verdrahtungen zu Entkoppelkondensatoren notwendig. Die monolithische Integration von Halbbrücken und Treibern eliminiert also nicht alle parasitären Induktivitäten in der Gate- und Leistungsschleife. Deshalb werden in dieser Arbeit auch fortschrittliche Aufbautechniken wie das Leiterplatten-Embedding von GaN Leistungsschaltungen in Kombination mit monolithischer Integration in Betracht gezogen.

Als Erstes erstellt diese Arbeit einen theoretischen Rahmen, um den Effekt von Substratkapazitäten auf die anwendungsnahen effektiven Halbbrückenkapazitäten für verschiedene mögliche Substrat Anschlussvarianten von diskreten und monolithischen GaN-on-Si Halbbrücken zu berechnen. Es wird erklärt und überprüft wie ein floatender Substratanschluss die effektive Ausgangskapazität reduziert. Um die Vorteile dieser reduzierten effektiven Kapazität nutzbar zu machen, wird ein verbessertes passives Substrat-Vorspannungsnetzwerk für monolithische Halbbrücken vorgeschlagen und experimentell verifiziert: Die vorgeschlagene Betriebsweise für monolithische Halbbrücken vermeidet negatives back-gating in allen Arbeitspunkten von DC-DC Wandlern, wobei die Reduktion der effektiven Ausgangskapazität im Vergleich zu diskreten Halbbrücken beibehalten wird.

Der experimentelle Betrieb einer monolithischen Halbbrücke mit dem vorgeschlagenen Substrat-Vorspannungsnetzwerk zeigt einen erhöhten Wirkungsgrad, verglichen mit einer diskreten Halbbrücke, und verifiziert damit die Wirksamkeit des vorgeschlagenen Tastgrad-unabhängigen Substrat-Vorspannungsnetzwerks. Im Vergleich zu einer konventionellen Halbbrücke mit zwei Transistoren die jeweils eine Substrat-zu-Source Verbindung

aufweisen, reduziert die vorgeschlagene Betriebsweise für monolithische Halbbrücken in einem DC-DC Wandler mit 200 V Eingangsspannung, 100 V Ausgangsspannung, 1.5 A Laststrom und 100 kHz Schaltfrequenz die Schaltenergien um über 20%, und die gesamte Verlustleistung in einem DC-DC Wandler um über 10%. Diese Wirkungsgradverbesserung ist das Ergebnis der in dieser Arbeit vorteilhaften Kombination eines (semi)-floatenden Substrats, was die effektive Ausgangskapazität reduziert, und des neuen Substrat-Vorspannungsnetzwerks, welches negative back-gating Spannungen während der Leitphasen durch Verschieben der mittleren Substratspannung hin zu positiven Spannungen vermeidet

Dann untersucht diese Arbeit den Spannungsverlauf bei Schaltvorgängen mit hoher Anstiegsgeschwindigkeit, und den Effekt parasitärer Induktivitäten in der Leistungsschleife auf Spannungsüberschwingungen am Schaltknoten. Eine auf Ersatzschaltplänen basierte Schaltungsanalyse wird durchgeführt, wobei die limitierte Anstiegsgeschwindigkeit der Spannung berücksichtigt wird. Im Vergleich zu einer vereinfachten Schaltungsanalyse eines Resonanzkreises mit einer unendlich schnellen Spannungssprung-Anregung gewährt diese Arbeit Einblicke in die Abhängigkeit der Überspannung von der Spannungsanstiegszeit. Obwohl die Leistungsschleife aufgrund des niedrigen Leitwiderstandes der Transistoren nahezu ungedämpft ist, wird gezeigt dass lokale Minima von Überspannung als Funktion der Schaltgeschwindigkeit existieren. Durch Wahl einer optimalen Schaltzeit ist es deshalb möglich die Spannungsüberschwingungen zu minimieren, und das ohne eine erhebliche Reduzierung der Schaltgeschwindigkeit. Des weiteren wird eine fortschrittliche Leiterplatten-Embedding Technologie von GaN ICs mit Gate- und DC-Link Kapazitäten direkt auf dem Gehäuse kombiniert. Dies reduziert die parasitäre Induktivität der GaN Halbbrücke mit integriertem Treiber auch auf Gehäuseebene.

Abschließend offenbart diese Arbeit, das die Substrat-zu-Source Verbindung von lateralen GaN Leistungstransistoren, so wie diese typischerweise auf Gehäuseebene realisiert ist, eine dritte parasitäre Schleife bildet. Zusätzlich zu den bekannten parasitären Gate- und Leistungspfad-Schleifen untersucht diese Arbeit den Effekt der parasitären Substrat-Schleifeninduktivität. Analytisch und experimentell wird die Stabilität von Schaltvorgängen untersucht. Um durch das Substrat ausgelöse Instabilitäten zu vermeiden werden Gegenmaßnahmen vorgeschlagen. Eine Dämpfungsschaltung für die Substrat-Schleife wird vorgeschlagen, welche Instabiltiäten nicht durch Reduzieren der Schaltgeschiwndigkeit, sondern durch das Dämpfen der Substrat-Schleife erreicht.

Die experimentellen und theoretischen Untersuchungen sowie Ergebnisse dieser Arbeit zum Schaltverhalten von GaN-on-Si Halbbrücken mit Treibern auf leitfähigem Si-Substrat tragen dazu bei die Vorteile von GaN HEMTs und monolitischer Integration von Leistungsschaltungen für kompakte, sauber schaltende und hoch effiziente Leistungselektronik nutzbar zu machen.

1 Introduction

1.1 Background

After the invention of the field-effect transistor (FET) [1] and the development of semiconductor technologies to fabricate them on large-scale wafers, multiple application branches emerged, which all benefit our everyday life, society, environment and were enablers for modern industry. Power electronics is one key application of transistors, and was aptly described by T.G. Wilson [2] as

> "the technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form"

with the goal

> "to control the flow of energy from an electrical source to an electrical load with high efficiency, high availability, high reliability, small size, light weight, and low cost."

For example, an on-board charger in an electric vehicle converts thousands of Watts electrical power from a sinusoidal 50 Hz alternating-current (ac) 230 V grid-voltage to an isolated direct-current (dc) higher battery voltage, for example 400 V [3]. Further power electronics then provides power conversion from the battery to 24 V electrical loads [4]. For data processing and computing the voltages are further converted down to below 1 V processor voltages [5]. Power electronics uses switched-mode power converter topologies (class-d) with at least one switched power transistor and at least one additional reactive intermediate energy storage component such as a power inductor. Compared to linear voltage regulators or other amplifier classes, the switched-mode converter approach can achieve ultra high power converter efficiencies exceeding 99% [6]. High efficiencies require a low conduction voltage of the power transistors, since it is in series to the power path.

Power MOSFETs as unipolar devices are traditionally used for highly efficient converters, since they have a low and ohmic on-resistance, compared to bipolar devices [7]. To reach low on-resistances, the size of the transistors can be increased. However, since the transistors are used for voltage-switching with a high frequency, additional switching loss then reduces the efficiency. The switching loss is also directly related to the device capacitances, which is linearly linked to the sizing of the transistors. Therefore a trade-off between conduction and switching loss exists. The product of on-resistance and off-state capacitance $R_{\mathrm{DS,ON}}C_{\mathrm{OFF}}$ at a nominal operation voltage is a figure-of-merit which describes the expected performance of a power semiconductor technology in power

converters [8]. Silicon-based MOSFETs have been optimized over 40 years, and Si superjunction MOSFETs [9] are used today in many power electronics applications in the 200 V to 600 V operation voltage range due to the good trade-off between performance and cost.

1.2 State of the Art

Wide bandgap (WBG) semiconductor materials for power transistors are an alternative to silicon-based devices [10]. There are are many materials which have better figure-of-merits [11] for power devices than silicon [12], resulting from the better physical properties which influence for example the on-resistance, off-state capacitance and blocking-voltage [13] capability. Examples are silicon-carbide (SiC), gallium-nitride (GaN) and diamond [14]. Even though power transistors based on these non-silicon materials with better device performance have been demonstrated, they also require a more sophisticated and expensive [15] fabrication process if the wide bandgap material is used as a bulk substrate for device fabrication. Instead of transistors based on a single semiconductor material, lateral high-electron-mobility transistors (HEMTs) based on a two-dimensional electron gas (2DEG) at the hetero-junction between two different semiconductors [16] are also suitable to create a power transistor. The compound semiconductor material GaN and the aluminum nitride based alloy AlGaN has been used first around 15 years ago in aluminum gallium nitride/gallium nitride (AlGaN/GaN) HEMTs [17] for high frequency applications [18]. Several years later then enhancement mode (e-mode, normally-off) GaN HEMTs were developed [19, 20]. Starting with low-voltage devices, then also 600 V-class devices were realized [21], which enabled usage of GaN HEMTs also for grid-tied power electronics applications. The superjunction concept known from Si MOSFETs was also applied to GaN power transistors to improve the trade-off between area-specific on-resistance and blocking voltage [22]. The lateral AlGaN/GaN HEMTs can be processed not only on GaN as a native substrate, but also on foreign and engineered substrates such as SiC, sapphire, diamond, silicon and silicon-on-insulator (SOI) [23]. The fabrication of AlGaN/GaN HEMTs on silicon substrate (GaN-on-Si HEMT) is especially interesting for power electronics: The wide bandgap device performance is combined with the low cost and scalability of standard large-scale silicon wafer processes. The ability to fabricate high performance GaN HEMTs on Si substrate was a breakthrough for power electronics, and cost parity with comparable Si-MOSFET based solutions was already achieved as claimed by the company Efficient Power Conversion (EPC) in 2015 [24].

Initially, the improved device performance compared to silicon devices was utilized by a 1:1 replacement of Si-based power transistors with their GaN-on-Si counterparts, and discrete GaN-on-Si power transistors were then commercialized. However, another significant feature of the lateral device structure was yet to be exploited: The lateral nature of the HEMT structure allows also the monolithic integration of complete power stages and additional control, sensing and auxiliary circuitry into a single chip.

Early works on monolithic integration in the GaN-of-Si technology already integrated the main building blocks of power converters [25] such as mixed-signal circuits [26, 27], gate drivers [28], sensors [29, 30, 31], high-voltage boost converters [32], half-bridges [33], H-bridges [34] or three-phase motor inverters [35] into a single chip. GaN-based

closed-loop control and converters in a single GaN IC with low-side transistors were already demonstrated [36, 37, 38]. Due to the lateral layout the design and fabrication does not require any additional steps compared to fabrication of a discrete transistor. An improvement of efficiency and power density of power converters based on *discrete* GaN HEMTs compared to Si-based solutions was experimentally demonstrated already a decade ago. Also below 100 V-class low-voltage GaN half-bridges showed better performance than two-chip solutions. The 30 V monolithic GaN half-bridge EPC2100 was commercialized in 2015. EPC also patented a back surface isolation [39] to increase the isolation in monolithic GaN ICs. A monolithic GaN-on-SiC half-bridge with drivers was operated at a very high switching frequency of 100 MHz at a low voltage of 20 V [40] in 2016. However, early attempts to operate *monolithic* high-voltage 600 V-class power topologies on a Si-substrate initially showed even worse performance and limited operation voltages compared to a circuit using discrete GaN devices. For example, the monolithic three-phase GaN inverter IC from Panasonic published in 2009 was fabricated in a high-voltage technology with over 700 V blocking capability. However, operation was demonstrated only at 100 V [35]. The high-voltage operation of monolithic power topologies is degraded by static and dynamic substrate biasing effects. The first high-voltage operation of a monolithic GaN half-bridge [41] was then demonstrated in 2017 by B. Weiss [42], and was enabled by a novel substrate biasing technique. The substrate biasing method proposed by B. Weiss did not completely avoid the substrate biasing effects, but allowed to control them and adjust the effect to a usable and predictable region. Still today in 2020 substrate biasing effects in high-voltage GaN-on-Si half-bridge operation are part of ongoing research [43]. Commercially, several companies promoted "monolithic half-bridges" very early [44] in a GaN-on-Si technology but did so far not demonstrate device operation. Instead, later it was confirmed that only a system-in-package half-bridge with two discrete half-bridge devices was actually commercialized. Today still only 100 V-rated monolithic GaN-on-Si half-bridges are commercially available (EPC2104). Even though no higher voltage GaN-on-Si half-bridges are commercially available, other technological more complex solutions were pursued, for example a 650 V GaN-on-SOI foundry process is available (IMEC, Europractice).

In addition to the monolithic integration, advanced packaging approaches have shown benefits in combination with GaN circuits: Embedding of GaN ICs in printed circuit boards (PCBs) not only avoids bond wires and parasitic inductance [45], but also allows to interface GaN power ICs with many high-current terminals on a small chip area, such as a multilevel inverter [46].

1.3 Problem

The root cause of degraded performance of monolithic high-voltage power stages on Si-substrate was investigated over years, and is well understood today. A close inspection of the device structure of monolithic circuits also explains the observed effects: The conductive Si substrate is separated from the channel of a HEMT device only by several micrometers, such that the conductive substrate (or backside/bulk) of the device forms a second gate (back-gate). While the substrate is conventionally tied to source for discrete power devices, which avoids static and dynamic influences from the substrate potential,

in monolithic power circuits all integrated devices share the same common conductive Si substrate potential [42]. Especially in circuits which have low-side and high-side devices such as a high-voltage half-bridge, it is not possible any more to permanently terminate the substrate to each source of all integrated deices. Application-oriented substrate biasing effects in discrete and monolithic GaN half-bridges were also investigated by the author of this work in [47, 48, 49, 50]. Prior works have investigated these substrate biasing effects and proposed solutions to push the operation voltage of monolithic GaN power circuits towards higher values.

In particular, the GaN buffer type is relevant for static and dynamic biasing effects. Both dynamic trap-related [51, 52, 53] effects and static back-gating [54, 55] by negative substrate-to-source voltages can result in a severe on-resistance increase. Prior works have shown that improvement of the GaN buffer structure and quality allows to reduce dynamic trap-related biasing effects, which influences the switching behavior of GaN ICs. For example, a thick superlattice buffer was used [56] as alternative to graded GaN buffers and enabled a reduction of biasing effects [57, 58]. On the other hand, substrate biasing-networks were used [59, 60] to externally control and shift the substrate potential towards more positive values, which reduces or avoids static back-gating effects. Successful combination of both solutions is a precondition for the fault-free operation of monolithic power circuits.

However, even if appropriate technological solutions are implemented to avoid dynamic and static substrate related on-resistance increase, there still remain application-oriented substrate-related effects.

For experimental investigations, this work uses a monolithic GaN-on-Si power IC as shown in Fig. 1.1 (published by the author in [61]). The GaN chip monolithically integrates a half-bridge with intrinsic freewheeling diodes, two gate driver final stages, current, voltage and temperature sensors. The shown IC is already fully monolithically integrated. To compare the results and analysis to conventional discrete half-bridge circuits, the two half-bridge sides of the IC were diced as needed, which allows to also assemble discrete half-bridge modules. (published by the author in [62, 63]. The design is already the second generation and based on an early work of the author published in 2015 [64], which was one of the first demonstrations of fast-switching GaN HEMTs with monolithic integrated drivers. Fig. 1.2 schematically shows a cross-section through a half-bridge on a common Si-substrate, where the high-side and low-side substrate-to-source voltages $V_{\mathrm{BS,HS}}$ and $V_{\mathrm{BS,LS}}$ are coupled and linked to the dc-voltage V_{DC}. The half-bridge is enhanced by a gate driver, and then used as fundamental building block for dc-dc converter demonstrators.

1.4 Scope of the Work

This work comprehensively investigates capacitive and inductive substrate-related effects which result from coupling of lateral GaN HEMTs through the conductive Si-substrate in GaN-based power circuits with multiple integrated devices such as a half-bridge or transistors with gate drivers.

In particular, the work addresses the following aspects:

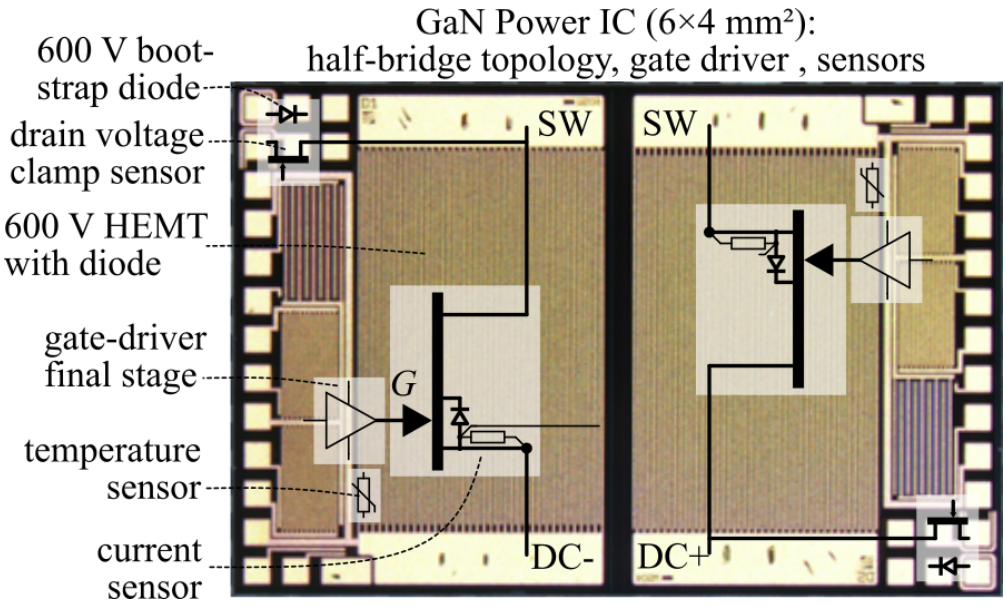

Figure 1.1: Monolithic GaN-on-Si half-bridge with gate drivers and further circuitry. [61]

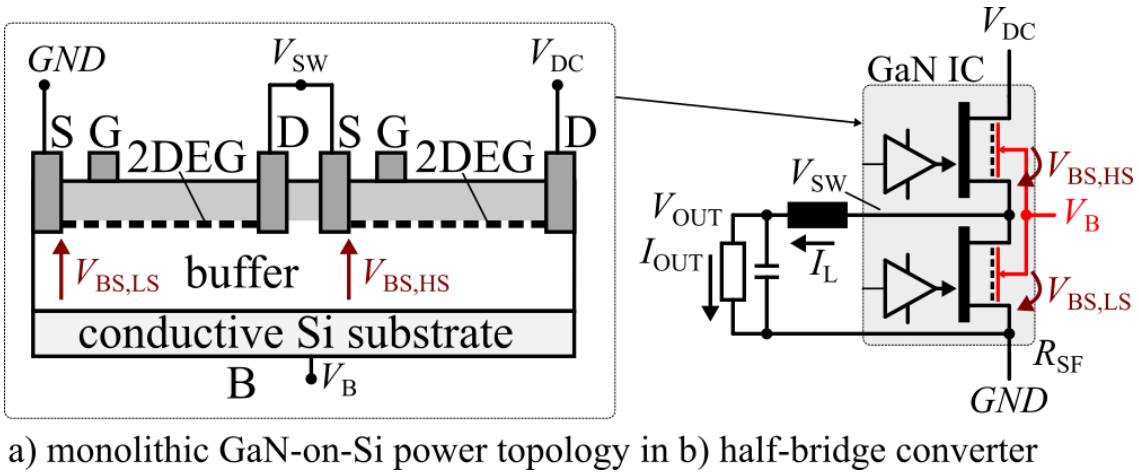

Figure 1.2: Cross-section of half-bridge on common conductive Si-substrate. The half-bridge is a fundamental building block of dc-dc converters. [61]

1. The lateral device geometry forms **substrate capacitances** from the integrated device terminals and channels to the conductive Si-substrate. In half-bridges and driver circuits on a common conductive Si-substrate, this capacitive coupling results in effective application-oriented device capacitances which differ from discrete GaN HEMTs with a substrate-to-source termination. The effect of capacitive substrate coupling in half-bridges on switching performance is investigated by this work. An improved substrate biasing scheme for the operation of monolithic half-bridges is proposed which avoids **static back-gating**. A dc-dc converter is experimentally operated and characterized to demonstrate the beneficial combination of reduced effective capacitances and back-gating avoidance, which results in an increased converter efficiency compared to conventional half-bridges.

2. Even if the monolithic integration of power circuits with drivers apparently allows to reduce **parasitic interconnect inductance**, still external interconnects to

dc supply capacitors are required. Effects on switching performance are investigated, resulting from the external interconnection between the dc-link capacitor and an integrated half-bridge, and between the gate supply capacitors and an integrated gate driver. A combination of monolithic power circuit integration and printed-circuit-board embedding technology with on-package bypass capacitors is realized this work, which reduces the parasitic inductance on both the chip-level and package-level.

3. Furthermore, also substrate effects for discrete GaN HEMTs exist and are investigated: If the substrate is terminated to source by means of an external bond-wire or other interconnects outside the chip, then this external interconnection forms another parasitic loop. This **parasitic substrate-loop** as third critical loop (in addition to the power-loop and gate-loop) is exposed by this work and effects on the stability and switching performance investigated. Instabilities from the substrate-to-source termination are theoretically analyzed and experimentally verified, as well as damping methods proposed to achieve stability without slowing down the switching transitions.

1.5 Research Questions

The work structures the research questions and investigation on switching particularities of integrated GaN half-bridges and drivers on Si substrate into three aspects, which are then also addressed in three main chapters.

Substrate capacitance related questions:

- How do the substrate capacitances, the substrate potential and different substrate terminations influence the effective capacitances of GaN-on-Si HEMTs and half-bridges?

- How to avoid static back-gating during operation of GaN half-bridges on a common Si substrate?

- How does the substrate termination influence the switching behavior and performance of GaN-on-Si half-bridges and drivers?

Gate-loop and power-loop related questions:

- How does parasitically increased inductance in the gate-loop or power-loop influence switching speed and overshoot?

- How much do monolithic integration and advanced packaging of GaN power circuits allow a reduction of parasitic inductances?

Substrate inductance related questions:

- How does the substrate termination as a third critical loop affect switching behavior and stability?
- How to reduce the substrate-loop inductance and avoid related instabilities?

1.6 Structure of the Thesis

Chapter 1 motivated the work and stated the research questions.

Chapter 2 describes the silicon substrate of lateral HEMTs in discrete half-bridges as two additional circuit terminals, and the common silicon substrate in a monolithic half-bridge as one additional circuit terminal. The substrate capacitances are systematically analyzed, and for multiple feasible substrate terminations an equivalent circuit transformation is carried out. A formulation of the effective half-bridge capacitances is the result of the analysis and allows a direct comparison of discrete and monolithic half-bridge for different substrate terminations. A duty-cycle independent substrate biasing network for the operation of monolithic GaN-on-Si half-bridges without back-gating under all operation points is proposed. Using this operation principle, operation of a monolithic GaN-on-Si half-bridge with drivers is verified, and dc-dc conversion efficiencies higher than a discrete half-bridge are presented.

Chapter 3 analyzes how parasitic interconnect inductance in the gate-loop and power-loop limits the switching speed and causes voltage overshoot. A switching transient analysis which takes a limited voltage slew-rate switching speed into account is carried out. It is derived, that despite the presence of parasitic inductance, local minima of voltage overshoot exist and are controllable by slight adjustment of the switching speed. In addition to the overshoot reduction by reduction of the switching speed, a PCB-embedded packaging technique is also shown to further reduce parasitic inductance as the root cause for overshoot and oscillations.

Chapter 4 shows that under certain conditions the half-bridge with gate driver is an unstable feedback amplifier, such that severe oscillations at fast switching speed will not decay over time, but instead cause an instability which ultimately leads to device destruction. While instabilities caused by direct feedback from the drain to the gate is well known, this work exposes that also a substrate-to-source termination forms a third parasitic loop, the substrate-loop. Analytically and experimentally the instability from the substrate-loop is investigated. Countermeasures such as resistive damping of the substrate-loop or reduction of the parasitic substrate-loop inductance are discussed and verified.

Chapter 5 summarizes the findings, contributions and conclusions of this work.

2 Substrate-Related Switching Characteristics of GaN-on-Si Half-Bridges

2.1 Problem and Approach

Fig. 2.1a shows a simplified cross section of a typical vertical three-terminal power transistor. Since the bulk substrate in vertical devices is used as part of the device, the substrate terminal is one of the transistor terminals. For example for vertical n-channel transistors, the bottom-side of the device thus is the drain terminal, and only three relevant terminal capacitances are formed: The gate-to-source C_{GS}, gate-to-drain C_{GD} and drain-to-source terminal capacitance C_{DS}. A more application-oriented representation of this terminal capacitances is possible by combining the terminal capacitances into the effective input capacitance $C_{ISS} = C_{GS} + C_{GD}$, output capacitance $C_{OSS} = C_{DS} + C_{GD}$ and reverse (feedback) capacitance $C_{RSS} = C_{GD}$.

Fig. 2.1b shows a cross section of a lateral GaN-on-Si HEMT as a four-terminal power transistor with the main transistor terminals (gate G, drain D, source S) on the top-side of the device. The active device channel and top-side electrodes are separated by an isolating buffer layer from the bottom-side of the device, where a conductive (silicon) carrier (substrate B) acts as another, fourth terminal. In this structure, the substrate is an additional electrical terminal and the additional substrate capacitances C_{BS}, C_{BG}, C_{BD} result in a total of six relevant terminal capacitances of a single lateral GaN-on-Si HEMT.

Fig. 2.1c shows a monolithic integrated half-bridge, consisting of two series-connected GaN HEMTs on a common conductive Si substrate. This configuration causes further cross-coupling between the two half-bridge transistors since both transistors now share a common substrate. For this common substrate there exist now many possible substrate terminations (including floating terminations), and it is questioned how the substrate termination and capacitances influence the switching characteristics. The substrate-to-source voltage in a monolithic half-bridge (Fig. 2.1c) also differs from discrete half-bridges and is influenced by capacitive coupling from the switch-node to the substrate-node. To avoid static on-resistance degradation, negative back-gating of both half-bridge transistors is required. How to adjust the substrate voltages to avoid back-gating during operation is a question investigated in this work.

Since there are many possible electrical terminations of the substrate, for example a separate short connection of the substrate to source (substrate-to-source termination B=S) for discrete half-bridges, or a floating termination of the substrate for a monolithic half-bridge, the following questions arise:

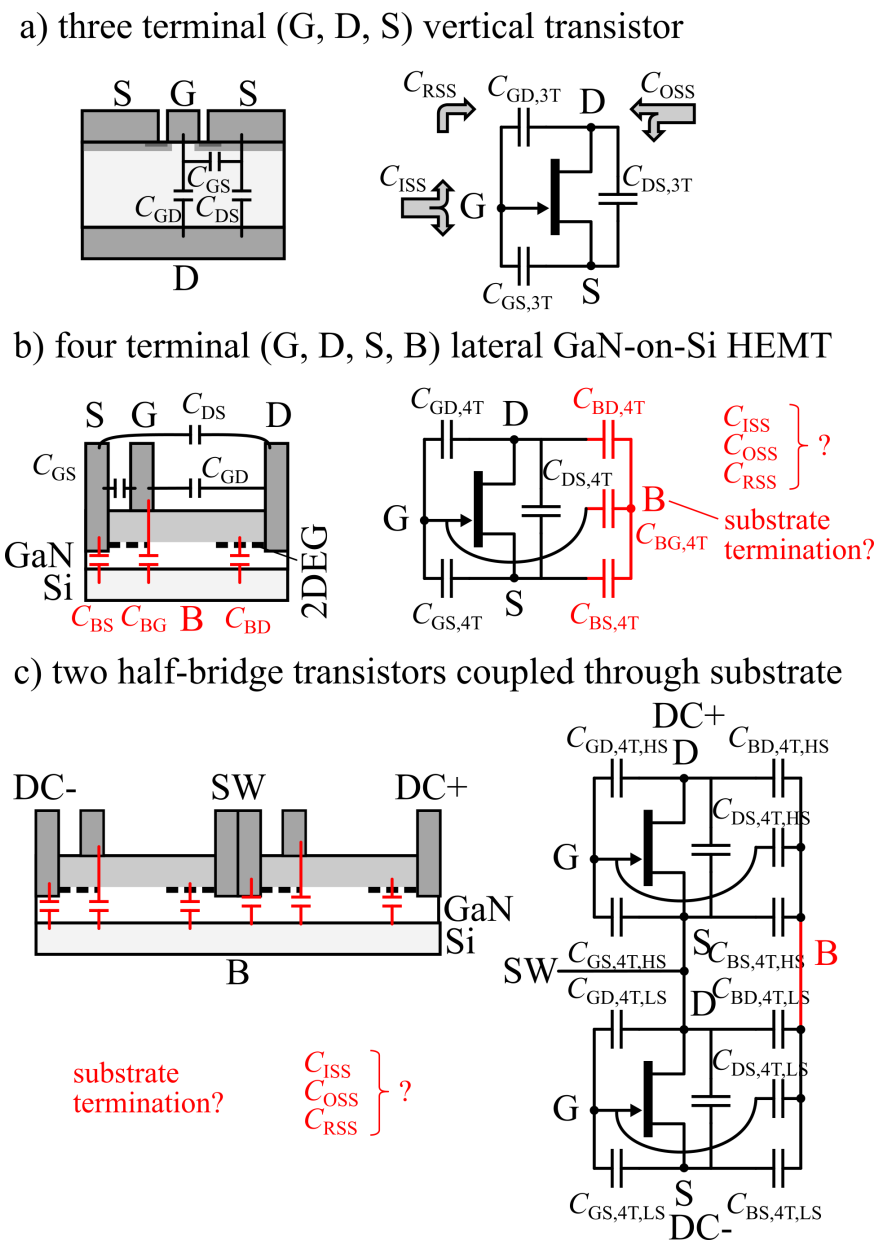

Figure 2.1: Cross-section of (a) vertical transistor as three-terminal (gate, drain, source) transistor with three terminal capacitances and (b) a lateral transistor as four-terminal transistor (gate, drain, source, substrate) with an isolating buffer layer between the transistor channel and a conductive substrate. (c) Lateral monolithic half-bridge on a single coupled conductive substrate.

Research questions:

- How do the substrate capacitances, the substrate potential and different substrate terminations influence the effective capacitances of GaN-on-Si HEMTs and half-bridges?

- How to avoid static back-gating during operation of GaN half-bridges on a common Si substrate?

- How does the substrate termination influence the switching behavior and performance of GaN-on-Si half-bridges and drivers?

Approach: This chapter analyzes the effect of the terminal-capacitances (Sec. 2.2) in combination with different substrate terminations for single transistors as well as in half-bridge configuration on the switching behavior. First, operation voltage limitations from vertical substrate leakage currents and negative substrate back-gating are discussed (Sec. 2.3). Then, the substrate voltage is calculated as a function of the switch-node voltage in half-bridges for a variety of substrate terminations, including monolithic half-bridges (Sec. 2.5). A novel duty-cycle independent substrate biasing network for monolithic half-bridges is proposed (Sec. 2.5), which avoids negative back-gating. The analysis then aims to transform the multi-terminal capacitances $C_{GS}, C_{GD}, C_{DS}, C_{BS}, C_{BG}, C_{BD}$ of up to two coupled half-bridge transistors into equivalent three-terminal capacitances $C_{GS,3T}, C_{GD,3T}, C_{DS,3T}$ (Sec. 2.6). The result of the analysis allows calculation of the more application-oriented effective capacitances $C_{ISS}, C_{OSS}, C_{RSS}$ (Sec. 2.7), and thereby a direct quantitative comparison of discrete and monolithic half-bridges with different substrate terminations. The effect of different substrate terminations on switching behavior is then experimentally and systematically quantified to verify the theory. (Sec. 2.8). Based on the results of the theoretical and experimental study on different substrate terminations, then in Sec. 2.9, finally, a monolithic half-bridge with drivers is operated with high efficiency.

2.2 Capacitances of Individual Transistors

2.2.1 Terminal Capacitances of Three- and Four-Terminal HEMTs

Fig. 2.2a shows measured three-terminal (3T) capacitances $C_{GS,3T}, C_{GD,3T}, C_{DS,3T}$ as a function of drain-source voltage V_{DS} in off-state $V_{GS} = V_{DRV,NEG}$. The data is normalized to 1 mm gate-width, and the devices measured and measurement method further described in Appendix A.3. This typical capacitance data in off-state, which is also provided in commercial devices' data sheets, is only a function of V_{DS}. It should be noted that if no substrate termination is explicitly mentioned, a conventional substrate-to-source (B=S) termination is assumed, which reduced the four-terminal transistor to a three-terminal device.

Fig. 2.2b shows the six measured four-terminal (4T) capacitances $C_{GS,4T}, C_{GD,4T}$, $C_{DS,4T}$, $C_{BS,4T}$, $C_{BG,4T}$, $C_{BD,4T}$ of the same device under test as a function of drain-source voltage V_{DS} in off-state $V_{GS} = V_{DRV,NEG}$ and a constant (conventional) substrate-to-source voltage $V_{BS} = 0\,V$. For the shown data for a conventional substrate-to-source substrate termination in Fig. 2.2a, it is already qualitatively observed that the three-terminal gate-to-source capacitance $C_{GS,3T}$ is the sum of the four-terminal gate-to-source and substrate-to-gate capacitances $C_{GS,4T} + C_{BG,4T}$. Likewise, the three-terminal drain-to-source capacitance $C_{DS,3T}$is the sum of the four-terminal drain-to-source and

substrate-to-drain capacitances $C_{DS,4T} + C_{BD,4T}$. The three-terminal gate-to-drain capacitance $C_{GD,3T}$ is equal to the four-terminal gate-to-drain capacitance $C_{GD,4T}$. In the following, this kind of relation between the three- and four-terminal capacitances is systematically analyzed in more detail for different substrate terminations.

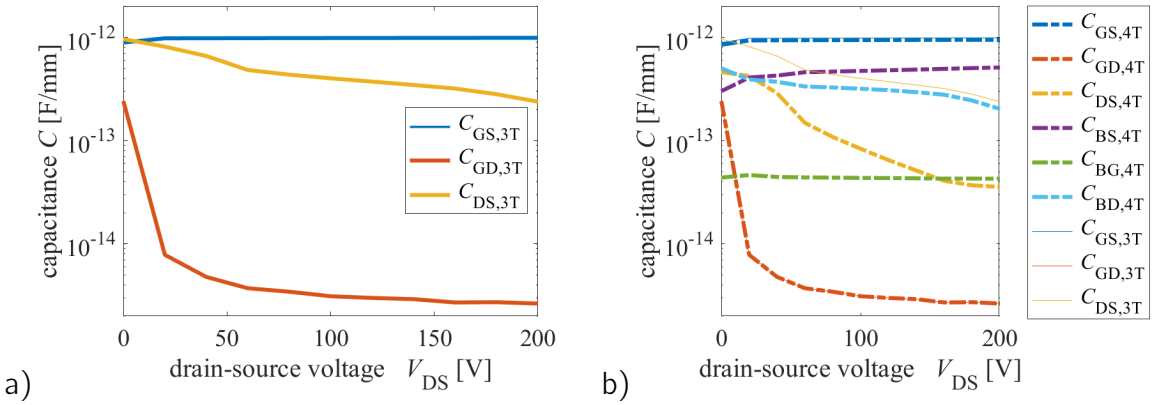

Figure 2.2: a) Measured three-terminal transistor capacitances (B=S termination with $V_{BS} = 0\,V$). b) Measured four-terminal transistor capacitances, including the substrate B as fourth terminal.

2.2.2 Effective Capacitances

While the three- and four-terminal capacitances directly describe the internal device structure, for switched-mode power converter applications it is more useful to describe the effective device capacitances which the external circuits (gate driver, power inductor connected to the switch-node in a half-bridge, dc-link capacitance in a half-bridge) "see" during switching operation. For this purpose the input, output and reverse capacitances $C_{ISS}, C_{OSS}, C_{RSS}$ are typically used instead of the terminal-capacitances. These more application-oriented capacitances are defined for three-terminal transistors as

$$C_{ISS} = C_{GS,3T} + C_{GD,3T} \tag{2.1}$$
$$C_{OSS} = C_{DS,3T} + C_{GD,3T} \tag{2.2}$$
$$C_{RSS} = C_{GD,3T}. \tag{2.3}$$

The three effective capacitances are well-defined for a three-terminal transistor. Fig. 2.3 shows the calculated effective capacitances based on the three-terminal data from Fig. 2.2a.

An intuitive description of the effective capacitances for switched-mode converter operations is:

C_{ISS}: The input capacitance C_{ISS} has to be charged and discharged by the gate driver to cause a switching transition. C_{ISS} is mainly relevant prior to and after the dV/dt phase of a voltage switching-transition.

C_{RSS}: During the dV/dt phase, the reverse capacitance C_{RSS} is effective (also known as "Miller-effect"). Since C_{RSS} as a feedback capacitance between the drain and gate

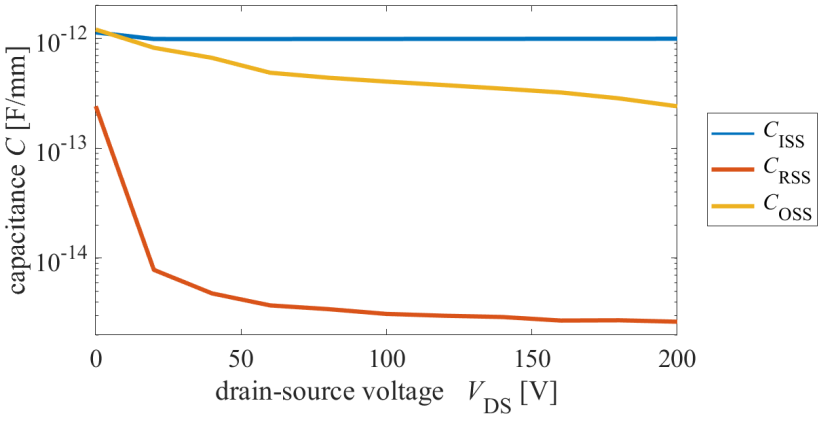

Figure 2.3: Effective input, output and reverse capacitances for a substrate-to-source termination.

has to be charged by the driver during hard-switching dV/dt voltage transitions, the gate charging current and magnitude of C_{RSS} limits the switching time during the dV/dt phase.

C_{OSS}**:** The output capacitance C_{OSS} has to be charged and discharged during each switching cycle. For hard-switching transitions it is related to switching energy losses and for resonant switching transitions related to the switching time.

For the four-terminal transistor and coupled half-bridge transistors however, the substrate termination additionally influences the effective capacitances. In order to allow a comparison of the effective capacitances also for four-terminal transistors and different substrate terminations, this work's approach is to transform the four-terminal capacitances $C_{GS,4T}$, $C_{GD,4T}$, $C_{DS,4T}$, $C_{BS,4T}$, $C_{BG,4T}$, $C_{BD,4T}$ for each investigated substrate termination to equivalent three-terminal capacitances $C_{GS,3T}$, $C_{GD,3T}$, $C_{DS,3T}$. This transformation then allows calculation of the effective capacitances according to Eqn. 2.1-2.3 and thereby a direct comparison between conventional three-terminal transistors and discrete or monolithic half-bridges based on four-terminal transistors for all substrate terminations.

In half-bridge circuits with two transistors, in addition to the effective capacitances $C_{ISS,LS}$, $C_{RSS,LS}$, $C_{OSS,LS}$ and $C_{ISS,HS}$, $C_{RSS,HS}$, $C_{OSS,HS}$ of both half-bridge transistors, a useful quantity is the overall switch-node capacitance C_{SW} for a constant dc-link voltage V_{DC}:

$$C_{SW}(V_{SW})|_{V_{DC}=\text{const}} = C_{OSS,LS}(V_{DS,LS} = V_{SW}) + C_{OSS,HS}(V_{DS,HS} = V_{DC} - V_{SW}) \quad (2.4)$$

where the switch-node voltage V_{SW} is equal to the low-side drain-source voltage $V_{DS,LS} = V_{SW}$ and related to the high-side drain-source voltage by $V_{DS,HS} = V_{DC} - V_{SW}$.

2.2.3 Non-linear Multi-Bias Capacitances

The terminal capacitances of a GaN-on-Si HEMT are non-linearly depended on V_{DS}, V_{BS} and V_{GS}. Only the off-state $V_{GS} = V_{DRV,NEG}$ is considered in this work and thus only the dependence on V_{DS} and V_{BS}.

The analysis in this chapter will be applied to high-voltage large-area GaN-on-Si HEMTs and half-bridge circuits. Therefore, exemplary calculations will be carried out. All calculations in this chapter are based on the same measurements of the four-terminal capacitances of a representative GaN-on-Si HEMT, as explained in Appendix A.3. The terminal capacitances are measured on-wafer with a LCR-meter, four bias-tees and a switch-matrix at a measurement frequency of 1 MHz. While this work uses a LCR-meter, which simplifies the calibration for measurement of vertical capacitances on a wafer prober, alternatively an network analyzer can be used. A network analyzer based measurement method for four terminal capacitances of GaN HEMTs is presented in [65] by C. Salcines, co-authored by the author of this thesis. An extended approach for measurement of on-state capacitances is also shown by C. Salcines in [66]. This work however is based only on off-state capacitances. The complete set of measurement data is shown in Appendix A.3 in two ways: One with V_{DS} on the x-axes and V_{BS} as parameter, and a second with V_{BS} on the x-axes and V_{DS} as a parameter.

Here, only two measured terminal capacitances are exemplarily shown: Fig. 2.4 shows the measured four-terminal drain-source and substrate-to-drain capacitances $C_{DS,4T}$ and $C_{BD,4T}$ as functions of V_{DS} as well as V_{BS}.

All terminal and effective capacitances in this chapter (C_{GS}, C_{GD}, ..., C_{ISS}, C_{OSS}, ..., C_{SW}, ...) are drain and substrate bias-dependent $C_{XY} = C_{XY}(V_{DS}, V_{BS})$, but for clarity of the equations the dependency is not always written in full.

2.2.4 Condensed Capacitances-Related Quantities at Nominal Operation Voltage

Even though the device capacitances are bias-dependent, for quantitative comparison of transistors and half-bridges it is beneficial to condense the bias-dependent capacitance data into single averaged values. For fixed operation voltages V_{DC} it is possible to condense the capacitance data into application-relevant quantities using various definitions.

Since $C_{XY} = C_{XY}(V_{DS}, V_{BS})$ is multi-bias dependent, but the condensed capacitance definitions only consider a V_{DS} dependency, this work's approach is to calculate equivalent three-terminal capacitances for each considered substrate termination. For this, in the following first the (floating) substrate voltage is calculated as an explicit function of the drain-source (or switch-node) voltage $V_{BS} = V_{BS}(V_{DS})$ for each substrate termination, such that $C_{XY} = C_{XY}(V_{DS}, V_{BS})$ simplifies to $C_{XY} = C_{XY}(V_{DS}, V_{BS}(V_{DS})) = C_{XY,SUB}(V_{DS})$, which enables a calculation of condensed capacitance data for each substrate termination.

For example, for a given operation voltage V_{DC} the bias-dependent three-terminal output capacitance $C_{OSS}(V_{DS})$ is condensed into the effective energy-related output capacitance

$$C_{OSS,ER} = \frac{2}{V_{DC}^2} \int_{0\,V}^{V_{DC}} C_{OSS}(V_{DS}) V_{DS}\, dV_{DS} \tag{2.5}$$

or the time-related output capacitance

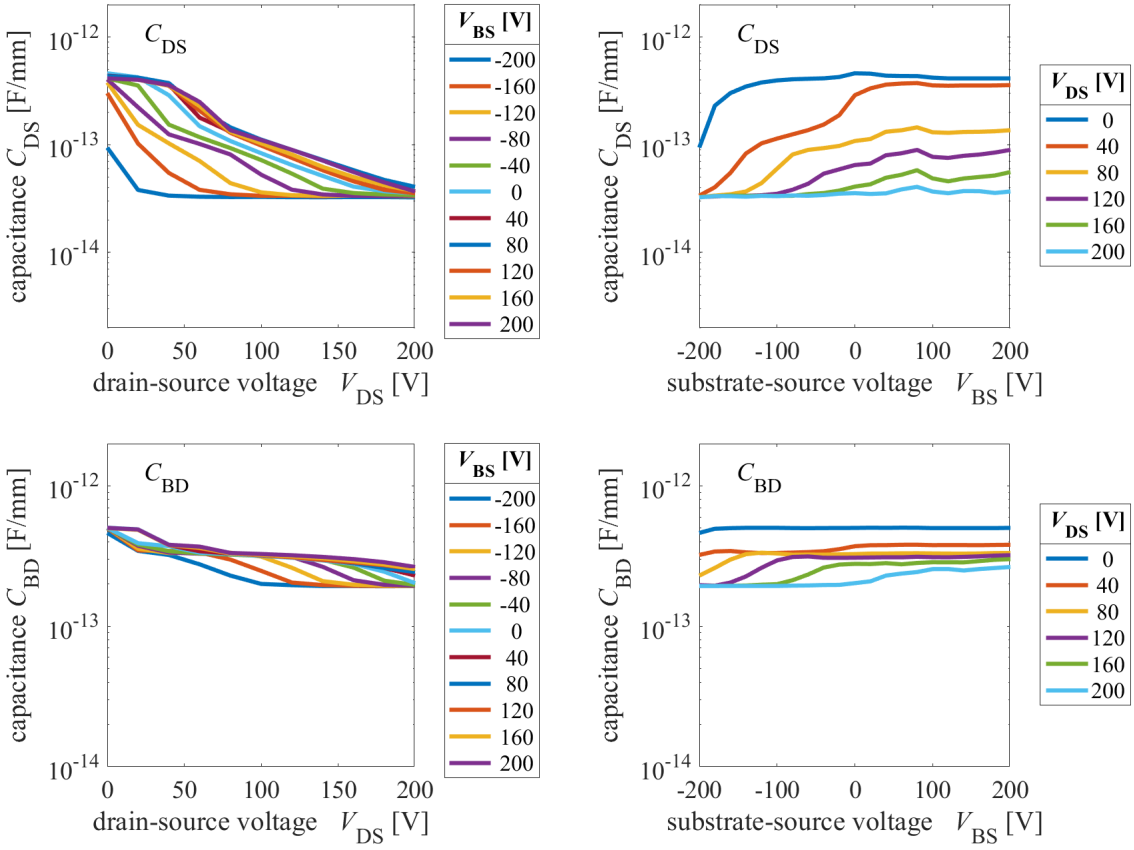

Figure 2.4: Measured four-terminal capacitances C_{DS} (top) and C_{BS} (bottom) of a lateral GaN-on-Si HEMT as a function of drain-to-source voltage V_{DS} (left) or substrate-to-source voltage V_{BS}. All six terminal-capacitances are shown in Appendix A.3.

$$C_{OSS,TR} = \frac{1}{V_{DC}} \int_{0\,V}^{V_{DC}} C_{OSS}(V_{DS}) dV_{DS}. \tag{2.6}$$

Similarly, the output capacitance charge $Q_{OSS}(V_{DS})$ is condensed into the effective output capacitance charge for a nominal operation voltage V_{DC} as

$$Q_{OSS} = \int_{0\,V}^{V_{DC}} C_{OSS}(V_{DS}) dV_{DS}. \tag{2.7}$$

The energy difference in the output capacitance [67] of a single transistor is

$$E_{OSS} = \int_{0\,V}^{V_{DC}} C_{OSS}(V_{DS}) V_{DS} dV_{DS} \tag{2.8}$$

and the energy dissipated [67], which results from one half-bridge transistor when switching the other half-bridge transistor is

$$E_{QOSS} = \int_{0\,V}^{V_{DC}} C_{OSS}(V_{DS})(V_{DC} - V_{DS}) dV_{DS}. \tag{2.9}$$

In a hard-switching voltage transition in a half-bridge, at least the sum $E_{OSS} + E_{QOSS}$ is dissipated as switching loss in one switching cycle [67]. In this work hard-switching denotes a switching transition where the stored energy in the output capacitances of the transistors is dissipated in one of the half-bridge transistors during a voltage switching transition. In addition to the stored energy from the output capacitances, additional energy is dissipated due to overlap of voltage and current during the switching transition [68]. This is in contrast to soft-switching, which in this work denotes a voltage transition which is caused by an external charging current, for example the inductor current, and where the stored energy in the output capacitances of the transistors is not dissipated in the half-bridge transistors. In soft-switching applications the switching loss can be avoided if the dielectric material of the output capacitance in the transistor is considered loss-less (low dissipation factor) [69, 70].

In a half-bridge with two identical transistors, the effective switch-node capacitance is averaged for a nominal operation voltage as

$$C_{SW} = \frac{1}{V_{DC}} \int_{0\,V}^{V_{DC}} [C_{OSS}(V_{DS}) + C_{OSS}(V_{DC} - V_{DS})] dV_{DS}. \tag{2.10}$$

2.3 Limited Operation Voltage from Substrate Biasing

This section discusses how the operation voltage of monolithic GaN-on-Si ICs is limited compared to single GaN-on-Si power HEMTs with a substrate-to-source termination. In the off-state of the transistor, the device structure has to withstand high voltages. In the off-state, the drain-source voltage is positive $V_{DS} > 0$. In the on-state, the drain-source voltage might become negative in the third quadrant by reverse conduction of the HEMT, or by conduction of an intrinsic or external freewheeling diode. In this section, this low voltage drop in reverse is neglected for discussion of the voltage blocking capability. In a discrete GaN HEMT with B=S termination ($V_{BS} = 0$), the substrate-to-source voltage is the inverse value of the drain-source voltage $V_{BS} = -V_{DS}$. For example, a 600 V-class device, the vertical layer stack of the GaN HEMT has to withstand also at least -600 V. The substrate thus has to withstand negative bias voltages (with respect to the top-side potentials). Due to the low on-state voltage (possible in third quadrant), the required positive substrate voltage blocking capability for single HEMTs vanishes. This means, that for discrete HEMTs a vertical buffer structure with a unipolar (asymmetric) voltage blocking capability is sufficient.

Fig. 2.5 shows measured and typical vertical buffer leakage currents for two different epitaxies (step-graded buffer and superlattice buffer). Both buffer types are compared in [57, 61, 71] and withstand more than -600 V negative substrate voltages with low vertical leakage. Both buffer types are thus applicable to operate 600 V-class single GaN HEMTs with B=S termination. However, if monolithic power topologies are fabricated in the same technology, and operated with alternative substrate bias voltages, then also a positive substrate blocking is required. In this chapter it will be further discussed that the efficient operation of monolithic half-bridges also requires positive substrate blocking capability. Since the GaN epitaxy used in this work was initially optimized for single devices, they show low leakage currents at negative substrate biasing voltage, but excessively increased leakage at positive substrate biasing. The origin of the asymmetry

in the vertical leakage current is explained for example in [72] by the asymmetrical layer stack from the 2-dimensional electron gas through the GaN buffer and to the conductive (highly p-doped) Si-substrate: At negative substrate voltages the 2DEG is depleted, and electrons generated in the Si substrate have to overcome a high energy barrier. In contrast, at a positive substrate voltage, electrons in the enhanced 2DEG or below the ohmic contacts are more easily injected into the buffer [73]. Fig. 2.5 shows that the graded buffer has only a +230 V positive substrate voltage blocking capability, compared to the -600 V negative blocking capability at equal absolute leakage currents. This severe asymmetry in the vertical leakage is significantly improved by the superlattice epitaxy [74], which shows a +620 V positive blocking capability, compared to -860 V negative blocking capability at equal absolute leakage currents. Low vertical leakage is a necessary condition for monolithic high-voltage circuit operation on conductive Si substrate. A worst-case assumption, neglecting any voltage de-rating, is that for monolithic GaN power stage operation (for example half-bridges) at a dc voltage of V_{DC}, the range $V_{BS} = -V_{DC}...+V_{DC}$ of vertical blocking voltage capability is required. Under this assumption, the feasible operation voltage range of a monolithic GaN power circuit with the step-graded buffer is reduced to below 230 V. This is a significant limitation, compared to the 600 V operation voltage which is possible for a single GaN HEMT using the same technology. For the superlattice buffer the vertical leakage is less asymmetrical, and the low vertical leakage promises a feasible operation range of up to 620 V, sufficient for mains-grid applications.

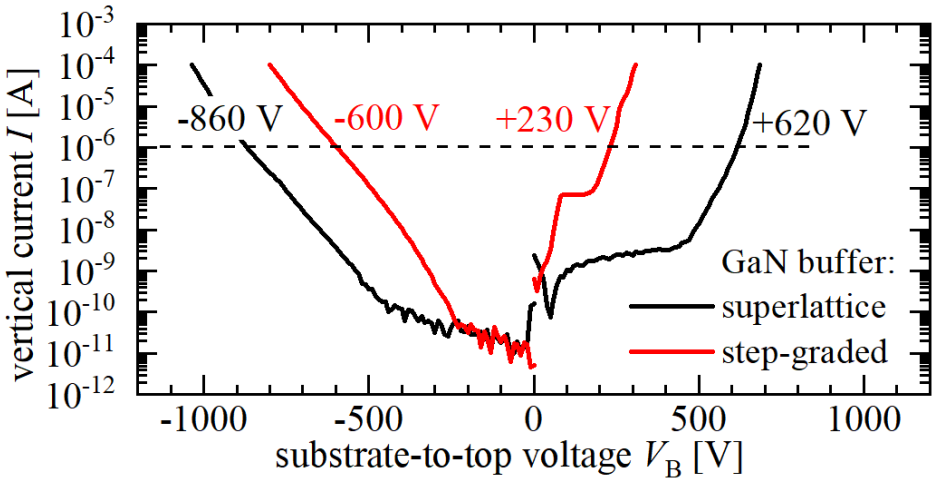

Figure 2.5: Measured vertical substrate leakage for a step-graded and a superlattice GaN buffer shows asymmetries depending in the substrate polarity.

Besides the low vertical leakage, the lateral channel current is also significantly influenced by the substrate bias voltage. Since the conductive substrate forms a second back-gate, depletion of the channel by negative back-gate voltages is expected. With a depleted channel, the on-resistance of the device likewise increases. Negative back-gated operation of the GaN HEMT is thus not desired, compared to a zero substrate bias operation with the full channel current, since the on-resistance will be significantly increased compared to a discrete GaN HEMT operation.

Fig. 2.6 shows measurements of a lateral channel current ($V_{DS} = 1\,V$) of a top-gateless test structure. The substrate voltage is ramped similar to [75] from -500 V to +300 V (graded-buffer, limited by vertical leakage) or +500 V (superlattice) and then back to -

500 V. The resulting measurement is a transfer characteristic, with the substrate as the controlling gate. From this measurement, it is apparent that the back-gate has a negative threshold voltage of around -100 V (graded-buffer) or -500 V (superlattice). At the back-gated threshold voltage the lateral channel current is already fully depleted. Under this negative substrate biasing conditions a lateral current conduction is not possible any more, independent from top-gate gate-source voltages. The ramped substrate voltage measurement also shows a hysteresis. From the worst-case part of the measurement (increasing V_B direction), it is observed that on the step-graded buffer at a very low negative back-gating voltage of around $V_{BS} \approx -40\,V$, the channel current is already halved, and a doubled on-resistance is expected. This measurement shows the dramatic consequences of negative back-gating on conduction behavior. To maintain the superior properties of discrete GaN HEMTs also for monolithic GaN power ICs, negative back-gating has to be avoided. Even though the super-lattice shows a more negative substrate threshold voltage, still at already approximately $V_{BS} = -250\,V$ the lateral channel current is halved. The lateral channel current depletion starts also already at very low negative substrate bias voltages. Thus, also for the superlattice buffer negative back-gating should be avoided to maintain a low on-resistance of the integrated devices.

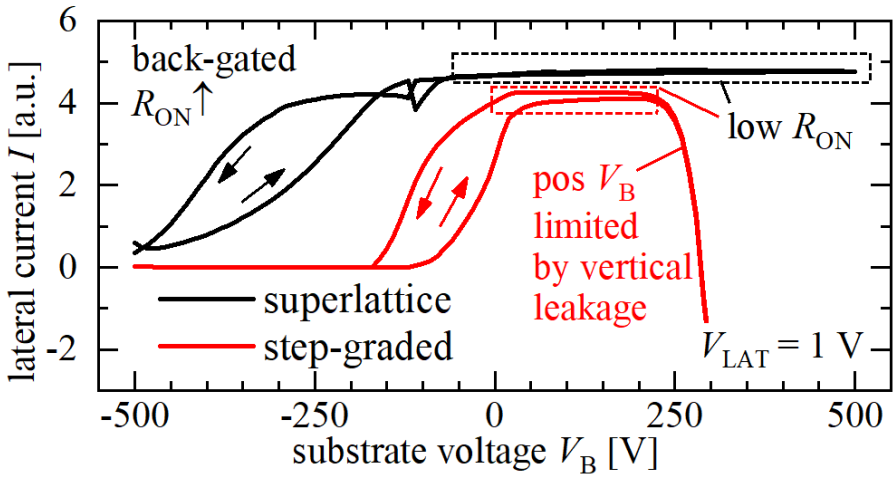

Figure 2.6: Measured lateral channel current reduction from back-gating for up- and down ramped substrate-voltage sweep.

In addition to the effect on the conduction current, the back-gating voltage also causes a threshold voltage shift [76, 77]. For the used superlattice epitaxy in this work however, the threshold voltage shift is published in [61] and below $\pm 1\,V$, which is acceptable low in the considered operation voltage range for reliable circuit operation. The measurement in Fig. 2.6 shows that for positive substrate bias voltages, the lateral channel current is almost constant. The positive substrate potential enhances the channel in comparison to the depletion from negative bias. However, since the two-dimensional electron gas in the channel has a limited saturation current, the current is not significantly increased compared to the case of a zero substrate bias voltage. To maintain a high channel current and low on-resistance of integrated GaN-on-Si ICs, it is concluded that negative substrate bias has to be avoided. However, depending on the buffer type, the possible operation voltage range of the monolithic ICs is then significantly limited by the asymmetric vertical leakage current.

In this chapter, for the sake of a systematic analysis of different substrate configurations, the operation voltage is thus limited to 200 V.

2.4 Analyzed Half-Bridge Substrate Terminations

Fig. 2.7 shows an overview on the investigated substrate terminations for half-bridges. Both half-bridges with separate substrate termination of the high-side and low-side de-

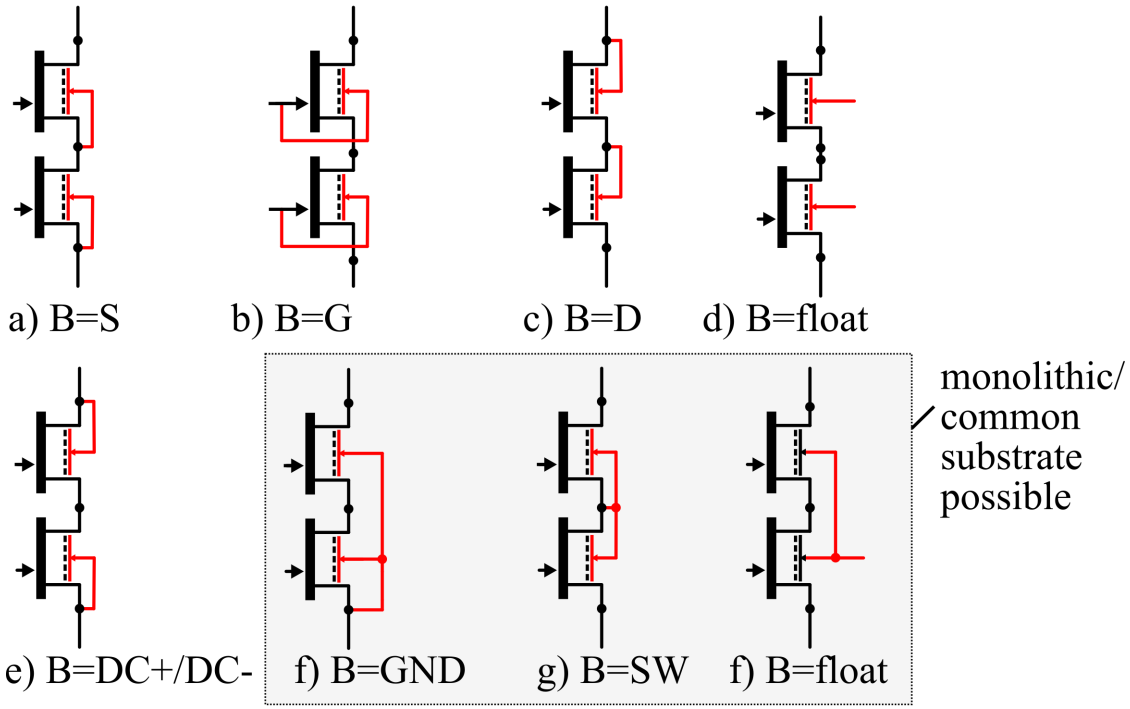

Figure 2.7: Overview on investigated substrate terminations. Further discussed variations with offset and biasing voltages and passive substrate biasing networks are not shown.

vice (as possible in discrete half-bridges) as well as common substrate terminations (for example of a monolithically integrated half-bridge) are investigated. While Fig. 2.7 classifies the substrate terminations into eight configurations, in the following for selected terminations further variations will be discussed. For example the addition of offset voltages instead of direct substrate terminations, or the addition of biasing networks to floating terminations.

2.5 Substrate Voltage Analysis

2.5.1 Substrate-to-Source Voltage Calculation for Fixed Substrate Terminations

For the substrate terminations, where the substrate terminal is referenced to another half-bridge transistor terminal with a fixed and constant voltage, the substrate-to-source voltage is derived from the drain-to-source or switch-node voltage as follows.

B=S substrate termination: For a direct B=S termination, the substrate-to-source voltage is zero, and can be adjusted by replacing the short-connection by offset voltage source ($V_{\mathrm{BS,0,LS}}$ and $V_{\mathrm{BS,0,HS}}$).

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = V_{\mathrm{BS}} = \begin{cases} 0\,\mathrm{V} & \text{(HS \& LS, no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.11}$$

B=G substrate termination: For the substrate-to-gate termination (B=G) in high-voltage circuits the analysis is simplified by the approximation that the gate voltage swing is small compared to the drain-source voltage switching. An offset voltage sources can replace a direct termination.

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = V_{\mathrm{BS}} \approx V_{\mathrm{BG}} = \begin{cases} 0\,\mathrm{V} & \text{(HS \& LS, no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.12}$$

B=D substrate termination: For a substrate-to-drain termination (B=D), the substrate-to-source voltage follows the drain-source voltage. Again, an offset voltage source can be added.

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = \begin{cases} V_{\mathrm{DS}} & \text{(HS \& LS, no offset)} \\ \begin{cases} V_{\mathrm{DS}} + V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{DS}} + V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.13}$$

In a half-bridge the high-side and low-side drain voltages $V_{\mathrm{DS,HS}}$ and $V_{\mathrm{DS,LS}}$ are linked by the constant dc-link voltage V_{DC}, and another formulation of Eqn. 2.13 as a function of the switch-node voltage instead of the individual drain-source voltages is

$$V_{\mathrm{BS}}(V_{\mathrm{SW}}) = \begin{cases} \begin{cases} V_{\mathrm{SW}} & \text{(LS)} \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} & \text{(HS)} \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{DS}} + V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} + V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.14}$$

B=DC+/DC- substrate termination: This mixed but fixed termination is a combination of the already discussed substrate terminations (high-side B=D and low-side B=S) and the substrate voltage is expressed as

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = \begin{cases} \begin{cases} 0\,\mathrm{V} & (\mathrm{LS}) \\ V_{\mathrm{DS}} & (\mathrm{HS}) \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & (\mathrm{LS}) \\ V_{\mathrm{DS}} + V_{\mathrm{BS,0,HS}} & (\mathrm{HS}) \end{cases} & \text{(with offset)} \end{cases} \tag{2.15}$$

Formulated as a function of the switch-node voltage in half-bridges:

$$V_{\mathrm{BS}}(V_{\mathrm{SW}}) = \begin{cases} \begin{cases} 0\,\mathrm{V} & (\mathrm{LS}) \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} & (\mathrm{HS}) \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & (\mathrm{LS}) \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} + V_{\mathrm{BS,0,HS}} & (\mathrm{HS}) \end{cases} & \text{(with offset)} \end{cases} \tag{2.16}$$

B=GND substrate termination: For a common substrate-to-ground (or DC-) termination (B=GND), the substrate of one of the half-bridge transistors is not connected to one of its own terminal nodes, but instead to an adjacent node of the other half-bridge transistor. Therefore, the substrate-to-source voltage of this transistor now depends on the magnitude of the dc-link voltage, and the formulation of the substrate-to-source voltage always includes the operation voltage. It is still possible to formulate the substrate voltage as a function of drain-to-source voltage, however, now also depending on V_{DC}.

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = \begin{cases} \begin{cases} 0\,\mathrm{V} & (\mathrm{LS}) \\ V_{\mathrm{DS}} - V_{\mathrm{DC}} & (\mathrm{HS}) \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & (\mathrm{LS}) \\ V_{\mathrm{DS}} - V_{\mathrm{DC}} + V_{\mathrm{BS,0,HS}} & (\mathrm{HS}) \end{cases} & \text{(with offset)} \end{cases} \tag{2.17}$$

Formated as a function of the switch-node voltage:

$$V_{\mathrm{BS}}(V_{\mathrm{SW}}) = \begin{cases} \begin{cases} 0\,\mathrm{V} & (\mathrm{LS}) \\ -V_{\mathrm{SW}} & (\mathrm{HS}) \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{BS,0,LS}} & (\mathrm{LS}) \\ -V_{\mathrm{SW}} + V_{\mathrm{BS,0,HS}} & (\mathrm{HS}) \end{cases} & \text{(with offset)} \end{cases} \tag{2.18}$$

The dc-link voltage can be considered as another offset voltage, similar to the previously discussed cases. For example, ac-wise, the B=GND termination without offset is similar (except for other absolute voltage levels) to the previously discussed B=DC+/DC- termination with a high-side offset voltage of $V_{\mathrm{BS,0,HS}} = V_{\mathrm{DC}}$.

B=DC+ substrate termination: In a similar way, a common B=DC+ substrate termination is possible, and is already covered (ac-wise, except other absolute voltage levels) by the equations from B=DC+/DC- with the offset voltage $V_{\mathrm{BS,0,LS}} = V_{\mathrm{DC}}$. Likewise, a fixed common substrate termination with any constant biasing voltage referenced to GND (or DC+) is already also covered by selecting the appropriate offset voltages.

B=SW substrate termination: A common substrate-to-switch-node termination (B=SW) consists of a low-side B=D and high-side B=S termination, and the substrate voltages are described by

$$V_{\mathrm{BS}}(V_{\mathrm{DS}}) = \begin{cases} \begin{cases} V_{\mathrm{DS}} & \text{(LS)} \\ 0\,\mathrm{V} & \text{(HS)} \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{DS}} + V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.19}$$

in a half-bridge the high-side and low-side drain voltages are linked by the constant dc-link voltage, and the substrate voltages are formulated as a function of the switch-node voltage as

$$V_{\mathrm{BS}}(V_{\mathrm{SW}}) = \begin{cases} \begin{cases} V_{\mathrm{SW}} & \text{(LS)} \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} & \text{(HS)} \end{cases} & \text{(no offset)} \\ \begin{cases} V_{\mathrm{DS}} + V_{\mathrm{BS,0,LS}} & \text{(LS)} \\ V_{\mathrm{DC}} - V_{\mathrm{SW}} + V_{\mathrm{BS,0,HS}} & \text{(HS)} \end{cases} & \text{(with offset)} \end{cases} \tag{2.20}$$

2.5.2 Substrate-to-Source Voltage Calculation for Floating Substrate Terminations

2.5.2.1 Separately Floating Substrate Terminations

In contrast to the fixed substrate terminations, where the substrate was fully-coupled by a short-circuit connection to one of the half-bridge nodes, a floating substrate is only partly coupled to the half-bridge nodes. The substrate however is still capacitively coupled to the half-bridge terminals through the substrate capacitances which still exist, even with a floating substrate termination. During the switching transitions any transient switch-node voltage change creates a displacement current through the substrate capacitances and influences the substrate voltage during switching transitions. Because the substrate capacitances are dependent on both the switch-node voltage (linked to the drain-source voltage V_{DS} and dc-link voltage V_{DC}) and the substrate voltage V_{BS}, and the substrate voltage is in turn influenced by the switch-node voltage change V_{SW}, the analysis requires careful consideration of the cross-coupling effects. In this section, the substrate voltage during a switching transition is formulated as an function of the switch-node voltage (for a given known initial offset voltage), which enables a simplified analysis of the floating substrate termination.

A coupling factor $k_{C,B} = \frac{dV_{BS}}{dV_{DS}}$ is introduced, which quantifies how much the drain-source voltage change (slew-rate $\frac{dV_{DS}}{dt}$) is coupled to substrate-to-source voltage change (slew-rate $\frac{dV_{BS}}{dt}$). Only passive substrate termination networks are considered by this work, and thus the coupling factor is limited to $k_{C,B} \in 0...1$. The coupling factor is defined for all substrate voltages V_{BS} which result from Eqn. 2.21 for $V_{DS} \in 0...V_{DC}$. During the switching transitions it is assumed that the capacitive displacement current through the substrate capacitances dominates any leakage current from the transistor or external highly-resistive biasing networks. Then the substrate network is a purely capacitive voltage divider in a star-connection, where the star-node is the substrate and outer nodes are drain and source (including the gate, for an almost constant gate-to-source voltage during the switching transition). From charge conservation [78] on the substrate node, the formulation of the substrate voltage for a floating substrate termination of an individual (half-bridge) transistor is

$$V_{BS}(V_{DS})|_{V_{BS,0}} = V_{BS,0} + \int_0^{V_{DS}} k_{C,B}(V_{DS}, V_{BS}(V_{DS})|_{V_{BS,0}}) dV_{DS} \tag{2.21}$$

where

$$k_{C,B}(V_{DS}, V_{BS}) = \frac{C_{BD,4T}(V_{DS}, V_{BS})}{C_{BS,4T}(V_{DS}, V_{BS}) + C_{BG,4T}(V_{DS}, V_{BS}) + C_{BD,4T}(V_{DS}, V_{BS})} \tag{2.22}$$

is the bias-dependent coupling factor. The boundary condition is that during on-state (either prior to or after a switching transition), the drain-source voltage is 0 V (simplified for a low on-state voltage compared to a high off-state voltage). The initial substrate offset voltage is $V_{BS,0} = V_{BS}(V_{DS} = 0)$.

In the half-bridge with separately floating substrates no direct cross-coupling between the high-side and low-side devices exists. Therefore the evaluation of Eqn 2.21 is valid for both the high-side and low-side transistors, when using the respective individual drain-source and substrate-to-source voltages of the respective device ($V_{DS,LS}, V_{BS,LS}, V_{BS,0,LS}$ for low-side and $V_{DS,HS}, V_{BS,HS}, V_{BS,0,HS}$ for high-side).

Numerical Calculation of Floating Substrate Voltage Eqn. 2.21 is an implicit function, but for a simplified analysis an explicit formulation of the substrate voltage V_{BS} as a function of only V_{DS} is beneficial, because it allows to substitute the substrate-to-source voltage dependence by a drain-source (or switch-node) voltage dependence. This work approximates the integral numerically by using the Riemann sum

$$\begin{aligned} V_{BS,k+1} &= V_{BS,k} \\ &+ \frac{C_{BD,4T}(V_{DS,k}, V_{BS,k})}{C_{BS,4T}(V_{DS,k}, V_{BS,k}) + C_{BG,4T}(V_{DS,k}, V_{BS,k}) + C_{BD,4T}(V_{DS,k}, V_{BS,k})} (V_{DS,k+1} - V_{DS,k}). \end{aligned} \tag{2.23}$$

If the measured capacitance data is on an equally spaced grid with step sizes ΔV_{DS}, ΔV_{BS}, then the Riemann sum in this equation can be calculated iteratively for each $V_{DS,k} = k\Delta V_{DS}$ from 0 Vto V_{DS} with a step size of ΔV_{DS}, if both 0 V and V_{DS} are grid points. Since V_{BS} is non-linearly increased in each step, $V_{BS,k}$ will not necessarily match

the measured grid points. Therefore, the capacitances are linearly interpolated between the two nearest measured V_{BS} values.

For a fine grid of measurement data, it was found that the Riemann sum is a sufficiently accurate approximation for the purpose of this work. The accuracy of the numerical approximation can be improved by reducing the voltage step of the capacitance measurement data or by using trapezoidal rule for numerical integration in at least the V_{DS} direction:

$$\begin{aligned} V_{BS,k+1} &= V_{BS,k} \\ &+\frac{1}{2}\left[\frac{C_{BD,4T}(V_{DS,k+1},V_{BS,k})}{C_{BS,4T}(V_{DS,k+1},V_{BS,k})+C_{BG,4T}(V_{DS,k+1},V_{BS,k})+C_{BD,4T}(V_{DS,k+1},V_{BS,k})}\right. \\ &\left.+\frac{C_{BD,4T}(V_{DS,k},V_{BS,k})}{C_{BS,4T}(V_{DS,k},V_{BS,k})+C_{BG,4T}(V_{DS,k},V_{BS,k})+C_{BD,4T}(V_{DS,k},V_{BS,k})}\right](V_{DS,k+1}-V_{DS,k}). \end{aligned} \tag{2.24}$$

2.5.2.2 Common Floating Substrate Termination

The analysis assumes a constant dc-link voltage V_{DC}, for example provided by the dc-link capacitors. The high-side and low-side drain-to-source voltages are linked to the switch-node voltage as

$$V_{DS,LS} = V_{SW} \tag{2.25}$$
$$V_{DS,HS} = V_{DC} - V_{SW}. \tag{2.26}$$

From the common substrate voltage V_B, which is referenced to the source of the low-side transistor (DC- node), the individual local substrate-to-source voltage of the half-bridge devices are linked to the switch-node voltage as

$$V_{BS,LS} = V_B \tag{2.27}$$
$$V_{BS,HS} = V_B - V_{SW}. \tag{2.28}$$

Similar to the already carried out analysis for separately floating substrate terminations in a discrete half-bridge, the common floating substrate-voltage V_B (e.g. in a monolithic half-bridge) follows from nodal analysis (capacitive voltage divider between DC+/DC-/SW and B) for a given initial offset voltage $V_{B,0} = V_B(V_{SW} = 0)$ and fixed dc-link voltage V_{DC} as

$$V_B(V_{SW})|_{V_{B,0},V_{DC}} = V_{B,0} + \int_0^{V_{SW}} k_{C,B}(V_{SW}, V_B(V_{SW})|_{V_{B,0},V_{DC}})\,dV_{SW}. \tag{2.29}$$

The capacitive substrate coupling coefficient is

$$\begin{aligned} &k_{C,B}(V_{SW},V_B) \\ &= \frac{C_{BD,LS,4T}(V_{DS,LS},V_{BS,LS})+C_{BS,HS,4T}(V_{DS,HS},V_{BS,HS})+C_{BG,HS,4T}(V_{DS,HS},V_{BS,HS})}{C_{B\Sigma,LS}(V_{DS,LS},V_{BS,LS})+C_{B\Sigma,HS}(V_{DS,HS},V_{BS,HS})}, \end{aligned} \tag{2.30}$$

where $C_{B\Sigma} = C_{BS,4T} + C_{BG,4T} + C_{BD,4T}$ is the sum of one transistor's substrate capacitances, and $V_{DS,LS}, V_{DS,HS}, V_{BS,LS}, V_{BS,HS}$ are only dependent on V_{SW} and V_B using the substitutions from Eqn. 2.25-2.28.

Numerical Calculation of Floating Substrate Voltage Eqn. 2.29 is again an implicit function. In this work, the integral is approximated by a numerical integration using a Riemann sum similar to Eqn. 2.23.

2.5.3 Transient Substrate Voltage Extrema and Swing

For each substrate termination, the absolute positive transient peak maximum (and minimum) of the substrate to any top-side terminal $V_{B,TOP,+} = \max(V_{BS+}, V_{BD+})$ (and $V_{B,TOP,-} = \min(V_{BS-}, V_{BD-})$) in switching operation determine the required vertical voltage blocking capability of the GaN buffer layer.

The substrate-to-source voltage swing ΔV_{BS} and the substrate-to-drain voltage swing ΔV_{BD} was found [42] to be related to the severity of dynamic trapping effects, and thus is also a useful quantity to compare substrate terminations. Furthermore, asymmetric buffer leakage depending on the substrate bias polarity can limit the operation voltage range of specific substrate terminations, if the required substrate voltage range exceeds the low-leakage region.

For the fixed substrate terminations the derivation of the quantities is trivial, since it directly results from the operation voltage. For example, for a B=S substrate termination with zero substrate offset voltage V_{DC}, the maximum and minimum substrate-to-source voltages are $V_{BS+} = 0\,V$ and $V_{BS-} = 0\,V$, the maximum and minimum substrate-to-drain voltages are $V_{BD+} = 0\,V$ and $V_{BD-} = -V_{DC}$, resulting in global maximum and minimum substrate-to-topside voltages $V_{B,TOP,+} = 0\,V$, $V_{B,TOP,-} = -V_{DC}$, the substrate-to-source voltage swing $\Delta V_{BS} = 0\,V$ and the substrate-to-drain voltage swing $\Delta V_{BD} = V_{DC}$. Only the floating substrate terminations require additional investigation of the extrema of transient substrate voltage, which is calculated in the following.

Separately Floating Substrate Terminations The average coupling factor over a full switching transition where the switch-node voltage changes between 0 V and V_{DC} is

$$\overline{k_{C,B}}\big|_{V_{BS,0}} = \frac{1}{V_{DC}} \int_0^{V_{DC}} k_{C,B}(V_{DS}, V_{BS}(V_{DS})|_{V_{BS,0}}) dV_{DS} \tag{2.31}$$

with the substrate coupling coefficient $k_{C,B}$ for separately floating substrates from Eqn. 2.22 and calculation of V_{BS} from Eqn. 2.23.

The substrate-to-source voltage swing during operation when switching V_{DC} follows as

$$\Delta V_{BS}|_{V_{BS,0}} = \overline{k_{C,B}}\big|_{V_{BS,0}} V_{DC}, \tag{2.32}$$

Since $0 \leq k_{C,B} \leq 1$ according to Eqn. 2.22, the substrate-to-source voltage swing (but not necessarily the initial offset voltage which is discussed later) is bounded between 0 V and V_{DC}.

The minimum and maximum absolute substrate-to-source voltages result from the initial substrate offset voltage and the voltage swing as $V_{\mathrm{BS,MIN}}|_{V_{\mathrm{BS,0}}} = V_{\mathrm{BS,0}}$ and $V_{\mathrm{BS,MAX}}|_{V_{\mathrm{BS,0}}} = V_{\mathrm{BS,0}} + \Delta V_{\mathrm{BS}}|_{V_{\mathrm{BS,0}}}$. During the conduction phase (on-state) of the transistor the substrate-to-source voltage $V_{\mathrm{BS,ON}} = V_{\mathrm{BS,MIN}}|_{V_{\mathrm{BS,0}}}$ is present.

Common Floating Substrate Termination The average coupling factor over a V_{DC} switching transition is

$$\overline{k_{\mathrm{C,B}}}\big|_{V_{\mathrm{B,0}}} = \frac{1}{V_{\mathrm{DC}}} \int_0^{V_{\mathrm{DC}}} k_{\mathrm{C,B}}(V_{\mathrm{SW}}, V_{\mathrm{B}}(V_{\mathrm{SW}})|_{V_{\mathrm{B,0}}}) dV_{\mathrm{SW}} \tag{2.33}$$

with the substrate coupling coefficient for a common floating substrate $k_{\mathrm{C,B}}$ from Eqn. 2.30 and calculation of V_{B} as explained in Sec. 2.5.2.2.

The low-side and high-side transistors are coupled through the common substrate, and thus the substrate-to-source voltage swings of the low-side and high-side transistors during operation when switching V_{DC} follow as

$$\Delta V_{\mathrm{BS,LS}}|_{V_{\mathrm{B,0}}} = \overline{k_{\mathrm{C,B}}}\big|_{V_{\mathrm{B,0}}} V_{\mathrm{DC}} \tag{2.34}$$

$$\Delta V_{\mathrm{BS,HS}}|_{V_{\mathrm{B,0}}} = (1 - \overline{k_{\mathrm{C,B}}}\big|_{V_{\mathrm{B,0}}}) V_{\mathrm{DC}}. \tag{2.35}$$

From the coupling of the low-side and high-side device and based on Eqns. 2.34-2.35 it is clear that with the common floating substrate termination at least one device is always subject to at least $\Delta V_{\mathrm{BS}} \geq \frac{1}{2} V_{\mathrm{DC}}$.

2.5.4 Semi-Floating Substrate Termination Networks

In the previous sections the substrate voltage during transient switching transitions was derived. However, so far the initial offset substrate voltages ($V_{\mathrm{B,0}}$ or $V_{\mathrm{BS,0,HS/LS}}$) have not been investigated and are discussed in this section.

If the substrate capacitances are considered as loss-less dielectrics without leakage currents, then the initial substrate voltage is set only by the initial charge on the substrate. From this initial condition, the transient substrate voltage follows. Since this condition is no well-defined, the operation of the transistor is not necessarily well-defined.

In a real transistor, the dielectric layer of the substrate capacitances consists of the GaN buffer layers. Depending on the type and epitaxy of the buffer, voltage-dependent and temperature-dependent vertical leakage currents exist, as already shown in Fig. 2.5. In a real transistor, even with a fully floating substrate termination, the initial and average substrate voltage is set by a steady-state condition of the vertical substrate leakage currents. The steady-state condition for the average substrate voltage is when the sum of all vertical leakage currents to the substrate is zero.

While for lower voltage devices (for example 48 V half-bridges) the fully-floating substrate is a viable and simple solution, for higher voltage devices the only weakly defined substrate voltages resulting only from vertical leakage currents can result in undesired

substrate-to-source voltages during operation. For example, highly negative substrate-to-source-voltages of the high-side device can result and cause static back-gating and thus reduce the on-resistance of the transistor.

An approach to manually set the initial (and thus also transient) substrate voltages is to use an additional substrate biasing network which superimposes the leakage currents and enables to manually set the initial and average substrate voltages to desired values. One way to realize the substrate biasing network is to connect a highly-resistive voltage divider network between the substrate and other half-bridge or transistor nodes. By dimensioning of the resistances of the divider for currents at least ten times higher than the maximum expected vertical leakage current, the resistive network superimposes the vertical leakage currents and thus manually biases the substrate. The first substrate biasing network for a monolithic GaN high-voltage half-bridge with floating substrate was proposed and published by B. Weiss in [59]. With the approach of the substrate biasing network, in [59] for the first time the operation of a monolithic GaN-on-Si half-bridge was experimentally demonstrated at operation voltages as high as 400 V under soft-switching conditions. This work generalizes the approach from [59] to discrete half-bridges (with separately floating substrates), and proposes an improved biasing network for monolithic half-bridges which overcomes an operation-limiting duty-cycle dependency of the circuit from [59]. In this work, as in [59], the term *semi-floating* is used for a floating substrate termination where the initial and average substrate voltage are not truly floating, but instead defined by a highly-resistive network which superimposes vertical leakage currents. Since a highly-resistive biasing network in conjunction with the substrate capacitances has a very slow RC time constant compared to typical switching transition times or switching periods in converters, only the offset (or average) substrate voltage is adjusted, but the transient behavior during switching transitions as derived in Eqn. 2.27 and Eqn 2.28 are not affected and the analysis still valid.

In the entire work, the term "floating" substrate always refers to a "semi-floating" substrate termination with a highly-resistive substrate termination network and known offset-voltages, and not to a truly floating substrate, where only the vertical leakage currents determine the substrate offset voltage.

Separately Floating Substrate Biasing Network For half-bridges with separate transistors which are not coupled through a common substrate, this work proposes the semi-floating substrate termination network in Fig. 2.8. The highly-resistive network has an upper and lower highly-resistive resistor ($R_{\mathrm{SF,H}}$ and $R_{\mathrm{SF,L}}$) connecting the drain, substrate and source. The resistance values are selected highly-resistive to limit additional power losses, and are dimensioned such that the current through $R_{\mathrm{SF,H}}$ and $R_{\mathrm{SF,L}}$ is at least 10 times higher compared to the expected vertical substrate leakage currents. The voltage rating of the resistors has to be at least the full intended operation voltage of the transistor. With the dimensioning $R_{\mathrm{SF,H}} = R_{\mathrm{SF,L}}(1/\left.\overline{k_{\mathrm{C,B}}}\right|_{V_{\mathrm{BS,0}}=0\,\mathrm{V}} - 1)$ of the divider, the circuit generates a zero offset-voltage $V_{\mathrm{BS,0}} = 0\,\mathrm{V}$, which is also present during the on-state $V_{\mathrm{DS}} = 0\,\mathrm{V}$ and thus avoids static back-gating. Furthermore, the dimensioning ensures that the substrate voltage follows the natural response of the capacitive substrate capacitances during switching transitions according to Eqn. 2.21. During off-state, when

the transistor blocks the full input voltage V_{DC}, a positive substrate-to-source voltage $V_{BS+} = V_{DC}\,\overline{k_{C,B}}\big|_{V_{BS,0}=0\,V}$ is present.

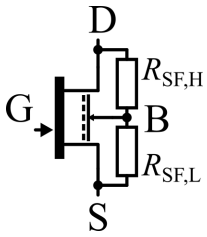

Figure 2.8: Semi-floating substrate termination using highly-resistive voltage divider.

Common Floating Substrate Biasing Network Fig. 2.9a shows a first semi-floating substrate biasing network for half-bridges on a common coupled substrate, which was proposed by B. Weiss in [59]. Even though the biasing network was found to be effective to reduce substrate biasing effects under certain conditions, the circuit has a drawback: Due to the connection of the voltage divider only to the fixed input voltages V_{DC} and GND and the substrate B, the absolute offset voltage $V_{B,0}$ depends on the duty cycle of the half-bridge during switching operation. This was also already observed and described in [79]. For duty cycles (here the ratio of low-side on-time to a switching cycle time) approaching 100%, the offset voltage is $V_{B,0} \approx 0\,V$ and for duty-cycles approaching 0%, the offset voltage is $V_{B,0} \approx V_{DC} - \Delta V_B$. In applications where the full duty-cycle range between 0% to 100% is used, also a very wide range of substrate voltages $V_{BS} = -\Delta V_B ... + V_{DC}$ and $V_{BD} = -V_{DC} ... + \Delta V_B$ during operation is required. The span $V_{DC} + \Delta V_B > V_{DC}$ of this range is even higher than the actual operation voltage V_{DC}, and thus gives rise to unnecessarily increased vertical substrate voltages. The substrate-to-source voltage during the conduction phases of the high-side transistor varies also with changing duty-cycle. As a result, operation points with highly negative substrate and thus significant static back-gating voltages occur and on the other hand, highly positive substrate voltages also occur.

To decouple the transient substrate bias voltages from the duty-cycle during operation, this work proposed a novel improved duty-cycle independent substrate biasing network for GaN-on-Si half-bridges, first published by the author in [50].

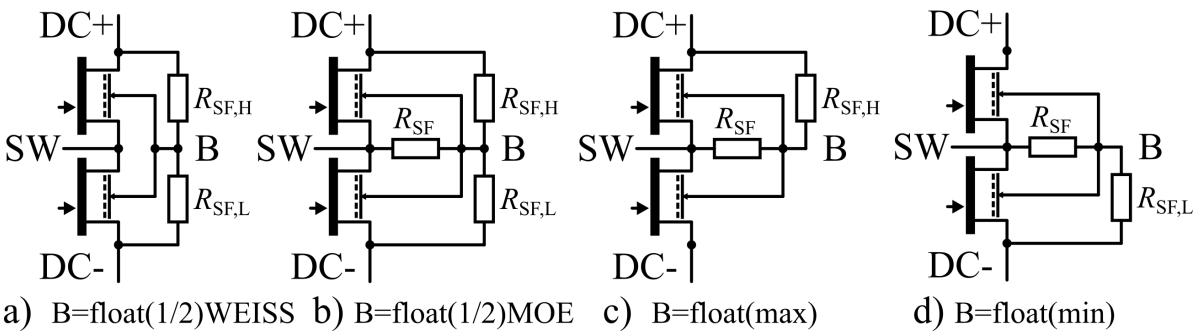

Figure 2.9: Semi-floating substrate termination using highly-resistive voltage-divider networks: a) the circuit from [59] (duty-cycle dependent) b) this work: duty-cycle independent network.

Fig. 2.9b shows the improved semi-floating substrate biasing network proposed by this work (as published by the author in [50]) which is duty-cycle independent (in contrast to Fig. 2.9a). The circuit includes the switching state into the biasing network by an additional path of the resistive divider to the switch-node.

Dimensioning of the resistive network allows to duty-cycle independently set the substrate offset voltage. With the dimensioning

$$\begin{aligned} R_{\mathrm{SF,H}} &= R_{\mathrm{SF}} \frac{\Delta V_{\mathrm{B}}}{V_{\mathrm{B,0}}} \\ R_{\mathrm{SF,L}} &= R_{\mathrm{SF}} \frac{\Delta V_{\mathrm{B}}}{V_{\mathrm{DC}} - (V_{\mathrm{B,0}} + \Delta V_{\mathrm{B}})}, \end{aligned} \tag{2.36}$$

the network tracks the natural substrate voltage swing ΔV_{B} and at the same time allows adjustable offset voltages between a minimum $V_{\mathrm{B,0}} = 0\,\mathrm{V}$ and maximum $V_{\mathrm{BS,0}} = V_{\mathrm{DC}} - \Delta V_{\mathrm{B}}$.

Now, in applications where the full duty-cyclce range between 0% to 100% is used, only the reduced range of substrate voltages $V_{\mathrm{BS}} = V_{\mathrm{B,0}} \ldots V_{\mathrm{B,0}} + V_{\mathrm{DC}}$ during operation is required. The span V_{DC} of this range is limited to the actual operation voltage V_{DC}, and thus a significant reduction compared to the previous duty-cycle dependent biasing network.

For the dimensioning with the highest offset voltage $V_{\mathrm{B,0}} = V_{\mathrm{DC}} - \Delta V_{\mathrm{B}}$ which the dimensioning of the biasing network allows, the biasing network simplifies to the circuit in Fig. 2.9c, since $R_{\mathrm{SF,L}} \to \infty$ according to Eqn. 2.36. The dimensioning rule from Eqn. 2.36 simplifies to $R_{\mathrm{SF}} = R_{\mathrm{SF,H}}(\frac{V_{\mathrm{DC}}}{\Delta V_{\mathrm{B}}} - 1)$ and the resistor for $R_{\mathrm{SF,L}}$ is omitted. If $\Delta V_{\mathrm{B}} \approx \frac{1}{2} V_{\mathrm{DC}}$ is assumed as approximately observed in experiments [79], the approximation $R_{\mathrm{SF}} = R_{\mathrm{SF,H}}$ results and is useful as a rough dimensioning for the practical implementation of the biasing network for prototypes.

The special case with the most positive offset voltage (Fig. 2.9c) is found to be beneficial, because at all times during conduction phases of either the low-side or high-side transistor, the substrate-to-source voltage of the respective transistor is non-negative and approximately zero, thus avoiding static back-gating. This is in contrast to the biasing network from Fig. 2.9a, where the high-side transistor is subject to a negative substrate-to-source voltage of $V_{\mathrm{BS,HS,ON}} \approx -\frac{1}{4} V_{\mathrm{DC}}$ at 50% duty-cycle, which caused static back-gating and on-resistance increase in [42].

Another special case with the most negative substrate offset voltage is shown in Fig. 2.9d and reduces to a two-resistor biasing network in a similar way.

2.5.5 Calculation of Substrate Voltages using Measured Capacitance Data

This sections presents the calculated dependency of the substrate-voltage from the switch-node voltage, as was theoretically derived in Sec. 2.5.2.1 and Sec. 2.5. The calculation is based on the multi-bias dependent measured capacitance data shown in Appendix A.3. Since it was shown that for particular substrate terminations the capacitances depend on the dc-operation voltage, here the calculation is carried out for $V_{\mathrm{DC}} = 200\,V$.

Fig. 2.10 shows the calculated substrate-to-source voltages of the low-side $V_{BS,LS}$ (solid) and high-side $V_{BS,HS}$ (dashed) transistors as a function of the switch-node voltage V_{SW}. Depending on the substrate termination, a wide range of substrate-to-source voltages are required during operation. For the B=fixed-to-GND(com,min) termination, the most negative substrate voltage $V_{BS} = -V_{DC}$ is present for the high-side device. Likewise, the highest positive substrate voltage $V_{BS} = +V_{DC}$ is present for several other substrate terminations. If the negative substrate potential occurs during the conduction-phase of the respective transistor, then back-gated on-resistance increase is expected.

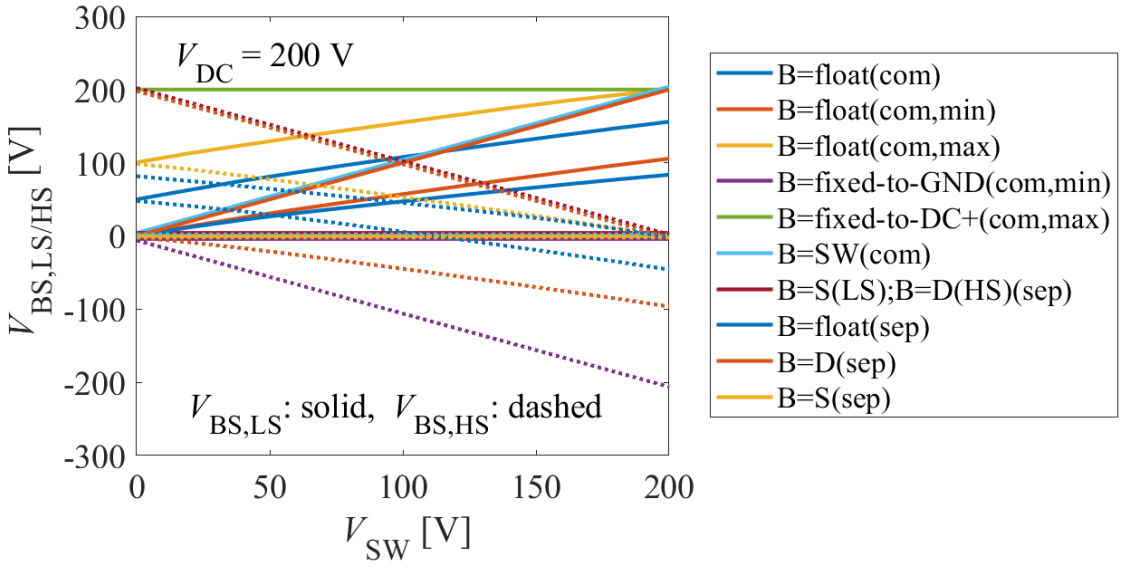

Figure 2.10: Substrate-voltage as a function of switch-node voltage $V_{BS}(V_{SW})$.

Fig. 2.11 visualizes the results from Fig. 2.10 in a different way. For each substrate termination, the required range of substrate-to-source voltage for the high-side and low-side device is shown. Since the back-gated on-resistance increase is mainly relevant during the conduction phase of the transistor, the on-state and off-state are marked with a circle and dash symbol, respectively.

2.6 Capacitance Transformation for Half-Bridges to Eliminate Substrate Dependence

This chapter carries out an equivalent circuit transformation to eliminate the substrate-connected capacitances and thus also the substrate voltage dependence for each substrate configuration from the analysis. The result of the method is an equivalent half-bridge capacitance formulation, which enables a quantification and comparison of the effective device capacitances of all half-bridge configurations using conventional application-oriented $C_{ISS}, C_{OSS}, C_{RSS}$ without the difficulty of the substrate as an additional node. The method enables a direct comparison of conventional half-bridges with discrete transistors, monolithic half-bridges as well as all discussed half-bridge configurations with different substrate terminations.

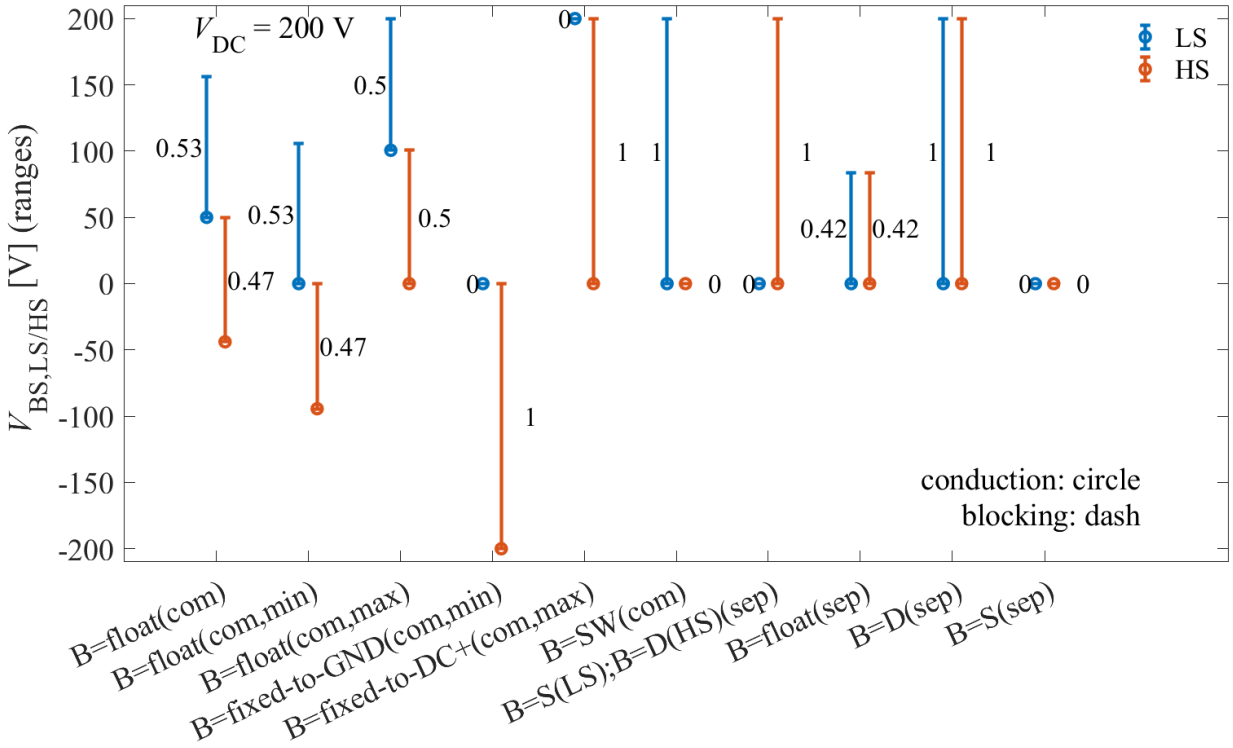

Figure 2.11: Range of substrate-to-source voltages for the high-side and low-side device for different substrate terminations. The on-state and off-state are marked to identify terminations with negatively back-gated conduction phases.

It should be noted that all discussed terminal capacitances are depending on the drain-to-source, substrate-to-source and gate-to-source voltages of the low-side and high-side device ($V_{DS,LS}, V_{BS,LS}, V_{GS,LS}$ and $V_{DS,HS}, V_{BS,HS}, V_{GS,HS}$, respectively). In this work, only the off-state capacitances are considered ($V_{GS} = V_{GS,OFF}$) to simplify the analysis, and also because typically only the off-state capacitances are known and measured. Even with this simplification, the considered capacitances are still non-linear and depended on multiple bias voltages (drain and substrate). A similar multi-bias dependence is often considered in RF circuits, where the drain and gate voltages are included in the analysis [80], instead of the drain and substrate as in this work. It should be noted that typical data-sheets of power transistors also do not provide on-state capacitances since the off-state capacitances already provide a sufficient degree of detail and reduced computational complexity for switched-mode converter circuit simulations. This work carries out an theoretical and experimental analysis, however, the measured capacitances can also be modeled to use circuit simulations. A model approach for GaN power HEMTs which includes the impact of the substrate voltage is published in [81]. For the sake of readability, throughout this chapter this voltage dependencies $C_{ij}(V_{DS}, V_{BS}, V_{GS})$ are not repeated in the following.

Furthermore, for half-bridge operation a constant dc-link operation voltage V_{DC} is assumed, such that the high-side and low-side voltages (for example $V_{DS,LS}$ and $V_{DS,HS}$) are linked through the dc-link voltage.

2.6.1 Method for Half-Bridges Without and With Coupled Substrates

The proposed capacitance transformation method consists of three steps:

- Formulation of the substrate-to-source voltage as a function of drain-source (or switch-node) voltage $V_{BS} = V_{BS}(V_{DS})$ (or $V_B = V_B(V_{SW})$). The derivation of all substrate voltage formulations has already been carried out in Sec. 2.5.1-2.5.2.
- Star-to-mesh transformation of all substrate-connected capacitances. This step eliminates the substrate node from the analysis.
- Summing of all capacitance contributions between the remaining half-bridge nodes. Based on this step's result, the application-oriented and comparable capacitances such as $C_{ISS}, C_{OSS}, C_{RSS}$ directly result.

The method is discussed first for a half-bridge based on two discrete transistors, which are only coupled through the switch-node, but not the substrate. Then, discrete and monolithic half-bridges are discussed, where an additional cross-coupling path through a coupled common substrate node exists.

Transistors for Half-Bridges Without Substrate Coupling: Fig. 2.12 illustrates the concept of the transformation for discrete transistors. Only a single transistor is shown, because the method for half-bridges without substrate coupling allows a separate calculation of the high-side and low-side capacitances. Fig. 2.12 shows the full four-terminal capacitance circuit, where all capacitances are multi-bias dependent on V_{DS}, V_{BS}, V_{GS} and no specific substrate termination is assumed. Then, for each investigated substrate termination, the substrate-to-source voltage is formulated as a function of the drain-source voltage $V_{BS} = V_{BS}(V_{DS})$ as described in Sec. 2.5.1-2.5.2. The transistor is furthermore analyzed in off-state $V_{GS} = V_{GS,OFF}$, since also the capacitances are measured in off-state. Fig. 2.12b shows the results of the two voltage substitutions, where all capacitances now only depend on the drain-source voltage. Finally, for the floating substrate termination a star-to-delta transformation of the substrate capacitances is carried out to eliminate the substrate node. For the fixed substrate terminations, no star-to-delta transformation is required. Finally, the substrate capacitances for the fixed terminations, or the transformed capacitances for the floating termination, are summed with the remaining terminal capacitances into equivalent three-terminal transistor capacitances, shown in Fig. 2.12c. Based on the resulting three-terminal capacitances, it is also possible to directly calculate the application-oriented capacitances $C_{ISS}, C_{OSS}, C_{RSS}$.

Transistors for Half-Bridges with Substrate Coupling: While the effective capacitance description of a discrete transistor as a single device is also sufficient and valid to describe the same device in a half-bridge, for four-terminal transistors this is not always the case: If the conductive substrates of the high-side and low-side transistor in a half-bridge are coupled, as for example in a monolithic GaN-on-Si half-bridge, an additional coupling path is created through the common substrate. In this general case of a half-bridge based on four-terminal transistors with possibly coupled substrates, it is still

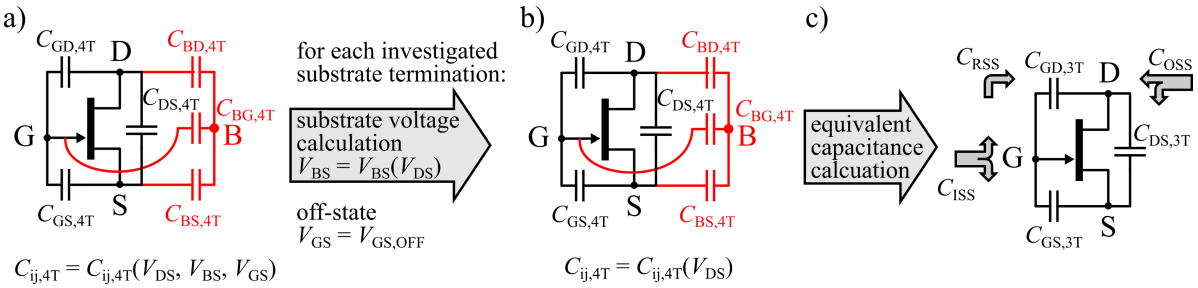

Figure 2.12: Four to three terminal substrate capacitance transformation method for discrete transistors.

possible to carry out an equivalent circuit transformation using star-to-mesh transformation (a generalized version of star-to-delta transformation, described in Appendix A.1. The star-to-mesh transformation successfully enables to remove the substrate nodes by redistributing the substrate-connected capacitances to equivalent capacitance between only gate, drain and source. However, due to the additional possible cross-coupling path, for specific common or coupled substrate terminations, a high-to-low-side gate-to-gate cross-coupling capacitance results. Nevertheless, because the 4-terminal to 3-terminal transformation removes the six substrate capacitances and only adds one cross-coupling capacitance, the transformed 3-terminal capacitance description is still preferred for further analysis. Since in general a cross-coupling capacitance can arise from the capacitance transformation, this work proposes to introduce a new effective capacitance, the (gate-to-gate) cross-coupling capacitance C_{XSS}. As a result, it is possible to fully describe a half-bridge with coupled substrate (as in a monolithic GaN half-bridge on conductive Si substrate) using the well-known effective capacitances C_{ISS}, C_{OSS}, C_{RSS} and the proposed C_{XSS}. Fig. 2.13 shows the generalized method for the 4-terminal to 3-terminal capacitance transformation, including a possible cross-coupling path through the substrate, which is lumped as C_{XSS} by the transformation.

It should be noted that in the following the terms describing the substrate terminations (such as B=S, B=D, B=G, ...) can be a AC+DC short, but for the analysis an AC short is sufficient. This means that for example B=S covers both the special case with zero offset voltage $V_{BS} = 0\,\mathrm{V}$ (AC+DC short), and the generalized case with a constant offset voltage $V_{BS}(t) = \text{const.}$ (only AC short). If an offset voltages is not explicitly mentioned, the AC+DC short case is assumed.

In addition to the capacitive cross-coupling between integrated devices which is discussed in this chapter, also further cross-coupling effects exist, such as conduction current degeneration from electrodes with high voltages nearby to integrated devices [82, 83].

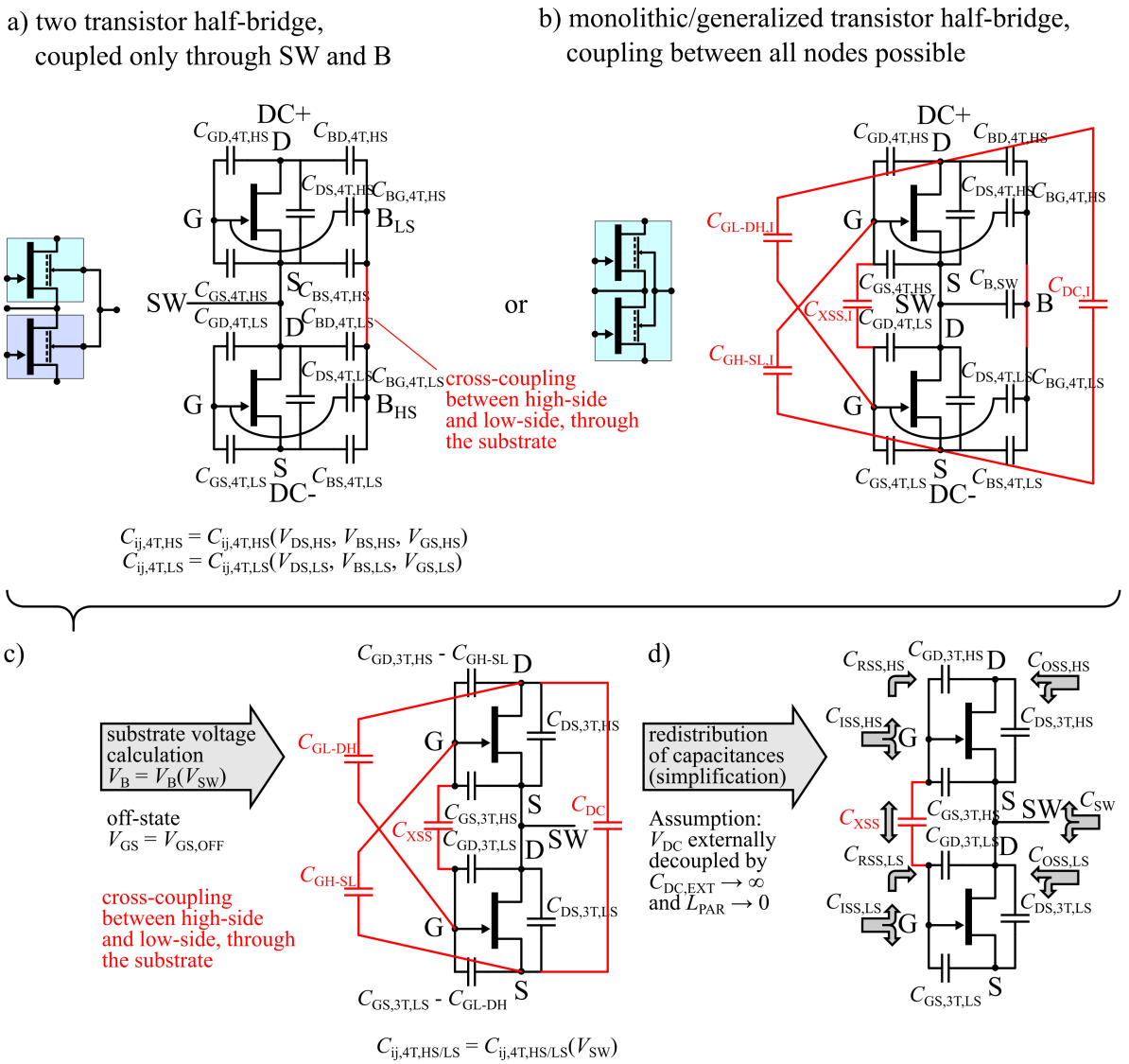

Figure 2.13: Substrate capacitance transformation method to transform discrete or monolithic half-bridges with a coupled common substrate to an equivalent half-bridge with eliminated substrate node, replaced by a pre-calculated substrate voltage calculation.

2.6.2 B=S (conventional) Termination

Even though lateral GaN-on-Si HEMTs are 4-terminal devices, they are often used in a 3-terminal configuration using a defined termination of the substrate terminal to one of the 3 other terminals. The most conventional substrate termination used in commercially available discrete power GaN-on-Si HEMTs is a substrate-to-source (B=S) termination. Fig. 2.14 illustrates the conventional B=S substrate termination.

4-terminal to 3-terminal reduction results in

$$C_{GS,3T} = C_{GS,4T} + C_{BG,4T} \tag{2.37}$$
$$C_{GD,3T} = C_{GD,4T} \tag{2.38}$$
$$C_{DS,3T} = C_{DS,4T} + C_{BD,4T} \tag{2.39}$$

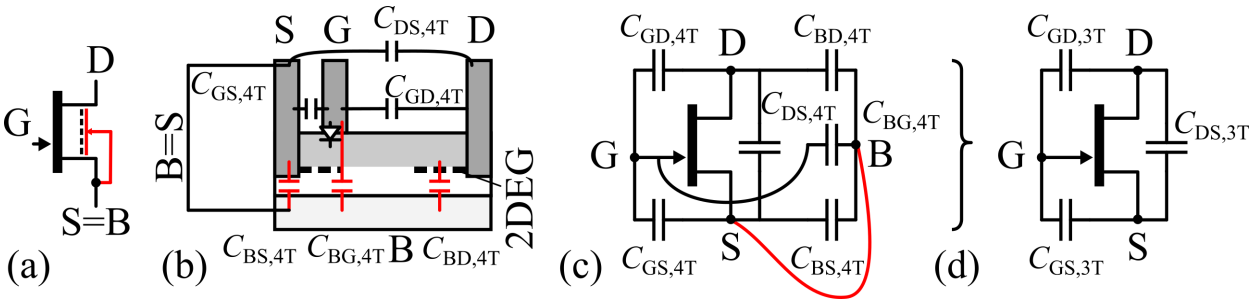

Figure 2.14: Substrate-to-source (B=S) termination of a single transistor. a) Schematic. b) Cross-Section. c) Full capacitive circuit. d) Transformed equivalent capacitive circuit.

A direct B=S termination, which is typical for commercial discrete high-voltage power GaN-on-Si transistors, was shown in Fig. 2.14 with $V_{BS,0} = 0\,V$. As a generalized B=S termination an offset voltage referenced to source $V_{BS,0} \neq 0\,V$ can be applied between the substrate and source, which is also covered by the equations.

Due to B=S, C_{BS} is shorted out and does not contribute to the dynamic behavior of the device. On the other hand, C_{BD} is completely effective and contributes to C_{OSS}. In typical high-voltage power HEMT devices with source-field plates which typically overlap the gate terminal, the substrate-to-source termination effectively shields the gate from the drain terminal, thus C_{RSS} is very low at higher drain-source voltages and only $C_{GD,4T}$ contributes to C_{RSS}.

2.6.3 B=D Termination

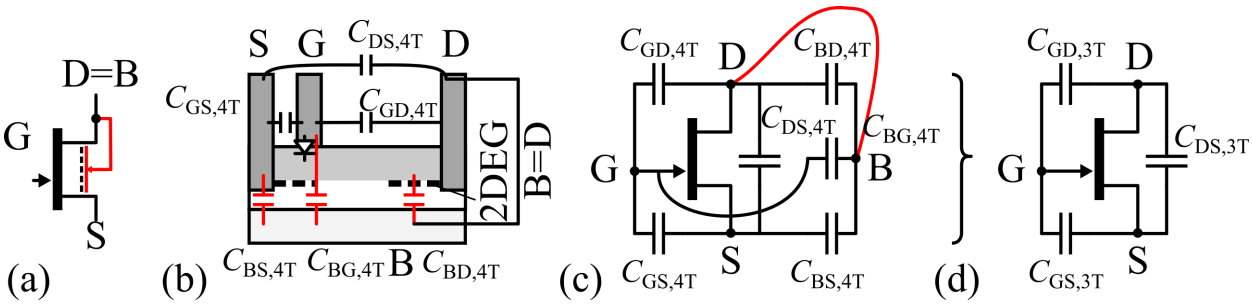

Figure 2.15: Substrate-to-drain (B=D) termination of a single transistor. a) Schematic. b) Cross-Section. c) Full capacitive circuit. d) Transformed equivalent capacitive circuit.

4-terminal to 3-terminal reduction results in

$$C_{GS,3T} = C_{GS,4T} \tag{2.40}$$
$$C_{GD,3T} = C_{GD,4T} + C_{BG,4T} \tag{2.41}$$
$$C_{DS,3T} = C_{DS,4T} + C_{BS,4T} \tag{2.42}$$

Due to B=D, C_{BD} is shorted out and does not contribute to the dynamic behavior of the device. A direct B=D termination is shown in Fig. 2.15 with $V_{BD,0} = 0\,V$. As a generalized B=D termination an offset voltage referenced to drain $V_{BD,0} \neq 0\,V$ can be applied to the substrate and is also covered by the equations.

For the B=D termination, $C_{GD,3T}$ is significantly increased compared to the B=S termination, since $C_{BG,4T}$ is now fully coupled to the gate-to-drain path.

2.6.4 B=G Termination

The B=G substrate termination is only discussed for the sake of completeness and not further considered in this thesis, because no significant advantage for applications resulting from this substrate termination in half-bridges was found using this termination in high-voltage half-bridge circuits. It should be mentioned however, that the B=G substrate termination is often used in lower voltage RF circuits, for example in common-gate amplifiers. Also, the B=G termination can be useful in a Baliga-pair (cascode), where a high-voltage transistor is in series with a low-voltage transistor (e.G. Si-MOSFET). If the gate of the high-voltage transistor is tied to the source of the low-voltage transistor (GaN HEMT), a B=G substrate termination can simplify the assembly of a cascode package, because both the low-voltage source and high-voltage transistor's substrate can share a common electrically connected thermal pad.

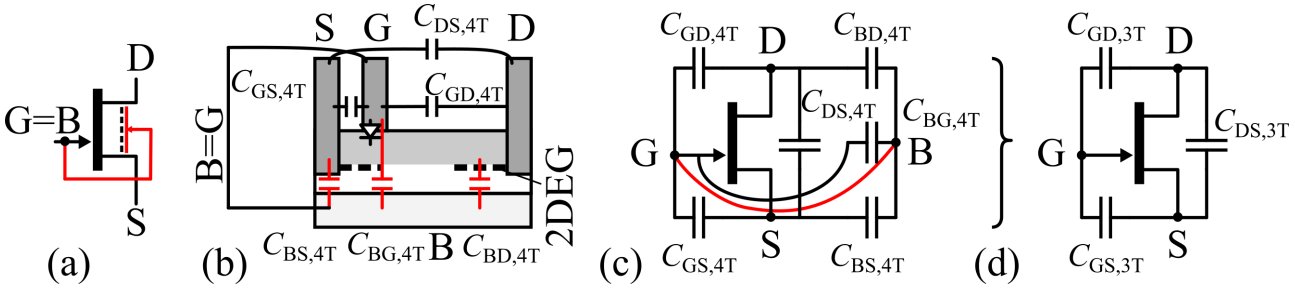

Figure 2.16: Substrate-to-gate (B=G) termination of a single transistor. a) Schematic. b) Cross-Section. c) Full capacitive circuit. d) Transformed equivalent capacitive circuit.

4-terminal to 3-terminal reduction results in

$$C_{GS,3T} = C_{GS,4T} + C_{BS,4T} \tag{2.43}$$
$$C_{GD,3T} = C_{GD,4T} + C_{BD,4T} \tag{2.44}$$
$$C_{DS,3T} = C_{DS,4T} \tag{2.45}$$

2.6.5 Separately B=Floating Termination (Discrete Devices)

With ΔY transformation, the 4-terminal to 3-terminal reduction results in

$$C_{GS,3T} = C_{GS,4T} + C_{BG,4T}\overbrace{\left(\frac{C_{BS,4T}}{C_{BS,4T}+C_{BG,4T}+C_{BD,4T}}\right)}^{<1} \tag{2.46}$$
$$C_{GD,3T} = C_{GD,4T} + C_{BG,4T}\left(\frac{C_{BD,4T}}{C_{BS,4T}+C_{BG,4T}+C_{BD,4T}}\right) \tag{2.47}$$
$$C_{DS,3T} = C_{DS,4T} + C_{BD,4T}\left(\frac{C_{BS,4T}}{C_{BS,4T}+C_{BG,4T}+C_{BD,4T}}\right) \tag{2.48}$$

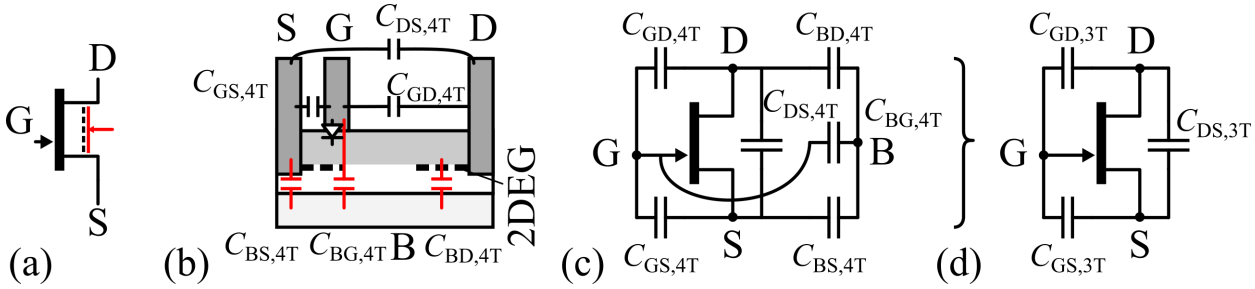

Figure 2.17: Floating substrate (B=float) termination of a single transistor. a) Schematic. b) Cross-Section. c) Full capacitive circuit. d) Transformed equivalent capacitive circuit.

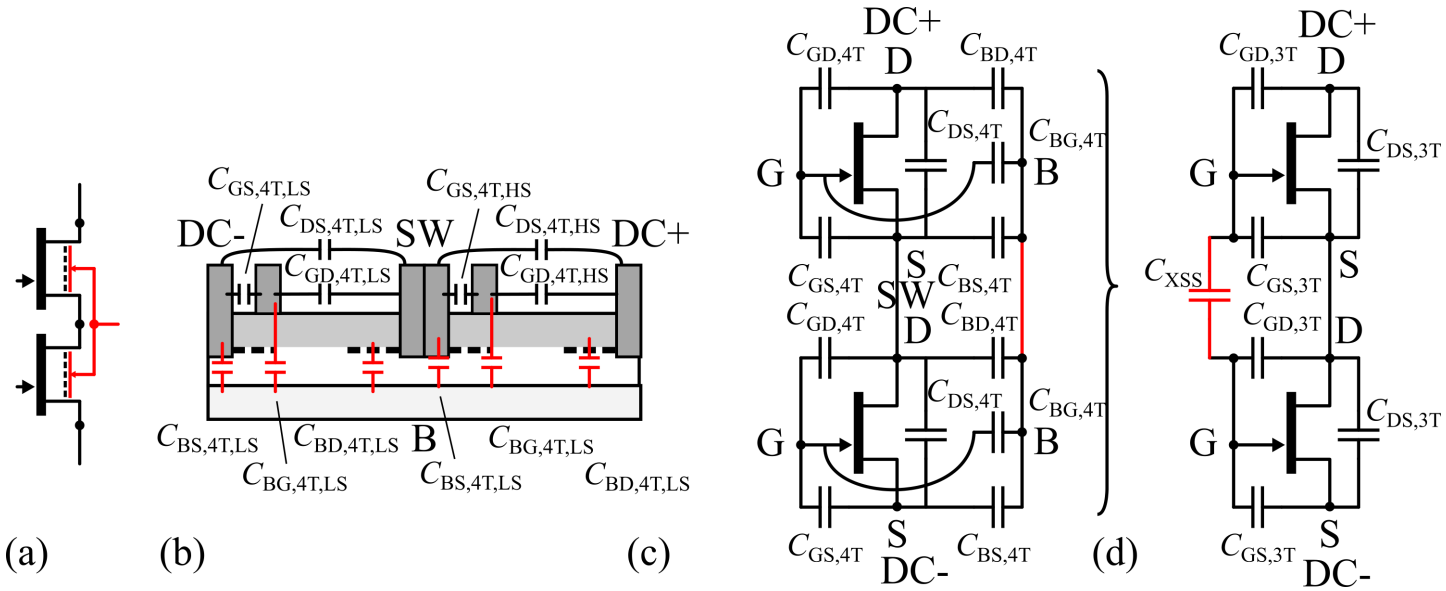

Figure 2.18: Floating substrate (B=float) termination of two transistors in a a half-bridge with a coupled common conductive substrate. a) Schematic. b) Cross-Section. c) Full capacitive circuit. d) Transformed equivalent capacitive circuit.

The capacitance transformation method for the separately floating transistors as in Eqn. 2.48 was initially derived for the special case of a half-bridge and bias-independent capacitances during the Master's thesis of Ren Li [84], and later also adapted by the Master's thesis of Alexander Beeren [85], both supervised by the author.

Due to the floating substrate, the substrate capacitances are now partly coupled to all top-side capacitances.

2.6.6 Common B=Floating Termination (Half-Bridge)

4-terminal to 3-terminal reduction of the half-bridge with both transistors being coupled through the substrate is possible using star-to-mesh transformation, a generalized method of star-to-delta transformation. The star-node is the common substrate B, with star-capacitances connected to the five nodes: DC- (=S_{LS}), SW (=$D_{LS} = S_{HS}$), DC+ (=D_{HS}) and both gates (G_{LS}, G_{HS}).

The first part of the capacitance transformation (from Fig. 2.13a/b to Fig. 2.13c) gives

$$C_{GL-DH} = C_{GL-DH,I} + \frac{C_{BG,4T,LS} C_{BD,4T,HS}}{C_{B\Sigma}} \quad (2.49)$$

$$C_{GH-SL} = C_{GH-SL,I} + \frac{C_{BG,4T,HS} C_{BS,4T,LS}}{C_{B\Sigma}} \quad (2.50)$$

where

$$C_{B\Sigma} = (C_{BS,4T,LS} + C_{BG,4T,LS} + C_{BD,4T,LS}) + (C_{BS,4T,HS} + C_{BG,4T,HS} + C_{BD,4T,HS}) \quad (2.51)$$

$$C_{XSS} = C_{XSS,I} + \frac{C_{BG,4T,LS} C_{BG,4T,HS}}{C_{B\Sigma}} \quad (2.52)$$

$$C_{DC} = C_{DC,I} + \frac{C_{BS,4T,LS} C_{BD,4T,HS}}{C_{B\Sigma}} \quad (2.53)$$

The second part of the capacitance transformation (from Fig. 2.13c to Fig. 2.13d) then gives the transformed capacitances

$$C_{GS,3T,LS} = C_{GS,4T,LS} + \frac{C_{BG,LS}(C_{BS,LS} + C_{BD,HS})}{C_{B\Sigma}} \quad (2.54)$$

$$C_{GS,3T,HS} = C_{GS,4T,HS} + \frac{C_{BG,HS}(C_{BS,HS} + C_{BD,LS})}{C_{B\Sigma}} \quad (2.55)$$

$$C_{GD,3T,LS} = C_{GD,4T,LS} + \frac{C_{BG,LS}(C_{BD,LS} + C_{BS,HS})}{C_{B\Sigma}} \quad (2.56)$$

$$C_{GD,3T,HS} = C_{GD,4T,HS} + \frac{C_{BG,HS}(C_{BD,HS} + C_{BS,LS})}{C_{B\Sigma}} \quad (2.57)$$

$$C_{DS,3T,LS} = C_{DS,4T,LS} + \frac{C_{BS,LS}(C_{BD,LS} + C_{BS,HS})}{C_{B\Sigma}} \quad (2.58)$$

$$C_{DS,3T,HS} = C_{DS,4T,HS} + \frac{C_{BD,HS}(C_{BD,LS} + C_{BS,HS})}{C_{B\Sigma}} \quad (2.59)$$

The transformed capacitances now allow a quantitative calculation of C_{ISS}, C_{OSS}, C_{RSS} according to Eqn.2.1-2.3.

As for the separately floating substrates, here now again the substrate capacitances are partly coupled to all top-side capacitances.

2.7 Calculated Switching Characteristics for Different Substrate Terminations

2.7.1 Output-Related Effective Capacitances C_{OSS}, C_{SW}, C_{DC}

Fig. 2.19 shows the calculated output-related effective capacitances $C_{OSS,LS}$ and $C_{OSS,HS}$ of the low-side and high-side devices in a half-bridge as a function of the respective drain-source voltage ($V_{DS,LS}$ and $V_{DS,HS}$) for all investigated substrate terminations. The data

is calculated using the previously described methods (Sec. 2.5, Sec. 2.6) and based on the multi-bias dependent measured four-terminal capacitances from Sec. 2.2.3. For substrate terminations where the drain-source voltage is linked to the dc-link voltage, an operation voltage of 200 V is assumed. To avoid overlapping lines, the different lines are slightly shifted in the y-direction.

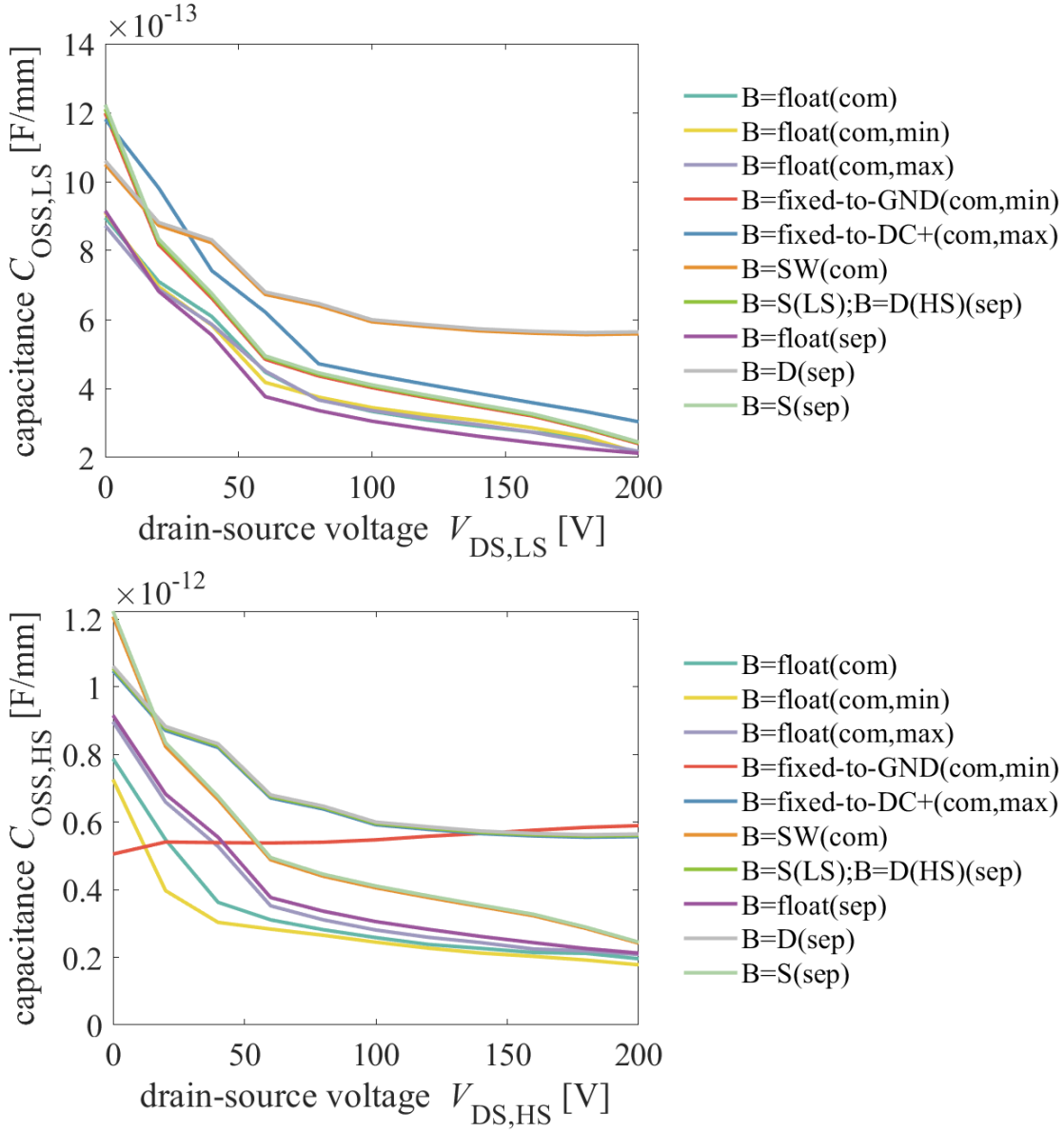

Figure 2.19: Output capacitance C_{OSS} as a function of drain-source voltage V_{DS} for different substrate terminations.

Compared to the conventional separate B=S termination, which is considered as a reference in the following (black lines), the floating substrate terminations have a reduced output capacitance. A drain-connected substrate termination increased the output capacitance compared to the reference. Comparing the high-side and low-side device for the floating substrate terminations, the high-side devices shows a slightly lower output compared to the high-side device. This is explained by the common substrate, which causes a lower substrate-to-source voltage in the low-side device due to the linkage of

the substrate voltage and the switch-node or dc-link voltage (see Sec. 2.5.2). The common fixed-to-GND substrate termination shows an untypical drain-source voltage dependence for the high side device, where the capacitance does not increase for drain-source voltages towards zero. This is because the channel of the high-side device with a fixed-to-GND substrate termination at an high operation voltage (here 200 V) is already significantly depleted by the high negative high-side substrate-to-source voltage of down to -200 V (see Sec. 2.5.1). The low capacitance seems beneficial to reduce switching loss and times. But the cause for this effect, the negative back-gating of the high-side device, also results in excessive on-resistance reduction and thus is not efficient in dc-dc converter operation as will be shown later.

The sum of the high-side and low-side output capacitances is calculated using the previously derived equations, and shown as the effective switch-node capacitance C_{SW} in Fig. 2.20. Since especially the fixed substrate terminations highly asymmetrically influence the low-side and high-side output capacitances, the switch-node capacitance is a useful quantity to describe the half-bridge with coupled substrates as a condensed characteristic. Fig. 2.20 clearly shows a large variation between the different substrate terminations compared to the reference (B=S). It is observed that the floating substrate terminations systematically reduce the switch-node capacitance, whereas the fixed terminations and terminations with a drain-connected substrate increase the switch-node capacitance.

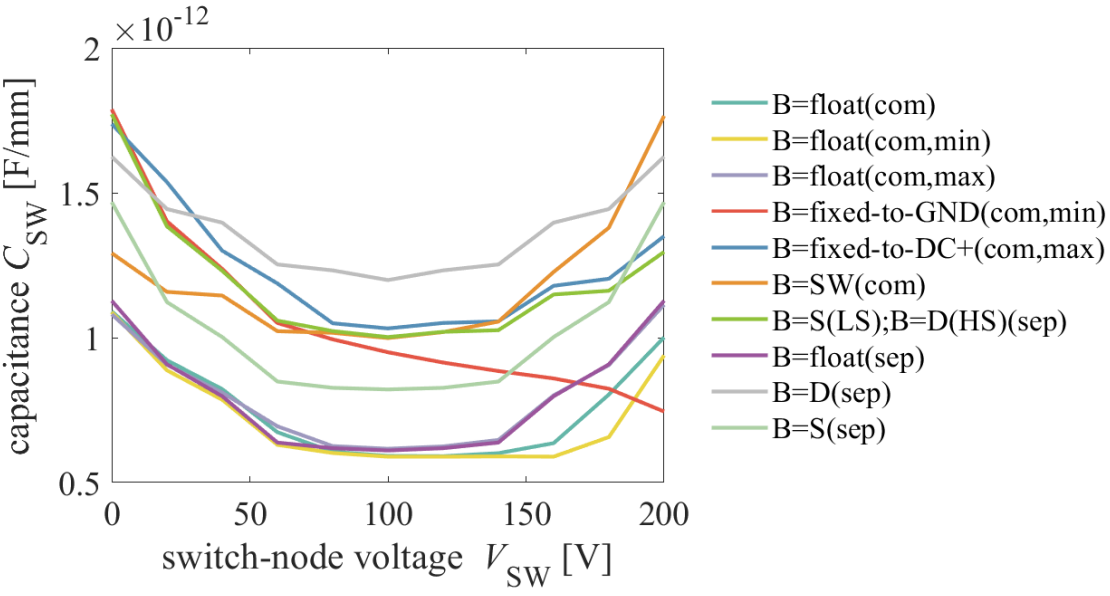

Figure 2.20: Switch-node capacitance C_{SW} of the half-bridge as a function of switch-node voltage for differens substrate terminations.

The switch-node voltage dependent switch-node capacitance $C_{SW}(V_{SW})$ is further condensed into the average switch-node capacitance C_{SW} and shown in Fig. 2.21. In addition to C_{SW}, the contributions from the high-side and low-side devices $C_{OSS,LS}$ and $C_{OSS,HS}$ are also shown to visualize the asymmetries. The bar plot is annotated by the relative increase compared to the reference B=S termination. The plot summarizes that the investigated floating substrate terminations reduce the switch-node capacitance at least

by -20%, whereas fixed and other terminations increase the switch-node capacitance up to +33%.

In Sec. 2.6.1 it was analyzed that cross-coupling through the floating substrate can cause an effective integrated dc-link capacitance C_{DC}. This quantity is also shown in Fig. 2.21. Compared to the output capacitances C_{OSS}, the integrated dc-link capacitance C_{DC} is small. This means that C_{DC} will provide a small fraction of charge during switching transitions, but is not sufficient to replace external dc link capacitors.

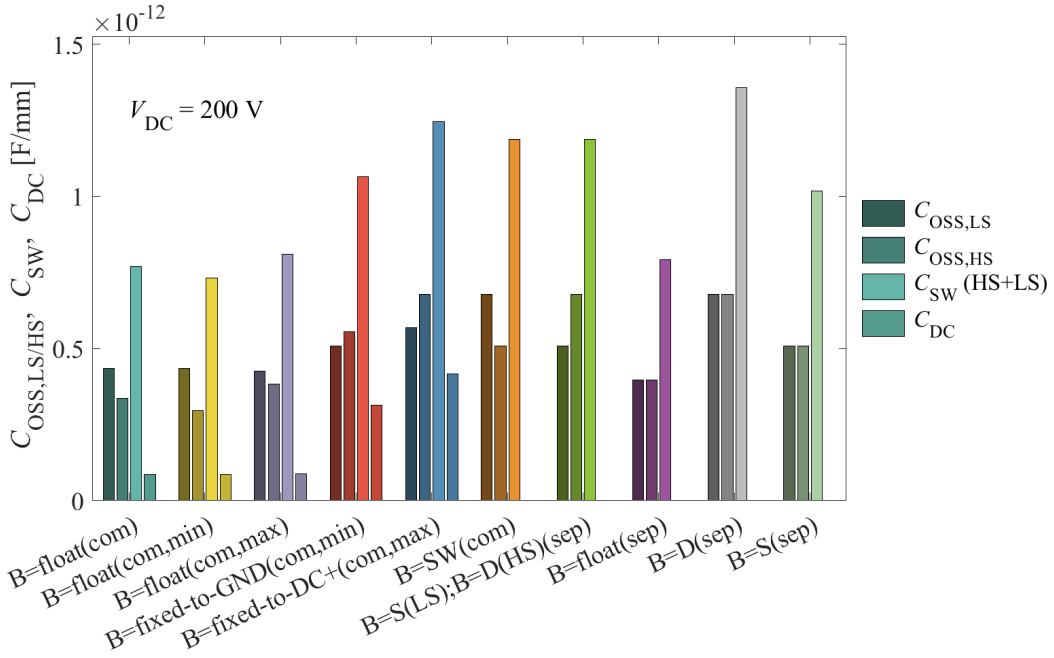

Figure 2.21: Effective output capacitance C_{OSS}, switch-node capacitance C_{SW} and integrated dc-link capacitance C_{DC}.

2.7.2 Switching Energies E_{OSS} and E_{QOSS}

The switching energies and losses are directly related to the effective output capacitances. In hard-switching applications the switching loss depends on which device in a half-bridge is switching. Since there are substrate terminations with asymmetric high-side and low-side output capacitances, also the energy dissipated in the actively switched transistor will be asymmetric. The energy dissipated in the low-side (or high-side) transistor is calculated. The dissipated energy in the low-side (or high-side) results from contributions of both the low-side and high-side devices. The sum $E_{\mathrm{OSS}} + E_{\mathrm{QOSS}}$ of switching energies for all substrate terminations is shown in Fig. 2.22.

2.7.3 Switching Charges Q_{OSS} and Q_{SW}

As a last output-related quantity, the contributions of the high-side and low-side devices to the switch-node charge $Q_{\mathrm{SW}} = Q_{\mathrm{OSS,LS}} + Q_{\mathrm{OSS,HS}}$ are calculated and shown in Fig. 2.23. The switching charge is directly related to the switching time in a resonant switching converter, where an inductor as a current source causes a resonant switch-node

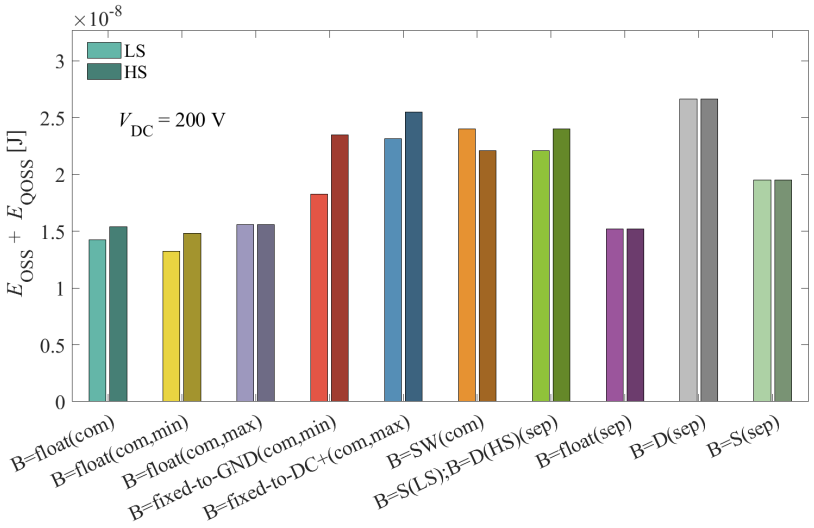

Figure 2.22: Switching energies, including the dissipated energies of the high-side and low-side capacitances of hard-switching turn-on transitions initiated by the low-side (LS) or high-side (LS) transistor.

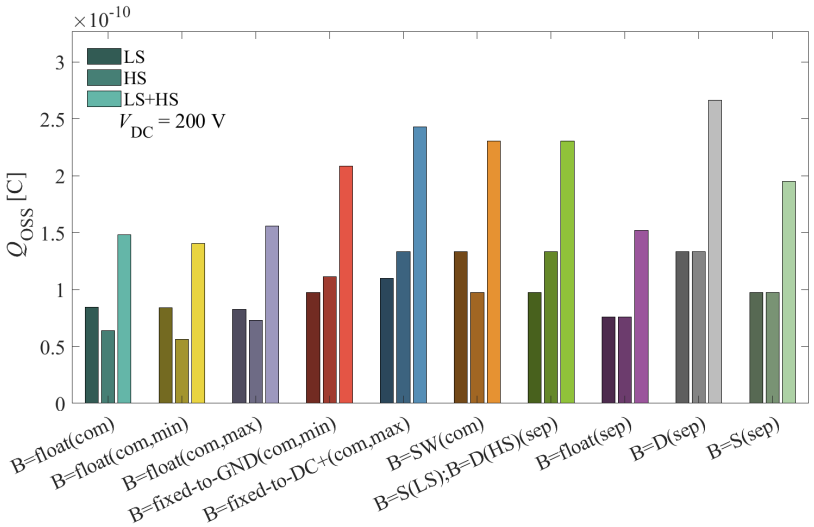

Figure 2.23: Output capacitance charge Q_{OSS} of the high-side and low-side devices for different substrate terminations.

voltage transition by charging the switch-node. As for the switching energies, the floating substrate terminations show more than -20% reduction of switching charge, whereas the fixed and other terminations increase the switching charge up to +37%.

2.7.4 Feedback-Related Effective Capacitances C_{RSS}, C_{XSS}

The reverse-capacitance C_{RSS} (also known as Miller-capacitance) is calculated and shown in Fig. 2.24 for both the high-side and low-side device in a half-bridge. The voltage-dependent $C_{RSS}(V_{DS})$ is further condensed into the average C_{RSS} at an operation voltage of 200 V and shown in Fig. 2.25. The reference B=S substrate termination shows the lowest reverse capacitance of all investigated substrate terminations. For the floating

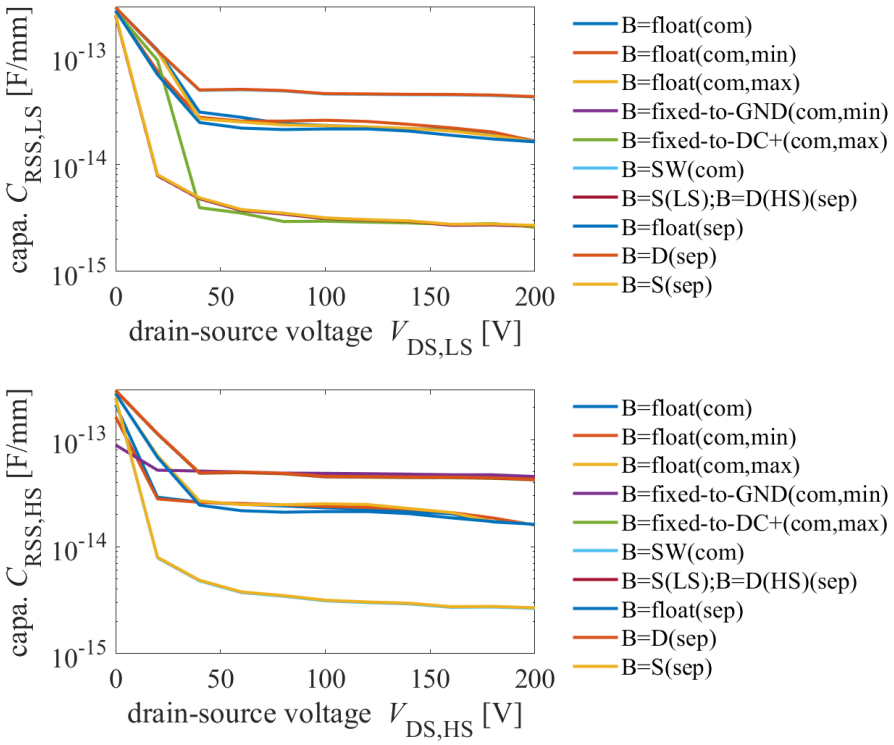

Figure 2.24: Reverse capacitance C_{RSS} as a function of drain-source voltage for different substrate terminations.

substrate terminations the increase is moderate (between +42% and +121%), whereas for the drain-connected termination the increase is as high as +190%. For the fixed terminations, the high-side and low-side increase is highly asymmetrical. The gate-to-gate cross-coupling capacitance C_{XSS} for half-bridges on a common floating substrate, which was derived in Sec. 2.6.1, is also shown in Fig. 2.25. This direct cross-coupling C_{XSS} between the gates through the substrate is negligibly small compared to C_{RSS}, and thus not exploited further.

2.7.5 Input-Related Effective Capacitances C_{ISS}, C_{RSS}, C_{XSS}

The effective input-capacitances for the low-side and high-side devices are calculated and shown in Fig. 2.26. The voltage dependent $C_{ISS}(V_{DS})$ is further condensed into the average C_{ISS} and shown in Fig. 2.27. The effect of the substrate termination on C_{ISS} is negligible. This is explained because the geometry between the source-connected field plates and the gate as a plate-like capacitor dominates C_{ISS} and channel related capacitances which are influenced by the substrate do not significantly contribute to C_{ISS}.

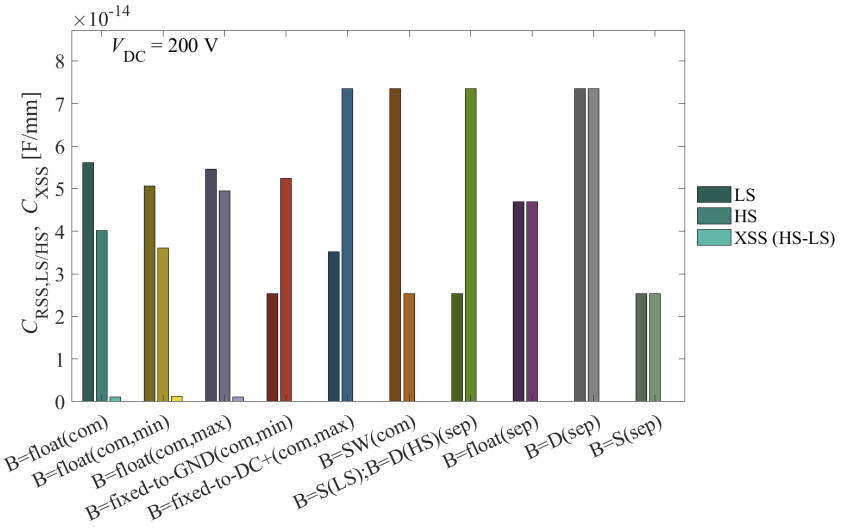

Figure 2.25: Reverse capacitance C_{RSS} and gate-to-gate cross-coupling capacitance C_{XSS} for different substrate terminations.

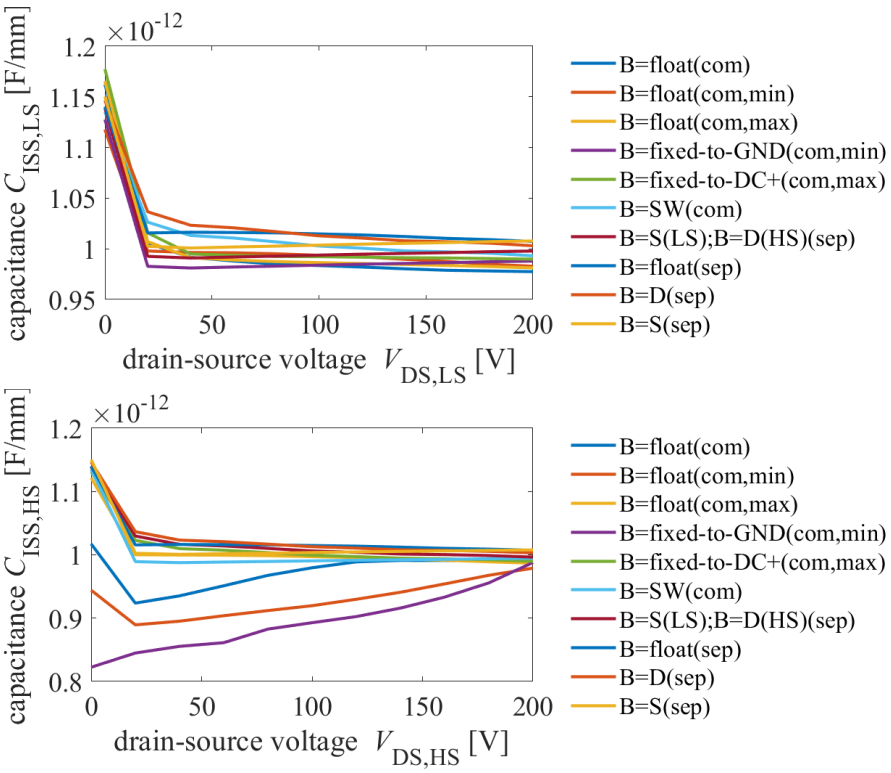

Figure 2.26: Input capacitance C_{ISS} as a function of drain-source voltage V_{DS} for different substrate terminations.

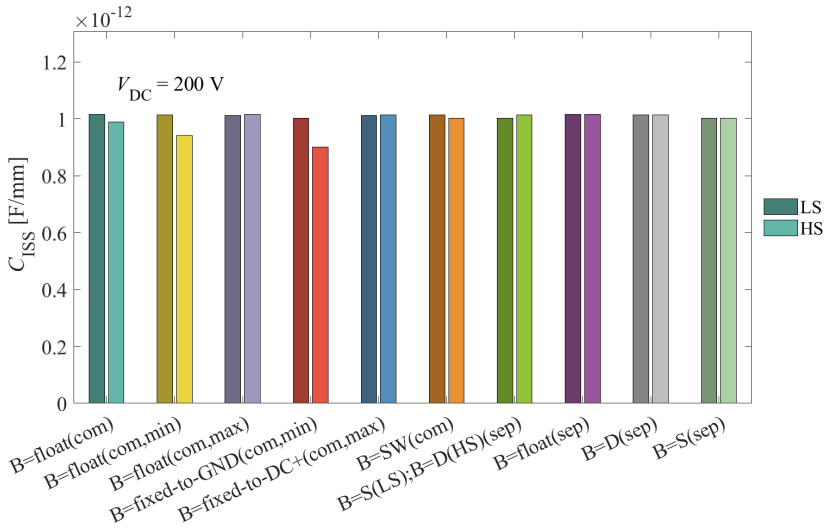

Figure 2.27: Effective input capacitance C_{ISS} for different substrate terminations.

2.8 Experimental Switching Characteristics for Different Substrate Terminations

This section now presents an experimental study on switching characteristics for different substrate terminations to verify the previously derived theoretical and simulated or calculated results. For this purpose, a discrete half-bridge power module using two GaN power ICs is built, where both ICs have separate substrate pads which are initially floating.

2.8.1 Experimental Setup for Substrate Termination Variation

Fig. 2.28 shows the power module and the schematic with the two separately accessible substrate terminals with variable external substrate terminations. This setup allows

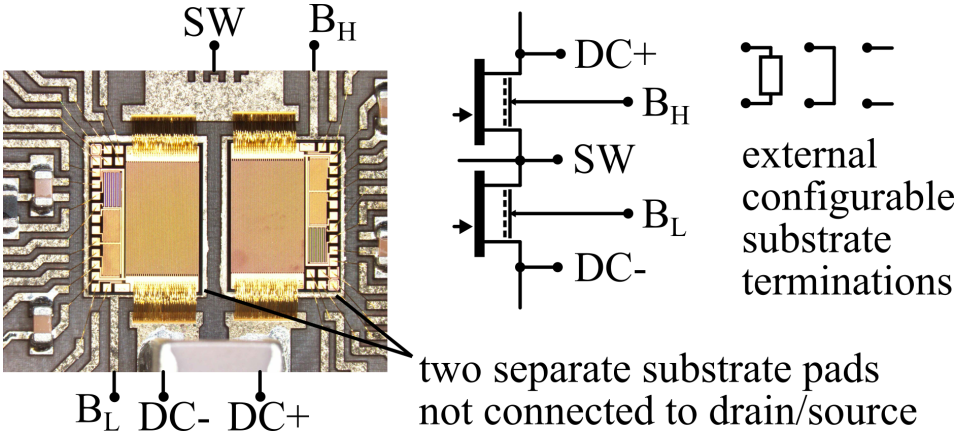

Figure 2.28: Discrete half-bridge module with two separately accessible substrate pads to realize a variety of substrate terminations by an external configurable substrate termination network.

connection of the high-side and low-side substrates to any other circuit node. Only one power module with exactly the same ICs are used for all measurements, to avoid part-to-part variations to influence the results. All investigated substrate terminations are realized by external termination of the substrate to the respective other circuit nodes. For the floating terminations, the resistors of the substrate biasing network have values of 330 kΩ. For fixed terminations, instead of an external short circuit, the terminations are realized by 5 Ω resistors. This measure was taken to reduce oscillations which result from the increased parasitic loop inductance formed by the external substrate termination. Substrate-loop instabilities and countermeasures will be discussed in detail in Chapter 3.

The half-bridge is operated in a dc-dc converter prototype with a power inductor (620 µH) in buck-configuration. The switching frequency is 100 kHz, the duty-cycle is 50% and symmetrical dead-times of 40 ns are used (if not otherwise denoted). The input of the converter is connected to a voltage source and the output to a electronic dc-load which is operated in constant current mode with adjustable output current. The power loss of the converter is measured with a power analyzer by measuring both the real dc input and output power. The measured power loss includes all power-stage losses and thus also the inductor core and winding loss. For floating substrate terminations where

external highly-resistive resistors are used in the external substrate biasing networks, the loss caused by these external resistors is calculated (typically around 0.1 W at 200 V) and is already subtracted from the power loss data presented in the following.

2.8.2 Switching Energies E_{SW}

The converter was operated without an inductor. In this operation both the high-side and low-side transistors initiate hard-switching switch-node voltage transitions. The power loss was measured at multiple frequencies f_i (100 kHz - 500 kHz, step: 100 kHz), and from the increase of power loss with frequency the switching loss energy per hard-switching voltage transition extracted as

$$E_{SW} = \frac{P_{LOSS}(f_i) - P_{LOSS}(f_j)}{2(f_i - f_i)}. \tag{2.60}$$

Since more than two frequencies were measured, E_{SW} was extracted by linear regression. Appendix A.2 shows the raw data and fitted function of the linear regression. The factor of two is because in the operation mode without inductor the high-side and low-side transistor cause a total of two switching transitions with switching loss in each switching period. Fig. 2.29 shows the switching energies at 200 V for all measured substrate terminations. The measured switching loss for the floating substrate terminations is reduced between -21% and -25% compared to the reference termination (B=S). This is in good agreement with the theoretically calculated reduction of between -20% and -28% shown in Fig. 2.21 and Fig. 2.22.

For the fixed terminations, the measured switching loss changed only by between −4.4% and +4.2%. The theoretically calculated increase from Fig. 2.21 and Fig. 2.22 was however between +5% and +33%. The discrepancy is explained by the difference between the experimentally used power IC and the device used for the calculation: While the theoretical calculation was based on a test structure of a discrete transistor, the experiment uses a power IC with integrates further functionality on further chip area. For example, the experiment uses a monolithic integrated gate driver final stage. This driver circuit is connected to the gate and source (through the gate driver supply capacitors) of the main power transistors, and thus does contribute additional substrate capacitance. As a result, the gate-to-substrate and source-to-substrate capacitance are higher than the data used for the theoretical analysis. As a consequence of this result, the difference between a B=S and B=D substrate termination (as used in the fixed terminations) is less significant. Despite the discrepancy it still is observed that only the floating substrate terminations allow a significant reduction of switching loss, whereas the fixed terminations have either similar or slightly increased switching loss compared to the reference termination.

It should be noted that this experiment was conducted without a power inductor. Thus, the measured switching loss does not include a load current dependence. In switched-mode converters there will be additional power loss during the switching time with overlap of voltage and current during hard switching transitions. Since this additional overlap loss is dependent on the switching time, and the switching time is dependent on the

reverse capacitance, in the following further measurements will be conducted to quantify the effect of substrate termination on switching times.

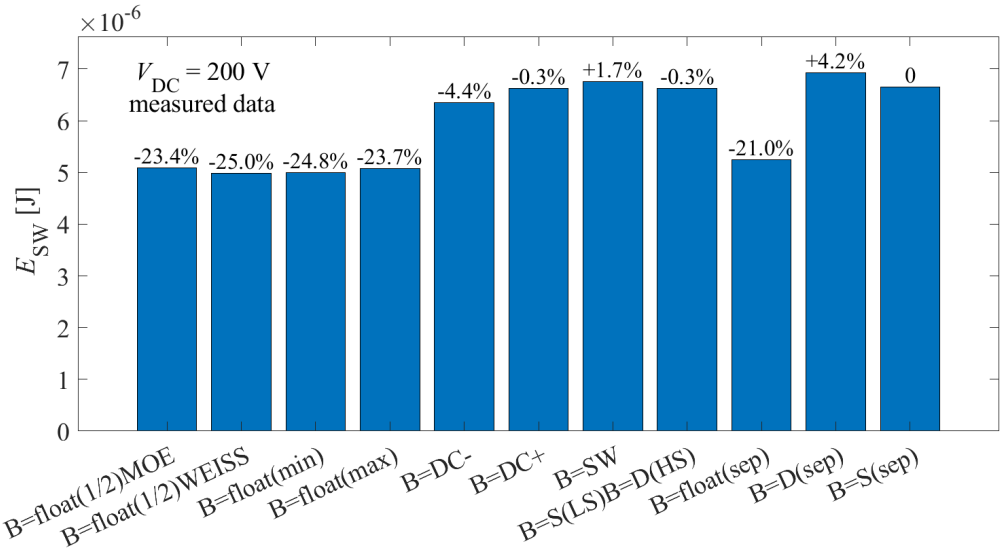

Figure 2.29: Measured switching energies for different substrate terminations.

2.8.3 Switch-Node Charge Q_{SW}

While the switching loss from the stored energy in the switch node is relevant for hard switching conditions, it is also possible to operate half-bridge converters only with resonant transitions and zero-voltage-switching. For this soft-switching operation, the effective switch node charge is the relevant quantity. To achieve fast voltage transition times, a lower switch-node charge will enable higher operation frequencies of soft switching converters. To quantify the switch-node charge, the following extraction method is used: The half-bridge is operated at 100 kHz and a load current of 2.5 A. In this continuous-conduction-mode operation there exist a hard-switching transition (rising switch-node voltage transition at an inductor current of 2.37 A) and a resonant transition (falling switch-node voltage transition at an inductor current of 2.76 A). The dead time of 40 ns is higher than the resonant voltage transition which avoid partial hard-switching and ensures a full resonant transition. The resonant 10/90% falltime $t_{SW,F,10-90}$ of the switch-node voltage is measured, and based on the known and measured inductor current $I_{L,F}$ which causes the resonant transition, the required charge for a full (0-100%) voltage transition is extracted as

$$Q_{SW} = I_{L,F} \frac{t_{SW,F,10-90}}{0.8}. \tag{2.61}$$

Fig. 2.30 shows the switch-node charge extracted from the resonant switching transitions. Similar to the switching energies, the floating substrate terminations significantly reduced the charge by around -30%. The fixed terminations show an increase of up to +16%. It is concluded that the floating substrate terminations allow faster resonant switching transitions for the same inductor current.

The measurement data for the fixed-to-GND termination is missing, because for this substrate termination only the measurements without inductor were possible up to 200 V. Due to the extreme back-gating and related on-resistance increase for this particular substrate termination, the operation with inductor and non-zero inductor current led to device destruction.

All other measurement results are in good agreement with the calculated results from Fig. 2.21.

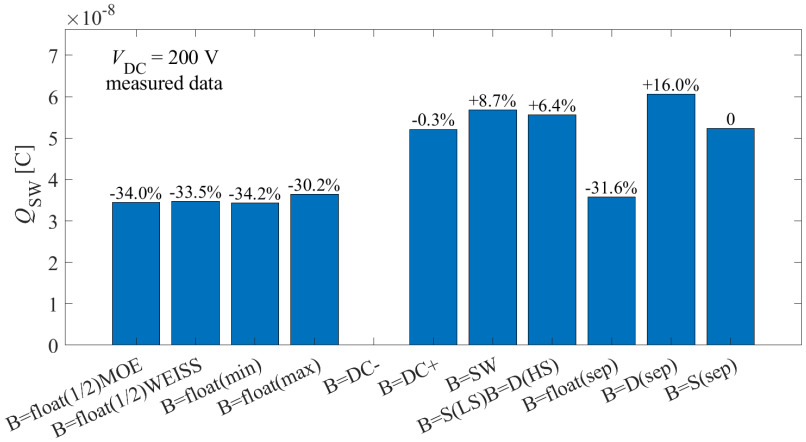

Figure 2.30: Measured switch-node charge for different substrate terminations.

2.8.4 Reverse Feedback-Related Quantities

To verify the theoretically derived significant increase of reverse capacitance C_{RSS} for all terminations other than the reference B=S termination, an experiment is conducted. C_{RSS} defines the duration of the "Miller"-plateau in hard-switching operation and thus also the duration of a hard-switching voltage transition. In contrary, for a zero-voltage switching transition C_{RSS} is not relevant because the drain voltage is already close to the source voltage. The duration of the Miller plateau is experimentally measured by comparing the gate-source voltage risetime of a zero-voltage switching and a hard-switching transition (at 200 V). Fig. 2.31 shows the measured gate-source voltage transition times.

The converter was only characterized for positive load current, and not operated as a bi-directional dc-dc converter. Therefore, by adjusting the load current only the low-side device operates both under hard-switching and resonant conditions, whereas the high-side device is always (partial)-hard-switching. For this reason, the comparison between ZVS and hard-switching is only shown for the low-side device in Fig. 2.31. The gate-source risetime under ZVS conditions is equally fast for all substrate terminations. Here, mainly the input capacitance C_{ISS} defines the gate-source risetime. In Sec. 2.7.5 it was shown that C_{ISS} is insignificantly influenced by the substrate termination. Due to the "Miller"-effect, the hard-switching gate-source risetimes are increased for all substrate terminations other than B=S. While for the floating substrate terminations the increase is moderate and almost symmetrical (between HS and LS), the fixed substrate terminations show highly asymmetric increase of the gate-source risetime. This measurement verifies

the likewise highly asymmetrical increase of C_{RSS} depending on the substrate termination which was derived in Sec. 2.7.4.

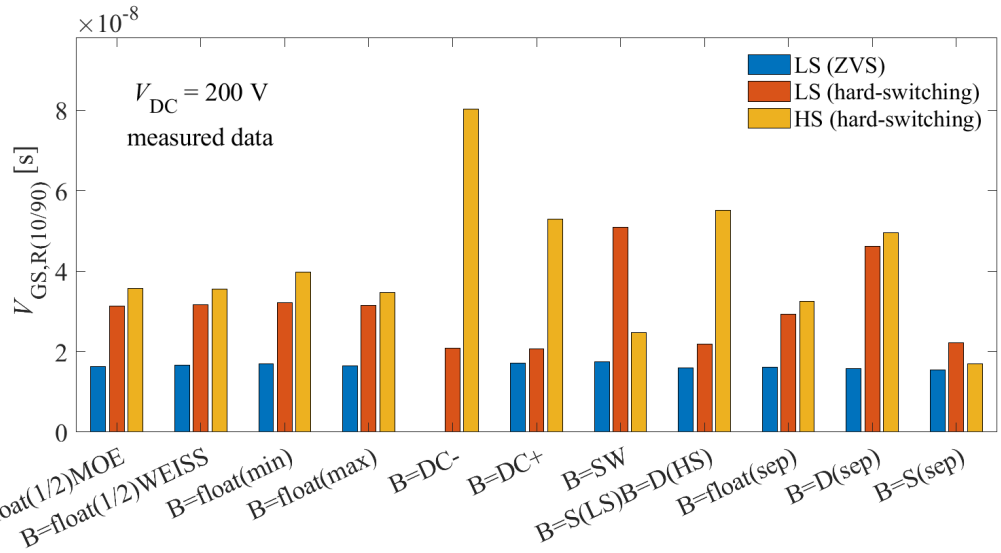

Figure 2.31: Measured gate-sourse risetime during hard-switching turn-on transitions and ZVS turn-on transitions of the high-side and low-side transistor for different substrate terminations.

Fig. 2.32 shows the gate-source voltage waveforms of the low-side transistor during the hard-switching turn-on transitions. Three characteristic durations of the "Miller"-plateau are marked: The source-connected terminations (marked "S") have the fastest, the drain-connected (marked "D") the slowest, and the floating terminations (marked "f") in between transition times. This is explained by the already discussed increase of C_{RSS} depending on the substrate termination. The initial part of the gate voltage from the off-state to the threshold voltage (-7.5 V to -2.5 V) is equally fast for all substrate terminations. This is explained by the almost constant C_{ISS} for all substrate terminations.

The measured data is in good agreement with the calculated data from Fig. 2.25, except for the B=DC-(both) termination, where the measured risetime is significantly lower than the calculated one. This is explained, because in the measurement the risetime is also influenced by the static back-gating from the negative substrate-to-source voltage of the high-side device during switching. The partly depleted channel results in less current and thus slower switching. The discrepancy is expected, because the theoretical analysis assumes avoidance of static back-gating (as achieved the proposed substrate biasing network in this work). As was stated in Sec. 2.3, avoidance of static back-gating is a necessary precondition for efficient switching operation. While the capacitance transformation method assumes that this precondition is met, in the experiment this is not the case.

2.8.5 Resistance Increase for Different Substrate Terminations

So far, only switching characteristics have been experimentally investigated. In this chapter the effect of substrate termination on the conduction characteristic is measured using a phenomenological approach. The half-bridge converter was operated at a fixed switching frequency of 100 kHz at a fixed input voltage of 200 V and fixed duty-cycle of 50%.

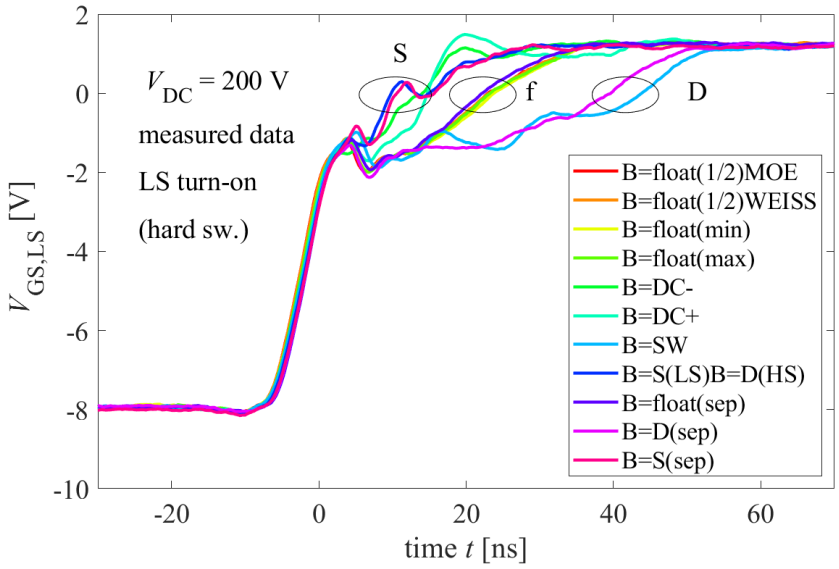

Figure 2.32: Measured gate-source voltage waveforms of the low-side transistor during hard-switching turn-on transitions for different substrate terminations.

The load current was varied for each substrate termination between 0 A and 2.5 A in steps of 0.5 A. The effective inductor current I_{RMS} and the total power loss P_{LOSS} of the converter for each load current and substrate termination is measured. As a first principle analysis, it is assumed that the conduction loss increases quadratically with the current. The measured power loss was thus fitted by quadratic regression. Appendix A.2 shows the raw data and fitted function of the quadratic regression. From the fitted coefficients, the quadratic coefficient gives a phenomenological resistance value R_{RMS}. This value includes the transistor on-resistance and also the inductor series resistance. Furthermore switching loss which increases with load current is also partially included in R_{RMS}. Nevertheless, R_{RMS} still is a single condensed quantity which allows comparison of the conduction behavior. Fig. 2.33 shows the extracted R_{RMS} for all substrate terminations.

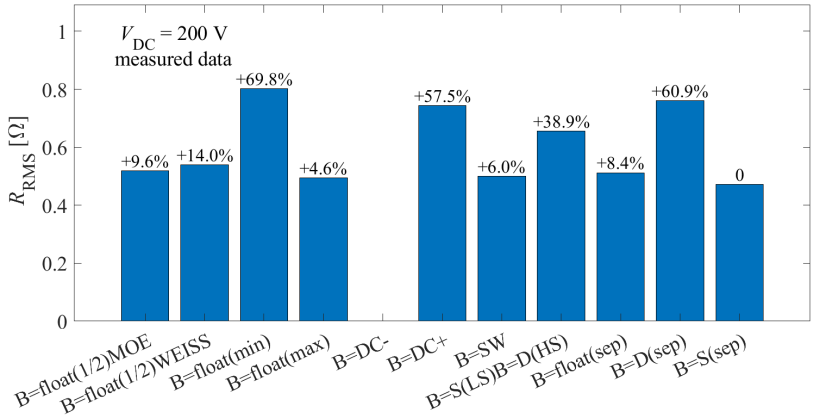

Figure 2.33: Extracted resistance from a polynomial fit of the measured load current dependent power loss for different substrate terminations.

All substrate terminations show an increased resistance R_{RMS} compared to the B=S termination. The common floating termination with the lowest offset voltage B=float(min) shows the highest resistance increase. This is explained, because this termination operates the high-side transistor with the most negative back-gating voltage during the high-side conduction phase. This verifies the analysis in Sec. 2.5.5 (see Fig. 2.11). The common floating termination with the highest offset voltage B=float(max) shows the lowest resistance increase. This is again as theoretically derived, because the particular substrate biasing network (Fig. 2.9c) shifts the substrate voltage in such a way that the negative back-gating of the high-side transistor during the conduction phase is avoided (see also Fig. 2.11). The common floating termination with intermediate offset voltages B=float(1/2) shows a resistance between the two already discussed boundary cases.

Compared to the conventional discrete half-bridge with separate B=S termination, the operation scheme proposed by this work shows the lowest measured on-resistance of only +4.6% increase of all investigated alternative substrate terminations.

2.8.6 Dc-Dc Converter Efficiency for Different Substrate Terminations

Previously, static and dynamic switching and conduction characteristics have been separately experimentally investigated. For actual power converter applications, however, the effects of the individual characteristics are combined. The efficiency η of an application-oriented dc-dc converter is a single quantity which allows a high-level comparison of the performance. Fig. 2.34 shows the measured dc-dc converter efficiency for all investigated substrate terminations in a load current range between 0.5 A and 2.5 A. The duty-cycle is 50% in all measurements. While the conventional separate B=S termination has a maximum efficiency of 98.59% at 2 A, all alternative substrate terminations show the maximum efficiency at a lower load current of 1.5 A. This shift of the maximum efficiency to lower currents is explained by the increase of effective resistance R_{RMS} for all alternative substrate terminations (see Fig. 2.33). Comparing the absolute maximum measured

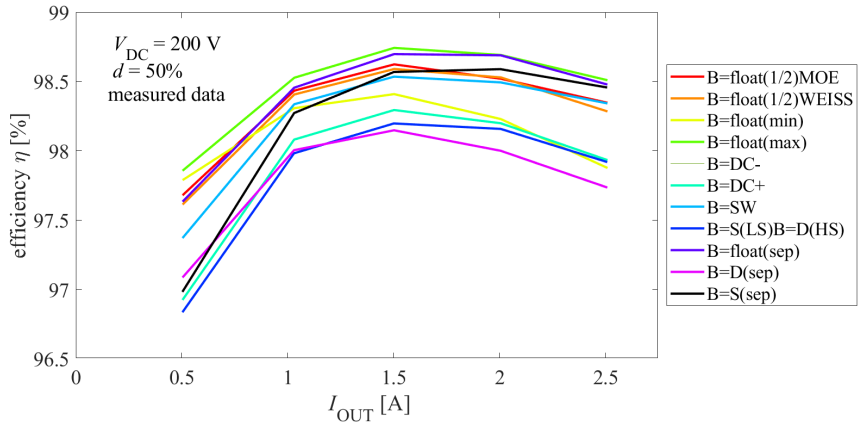

Figure 2.34: Measured dc-dc conversion efficiency η at 50% duty-cycle, 200 V input voltage, 100 kHz switching frequency for different substrate terminations.

efficiencies shows that there exist substrate terminations other than the conventional B=S(sep) with a higher efficiency than the maximum of the B=S(sep) termination. The common floating termination with the highest offset voltage B=float(max) shows the highest efficiency over the whole measured current range. The maximum efficiency is 98.74% at a load current of 1.5 A. The floating-substrate termination network proposed by this work thus enabled a 10% power loss reduction at the maximum efficiency compared to the conventional half-bridge circuit.

2.8.7 Duty-Cycle Dependent Power Loss

For the purpose of a comparison so far only a duty-cycle of 50% was considered. In many real applications however, a wide range of duty-cycles are required during operation. For example, in a power-factor-correction (PFC) circuit the instantaneous input/output varies between 0% and up to almost 100%. For these applications high efficiency is required under all duty-cycle conditions. At a load current of 2.5 A, input voltage of 200 V and 100 kHz switching frequency, the duty-cycle was varied in a wide range between 5% and 95%. Fig. 2.35 shows the measured power loss as a function of duty-cycle for all substrate terminations. The typical signature of a conventional half-bridge with two identical but separate half-bridge transistors is as measured for the B=S(sep) termination, where the power loss is highest at 50% (worst-case) and slightly reduces towards duty-cycles of 0% or 100%. The novel substrate biasing network for a common floating substrate allows to shift the substrate towards positive values to avoids back-gating during high-side conduction (see Fig. 2.9). The effectiveness of these networks is verified by the measurement of the duty-cycle dependent power loss. While the previous state-of-the-art substrate biasing network is duty-cycle dependent (B=float(1/2)WEISS) and thus shows a high increase of power loss at low duty-cycles, the proposed biasing network generates duty-cycle independent substrate voltages, which maintain the same back-gating voltages for all duty-cycles during operation. In Fig. 2.35 it is visible, that the new biasing network (B=float(1/2)MOE) for the floating substrate has the highest power loss at 50% an reduced power loss towards 0% and 100%, whereas the previously known biasing network (B=float(1/2)WEISS) has a similar power loss only at 50% duty-cycle, but shows a severe increase of power loss at low duty-cycle. Furthermore, dimensioning of the proposed biasing network allows to shift the average substrate voltage towards the desired positive values to avoid back-gating. By this measure, the proposed B=float(max) biasing avoids negative back-gating independent from the duty-cycle and shows the lowest power loss.

2.8.8 Verification of Duty-Cycle Independent Substrate Biasing Network

The duty-cycle independence of the proposed semi-floating substrate termination network is further analyzed and compared to a conventional and previously known biasing network. For the same operation points where the efficiency and power loss was already shown as a function of duty-cycle (Fig. 2.35), the transient switching waveforms are investigated. In addition to the switch-node voltage $V_{SW}(t)$, the common substrate voltage $V_B(t)$

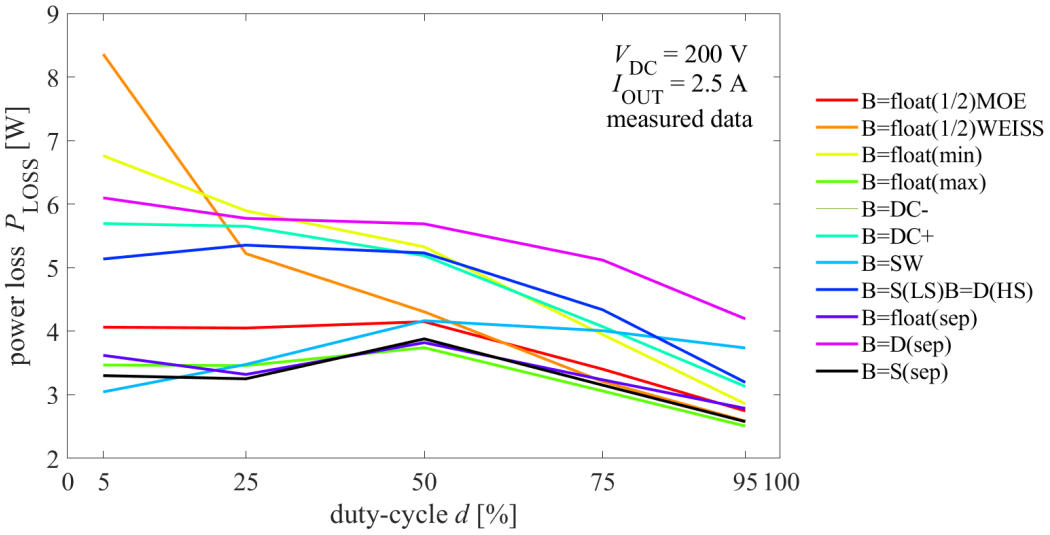

Figure 2.35: Measured power loss as a function of duty-cycle at an output load current of 2.5 A, an input voltage of 200 V and for different substrate terminations.

was also measured. Due to the half-bridge working principle, the switch-node voltage has duty-cycle independent state-levels (here 0 V and 200 V). The state-levels of the substrate-voltage V_B, however, depend on the substrate biasing network.

Conventional biasing network (B=float(1/2)WEISS): Fig. 2.36 shows the switching waveforms for the state-of-the-art biasing network (B=float(1/2)WEISS) for a wide range of duty-cycles d. This biasing network together with the substrate capacitances is a RC circuit, and with an equivalent circuit analysis the highly-resistive voltage divider in combination with the substrate capacitances shows a transient behavior which exponentially and asymptotically approaches $\frac{1}{2}V_{DC}$. The exponential behavior is shown in Fig. 2.37 exemplarily for a duty-cycle of 25%. From the biasing network, the average $V_B(t)$ over a switching period follows this constant final value $\frac{1}{2}V_{DC}$. Since the time-averaged $V_B(t)$ depends on the duty-cycle, the state-levels of V_B also depend on the duty-cycle. For all duty-cycles, the substrate-to-source voltage during the high-side conduction phase $V_{BS,HS,ON}$ is marked with an arrow in Fig. 2.36. As also discussed in [79], $V_{BS,HS,ON}$ depends on the duty-cycle. While for $d \to 0\%$, a very high negative back-gating voltage $V_{BS,HS,ON} \approx -\frac{1}{2}V_{DC}$ increases the on-state resistance, only for $d \to 100\%$ the back-gating is avoided by $V_{BS,HS,ON} \approx 0\,V$. The duty-cycle dependent back-gating and related on-resistance increase is also the cause for the already presented efficiency reduction in Fig. 2.35.

Proposed biasing network (B=float(1/2)MOE): The proposed substrate biasing network allows two improvements, namely a duty-cycle independent substrate voltage and an adjustable substrate offset voltage. The improvement is presented in two steps. Here, first only the duty-cycle independence is shown. Therefore, this work's substrate biasing network was dimensioned as in Fig. 2.9b, such that it has similar substrate state levels as the state-of-the-art biasing network at a duty-cycle of 50%. The voltage waveforms of

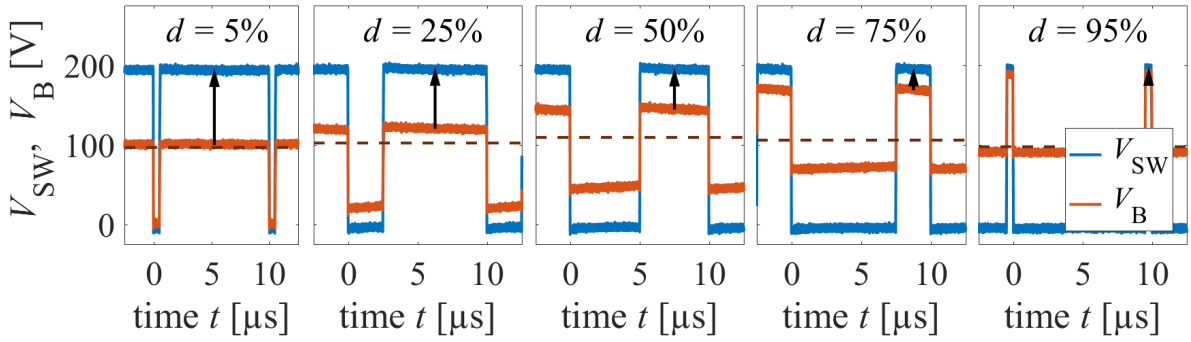

Figure 2.36: Measured transient switch-node and substrate voltages for different duty-cycles. The "B=float(1/2)WEISS" terminations is used.

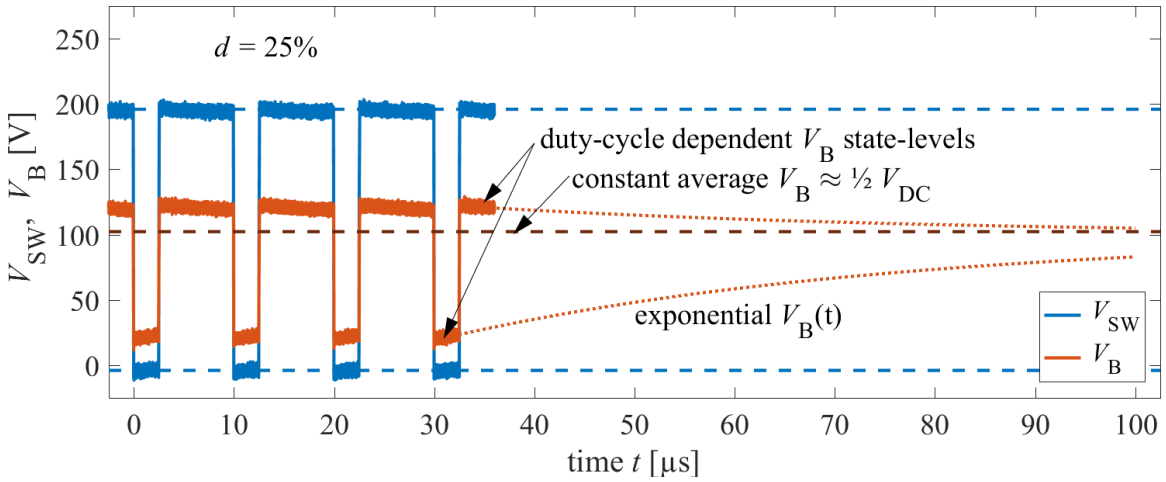

Figure 2.37: Detailed analysis of the measured transient switch-node and substrate voltages for the "B=float(1/2)WEISS" termination.

this configuration (B=float(1/2)MOE) are shown in Fig. 2.38. It is observed, that the state-levels of substrate-voltage now are always around $\frac{3}{4}V_{DC}$ and $\frac{1}{4}V_{DC}$, independent from the duty-cycle. The constant V_B state-levels are also shown in Fig. 2.39. The substrate-to-source voltage of the high-side transistor during the conduction phase is now constant and $V_{BS,HS,ON} \approx -\frac{1}{4}V_{DC}$. Compared to the (B=float(1/2)WEISS) termination with up to $V_{BS,HS,ON} \approx -\frac{1}{2}V_{DC}$ at duty-cycles $d \to 0\%$, this is a reduction by 50%. However, with this configuration the high-side transistor is still significantly negatively back-gated.

This work's biasing network without negative back-gating (B=float(max)MOE): This work's proposed duty-cycle independent substrate biasing network also allows adjustment of the substrate offset voltage. By dimensioning of the biasing network as in Fig. 2.9c (B=float(max)MOE), the average substrate voltage is shifted to higher values compared to the previous discussed case. The switching waveforms for this configuration are shown in Fig. 2.40. With this configuration, negative back-gating of the high-side device is avoided, which is furthermore also the case for all duty-cycles. The zero $V_{BS,HS,ON}$ is marked in Fig. 2.40 by the vanishing arrowheads. A static on-resistance increase of the high-side transistor is avoided by this biasing network in all operation points. This

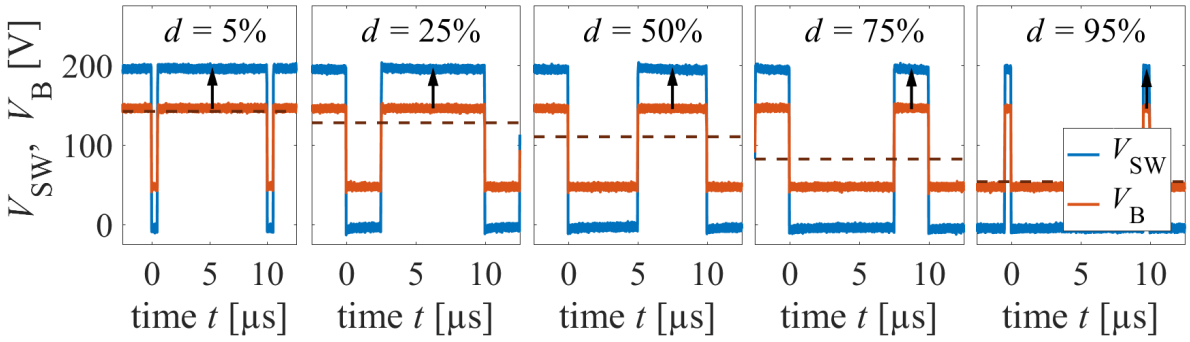

Figure 2.38: Measured transient switch-node and substrate voltages for different duty-cycles. The "B=float(1/2)MOE" terminations is used.

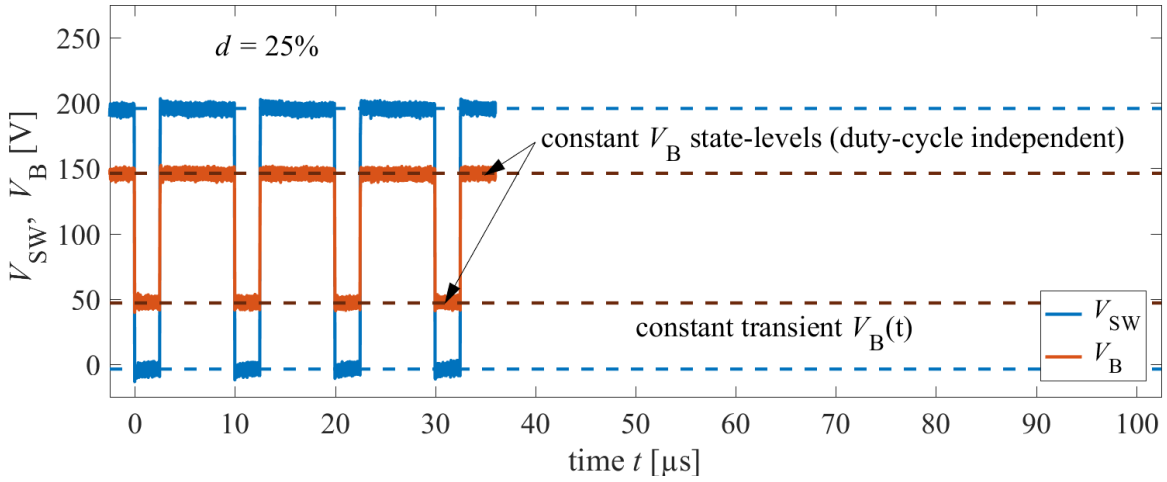

Figure 2.39: Detailed analysis of the measured transient switch-node and substrate voltages for the "B=float(1/2)MOE" terminations.

allows a predictable operation with low power loss and thus high efficiency over the wide range of duty-cycles which is typically required in power converter applications.

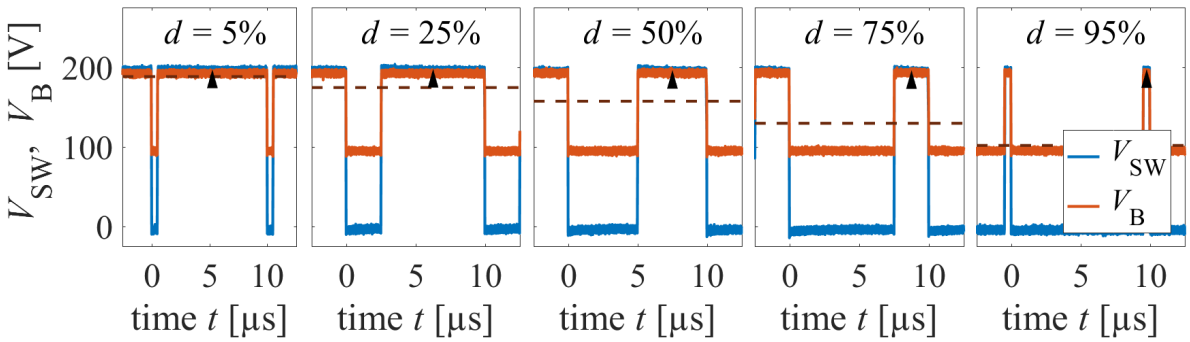

Figure 2.40: Measured transient switch-node and substrate voltages for different duty-cycles. The "B=float(max)MOE" terminations is used. Negative back-gating of the high side device is avoided for all duty-cycles.

2.9 Experimental Monolithic GaN-on-Si Half-Bridge and Driver Operation

The systematic substrate termination study in the previous sections was carried out with a discrete half-bridge, using two ICs on separate substrate pads. Based on the findings of that experimental study, now a monolithic half-bridge with driver is presented and operated with the previously proposed and verified duty-cycle independent substrate biasing network, which also allows to avoid negative back-gating under all operation conditions.

Fig. 2.41 shows the fabricated monolithic GaN-on-Si power IC, which integrates a half-bridge and drivers. The IC is assembled on a ceramic power module. A more detailed description of the layout will be discussed in the next chapter, where also a photo of the power module layout is shown in Fig. 3.24a. This section uses the proposed substrate biasing network B=float(max) from Fig. 2.9c for the operation of the monolithic half-bridge. This biasing network was chosen, because it showed the highest efficiency in the previously presented study.

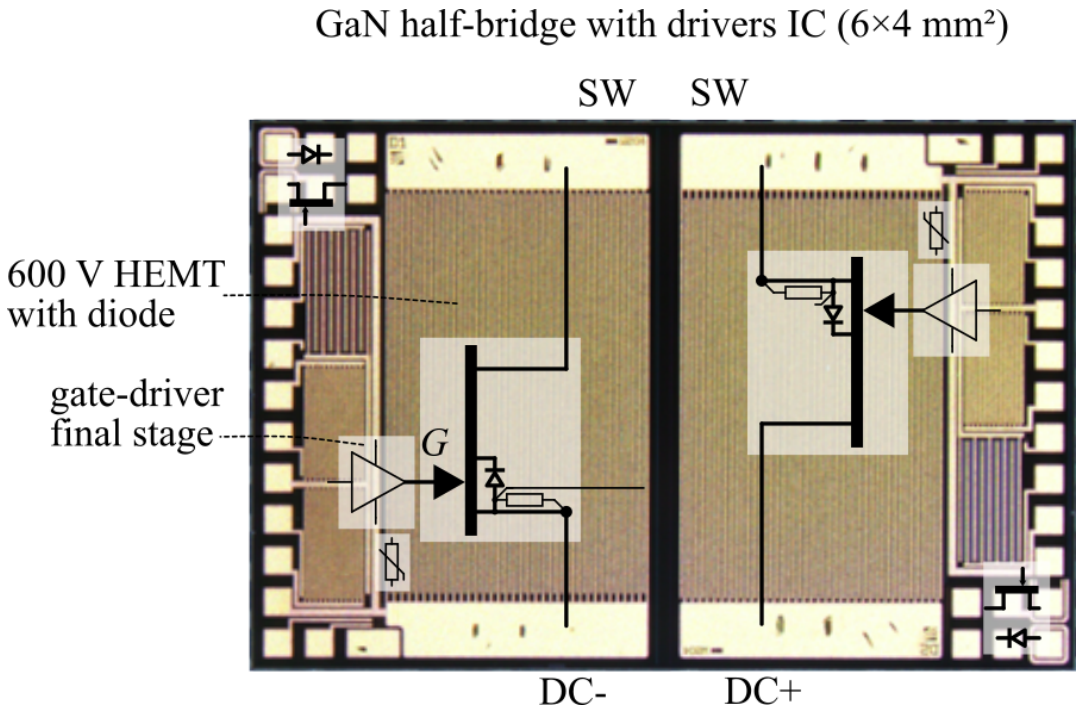

Figure 2.41: Monolithic GaN-on-Si half-bridge with driver IC.

Fig. 2.42 shows the measured dc-dc conversion efficiency and total power loss at a duty-cycle of 50%, and input voltages up to 200 V. The measurement verifies the efficient operation of a monolithic GaN half-bridge with integrated drivers on conductive Si substrate without further vertical isolation measures (such as GaN-on-SOI) at a high voltage of 200 V.

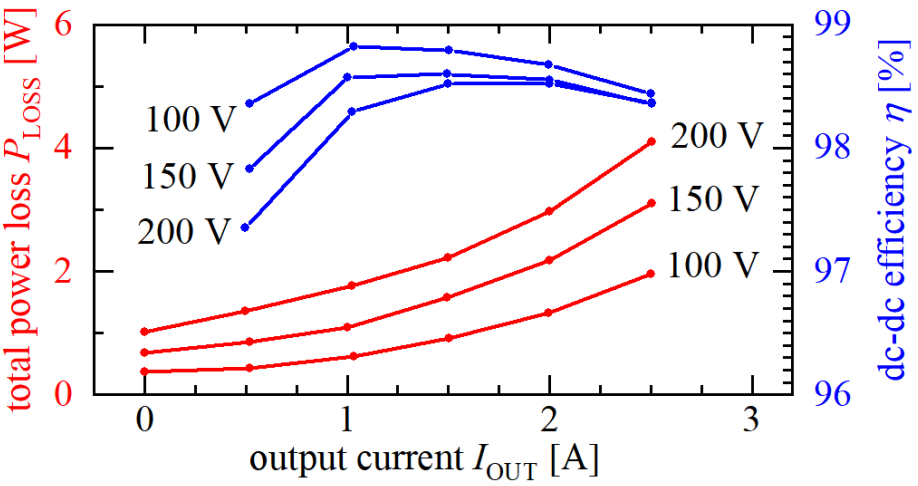

Figure 2.42: Measured dc-dc conversion efficiency of monolithic GaN-on-Si half-bridge with driver IC.

2.10 Summary and Conclusion

To summarize this chapter, first the research questions are restated, then the results are summarized and finally conclusions are drawn.

- How do the substrate capacitances, the substrate potential and different substrate terminations influence the effective capacitances of GaN-on-Si HEMTs and half-bridges?

This work considers the substrate of lateral GaN HEMTs as a fourth terminal in addition to the gate, drain and source. The four-terminal description allows separation of the substrate capacitances C_{BS}, C_{BG}, C_{BD} from the other capacitances C_{GS}, C_{GD}, C_{DS}, and thereby evaluation of effective half-bridge capacitances such as $C_{ISS}, C_{OSS}, C_{RSS}$ for a variety of substrate terminations.

Measured capacitances show a dependence on both the drain-to-source and the substrate-to-source voltage $C(V_{DS}, V_{BS})$. The substrate-voltages are formulated and calculated for all investigated substrate terminations as a function of the drain-source or switch-node voltages ($V_{BS} = V_{BS}(V_{DS})$ or $V_{BS} = V_{BS}(V_{SW})$). This methods allows to substitute $C(V_{SW}, V_{BS}(V_{SW}))$ and thus eliminate the substrate voltage dependence from the capacitance description.

To analyze the substrate-related half-bridge capacitances, an equivalent circuit transformation method was proposed and carried out: A start-to-mesh capacitance transformation is applied to the substrate capacitances of half-bridges. Together with the previously described formulation of the substrate potentials as a function of switch-node voltage $V_{BS}(V_{SW})$, the full half-bridge capacitance network is represented by equivalent half-bridge capacitances similar to discrete half-bridges. Based on this method the effective half-bridge capacitances are then described and calculated based on measured terminal capacitances. From the capacitance transformation insight into coupling mechanisms in half-bridges is derived: On a floating substrate, a gate-to-gate cross-coupling capacitance C_{XSS} results, which is not the case in discrete half-bridges. However, quantitative evaluation shows that C_{XSS} is negligible compared to C_{RSS} for the investigated

circuits. Thus, the result of this work's capacitance transformation method allows a direct quantitative comparison using effective capacitance values. Furthermore, an unintentionally integrated dc-link capacitance C_{DC} is identified for several substrate terminations of a a monolithic half-bridge, caused by cross-coupling from the low-side source to the high-side drain through the substrate. However, with a floating-substrate C_{DC} is much lower than the switch-node capacitance C_{SW}, and thus alone not sufficient for integrated low-inductive decoupling of the half-bridge power-loop. For monolithic half-bridges with a common substrate which is terminated to either low-side source (DC-) or high-side drain (DC+) of the half-bridge, a higher integrated dc-link capacitance, but still lower than C_{SW} is calculated. Again, this only allows partial decoupling and does not replace the need for external dc-link decoupling capacitors.

Calculation of the effective output capacitance shows that the substrate termination changes C_{OSS} in a wider range from -28% to +33% compared to a conventional discrete half-bridge. Consequently, the calculated switching energies E_{SW} differ for all substrate terminations. From all substrate terminations, the floating substrate terminations show the highest reduction of E_{SW} in a range from -20% to -32% compared to a discrete half-bridge with separate substrate-to-source termination. These reduced capacitances allow reduced switching losses and increased switching speed. However, the expected reduction of switching loss can be jeopardized during actual converter operation by back-gated on-resistance increase.

- How to avoid static back-gating during operation of GaN half-bridges on a common Si substrate?

The common conductive substrate in a monolithic half-bridge not only couples the substrate capacitances, but also links the high-side and low-side substrate voltages to the dc operation voltage. The operation voltage of monolithic GaN-on-Si half-bridges on a common conductive is thereby limited by measured excessive vertical substrate leakage currents at positive substrate bias, and on-resistance increase at negative back-gated substrate. For the used GaN technology a single device can operate up to 600 V, however, for monolithic half-bridges the operation voltage is reduced.

Nevertheless, for the reduced operation voltage a variety of substrate terminations and the effect on the effective capacitances for discrete and monolithic half-bridges were systematically analyzed.

For the operation of a monolithic GaN-on-Si half-bridge, a novel substrate biasing network was proposed, which in contrast to the state of the art is independent from the duty-cycle during operation. Furthermore, the biasing network allows to shift the average substrate voltage towards positive values, which avoids static negative back-gating of the high-side transistor under all operation conditions.

- How does the substrate termination influence the switching behavior and performance of GaN-on-Si half-bridges and drivers?

The overall switching behavior of GaN power circuits on a common Si substrate depends on the combination of the two previously discussed effects: On the one hand, only if the effective half-bridge capacitances are reduced compared to a discrete half-bridge,

then an improved switching behavior is expected. On the other hand, only if a static on-resistance degradation is avoided by avoidance of negative back-gating, then the improvement by the reduced effective capacitances actually leads to an overall improved efficiency.

This work's proposed operation scheme for monolithic half-bridges ensures that none of both aspects are deteriorated. Rather, the proposed substrate biasing network for monolithic half-bridges avoids static on-resistance degradation but still allows beneficial utilization of the reduced effective device capacitances on a common semi-floating Si substrate.

A comprehensive experimental study on switching characteristics such as switching time, switching energies and dc-dc converter efficiency verified the analysis and proposed operation method for GaN-on-Si half-bridges on a common substrate. Since the proposed substrate biasing network for monolithic half-bridges not only avoids back-gating, but also reduces the effective switch-node capacitance of a half-bridge compared to a discrete half-bridge, it was possible to operate a dc-dc converter with higher efficiency compared to the operation of a discrete half-bridge using the same transistor technology and operation point.

Experimentally, a monolithic GaN-on-Si half-bridge with integrated gate drivers was operated at an input voltage of 200 V with a maximum efficiency of 98.75%. The proposed operation scheme reduced the power loss by over 10% compared to a comparable discrete half-bridge.

For the operation of monolithic half-bridges on a common conductive substrate, it is thus concluded that this work's proposed operation scheme enables highly efficient dc-dc conversion of monolithic GaN-on-Si half-bridges, with efficiencies exceeding that of a conventional discrete half-bridge with separate substrate-to-source terminations.

Furthermore, the proposed duty-cycle independent substrate biasing network avoids back-gated on-resistance increase over the full range of duty-cycles which is typically required in real power conversion applications.

3 Low-Inductive and Clean Switching of Half-Bridges and Gate Drivers

3.1 Problem and Approach

The monolithic integration of transistors allows to avoid external interconnect parasitics compared to a realization of the same circuit with discrete devices. For example, a monolithic half-bridge allows to avoid parasitic interconnection inductance between the high-side transistor's source and low-side transistor's drain terminals, and thus a reduction of the parasitic power-loop inductance. Monolithic integration of a gate driver final stage and the driven power transistor avoids the parasitic interconnection inductance between the main power transistor's gate and the driver output, and thus a reduction of the parasitic gate-loop inductance. Even though the monolithic integration of complete power topologies with control seems as a great solution to avoid parasitic inductance, a more detailed investigation is required: Both in the gate-loop and in the power-loop transistors switch between two different voltage potentials. And since the nature of a switched-mode power converter is that a switch-node (or the gate-node) is switched between (at least) two different voltages, at least one of the voltages is not zero. The non-zero voltage in the power-loop is the dc-link voltage, and in a unipolar gate driver for example it is the positive driver supply voltage. The dc-link and gate supply voltages are provided by external supplies which are stabilized by capacitors. Thus, external capacitors are part of the critical switched-current loops in both cases. Despite the possibility of monolithic integrated power stages and gate drivers, there are still interfaces from the IC to the external decoupling capacitors required. All external interfaces to the IC where fast switched-current changes occur are thus still critical, despite monolithic circuit integration, and can result in severe oscillations and even instabilities.

Fig. 3.1a gives an overview of all relevant parasitic interconnect inductances for a discrete half-bridge with discrete gate drivers.

Even though the monolithic integration reduces part of the loop inductance, the switching behavior of power circuits is still limited by the required external interconnects. Therefore, a careful design of the packages and a reduction of interconnect inductance is still relevant also for integrated GaN ICs.

Fig. 3.1b shows the remaining relevant parasitic interconnect inductances for a monolithic integrated half-bridge with integrated gate driver final stages. The monolithic half-bridge requires an alternative substrate termination compared to the separate substrate-to-source termination of a discrete half-bridge. Parasitic inductance issues related to the substrate-loops are discussed separately by this work in Chapter 4. This chapter focuses on the gate-loop and power-loop inductances and resulting effects on the switching characteristics.

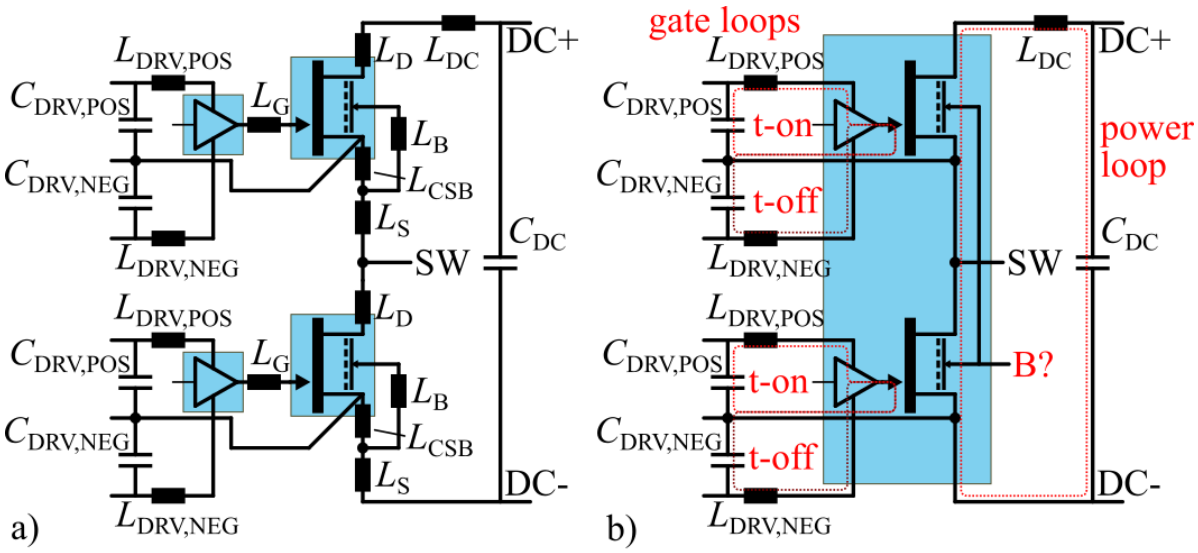

Figure 3.1: Parasitic interconnect inductances for a) a discrete half-bridge with discrete bipolar gate driver and external decoupling capacitors, and for b) a monolithic half-bridge with integrated bipolar gate driver and external decoupling capacitors.

One major issue of parasitic inductance are overvoltages due to overshoot. Overshoot voltages which exceed the blocking voltage of the transistors can result in device destruction and reliability issues. Therefore, overshoot should be minimized. By increasing the switching transition time it is possible to reduce also overshoot. However, at the same time switching losses can increase. Instead of a reduction of switching speed, reduction of parasitic inductance will also reduce the overshoot.

The severity of the effect of parasitic inductance is classified into three categories: 1. Negligible effect on the switching performance. 2. Limiting the switching performance and cause of oscillations with overshoot but still with stable and decaying envelope. 3. Instabilities which cause device destruction, typically due to excessive feedback to the gate terminal. In this chapter only the passive cases 1 and 2 are discussed. Instabilities caused by feedback to the gate will be separately discussed in Chapter 4.

This chapter investigates the dependency between parasitic inductance, switching speed and overshoot. Then measures to reduce parasitic inductance by both monolithic integration and advanced packaging of GaN circuits are presented.

The chapter addresses the following problems:

Research questions:

- How does parasitically increased inductance in the gate-loop or power-loop influence switching speed and overshoot?
- How much do monolithic integration and advanced packaging of GaN power circuits allow a reduction of parasitic inductances?

Approach: First it is theoretically analyzed how parasitic inductance causes overshoot, and how the overshoot is controllable by the voltage switching speed (Sec.3.2). It is theoretically and experimentally demonstrated that local minima of voltage overshoot

as a function of the switching speed exist for specific optimal switching times which beneficially utilize the resonance from the parasitic inductance (Sec.3.3). It is quantitatively shown how the optimal switching time depends on the damping factor of the parasitic loop (Sec.3.4). The effectiveness of monolithic gate driver and half-bridge integration for reduction of parasitic inductance in the gate-loop and power-loop is quantified by comprehensive electro-magnetic simulations. Several integrated circuit layouts as part of different bond-wire and printed-circuit-board (PCB)-embedded packages with on-package capacitors are compared (Sec.3.5). A PCB-embedded half-bridge with drivers and on-package decoupling capacitors is designed and experimentally verified (Sec.3.6).

3.2 Analysis of Parasitic Inductance-Related Voltage Switching Transitions

The intentional switching and conduction behavior of a power transistor is of resistive-capacitive type. For hard-switching transitions, the final on-state with a linear on-resistance R_{ON} is reached after a switching trajectory through the saturation region. The switching speed is limited due to the inherent device terminal capacitances. The saturation region in the I-V plane can be described with a non-linear resistance. For resonant transitions, the final on-state with again linear on-resistance is reached after the switch-node capacitance C_{SW} is charged for example by an externally provided inductor current. In both cases, the switching speed is intrinsically defined mainly by the resistive and capacitive parts of the transistor.

The intrinsic resistive and capacitive parts of the transistors will be considered as R and C in the following first principle analysis. Additional parasitic inductance is summed for a first principle analysis into L, and might include external interconnect inductance, on-chip interconnect inductance, as well as the self-inductance of large-area GaN ICs.

Voltage switching transitions will be described by either a step voltage source or a voltage ramp source with limited voltage slew-rate. For a theoretical analysis of switching transitions, the three lumped components R, L, C form a resonant circuit that is excited by the step or ramp voltage source.

Fig. 3.2 shows simplified equivalent circuits of the resonant circuits used in the following. While the time-domain analysis of a RLC circuit with instantaneous step-voltage excitation (Fig. 3.2a) is also found in textbooks, this work extends this analysis to a limited voltage slew-rate ramp-voltage excitation (Fig. 3.2b), which models the limited slew-rate voltage transition in bridge circuits in more detail. For the sake of completeness and comparison, both cases are analysis in the following.

3.2.1 Instantaneous Step-Voltage Switching

As a first principle analysis the intentional switching transition is described either as an R-C (resistor-capacitor) or I-C (current source-capacitor) circuit (zero parasitic inductance $L = 0$), depending on the momentary operation region (linear or saturation) during a switching transition and switching mode (hard or resonant). For analysis of the R-C case, the time t is normalized as $t' = \frac{t}{\tau_{\mathrm{R\text{-}C}}}$ to the time constant $\tau_{\mathrm{R\text{-}C}} = RC$, the capacitor

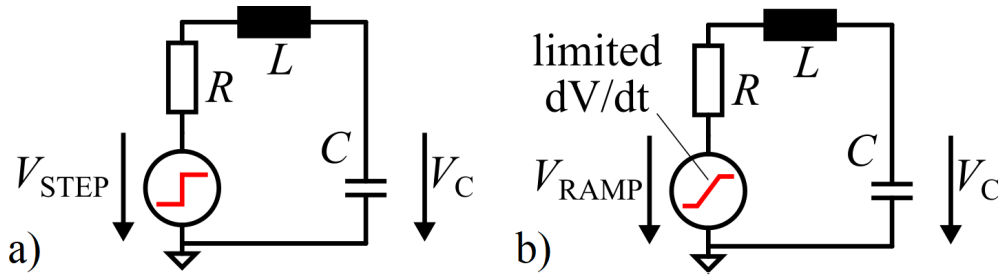

Figure 3.2: Simplified equivalent resonant circuit with a) instantaneous step-voltage excitation or b) limited voltage slew-rate ramp-voltage excitation.

voltage V_C as $V'_C = \frac{V_C}{V_{STEP}}$ and the capacitor current I_C as $I'_C = I_C \frac{R}{V_{STEP}}$ (with initial values V_{STEP} and I_0). Here, V_{STEP} is the step voltage, which in a (half-bridge) converter is the dc-link voltage V_{DC}, or part of it in case of partial hard-switching. For the I-C case, the time t is normalized as $t' = \frac{t}{\tau_{IC}}$ to the time constant $\tau_{IC} = \frac{V_{STEP} C}{I_0}$, and the capacitor current I_C as $I'_C = \frac{I_C}{I_0}$.

In any momentary operation point thus the subsequent switching transient is described as

$$V'_C(t') = 1 - e^{-t'}, t \geq 0 \quad (3.1)$$
$$I'_C(t') = e^{-t'}, t \geq 0 \quad (3.2)$$

in linear (constant resistance) operation (R-C) and

$$V'_C(t') = 1 - t', t \geq 0 \quad (3.3)$$
$$I'_C(t') = 1, t \geq 0 \quad (3.4)$$

in constant-current (I-C) operation.

Since the voltage response is always constrained between the initial (here: dc-link voltage V_{DC}) and final value (here: zero), no over- or undershoot is present. The voltage is monotonously changing during the switching time, and thus the final voltage is reached without superimposed high frequency oscillations or overshoots. In the R-C case, after the time $\tau_{R\text{-}C}$ the voltage changed by 65% of V_{STEP} and after $5\tau_{R\text{-}C}$, the voltage transitioned more than 99% and then further asymptotically approaches the final value. For the I-C case, after τ_{IC}, the voltage transitioned completely.The I-C transition then stops because in typical half-bridge converters the switch node voltage is then clamped to either zero or the dc-link voltage, either with a small positive linear on-state offset voltage (1st quadrant conduction) or a small negative reverse conduction offset voltage (typically from a freewheeling diode or reverse-diode behavior of the used transistors).

In the following, the R-C response will be used as reference and then parasitic inductance is added and the effect on transient response investigated.

As soon as there is (parasitic) inductance L inside the loop which is formed by the voltage step source (from switched transistors) and the RC components (part of the switching cell and transistors), the transient response to an infinitely fast instantaneous step voltage

$$V_{STEP}(t) = \begin{cases} 0 & t \leq 0 \\ V_{STEP} & t > 0 \end{cases} \quad (3.5)$$

is described for $t > 0$ by the differential equation

$$V_{\mathrm{STEP}}(t) = RI_{\mathrm{C}}(t) + L\frac{dI_{\mathrm{C}}(t)}{dt} + \frac{1}{C}\int_0^t I_{\mathrm{C}}(t')dt', t > 0. \tag{3.6}$$

The Laplace transformation of the differential equation

$$\frac{V_{\mathrm{STEP}}}{s} = RI_{\mathrm{C}}(s) + sLI_{\mathrm{C}}(s) + \frac{I_{\mathrm{C}}(s)}{sC} \tag{3.7}$$

is solved and then the inversely Laplace transformation of the solution gives the time response of the capacitor current $I_{\mathrm{C}}(t)$.

The transient response is divided into two cases with different characteristics.

Depending on the magnitude of the damping coefficient

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} > 0, \tag{3.8}$$

two distinct regions $\zeta > 1$ and $\zeta < 1$, separated by the boundary case $\zeta = 1$ result. At the boundary case $\zeta = 1$, the critial inductance value is defined as

$$L_{\mathrm{crit}} = \frac{CR^2}{4} \tag{3.9}$$

and the critical resistance value as

$$R_{\mathrm{crit}} = \sqrt{\frac{4L}{C}}. \tag{3.10}$$

Overdamped Case for Small Parasitic Inductance $L < L_{\mathrm{crit}}$ For small parasitic inductance $0 < L < L_{\mathrm{crit}}$, the LCR circuit is overdamped $\zeta > 1$. A time domain solution of the differential equation Eqn. 3.6 and $\zeta > 1$ is

$$I_{\mathrm{C}}(t) = \frac{V_{\mathrm{STEP}}}{L}\sqrt{\frac{1}{\left(\frac{R}{2L}\right)^2 - \left(\frac{1}{\sqrt{LC}}\right)^2}}e^{-\frac{Rt}{2L}}\sinh\left(t\sqrt{\left(\frac{R}{2L}\right)^2 - \left(\frac{1}{\sqrt{LC}}\right)^2}\right) \tag{3.11}$$

$$V_{\mathrm{C}}(t) = V_{\mathrm{STEP}} - \frac{V_{\mathrm{STEP}}}{\sqrt{\left(\frac{R}{2}\sqrt{\frac{C}{L}}\right)^2 - 1}}e^{\frac{-Rt}{2L}}\sinh\left(t\sqrt{\left(\frac{R}{2L}\right)^2 - \left(\frac{1}{\sqrt{LC}}\right)^2} + \cosh^{-1}\left(\frac{R}{2}\sqrt{\frac{C}{L}}\right)\right). \tag{3.12}$$

The voltage response $V_{\mathrm{C}}(t)$ follows from the current solution $I_{\mathrm{C}}(t)$ by integration $V_{\mathrm{C}}(t) = \int_0^t \frac{I_{\mathrm{C}}(t)}{C}dt$.

A general form of the expression is derived by substitution of the natural resonance frequency of the reactive components

$$\omega_{\mathrm{N}} = \frac{1}{\sqrt{LC}}. \tag{3.13}$$

Normalization to voltage, current and time using the same substitutions as for the R-C circuit simplifies Eqn. 3.12 to

$$I'_C(t') = \frac{2\zeta}{\sqrt{\zeta^2-1}} e^{-2\zeta^2 t'} \sinh\left(2\zeta\sqrt{\zeta^2-1}\,t'\right) \tag{3.14}$$

$$V'_C(t') = 1 - \frac{1}{\sqrt{\zeta^2-1}} e^{-2\zeta^2 t'} \sinh\left(2\zeta\sqrt{\zeta^2-1}\,t' + \cosh^{-1}(\zeta)\right). \tag{3.15}$$

In this work the voltage response is the critical quantity, because in switched-mode voltage converters the used transistors only have limited overvoltage margin. Thus, in the following, only the voltage response (Eqn 3.15) is further analyzed.

Fig. 3.3 plots the normalized voltage response (Eqn.3.15) and instantaneous switched voltage step (dashed) for different damping factors $\zeta > 1$ (overdamped case). The real-valued hyperbolic sinus terms in Eqn.3.15 represent no oscillation, but delays the current peak at $t' = 0$ compared to the R-C response (Eqn. 3.2) towards a delayed current peak with reduced amplitude. The voltage response likewise is smoothed at first, but the total risetime of the voltage is very similar to the R-C response. For vanishing small parasitic inductance $L \to 0$ the damping factor is very high $\zeta \to \infty$ and the response approaches the ideal RC response, except for a very rapid, but continuous, rise of the current to the initial value of the RC response. For the lowest damping factor $\zeta = 1^+$ which is still overdamped, the final voltage is approached quickest, but still monotonic without overshoot. It should be noted that since interconnections in circuits always exist the heavily damped case is a realistic achievable response, whereas an ideal RC response with a discontinuous current step at $t = 0$ is physically impossible. Typical dc-dc power stages with low on-resistance transistors in a half-bridge power-loop are typically not overdamped and also far away from critical damping due to the combination of low on-resistance and low device capacitances. Only in the gate-loop overdamping can be achieved without sacrificing the switching speed, since the gate driver typically provided a significantly higher series resistance.

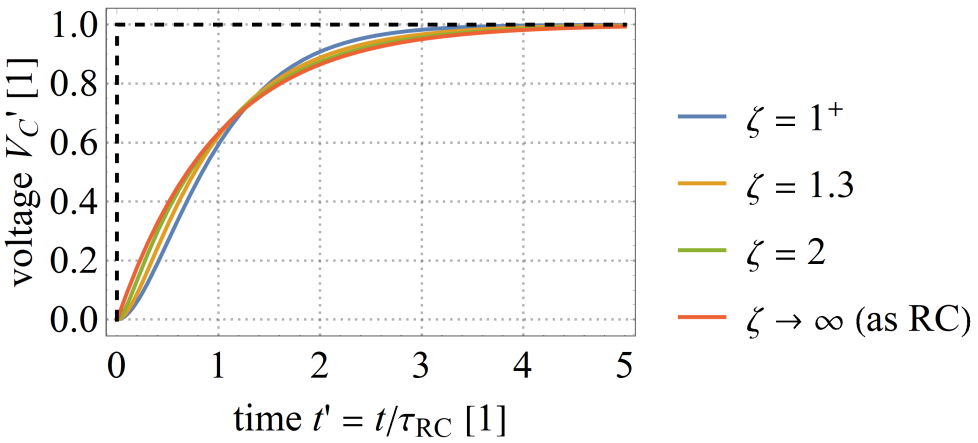

Figure 3.3: Overdamped voltage response to instantaneous voltage step switching for different damping factors.

Underdamped Case for Large Parasitic Inductance $L > L_{crit}$ If the parasitic inductance is higher than the critical inductance $L > L_{crit}$, the LCR is underdamped $\zeta < 1$. From Eqn. 3.9 and Eqn. 3.10 an alternative formulation of the condition is: If the series-resistance which provides damping is lower than the critical resistance $R < R_{crit}$, the LCR circuit is underdamped $\zeta < 1$. Since in power converters low on-resistance transistors are used to reduce conduction loss, and the layout and interconnects of the transistors limits the achievable reduction of parasitic inductance, typical power-loops of switching cells are underdamped, which will be quantified later.

The normalized transient response now results in

$$I'_C(t') = \frac{2\zeta}{\sqrt{1-\zeta^2}} e^{-2\zeta^2 t'} \sin\left(2\zeta\sqrt{1-\zeta^2}t'\right) \tag{3.16}$$

$$V'_C(t') = 1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-2\zeta^2 t'} \sin\left(2\zeta\sqrt{1-\zeta^2}t' + \cos^{-1}(\zeta)\right). \tag{3.17}$$

The underdamped response still has an exponentially decreasing envelope, but is now super-positioned with a damped sinusoidal oscillation with the damped resonance frequency

$$\omega_D = \omega_N\sqrt{1-\zeta^2} = \sqrt{\left(\frac{1}{\sqrt{LC}}\right)^2 - \left(\frac{R}{2L}\right)^2}. \tag{3.18}$$

While in the overdamped case the transient response had a characteristic time constant of $\tau_{R\text{-}C}$, almost independent of L (see Fig. 3.3, where the time axis is normalized to $\tau_{R\text{-}C}$), in the underdamped case now the reactive components define the characteristic time constant. The dominant time constant in the underdamped case is now linked to the damped resonance frequency ω_D. For low damping factors $\zeta \to 0$ the damped resonance frequency approaches the natural resonance frequency ω_N. Since the dominant time constant now strongly varies with the damping factor, in the following the time axis of the transient response is normalized to the natural resonance frequency $t' = t\frac{\omega_N}{2\pi}$.

Fig. 3.4 shows the normalized transient response for the underdamped case for different damping factors ζ. The dashed black line represents the instantaneous step-voltage

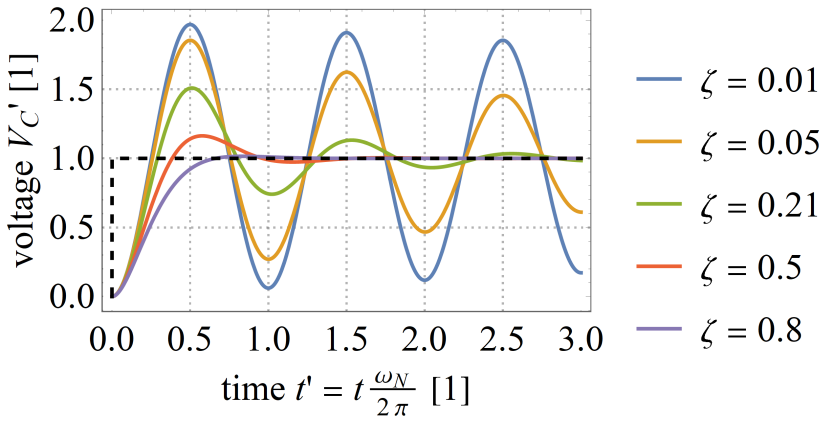

Figure 3.4: Transient response to instantaneous voltage step switching for different dampingfactors.

which is the excitation signal for the resonant circuit. For damping factors above $\zeta = 0.5$ still low overshoot <17% is observed. For vanishing low damping factors $\zeta \to 0$ however, the overshoot approaches +100%. The response has a superimposed damped sinusoidal with decaying envelope and thus multiple repetitive peaks of overshoot. The first overshoot has the highest amplitude and thus is of concern and analyzed further. Fig. 3.5 evaluates the maximum overshoot S_+ for different damping factors ζ. Starting

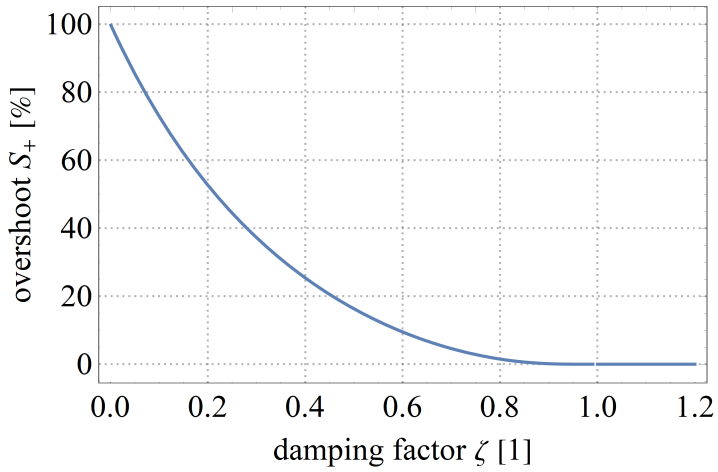

Figure 3.5: Overshoot as a function of the damping factor, assuming instantaneous step-voltage switching.

with a vanishing damping factor of $\zeta = 0$, the overshoot is +100%, and then decreases to +0% at a damping factor of $\zeta = 1$. For damping factors $\zeta > 1$, the data is from the overdamped case with no overshoot

Discussion and Conclusion on Instantaneous Step-Voltage Switching As an example for discussion, GaN power transistors for sub-1 kW class converters similar to the devices used in this work with an on-resistance of $R = 100\,\text{m}\Omega$ have an output capacitance of roughly 100 pF. Even a very low-inductive power module layout with $L = 1\,\text{nH}$ results in a low and underdamped damping factor of $\zeta = 0.016 \approx 0$. From Fig. 3.5 this would result in almost +100% overshoot, which is on the one hand unacceptable and on the other hand not as typically measured overshoot in switching experiments and real converters.

The analysis so far suggests the conclusion, that the damping factor (and thus the design and parameters of the transistors and switching-cell layout which causes parasitic inductance) is *the only* parameter to reduce the overshoot of a switching cell. As a consequence, if the switching cell is underdamped at first, for example due to low on-resistance transistors and parasitic inductance of the layout, then low overshoot is only achieved by improving the layout further (reducing L) or increasing the on-resistance, which is not desired from an application point of view. A voltage overshoot of +100% is not acceptable in most applications, and in experiments typically significantly lower overshoot is observed, despite low on-resistance transistors in an underdamped switching cell. The presented analytical model of instantaneous step-voltage switching, even though often adopted in the discussion of parasitic effects of switching cells and especially the gate driver loop inductance [86] [87] , thus is not complete and insufficient to

describe overshoot in real switching applications. In the following an extended analytical model will be described, where the damping factor is not the only parameter anymore to reduce overshoot.

3.2.2 Limited Voltage Slew-Rate Switching

A known countermeasure to reduce overshoot is to reduce the switching speed. The previous analysis however does not include the switching speed as a parameter. Instead, the previous analysis assumed an instantaneous step-voltage switching with infinitely fast switching speed. However, the switching speed of real power transistors is intrinsically limited by the maximum available saturation current and the terminal capacitances. Furthermore, it is well known that increasing the gate driver resistance allows to control and slow down a switching transition. Common practice is to experimentally adjust the gate resistor until excessive overshoot is avoided. Often the gate resistance is adjusted in large resistance steps, since resoldering of the gate resistors is a cumbersome process. It might be assumed that increasing the gate resistance monotonically reduces the overshoot. However, in the following it will be derived that the peak overshoot is not a monotonic function of the switching speed, and local minima of overshoot exist for specific optimal voltage transition times. It will be derived that low overshoot switching is possible by utilizing the resonance of the parasitic inductance in combination with limited voltage slew-rate switching. If the switching transition is considered as a ramp voltage transition with limited non-zero switching time, then the transient response is a superposition of a ramp voltage response and a delayed but inverted ramp voltage response (starting at the end of the switching transition). Both responses in the underdamped case cause decaying sinusoidal oscillations. Local minima of overshoot exist if the phase relation between both sinusoidal components is such that they cancel each other out as much as possible.

Only the underdamped case is considered here in detail ($\zeta < 1$), because the damped case is unproblematic and requires no further analysis. The infinitely fast and unphysical step voltage is replaced by a step-ramp voltage source

$$V_{\mathrm{STEP,dV/dT}}(t) = \begin{cases} 0 & t \leq 0 \\ V_{\mathrm{STEP}} \frac{t}{t_0} & 0 < t \leq t_0 \\ V_{\mathrm{STEP}} & t > t_0 \end{cases} \tag{3.19}$$

with a limited and constant voltage slew-rate dV/dt ($= \frac{V_{\mathrm{STEP}}}{t_0}$). For $t > 0$ the resonant circuit which is excited by the step-ramp voltage is described by the differential equation (in the Laplace domain)

$$\frac{V_{\mathrm{STEP}}}{s} \frac{1}{t_0 s}(1 - e^{-s t_0}) = R I_{\mathrm{C}}(s) + s L I_{\mathrm{C}}(s) + \frac{I_{\mathrm{C}}(s)}{sC}. \tag{3.20}$$

To the solution of the differential equation the inverse Laplace transformation is applied and gives the time domain response for the current $I'_{\mathrm{C}}(t)$. The response for the voltage $V'_{\mathrm{C}}(t)$ follows by integration. Using ramp functions

$$V_{\mathrm{RAMP}}(t) = \begin{cases} 0 & t \leq 0 \\ V_{\mathrm{STEP}} \frac{t}{t_0} & 0 < t \end{cases} \tag{3.21}$$

the step-ramp function $V_{\mathrm{STEP,dV/dT}}$ with limited slew-rate is expressed as

$$V_{\mathrm{STEP,dV/dT}}(t) = \begin{cases} 0 & t \leq 0 \\ V_{\mathrm{RAMP}}(t) & 0 < t \leq t_0 \\ V_{\mathrm{RAMP}}(t) - V_{\mathrm{RAMP}}(t - t_0) & t_0 < t, \end{cases} \tag{3.22}$$

which is the sum of a ramp function and an delayed inverted ramp function. Due to linearity, the transient response $V'_{\mathrm{C}}(t)$ is the sum of the response to the ramp function and the time delayed inverted response to the ramp function

$$V'_{\mathrm{C}}(t') \;=\; V'_{\mathrm{C,RAMP}}(t') - V'_{\mathrm{C,RAMP}}(t' - t'_0), \tag{3.23}$$

where

$$V'_{\mathrm{C,RAMP}}(t') = \frac{(t'-1)}{t'_0} + \frac{1}{2t'_0\zeta\sqrt{1-\zeta^2}} e^{-2\zeta^2 t'} \sin\left(2\zeta\sqrt{1-\zeta^2}t' + 2\cos^{-1}(\zeta)\right) \tag{3.24}$$

is the voltage response for the unclamped ramp input $V_{\mathrm{RAMP}}(t)$ and the voltage rise time t_0 is normalized to $\tau_{\mathrm{R\text{-}C}}$ as $t'_0 = \frac{t_0}{\tau_{\mathrm{R\text{-}C}}}$.

The discussed response here is always under-damped ($\zeta < 1$), but there is still a way to optimize the overshoot. The ramp response has a damped sinusoidal component with the same damped resonance frequency ω_{D} as in the ideal voltage step case, since only the excitation signal is changed but not the R-L-C system.

Based on Eqn. 3.23 and Eqn. 3.24 now the effect of limited voltage slew-rate on transient response is investigated. After the step-ramp voltage transition is finished ($t' > t'_0$), two damped sinusoidal oscillations with the same damped resonance frequency are superimposed. Despite a constant offset term, the superimposed sinusoidal signal components from evaluation of Eqn. 3.23 are

$$\sin\left(2\zeta\sqrt{1-\zeta^2}t' + 2\cos^{-1}(\zeta)\right) - e^{2\zeta^2 t0'} \sin\left(2\zeta\sqrt{1-\zeta^2}(t' - t0') + 2\cos^{-1}(\zeta)\right) \tag{3.25}$$

The transient response contains the sum of two time delayed and inverted sinusoidal signals of the same frequency. Since both oscillations are exponentially damped, the repeating local extrema have decreasing absolute amplitudes.

Minimum Overshoot Switching: The first peak of overshoot voltage after the transition is finished ($t' > t'_0$) is minimized if the first ($k = 1$) local maximum of the delayed signal is time-aligned to the first local minimum of the non-delayed signal. This is achieved for a phase difference $\phi = 2\pi$ between the delayed and non-delayed signal (Since the two sinusoidal signals are inverted according to Eqn. 3.24 or Eqn. 3.25, the optimal phase relation for signal canceling is $\phi = 2\pi$ and not $\phi = 1\pi$). Further local minima exist at phase differences $\phi = k2\pi, k \in \mathbb{Z}$. In the following only the first minimum is considered, because the others require a further increase of switching time (further limiting the voltage slew-rate), but do not yield a further significant overshoot reduction. Nevertheless, it should be noted that the analysis can also be adapted to resonant

(soft) switching converters, where the inductor current and not the transistor saturation current defines the switching time. There are especially efficient converters operating in triangular current mode (TCM), where the negative turn-off current of a rising (or falling) voltage transition is set to around 5%-30% of the positive turn-off current of the other falling (or rising) voltage transition. Since the current set-point typically is only constrained by efficiency considerations and can be slightly varied, it is possible to set the turn-off current to such discrete current values that the voltage transition ends exactly at any of the later optima $k > 1$.

Evaluation of $2\pi = 2\zeta\sqrt{1-\zeta^2}\mathrm{t_0}'$ from the phase difference in Eqn. 3.25 results in the normalized overshoot-optimal voltage transition time (switching time)

$$t'_{0,\mathrm{OPT}} = \frac{\pi}{\zeta\sqrt{1-\zeta^2}}, (\zeta < 1) \tag{3.26}$$

After canceling of the substitutions, the overshoot-optimal voltage transition time is

$$t_{0,\mathrm{OPT}} = \frac{2\pi}{\omega_\mathrm{D}} = \frac{2\pi}{\omega_\mathrm{N}\sqrt{1-\zeta^2}} = \frac{2\pi\sqrt{LC}}{\sqrt{1-\zeta^2}}. \tag{3.27}$$

The analysis is especially interesting for the case of an almost un-damped switching cell, where $\zeta \to 0$ and thus the optimal switching time is approximated independent from the resistance R as

$$t_{0,\mathrm{OPT}} \approx \frac{2\pi}{\omega_\mathrm{N}} = 2\pi\sqrt{LC}. \tag{3.28}$$

The approximation is accurate within 5% for damping factors $0 < \zeta < 0.32$ (calculated from Eqn. 3.18), and thus sufficiently accurate for typical applications with very low on-resistance transistors.

Fig. 3.6 plots the normalized voltage response to limited voltage slew-rate ramp functions for different switching transition times t_0 and three different damping factors. For infinitely fast instantaneous switching $t_0 \to 0$, the highest overshoot is observed, with peak overshoot up to +100% as already shown in Fig. 3.5. For the optimal switching $t_0 = t_{0,\mathrm{OPT}}$, the overshoot is reduced to a local minimum. For switching times which are slightly lower or slightly higher than the optimal switching time, in both cases the peak overshoot increases. For a vanishingly damping factor of $\zeta \to 0$, the local minimum is even reduced to zero overshoot. This finding is significant, because it means that it is possible to switch a low-resistive switching-cell very fast with low overshoot, by slight adjustments of the switching time and advantageous usage of the resonance of the parasitic inductance. A similar finding was also experimentally observed and verified by Stefan Matlok for a special case in [88, 89]. For non-zero damping factors, the first local overshoot minimum at the optimal switching time still is always below +8%.

For the the optimal voltage switching time, the optimal response is reconstructed by evaluation of Eqn. 3.23 for $t'_{0,\mathrm{OPT}}$:

$$V'_\mathrm{C}(t') = \begin{cases} \frac{\zeta\sqrt{1-\zeta^2}}{\pi}(t'-1) + \frac{1}{2\pi\zeta\sqrt{1-\zeta^2}} e^{-2\zeta^2 t'} \sin\left(2\zeta\sqrt{1-\zeta^2}t' + 2\cos^{-1}(\zeta)\right) & 0 \le t' < t'_{0,\mathrm{OPT}} \\ 1 - \frac{1}{2\pi} e^{-2\zeta^2 t''}(1 - e^{\frac{-2\pi\zeta}{\sqrt{1-\zeta^2}}}) \sin\left(2\zeta\sqrt{1-\zeta^2}t'' + 2\cos^{-1}(\zeta)\right) & 0 \le t'', \end{cases} \tag{3.29}$$

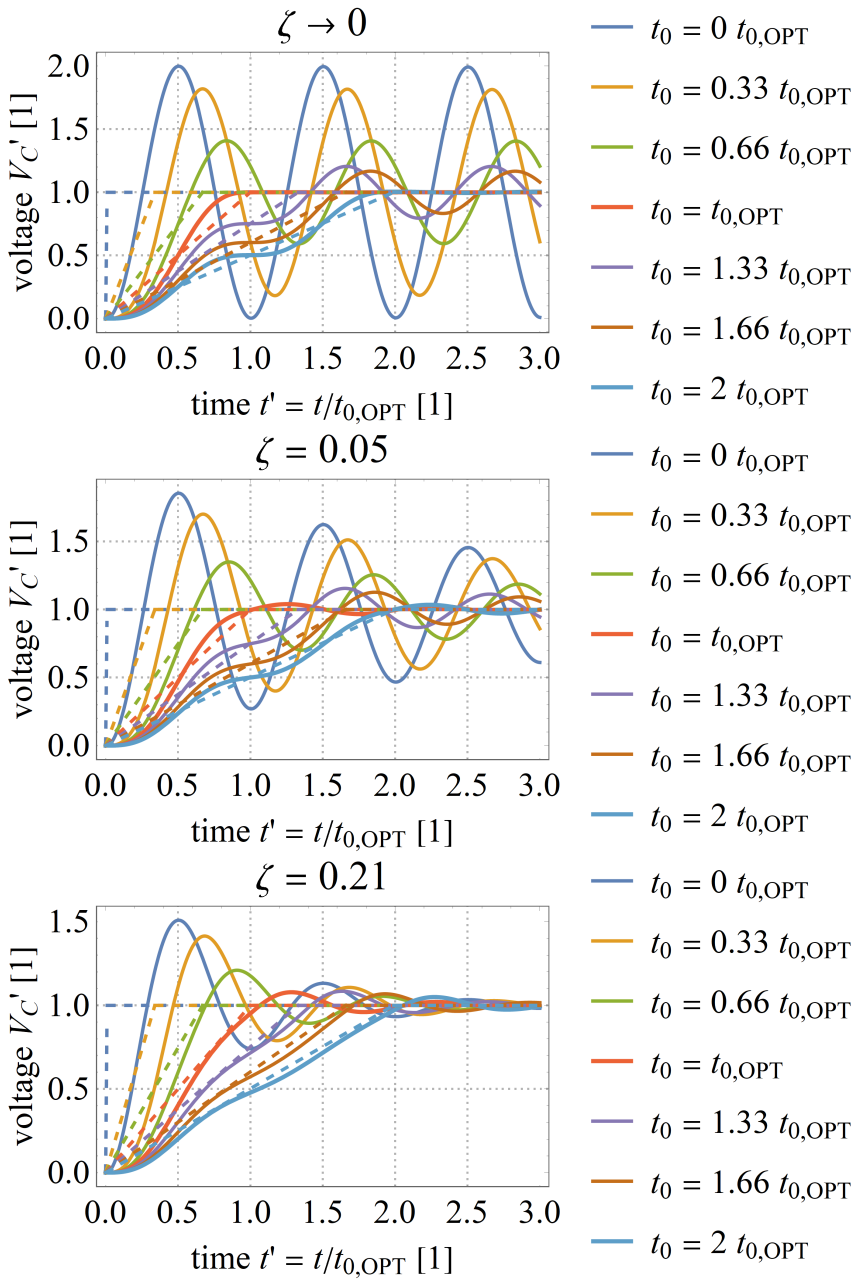

Figure 3.6: Voltage response for three underdamped damping factors ζ. The voltage response shows oscillations with different peak values, depending on the switching time of the limited slew-rate voltage excitation signal.

where for readability the time shift $t' = t'' + t'_{0,\mathrm{OPT}}$ into a time system which starts at $t'' = 0$ was applied to the second expression which starts at $t' = t'_{0,\mathrm{OPT}}$, Fig. 3.7 shows the transient response to the optimal switching time, and also the second and third local minima for multiples of the optimal switching time. Again, three different damping factors are evaluated.

The first local minimum is analyzed further, since it is the fastest transition with a local overshoot minimum. Fig. 3.8 shows the response to the optimal switching time for a wide range of damping factors. While at $\zeta \approx 0.21$ the overshoot is highest with $\approx 8\%$, for both $\zeta \to 0$ and $\zeta \to 1$ the overshoot vanishes. Fig. 3.9 evaluates the peak overshoot

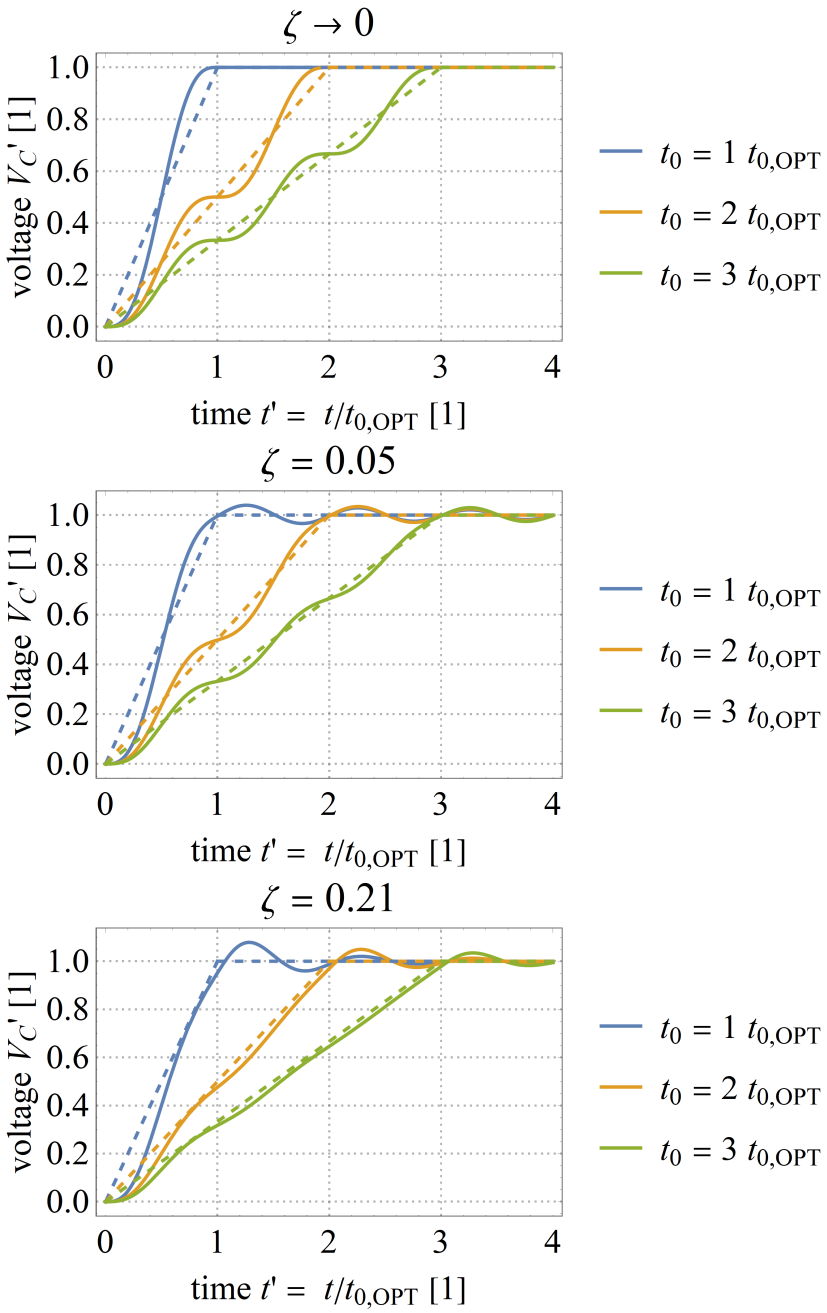

Figure 3.7: Voltage response for three underdamped damping factors ζ. The overshoot of the first peak of the voltage response is minimized by adjustment of the switching times to integer-multiples of the overshoot-optimal switching time $t_{0,\mathrm{OPT}}$.

for the first three optimal switching times as a function of the damping factor. The plot again shows that for $\zeta \to 0$ and optimal switching times the overshoot is mitigated.

Finally, Fig. 3.10 compares the results of the analysis with limited slew-rate switching to the instantaneous step-voltage switching analysis.

By comparison to the analysis with an infinitely fast voltage step, where for very low damping factors up to 100% voltage overshoot is encountered, the presented method to adjust the switching time allows below 8% overshoot despite an almost undamped system. For damping factors $\zeta < 0.21$, the lower the damped factor of the switching, the

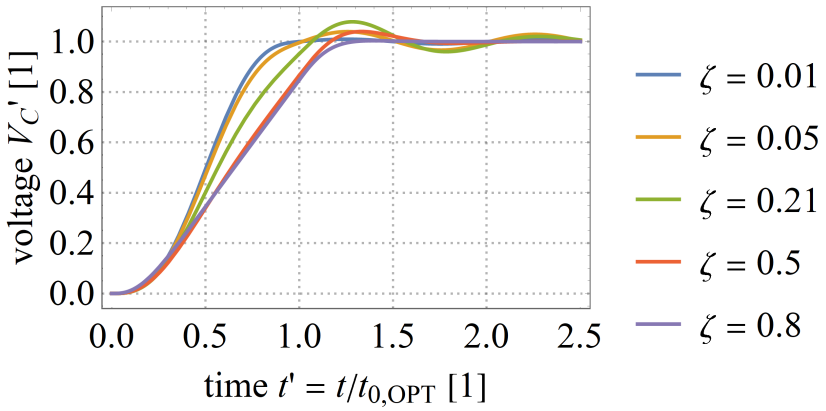

Figure 3.8: Voltage response for the overshoot-optimal switching time and wide range of underdamped damping factors.

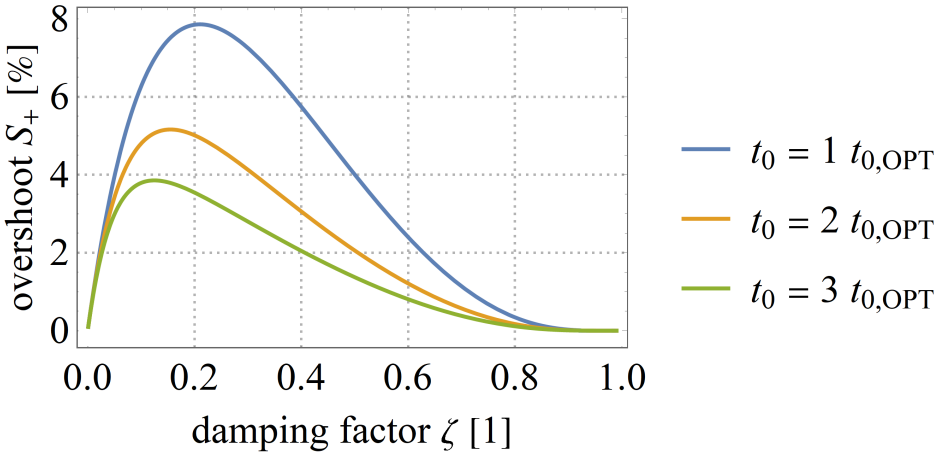

Figure 3.9: Overshoot for the three first overshoot-optimal switching times as a function of the damping factor.

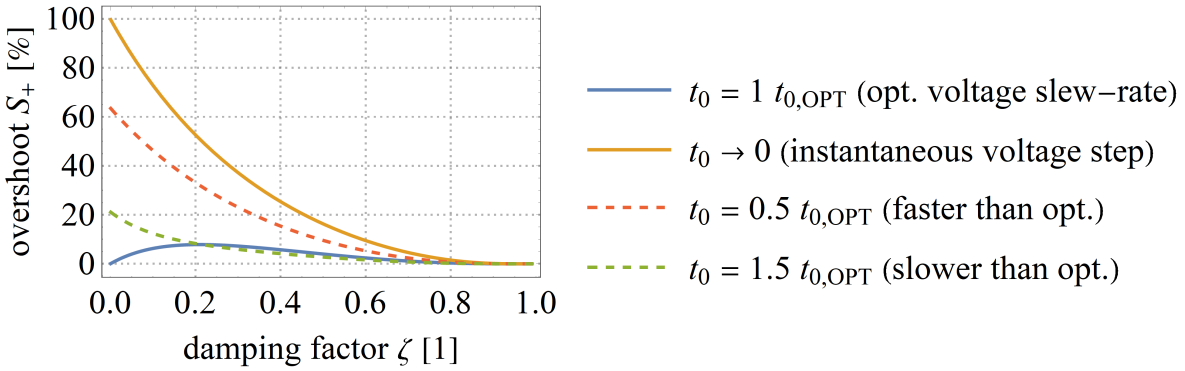

Figure 3.10: Comparison of the overshoot for instantaneous voltage switching ($t_0 \to 0$) compared to a reduced overshoot-optimal switching time $t_{0,\mathrm{OPT}}$.

better it theoretically allows zero overshoot switching at an optimal switching time. This counter-intuitive phenomenon is explained because for zero damping with the optimal switching time the LC-resonance is optimally used in such a way that at the end of the switching time the resonance has a maxima and the voltage is then clamped to the conduction voltage of the other half-bridge transistor. Another formulation is that for

a completely undamped system the derivative of the voltage at the end of the optimal switching time is zero and thus as soon as the voltage is clamped to the operation voltage, for example in a half-bridge circuit, the voltage after the switching transition continues without superimposed oscillations.

Since real switching cells are not ideal RLC systems, and the slew-rate during switching transitions is not constant (for example from non-linear terminal capacitances), non optimal switching transition times typically occur. Fig. 3.11 plots the overshoot for a continuous range of switching times, normalized to the optimal switching time and for different damping factors.

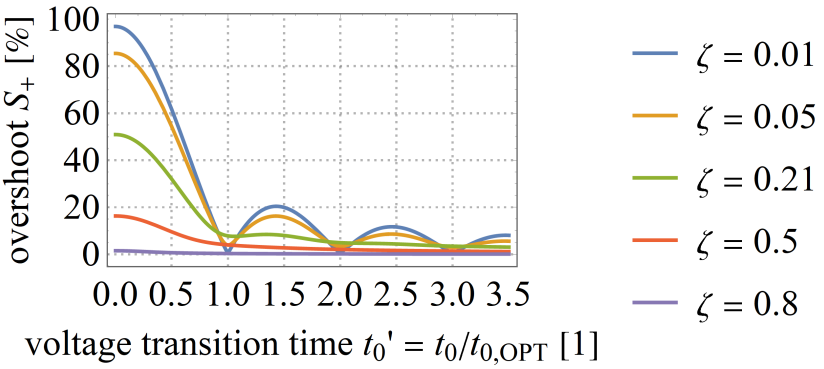

Figure 3.11: Overshoot for different damping factors as a function of switching time, normalized to the overshoot-optimal switching time. Local minima of overshoot are observed at multiples of the first optimal switching time $t_{0,OPT}$.

From Fig. 3.11 several practical dimensioning rules are derived. If the intrinsic time constant of the transistor is faster than the optimal switching time, then the voltage transition time should be increased (for example by the gate driver) to at least $0.8t_{0,OPT}$, which ensures below 25% overshoot. Reducing the switching time further is not advised, because if the switching time is just slightly further reduced to $0.6t_{0,OPT}$, already 50% overshoot are expected. A conservative approach is to dimension the switching time to $t_{0,OPT}$ or multiples of $t_{0,OPT}$.

3.2.3 Discrepancy between Measured and Intrinsic Switching Times

While the theoretical analysis allows calculation of any internal node voltages, in experiments voltage probes are required to measure the switching transitions. The voltage probes are connected across externally accessible nodes of the switching cell. The measured voltage thus can includes a large part of the parasitic loop inductance. The measured switching voltages then includes the induced voltage across the inductance and deviates from the intrinsic switching voltage of the transistors.

This subsection discusses the discrepancy between measured and intrinsic switching times. The discussion is a worst-case analysis, where it is assumed that the parasitic inductance (L in the previous sections) of the switched loop is completely included in the measured voltage. The measured voltage thus is V_C and the intrinsic switched voltage is the limited voltage slew-rate ramp function $V_{STEP,dV/dT}$. The transition time of $V_{STEP,dV/dT}$ is t_0. Typically, the measured switching times are the voltage transition

times between the 10% and 90% state levels. In a half-bridge, the two voltage levels are 0 V and V_{DC} and the 10% and 90% state levels are $0.1V_{DC}$ and $0.9V_{DC}$. If the step voltage source $V_{STEP,dV/dT}$ with a total transition time (0%-100%) of t_0 is described with the typical 10%-90% definition, only $0.8t_0$ is the measured 10%-90% transition time. The 10%-90% transition times are in the following denoted as part of the variable names such as $t_{0,10/90} = 0.8t_0$.

Now the voltage which can be measured and includes the parasitic inductance V_C is compared to the intrinsically switched voltage $V_{STEP,dV/dT}$. For slow switching transitions $t_0 \gg t_{0,OPT}$ or an overdamped response, the effect of the parasitic inductance is low and the measured voltage is approximately the intrinsic voltage. For fast switching transitions, however, a discrepancy is unveiled: For example, for the overshoot-optimal switching time $t_{0,OPT}$, and an almost undamped circuit $\zeta \to 0$, the measured transition time is faster than the intrinsic switching time. This exemplary case is shown in Fig. 3.7. Here, the (measured 10%-90%) transition time is only 49% of the (intrinsic 0%-100%) switched voltage time $V_{STEP,dV/dT}$.

Fig. 3.12 shows the calculated dependency of the ratio $t_{10/90}/t_0$ between the 10%-90% transition time (which includes the parasitic inductance) and the intrinsic switched voltage transition time. For slow voltage transitions $t_0 \gg t_{0,OPT}$, the ratio is approximately constant and 0.8 as expected due to the 10%-90% definition. For faster transitions in a range of around $0.25t_{0,OPT}...1.1t_{0,OPT}$ the ratio is reduced and gets as low as 0.49. The discrepancy is highest for almost undamped systems $\zeta \to 0$, such as the power-loop of a half-bridge. For theoretical even faster switching transitions $t_0 < 0.1t_{0,OPT}$, the resonance of the parasitic inductance dominates the transient response, such that the measured transition time does not reduce to zero, even for theoretically infinitely fast instantaneous voltage step switching. In this case, the measured voltage transition time is significantly higher than the intrinsic switching time.

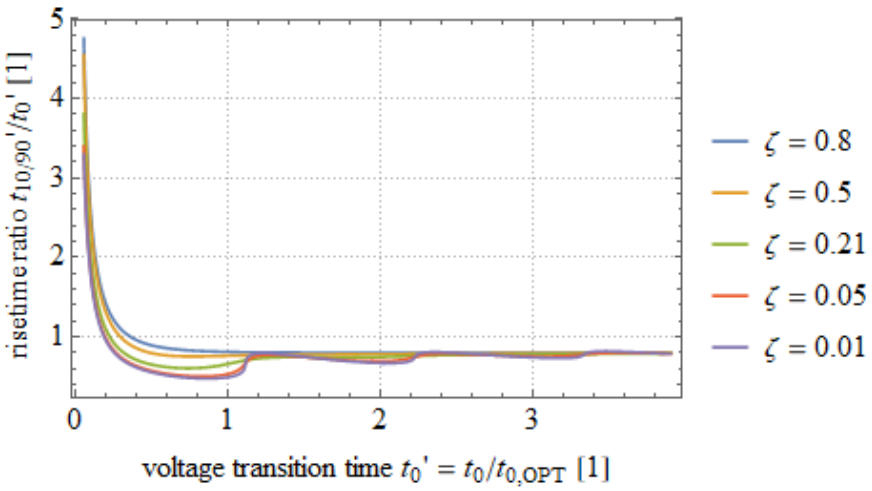

Figure 3.12: The discrepancy between the measured rise-time and the intrinsic switching time, calculated as a function of switching time. For switching times lower than the optimal switching time t_0, the measured switching time shows a significant discrepancy from the intrinsic switching time.

3.3 Experimental Overshoot Measurement for Limited Slew-Rate Switching

To verify the theoretically derived local minima of overshoot depending on the switching speed, a measurement is carried out. The setup uses a discrete GaN half-bridge on a ceramic substrate with low-inductive power-loop. The parasitic power-loop inductance of the particular bond-wire assembly is approximately 2.64 nH (the quantification of power-loop inductance will be discussed later in detail), the power transistors have around 85 mΩ on-resistance and the effective output capacitance of the high-side and the low-side transistor at 200 V switch-node voltage is in the range of 10-100 pF. The calculated expected damping factor ζ is below 0.01, which is almost undamped and thus covered by the previous theoretical analysis. The calculated optimal switching time for the range of effective capacitance is between 1.02 ns and 3.23 ns. The transistor does not allow instantaneous voltage step switching, but is limited in voltage slew-rate due to the device capacitances and the current which charges/discharges this capacitance during the switching transitions. As an estimation of the fastest achievable intrinsic switching time, both a hard-switching and a soft-switching case are considered. During hard-switching, the internal channel current is limited by the saturation current of the 2DEG. Furthermore, due to the feedback from drain to the gate, the actual channel current is practically lower than the saturated drain current and limited by the strength of the gate driver. In soft-switching operation the external inductor current has to be lower than the saturated drain current, otherwise the transistor cannot conduct the current with a low on-state voltage after the soft-switching transition is finished. A typical measured saturation current of the used device of 50 A [62] is assumed as the maximum drain current. With 50 A, a 200 V voltage transition of the output capacitance in the range of 100 pF is 0.5 ns. For the used technology, this is an estimate of the minimum achievable intrinsic switching time for 200 V voltage switching. Since the calculated minimum possible switching time is less than half of the overshoot-optimal switching time, it is possible to experimentally vary the switching time around the calculated optimum and experimentally quantify the overshoot.

In typical power converters the gate driver has a fixed gate resistor value, such that hard-switching transitions at the same voltage and current levels will always result in the same switching speed. To modify the switching speed in hard-switching conditions over a wide range with many measurement points, it would be necessary to change the gate resistor in very fine steps. It should be noted that there exist programmable active gate drivers which allow adjustment of the driver strength over time without component changes [90, 91]. However, these drivers typically are very complex and realized in a Si-CMOS technology, and thus not considered further, since in this work a integrated driver final stage with lower complexity is used. Since the required re-soldering or manual replacement of the resistors is an unnecessarily timeconsuming approach, here another approach to modify the switching time is followed. Instead of hard-switching transitions, where the switching speed is mainly defined by the channel saturation current, here soft-switching transitions are measured. In (resonant) soft-switching operation, the voltage transitions are caused by the inductor current. The inductor current in turn is easily adjusted by pulse duration of multiple switching pulses. Similar to the well-

known double-pulse measurement, here a multi-pulse experiment is carried out. The power inductor, pulse length, duty-cycle and number of pulses were selected in such a way, that in 80 consecutive pulses the inductor current is increased from 0 A in steps of 0.54 A up to 43.7 A. The resulting switching time t_R (here the rise-time of V_{SW}) of the resonant switching transition is inversely proportional to the inductor current I_L. With the wide range of selected inductor currents, the range of switching times between <1 ns and 6 ns is covered by a fine grid of measurement points. This range exceeds the theoretically calculated and expected optimal switching time between 1.02 ns and 3.23 ns with a sufficient margin.

Fig. 3.13 shows the measured switch-node voltage and inductor current for the experiment. From the measured envelope of V_{SW}, the observed peak overshoot shows as a non-monotonic function depending on the inductor current. The measured overshoot is extracted for all switching transitions. Furthermore, the rise-time of the voltage transitions is measured. It was previously discussed that the measured rise-time deviates from the intrinsic switching time. As an alternative value which represents the intrinsic switching time, the inverse inductor current is additionally used as a measure of the switching time.

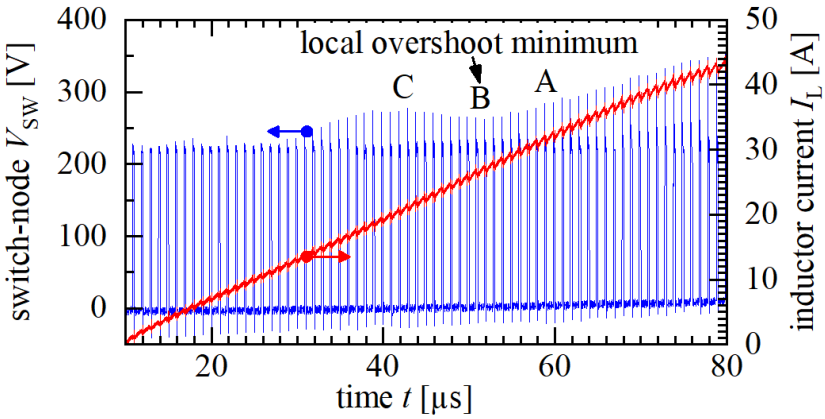

Figure 3.13: Multi-pulse measurement with linearly increasing inductor current shows non-linear overshoot with a local minimum of overshoot.

Fig. 3.14 shows the extracted overshoot as a function of the measured voltage switching time (lower x-axis) and alternatively as a function of the inverse inductor current (upper x-axis). For the fastest switching times (at the highest inductor current of 43.7 A), the measured overshoot was as high as +67%. The fastest directly measured switching time here is 0.96 ns. Since the measured switching times did not increase further above 20 A, the fastest switching time estimated from the inverse inductor current is below 0.5 ns and also shown in Fig. 3.14.

At around 1.2 ns the first local minimum of overshoot is observed. At this first overshoot-optimal switching time, the measured overshoot is reduced to +19%. The measurement shows that the small reduction of switching time from below 1 ns to 1.2 ns significantly reduced the overshoot. This highlights the importance of switching time as a parameter for reduction of overshoot.

For switching times higher than the first optimal switching time, the overshoot increases again up to +25% (at around 1.7 ns). Around 2.4 ns, which is twice the optimum

switching time and thus the second local minimum, the overshoot is further reduced to 8%.

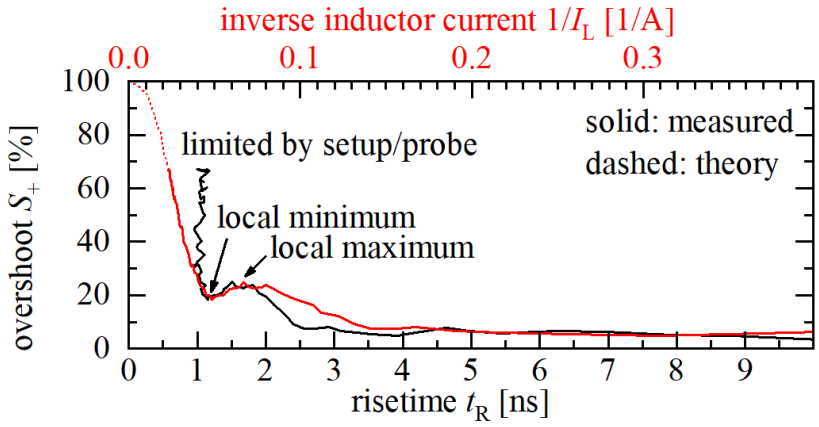

Figure 3.14: Measured overshoot as a function of the switching time (voltage risetime). The inverse inductor current at the resonant transitions is proportional to the switching time and given as an indirect alternative quantification of to the switching time.

Fig. 3.15 compares the first overshoot-optimal fast switching transition (B) with a slightly faster switching transition (A) and a slightly slower switching transition (C). The three selected transitions are also marked in Fig. 3.13.

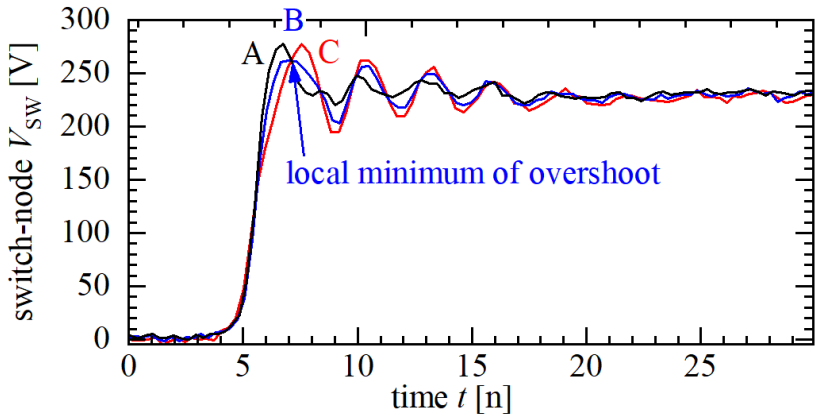

Figure 3.15: Comparison of three voltage switching waveforms with monotonic increasing switching time shows a local minimum of overshoot.

The measurement verifies that there exist local overshoot minima and that the adjustment of the switching-time is an effective approach for overshoot reduction in the presence of parasitic inductance. Since the switching behavior however is still limited by the parasitic inductance, in the following measures to reduce the parasitic inductance will be extensively discussed.

	$R = 0.1\,\Omega$ (e.g. power-loop)					
$L \rightarrow$	0.1 nH		1 nH		3 nH	
$C \downarrow$	ζ	$t_{0,\mathrm{OPT}}$	ζ	$t_{0,\mathrm{OPT}}$	ζ	$t_{0,\mathrm{OPT}}$
10 pF	0.022	0.3 ns	0.007	0.9 ns	0.004	1.5,ns
40 pF	0.032	0.4 ns	0.010	1.3 ns	0.006	2.2 ns
100 pF	0.050	0.6 ns	0.016	2.0 ns	0.009	3.4 ns
	$R = 5\,\Omega$ (e.g. gate-loop)					
$L \rightarrow$	0.1 nH		1 nH		3 nH	
$C \downarrow$	ζ	$t_{0,\mathrm{OPT}}$	ζ	$t_{0,\mathrm{OPT}}$	ζ	$t_{0,\mathrm{OPT}}$
10 pF	1.12	overdamped	0.35	1.0 ns	0.20	1.6 ns
40 pF	1.58	overdamped	0.50	1.5 ns	0.29	2.3 ns
100 pF	2.50	overdamped	0.79	3.2 ns	0.45	3.9 ns

Table 3.1: Damping factor ζ and overshoot-optimal switching time $t_{0,\mathrm{OPT}}$ for different C/L combinations and damping resistances $R = 5\,\Omega$ (similar to the gate driver in this work) and $R = 0.1\,\Omega$ (similar to the power transistors in this work).

3.4 Estimation of Typical Damping Factors and Optimal Switching Times

As an estimation of the damping factors, here several boundary cases are quantified. Since the capacitances of the transistors are highly non-linear and bias-dependent, here the calculation is presented for three typical averaged capacitance values. Both the switch-node capacitance (power-loop) and the input capacitance of the transistors (gate-loop) are within the shown range of $C = 10...100\,\mathrm{pF}$. Two representative damping resistances are used for the calculation. For the power-loop a damping resistance of $R = 0.1\,\Omega$ is chosen, which is similar to the on-resistance of the main power transistors used in this work. For the gate-loop a total damping resistance of $R = 5\,\Omega$ is chosen, which is similar to the sum of the integrated gate driver resistance and external additional gate resistance in this work.

The damping factor ζ and the overshoot-optimal switching time $t_{0,\mathrm{OPT}}$ are then calculated for all combinations. Tab. 3.1 lists the calculated values for three parasitic inductance values: A very low parasitic inductance value of $L = 0.1\,\mathrm{nH}$ mimics an extremely optimized loop layout, which can be difficult to realistically achieve. A low parasitic inductance value of $L = 1\,\mathrm{nH}$ represents optimized layouts, which are achieved in state-of-the-art modules with a careful loop optimization. An increased parasitic inductance of $L = 3\,\mathrm{nH}$ is a typical value for well-designed but not optimized conventional layouts, for example using semiconductor devices which are interconnected with bond-wires and packaged in surface-mount cases.

Evaluation of the damping factor for the power-loop ($R = 0.1\,\Omega$) shows a damping factor $\zeta \leq 0.05$ for all selected parameter combinations. The power-loop thus is always an almost undamped ($\zeta \rightarrow 0$) resonant circuit. The optimal switching time $t_{0,\mathrm{OPT}}$ is now compared to an intrinsic switching speed limit of the transistors. From Tab. 3.1

is is clear, that this intrinsic switching speed is faster than the optimal switching times (except for the two lowest-L and low-C cases). For $L \geq 1\,\text{nH}$ the optimal switching time is more than double the intrinsic switching time. This means, that the switching speed in the power-loop should be limited (by the gate driver). Likewise, the calculations show the importance of low parasitic inductance. To release the full switching speed without excessive overshoot, the power-loop should be minimized. Several approaches to reduce the power-loop inductance are presented in the following section.

Evaluation of the damping factor for the gate-loop ($R = 5\,\Omega$) shows that for very low $L = 0.1\,\text{nH}$ the gate-loop is overdamped and no overshoot is expected. For $L = 1...3\,\text{nH}$, the damping factor is in a range of 0.2 to 0.79, which is underdamped. The damping factor in the gate-loop, even though underdamped, is significantly higher than in the power-loop. In order to compare the optimal switching times to intrinsic switching speed limits for the underdamped cases, from a gate-resistance $R = 5\,\Omega$ and typical switching gate voltages in the range of 5 V, for the typical input capacitance of $C = 100\,\text{pF}$, a minimum switching speed limit of $t_{\text{SW,MIN}} \approx \frac{C\Delta V}{I} = 0.5\,\text{ns}$ follows. This sub-nanosecond intrinsic switching-speed from the particular gate driver is similar to the limit of the power-loop. One reason for this similarity is that the layout of the transistor structure itself, including the field plates, uses already a well-balanced intrinsic HEMT design (including for example field plates and gate length dimensioning). For low parasitic inductance $L = 1...3\,\text{nH}$ the overshoot optimal switching times are however slower than the intrinsic switching speed limit. To avoid overshoot in the driver, the gate resistance could be further increased $R > 5\,\Omega$. As in the power-loop, the intrinsic switching speed of the transistor cannot be fully exploited until the parasitic inductance is reduced to very low values. This motivates the next section, which discusses several approaches to also reduce the gate-loop inductance.

3.5 Reduction of Parasitic Gate-Loop and Power-Loop Inductance

3.5.1 Monolithic Integrated Gate Driver

Fig. 3.16a shows a typical gate driver circuit which is connected to a main power transistor. The driver switches two gate driver supply voltages through a resistive path to the gate of the main power transistor. The positive (or higher) driver supply voltage is $V_{\text{DRV,POS}}$ and the negative (or lower) driver supply voltage is $V_{\text{DRV,NEG}}$. Depending on the type and threshold voltage of the transistor, one of the supply voltages can be zero. The switching and resistive path in the driver is realized by two transistors in a push-pull configuration. Optionally, additional external resistors can be used in series to the driver final stage in order to increase the driver's output resistance, for example to dampen unwanted oscillations or to slow down switching transients. The two pull-up (PU) and pull-down (PD) transistors of the push-pull gate driver final stage enable separate control of the turn-on and turn-off transitions. Because of these two different paths, at least two different gate-loops (turn-on/pull-up and turn-off/pull-down gate-loops) are formed. Therefore, in the following the two different gate-loops (PU and PD) will be separately analyzed.

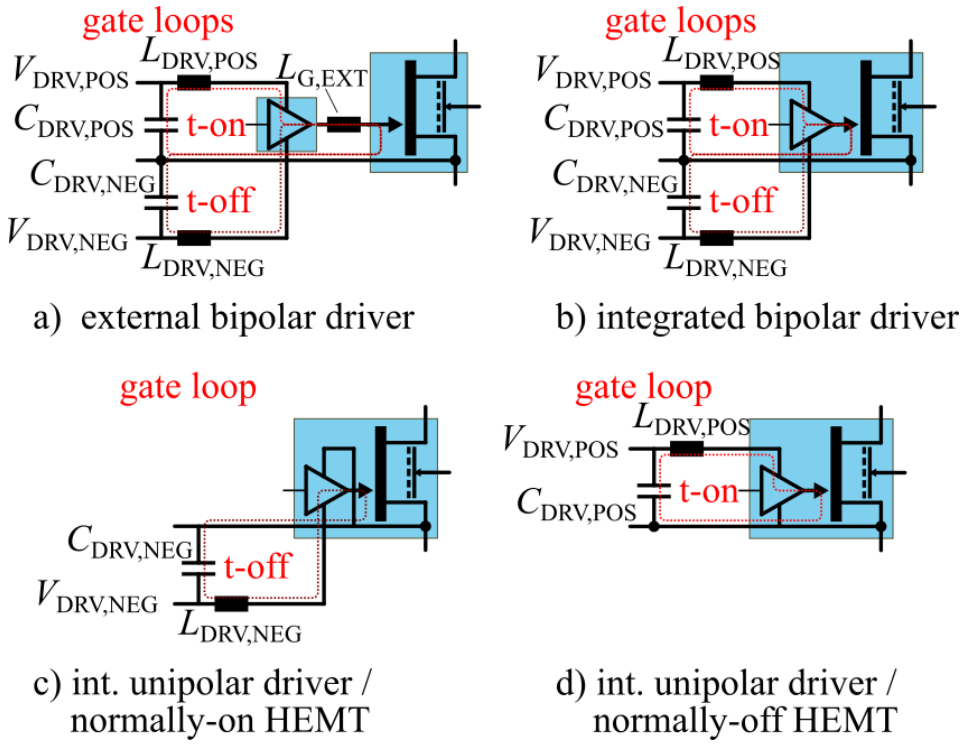

Figure 3.16: Gate-loops of a) external bipolar gate driver (two loops), b) integrated bipolar gate driver (two loops), c) integrated unipolar gate driver for normally-off transistor (only one turn-off loop), d) integrated unipolar gate driver for normally-on transistor (only one turn-on loop).

For a bipolar gate driver with two non-zero supply voltages ($V_{DRV,POS}$ and $V_{DRV,NEG}$) which are provided by external gate supply decoupling capacitors ($C_{DRV,POS}$ and $C_{DRV,NEG}$), the interconnect inductances sum up in the gate-loop to the total gate-loop inductance $L_{G,PAR}$

$$L_{G,PAR} = \begin{cases} L_{DRV,POS} + L_G + L_{CS} & \text{turn-on / pull-up} \\ L_{DRV,NEG} + L_G + L_{CS} & \text{turn-off / pull-down.} \end{cases} \tag{3.30}$$

The following analysis of the different partial inductance contributions of the gate-loops provides insight to derive measures for the reduction of the parasitic gate-loop inductance.

Unipolar and Bipolar Gate Drive: Depending on the gate driver voltage requirements of the main power transistor, more or less components are required in the gate-loops, potentially increasing the parasitic gate-loop inductance: While the main power transistor and either the pull-up or pull-down transistor are always part of the gate-loops, an additional (external) capacitor to provide the gate driver supply voltages is only required for non-zero supply voltages. If the main power transistor requires bipolar driver supply voltages, two external capacitors are required (one in the PD and one PU gate-loops). If the main power transistor can be driven with a unipolar supply voltage, only one external capacitor is required, because the zero voltage can be realized without a discrete component, but instead by a direct on-chip connection. This is the case for a normally-off transistor with positive threshold voltage if the off-state can be realized with zero

turn-off voltage $V_{\mathrm{DRV,NEG}} = 0\,\mathrm{V}$; and for a normally-on transistor with negative threshold voltage if the on-state can be realized with zero turn-on voltage voltage $V_{\mathrm{DRV,POS}} = 0\,\mathrm{V}$. These two unipolar driver configurations are shown in Fig. 3.16c-d. From the figure it is clear that despite the monolithic integration still an external critical interconnection to at least one gate supply capacitor is required. As a consequence, also for the monolithic power ICs a careful power module design with low-inductive loops to the supply capacitors is required. The monolithic integration of the gate driver does not fully eliminate the parasitic gate-loop inductance, but allows a significant reduction due to less external required interconnections.

Common-Source Inductance: The so-called common-source inductance L_{CS} results if the gate driver return path to the source of the main power transistor is realized by connection to an external source terminal of the main transistor. In this case, the power-loop and gate-loop share the common parasitic inductance L_{CS}, and fast current change in the power-loop will also directly affect the gate-loop. The common-source inductance is significantly reduced by utilizing a second separate source terminal (also called source-sense SS or Kelvin-source) of the transistor to connect the current return path of the driver stage. This approach has even been adopted for conventional vertical power transistors, which are available in 4-pin packages with an additional SS terminal. A source-sense terminal is always used in this work, such that L_{CS} is not an issue and negligibly small. It is therefore also not shown in the schematics.

On-Chip Gate Interconnect Inductance The gate interconnect inductance L_{G} results from several origins: If a discrete (external) gate driver is used, the interconnection between the gate driver and the power transistor causes additional parasitic inductance (for example by bond-wires, or PCB traces). This interconnect inductance is significantly reduced by a monolithic integrated gate driver which avoids chip-to-chip interconnects. Fig. 3.16b shows a GaN power IC which combines the gate driver and power transistor in a single chip, avoiding the external interconnection between the driver and gate. However, it should be noted that also a monolithic integrated driver stage has to be routed on-chip and connected to the main power transistor. If this interconnection is realized by thin metal on-chip traces across a large-area GaN IC, then L_{G} is still relevant and not zero. This work quantifies the on-chip inductance of the pull-up and pull-down transistor by electro-magnetic simulations of the monolithic circuit layout. Simulated up to the respective pads of the ICs as interface to gate supply capacitors, the on-chip parasitic inductance of the pull-up and pull-down driver transistors with on-chip wiring amounts to 1.8 nH and 0.9 nH, respectively. Despite the monolithic integration, this on-chip inductance is not negligible and surprisingly high. The cause of this on-chip inductance is twofold: First, the IC design uses several separate chip areas to realize the driver and main power transistor, which are then interconnected by thin on-chip traces. This on-chip inductance can be further reduced by improved placement of the driver within the IC, or by a distributed layout, where each finger of the main power transistor has a dedicated part of a distributed gate driver layout. Further reduction of on-chip inductance is possible by applying design methods which were previously used for external circuits and PCBs also for the IC design. For example, a parallel plate-like routing strategy instead of the used thin wires will reduce on-chip parasitic inductance.

The gate supply inductance $L_{\mathrm{DRV,POS}}$ and $L_{\mathrm{DRV,NEG}}$ include the interconnection from the (integrated) driver to the required external supply capacitors.

Fig. 3.17 shows a layout of the used GaN IC with two dedicated areas for the pull-up and pull-down driver transistors. The third visible area between the two driver transistors is a third transistor similar to the pull-down transistor and not used in this work. The driver circuit is monolithic integrated, but still separated from the main power transistor. The gate-loop is formed by the on-chip connection of the driver transistors to the gate (G) of the main power transistor, and a return connection with an on-chip source-sense (SS) contact. On the other side, the driver transistors are routed to pads, which serve as interface to two external bipolar supply capacitors $C_{\mathrm{DRV,POS}}$ and $C_{\mathrm{DRV,NEG}}$. To give a quantitative idea of the on-chip parasitic inductance, several partial interconnections are calculated based on transmission line models. The calculation include a current return path which is arranged co-planar to the traces. A differential calculation at one side of the traces with the other side short-circuited is carried out, which gives the parasitic inductance value which is relevant for the loop inductance. In the insets in Fig. 3.17 for both the pull-up and pull-down layout several structures are calculated. Some of the structures are simulated twice, but with different current return paths and different orientation. From these calculations, it is obvious that the long but thin interconnection from the pull-up transistor to the main power transistor with more than 1 nH is a bottleneck in the design, which can be avoided by different or distributed placement of the driver transistors. The driver transistors themselves are also large-area devices, and they contribute ≈ 0.4 nH. This self-inductance of the transistors could be further reduced by down-scaling of the driver transistors. The gate-to-drain distance of the driver transistors is more than double than required for for the low-voltage requirement of the driver. Since the parasitic inductance values in the insets of Fig. 3.17 consider some structures twice, a full IC layout electro-magnetic simulation was carried out. From this simulation, the total on-chip parasitic inductance of the drivers, as seen from the interface pads as differential port, was extracted as 1.8 nH (pull-up) and 0.9 nH (pull-down).

External Gate Supply Capacitors with Interconnection: Also the capacitors themselves have a geometry which further increases $L_{\mathrm{DRV,POS}}$ and $L_{\mathrm{DRV,NEG}}$. The required external interconnect of the GaN IC to the driver supply capacitors also increases the parasitic inductance. Placement of the gate supply capacitors as close as possible to the driver, and utilization of low-inductive capacitor packages enable a reduction of this parasitic inductance. Fig. 3.18 shows the GaN IC assembled on a power module with gate supply capacitors and bond wires for interconnection. Exemplarily two small surface-mount capacitor packages are shown in a cross-section. If multi-layer ceramic capacitors (MLCC) are used, small package dimensions (such as 0201 SMD package or smaller) should be used to avoid a high distance from the internal plate capacitances to the interconnect pads. This work also uses silicon chip capacitors (Si-Caps) which have a reduced parasitic series inductance compared to the MLCC capacitors, because the capacitance in the Si-Caps is realized close to the surface of the chips which allows a flip-chip assembly with very low interconnect inductance.

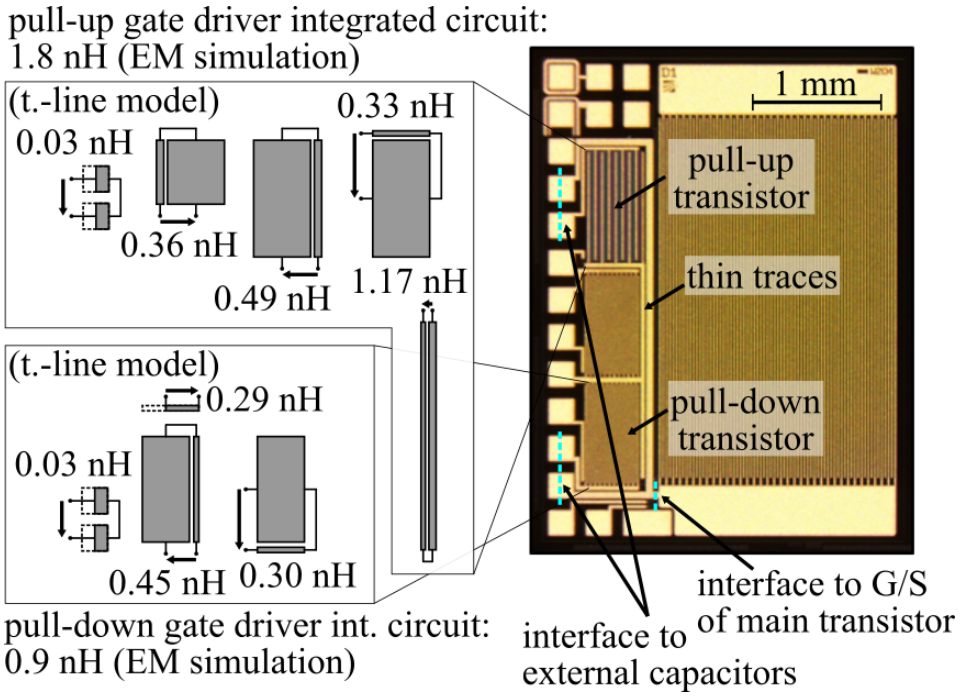

Figure 3.17: On-chip parasitic gate-loop inductance from coupled interconnect traces and extensive geometry of the transistors. L_{PAR} [nH] is extracted from transmission-line models, using the the GaN-on-Si layer stack as substrate.

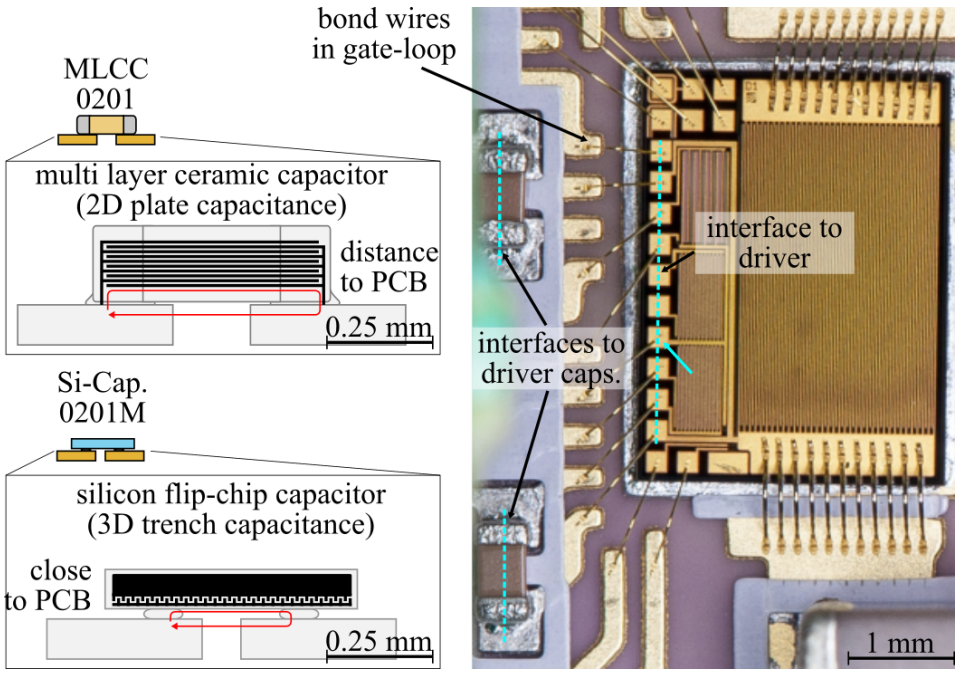

Figure 3.18: Cross-sections of multi-layer ceramic capacitors and Si-chip capacitors with additional parasitic loop inductance.

3.5.2 Monolithic Integrated Half-Bridge

In a typical power converter which is based on a half-bridge power circuit, the external dc voltage V_{DC} is provided by a dc-link capacitor C_{DC}. Since C_{DC} is part of the critical

power-loop, the interconnection of a the half-bridge transistors to the dc-link contributes a parasitic dc-link interconnection inductance $L_{\mathrm{DC,Con.}}$. The (high-voltage) external dc-link capacitor itself has a parasitic inductance $L_{\mathrm{DC,Cap.}}$ due to the capacitor geometry. The conventional way to realize a half-bridge is to series connect two power transistors. This series-connection of two power transistors and the interconnections contributes to the parasitic power-loop inductance.

Discrete half-bridge: A discrete half-bridge with two separate transistors contributes parasitic inductance: The drain-side interconnection from the used packaging technology (for example bond-wires) contributes the drain inductance L_{D}, and the source-side interconnection contributes the source inductance $L_{\mathrm{CS}} + L_{\mathrm{S}}$. Here L_{CS} is the common-source inductance, which is part of both the gate-loop and power-loop if no source-sense connection of the driver is used. As already discussed, this work uses only ICs with source sense terminals for the gate driver such that $L_{\mathrm{CS}} = 0\,\mathrm{nH}$, and L_{CS} is not further considered. Due to the large-area geometry of the power transistors, the devices in on-state themselves are similar to a short conductive trace. The geometry of the ICs is described by the IC parasitic inductance L_{IC}. From electro-magnetic simulations of the GaN IC on a carrier power module, the large-area layout of the main power transistor adds around $L_{\mathrm{IC}} \approx 0.5\,\mathrm{nH}$. Fig. 3.19 shows the GaN IC and a cross section through the main power transistor, where the large distance from the drain and source pads, as well as the isolating GaN buffer layer on low-resistivity Silicon is visible, which together form the parasitic inductance L_{IC}.

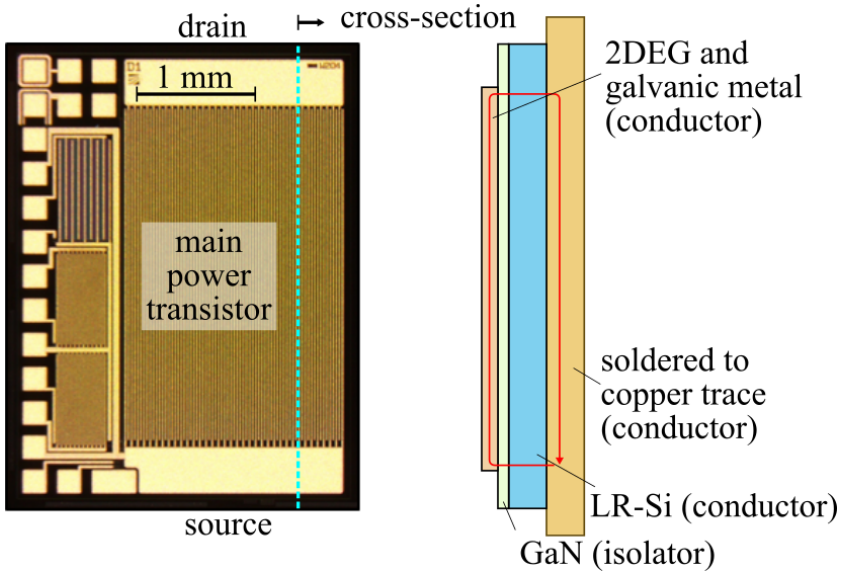

Figure 3.19: On-chip parasitic inductance L_{IC} from the large-area geometry of the main power transistor.

This parasitic inductance can be reduced by changing the aspect ratio of the large-area transistor layout. Instead of the $2 \times 3\,\mathrm{mm}^2$, which is longer than wide, the same active area could be realized for example on a chip area of $3 \times 2\,\mathrm{mm}^2$ or $1.5 \times 4\,\mathrm{mm}^2$. This reduction of the length and increase of width will reduce L_{IC}.

In total, the power-loop inductance of a discrete half-bridge converter is

$$L_{\mathrm{P}} = 2(L_{\mathrm{IC}} + L_{\mathrm{D}} + L_{\mathrm{S}} + L_{\mathrm{CS}}) + L_{\mathrm{DC,Cap.}} + L_{\mathrm{DC,Con.}} \tag{3.31}$$

Fig. 3.20a shows a schematic of a discrete half-bridge with dc-link capacitor and the series-connected parasitic inductance are marked. In a half-bridge converter the switch-

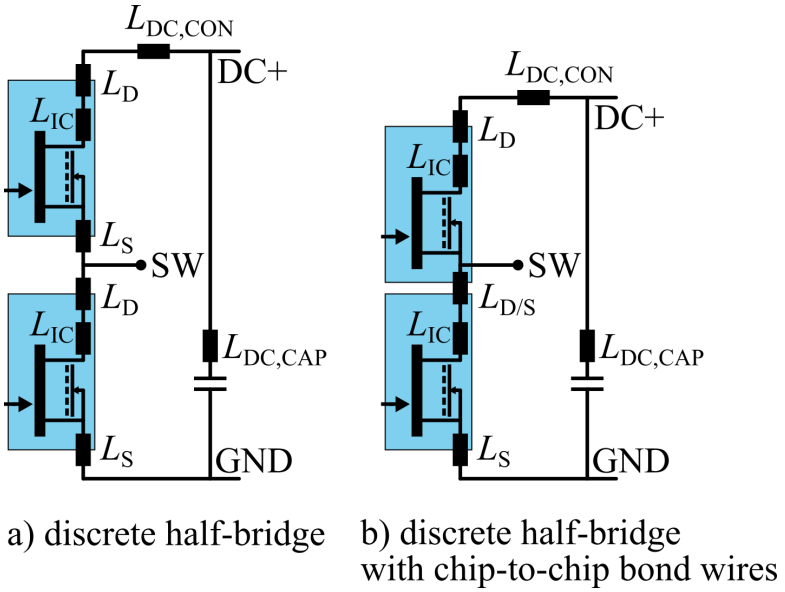

Figure 3.20: Schematic of discrete half-bridge with parasitic inductances in the power-loop. a) Conventional interconnect. b) Chip-to-chip interconnect around the switch-node.

node has to be externally accessible in order to connect a power inductor. Typically a total of four chip-to-board interconnects (bond-wires) with a parasitic inductance of $2(L_D + L_S)$ are used. From this the first approach to reduce the parasitic inductance in the power-loop is derived: Instead of the two chip-to-board interconnections around the switch-node, it is possible to place the transistor in a way to realize a direct chip-to-chip interconnection around the switch-node. This configuration is shown in Fig. 3.20b. Now the two bond-wire series-connections $(L_D + L_S)$ around the switch-node are replaced by a single bond-wire interconnection. This cuts the part of the parasitic inductance around the switch-node approximately in half $L_{D/S} \approx (L_D + L_S)/2$. However, independent of the discussed layout around the switch-node, still two additional interconnects to the dc-link capacitor are required. Fig. 3.21a shows a conventional discrete half-bridge assembly with bond-wires to realize the schematic from Fig. 3.20a. Fig. 3.21a shows the improved discrete half-bridge assembly with bond-wires and chip-to-chip connection around the switch-node to realize the schematic from Fig. 3.20b. In later sections the two interconnection schemes will be referenced by the number of series connected interconnects in the power-loop as "3×" and "4×".

Monolithic half-bridge: A further reduction of the parasitic inductance is possible by monolithic integration of the half-bridge. However, still external interconnections to the dc-link capacitor are required. Fig. 3.22a shows a half-bridge circuit using a monolithic half-bridge, where both half-bridge transistors are realized on the same chip. If the two transistors are not connected at the switch-node on-chip (Fig. 3.22a) then the improvement is small, because still two chip-to-board interconnections $(L_D + L_S)$ are required around the switch-node (indicated in Fig. 3.22a). Only if the high-side and low-side transistor connection is formed already on-chip by connection of both transistors,

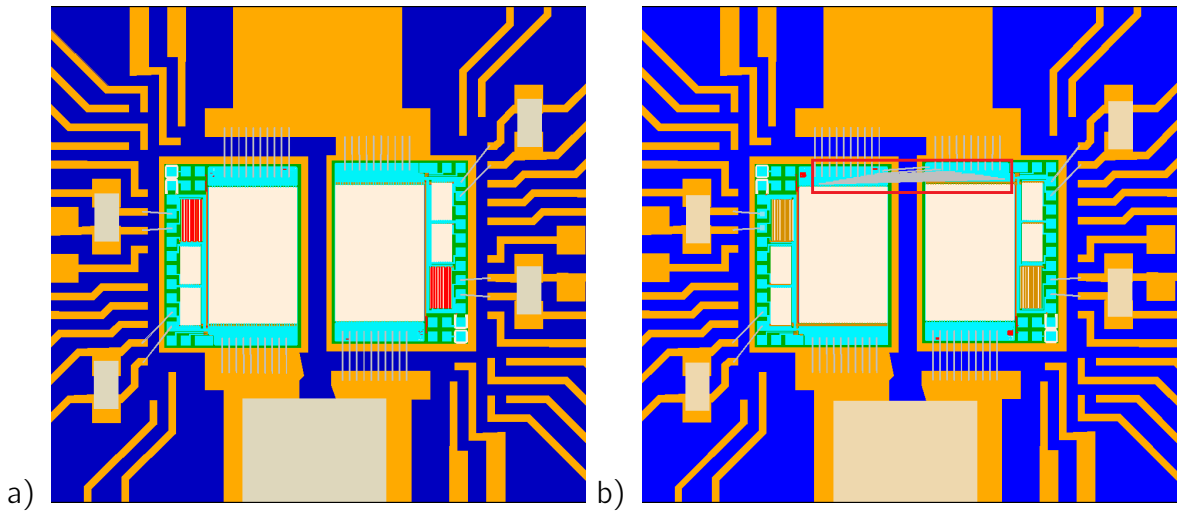

Figure 3.21: Layout of discrete half-bridges on ceramic substrates with gate-loop and power-loop capacitors. a) Conventional interconnect. b) Chip-to-chip interconnect around the switch-node (marced red).

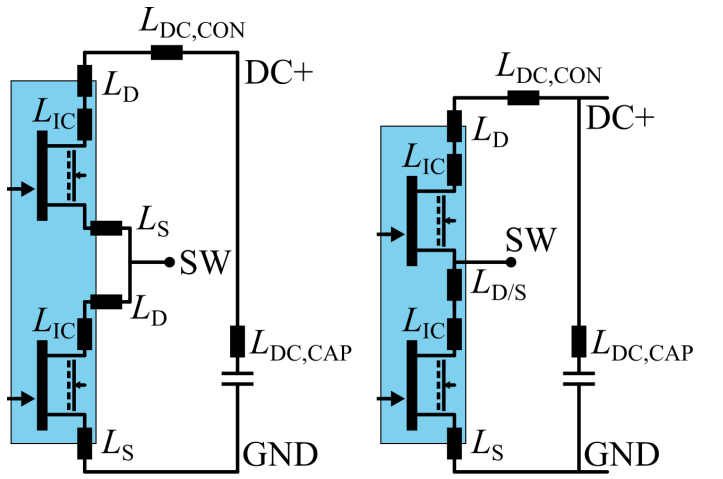

Figure 3.22: Schematic of a monolithic half-bridge with parasitic inductances in the power-loop. a) Two monolithic half-bridge transistors without interconnect. b) On-chip interconnect around the switch-node.

then the external interconnections around the switch node are avoided and reduced to $L_{D/S} < (L_D + L_S)/2$, which is lower than the chip-to-chip assembly of a discrete half-bridge due to lower distance between the high-side and low-side device, and also due to the avoidance of external bond-wires. The benefit of the monolithic integrated half-bridge thus is highest if the two half-bridge transistors are already connected on-chip, as shown in Fig. 3.22b. Fig. 3.23a shows the layout of the monolithic power IC, where a half-bridge is monolithic integrated, but the high-side and low-side devices are not yet connected on-chip. Fig. 3.23b shows the same layout, extended by an on-chip connection around the switch-node. Even with this layout, still the interconnections from the high-side drain and the low-side source to the external dc-link capacitor remain. Fig. 3.24

shows two power module assemblies on a ceramic substrate where these at least two bond wire interconnects to the dc-link capacitor are visible (in the middle at the bottom of the figures) . Fig. 3.24a uses a monolithic half-bridge without on-chip interconnect around the switch-node, and Fig. 3.24b uses a monolithic half-bridge layout with on-chip interconnect around the switch-node.

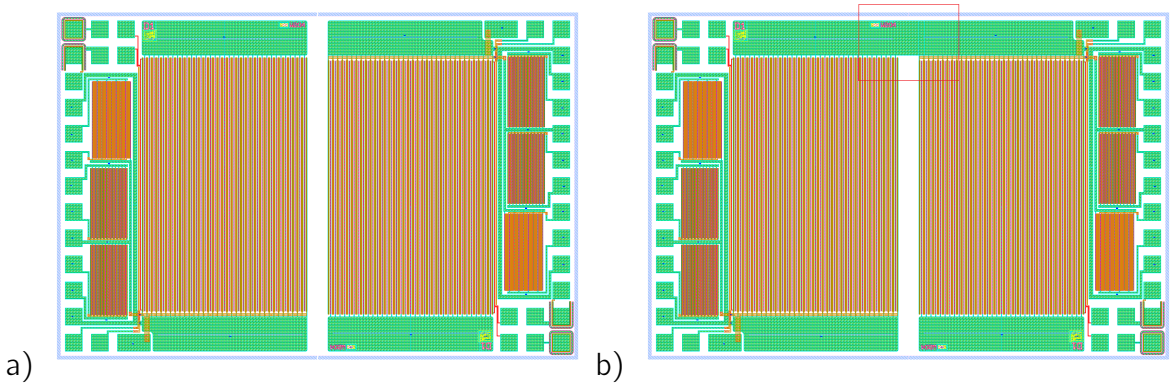

Figure 3.23: GaN power IC layout with monolithic half-bridge and gate drivers. a) IC layout without half-bridge transistor interconnect. b) On-chip half-bridge transistor interconnection (marked red).

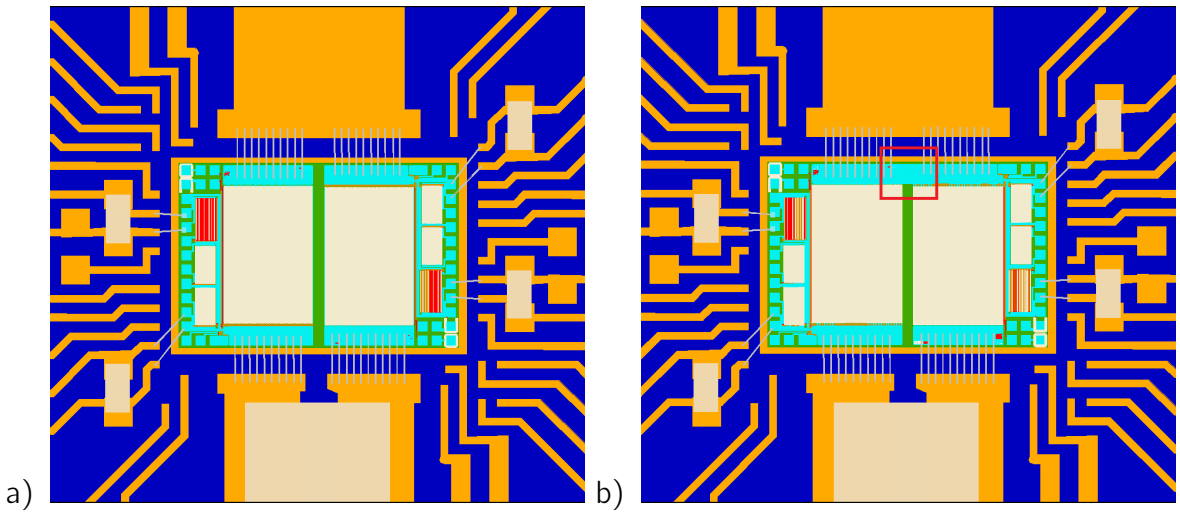

Figure 3.24: Layout of monolithic half-bridges on ceramic substrates with gate-loop and power-loop capacitors. a) The two monolithic half-bridge transistors are externally interconnected. b) On-chip interconnect around the switch-node.

3.5.3 Package-Level Integration using PCB-Embedding

In the previous sections it was shown that monolithic integration of the gate driver and half-bridge enables a reduction of parasitic inductance. However, it was also shown that in both cases still external decoupling capacitors and thereby also the interconnection to external capacitors is required. The monolithic integration alone thus cannot completely eliminate parasitic inductance. For clean switching of the GaN power ICs used in this work, though highly integrated, still a low-inductive packing is required. Otherwise, the

switching behavior will still be limited by the external interconnect parasitic. To address this issue, a second integration approach (beside monolithic integration) is possible to reduce parasitic inductance: Conventional bond-wire assembly is replaced by a PCB-embedding technique. PCB-embedding of the GaN ICs allows to replace bond-wire chip-to-board connections with micro-via interconnections inside the PCB. With PCB-embedding it is possible to integrated a GaN Power IC within a multi-layer PCB and to establish all the required interconnects to the capacitors already in the same package. For a low-inductive assembly, also the placement of the capacitors is critical. In addition to monolithic integration and PCB-embedding also the capacitors are included in the package design. Compared to the bond-wire assembly, where the bond-wires limited the placement of the capacitors, with the PCB-embedded package it is possible to place the capacitors next to or even directly on the package above the ICs. In the PCB embedded design, this improved placement of the gate supply capacitors is realized, and in Fig. 3.25 it is visible how the pull-down capacitors are placed directly above the ICs and the pull-down capacitor are placed directly next to the edge of the ICs.

The result of the combined approaches are monolithic integrated GaN power ICs in a PCB-embedded package with on-package gate and dc-link capacitors. This approach and results were also published in [92]. PCB-embedding is a variation of a PCB manufacturing process, and is also known to be used for packaging of commercial discrete GaN HEMTs (for example from GaNSystems), as well as other active and passive components (resistors, capacitors, inductors, Si ICs).

To compare the effect of the different integration schemes on parasitic gate-loop and power-loop, PCB-embedded packages were designed similar to the already shown bond-wire assemblies. Fig. 3.25a shows the layout of a PCB-embedded discrete half-bridge with on-package capacitors. Fig. 3.25b and Fig. 3.25c show the layouts of PCB-embedded monolithic half-bridges, without and with on-chip switch-node interconnect, respectively.

3.5.4 Quantified Reduction of the Parasitic Inductance

This section now quantifies the effect of combinations of the already discussed integration approaches on the reduction of parasitic gate-loop and power-loop inductance. Electro-magnetic simulations of complete half-bridge packages with one or two GaN ICs and interconnections up to the gate and dc-link capacitors are carried out. For computational efficiency, 2.5D simulations using the Method-of-Moments are used for layout simulations [93] with the tool "Advanced Design System" (ADS) from Keysight Technologies. The full IC layout of the with all transistor channels in the on-state is included in the simulation. The vertical layer stack of the GaN IC is merged into a small number of equivalent layers prior to the simulation. For example, the galvanic top metal layer, on-chip via structures and conductive layers down to the 2DEG are merged to reduce the complexity of the simulation. The following parameters are varied in the simulations:

Monolithic Integration: 1. Two separate $3\times4\,\mathrm{mm}^2$ GaN ICs are arranged as a discrete half-bridge. Each IC has an integrated gate driver final stage. 2. A single $6\times4\,\mathrm{mm}^2$ GaN IC which integrates the half-bridge and the drivers is used. 3. For the monolithic half-

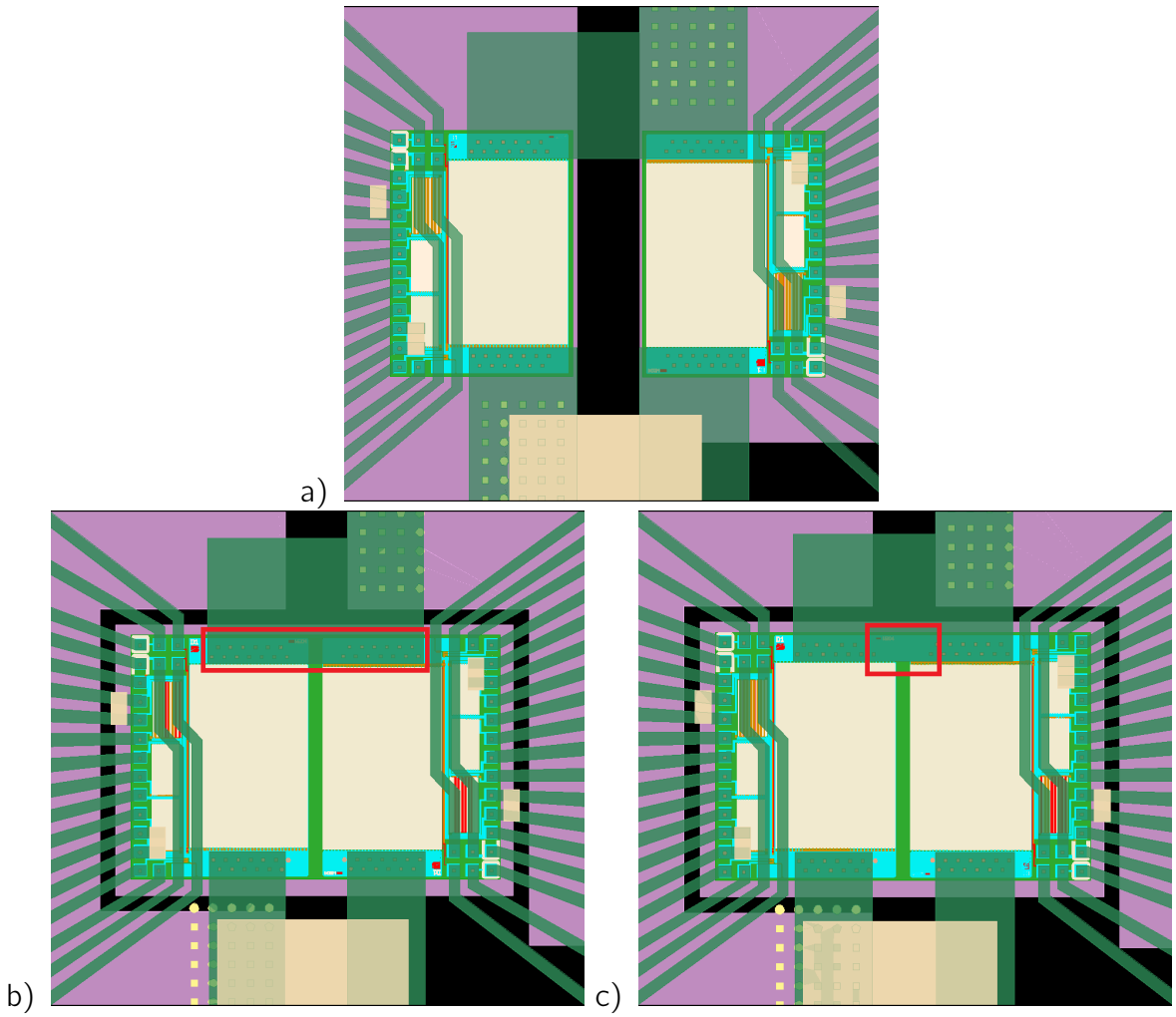

Figure 3.25: Layout of half-bridges in a PCB-embedded package with on-package gate-loop and power-loop capacitors. a) Discrete half-bridge. b) Monolithic half-bridge without on-chip switch-node interconnection c) Monolithic half-bridge with on-chip switch node interconnection.

bridge two layout variations are considered: One with and one without on-chip connection of the half-bridge around the switch-node (see Fig. 3.23).

Assembly: 1. A conventional bond-wire assembly with bond-wires on a ceramic power module (named "DCB"). 2. A PCB-embedded package without bond-wires (named "Embedded"). Both variants use gate and dc-link capacitors either on the DCB module or on the PCB-embedded package.

Bond-wires: This parameter is only relevant for the DCB assembly. 1. Bond-wires are only used for chip-to-board connections, a total of four series connected bond wire arrays is used to realize the power-loop (named "4×", Fig. 3.21a). 2. To form the half-bridge around the switch-node, chip-to-chip bond-wires between the low-side drain and high-side source are used (named "3×", Fig. 3.21b).

Based on these parameters, a total of seven layouts are simulated. The four DCB-based layouts are shown in Fig. 3.21 and Fig. 3.24. The three PCB-embedded package based layouts are shown in Fig. 3.25.

To quantify the parasitic inductance of the gate and power-loops, differential ports are placed at the terminals of the gate and dc-link capacitors instead of the capacitors. Since the transistors are co-simulated in on-state, the differential ports "see" closed loops, where the simulated impedance includes the very low resistance of the transistors in on-state and also the parasitics of the interconnects. Since the geometry of the packages also has capacitive elements, a simulation frequency of 100 MHz was used. At this frequency the parasitic inductances dominate the imaginary part of the simulated impedance and the capacitive contributions can be neglected. To extract the impedance, the simulated S-parameters were transformed to Z-parameters. Ports at the pull-up and pull-down gate capacitors, as well at the dc-link capacitor are used to simulate the two gate-loop and one power-loop parasitic inductances.

Tab. 3.2 shows the simulated parasitic inductance values. While in this work for the sake of a first-principle comparison only the total gate-loop and power-loop inductance are discussed, the author has published a more detailed analysis with a breakdown of the total loop inductance into the individual series-connected parasitic contributions for a discrete half-bridge on DCB and in a PCB-embedded package in [92].

assembly half-bridge bonds	**DCB discr.** 4×	**DCB discr.** 3×	**Embedded discr.**	**DCB mono.** 4×	**Embedded mono.**	**DCB mono.** 3×	**Embedded mono.**
Power-loop	2.64 nH	2.19 nH	2.22 nH	2.57 nH	1.78 nH	1.82 nH	1.53 nH
Gate-loop PU	3.40 nH	3.42 nH	1.94 nH	3.49 nH	1.94 nH	3.47 nH	1.96 nH
Gate-loop PD	3.06 nH	3.09 nH	0.85 nH	3.10 nH	0.84 nH	3.10 nH	0.84 nH

Table 3.2: Parasitic loop inductances * switch-node closed on-chip. ^{C}: capacitive.

3.5.5 Discussion of Low-Inductive Integration Approaches

This section discusses the results from Tab. 3.2.

Effect on power-loop Inductance: The power-loop inductance of 2.64 nH of the discrete half-bridge on a DCB module with conventional bond-wire configuration (DCB, discr., 4×) is used as a reference. Replacing the two discrete half-bridge ICs with a monolithic half-bridge IC where only the half-bridge transistors are on the same chip, but not connected on-chip, reduced the simulated power-loop inductance only insignificantly to 2.57 nH (DCB, mono., 4×). This variation shows that monolithic integration itself is not a guarantee for low parasitic inductance, but further layout adjustments are required. The low reduction of the parasitic inductance in this first variation is because only the distance between the half-bridge IC is changed, but not the half-bridge interconnection scheme. The two series-connected bond-wire arrays to form the switch-node connection still fully contribute to the power-loop inductance. By additional connection of the

half-bridge transistors already on-chip, still assembled with bond-wires, shows a higher reduction of parasitic inductance to 1.82 nH (DCB, mono.*, 3×). This shows that not the monolithic integration of the half-bridge transistors itself is the cause for the reduction of the power-loop inductance, but instead mainly the modified interconnection scheme which avoids two series-connected bond-wire arrays is the main cause. Based on this finding, this work also adapts the identified improved interconnection scheme as an approach for power-loop inductance reduction to a discrete half-bridge: The discrete half-bridge assembly is also simulated with a direct chip-to-chip bond-wire interconnection (DCB, discr., 3×). This improved interconnection scheme for a discrete half-bridge shows still a significantly reduced power-loop inductance of 2.19 nH compared to the original layout.

The PCB-embedding of the discrete half-bridge reduces the simulated power-loop inductance to 2.22 nH (Embedded, discr.). Even though this is reduced compared to the original discrete DCB assembly, it is similar and even slightly higher than the DCB-based assembly with the improved chip-to-chip switch-node bond-wire connection (2.19 nH). The similarity and even slight increase is explained by the fact that for the PCB-embedding due to voltage isolation concerns the discrete ICs were separated by over 2 mm, whereas on the DCB a smaller distance was realized. The smaller IC separation on the DCB module was possible because after assembly the module was covered with highly isolating Silicone-based insulating varnish. The distance of the ICs in the PCB-embedded package is avoided by integration of a monolithic half-bridge. PCB-embedded and monolithic integrated half-bridges without and with the on-chip switch-node connection are simulated and show a further power-loop inductance reduction to 1.82 nH and 1.53 nH.

Effect on Gate-Loop Inductance: Since in all variations always GaN ICs with monolithic integrated gate drivers are used, the variation of the half-bridge layout has no effect on the gate-loop parasitics. Only two main cases (bond-wires or PCB-embedding) remain and are compared. For the DCB-based modules, gate supply capacitors were placed as close as possible to the GaN ICs, but still separated by the bond-wires in the gate-loop (see Fig. 3.21 and Fig. 3.24). The simulated pull-up gate-loop inductance for the bond-wire assemblies is ≈ 3.4 nH, and the pull-down gate-loop inductance ≈ 3.1 nH. These values also include the on-chip interconnects which contribute 1.8 nH and 0.9 nH to the pull-up and pull-down loops as discussed in Sec. 3.5.1. For the PCB-embedded packages, the parasitic gate-loop inductance is significantly reduced to ≈ 1.95 nH (pull-up, reduction by 43%) and to ≈ 0.84 nH (pull-down, reduction by 73%). If the self-inductance from the pull-up transistor is subtracted from the total gate-loop inductance, the difference of only 150 pH can be assigned to the contribution by the PCB-embedding. The total pull-down gate-loop inductance of the PCB-embedded module is slightly lower than the previously stated simulated self-inductance of only the pull-down transistor $0.84\,\text{nH} < 0.9\,\text{nH}$. While it seems incorrect that the PCB-embedded pull-down transistor has a lower inductance than just the transistor, there is an explanation: In the PCB-embedded layout, the pull-down supply capacitor is placed directly above the pull-down transistor, separated only by the micro-vias which connect the IC to the capacitor. For the attachment of the capacitor, the PCB package has conductive pads and traces

to solder the capacitor. The resulting pull-down gate-loop layout is now similar to a broadside coupled trace structure with a very small distance (thickness of a thin isolating PCB layer) between the traces. It is well known that a broad-side coupled trace structure has lower inductance than the self-inductance of a single trace.

Summarized, the combination of the monolithic half-bridge integration, the PCB-embedding as package-level integration and on-package dc-link capacitors allowed a reduction of the parasitic power-loop inductance by 42% and a reduction of the gate-loop inductance between 43% and 73%, both compared to the original DCB-based and discrete layout with bond-wires.

3.6 Experimental PCB-Embedded Discrete Half-Bridge with Drivers and On-package Capacitors

The PCB-embedded package with an integrated discrete half-bridge and on-chip capacitors as already shown and simulated in Fig. 3.25a is realized and presented in this section. The power module combines the discussed approaches to reduce the parasitic inductances: First, a monolithic integrate gate driver and transistor is used. Next, the PCB-embedding avoids bond-wire interconnect inductance. Last, the layout of the package already provides solder pads to close the gate-loop and power-loop by on-chip decoupling capacitors.

Fig. 3.26 shows the assembled package and an X-ray photo. The large capacitor is the dc-link capacitor. Furthermore in the middle of the photo, very small Si-chip capacitors as gate decoupling capacitors are positioned directly above the monolithic gate driver stages. Further gate supply supply capacitors are placed on the pads on the edges of the package.

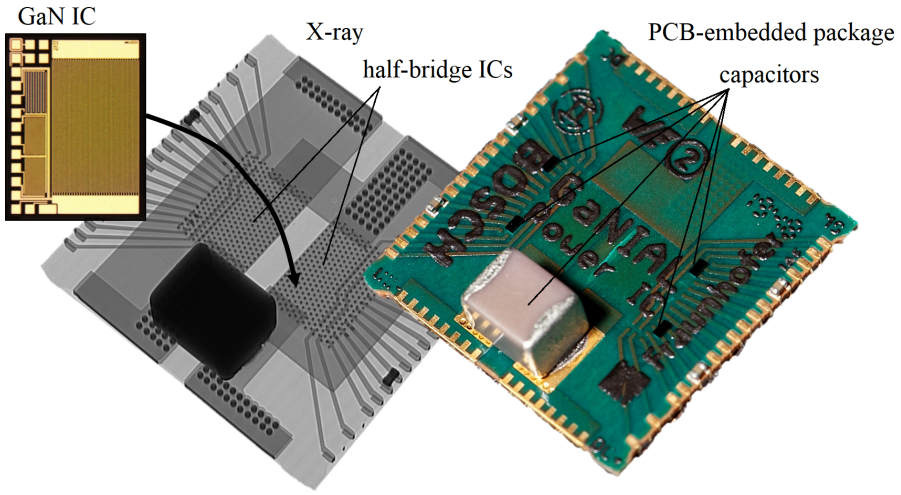

Figure 3.26: Photo and X-Ray of PCB-embedded discrete half-bridge with monolithic gate drivers and on-package gate and dc-link capacitors.

The PCB-embedded half-bridge with drivers and capacitors is characterized in pulsed and continuous operation. Fig. 3.27 shows switch-node voltage waveforms at 380 V half-bridge operation without an inductor. In this operation, both the high-side and low-side

transistor are hard-switched with high slew-rates. Despite the high voltage slew-rates above 120 V/ns, only low overshoot (9%) and undershoot (-12%) was measured. These measurements shows that clean and stable voltage transitions at high slew-rate switching are possible with low overshoot, by combination of monolithic circuit integration, advanced packaging and on-package gate and dc-link capacitors. This combination allows to exploit the intrinsic switching speed of the used GaN-on-Si power technology.

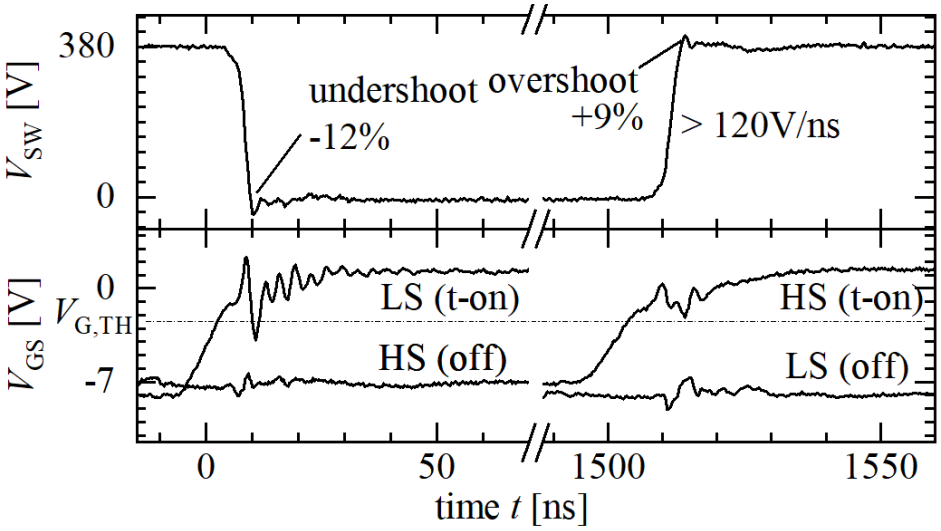

Figure 3.27: Clean hard-switching switching voltage waveforms at 380 V with low overshoot despite high voltage slew-rate switching.

To compare the achieved clean switching characteristics with conventional packaging approaches, the author published a comparison of the presented results with a conventional DCB and bond-wire based power module in [92]. For comparable switching conditions in [92] an overshoot of +21% and undershoot of -18% was reported, which is in contrast to this work's approach with +9% and -12% a significant improvement of the switching characteristic.

3.7 Summary and Conclusion

This chapter investigated the research questions:

- How does parasitically increased inductance in the gate-loop or power-loop influence switching speed and overshoot?

Theoretically, parasitic inductance in the gate or power-loop of power modules can cause up to 100% overshoot voltage and severe oscillations. However, this is only the case for instantaneous and infinitely fast voltage switching. Practically, the switching speed is limited by the intrinsic resistive-capacitive elements of the used transistors. For limited voltage slew-rate switching, a more detailed analysis which takes the switching speed into account shows that by a small reduction of the switching time, it is possible to beneficially use the resonance of the parasitic inductance to cancel out overshoot voltages. If the switching speed is set to multiples of the overshoot-optimal switching

time, then the analysis shows that independent of the damping factor of the circuit, the overshoot is limited and reduced to below 8%. While it is intuitively understood that a reduction of the switching speed also reduces the overshoot, this work theoretically derived that the overshoot is not a monotonic function dependent on the switching speed, but instead local minima of overshoot exist. Experimentally, the local minima of overshoot were verified by a pulse setup, where the switching time was adjusted in very fine steps.

- How much do monolithic integration and advanced packaging of GaN power circuits allow a reduction of parasitic inductances?

Beside the switching time as a parameter to control overshoot voltages, improvements of the layout of a power module which reduce the parasitic inductance are also useful measures for clean voltage switching. Since the parasitic gate-loop and power-loop include external decoupling capacitors, even with monolithic integrated half-bridge and driver ICs, still a low-inductive interconnection to the external capacitors is required. Simulation of the parasitic inductance of switching cells with discrete and monolithic half-bridges in conventional bond-wire layouts shows that a side-by-side (but not on-chip interconnected) monolithic integration of two half-bridge transistors reduce the overall power-loop inductance in a bond-wire assembly only insignificantly (from 2.64 nH to 2.57 nH), if the external interconnection layout is not adapted. Instead, it was shown that the replacement of the four separate source and drain bond wire arrays an alternative chip-to-chip bonding schema around the switch-node allows a significant reduction of the power-loop inductance to 2.19 nH. The on-chip interconnection of the half-bridge transistors around the switch-node has a similarly significant effect: The parasitic power-loop inductance of the monolithic half-bridge with on-chip switch-node interconnection and bond-wire assembly was thereby reduced to 1.82 nH. This means that not the monolithic integration of half-bridge transistors on a single chip per se reduces the parasitic inductance, but that the on-chip interconnection of the half-bridge transistors contributes mostly to the reduction of parasitic inductance.

However, even for the investigated monolithic half-bridge with integrated gate drivers, both the power-loop and gate-loop parasitic inductance with optimized bonding scheme and on-chip interconnection of the half-bridge and drivers are still not negligible (1.82 nH power-loop and 3.4 nH/3.1 nH pull-up/pull-down gate-loop). The reason is that the monolithic integration of the active semiconductor circuits alone does not fully eliminate the external interconnections to the required gate-loop and power-loop decoupling capacitors. It is concluded that monolithic integration allows a reduction of parasitic inductance on-chip, but is not yet a comprehensive solution for power modules for actual converters.

For a further reduction of parasitic inductance, this work combines monolithic gate driver integration, PCB-embedding of the GaN half-bridge ICs and on-package flip-chip capacitors. With the resulting PCB-embedded power module, high slew-rate switching $> 120\text{V/ns}$ is experimentally demonstrated with a low overshoot of 9%. By the combination of monolithic power ICs and advanced packaging and on-package decoupling capacitors, the parasitic power-loop and gate-loop inductance are significantly reduced (here: to 1.53 nH and 0.84 nH in case of a PCB-embedded monolithic half-bridge, and

2.22 nH and 0.85 nH in case of a PCB-embedded discrete half-bridge, both with monolithic gate drivers).

The findings show that monolithic half-bridge and driver integration is not a guarantee for low-inductive and clean switching, because external interconnections to the decoupling capacitors still contribute significant parasitic inductance. The work's approach, to combine monolithic integration, PCB-embedding as an advanced packaging technology, and on-package capacitors, thus is a comprehensive solution to full switching potential of GaN ICs.

4 Parasitic Substrate-Loop Inductance and Related Instabilities

4.1 Problem and Approach

In the previous chapter, parasitic inductance in the gate-loop and power-loops in combination with the resistive/capacitive transistor behavior was analyzed using a purely passive RLC equivalent circuit approach. Event though voltage overshoot up to theoretically 100% in the worst-case was observed and discussed, the first occurrence of a peak overshoot voltage was assumed as the worst-case condition, since all subsequent peaks of the oscillating overshoot had a decaying envelope. Even though overshoot voltages can lead to undesired overvoltage, still the transient behavior was stable since the resistive part of the circuit was sufficient to dampen the oscillation and ultimately lead to a stable steady-state voltage. In contrast to the underdamped, but *stable* previously discussed switching behavior, assuming a passive RLC equivalent circuit, this chapter now takes the gain from the transistor as an active device into account. The channel (drain) current in the GaN HEMT is controlled by the gate-source voltage. By capacitive feedback, for example through the gate-to-drain capacitance, and in combination with parasitic inductance, the passive RLC-circuit equivalent circuit is not valid any more. Instead, the feedback has to be considered, and in the worst case the feedback causes an *instability* of the switching behavior, where after a first voltage overshoot the successive voltage waveform has an increasing envelope. The increasing oscillating energy and voltage amplitudes of an instability can lead to circuit destruction, and thus should be closely examined and avoided.

Instabilities caused by parasitic inductance in the gate-loop (Fig. 4.1a) or power-loop (Fig. 4.1b) of half-bridge circuits have been extensively discussed in literature [86, 94, 95, 96]. However, instabilities from the substrate as an additional terminal in lateral GaN HEMTs has not yet been investigated.

This work, for the first time exposes that the substrate-to-source termination (B=S) of lateral GaN-HEMTs as part of a half-bridge circuit forms a third critical loop, the substrate-loop. Since the lateral channel current of a GaN HEMT is not only controlled by the top-gate, but also through the substrate, oscillations of the substrate-to-source voltage can also cause instabilities, analogous to the well-known oscillations of the gate-to-source voltage. The results are partly published by the author in [97].

Research questions:

- How does the substrate termination as a third critical loop affect switching behavior and stability?

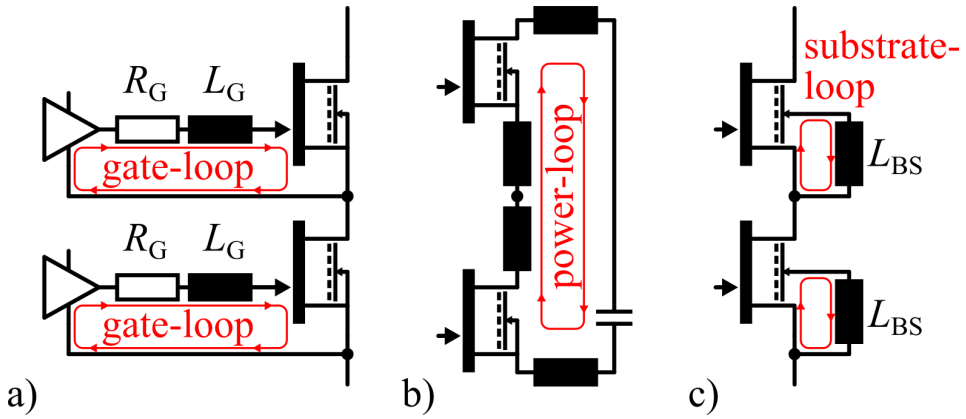

Figure 4.1: Parasitic Loops: a) Gate-Loop, b) Power-Loop, c) Substrate-Loop. © 2018 IEEE. Reprinted, with permission, from [97].

- How to reduce the substrate-loop inductance and avoid related instabilities?

Approach: Sec. 4.2 provides the theoretical background on gate-connected feedback loops. Sec. 4.3.1 carries out an equivalent circuit transformation to describe the half-bridge with parasitic substrate-loop inductance as a feedback amplifier. Sec. 4.4 then evaluates stability conditions to quantify for which combinations of circuit parameters and parasitic inductance values stability is achieved. Sec. 4.5 proposes a resistive damping method to avoid instability by the parasitic substrate-loop. The effectiveness of the approach is then experimentally verified in Sec. 4.6. Sec. 4.7 shows packaging and layout considerations to reduce the parasitic substrate-loop inductance.

4.2 Parasitic Inductance from the Substrate Termination

In the analysis of switching transients in Sec. 3.2 the transistor was considered as a controlled source which is active only during the switching transition and forces a voltage step or ramp during the transition. However, in a real transistor the current which is responsible for the voltage change is controlled by the gate-to-source voltage. A gate driver circuit is intentionally used to control the channel current. However, if the gate driver circuit is not tightly coupled to the internal gate and source nodes of the transistor, other coupling mechanisms can superimpose the internal gate-to-source voltage, resulting in unintentional modulation of the channel current. The non-zero gate driver resistance which is used to slow down the switching transition in order to avoid oscillations, the internal gate resistance from the gate finger metal, as well as the parasitic gate-loop inductance reduce the coupling of the gate driver to the gate and source nodes of the transistor. If other circuit nodes are more tightly coupled to the gate than the gate driver, controlability of the transistor current by the driver may be lost. If other gate-coupled nodes are part of the switched power-loop, feedback loops can result. In the worst case of positive feedback to the gate, the channel current of the main power transistor is unintentionally modulated by the feedback loop, such that the power-loop and gate-loop oscillations which were always decreasing in the passive RLC circuit (without feedback in Sec. 3.2), now actively gain more energy during each oscillation period than the

resistive part (for example the on-resistance of the power transistor, or gate resistance of the driver) of the loops dissipate. Oscillations with increasing envelope result. These instabilities can destroy the circuit if the increasing voltage and current envelopes exceed the operating area of the device. Furthermore, the well-defined conduction and switching periods which are required for dc-dc converter operation are no longer present.

One well-known coupling mechanism to the gate is the "Miller"-effect during switching transitions: A fast changing drain-to-source voltage with a high slew-rate $\frac{\mathrm{d}}{\mathrm{d}t}V_{\mathrm{DS}}$ causes a displacement current through the gate-to-drain capacitance C_{GD} (reverse "Miller" capacitance C_{RSS}). Depending on switching speed and the sign (direction) of the voltage change, the displacement current $I_{\mathrm{GD}} = C_{\mathrm{RSS}}\frac{\mathrm{d}}{\mathrm{d}t}V_{\mathrm{GD}}$ superimposes the gate drive current I_{G} to the effective current $I_{\mathrm{G,INT}} = I_{\mathrm{G}} + I_{\mathrm{GD}}$ which controls the gate voltage and thus the channel current. This capacitive "Miller" feedback itself in an ideal (purely capacitive, no parasitic inductance) switching cell does not cause instabilities, due to the negative feedback, but it even dampens the circuit. For example, during a turn-on transition where the gate driver tries to increase the gate voltage by supplying a positive gate charging current, the reverse feedback current through C_{GD} has an opposite sign, and thus reduces the effective internal gate charging current. It is common practice to include the "Miller" effect into the dimensioning of the gate driver circuit in order to set the switching speed to an intended slew-rate limited value.

However, as soon as there are inductive components in the circuit, due to the opposite phase compared to capacitive components, it is possible that positive feedback loops exist which cause unstable circuit behavior and ultimately circuit destruction if the feedback provides more gain than the natural damping of the circuit.

Previously in Sec. 3.2 the parasitic inductance of the gate-loop and power-loop was discussed. Both parasitic inductances can form a positive feedback to the gate and cause instabilities if the feedback circuit is underdamped. Furthermore it was already discussed that a common-source inductance from an overlap between the gate-loop and power-loop is avoided by a source-sense terminal for the driver, which is always used in this work to connect the gate driver. However, even with the source-sense terminal for the driver it is not yet ensured that all common-source inductance is avoided: As will be discussed in this chapter, the substrate-to-source termination also forms a parasitic loop which may form a common-source inductance. In this chapter thus the common-source inductance resulting from the substrate termination is discussed, whereas the already known common-source inductance resulting from the gate-loop and power-loop is already avoided and thus not further investigated.

To analyze the effect of non-zero gate-loop and power-loop inductance on stability of half-bridges, in literature oscillator theory is often used. For example, in [94] and [96] extensive studies are presented which derive stability conditions, and experimentally verify the predicted instabilities in half-bridges. In this chapter the oscillator theory and feedback amplifier analysis described in [94, 96] is adopted to substrate-related instabilities, and the root-locus stability criterion [98] is used.

For the first time, and extending the published state-of-the-art analysis of gate-loop and power-loop inductance, this chapter unveils the parasitic substrate-loop as a third parasitic loop which can cause instabilities and thus should be carefully considered during the design of transistors and power modules.

Fig. 4.2 shows a transistor with driver and indicates the gate-loop inductance L_G and the power-loop inductance L_P. A source-sense terminal is already used for the return path of the driver. In addition to these well-known parasitic loops, Fig. 4.2 also shows a substrate-to-source termination, which forms the substrate-loop as a third loop. The parasitic substrate-loop includes at least a dedicated parasitic substrate-loop inductance L_B, and can furthermore include a common-source inductance L_{CSB} if the power-loop and substrate-loop share part of the interconnects.

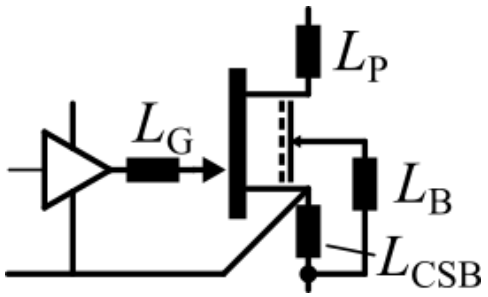

Figure 4.2: Transistor with driver and gate-loop inductance L_G, power-loop inductance L_P, substrate-loop inductance L_B and common-source inductance L_{CSB}, shared between the power-loop and substrate-loop.

4.3 Equivalent Feedback Amplifier

4.3.1 Circuit Transformation Method

Fig. 4.3a shows a simplified small-signal equivalent circuit of a GaN HEMT (here the low-side transistor) in a half-bridge, where the active low-side transistor's drain-to-source channel current I_D is controlled by the gate-to-source voltage V_{GS}. A parasitic substrate inductance L_B is shown, externally connecting the substrate to source. The six terminal-capacitances of the transistor, including the substrate capacitances which are required for this analysis, are also included in the circuit. The gate-loop includes a resistive element R_G (e.g. the gate-resistor), and the power-loop also has a resistive element R_{EP} (equivalent parallel resistance from the high-side transistor). The circuit in Fig. 4.3a is shown with L_B as the only parasitic inductive component in the half-bridge. This simplified case will be used in the following to demonstrate that despite zero gate-loop and power-loop inductance, non-zero substrate-loop alone is sufficient to cause instabilities. Despite this special case, a full equivalent circuit including gate-loop inductance L_G and power-loop inductance L_P, as well as common-source substrate inductance L_{CSB} is also analyzed in this chapter.

Fig. 4.3b shows the method to transform the circuit into an equivalent feedback amplifier. The substrate is eliminated by circuit transformation, such that only the gate node (which controls the channel current) and the drain-node remain. For this two-node amplifier circuit with an active source and feedback elements between the nodes the feedback amplifier stability analysis method is applied, similar to [94, 96].

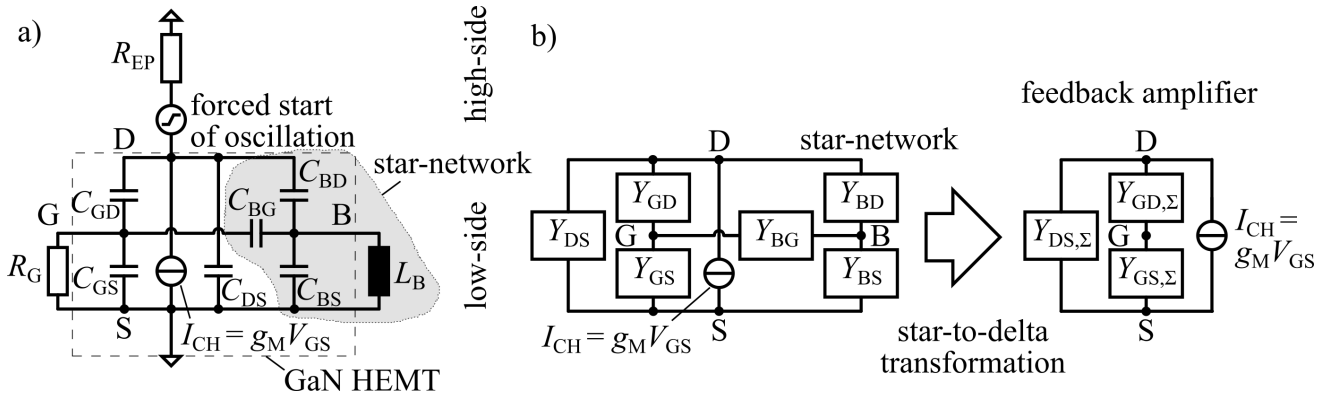

Figure 4.3: a) Equivalent small-signal circuit with parasitic substrate loop inductance, b) Simplified equivalent circuit c) equivalent feedback amplifier after star-to-delta transformation to eliminate the substrate node B.

4.3.2 Full Equivalent Circuit Transformation

Fig. 4.4 shows the full equivalent circuit which is analyzed. Instead of the simplified equivalent circuit from Fig. 4.3a, the extended full equivalent circuit which includes all investigated parasitic inductance (L_G, L_P, L_B, L_{CSB}) and already an additional resistive substrate-damping (R_B) resistor proposed and discussed later by this work. From the analysis of the full equivalent circuit, special cases can easily be derived by zeroing of the elements not to be examined. For example, the special case of the simplified circuit from Fig. 4.3a where a parasitic inductance L_B is only considered in the substrate-loop follows by zeroing of L_G, L_P, L_{CSB}, R_B in the following analysis.

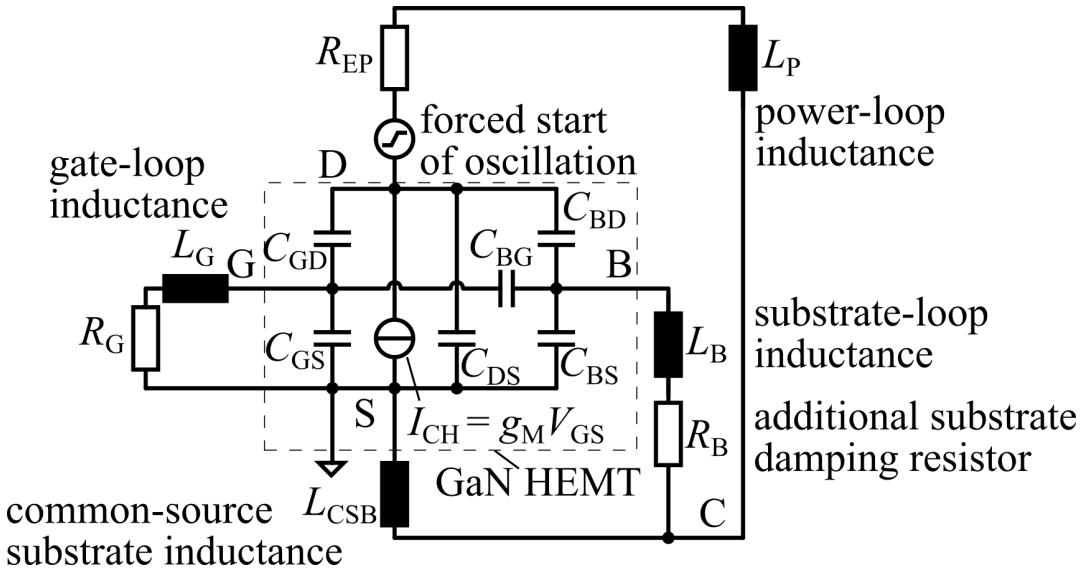

Figure 4.4: Full equivalent circuit including parasitic substrate-loop inductance L_B, common-source substrate inductance L_{CSB}, gate-loop inductance L_G and power-loop inductance L_P.

The full equivalent circuit now includes another fourth node: The common-source substrate node C which connects the substrate inductance L_B, the power-loop inductance L_P and the common-source substrate inductance L_{CSB}. The substrate node B also still exists in addition to the gate and drain nodes (G, D). The passive RLC-components

from Fig. 4.4 are represented as admittance parameters Y in the following. In order to analyze the circuit using feedback amplifier theory, a two-step circuit transformation is carried out: First, the common-source substrate node C as a star-node of an outer star-network around C is transformed to a delta-circuit. Then, the transformed elements are combined, and the remaining substrate node B as a star-node of an inner star-network around B is also transformed to a delta-circuit. After the two star-to-delta transformations, the four-node (G,D,B,C) circuit is described as an equivalent two-node (G,D) feedback amplifier.

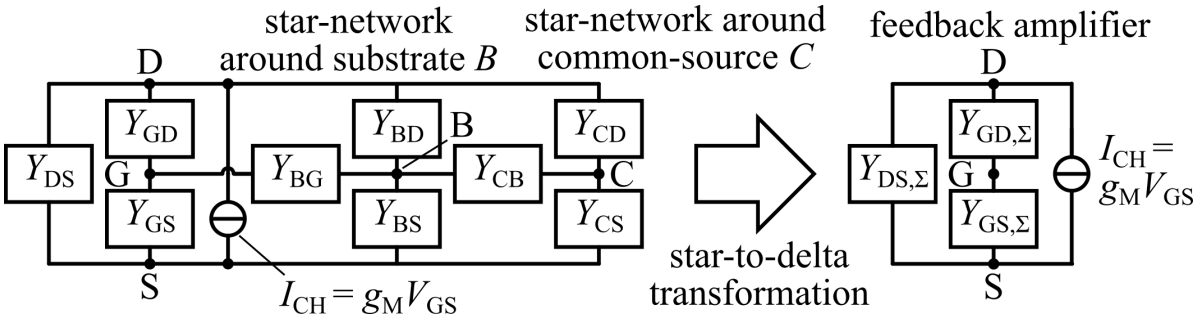

Figure 4.5: Circuit transformation method to eliminate the two inner star-nodes C, and B results in a two-port feedback-amplifier description.

The inner node C of the star-network which connects the three admittances

$$Y_{CS} = \frac{1}{i\omega L_{CSB}} \tag{4.1}$$

$$Y_{CB} = \frac{1}{i\omega L_B + R_B} \tag{4.2}$$

$$Y_{CD} = \frac{1}{R_{EP} + i\omega L_P} \tag{4.3}$$

is eliminated by star-to-delta transformation

$$Y_{BS,C,\Delta} = \frac{1}{i\omega L_{CSB}(i\omega L_B + R_B)\left(\frac{1}{R_{EP}+i\omega L_P} + \frac{1}{i\omega L_B + R_B} + \frac{1}{i\omega L_{CSB}}\right)} \tag{4.4}$$

$$Y_{BD,C,\Delta} = \frac{1}{(R_{EP} + i\omega L_P)(i\omega L_B + R_B)\left(\frac{1}{R_{EP}+i\omega L_P} + \frac{1}{i\omega L_B + R_B} + \frac{1}{i\omega L_{CSB}}\right)} \tag{4.5}$$

$$Y_{DS,C,\Delta} = \frac{1}{(R_{EP} + i\omega L_P)i\omega L_{CSB}\left(\frac{1}{R_{EP}+i\omega L_P} + \frac{1}{i\omega L_B + R_B} + \frac{1}{i\omega L_{CSB}}\right)}. \tag{4.6}$$

The connected admittances of the star-network around the substrate node B are combined as

$$Y_{S,BC} = i\omega C_{BS} + Y_{BS,C,\Delta} \tag{4.7}$$

$$Y_{G,BC} = i\omega C_{BG} \tag{4.8}$$

$$Y_{D,BC} = i\omega C_{BD} + Y_{BD,C,\Delta}. \tag{4.9}$$

The substrate node B is eliminated from the analysis by star-to-delta transformation of $Y_{S,BC}, Y_{G,BC}, Y_{D,BC}$ to $Y_{GS,BC,\Delta}, Y_{GD,BC,\Delta}, Y_{DS,BC,\Delta}$ and the resulting three equivalent admittances between gate, drain and source are finally combined by the sums

$$Y_{GS,\Sigma} = \frac{1}{R_G + i\omega L_G} + i\omega C_{GS} + Y_{GS,BC,\Delta} \tag{4.10}$$

$$Y_{GD,\Sigma} = i\omega C_{GD} + Y_{GD,BC,\Delta} \tag{4.11}$$

$$Y_{DS,\Sigma} = i\omega C_{DS} + Y_{DS,C,\Delta} + Y_{DS,BC,\Delta}. \tag{4.12}$$

The two-port expression (Eqn. 4.10-4.12) of the equivalent admittances $Y_{GS,\Sigma}, Y_{GD,\Sigma}, Y_{DS,\Sigma}$ in combination with the gate-controlled drain current allows a stability analysis of the circuit using two-port feedback amplifier theory. The equivalent two-port feedback amplifier circuit is shown in Fig. 4.5 (right).

4.4 Stability Analysis

4.4.1 Evaluation of Stability Condition

Similar to Sec. 3.2, the damping factor ζ is used to evaluate the circuit behavior. The response of the passive RLC circuit was already discussed and was divided into an over-damped region $\zeta > 1$ and an under-damped region $0 < \zeta < 1$ (oscillations with decreasing envelope). Now, in the case of a feedback circuit with the modulated channel current as active energy source, gain is introduced into the system and the damping factor might become negative $\zeta < 0$, resulting in instabilities in form of oscillations with increasing envelope over time.

For a stability analysis, the transformed full equivalent circuit with the three equivalent admittances $Y_{GS,\Sigma}, Y_{GD,\Sigma}, Y_{DS,\Sigma}$ and the voltage controlled channel current $I_D = g_M V_{GS}$ are combined as a feedback amplifier system. The equivalent drain-to-gate feedback transfer function is

$$F(s) = \frac{-Y_{GD,\Sigma}}{Y_{GS,\Sigma}Y_{GD,\Sigma} + Y_{GS,\Sigma}Y_{DS,\Sigma} + Y_{GD,\Sigma}Y_{DS,\Sigma}}, \tag{4.13}$$

the equivalent gate voltage to channel current open-loop gain is $A(s) = g_M$ (transconductance of the transistor). The closed-loop transfer function of the feedback amplifier results according to feedback amplifier theory [94] $T(s) = \frac{A(s)}{1-A(s)F(s)} = \frac{1}{\frac{1}{A(s)}-F(s)}$ as

$$T(s) = \frac{1}{\frac{1}{g_M} - \frac{-Y_{GD,\Sigma}}{Y_{GS,\Sigma}Y_{GD,\Sigma}+Y_{GS,\Sigma}Y_{DS,\Sigma}+Y_{GD,\Sigma}Y_{DS,\Sigma}}}. \tag{4.14}$$

For each of the N poles p_k of $T(s)$, the damping factor $\zeta_k = -\Re(p_k)/|p_k|$ is calculated. If the lowest of all evaluated damping factors $\zeta_{MIN} = \min_{k\in 1\ldots N}(\zeta_k)$ is negative $\zeta_{MIN} < 0$ the system is unstable. If all damping factors are positive $\zeta_{MIN} > 0$, the system is stable. In the following the stability is evaluated for specific circuit parameter combinations, and the boundary between stability and instability is plotted by parametric region plots.

Since instabilities from the parasitic substrate-loop have not been analyzed in literature and for application-oriented real switching cells, this work aims to quantify the stability conditions for real application-oriented circuits. For this reason, in the following the boundary between the stable and unstable circuit is numerically investigated using equivalent capacitance values and typically expected parasitic inductance values of actual experimental setups.

4.4.2 Parameters for Quantitative Stability Evaluation

For a quantitative stability analysis, Table 4.1 shows the circuit parameters used in the following for numerical evaluation of the stability condition. Two PCB-embedded power modules are analyzed. The 1st generation of PCB-embedded half-bridge module uses a GaN HEMT with integrated driver and externally paralleled GaN-based Schottky diode. The 2nd generation uses a GaN HEMT with approximately double the gate-width, an integrated driver and intrinsic Schottky diodes. The 2nd generation of module was already presented in Sec. 3.5.3 (Fig. 3.25a). Since the intrinsic Schottky diodes do not significantly increase the required chip area, only the gate-connected capacitances are approximately doubled, whereas the integration of the Schottky diode instead of external diodes allows doubling the gate width compared to an externally paralleled GaN HEMT and GaN diode without doubling the drain and source connected capacitances. A detailed analysis of the contribution of capacitances with and without intrinsic Schottky diodes is published in [63]. The main reason why two generation of modules are compared is however not because of the origin of terminal capacitances, but instead due to different approaches for external substrate-to-source termination: The 1st generation of power modules does not interconnect the substrate and source on package level, but instead provides a dedicated substrate pin on package level which can be connected in different ways to other circuit nodes. This flexibility to realize alternative substrate terminations resulted in instability for an external substrate-to-source termination, which is discussed in the following. The 2nd generation of power modules interconnects the substrate and source already inside the PCB-embedded package with a low substrate-loop inductance. Even though the 2nd generation has double the gate width, the integrated gate driver resistance was not increased, because in the 1st generation the gate driver was over-dimensioned.

	C_{GS}	C_{GD}	C_{DS}	C_{BS}	C_{BG}	C_{BD}	g_M	R_{EP}	R_G
1st generation	100 pF	2 pF	300 pF	45 pF	30 pF	90 pF	5 S	1 Ω	1.5 Ω
2nd generation	200 pF	4 pF	300 pF	45 pF	60 pF	90 pF	10 S	0.5 Ω	1.5 Ω

Table 4.1: Parameters of circuit components used for the evaluation of stability. Two generations of power modules are analyzed.

4.4.3 Effect of Gate-Loop and Power-Loop Parasitic Inductance

The effect of parasitic gate-loop and power-loop inductance on half-bridge stability, without considering the substrate-loop, has been analyzed in literature [94, 95, 96]. For the

sake of completeness and to allow better classification of the following quantitative results with substrate inductance, here the case of only gate-loop and power-loop inductance is also discussed. As already stated, a common-source inductance between the gate-loop and power-loop is not considered here, since it is always assumed (and realized in all GaN ICs and experimental setups in this work) that a dedicated source-sense pin is used to connect the gate driver.

Fig. 4.6 shows the equivalent circuit with gate-loop inductance L_G and power-loop inductance L_P and an ideal substrate-to-source termination (B=S).

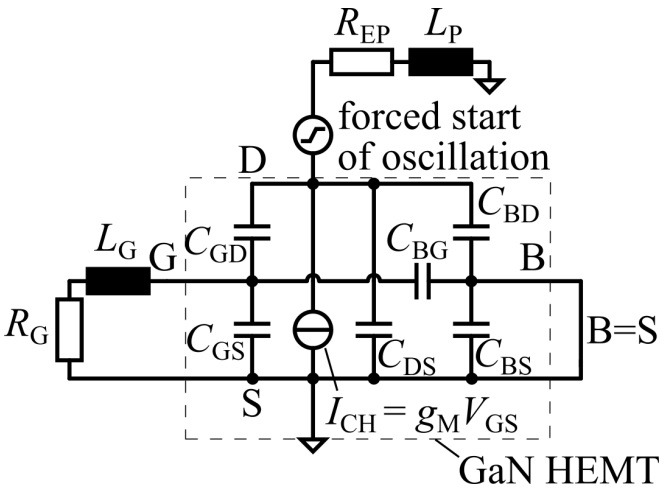

Figure 4.6: Only parasitic gate-loop and power-loop inductances. Ideal substrate-to-source (B=S) termination.

Fig 4.7 quantitatively shows the region of minimum required gate resistance R_G as a function of power-loop inductance L_P, for multiple discrete gate-loop inductances L_G. The plot enables to determine for combinations of $R_\mathrm{G}, L_\mathrm{P}, L_\mathrm{G}$, if the circuit is stable (white regions) or unstable (red regions).

The circuit seems quite stable over a wide parameter space, because only for relatively high gate-loop inductance values $L_\mathrm{G} > 4\,\mathrm{nH}$ instabilities are observed. For lower gate-loop inductance $L_\mathrm{G} < 4\,\mathrm{nH}$, as it is realistically achievable for example with integrated gate drivers, the circuit seems stable even for an infinitely strong gate driver ($R_\mathrm{G} \rightarrow 0\,\Omega$). Since the theoretical case of $R_\mathrm{G} \rightarrow 0\,\Omega$ seems stable, it might be concluded that the transistor can unconditionally operate at its maximum switching speed, approaching the discussed instantaneous step-voltage switching in Sec. 3.2.1. Of course, as also discussed in Sec. 3.2.1, high overshoot up to +100% is also expected. If the transistor can withstand the high over-voltage, for example when operated below 50% of the breakdown voltage, then no instability is expected and the oscillation which follows the overshoot will decay to a stable steady-state condition. It should be noted that the stable region of slightly increased power-loop inductance can be advantageously used, as discussed in Sec. 3.2.2, where the resonance of terminal capacitances with a low non-zero power-loop inductance is used for low-overshoot switching transitions.

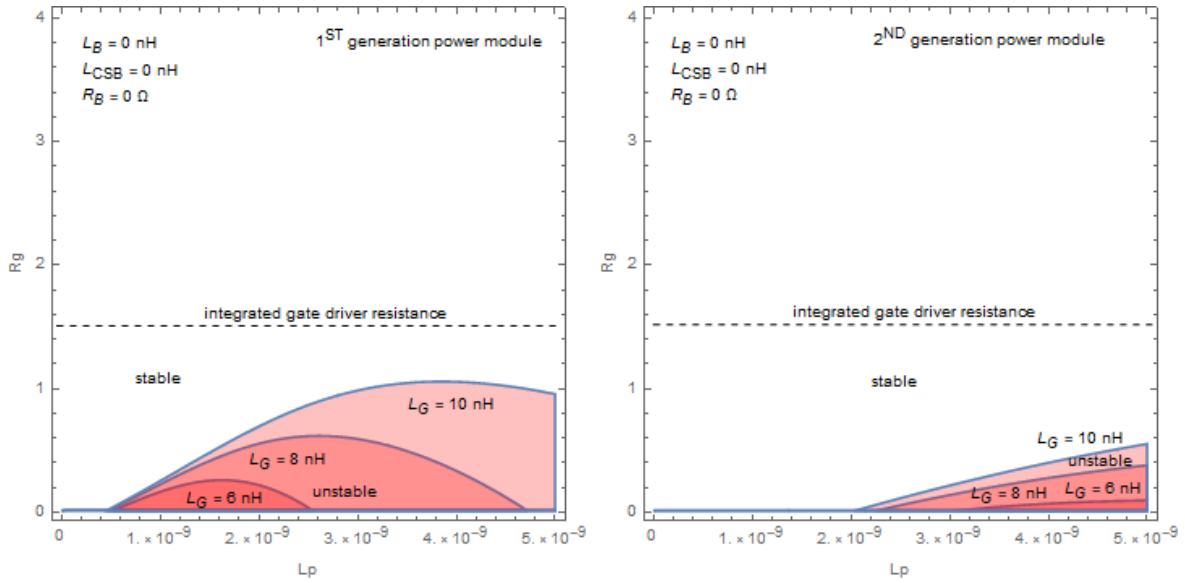

Figure 4.7: Calculated instability regions depending on power-loop inductance L_P, gate-resistance and for different gate-loop inductances L_G.

4.4.4 Instabilities from Substrate-Loop Despite Ideal Gate and Power-Loop

This work exposes that the stability analysis in the previous paragraph which considered only the gate-loop and power-loop is not sufficient for a lateral GaN HEMT on conductive Si substrate. The lateral GaN-on-Si HEMT is a four-terminal device (see the four-terminal capacitance discussion in Chap. 2), and compared to a vertical three-terminal power transistor an additional capacitive coupling results from the substrate capacitances. If the substrate is connected to other parts of the circuit, for example by a substrate-to-source termination as conventionally realized, a third parasitic loop with capacitive and inductive components is formed. Compared to high-frequency GaN-on-Si or GaN-on-SiC circuits [99, 100], the lower-frequency GaN-on-Si power transistor technology for power converter applications typically does not employ conductive vias from the integrated active circuit on the top-side of the die to the silicon backside. Instead, the substrate is typically terminated to the source terminal by means of an external connection on the package-level. Since power transistors typically are large-area devices with die dimensions exceeding several square-millimeters, it is apparent that if no internal via process is used, then the substrate-to-source termination always creates a loop, in the worst case along the complete top-side dimension of the die, around the edge of the die, and again back along the complete back-side dimension of the die. If the external substrate-to-source termination is realized by bond-wires or other assembly techniques, the substrate-loop is further increased. Even though source-vias are not typically used in GaN-on-Si power ICs, there is an experimental work which employs source-via grounding in a 350 V GaN HEMT on silicon [101], and achieved below 100 ps switching times at 10 V [102]. It should be noted that integrated source-vias on a common conductive Si substrate will prevent monolithic integration of high-side GaN-on-Si circuits such as half-bridges if no additional vertical isolation measures are implemented.

This subsection analyzes the circuit in Fig. 4.8, where only the substrate-loop has a parasitic inductance, but the gate-loop and power-loop have zero (ideal) parasitic inductances. Furthermore, the parasitic gate-loop and substrate-loop inductance as shown in Fig. 4.9 is also analyzed.

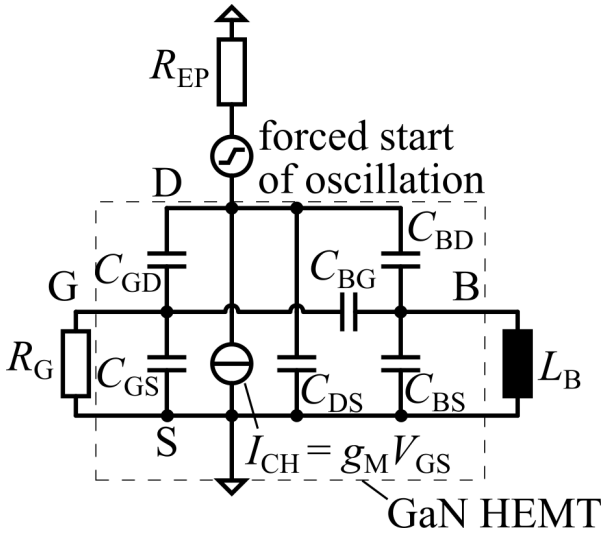

Figure 4.8: Circuit with zero gate-loop and power-loop inductance, but only the substrate-loop inductance causing instabilities.

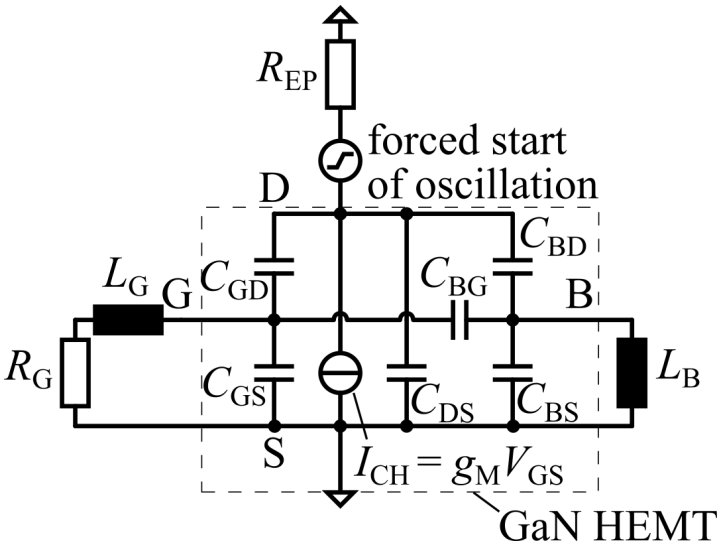

Figure 4.9: Equivalent circuit including a parasitic substrate-loop inductance L_B from the substrate-to-source interconnection. Gate-loop parasitic inductance L_G is also included.

Fig. 4.10 shows the evaluation of the stability criteria for a wide range of substrate-loop inductance and gate damping resistors for both power module generations. The special case from Fig. 4.8 with only a parasitic substrate-loop inductance is included in Fig. 4.10 by the parameter combination $L_P = L_G = 0\,\text{nH}$. From this parameter combination, it is apparent that the parasitic substrate-loop alone, despite zero gate-loop and power-loop inductance is sufficient to cause instabilities. For the integrated gate driver resistance of $R_G = 1.5\,\Omega$ and despite $L_P = L_G = 0\,\text{nH}$, instabilities are

predicted starting at $L_B > 1.1\,nH$ (1^{st} generation) or $L_B > 1.4\,nH$ (2^{nd} generation). If a non-zero parasitic gate-loop inductance of $L_G = 1\,nH$ is further taken into account, then instabilities are predicted already at even lower parasitic substrate-loop inductances of $L_B > 0.5\,nH$ (1^{st} generation) or $L_B > 0.7\,nH$ (2^{nd} generation).

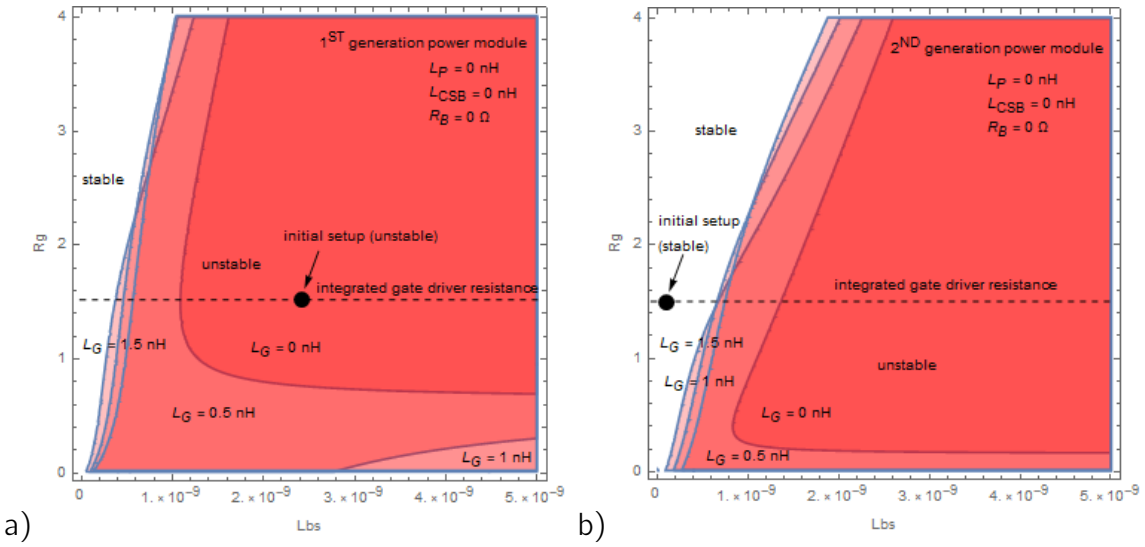

Figure 4.10: Calculated instability regions depending on substrate-loop inductance L_B and gate-resistance and for different gate-loop inductance L_G down to zero and zero power-loop inductance $L_P = 0\,nH$.

4.4.5 Parasitic Common-Source Substrate Inductance L_{CSB}

By a slight modification of the interconnection scheme, it is possible that the substrate-loop from the substrate-to-source termination is partly included and thus shared by the power-loop. In this case, the substrate-loop includes a common-source substrate inductance L_{CSB}. Fig. 4.11 shows the circuit used for analysis of the stability condition for a special case where the substrate-loop is fully included in the power-loop. Fig. 4.12 shows the evaluation of the stability condition over a wide range of common-source substrate inductance L_{CSB} in combination with a gate damping resistance R_G, and for several parasitic gate-loop inductance values L_G. This theoretical case where the substrate-loop is fully shared with the power-loop shows that also for non-zero L_{CSB} stability is only achieved by damping of the circuit by an increased gate resistance.

In addition to this theoretical case to analyze just L_{CSB}, next a more realistic case is investigated, where beside gate-loop L_G and power-loop L_P inductance also a partial shared common-source substrate inductance L_{CSB} exists. Fig. 4.13 shows the equivalent circuit. For a realistic common-source parasitic inductance value of $L_{CSB} = 0.4\,nH$ now again the stability condition is evaluated and shown in Fig. 4.14. The chosen value of $L_{CSB} = 0.4\,nH$ will be derived from the used layout later in this chapter.

Fig. 4.14 shows the evaluated stability for the constant L_{CSB} over a wider range of substrate-loop inductance L_B, gate resistance R_G and for several parasitic gate-loop inductance values L_G. For the special case of an ideal gate-loop $L_G = 0\,nH$ (in addition to the ideal power-loop $L_P = 0\,nH$) it is again predicted that the parasitic substrate

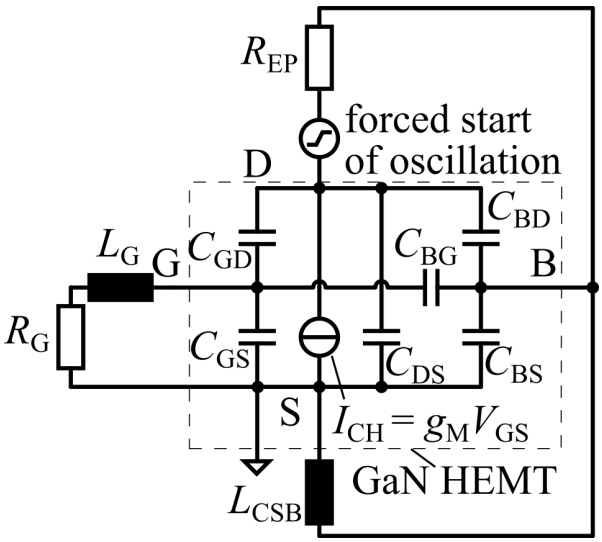

Figure 4.11: Equivalent circuit including only a parasitic common-source substrate-loop inductance L_{CSB} from a substrate-to-source interconnection which is shared with to the power-loop. Gate-loop parasitic inductance L_G is also included.

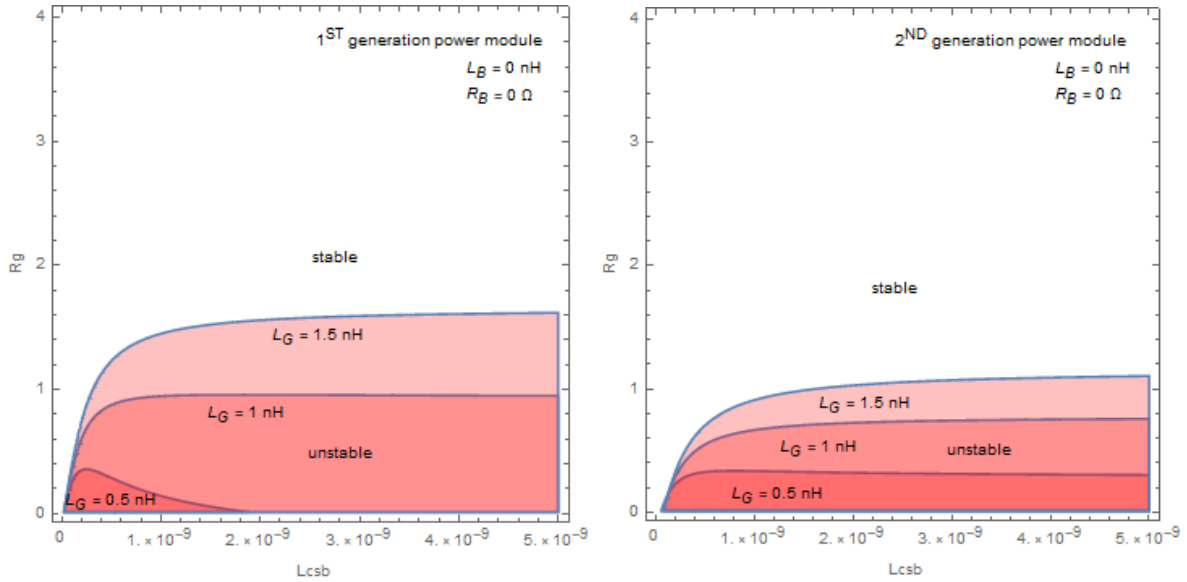

Figure 4.12: Calculated instability regions depending on common-source-substrate-loop inductance L_{CSB} and gate-resistance and for different gate-loop inductance L_G down to zero and zero substrate-loop inductance $L_B = 0\,nH$.

inductance alone is sufficient to cause instabilities. For the used gate resistance of $R_G = 1.5\,\Omega$, now $L_B > 2.6\,nH$ (1st generation) or $L_B > 3.5\,nH$ (2nd generation) are sufficient to cause instabilities. For a parasitic gate-loop inductance of $L_G = 1\,nH$, already $L_B > 0.9\,nH$ (1st generation) or $L_B > 1.6\,nH$ (2nd generation) are sufficient to cause instabilities.

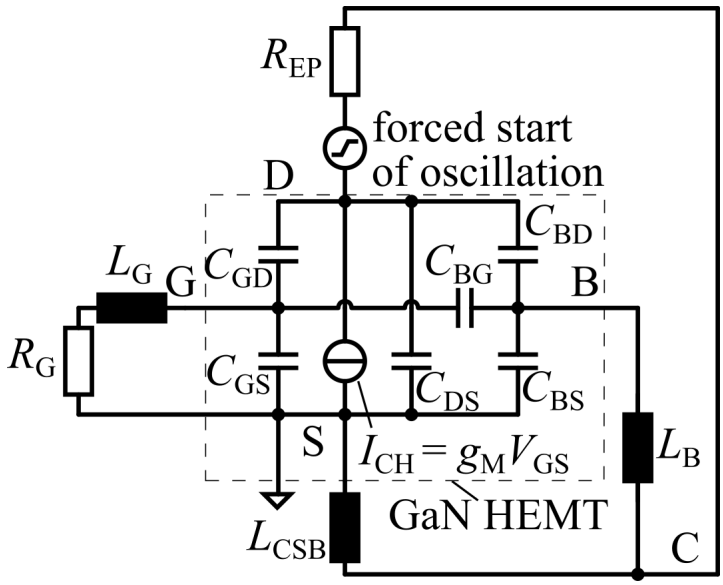

Figure 4.13: Equivalent circuit including a parasitic common-source substrate-loop inductance L_{CSB} and also a substrate-loop inductance L_B from a substrate-to-source interconnection. Gate-loop parasitic inductance L_G is also included.

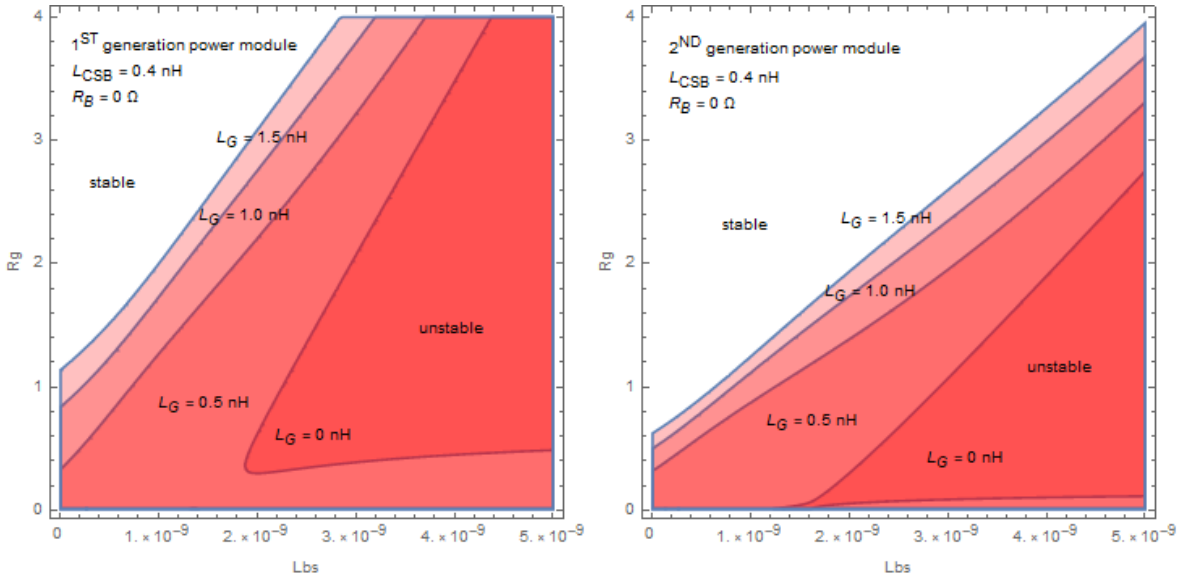

Figure 4.14: Calculated instability regions depending on the substrate-loop inductance $L_B$and gate-resistance and for different gate-loop inductances L_G down to zero and a substrate-loop inductance of $L_{CSB} = 0.4\,nH$.

4.5 Resistive Damping of Parasitic Substrate-Loop

In the parameter study so far only increasing the gate-resistance R_G was considered as an adjustable parameter to avoid instabilities. However, increased R_G also reduces the switching speed. This work recognized that other measures than increasing R_G are possible to avoid instabilities from the substrate. Since the substrate-to-source termination is the cause for the discussed instabilities, but it is not intentionally dampened, this work proposes to introduce a low-resistive substrate damping resistance R_B in the

substrate-loop for damping of the substrate as an alternative to the direct substrate-to-source termination. Intuitively, the effectiveness of this approach is understood: While the lateral GaN HEMT is intentionally controlled by the top-gate, and a gate-resistance is used for damping in the gate-loop, in an analog way the control of the GaN HEMT by the substrate as a back-gate is now also damped by the introduced substrate-resistance in the substrate-loop.

Fig. 4.15 shows the proposed substrate-to-source termination circuit with an additional substrate damping resistance R_B. This additional component was already included in the presented stability analysis in Sec. 4.4.

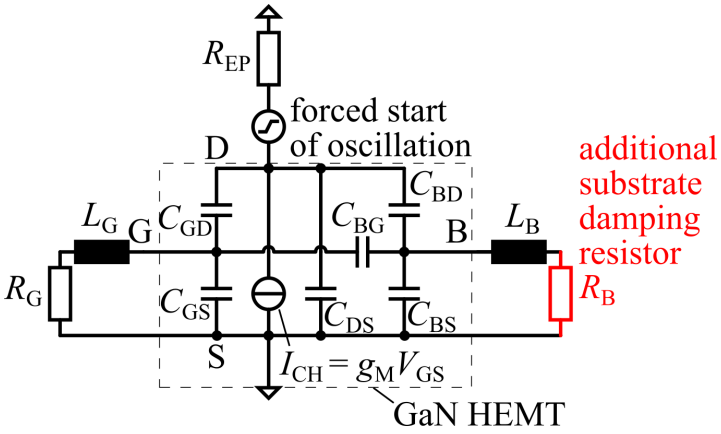

Figure 4.15: Resistive substrate damping by additional external substrate resistor R_B

To demonstrate that the proposed substrate damping by R_B is an alternative solution to achieve stability, instead of increasing R_G, exemplarily an initially unstable parameter combination for the 1^{ST} generation of power module is further analyzed. This inital unstable operation point was also already marked in Fig. 4.10. In Fig. 4.10 the only apparent way to achieve stability (without improving the layout to reduce the parasitics), is to significantly increase R_G.

Fig. 4.16 shows the evaluation of the stability condition, now as a function of both the gate-resistance R_G and additionally the introduced substrate resistance R_B. Assuming an ideal gate-loop ($L_G = 0\,\text{nH}$), now instead of the required increase of the gate resistance to $R_G > 6.7\,\Omega$ (marked as method 1 in Fig. 4.16), a low-resistive substrate damping resistance of just $R_B > 0.13\,\Omega$ predicts stability without an increase of R_G. For a more realistic non-ideal gate-loop inductance of $L_G = 1\,\text{nH}$, instead of the required increase of $R_G > 8\,\Omega$, the insertion of a low-resistive substrate damping resistance $R_B > 0.8\,\Omega$ also achieves stability.

4.6 Experimental Verification of Substrate-Loop Damping Method

The effectiveness of resistive substrate-loop damping as theoretically proposed is now experimentally demonstrated and verified. The first generation of a discrete PCB-embedded half-bridge is used for this study, because is has no direct substrate-to-source

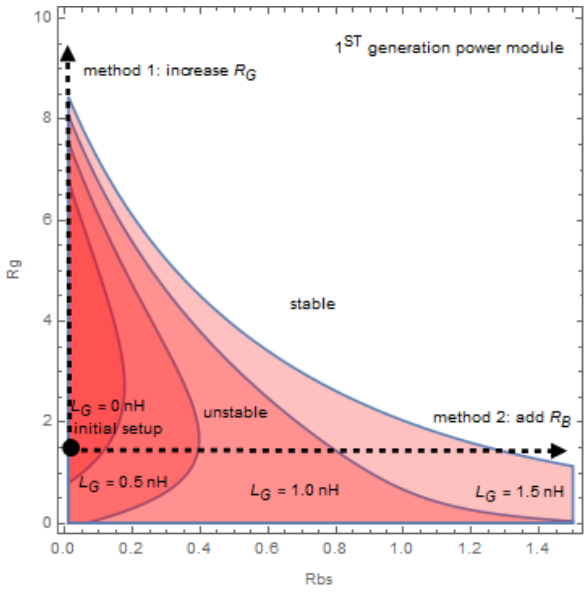

Figure 4.16: Evaluation of stability condition using either a gate-resistor R_G or non-zero substrate-loop damping resistor R_B.

termination already in the package, but instead separate dedicated pads for the substrate and source.

Fig. 4.17a shows the layout of the first generation of PCB-embedded GaN transistors, where the substrate is not connected to source already on the package-level, but instead two pads are provided. The substrate-to-source termination is then created on an external PCB, such that the interconnection through two arrays of vias and an external PCB trace creates a large substrate-loop with a high parasitic substrate-loop inductance. The large substrate-loop is marked in red in Fig. 4.17a. Fig. 4.17b shows an improved layout, where the substrate-loop is minimized by a direct on-package substrate-to-source interconnection.

For the experimental verification, the initial layout as in Fig. 4.17a is used. For the cases where an additional R_B is used, the PCB trace at the top in Fig. 4.17a is replaced by a surface-mount resistor, as shown in Fig. 4.18.

Fig. 4.19 shows the complete assembled half-bridge switching cell with embedded package and substrate damping resistor, as published in [97].

Hard-switching turn-on transitions of the half-bridge were characterized at an operation voltage of 100 V. The gate-loop was not additionally damped, and only the internal gate driver contributes $R_G = 1.5\,\Omega$ to the gate-loop.

Fig. 4.20 shows the measured transient voltage waveforms of the switch-node voltage V_{SW} and both gate-source voltages V_{GS} and V_{GS}. The initial setup with no substrate-loop damping shows an instability (Fig. 4.20a). Insertion of a substrate-loop damping resistance of just $R_B = 1\,\Omega$ already shows stable circuit behavior (Fig. 4.20b). Higher damping of the substrate by $R_B = 10\,\Omega$ causes the oscillation to decay faster (Fig. 4.20c). While it might seem that an arbitrary further increase of R_B improves the stability, a closer investigation shows that significant higher R_B cause another issue and thus should be avoided. The substrate damping resistor was further increased to a highly-resistive value (instead of low-resistive) of $R_B = 330\,000\,\Omega$. Even though the instability is

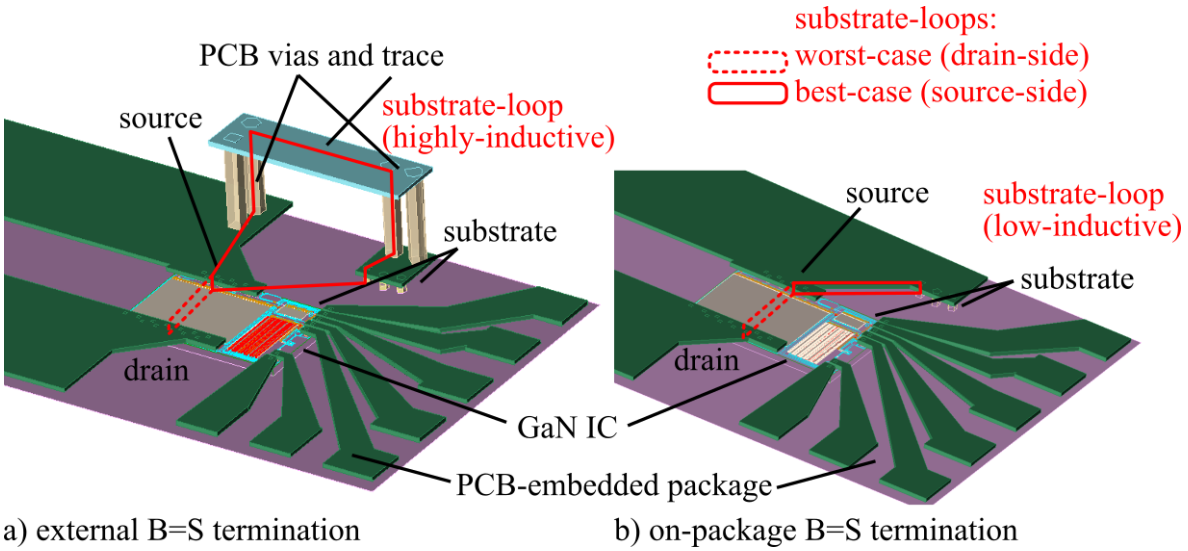

Figure 4.17: Layout of first generation of PCB-embedded power module, with a) external substrate-to-source termination through PCB vias create a large parasitic substrate-loop. b) Improved layou where the substrate is connect low-inductive to source already on the package-level.

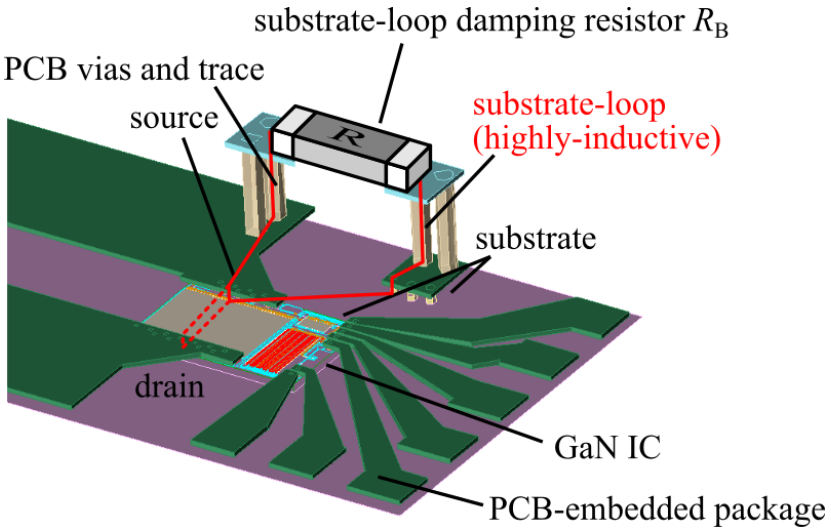

Figure 4.18: Experimental implementation of proposed insertion of substrate-loop damping resistor R_B instead of direct substrate-to-source termination.

avoided (Fig. 4.20c) the highly-resistive substrate-to-source termination is now effectively a floating substrate termination.

For the extreme case of a highly-resistive substrate resistor $R_B \to \infty$, the substrate potential is effectively floating. The floating substrate termination has been discussed in Sec. 2.6.6, and it was shown that for a floating substrate the substrate-to-source voltage changes during a complete switching cycle with a substrate voltage swing up to half of the dc voltage $\Delta V_{BS} \approx \frac{1}{2} V_{DC}$. A fully floating substrate termination completely breaks the substrate-loop, such that now instabilities from the substrate are possible. However, even though the floating substrate termination avoids the substrate-loop, now other effects dominate. Negative average substrate potential can cause static back-gating effects, and positive average substrate potentials can cause high vertical leakage currents, which

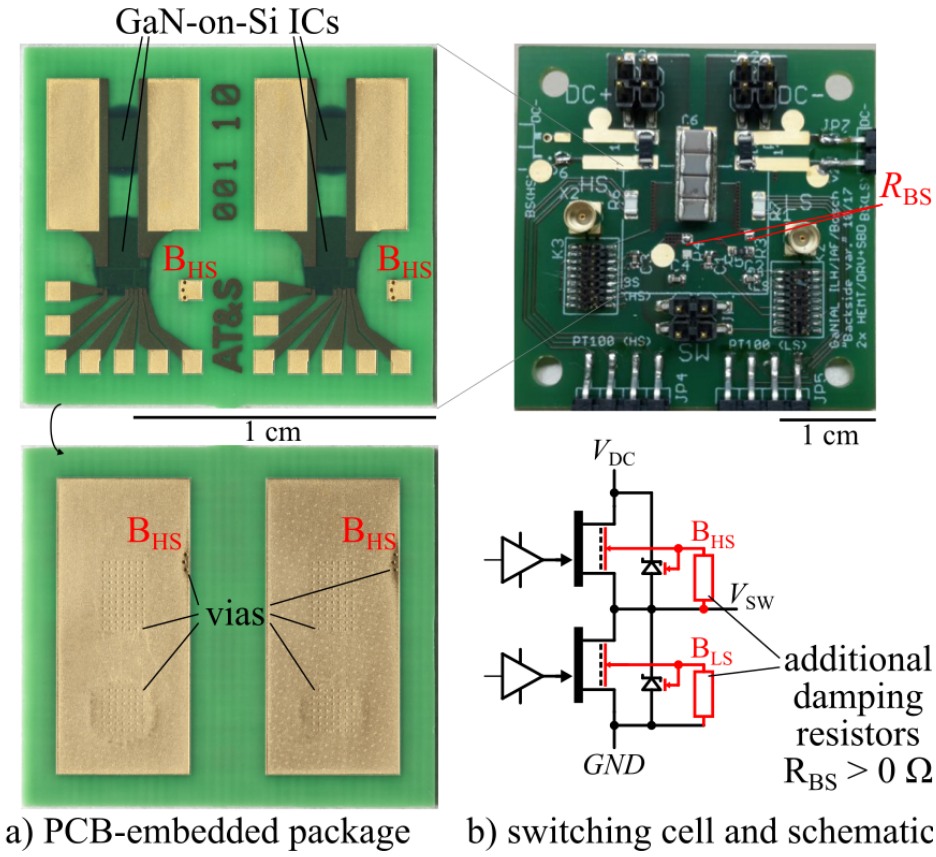

Figure 4.19: a) Half-bridge package in b) switching cell with substrate-loop damping resistor. © 2018 IEEE. Reprinted, with permission, from [97].

should both be avoided. Furthermore, as was discussed in Sec. 2.7.4 , the effective reverse capacitance is significantly increased for the floating substrate termination. To dampen instabilities from the parasitic inductance of the substrate-to-source termination, thus only low-resistive R_B should be used.

The parasitic substrate-loop inductance is not only relevant for the stability of half-bridges, but any monolithic GaN-on-Si power IC with a fixed substrate termination. After publication of this work's proposed substrate damping method in [97], a work of C. Kuring [103] also experimentally demonstrated the effectiveness of a non-zero but still low-resistive substrate damping resistor for a bi-directional GaN switch.

4.7 Reduction and Avoidance of Parasitic Substrate-Loop Inductance

Even though the damping of the substrate by an additional damping resistance R_B was found to be effective, a better solution to avoid the instabilities is to mitigate the cause of the instability, namely the parasitic substrate-loop inductance. For the lowest possible L_B, the substrate, which is the backside of the IC, should be interconnected as close as possible to the source, which is on the top-side of the IC. This is possible by including the substrate-to-source termination already in the design of the package.

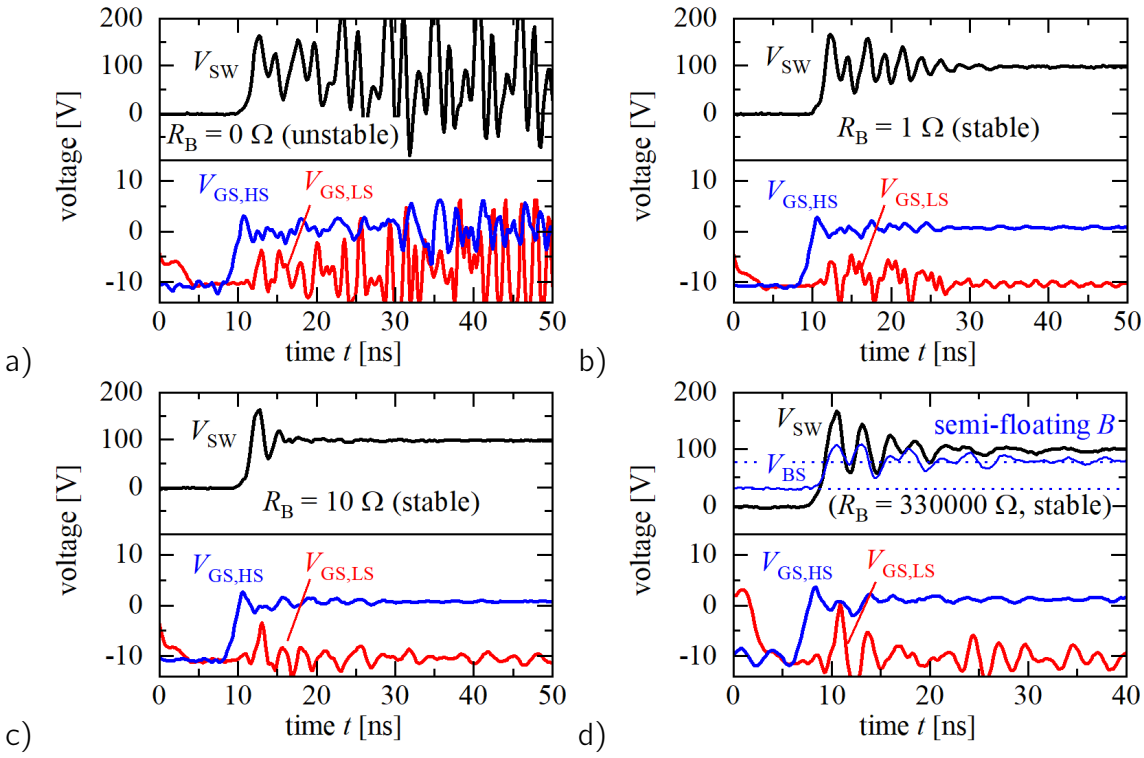

Figure 4.20: Measured hard-switching voltage transitions of the 1^{st} generation of PCB-embedded power module which shows an instability for direct substrate-to-source termination $R_B = 0\,\Omega$, due to an excessive high parasitic substrate interconnect inductance $L_B = 2.4\,\text{nH}$. An additional substrate damping low-resistive resistor R_B stabilizes the circuit, and for highly-resistive R_B the substrate-to-source termination is lost and the substrate voltage V_{BS} is semi-floating.

Table 4.2 shows simulated parasitic substrate-loop inductances for different layouts. The already discussed first generation of PCB-embedded power module from Fig. 4.17a, and the improved version of the first generation of PCB-embedded power module from Fig. 4.17b are included. Since the substrate-loop is closed through the main power transistor, a worst-case simulation extracts the loop up to the drain-terminal, and a best-case simulation only to the source-terminal. The difference between both simulations is from the large-area geometry of the main power transistor, which increases the parasitic loop. The substrate-loop in the best-case simulation mainly consists of the external interconnection from the source to the substrate, for example by bond-wires (DCB modules) or PCB vias (PCB-embedded modules). While the initial module has a high $L_B \approx 2.4\,\text{nH}$, the improved layout where the substrate-to-source termination is realized already on the package-level significantly reducethis value to $L_B \approx 0.4\,\text{nH}$. The simulated common-source substrate inductance is much lower and in the range $L_{CSB} \approx 0.1...0.4\,\text{nH}$.

Based on these discussed findings, a second generation of PCB-embedded module is designed, where a low-inductive substrate-to-source termination is realized already in the package. Fig. 4.21a shows the layout of the second generation of PCB-embedded half-bridge module. By placing an wide array of vias at the source-edge of the IC, the substrate is interconnected as close as possible to the source. Also for bond-wire and DCB-based packages a low parasitic substrate-to-source inductance is possible. Fig. 4.21b shows a DCB-based layout, where the IC is soldered onto a conductive pad which also serves as bond landing pad for power-loop bond-wires. Table 4.2 also shows the simulated parasitic

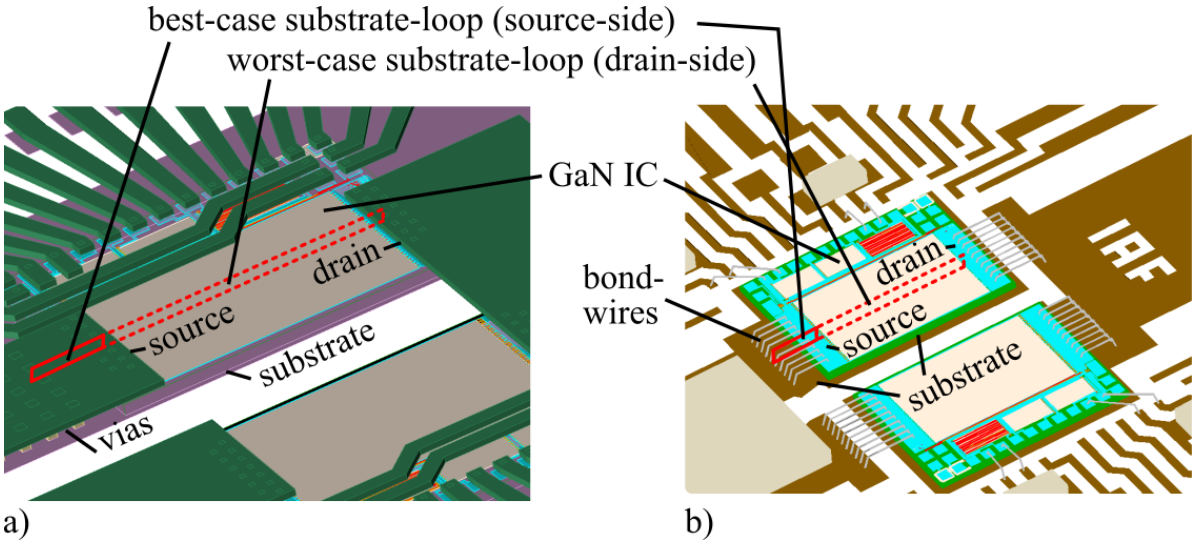

Figure 4.21: Marked worst-case and best-case substrate-loops resulting from the substrate-to-source termination outside the IC area in a) a PCB-embedded package with in-package B=S termination and b) a DCB and bond-wire based module with on-package B=S termination.

substrate-loop inductance for the second generation PCB-embedded and a DCB-based power module. The substrate-to-source termination is only relevant for discrete half-bridges or monolithic half-bridges with a fixed substrate termination. Monolithic half-bridges with a fully-floating substrate do not form a substrate-loop, such that a parasitic substrate-loop inductance is not present. For monolithic half-bridges on a semi-floating substrate with highly-resistive substrate biasing resistors, even though a substrate-loop exists, it is not relevant for the stability since the substrate-loop is highly over-damped.

assembly **half-bridge** **generation** Figure	**Embed.** **discr.** 1st 4.17a	**Embed.** **discr.** 1st (impr. layout) 4.17b	**DCB** **discr.** 2nd 4.21b	**Embed.** **discr.** 2nd 4.21a	**DCB** **mono.** 2nd	**Embed.** **mono.** 2nd
drain-side L_B	2.42 nH	0.39 nH	0.17 nH	0.09 nH	none^C	none^C
drain-side L_{CSB}	0.36 nH	0.22 nH	0.33 nH	0.31 nH	none^C	none^C
source-side L_B	2.40 nH	0.36 nH	0.13 nH	0.05 nH	none^C	none^C
source-side L_{CSB}	0.20 nH	0.09 nH	0.13 nH	0.10 nH	none^C	none^C

Table 4.2: Simulated parasitic substrate-loop inductance and common-source substrate-loop inductance. (^{C}): capacitive

4.8 Summary and Conclusion

This work exposed for the first time that the substrate-loop from external substrate-to-source termination (B=S) of lateral GaN power transistors forms a third critical loop, in addition to the gate-loop and power-loop.

This chapter then investigated the research questions:

- How does the substrate termination as a third critical loop affect switching behavior and stability?

The interconnections in the substrate-loop which are required for the substrate-to-source termination of discrete GaN-on-Si HEMTs (without vertical via technologies) result in a non-zero parasitic substrate-loop inductance. An equivalent feedback circuit analysis was carried out. Similar to parasitic inductance in the gate-loop and power-loop, it was shown that parasitic substrate-loop inductance can cause oscillations and instabilities of the switch-node. Furthermore it was shown that parasitic substrate-loop inductance alone is sufficient to cause unstable switch-node voltages, even for zero gate-loop and power-loop inductance. The stability analysis was further refined to also consider a common-source substrate inductance.

- How to reduce the substrate-loop inductance and avoid related instabilities?

In the previous chapters of this work it was shown that monolithic gate driver and transistor integration allows a significant reduction of the gate-loop and power-loop inductance. However, in this chapter it was shown that the monolithic integration alone is not a guarantee for clean and stable switching waveforms. Experimentally, a power module with an initially high parasitic substrate-loop inductance was characterized and showed a severe instability caused by the substrate. Instead of slowing down of the switching transition by increasing the gate resistor, an alternative solution to dampen the substrate-loop by an additional low-resistive substrate-loop resistor was proposed and verified. It was shown that a floating substrate or highly-resistive termination of a floating substrate breaks the substrate-loop and avoids the instability. However, the floating substrate at the same time causes other substrate-related effects which were already extensively studied in the previous chapters.

Especially for the used cost-competitive GaN-on-Si power transistor technology without a via process a careful design of the substrate-to-source termination on the packaging level is required. This is because due to the lack of a via process the substrate-to-source termination has to be realized always outside the IC by external interconnects. Layout guidelines were discussed which allow reduction of the parasitic substrate-loop inductance to low values which are sufficiently low to avoid instabilities from the substrate. For a GaN power IC it was exemplarily shown that the monolithic integration of a gate driver stage with the main power transistor does not guarantee stability. To ensure stability, it was shown that the external substrate-to-source termination of the ICs' top-side source to the back-side substrate terminations should be realized low-inductive, for example by a wide array of bond-wires or PCB-vias close to the source-edge of the IC.

Both a PCB-embedded half-bridge package and a DCB and bond-wire based half-bridge module were designed with very low parasitic substrate-loop inductance. The combination of monolithic gate driver and transistor integration with advanced packaging was shown to be a powerful solution to exploit the intrinsic switching capability of GaN power ICs.

5 Summary and Conclusion

This work investigated the performance of integrated GaN-on-Si half-bridges and drivers, focusing on the influence of effects related to the conductive Si substrate.

In addition to the more detailed and quantitative summaries which were included at the end of each main chapter, here the main findings and conclusions are summarized on a higher and more general level:

- The monolithic integration of GaN-on-Si half-bridges requires an alternative substrate termination compared to discrete half-bridges where conventionally two separate substrate-to-source terminations are used.
- The effective capacitances C_{ISS}, C_{OSS}, C_{RSS} of GaN-on-Si half-bridges depend on the substrate termination.
- GaN HEMTs on Si substrate have six terminal capacitances, where the substrate is a fourth termination in addition to gate, drain and source.
- Considering the GaN HEMT as a four-terminal device with all six terminal capacitances allows the investigation of coupling effects through the substrate.
- For each particular substrate termination of half-bridges, star-to-mesh transformation of the capacitive equivalent circuit and an explicit calculation of the dependence of the substrate voltage from the switch-node voltage allows to lump the four-terminal device into a conventional three-terminal equivalent circuit model.
- In monolithic GaN-on-Si half-bridges at least one transistor has significantly increased reverse capacitance C_{RSS}, resulting from increased coupling through the substrate.
- In monolithic GaN-on-Si half-bridges, the effective output capacitance is reduced for (semi)-floating substrate terminations, and increased for fixed-potential substrate terminations.
- The input capacitance C_{ISS} is not significantly influenced for the investigated devices by the monolithic integration.
- Monolithic GaN-on-Si half-bridges on a (semi)-floating substrate have an effective gate-to-gate coupling capacitance C_{XSS}, resulting from capacitive coupling through the substrate, which is small compared to C_{RSS}.
- Monolithic GaN-on-Si half-bridges form an unintentional integrated dc-link capacitance C_{DC}, which is small compared to C_{OSS}.

- The reduced C_{OSS} of monolithic half-bridges on floating substrates also causes reduced switching energies and switching times.
- The on-resistance of half-bridge transistors is statically degraded if negative substrate-to-source voltages occur during conduction phases.
- Static back-gating in half-bridges on floating substrates is avoided by utilizing a substrate termination network which shifts the average substrate voltage towards more positive values.
- Monolithic GaN-on-Si half-bridge operation in a dc-dc converter is more efficient than a discrete half-bridge, if the reduction of output capacitance on floating substrate is combined with a substrate biasing network which avoids back-gating related on-resistance degradation.
- Parasitic inductance in the gate-loop and power-loop causes voltage overshoot, and might result in instabilities.
- Local minima of voltage overshoot exist if the excitation signal of the parasitic network has a limited voltage slew-rate.
- Optimal switching times exist, for which the overshoot is locally minimized.
- A slight reduction of switching times is sufficient to significantly reduce voltage overshoot.
- Monolithic integration of half-bridges and drivers alone is not sufficient to fully eliminate the parasitic gate-loop and power-loop inductance, since external interconnection to gate and dc-link decoupling capacitors are still required.
- Not the (side-by-side) integration of two half-bridge transistors in a single chip per se reduces the parasitic inductance, but the on-chip interconnection around the switch-node between the half-bridge transistors does.
- Combination of monolithic integration, advanced packaging and on-package decoupling capacitors is a comprehensive solution to minimize parasitic effects.
- The substrate-loop which is formed by the external connection from the substrate to source is a third critical parasitic loop, in addition to the well-known gate-loop and power-loops.
- The substrate-to-source termination of GaN-on-Si HEMTs may cause voltage oscillations and even instabilities.
- In the presence of parasitic substrate-loop inductance an unstable switching behavior is possible even for zero gate-loop and power-loop inductance.
- The parasitic substrate-loop is eliminated on a floating substrate without substrate-to-source termination.

- Instabilities from the substrate may be dampened by insertion of an additional substrate-loop damping resistor into the substrate-loop.

It is now clear that besides the discussed advantages of integrated GaN power circuits, the monolithic integration alone is not a complete solution for power converters. Instead, also for monolithic integration still the interconnection and interaction with external components is of importance. Since the packaging of the semiconductor devices serves as link between the ICs and external components, they still are highly relevant for the overall circuit behavior.

A combination of advanced packaging, on-package capacitors and monolithic integrated GaN circuits as presented in this work is a viable solution which advantageously combines the benefits of the different integration approaches.

The findings of this work increase the knowledge about GaN-on-Si power ICs, and enable an improved design and efficient operation of future integrated power circuits for power conversion applications.

A Appendix

A.1 Star-to-Delta and Star-to-Mesh Transformation

Three capacitances which connect the star-node k with three outer nodes can be transformed to a delta circuit without the star-node. The transformed capacitances, calculated as

$$C_{ij} = \frac{C_{ik}C_{jk}}{C_{1k} + C_{2k} + C_{3k}} \tag{A.1}$$

are now between the three outer nodes. The star-to-delta transformation based on three ($N = 3$) star capacitances as input results in three ($M = N = 3$) delta capacitances.

A number of N capacitances which connect the star-node k with outer nodes can be transformed to an equivalent mesh circuit without the star-node. The transformed capacitances, calculated as

$$C_{ij} = \frac{C_{ik}C_{jk}}{C_{1k} + C_{2k} + ... + C_{nk}} \tag{A.2}$$

are now between the outer nodes. The star-to-mesh transformation based on N star capacitances as input results in $M = N(N-1)/2$ delta capacitances. For example, $N = 4$ (as used in the half-bridge transformation in Chap. 2) results in $M = 6$ mesh capacitances. The generalized star and mesh transformation method is described in [104].

It should be noted that in the half-bridge transformation in Chap. 2) there are $N = 5$ star-nodes (HS/LS gates, HS drain, LS source, SW). Applying Eqn. A.2 results in $M = 10$ mesh capacitances. This work uses a simplification: Because the high-side drain and low-side source are connected by a fixed dc-link voltage V_{DC}, both nodes can be combined for the transformation. This simplifies the transformation to a $N = 4$ to $M = 6$ transformation. For example, in a monolithic half-bridge on floating substrate the high-side $C_{BD,HS}$ and low-side $C_{BS,LS}$ are coupled through V_{DC}. For the transformation they are combined as an equivalent ac-wise parallel capacitance. Of course, the correct bias-dependence of the capacitances has to be taken into account, and after the transformation the transformed capacitances have to be partitioned back to the correct original star-nodes. For example, in the monolithic half-bridge transformation on floating substrate, two mesh capacitances result which connect the low-side gate with the high-side drain (DC+) and the high-side gate with the low-side source (DC-/GND). This two capacitances are redistributed to the high-side gate-to-drain and the low-side gate-to-source mesh connections. This redistribution allows to lump the transformed capacitances into the already existing and well-known three terminal capacitances, expect for C_{XSS} and C_{DC} which were discussed separately.

A.2 Extraction of Parameters from Measurement Data

In Sec. 2.8.2, the switching loss per hard-switching voltage transition of the dc-dc converter without an inductor is extracted according to Eqn. 2.60 based on a linear regression and multiple measured frequencies. The raw measurement data (dots) and fitted function (line) is shown in Fig. A.1, which also shows that the fit function is suitable with low error. The different colors represent the different substrate terminations and are labeled in the condensed data in Fig. 2.29

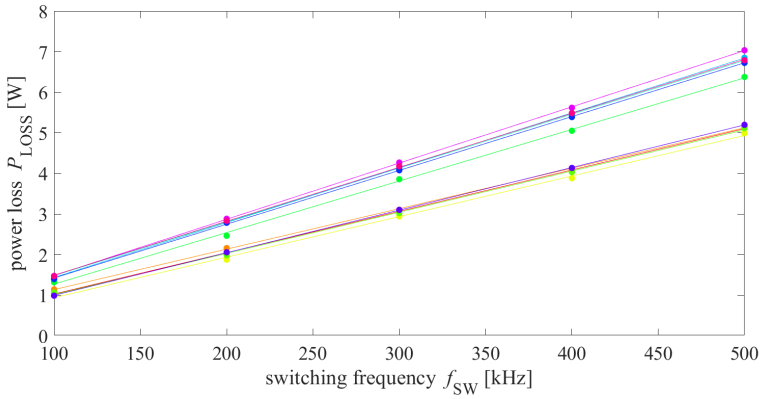

Figure A.1: Measured power loss (dots) and fitted function by linear regression to extract the switching energy for different substrate terminations.

In Sec. 2.8.5 the on-resistance is extracted by fitting the measured power loss at different output currents with a quadratic regression. The raw measurement data (dots) and fitted function (line) is shown in Fig. A.2, which again shows that the quadratic fit function is suitable with low error, since the power loss is expected to increase quadratic due to the on-resistance of the transistor. The different colors represent the different substrate terminations and are labeled in the condensed data in Fig. 2.33.

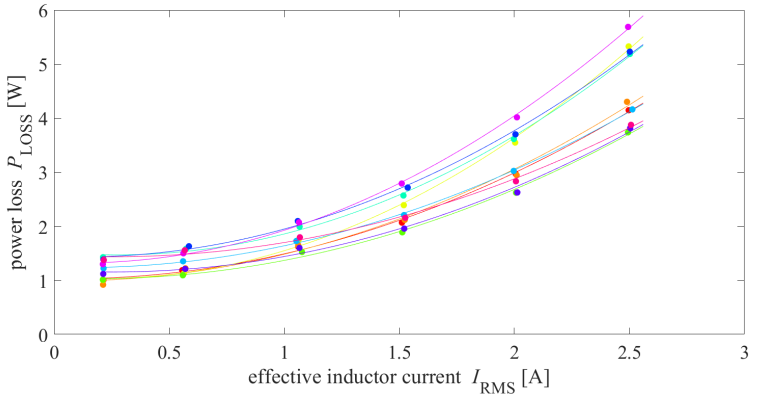

Figure A.2: Measured power loss(dots) and fitted function by quadratic regression to extract the on-resistance for different substrate terminations.

A.3 Four-Terminal Capacitance Multi-Bias Measurement Data

To extract the terminal capacitances, two GaN-on-Si HEMT test structures with 1 mm and 5 mm gate-width were measured, and from the difference of measurement data the capacitance data was extracted. This method effectively removes the capacitance of the probe-pads from the active HEMT structure.

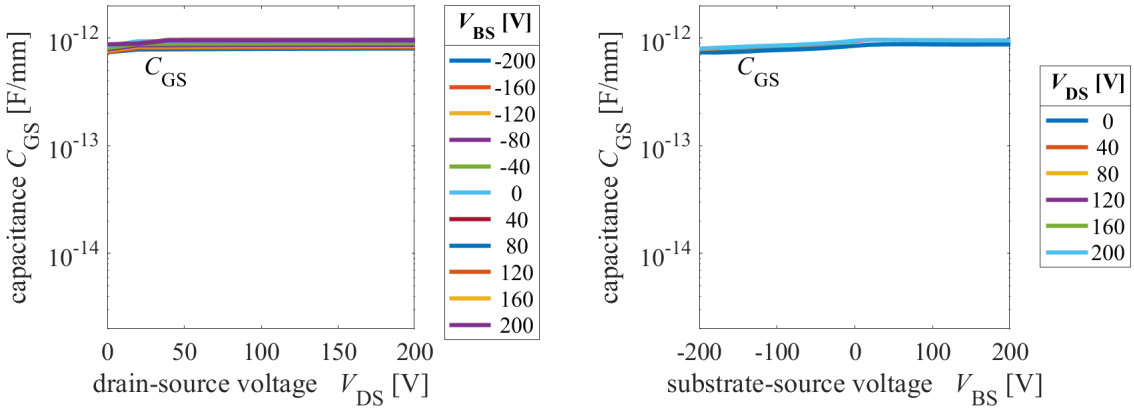

Figure A.3: Gate-source capacitance $C_{GS}(V_{DS}, V_{BS})$

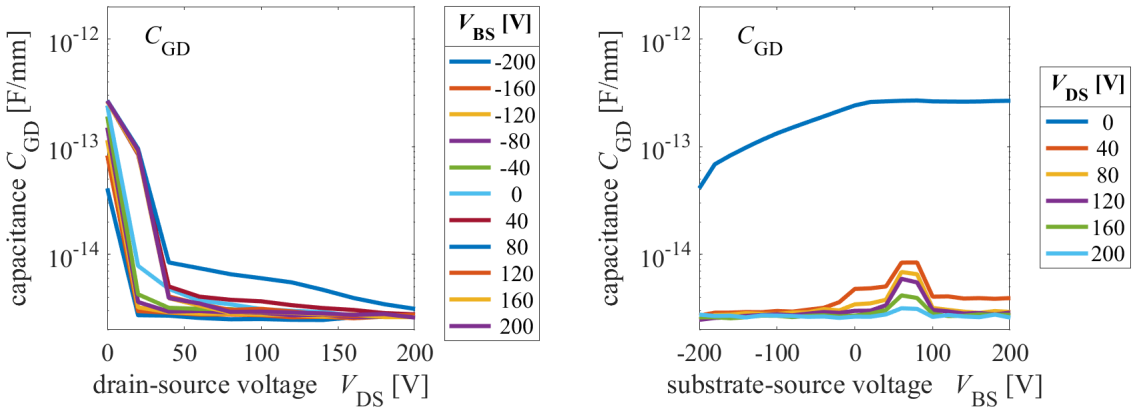

Figure A.4: Gate-drain capacitance $C_{GD}(V_{DS}, V_{BS})$

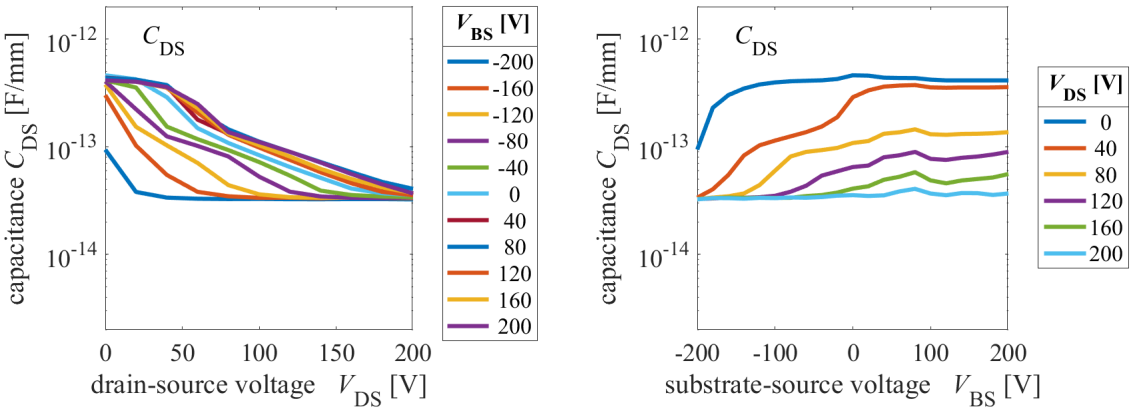

Figure A.5: Drain-source capacitance $C_{DS}(V_{DS}, V_{BS})$

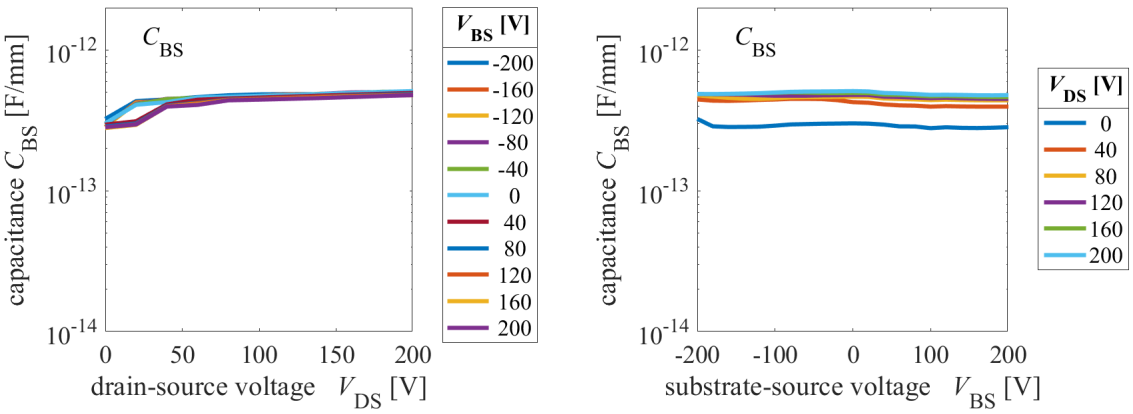

Figure A.6: Substrate-source capacitance $C_{BS}(V_{DS}, V_{BS})$

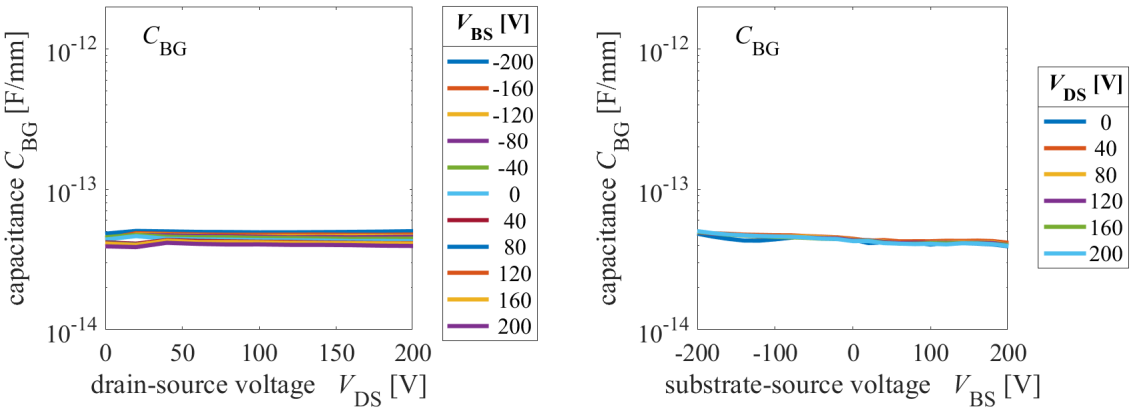

Figure A.7: Substrate-gate capacitance $C_{BG}(V_{DS}, V_{BS})$

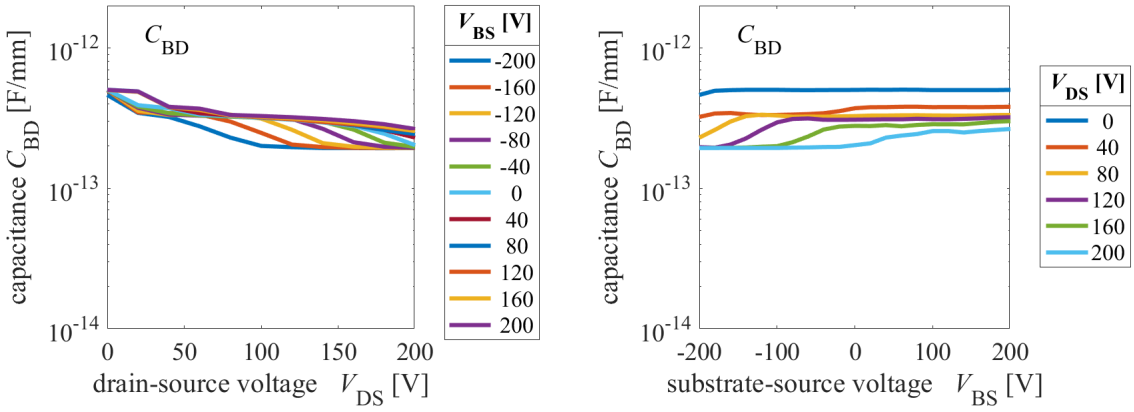

Figure A.8: Substrate-drain capacitance $C_{BD}(V_{DS}, V_{BS})$

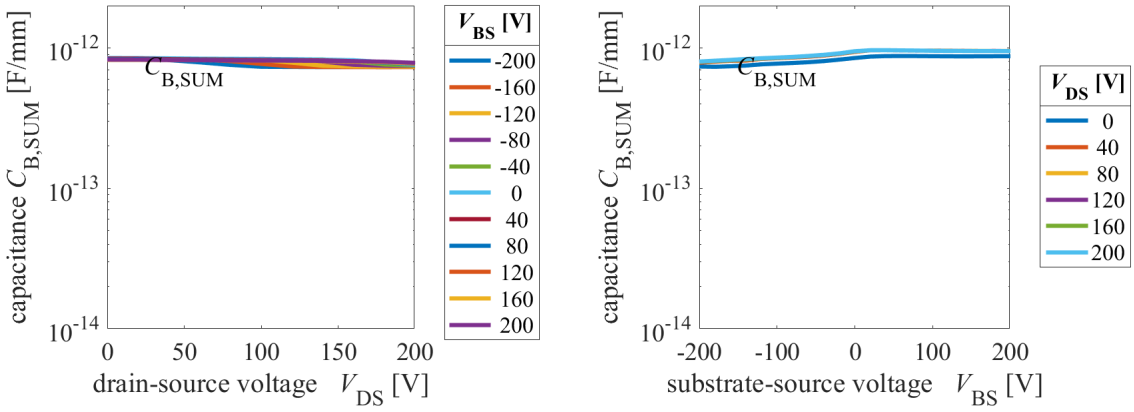

Figure A.9: Sum of substrate capacitances (V_{DS}, V_{BS})

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