Novel characterization techniques for the study of the dynamic behavior of silicon carbide power MOSFETs

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Abstract

This dissertation provides insight into the dynamic behavior of SiC power MOSFETs from their inherent static IV and CV characteristics. While conventional dynamic measurements extracted from a DPT or a similar dynamic test-bench yield accurate quantitative data, the static IV and CV characteristics of a power semiconductor device offer more qualitative information to delve into the root mechanisms responsible for its dynamic behavior. Conventional characterization techniques are limited to power levels way below those which the power device withstands in the application. As a result, the static IV and CV characteristics attained by available measurement solutions are reduced to a limited scope of bias conditions insufficient to infer information about the dynamic behavior of the power device. This work tackles this gap and proposes novel measurement techniques that enable the characterization of the static IV and CV characteristics of SiC power MOSFETs at the full range of bias conditions the power device goes through in the application. Iso-thermal IV characteristics of a commercially available SiC power MOSFET are measured up to 40 kW power (instantaneous 50 A and 800 V) at junction temperatures ranging from 25 °C to 175 °C. The CV characteristics are mapped at drain-source and gate-source bias combinations of V_{DS} = 0 - 40 V and V_{GS} = 0 - 20 V, respectively, at junction temperatures ranging from 25 °C to 150 °C. The results of these measurements reveal unique insights into the electrical characteristics of SiC power MOSFETs which impact their performance in the application and explain unclear phenomena observed in their dynamic behavior. On the one hand, the intrinsic capacitances of the SiC power MOSFET extend their non-linearity, function of both V_{GS} and V_{DS}, to the saturation region of the power device. Moreover, they are also affected by the junction temperature of the power device. The impact of these in the voltage commutation speed of

the device under different switching conditions is thoroughly analyzed in the thesis. On the other hand, the IV characteristics of the SiC power MOSFET reveal the existence of short channel effects that drastically affect the transconductance of the power device in its high voltage saturation region. Furthermore, the measurements show a positive temperature coefficient of the drain current in the high voltage saturation region of the SiC power device, attributed to the density of trap energy states in the SiC/SiO_2 interface. These effects effectively lower the plateau voltage of the device and lead to faster current commutation speeds in the application than those expected from the datasheet values. The insights revealed by the proposed characterization techniques are intended to help fine-tune semiconductor technology processes and improve the accuracy of simulation models to achieve a higher grade of optimization in the design of future SiC-based energy conversion circuits.

Kurzzusammenfassung

Diese Dissertation gibt Aufschluss über das dynamische Verhalten von SiC Power MOSFETs aus deren inhärenten statischen IV- und CV-Charakteristiken. Während herkömmliche dynamische Messungen, die aus DPT oder ähnlichen Testaufbauten extrahiert werden, akkurate quantitative Daten liefern, bieten die statischen IV- und CV-Charakteristiken eines LeistungsTransistors mehr qualitative Informationen, um die zugrundeliegenden Mechanismen zu erforschen, die für das dynamische Verhalten verantwortlich sind. Konventionelle Charakterisierungsmethoden sind beschränkt auf Leistungsniveaus, die weit unter denen liegen, welchen der Transistor im Einsatz standhalten muss. Dementsprechend werden statische IV- und CV-Charakteristiken aus den derzeit verfügbaren Messlösungen auf begrenzte Vorspannungen reduziert, die unzureichend für die Herleitung von Wissen über das dynamische Verhalten des Leistungstransistors sind. Um diese Lücke zu schließen, stellt diese Arbeit neue Messmethoden vor, welche die Charakterisierung der statischen IV- und CV-Charakteristiken von SiC Power MOSFETs im vollen Umfang der im Einsatz durchlaufenen Vorspannungen erfassen. Isothermische IV-Kennlinien eines kommerziell erhältlichen SiC Power MOSFETs werden gemessen bis zu 40 kW Leistung (50 A und 800 V gleichzeitig) mit Sperrschichttemperaturen von 25 °C bis 175 °C. Die Abbildung der CV-Charakteristiken erfolgt bei Drain-Source und Gate-Source-Bias-Kombinationen von $V_{\mathrm{DS}} = 0$ - 40 V beziehungsweise $V_{\mathrm{GS}} = 0$ - 20 V, jeweils mit Sperrschichttemperaturen von 25 °C bis 150 °C. Die Messergebnisse offenbaren einzigartige Erkenntnisse über die elektrischen Eigenschaften von SiC Power MOSFETs, die die Leistung beeinflussen und beobachtete rätselhafte Phänomene im dynamischen Verhalten des Transistors im Betrieb erklären. Einerseits erweitern die intrinsischen Kapazitäten von SiC Power MOSFETs deren Non-Linearität (die Funktion sowohl von V_{GS} als auch von V_{DS})

bis zum Sättigungsbereich des Transistors, wobei sich die individuellen Sperrschichttemperaturen auch auf die Kapazitäten auswirken. Die damit einhergehende Wirkung auf die Spannungsumwandlungsgeschwindigkeit unter verschiedenen Schaltbedingungen wird in dieser Arbeit gründlich analysiert. Andererseits legen die IV-Charakteristiken von diesem SiC Power MOSFET die Existenz von gewissen Short-Channel-Effekten offen, welche die Transkonduktanz des Transistors in dessen Hochspannungs-Sättigungsbereich drastisch beeinflussen. Darüber hinaus zeigen die Messungen einen positiven Temperaturkoeffizienten des Drain-Stroms im Hochspannungs-Sättigungsbereich des SiC MOSFET, der zurückzuführen ist auf die Verdichtung von Trap-Energiezuständen in der SiC/SiO_2-Schnittstelle. Diese Effekte verringern maßgeblich die Plateau-Spannung des Leistungstransistors und haben schnellere Stromumwandlungsgeschwindigkeiten in der Anwendung zur Folge als laut Datenblatt-Werten zu erwarten wäre. Die durch die vorgeschlagenen neuen Messmethoden gewonnenen Erkenntnisse sollen dabei helfen, Halbleiterprozesse zu verfeinern und die Genauigkeit von Simulationsmodellen zu verbessern, sodass ein höherer Optimierungsgrad im Entwurf von zukünftigen SiC-basierten Energieumwandlungsschaltkreisen erreicht werden kann.

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List of Abbreviations and Symbols

C_{DS}	Drain-Source Capacitance
C_{GD}	Gate-Drain Capacitance
C_{GS}	Gate-Source Capacitance
C_{ISS}	Input Capacitance
C_{OSS}	Output Capacitance
C_{RSS}	Reverse Transfer Capacitance
CLM	Channel Length Modulation
CV	Capacitance-Voltage
CT	Curve Tracer
D_{it}	Density of Trap States in the SiO_2/SiC Interface
DC	Duty Cycle
DIBL	Drain-Inducted Barrier Lowering
DPT	Double Pulse Test
DUT	Device Under Test
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
f_{meas}	Measurement Frequency
FEM-Simulation	Finite Element Method Simulation
FOM	Figure Of Merit
FWD	Free Wheeling Diode
G_{m}	Transconductance
G_{DS}	Output Conductance
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
I_{D}	Drain Current
i_{D}	Time-Varying Drain Current
I_{G}	Gate Current
i_{G}	Time-Varying Gate Current
IF-BW	Intermediate Frequency Bandwidth

IGBT	Insulated-Gate Bipolar Transistor
IV	Current-Voltage
L_{D}	Drain Terminal Parasitic Inductance
L_{G}	Gate Terminal Parasitic Inductance
L_{S}	Source Terminal Parasitic Inductance
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient
OSLT-Calibration	Open-Short-Load-Through Calibration
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
PTC	Positive Temperature Coefficient
R_{Ch}	MOSFET Channel Resistance
Q_{G}	Gate Charge
Q_{GD}	Gate-Drain Charge
Q_{GS}	Gate-Source Charge
Q_{Gtot}	Total Gate Charge
R_{CD}	Drain Contact Resistance
R_{CS}	Source Contact Resistance
R_{D}	Drain Terminal Total Parasitic Resistance
$R_{\mathrm{D_ext}}$	Drain Terminal Extrinsic Resistance
R_{Drift}	Epi-Layer or Drift Region Resistance
R_{DS}	Drain-Source Resistance
R_{G}	Gate Terminal Total Parasitic Resistance
$R_{\mathrm{G_ext}}$	Gate Terminal Extrinsic Resistance
R_{Gint}	Internal Gate Electrode Resistance
R_{S}	Source Terminal Total Parasitic Resistance
$R_{\mathrm{S_ext}}$	Source Terminal Extrinsic Resistance
RF	Radio Frequency
S-Parameter	Scattering Paremeter
SCE	Short Channel Effect
SCT	Short Circuit Test
SNR	Signal to Noise Ratio
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Oxide
SPICE	Simulation Program with Integrated Circuit Emphasis
T_{C}	Case Temperature
T_{J}	Junction Temperature
TLP	Transmission Line Pulse
V_{DS}	Drain-Source Voltage

v_{DS}	Time-Varying Drain-Source Voltage
$v_{\mathrm{DS_ext}}$	Time-Varying Extrinsic Gate-Source Voltage
$v_{\mathrm{DS_int}}$	Time-Varying Intrinsic Gate-Source Voltage
V_{GS}	Gate-Source Voltage
v_{GS}	Time-Varying Gate-Source Voltage
$v_{\mathrm{GS_ext}}$	Time-Varying Extrinsic Gate-Source Voltage
$v_{\mathrm{GS_int}}$	Time-Varying Intrinsic Gate-Source Voltage
V_{GD}	Gate-Drain Voltage
V_{Plateau}	Plateau Voltage
V_{th}	Threshold Voltage
VNA	Vector Network Analyzer
WBG	Wide Bandgap
Y-Parameter	Admittance Parameter
Z-Parameter	Impedance Parameter
ZA	Impedance Analyzer

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Chapter 1

Introduction

1.1 Silicon carbide for energy conversion applications

The demand on more efficient energy conversion applications increases every year. According to the 2019 international energy outlook, the World energy consumption will rise nearly 50% by 2050 [1], being industry and transportation the largest consumer sectors. Renewable energies are forecast the highest growth among primary energy sources, and electrical energy is the preferred energy source due to its relatively easy long distance transportation. To meet the forecast energy demands, energy conversion applications need to improve their overall efficiency though, beyond today values between 80-90%. One of the limiting factors here are the switching and conduction losses of power semiconductor devices [2, 3]. The technology development of Silicon (Si), the most widely used semiconductor material for the fabrication of power devices, is gradually reaching its theoretical limits. This technological bottleneck requires a semiconductor technology leap that breaks with the excessive power dissipation constrains imposed by Si power devices. Emerging power devices based on wide bandgap (WBG) semiconductor compounds, such as Silicon Carbide (SiC), feature superior thermal and electrical characteristics [4, 5] and showcase as the Si-successors to realize the next generation of efficient power converters [3, 6].

Silicon Carbide excels at semiconductor figures of merit (FOM) for power semiconductor devices [7, 8, 9, 10, 5] and finds its application specifically in the high-voltage (above 600 V) high power (above

1 kW) power electronics sector [3]. Compared to Si, the wide energy bandgap of SiC enables higher doping levels in thinner voltage blocking layers for a fixed breakdown voltage. Moreover, the drift saturation velocity of minority carriers in SiC substrates is also higher than that of Si. Consequently, SiC permits to realize power switches with higher blocking voltages and lower on-resistances. These electrical characteristics also permit a significant reduction of the active area of a power device. As a result, the inherent parasitic capacitances of this are much smaller than that of Si-counterparts, what results in much faster switching speeds. At circuit level, the associated reduction in switching losses permits increase the switching frequency at a fixed losses budget, what achieves a substantial volume reduction of passives and a much higher achieved compactness. On the thermal aspect, the higher melting point and thermal conductivity of SiC, permit the operation at very high temperatures, surpassing the 200 °C limit typical of Si-based technologies [11, 12]. This enables new applications at extreme and harsh environments and diminishes thermal handling requirements [13, 14]. The optimization and development of SiC manufacturing techniques has gradually evolved during the last years and has brought to the market power semiconductor devices ranging from the simplest diodes to more complex MOSFETs or IGBTs [15, 16, 3, 4]. Manifold circuit topologies based on SiC semiconductor devices have already demonstrated a promising increase of efficiency and achieved power density of power converters[17].

1.2 State of the art of SiC power devices characterization

The current-voltage (IV) characteristics of SiC power MOSFETs exhibit a non-saturating behavior influenced by the presence of short channel effects [18, 19] that differs from the classical flat IV characteristics of Si-devices in the high voltage saturation region. This affects the transconductance (i.e. the current commutation speed) of SiC power MOSFETs, which is strongly dependent on the V_{DS} voltage [20]. Furthermore, the IV characteristics of SiC power MOSFETs are highly sensitive to temperature variations [21, 22]. The root cause of this arises from strong temperature dependence of the density of trap states D_{it} originating from defects in the SiO_2/SiC interface of the SiC MOSFET structure [23]. Recent improvements in

the semiconductor processing techniques have achieved a substantial reduction of D_{it} [24], but a higher level of maturity of the semiconductor processing techniques is still to be achieved. Consequently, IV characterization techniques for SiC power MOSFETs require special considerations to maintain self-heating at the lowest level possible. The characterization of the IV characteristics of SiC power MOSFETs at high V_{DS} voltages and high currents results challenging due to power limitations of modern curve tracers (CT) [25]. Alternative characterization solutions such as transmission line pulse (TLP) systems can reach higher power bias conditions than a CT, but lead to excessive self-heating though [26, 27]. Recent studies propose the use of dynamic characterization fixtures such as a double pulse test (DPT) or short circuit testers (SCT) to extract the static IV characteristics of modern SiC power MOSFETs [20, 28, 29, 30]. However, these solutions suffer from a poor accuracy due to either the presence of dynamic phenomena arising from the measurement fixture or the excessive self-heating introduced in the measurements.

The intrinsic parasitic capacitances of power MOSFETs experiment a non-linear behavior function of the terminal voltages V_{DS} and V_{GS}. These determine to a large extent the dynamic behavior of the power device. More specifically the input capacitance C_{ISS} affects the current commutation interval, and the reverse transfer capacitance C_{RSS} is responsible for the voltage commutation interval (see fig. 1.1). Conventional capacitance-voltage (CV) measurement techniques restrict the CV characterization of power devices to zero-current bias conditions [31], which is not sufficient to describe the full non-linearity of the interelectrode capacitances at application bias conditions. As a result, application engineers rather rely on gate-charge measurements $Q_{\mathrm{G}} - V_{\mathrm{GS}}$, extracted at application conditions, to predict the dynamic behavior of the power switch [32, 33, 34, 35]. Such measurements have been used to infer information on more realistic values of C_{ISS} and C_{RSS} at application bias points [36, 37, 38, 39, 40]. However these methods suffer from limited accuracy and are still insufficient to reproduce the complete non-linearity of the intrinsic capacitances required for example in transistor modeling. Furthermore, the non-saturating IV characteristics of SiC power MOSFETs results in non-flat $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ characteristics which lead to an inaccurate estimation of Q_{GD} applying characterization standards developed for Si-based devices [41], a parameter often used to estimate the switching energy losses of SiC power MOSFETs.

The International Technology Roadmap for Widebandgap Power Semiconductors (ITRW) has announced the need for new measurement standards and SPICE simulation models that meet the higher grade of complexity of SiC power semiconductor devices [42]. Datasheets and transistor models, tailored for Si-based devices, need to be adapted to new SiC power devices too in order to provide application engineers key electrical parameters required to optimize the design of modern power conversion circuits [43]. The added complexity brought by SiC power MOSFETs accentuates the necessity of new measurement techniques that permit an accurate characterization of the pertinent electrical characteristics necessary to consolidate and unlock the full potential of this promising semiconductor technology in the application.

1.3 Scope of this work

This work proposes novel measurement techniques tailored for SiC power MOSFETs that permit the current-voltage (IV) and capacitance-voltage (CV) characterization at bias conditions similar or even above application power levels (See fig. 1.1). The proposed characterization techniques enable the acquisition of relevant measurement data which permits the analysis of the dynamic behavior of SiC power MOSFETs from their inherent static electrical characteristics in a comprehensive form. This is of utmost importance, among others, to optimize technology processes, improve the accuracy of switching losses prediction or generate reliable device compact models for circuit simulation.

The thesis is structured in the following manner. Chapter 2 motivates the use of vector network analyzers (VNA) as a characterization instrument for power transistors. The versatility of VNAs, in contrast with that of conventionally used impedance analyzers (ZA), enable new possibilities for the characterization of modern fast-switching power semiconductor devices. These are detailed in the comparison between VNAs and ZAs provided in the chapter. The basis of S-Parameter theory is developed and tailored for the characterization of vertical power MOSFETs. Based upon that, a measurement technique is proposed which provides higher versatility and reduce the complexity of the required measurement setup in comparison with standard characterization solutions. The proposed measurement technique permits the characterization of each individual component

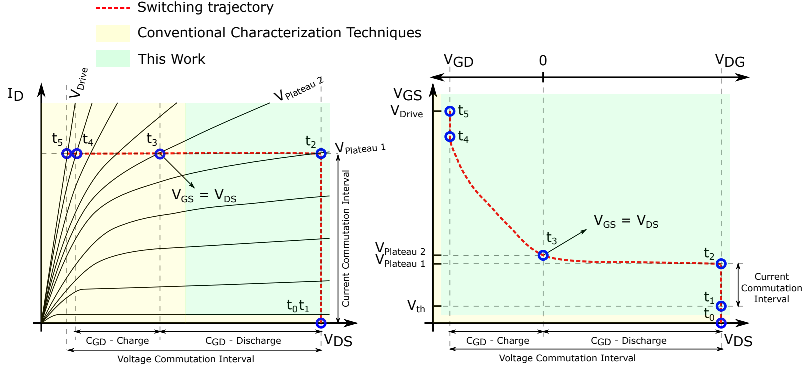
of the equivalent circuit of a vertical power MOSFET from a single measurement fixture. This includes intrinsic capacitances, extrinsic inductances, and the different resistance components contributing to the total on-resistance. Compared to standard measurement techniques that require separate measurements for each of these components, the proposed technique reduces this complexity to a single measurement and thus speeds up the overall characterization speed. A measurement setup that operates up to ± 1 kV bias voltages is presented. Furthermore, an analysis of the accuracy of the proposed methodology is provided.

Chapter 3 provides an extension of the measurement methodology presented in chapter 2, which enables the static characterization of the intrinsic capacitances of a power MOSFET under high current bias conditions from depletion mode to its linear and saturation mode operation. This permits characterize the non-linearity of intrinsic capacitances beyond the zero-current bias conditions imposed by standard characterization techniques, which is of interest to study the dynamic behavior of SiC power switches under application operating conditions. CV measurements of a commercially available SiC power MOSFET up to bias conditions of $V_{\mathrm{DS}} = 40$ V, $V_{\mathrm{GS}} = 20$ V and $I_{\mathrm{D}} = 50$ A at junction temperatures ranging from $T_{\mathrm{J}} = 25$ °C to $T_{\mathrm{J}} = 150$ °C are carried out. The results of the measurements are analyzed and contrasted with phenomena in the dynamic behavior of SiC power switches reported in recent publications. Furthermore, a method to compute the $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ characteristics of SiC power MOSFETs is presented which provides a higher accuracy for the characterization of SiC power MOSFETs than conventional techniques do and validates the capacitance measurements presented in this chapter.

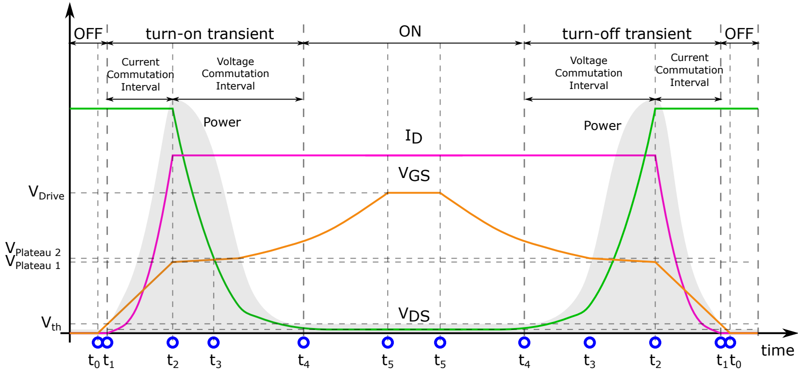
Chapter 4 proposes a novel methodology to characterize the static current-voltage (IV) characteristics of SiC power MOSFETs in the high voltage high current saturation region, beyond the power levels reached by standard IV-characterization solutions and with negligible self-heating. This unlocks the study of the IV characteristics of SiC power switches in the high power operation region, which determines its dynamic behavior. Iso-thermal static IV characteristics of a commercially available SiC power MOSFET are extracted up to 800 V and 50 A at junction temperatures ranging from $T_{\mathrm{J}} = 25$ °C to $T_{\mathrm{J}} = 175$ °C. The impact of V_{DS} and temperature in the IV characteristics of SiC power MOSFETs is discussed and contrasted with the dynamic behavior of similar SiC power devices reported in the

literature.

The measurements presented along the chapters of this work explain unclear phenomena on the dynamic behavior of SiC power MOSFETs reported in recent publications. The physical root cause of these phenomena is identified and its impact in the dynamic behavior of the SiC power device in the application is analyzed in detail in the respective chapters. Conclusions are summarized in chapter 5.



(a) Operation points covered by conventional characterization techniques (yellow) and the extended bias scope achieved by the characterization techniques presented in this work (green) in the IV Characteristics (left) and CV Characteristics (right)of a power MOSFET



(b) Sketched transient waveforms of the turn-on and turn-off commutation events of a switching cycle. The time intervals depicted correspond to the time intervals represented in figure (a).

Figure 1.1: This thesis presents novel measurement techniques that permit the characterization of the static IV and CV characteristics of a power MOSFET in the full bias scope the power device goes through in the application

Chapter 2

Characterization of the equivalent circuit of power MOSFETs based on S-Parameters

Power MOSFETs are semiconductor devices used in the application as switches, i.e. to commute between on and off steady states. In reality power MOSFETs are not ideal switches. First, their resistive nature leads to certain power dissipation both in on- or in off-state. Second, the commutation between states does not occur instantly, but requires certain time to be accomplished. The highest power peak dissipation occurs during the commutation interval.

The non-ideal behavior of a power switch arises from the parasitic components inherent in the semiconductor structure and its package [4, 35]. These parasitic components behave electrically as resistors, inductors and capacitors, which together build an equivalent circuit of the power switch. The characterization of each of these components permits understand the dynamic and static behavior of the power switch, which is essential to achieve an optimized circuit design.

The passive components of the equivalent circuit of a power transistor are conventionally characterized with methods based on the use of impedance analyzers (ZA) [31]. These instruments provide a superior accuracy in the measurement of passive devices such as resistors, inductors or capacitors [44]. Vector network analyzers (VNA) are measurement instruments widely used in microwave engineering [45, 46]. In contrast with ZAs, that measure impedances, VNAs measure scattering parameters (S-Parameters)[47, 46]. This enables the possibility to apply network theory, that comes in handy to characterize and model complex networks (such as the equivalent circuit of a transistor) in a holistic way [48, 49, 50, 51, 52]. Despite the fact

that VNAs are more versatile measurement instruments than ZAs, countless publications have reported on their use and their accuracy to characterize power devices for switching applications.

This chapter provides a comprehensive study of the viability of VNAs as potential instruments for the characterization of power transistors. S-Parameter theory is developed and tailored to characterize the equivalent circuit of vertical power MOSFETs. Based upon this theory, a measurement technique is proposed which permits the complete characterization of the equivalent circuit of vertical power MOSFETs up to high voltages from a single measurement fixture. The accuracy of the proposed methodology is also analyzed and discussed.

2.1 Vector Network Analyzer vs. Impedance Analyzer

Impedance analyzers (ZA) are measurement instruments designed specifically to precisely measure impedance values. ZAs come in handy when characterizing and modeling equivalent circuit of passive electric components such as capacitors, inductors or resistors. ZAs basically work based on the operating principle of the auto-balancing bridge [44, 53, 50]. This circuit permits to measure impedance magnitudes in the range of mΩ to MΩ in a frequency range from few Hz to 100 MHz approximately. Impedance analyzers are often used to characterize the capacitance-voltage (CV) characteristics of the inter-electrode capacitances of power transistors [31]. One of the complications of this measurement technique is that each inter-electrode capacitance requires a dedicated measurement fixture. As a result, the high complexity of the required measurement setup may lead to poor repeatability, large characterization times and introduction of human errors if the characterization work is carried out manually. Automated measurement setups solve this problem [54] and are commercially available [55, 56].

Vector Network Analyzers (VNA) are measurement instruments mainly conceived to characterize linear electrical networks when subjected to steady state stimuli [45]. They are widely used in high frequency electronics to characterize linear time-invariant system blocks such as amplifiers, filters, directional couplers [46] and to model and characterize high frequency transistors [51, 52]. VNAs handle Scat-

tering Parameters, or S-Parameters, which are complex numbers that fully describe an electrical network. These are extracted from measured incident and reflected voltage waveforms at the ports of the network [47, 46].

A comparison of the pros and cons of VNAs and ZAs for the characterization of power transistors is summarized in fig. 2.1 and discussed point by point below:

- *Accuracy*: VNAs are not originally conceived to measure impedances and are generally speaking less accurate in this matter than impedance analyzers [57, 58]. However, VNAs can also be used to characterized passive electrical components such as resistors, capacitors or inductors [59]. Indeed, the accuracy of a VNA is more than sufficient to characterize modern power transistors. In section 2.2.6 a detailed analysis of the accuracy of a VNA is provided.

- *Frequency range*: Whereas ZAs are limited to max frequencies of $\approx 100\,\text{MHz}$, VNAs operate up to hundreds of GHz. Both ZAs and VNAs can measure at very low frequencies.

- *Measurement speed*: ZAs require measurement times in the range of ms per measurement point. VNAs can measure at much faster speed and accomplish a measurement point in the µs regime at a frequency measurement of MHz. The factor thousand faster measurement speed of VNAs enables the characterization of power transistors within the biasing pulses of a curve tracer, something impossible for ZAs. This permits the biasing of the power device inside their safe operating area (SOA) at isothermal conditions. Chapter 3 develops this concept further.

- *Setup complexity*: Impedance analyzers require a dedicated measurement fixture for the characterization of each inter-electrode capacitance of a power transistor. Thus, the complete characterization of a three-terminals power transistor requires at least three independent measurements in three different fixtures. Since VNAs are conceived to characterize N-Port electrical networks, a single fixture is sufficient to completely characterize the equivalent circuit of a power transistor. This fact makes VNAs very attractive in comparison with ZAs since they demand a lower complexity of the final measurement setup. As

a result, VNAs reduce the overall characterization time and eases automation.

- *Versatility*: The fast measurement speed of VNAs and lower complexity of the measurement fixtures enable new measurement possibilities not possible for ZAs. An example of this is the measurement technique proposed in chapter 3 whicn unlocks the characterization of the intrinsic capacitances of a power transistor at high current conduction bias conditions. Thanks to S-Parameter and network theory, VNAs permit the extraction of the equivalent circuit of a transistor from a single S-Parameter measurement as detailed in section 2.3.

- *Cost*: VNAs are in general slightly more expensive than ZAs. However, for the specific application use of characterization of power transistors, considering the faster measurement speed, required lower complexity of the measurement setup and added versatility, VNAs may provide an overall cheaper solution.

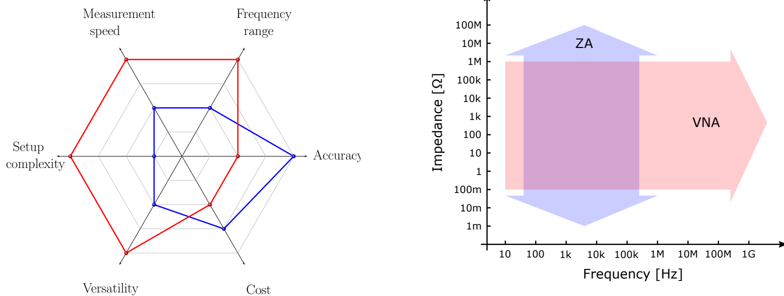


Figure 2.1: Comparison of VNA (red) and ZA (blue)

2.2 Proposed method based on Vector Network Analyzers

2.2.1 S-Parameters

Every electrical circuit can be described as electric and magnetic fields by solving Maxwell equations. However, electric or magnetic fields are complicated to handle and make difficult the behavioral modeling of an electric circuit. Classical circuit theory describes the behavior of a network by using current and voltage magnitudes instead and thus makes the analysis of circuits much easier. A magnitude that relates voltages and currents is the impedance or its inverse, the admittance. The electrical behavior of an unknown network can be totally described by an impedance or admittance matrix [Z] or [Y] that interrelates the currents coming in and out and the voltage across each port of the network.

Hence, the electrical behavior of any generic unknown network can be completely described by its impedance matrix [Z] as

$$\begin{bmatrix} V_1 \\ \vdots \\ V_{\mathrm{n}} \end{bmatrix} = \begin{bmatrix} Z_{11} & \dots & Z_{1\mathrm{n}} \\ \vdots & \ddots & \vdots \\ Z_{\mathrm{n}1} & \dots & Z_{\mathrm{nn}} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ \vdots \\ I_{\mathrm{n}} \end{bmatrix} \tag{2.1}$$

Or alternatively by its admittance matrix [Y] as

$$\begin{bmatrix} I_1 \\ \vdots \\ I_{\mathrm{n}} \end{bmatrix} = \begin{bmatrix} Y_{11} & \dots & Y_{1\mathrm{n}} \\ \vdots & \ddots & \vdots \\ Y_{\mathrm{n}1} & \dots & Y_{\mathrm{nn}} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_{\mathrm{n}} \end{bmatrix} \tag{2.2}$$

Where each component of the impedance and admittance matrices are calculated as

$$Z_{\mathrm{ij}} = \left. \frac{I_{\mathrm{i}}}{V_{\mathrm{j}}} \right|_{I_{\mathrm{k}} = 0 \text{ for k} = \mathrm{j}} \tag{2.3}$$

and

$$Y_{\mathrm{ij}} = \left. \frac{V_{\mathrm{i}}}{I_{\mathrm{j}}} \right|_{V_{\mathrm{k}} = 0 \text{ for k} = \mathrm{j}} \tag{2.4}$$

One of the limitations of using impedance or admittance magnitudes to describe high frequency circuits is the difficulty to measure

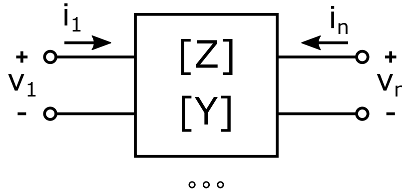


Figure 2.2: A generic N-port network can be fully described by its impedance [Z] or admittance [Y] matrices

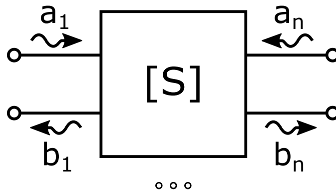


Figure 2.3: A generic N-port network can be fully described by its S-parameter matrix. Boundary conditions of S-Parameters are easier to realize at high frequencies with matched impedances than open and short conditions

current and voltage waveforms at high frequencies. Additionally, the calculation of each matrix component requires perfect open and short boundary conditions ($I_\mathrm{k} = 0$ and $V_\mathrm{k} = 0$ in equations eq. (2.3) and eq. (2.4) respectively), which is complicated to realize at high frequencies. S-Parameter theory was developed in the 60's to describe N-port arbitrary networks at very high frequencies applying circuit theory without the need of measuring instantaneous current and voltage waveforms. Different ways to define S-Parameters can be found in literature and may result confusing to the reader. Some authors such as Pozar [46] define S parameter using the concept of incident and reflected "voltage-waves". Kurokawa [47] instead uses the concept of incident and reflected "power-waves". Essentially, S-Parameter are dimensionless entities that provide a complete description of any N-port unknown network by accounting how much of a waveform applied to any port reflects in the stimulated port and how much is transmitted (or scattered) through the unknown network to the remaining ports.

An unknown N-port network can be totally characterized by its S-Parameter matrix [S]

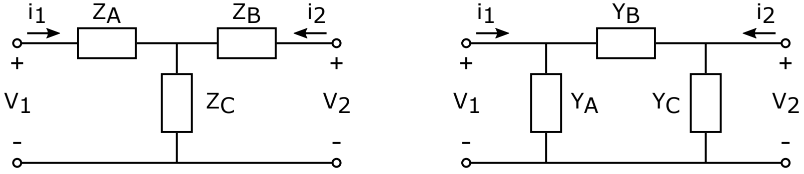


Figure 2.4: T and Π-equivalent circuit caption

$$\begin{bmatrix} b_1 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & \dots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \dots & S_{nn} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} \tag{2.5}$$

Where each component of the S-Parameter matrix S_{ij} can be calculated as

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k \,=\, 0 \text{ for } k \,=\, j} \tag{2.6}$$

The advantage of S-Parameters is that they do not require open or short boundary conditions to characterize the network, but instead, a matched load Z_k* on each port that absorbs all incident power and does not reflect any power back to the network (in equation eq. (2.6), $a_k = 0$). This is easy to achieve at high frequencies in comparison with the open and short boundary conditions required to extract [Z] and [Y] matrices. Furthermore, [Z] and [Y] can be quickly calculated from [S] by applying pertinent mathematical transformations [60, 46]. These indeed come in handy to extract the equivalent circuit of a transistor as will be seen in the following section.

2.2.2 Π- and T-equivalent circuits of a vertical power MOSFET

Impedance and admittance matrices are very powerful to characterize each component of an equivalent circuit. Most 2-port circuits can be reduced to an equivalent Π- or T-network like those shown in fig. 2.4 or nested combinations of these two as analyzed in detail in section section 2.2.3.

The [S] parameter matrix of a generic 2-port network is sufficiently self-contained to characterize each of its building components. Applying corresponding mathematical transformations, the 2-port [Z]

and [Y] parameter matrices of the equivalent T- and Π-networks can be calculated as

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} \, Z_{12} \\ Z_{21} \, Z_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (2.7) \qquad \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} \, Y_{12} \\ Y_{21} \, Y_{22} \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (2.8)$$

where[1]

$$Z_{11} = \left. \frac{v_1}{i_1} \right|_{i_2=0} \quad (2.9) \qquad Y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2=0} \quad (2.10)$$

$$Z_{21} = \left. \frac{v_2}{i_1} \right|_{i_2=0} \quad (2.11) \qquad Y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2=0} \quad (2.12)$$

$$Z_{12} = \left. \frac{v_1}{i_2} \right|_{i_1=0} \quad (2.13) \qquad Y_{12} = \left. \frac{i_1}{v_2} \right|_{v_1=0} \quad (2.14)$$

$$Z_{22} = \left. \frac{v_2}{i_2} \right|_{i_1=0} \quad (2.15) \qquad Y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1=0} \quad (2.16)$$

The zero-current $i_{\mathrm{k}} = 0$ boundary conditions (open) of impedance parameters ease the characterization of T-networks. This can be clearly seen looking at fig. 2.4. By forcing zero current in the port 2, i.e. $i_2 = 0$, the voltage drop across Z_{B} is zero and v_2 corresponds

[1] The open and short boundary conditions assumed in the ports of the network are a mathematical assumption inherited from an assumed impedance match in the ports of the VNA during the extraction of the original S-Parameter matrix.

exclusively to the voltage drop across Z_{C}. Known the current i_1, the impedance Z_{C} can be directly calculated as

$$Z_{\mathrm{C}} = \left.\frac{v_2}{i_1}\right|_{i_2=0} = Z_{21} \tag{2.17}$$

Which indeed corresponds to the parameter Z_{21} of [Z]. Known $Z_{\mathrm{C}} = Z_{21}$ and assuming $i_1 = 0$ and $i_2 = 0$ boundary conditions, the calculation of Z_{A} and Z_{B} from Z_{11} and Z_{22} is straightforward

$$Z_{11} = \left.\frac{v_1}{i_1}\right|_{i_2=0} = Z_{\mathrm{A}} + Z_{\mathrm{C}} \rightarrow Z_{\mathrm{A}} = Z_{11} - Z_{\mathrm{C}} = Z_{11} - Z_{21} \tag{2.18}$$

$$Z_{22} = \left.\frac{v_2}{i_2}\right|_{i_1=0} = Z_{\mathrm{B}} + Z_{\mathrm{C}} \rightarrow Z_{\mathrm{B}} = Z_{22} - Z_{\mathrm{C}} = Z_{22} - Z_{21} \tag{2.19}$$

In the same manner, zero-voltage $i_{\mathrm{k}} = 0$ boundary conditions (short) ease the characterization of Π-networks. Thus, Y-parameters are convenient when characterizing Π-networks (See fig. 2.4). This time, forcing zero voltage in the port 2, i.e. $v_2 = 0$, the admittance between port1 and port2, Y_{C}, can be calculated as

$$Y_{\mathrm{C}} = \left.\frac{-i_2}{v_1}\right|_{v_2=0} = -Y_{21} \tag{2.20}$$

which indeed corresponds to the negative Y_{21} parameter of [Y]. Known Y_{C} and forcing zero-voltage in the port 2 ($v_2 = 0$) and port 1 ($v_1 = 0$), the admittances Y_{A} and Y_{B} can be respectively calculated as

$$Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = Y_{\mathrm{A}} + Y_{\mathrm{C}} \rightarrow Y_{\mathrm{A}} = Y_{11} - Y_{\mathrm{C}} = Y_{11} + Y_{21} \tag{2.21}$$

$$Y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} = Y_{\mathrm{B}} + Y_{\mathrm{C}} \rightarrow Y_{\mathrm{B}} = Y_{22} - Y_{\mathrm{C}} = Y_{22} + Y_{21} \tag{2.22}$$

This analysis concludes that a transformation of the [S] matrix into impedance [Z] or admittance [Y] matrices permits the complete characterization of an equivalent T- or Π-equivalent network without the need of applying open and short boundary conditions. As a general rule, impedance parameters [Z] ease the characterization of T-networks whereas admittance parameters [Y] are convenient to characterize Π-networks.

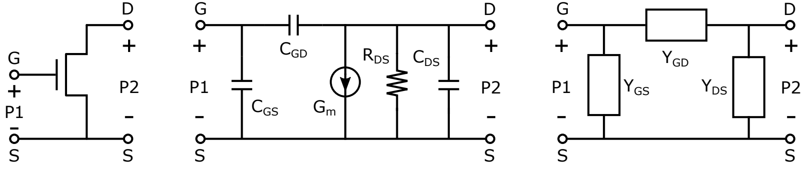


Figure 2.5: Intrinsic equivalent circuit of a 3-terminal vertical power MOSFET and its representation as a Π-structure

2.2.3 3-Terminal power device characterization with S-Parameters

A simplistic approximation of the equivalent circuit of a vertical power MOSFET, comprising its inter-electrode capacitances, can be realized with the Π-equivalent circuit shown in fig. 2.5. The gate and drain terminals referenced to a common source terminal represent port 1 and port 2 of the Π-network respectively.

According to the theory developed in section section 2.2.2, each element of the Π-equivalent structure can be easily calculated from the admittance matrix of the network [Y] which can be obtained applying mathematical transformations [60] from a 2-port S-Parameter matrix [S]. Assuming admittance notation as $Y = G + \mathrm{j} \cdot B$

$$
\begin{aligned}
[S] \rightarrow [Y] &= \begin{bmatrix} Y_{11} \, Y_{12} \\ Y_{21} \, Y_{22} \end{bmatrix} \\
&= \begin{bmatrix} 0 & 0 \\ G_{\mathrm{m}} & G_{\mathrm{DS}} \end{bmatrix} + \mathrm{j} \begin{bmatrix} B_{\mathrm{GS}} + B_{\mathrm{GD}} & -B_{\mathrm{GD}} \\ -B_{\mathrm{GD}} & B_{\mathrm{GD}} + B_{\mathrm{DS}} \end{bmatrix} \\
&= \begin{bmatrix} 0 & 0 \\ G_{\mathrm{m}} & G_{\mathrm{DS}} \end{bmatrix} + \mathrm{j}\omega \begin{bmatrix} C_{\mathrm{GS}} + C_{\mathrm{GD}} & -C_{\mathrm{GD}} \\ -C_{\mathrm{GD}} & C_{\mathrm{GD}} + C_{\mathrm{DS}} \end{bmatrix}
\end{aligned}
\tag{2.23}
$$

Thus, C_{GS}, C_{GD} and C_{DS} can be calculated from the [Y] matrix as

$$
C_{\mathrm{GD}} = \frac{-\mathrm{Im}(Y_{12})}{2\pi \cdot f} \tag{2.24}
$$

$$
C_{\mathrm{GS}} = \frac{\mathrm{Im}(Y_{11})}{2\pi \cdot f} - C_{\mathrm{GD}} \tag{2.25}
$$

$$
C_{\mathrm{DS}} = \frac{\mathrm{Im}(Y_{22})}{2\pi \cdot f} - C_{\mathrm{GD}} \tag{2.26}
$$

Figure 2.6: Equivalent circuit of a power MOSFET (left) and its representation as a Π- and T-structure (right). The red and blue regions enclose the intrinsic and extrinsic components respectively.

And so can be calculated the input capacitance C_{ISS}, the output capacitance C_{OSS} and the reverse transfer capacitance C_{RSS} of the transistor as

$$C_{\mathrm{ISS}} = C_{\mathrm{GS}} + C_{\mathrm{GD}} \tag{2.27}$$

$$C_{\mathrm{OSS}} = C_{\mathrm{DS}} + C_{\mathrm{GD}} \tag{2.28}$$

$$C_{\mathrm{RSS}} = C_{\mathrm{GD}} \tag{2.29}$$

The transconductance G_{m} and output conductance G_{DS} of the MOSFET can be calculated as

$$G_{\mathrm{m}} = \mathrm{Re}(Y_{21}) \tag{2.30}$$

$$G_{\mathrm{DS}} = \mathrm{Re}(Y_{22}) = 1/R_{\mathrm{DS}} \tag{2.31}$$

In reality, the purely capacitive Π-network assumed in this analysis is only valid in a limited frequency range in which the impedance of the inter-electrode capacitances dominates over the impedance of adjacent parasitic components such as stray capacitive coupling paths or parasitic series inductances and resistances.

A more complex equivalent network of the passive components of the transistor is provided in fig. 2.6. In this representation, the Π-network corresponding to the inter-electrode capacitances is enclosed in a T-network with parasitic series resistances and inductances. The effect of the outer parasitic shell may impact the accuracy of the inter-electrode capacitance measurements. For this reason, the equivalent circuits considered in these calculations are only valid in certain frequency range. This is the frequency range in which the impedance of

the components we want to calculate dominate over the rest of parasitics. If the values of the components of the extrinsic parasitics are well known, they can be stripped off by subtracting their impedance and applying recurrent Π-to-T conversions until reaching the inner intrinsic Π-structure. In some cases, the extrinsic parasitic shell of a fixture or a package can be characterized with FEM simulators [61].

Another way to separate the characterization of the parasitic series inductances and the intrinsic capacitances is by considering two different measurement frequencies. At low frequencies, the impedance of the intrinsic capacitances dominates over the impedance of the parasitic LR-shell and this can be neglected, thus assuming the equivalent circuit of fig. 2.5. At high frequencies, the capacitances present a negligible impedance. Hence, the equivalent circuit can be reduced to a simple T-structure comprised purely by the parasitic series inductances and resistances. Thus, a simple conversion of the S-Parameter matrix into a Z-Parameter matrix with notation $Z = R + \mathrm{j} \cdot X$

$$\begin{aligned} [S] \rightarrow [Z] &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \\ &= \begin{bmatrix} R_\mathrm{G} + R_\mathrm{S} & R_\mathrm{S} \\ R_\mathrm{S} & R_\mathrm{D} + R_\mathrm{S} \end{bmatrix} + \mathrm{j} \begin{bmatrix} X_{11} & X_{12} \\ X_{21} & X_{22} \end{bmatrix} \\ &= \begin{bmatrix} R_\mathrm{G} + R_\mathrm{S} & R_\mathrm{S} \\ R_\mathrm{S} & R_\mathrm{D} + R_\mathrm{S} \end{bmatrix} + \mathrm{j}\omega \begin{bmatrix} L_\mathrm{G} + L_\mathrm{S} & L_\mathrm{S} \\ L_\mathrm{S} & L_\mathrm{D} + L_\mathrm{S} \end{bmatrix} \end{aligned} \tag{2.32}$$

permits the characterization of each parasitic series inductance and resistance independently as

$$L_\mathrm{S} = \frac{\mathrm{Im}(Z_{21})}{2\pi \cdot f} \tag{2.33}$$

$$R_\mathrm{S} = \mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) \tag{2.34}$$

$$L_\mathrm{G} = \frac{\mathrm{Im}(Z_{11} - Z_{12})}{2\pi \cdot f} \tag{2.35}$$

$$R_\mathrm{G} = \mathrm{Re}(Z_{11} - Z_{12}) \tag{2.36}$$

$$L_\mathrm{D} = \frac{\mathrm{Im}(Z_{22} - Z_{12})}{2\pi \cdot f} \tag{2.37}$$

$$R_\mathrm{D} = \mathrm{Re}(Z_{22} - Z_{12}) \tag{2.38}$$

Where R_{G} is the gate resistance of the DUT (gate electrode + package) and the drain-source resistance of the DUT (channel resistance + Drift Resistance + source and drain contact resistance + package resistance) can be calculated, in addition to equation eq. (2.31) as

$$R_{\mathrm{DS}} = Re(Z_{22}) \tag{2.39}$$

At this point, two different ways to calculate R_{DS} have been presented, either by using eq. (2.31) or eq. (2.39). Section section 2.4.4 provides an extended explanation on the difference between the two equations, illustrated with an example and measurements. Furthermore, a method is proposed to separate the channel resistance and the drift resistance from the total on-resistance R_{DS}.

If R_{DS} can be calculated from assuming either a Π- or T-equivalent circuit, the same does not apply to the calculation of R_{G} since this is a series resistance connected to only one terminal of the DUT.

It may result trivial to the reader, but is important to highlight that in the calculation of resistances between two terminals (such as R_{GS}, R_{GD} or R_{DS}) from Y-Parameters, one can not directly apply the transformation $1/\mathrm{Re}(Y_{\mathrm{XY}})$. That is $1/G$ and differs from $1/R$.

The equations eqs. (2.33), (2.35) and (2.37) are only valid in a frequency range where their impedance dominate over the impedance of the intrinsic capacitance network. This generally occurs at high frequencies. Keeping in mind the non-linearity of the intrinsic capacitances with the applied bias voltages, a selection of a bias point at which the intrinsic capacitances are largest may ease the characterization of the parasitic inductances at lower frequencies. In some cases, the outer extrinsic parasitic shell comprised by coupling capacitances may complicate the extraction of the extrinsic inductances since these do not find a frequency range where its impedance dominate. In such case, the resonance frequency of the equivalent circuit can be used to estimate some inductance values [62, 63].

Depending on the situation, the definition of an optimal frequency for each parasitic component is not trivial and the characterization of the extrinsic parasitic shell may be tedious and uncertain. In the case the characterization of the extrinsic shell is not required, mathematical correction techniques, also known as de-embedding techniques, can be applied. These mathematical corrections extend the validity of the assumed pi equivalent circuit of fig. 2.5 up to higher frequencies

without the need to characterize any complex extrinsic parasitic shell surrounding the DUT, as further explained in section section 2.2.4.

2.2.4 Calibration and de-embedding

By means of so-called correction techniques, the phase and time delays and parasitic components existing between the reference plane of the VNA and the DUT can be subtracted. This helps improving the accuracy of the measurement setup and extends the overall measurement frequency range. The calibration of the VNA is often performed with calibration standards. These are known reference impedances that are measured, so that the VNA can apply the pertinent corrections to compensate the systematic error introduced by the measurement setup. Different standards can be defined depending on the frequency range required and the type of DUT. More information can be found in the references [64, 65, 66]. For the measurements performed in this work open-short-load-through (OSLT) standards of a Keysight 85052D calibration-kit have been used to correct all systematic error sources from the VNA to the SMA connectors of the measurement fixture. These are: VNA port adapters, phase stable cables and SMA connectors of the measurement fixture.

De-embedding is another short of correction technique. This consists in the substraction of a part of the network, often an extrinsic shell, to get access to a desired intrinsic network. An example may be a packaged transistor where the bare die is the DUT and the parasitic extrinsic shell conformed by pin leads, packaging mold and bond wires conform the surrounding extrinsic shell which introduces systematic error and that needs to be de-embedded. Depending on the frequency range and the complexity of the network to be de-embedded, different de-embedding techniques are available. In this work, the OPEN/SHORT de-embedding technique [67, 68, 69] is chosen since it offers a low complexity solution and provides good accuracy within the frequency range at which a power transistor is often characterized [37].

2.2.5 Dynamic range, ports-Power and IF-bandwidth

Mostly due to the sensitivity of its receivers, VNAs have accuracy limitations when it comes to measuring impedances. In general, the higher the signal to noise ratio (SNR) achieved in the receivers, the

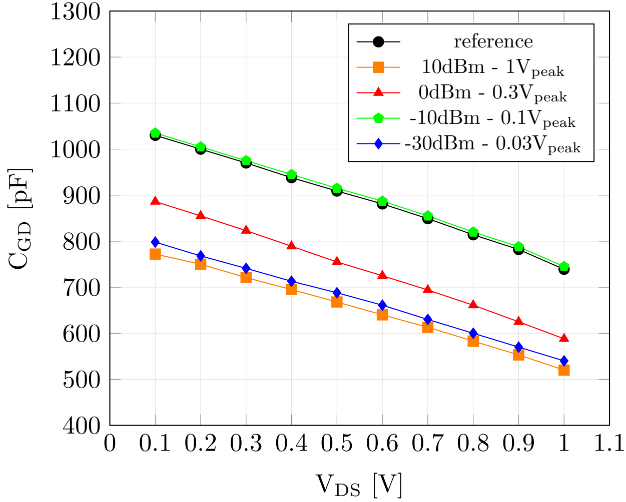


Figure 2.7: C_{GD} capacitance extracted at different RF power levels configured in the VNA. A power of -10 dBm provided the closest results to the expected value

higher the accuracy achieved in the measurement. A typical figure of merit to benchmark VNAs is their dynamic range, which is the difference between the maximum power delivered and the minimum power detectable (noise floor) at the ports of a VNA [70, 71].

The power of the ports of a VNA need to be properly adjusted prior to the measurements. In principle, the higher the power of a port, the higher the SNR achieved in the receivers and so the higher the accuracy of the measurement. This is true only if the power of the VNA doesn't exceed the limits in which the DUT can be assumed linear. The fig. 2.7 shows the measurement of C_{GD} vs V_{DS} extracted at different power levels. High power levels in the VNA stimulate the non-linearity of the capacitance and lead to a higher error introduced in the measurements. On the contrary, if the power level is too low, it may lead to a lower SNR in the receiver and so to a poor accuracy in the measurement. This criteria is used to set proper power levels in the VNA used to extract all measurements presented in this work. Power levels between -15 dBm and -10 dBm are optimal for the characterization of power transistors with the Keysight E5080A VNA used in this work.

These power levels are way below the maximum power level attained by a conventional VNA. Hence, when selecting a VNA for power transistor characterization one should pay more attention to the minimum noise floor detectable rather than the maximum power level, and separately from the dynamic range, which will mostly determine the accuracy of the VNA for these purposes. It is also important to mention that the dynamic range of a VNA is not constant in all its frequency range and it degrades near the frequency corners of the measurement equipment.

Receivers of a VNA present a superheterodyne topology [72]. This means RF signals in the receivers of the VNA are down-converted to the intermediate frequency and filtered by a band-pass filter of intermediate frequency bandwidth (IF-BW). The IF-BW of the VNA can be configured and plays an important role in the overall accuracy of the measurements. A narrow IF-BW improves the SNR in the receivers and so does improve the accuracy of the VNA. However, it also requires a higher sampling data and thus a higher time to complete the measurement. As a result, an optimal trade-off between measurement accuracy and speed needs to be found. The IF-BW needs to be selected according to the measurement frequency. A factor $f_{\text{meas}}/IF_{\text{BW}} > 100$ provides in most of the cases good accuracy.

By averaging multiple measurement samples, the effective IF-BW is reduced and the overall accuracy improved [71]. This comes in handy in situations when the measurement time per point is critical, such as in chapter 3, where the measurement time per point is restricted to the microseconds range at a measurement frequency of 1 MHz.

2.2.6 Accuracy study of a VNA

All the measurements presented in this work are performed with a Keysight E5080A which has a measurement frequency range of 9 kHz - 9 GHz, a max dynamic range of 135 dB and a minimum noise floor of -130 dBm [73].

Besides the technical characteristics of the VNA discussed in section 2.2.5, external factors also affect the accuracy of the measurements. The way a DUT is connected to the VNA determines the accuracy with which this can be characterized [59, 57, 74]. Measurement instrument manufactures may offer impedance-frequency graphs that show the boundaries where the instrument provides cer-

tain accuracy levels. However these graphs are not always provided by the manufacturer. In such cases, the characterization of the accuracy of the measurement instrument is required.

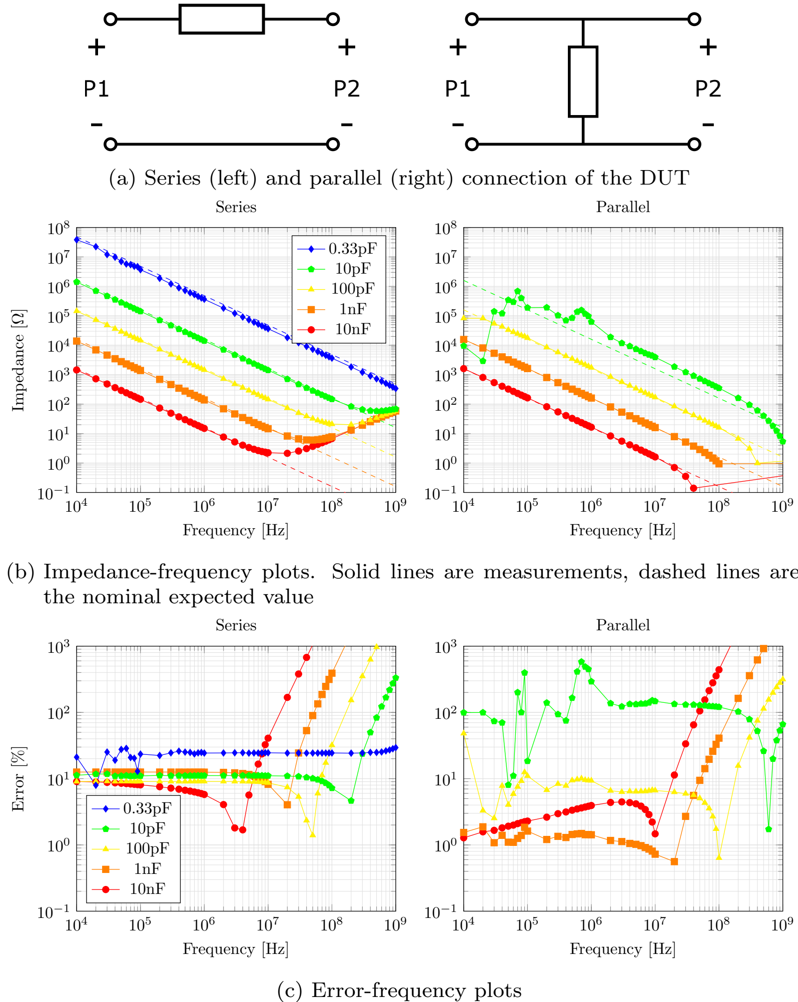
Series and parallel connections

To analyze the specific accuracy of the Keysight E5080A vector network analyzer to measure 2-port networks impedances, known capacitances of nominal value ranging from 10 nF to 0.33 pF (which are maximum and minimum values of the inter-electrode capacitances expected from a modern power transistor) have been measured in the full frequency range of the VNA. A similar analysis using a Keysight E5061B has been published in [75]. The DUTs have been connected both in series or parallel connection between port-1 and port-2 as depicted in fig. 2.8a. OSLT calibration was applied prior to the measurements and OPEN/SHORT de-embedding was used to subtract the systematic errors introduced by measurement fixture. Following the criteria described in section 2.2.5, the power of the VNA ports and the IF-BW were set to -10 dBm and 10 Hz respectively. Results of the impedance-frequency graphs extracted are plotted in fig. 2.8b. The error corresponding to the measured capacitance values with respect to the expected nominal value is also provided. The tolerance of the measured capacitors is 10 %, which needs to be considered to asses the accuracy of the measurements.

The measurement results show that a series connection of the DUT yields to the best accuracy when measuring large impedances, whereas a parallel connection is better suited to measure small impedances. Capacitances in the range of 10 nF - 0.33 pF were measured with low error in the frequency range of 10 kHz - 10 MHz in series connection. Whereas a parallel connection of the same capacitances provided poor accuracy to measure values below 10 pF in the same frequency range.

Influence of adjacent components in complex networks

When considering a network comprised by multiple components, each component of the network affects the overall accuracy with which the rest of components can be characterized. As an example, let us assume the basic equivalent Π-structure that forms the inter-electrode capacitances of a 3-terminal power MOSFET like that seen in fig. 2.5. If C_{GS} is an ideal infinite capacitor, the RF signals sent from port



(a) Series (left) and parallel (right) connection of the DUT

(b) Impedance-frequency plots. Solid lines are measurements, dashed lines are the nominal expected value

(c) Error-frequency plots

Figure 2.8: Accuracy analysis of the Keysight E5080A VNA in performing 2-port measurements in series (left) and parallel (right) connection. The DUTs are 0603 SMD capacitors with 10% tolerance. Results of the 0,33 pF capacitor measurements (blue) were omitted in the right hand plots due to the poor accuracy achieved in parallel connection

1 and port 2 of the VNA will be shorted to ground and the transmission parameters S_{21} and S_{12} will never be successfully measured (the power received in the receivers will be below the noise floor). As a result of this, C_{GD} could not be characterized. Furthermore, the complexity of the problem increases if the non-linearity of the capacitances is considered. Depending on the technology of the DUT, the range between maximum and minimum value of each inter-electrode capacitance may affect the accuracy of the setup at certain bias points. As a result of this, the optimal measurement frequency may differ at different bias-points in order to compensate the change in impedance arising from the capacitances non-linearity. This means, when characterizing each component of a network, the effect of the adjacent components integrating the network and their non-linearity with the bias point must be considered. A value that remains constant when plotted in frequency may not be the real value, but suffer from error influenced by adjacent components.

A very challenging characterization case is presented with power transistors at bias voltages beyond their threshold voltage. The low on-resistance of these may lie in the range of a few mΩ. This creates a low impedance path to ground to the RF signals that complicates the characterization of the transmission components. In the case of a MOSFET with the equivalent circuit of fig. 2.5, this affects particularly C_{GD} and any other component connected to port 2.

In order to analyze and quantify this phenomena, a measurement fixture that replicates a simplified structure of the parasitics of a power MOSFET (like that shown in fig. 2.9) has been constructed using different combinations of capacitors and resistors of known value. For sake of simplicity, C_{DS} has been omitted since this capacitance is simply not measurable when R_{DS} presents a low impedance. In this study, C_{GS} was chosen as a constant capacitance with a typical value of 1 nF. In order to find out the accuracy limits of the proposed characterization technique, C_{GD} and R_{DS} were chosen as small as 1 pF and 5 mΩ respectively. These are extreme values that can be found in state-of-the-art power MOSFETs.

The fig. 2.10 a) and b) show the values of C_{GS}, C_{GD} and R_{DS} extracted at different combinations of values. Curves plotted in green represent values which could be accurately measured in a wide frequency range. Curves plotted in yellow show values that were measured with good accuracy but in a limited frequency range. Curves plotted in red show values which could not be characterized. These

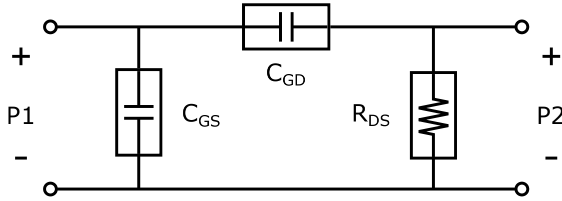


Figure 2.9: Equivalent circuit of the proposed measurement fixture used to study the influence of the impedance of each component of a Π-structure in the accuracy achieved to characterize the complete network

results are summarized in table 2.1 with the same color code. Results show a strong influence of R_{DS} in the accuracy and frequency range within C_{GD} can be characterized. C_{GD} values smaller than 10 pF could not be characterized for R_{DS} values below 5 mΩ.

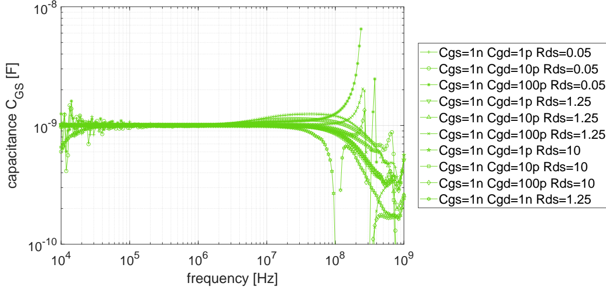
The results here presented serve just an example to illustrate how each component of a Π-equivalent network may affect the accuracy within which the others can be characterized. However, these results should not be considered as an accurate reference. Indeed a different measurement setup may yield different values. No bias-tees were attached to the PCB-fixture. The size of the PCB-fixture was designed relatively large to easy the mount of the components. OPEN/SHORT de-embedding of this was carried out to subtract the error introduced by the feeding lines. The SMD components assembled are not ideal and contain parasitics that limit the accuracy of the measurements. A power transistor have smaller parasitic series inductances and might be able to be characterized beyond the boundaries defined in this study.

From these results, the following conclusions have been summarized:

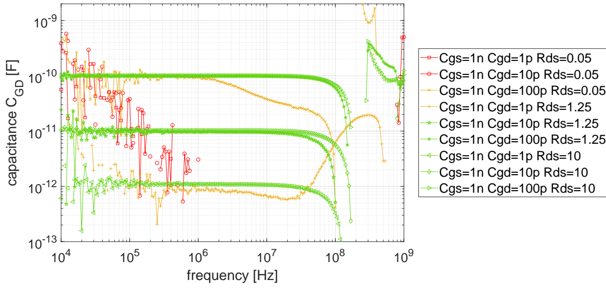
- The accuracy to characterized C_{GS} is in general not drastically affected by C_{GD} or R_{DS}.

- The value of R_{DS}, if too small, reduces the accuracy and frequency range within which C_{GD} can be characterized.

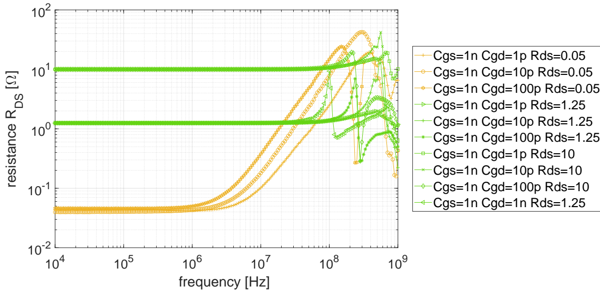
- C_{GD} affects also the accuracy within which R_{DS} can be characterized. The higher C_{GD}, the lower the maximum frequency at which R_{DS} can be characterized.



(a) Measured C_{GS} plotted vs. frequency



(b) Measured C_{GD} vs. frequency



(c) Measured R_{DS} vs. frequency

Figure 2.10: Frequency range and accuracy in the extraction of the components of equivalent Π-structure of fig. 2.9 for different value combinations

C_{GS} [nF]	C_{GD} [pF]	R_{DS} [Ω]
1	1	0.05
1	10	0.05
1	100	0.05
1	1	1.25
1	10	1.25
1	100	1.25
1	1	10
1	10	10
1	100	10

Green - Characterized in a wide frequency range
Orange - Characterized in a limited frequency range
Red - Could not be characterized

Table 2.1: Combinations of C_{GS}, C_{GD} and R_{DS} measured. The color code indicates the accuracy with which each component could be measured

2.3 High voltage S-Parameters characterization

VNA raw measurements are presented to the user as touchstone files or S-parameter files. These contain the information that describes a linearization of the equivalent circuit of the DUT at a fixed bias condition. To accomplish the basing of the DUT and an accurate extraction of its S-Parameters, an appropriate measurement setup and a post-processing of the measurement data are required. This section presents a measurement setup and the characterization steps to accomplish the complete extraction of the equivalent circuit of a power MOSFET from S-Parameter measurements under no current conduction conditions up to very high bias voltages.

2.3.1 Proposed measurement setup

The inter-electrode capacitances of power MOSFETs present an acute non-linearity of their value function of the applied terminal voltages. Power MOSFETs may operate up to thousands of volts. A measurement setup must be able to cover such biasing conditions without

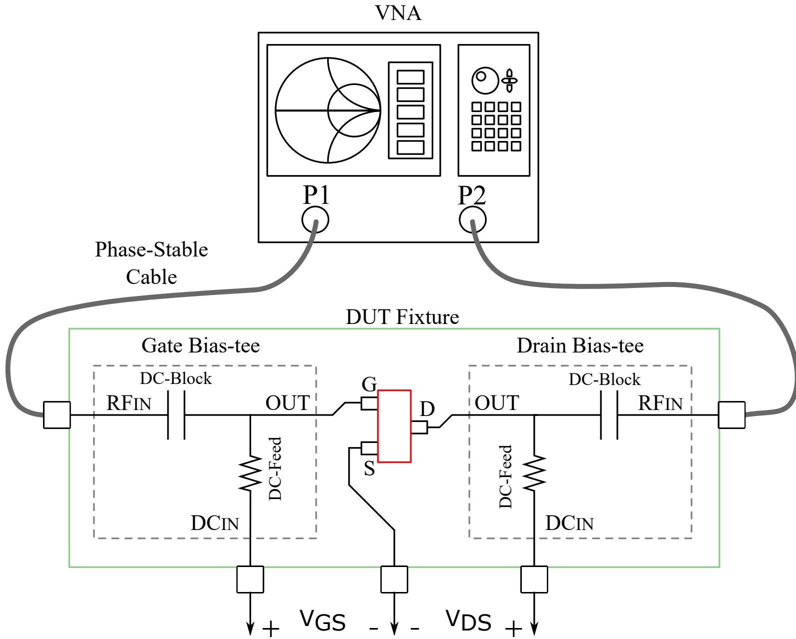


Figure 2.11: Block diagram of the proposed measurement setup. The high voltage bias-tees are integrated in the measurement fixture to minimize the parasitic series inductance of the measurement setup

harnessing the measurement instruments.

The proposed measurement setup consist of a VNA, two power supplies and two bias-tees arranged as shown in figure fig. 2.11 and has been published in [75]. This measurement setup can be extended to characterize 4-terminal devices, such as power GaN HEMTs, by adding an extra port in the VNA, an extra power supply and the corresponding additional bias-tee to the proposed measurement setup. More information on this extended characterization setup and its application has been published in [76, 77].

The VNA sends and receives RF-signals at different frequencies that are later postprocessed to calculate the equivalent circuit of the DUT at a desired bias condition. The power supplies provide the DC-voltage biasing for the gate and drain terminals. The two bias-tees combine in the DUT terminals the RF signals of the VNA with

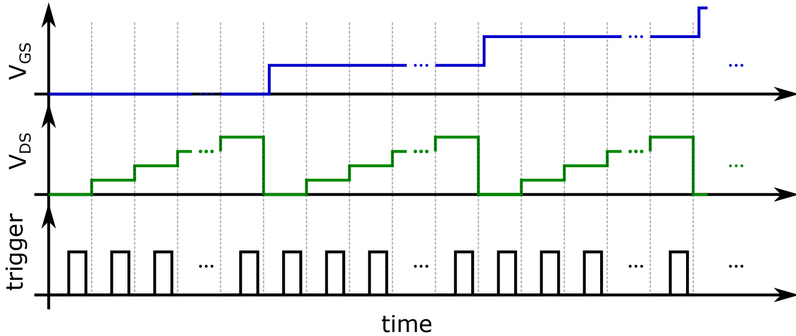


Figure 2.12: Time profile of the biasing pulses and the trigger signal sent to the VNA

the DC biasing of the power supplies while isolating VNA and power supplies from each other. More information about the bias-tees is provided in section 2.3.1.

Keysight N9910X-708 3.5mm(m)-3.5mm(m) rugged phase-stable RF cables are used in the measurement setup. These cables guarantee no change in phase and characteristic impedance of the cable under certain bending radius. With that, we ensure that a calibration performed prior to the measurements is still valid after bending the cables in the process of accommodating the DUT in the measurement setup.

The VNA used in this measurement setup is a Keysight E5080A with a frequency range of 9 kHz - 9 GHz and 4 ports. Thus, both 2- and 3-port S-Parameter measurements enables the characterization of 3- and 4-terminal devices respectively.

Two types of power supplies provide the DC bias voltages in the different terminals of the DUT. The gate of the DUT does not require high voltage biasing. Hence, a power supply with a voltage range of ±20 V is sufficient for most type of power transistors. The Drain terminal however requires high voltage biasing. A Keithley 2557A SMU, connected to Drain, supplies voltages up to ±3 kV. The Kelvin contacts of the SMU permit an accurate voltage set in the DUT even for leaky devices.

VNA and power supplies are all connected to a common LAN together with a PC with LabView. The PC centralizes the control of all the measurement equipment involved in the measurement setup

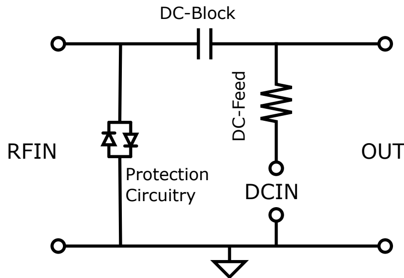


Figure 2.13: Equivalent circuit of a bias-tee with a resistive DC-Feed component.

and automates the biasing and S-Parameter measurements. The automation of the measurement setup abstracts the characterization process from human interaction and human errors and permits the very fast acquisition of measurements. A time line of the waveforms and events involved in the CV characterization process is provided in fig. 2.12. A LabView driver controls all the components of the setup and defines a delay between measurements to guarantee that, before triggering the VNA, the bias voltages are properly set in the DUT.

High voltage bias-tees

Bias-tees are passive circuits that combine a DC and an RF signal into an output port. A peculiarity of bias-tees is that they guarantee isolation between the two input ports (DCIN and RFIN) while minimizing the transmission losses from the input ports to the output port (OUT). These circuits can be realized in different ways depending on the requirements.

The DCIN-OUT „DC-Feed“ branch must present a high impedance at the measurement frequency and can be implemented either with an inductor or with a resistor. In the case that concerns high voltage measurements, the DUT is biased below its threshold voltage and no current flows through its channel. Thus, the DC-Feed branch can be simply realized with a large resistor that presents a high impedance to the AC signal coming from RFIN port in a very wide frequency range. This simplifies the design requirements and performs very well for the purpose of this measurement setup.

The RFIN-OUT „DC-block“ branch is realized with a high volt-

age capacitor. The value of this capacitor is designed to present a negligible impedance in the frequency range of the RF signal. A good practice from the author's experience is to use a value of capacitance at least 2-3 orders of magnitude higher than the highest value of capacitance to be measured. The capacitor must be able to withstand the biasing voltages and introduce the lowest possible series inductance ESL and series resistance ESR in the measurement setup. Ceramic capacitors offer a good solution for this purpose. If a very large voltage measurement setup is required, eletrolitic capacitors may be more suitable at the cost of adding a higher series inductance.

To select the adequate resistor and capacitance values, the designer must take into account the charging and discharging times „tau“ of the equivalent RC circuit. A very large resistor, provides a very good RFIN-DCIN isolation, but also a slow „tau“ time constant of the RC circuit. This means the use of large resistors may result in larger required "setting times" between measurements at different bias voltages to guarantee that the bias voltage has been properly set in the DUT. A large capacitance value presents a desirable low impedance path to the RFIN-OUT branch. However, it will also lead to longer „tau“ charge/discharge time. Furthermore the energy store in the bias-tee capacitor also needs to be consider since this may lead to a harmful setup in case of faulty DUTs.

A very important aspect to consider in the design of a bias-tee is the protection of the VNA. Hazardous voltage spikes or surge currents may damage the ports of the VNA during the DC-Block capacitor charging/discharging transients. An extreme case may be presented in the hypothetical case that DUT fails and creates a sudden short to ground. For example if the DUT breaks during the test. In such case, the DC-block capacitor will quickly discharge through the port of the VNA destroying it. To avoid this, an antiparallel diode circuit connected to the port of the VNA provides an alternative path for surge currents and acts as transient voltage suppressor. The $\pm 0.7\,\mathrm{V}$ calmping voltage of the diodes limits the maximum RF-power that can be used by the VNA though. Since the -10dBm RF-Power recommended in section 2.2.5 corresponds to a voltage below $0.7\,\mathrm{V}$, the diodes will not distort the RF-Signal used in the measurement setup.

The traces interconnecting the different components of the bias-tee were designed as $50\,\Omega$ characteristic impedance microstrip lines at a frequency of $1\,\mathrm{MHz}$. This minimizes wave reflections in the SMA-microstrip transitions and optimize the overall frequency response of

Component	Manufacturer	Series	Characteristics
DC-Block cap. gate bias-tee	Epcos	Z5U2F4	0.22 µF / 25 V
DC-Block cap. drain bias-tee	Murata	KRM55	0.22 µF / 1 kV
DC-Feed resistor drain & gate bias-tee	Yaego	MPF	100 kΩ / 0.25 W
Protection diodes drain bias-tee	Toshiba	1SS427	80 V / 10 mA / 0.3 pF

Table 2.2: List of components used for the high voltage bias-tees in the proposed measurement setup

the bias-tee in the targeted frequency range of 100 kHz - 10 MHz.

To minimize the parasitic series inductance introduced in the setup, and so achieve the broadest measurement frequency range, the bias-tees and DUT fixture are integrated in the same PCB as shown in fig. 2.15. A modular solution with separated DUT fixture and bias-tees does also the work and may be more versatile in some cases. For example in a setup tailored to measure a large number of DUTs.

The components of the proposed high-voltage bias-tee are summarized in table 2.2 and permit the characterization of power transistors up to ± 1 kV. The voltage range of the presented setup may be increased by serializing capacitors (creating a voltage divider) or using capacitors of a hihger voltage class.

2.4 Power MOSFET equivalent circuit characterization

The equivalent circuit of a vertical power MOSFET is depicted in fig. 2.14. The inter-electrode capacitances C_{GS}, C_{GD} and C_{DS} form an inner Π-structure and are assumed constant at a fixed bias point. For sake of simplicity, only the two major contributors to the on-resistance of the transistor, i.e. the channel resistance R_{Ch} and the epi-layer resistance R_{Drift}, are considered. The contact resistance of each electrode R_{cx}, parasitic series resistance $R_{\mathrm{x_ext}}$ and inductances L_{x} due to package and bond wires conform a T-shaped parasitic shell that wraps the intrinsic Π-network. This in turn is also surrounded by

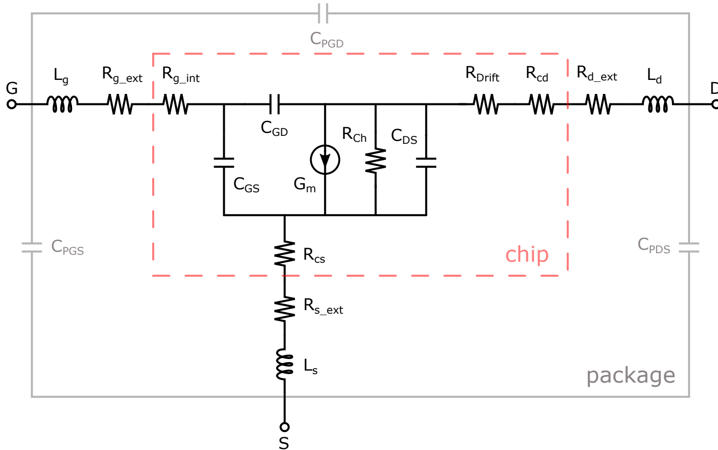


Figure 2.14: Equivalent circuit of a vertical power MOSFET

the parasitic capacitances C_{PGS}, C_{PGD} and C_{PDS} that model the coupling effects between the pins of the transistor package.

The theoretical basis to extract each of the aforementioned components of the equivalent circuit of a power MOSFET was provided in section 2.2.3. In section 2.2.6 it was also discussed that the extraction of each of these components was influenced by the adjacent components in the network. The boundaries of the accuracy of the proposed method can thus not be generalized and may change depending on the selected DUT.

This section provides a characterization sequence that permits the extraction of each of the components comprised in the equivalent circuit of a power MOSFET (see fig. 2.14) using the measurement setup proposed in section 2.3.

The complete characteriaztion of the equivalent circuit of a commercially available Silicon power MOSFET, the RDR005N25 [78], is extracted step by step to illustrate the proposed characterization method. This transistor features a very small C_{GD}, in the range of femtoFarads, that serves as a proof of the accuracy of the proposed measurement methodology. A photo of the DUT fixture with integrated bias-tees connected to the VNA and power supplies is shown in figure fig. 2.15.

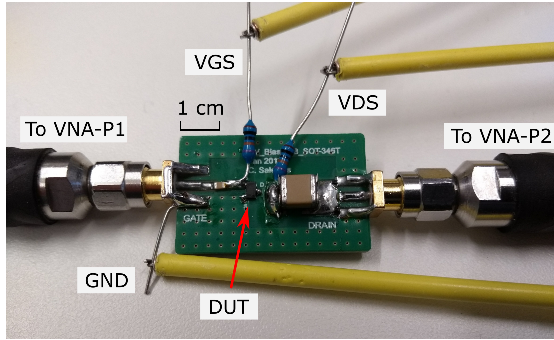


Figure 2.15: Photo of the 40x25 mm^2 measurement fixture with integrated bias-tees and the RDR005N25 as DUT. Bias tees are de-embedded using OPEN/SHORT de-embedding fixtures.

2.4.1 C-$V_{\mathbf{DS}}$ characterization

The variation of the inter-electrode capacitances with V_{DS} was extracted using eqs. (2.24) to (2.26) at $V_{\mathrm{GS}} = 0$ V. The values of C_{GS}, C_{GD} and C_{DS} versus V_{DS} at a frequency of 1 MHz are shown in fig. 2.16. On the right side of the figure, the maximum and minimum values of each capacitance are plotted versus frequency. This frequency plot is helpful to check within which frequency range the assumed equivalent circuit, and so the extracted measurements, are valid. This is the frequency range in which the values are frequency independent and thus remain constant. In case of this device, the measurement setup covers the complete range of variation of all inter-electrode capacitances with accuracy in almost 2 frequency decades, from 100 kHz to 100 MHz.

The characterization of the intrinsic capacitances of a power transistor with respect to V_{DS} at a fixed V_{GS} bias value below the threshold voltage is very often performed and used as a measure to characterize the dynamic behavior of the power MOSFET. These graphs are often provided by manufacturers and used to generate transistor models.

2.4.2 C-$V_{\mathbf{GS}}$ characterization

Less often seen in literature and practice is the study of the inter-electrode capacitances dependence of the gate-source voltage V_{GS}.

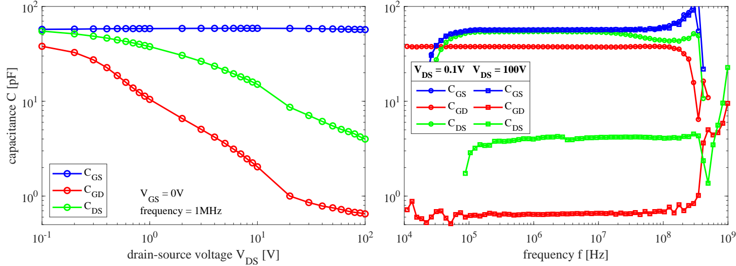


Figure 2.16: Extracted capacitances plotted versus drain-source voltage (left) and frequency (right)

Varying V_{GS} makes the transistor experience physical variations that are reflected on its intrinsic capacitance values. Figure fig. 2.17 shows the inter-electrode capacitances C_{GS}, C_{GD} and C_{DS} vs V_{GS} extracted using eqs. (2.24) to (2.26) at a constant bias condition $V_{\mathrm{DS}} = 0$ V. Three different operation modes can be identified in fig. 2.17 left according to the V_{GS} value. From left to right: accumulation, depletion and strong inversion. C_{GS} and C_{GD} could be successfully characterized in the complete range V_{GS} without problems. However, C_{DS} could not be characterized in inversion mode (i.e. when $V_{\mathrm{GS}} > V_{\mathrm{th}}$). The small on-resistance of the inversion layer, in parallel with C_{DS}, creates a low impedance path to the RF-signal of the VNA that bypasses C_{DS} as discussed in section section 2.2.6.

The right plot of fig. 2.17 shows how the maximum and minimum values of the capacitances could be accurately extracted in the frequency range of 100 kHz to 20 MHz.

2.4.3 R_{Gint} characterization

The total gate resistance R_{G} of the equivalent circuit of the DUT (see fig. 2.14) can be extracted using eq. (2.36) as discussed in section 2.2.3.

High frequencies are generally ease the characterization of R_{G} since the impedances of C_{GS} and C_{GD} become negligible. However, very high frequencies may lead to skin effect which appears as a frequency dependence of the extracted values in the measurements. Thus, an optimal frequency for the characterization of R_{G} must find a trade off between these two effects.

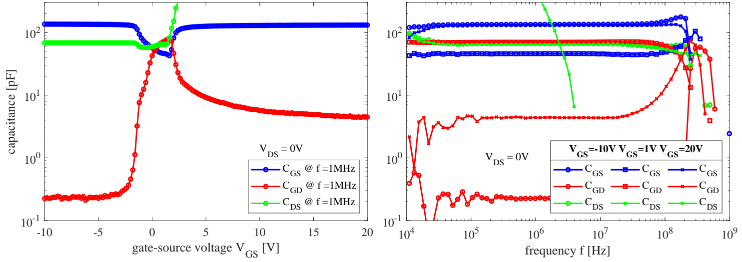


Figure 2.17: Extracted capacitances plotted versus gate-source voltage (left) and frequency (right)

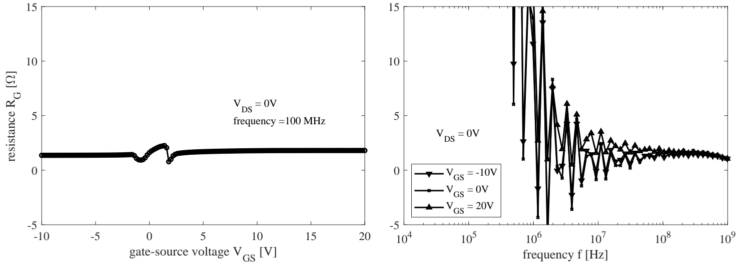


Figure 2.18: Extracted R_{G} plotted versus gate-source voltage (left) and frequency (right)

The optimal frequency range for the characterization of R_{G} in this DUT can be obtained by looking at the frequency plot of fig. 2.18, which reveals an optimal value in the range of 50 MHz - 500 MHz.

The impact of V_{GS} in the extraction of R_{G} seems to be negligible from the results plotted at V_{GS} = -10 V (accumulation), V_{GS} = 0 V (depletion) and V_{GS} = 20 V (inversion).

A slight error in the measurements can be appreciated at the threshold and flatband voltages of the device. This is attributed to the physical fluctuations at these two boundaries between accumulation-depletion-inversion regions. The value of R_{G} measured in the depletion region is a measurement artifact (an thus an invalid) arising from to the large C_{GD} to C_{GS} ratio (see fig. 2.17). This phenomena and its impact in the accuracy of the measurements was discussed and analyzed in section 2.2.6.

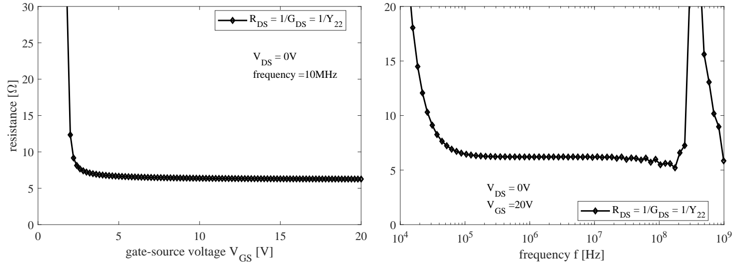


Figure 2.19: Extracted R_{DS} plotted versus gate-source voltage (left) and frequency (right)

2.4.4 R_{DS} characterization

R_{DS} represents the total resistance between drain and source terminals. This value can be extracted as $1/G_{\mathrm{DS}}$ from Y_{22} using eq. (2.31). The fig. 2.19 shows the extracted value of R_{DS} versus V_{GS} at $V_{\mathrm{DS}} = 0$ V at an optimal frequency of 10 MHz. The measured total on-resistance $R_{\mathrm{DS_ON}} = 6.4\ \Omega$ correlates exactly with the expected typical value provided by the manufacturer in the dathaseet [78]. The measurement setup could extract the R_{DS} of this specific DUT within almost 3 frequency decades, i.e. from 100 kHz to 100 MHz.

R_{DS} requires a more in-depth analysis indeed. As depicted in figs. 2.14 and 2.20 this is comprised by by the series construction of the following extrinsic and intrisic components:

- $R_{\mathrm{d_ext}}$ and $R_{\mathrm{s_ext}}$ are the series resistance of the package lead and the bond wire in the drain and source terminals respectively.
- R_{cd} and R_{cs} are the contact resistances of the drain and source electrodes respectively. These are considered constant in this analysis, though they may be temperature dependent.
- R_{Drift} is the epi-layer or drift-region resistance.
- R_{Ch} is the channel resistance.

Whereas $R_{\mathrm{d_ext}}$, $R_{\mathrm{s_ext}}$, R_{cd}, R_{cs} are bias-independent, both R_{Drift}, and R_{Ch} are bias-dependent resistances.

This work assumes $R_{\mathrm{Ch}} = \mathrm{f}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$ and $R_{\mathrm{Drift}} = \mathrm{f}(V_{\mathrm{DS}})$.

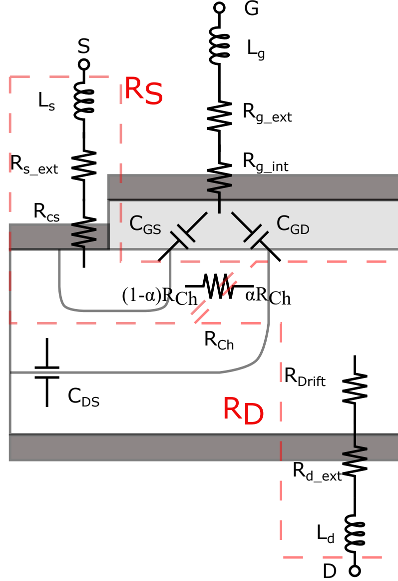


Figure 2.20: Simplified cross section of a vertical power MOSFET and its passive parasitic components. R_{D} can be extracted from eq. (2.38) and R_{S} from eq. (2.34). The channel resistance R_{Ch} is shared between R_{D} and R_{S} components by a factor α. For simplification, only the dominant parasitic components are sketched in the plot

R_{Drift} is in general the limiting component of the total on resistance since its lowest value is intrinsic to the semiconductor electrical properties that conforms the substrate. In other words, R_{Drift} determines the technological limit of a high voltage vertical power MOSFET. The higher the voltage rating of the device, the higher this resistance gets. TCAD simulations [4, 79] or measurements on specific wafer structures [80] show a dominant R_{Drif} in strong inversion and dominant R_{Ch} in weak inversion mode of power MOSFETs. Figure 6.a in [80] shows the ratio of $R_{\mathrm{Drift}}/(R_{\mathrm{Drift}} + R_{\mathrm{Ch}})$ for a Si MOSFET at different bias points. MOSFETs with different voltage classes, due to their different geometry, have a different ratio in the values of these resistors [32].

Each of these resistive components of R_{DS} have indeed different temperature coefficients and voltage dependencies. As a result, the

individual characterization of these is of interest for tasks such as technology benchmarking, process optimization or transistor modeling. The methodology proposed in the next lines provides a solution to this problem.

The total drain-source resistance of the MOSFET R_{DS} can be extracted from eq. (2.31) as

$$\begin{aligned} R_{\mathrm{DS}}\Big|_{V_{\mathrm{GS}}>V_{\mathrm{th}}} &= \underbrace{R_{\mathrm{d_ext}} + R_{\mathrm{cd}} + R_{\mathrm{Drift}} + \alpha \cdot R_{\mathrm{Ch}}}_{R_{\mathrm{D}}} \\ &+ \underbrace{(1-\alpha) \cdot R_{\mathrm{Ch}} + R_{\mathrm{cs}} + R_{\mathrm{s_ext}}}_{R_{\mathrm{S}}} \end{aligned} \tag{2.40}$$

where the components R_{D} and R_{S} can be calculated separately from eqs. (2.34) and (2.38) respectively. The parameter α depends on the transistor characteristics and represents how much percentage of R_{Ch} belongs to R_{D} and R_{S}.

At a bias point below the threshold voltage of the DUT, R_{Ch} is very large, in the range of MΩ. Selecting a frequency relatively high, R_{Ch} can be bypassed through C_{DS} (see figs. 2.14 and 2.20). Thus, applying eq. (2.31), the sum of $R_{\mathrm{d_ext}} + R_{\mathrm{cd}} + R_{\mathrm{Drift}} + R_{\mathrm{s_ext}} + R_{\mathrm{cd}}$ can be calculated as

$$R_{\mathrm{DS}}\Big|_{V_{\mathrm{GS}}<V_{\mathrm{th}}} = R_{\mathrm{d_ext}} + R_{\mathrm{cd}} + R_{\mathrm{Drift}} + R_{\mathrm{cs}} + R_{\mathrm{s_ext}} \tag{2.41}$$

Assuming R_{Drift} does not change much with V_{GS}, the channel resistance of the DUT R_{Ch} in strong inversion can be then approximated using eqs. (2.40) and (2.41) as

$$R_{\mathrm{Ch}} = R_{\mathrm{DS}}\Big|_{V_{\mathrm{GS}}>V_{\mathrm{th}}} - R_{\mathrm{DS}}\Big|_{V_{\mathrm{GS}}<V_{\mathrm{th}}} \tag{2.42}$$

Thus, known R_{Ch} from eq. (2.42), the total extrinsic resistance in the source terminal can be calculated from eq. (2.34) as

$$R_{\mathrm{ext_s}} + R_{\mathrm{cs}} = R_{\mathrm{S}}\Big|_{V_{\mathrm{GS}}>V_{\mathrm{th}}} - (1-\alpha) \cdot R_{\mathrm{Ch}}\Big|_{V_{\mathrm{GS}}>>V_{\mathrm{th}}} \tag{2.43}$$

In a similar manner, the total extrinsic drain resistance in series with the drift resistance R_{Drift} can be calculated from eq. (2.38) as

$$R_{\mathrm{Drift}} + R_{\mathrm{ext_d}} + R_{\mathrm{cd}} = R_{\mathrm{D}}\Big|_{V_{\mathrm{GS}}>V_{\mathrm{th}}} - \alpha \cdot R_{\mathrm{Ch}}\Big|_{V_{\mathrm{GS}}>>V_{\mathrm{th}}} \tag{2.44}$$

Short channel transistors at a strong inversion bias conditions $V_{\mathrm{GS}} >> V_{\mathrm{th}}$, it can be assumed that the channel resistance R_{Ch} is divided half and half between the components R_{S} eq. (2.34) and R_{D} eq. (2.38). i.e. $\alpha \approx 0.5$. Furthermore, let us assume the total extrinsic resistance of the drain and source contact are equal in magnitude[2] i.e. $R_{\mathrm{cd}} + R_{\mathrm{d_ext}} = R_{\mathrm{cs}} + R_{\mathrm{s_ext}}$. Thus, the Drift resistance of the transistor R_{Drift} can be approximated from eqs. (2.34) and (2.39) as

$$R_{\mathrm{Drift}} = R_{\mathrm{DS}}\Big|_{V_{\mathrm{GS}}>>V_{\mathrm{th}}} - 2 \cdot R_{\mathrm{S}} = \mathrm{Re}(Z_{22} - Z_{21}) - 2 \cdot \mathrm{Re}(Z_{12}) \quad (2.45)$$

With that, the contribution of the drift resistance and channel resistance to the total drain-source resistance R_{DS} can be calculated from eqs. (2.42) and (2.45) as

$$K = R_{\mathrm{Drift}}/(R_{\mathrm{Drift}} + R_{\mathrm{Ch}}) \quad (2.46)$$

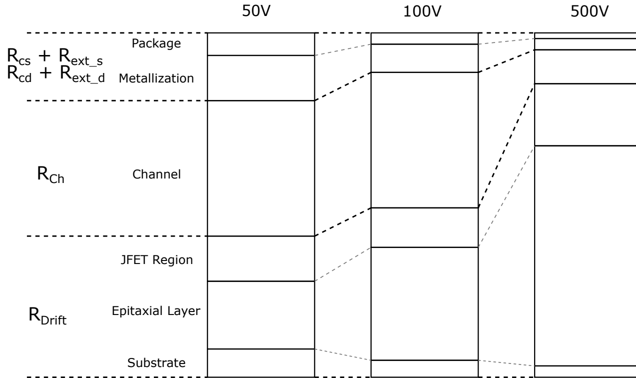


Figure 2.21: Breakdown of R_{DSon} of a vertical power MOSFET in its different components for different voltage classes. Adapted from [32]

The values of extracted from eqs. (2.34), (2.38) and (2.39) are plotted in black in fig. 2.22 left. These are used to extract the channel resistance (red curve) and the drift resistance (green curve) using

[2]Vertical power MOSFETs often feature a smaller parasitic resistance in the drain terminal than in the source terminal due to the fact that the source pads growth on top of the chip with the gate pads occupy slightly less area than the bottom of the chip or drain pad. If the chip structure is known, a correction factor can be applied.

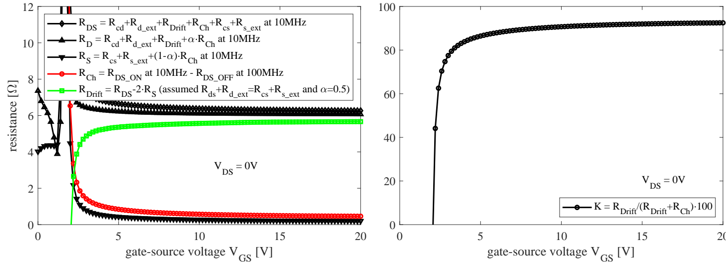


Figure 2.22: Different resistance components extracted from eqs. (2.34), (2.38), (2.39), (2.42) and (2.45) in descending order (left) and the K value extracted from eq. (2.46) (right)

Parameter	Measurement	Reference	Source of reference
total$R_{\mathrm{DS_on}}$	6.41 Ω	6.8 Ω	Typ. in datasheet [78]
$R_{\mathrm{cs}} + R_{\mathrm{ext_s}}$	0.28 Ω	0.3 Ω	SPICE Model [81]
R_{Ch}	0.57 Ω	NA	NA
R_{Drift}	5.56 Ω	NA	NA
K	90.7 %	90 %	TCAD simulations in [80, 32]

Table 2.3: Total $R_{\mathrm{DS_on}}$ and breakdown of its components: channel, drift region and extrinsic resistances of the DUT at $V_{\mathrm{DS}} = 0$ V and $V_{\mathrm{GS}} = 10$ V. The K factor serves as reference to prove the accuracy with which the channel and drift resistances are characterized

eqs. (2.42) and (2.45) respectively. The value of K calculated from eq. (2.46) is plotted in fig. 2.22 right. These values are summarized in table 2.3 for the bias point $V_{\mathrm{GS}} = 10$ V. The value of the extrinsic resistances $R_{\mathrm{cs}}+R_{\mathrm{ext_s}}$ correlates well with the 0.3 Ω parasitic resistor defined in the PSPICE model provided by the vendor. The manufacturer does not provide any information of R_{Ch} and R_{Drift} values that can be contrasted with the measurements here shown. However, the evolution of K with V_{GS} correlates well with results of TCAD simulations of a similar device in [80] and with the expected values from a device of its voltage class (250V)[32] saturating to a value of 90 % at max V_{GS}. This together with the fact that the total on-resistance and the parasitic series resistances correlate well with values provided by the manufacturer is a proof that the calculated values for R_{Ch} and R_{Drift} are correct.

2.4.5 Parasitic inductances characterization

The extraction of the extrinsic inductances L_g, L_d and L_s can be better accomplish at high frequencies at which their impedance dominate over the impedance of the rest parasitic components of the equivalent circuit. Thus an equivalent T-structure of the equivalent circuit can be assumed as explained in section 2.2.3. The fig. 2.23 shows the extracted extrinsic inductances using eqs. (2.33), (2.35) and (2.37) at max. V_GS bias of the DUT. This bias condition eases the extraction of the parasitic series inductances since the channel of the transistor and the intrinsic capacitances present their lowest impedance. L_d and L_s could be extracted with reasonable values of 0.3 nH and 1 nH respectively at a frequency of 300 MHz.

L_g however could not be extracted from this device. The extracted value is too large to be reasonable. This accuracy problem is attributed to two main factors. On the one hand, the SHORT dummy used for the de-embedding is not ideal and introduces added inductance. On the other hand, the gate and source pins of the package may be too close to each other leading to a relatively large C_PGS (see fig. 2.14. At certain frequencies this capacitance can thus bypass the RF signal coming from the VNA and never reach the bare die.

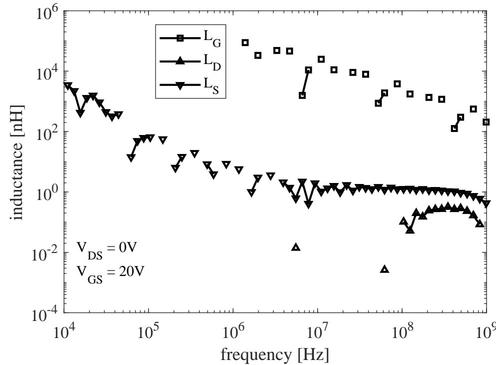


Figure 2.23: Extracted inductances plotted versus frequency

2.5 Conclusions of this chapter

A measurement technique and measurement setup to characterize the equivalent circuit of power MOSFETs up to high voltages was proposed. In contrast with conventional characterization techniques, based on impedance analyzers, the proposed technique is based on the analysis of S-Parameter measurements extracted with a vector network analyzer. Network theory applied to S-Parameter measurements permit the characterization of each individual component of the equivalent circuit of a power MOSFET from the measurements of a single fixture. This reduces drastically the complexity the measurement setup and provides versatility compared to the conventional approaches based on impedance analyzers. A thorough analysis of the accuracy of the measurement technique and its limitations was provided and discussed and a measurement setup to achieve S-Parameter measurements up to $\pm 1\,\mathrm{kV}$ was presented. The characterization of a Si power MOSFET was used as vehicle to illustrate the process of its equivalent circuit extraction. The results are contrasted with the datasheet and PSPICE model provided by the manufacturer showing very good agreement. Additionally, the channel and drift resistances of the device could be characterized separately with the proposed methodology. Measured values correlate well with TCAD simulation values of similar devices reported in the literature. This chapter presented the basis to perform the conventional characterization of a power MOSFET using S-Parameter theory. The versatility of this technique enables new characterization possibilities. An example of this is the characterization of the intrinsic capacitances of a SiC power MOSFET under high current conduction. This is developed further in the next chapter.

Chapter 3

Extended CV characterization of SiC power MOSFETs

The dynamic behavior of a power MOSFET is to a large extent determined by its intrinsic parasitic capacitances and their non-linear dependence of the applied bias voltages V_{GS} and V_{DS} [4]. These capacitances determine how the charge is distributed during a switching transient along the intrinsic structure of the device and thus its current-voltage characteristics [82]. A good understanding of the charge distribution inside a power MOSFET is therefore crucial to understand its dynamic behavior and achieve optimized circuit designs.

Characterization setups based on impedance analyzers are widely used to extract the capacitance-voltage (CV) characteristics of power MOSFETs often provided in datasheets [31]. One of the drawbacks of conventional CV characterization techniques is that they are restricted to zero-current bias conditions. Therefore, the effect of V_{GS} in the intrinsic capacitances is neglected and the dynamic behavior of the power switch oversimplified.

An accurate study of the dynamic behavior of power MOSFETs requires the extra evaluation of the switch in dynamic test fixtures such as double pulse testers. These, among others, permit the extraction of $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graphs at application switching conditions, which represent the total charge injected in the gate of the MOSFET required to fully turn-on the power device [33, 34, 37]. Hence, $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graphs provide a more accurate representation of the dynamic characteristics of a power switch than its CV graphs extracted at zero-current bias conditions. Though the voltage dependence of

each inter-electrode capacitance can not be fully derived from the $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graphs.

In [83, 84], the authors proposed the use of a dynamic test to study the non-linearity of the the input and reverse transfer capacitance of power MOSFETs under high current conduction. This idea was further developed in [36, 37, 38, 39, 40]. The results of these studies revealed an increase of the input and reverse transfer capacitances at bias voltages beyond the threshold voltage of the device i.e. when the device operates in strong inversion under high current conduction. One of the limitations of these techniques is the limited scope of bias conditions under which the non-linearity of the intrinsic capacitances can be characterized. Moreover, they do not ease a clear distinction between the inter-electrode capacitances C_{GS} and C_{GD}.

This chapter proposes a novel characterization approach that builds upon the S-parameter based methodology presented in chapter 2 and extends the bias conditions of conventional CV characterization techniques, limited to zero-current bias conditions, to the high current linear and saturation region of a power MOSFET. The proposed measurement technique has been published in [74]. Furthermore, this methodology permits the analysis of the gate charge distribution between the gate-source and gate-drain electrodes of the DUT during a switching transient. The intrinsic capacitances and charge distribution of a 1200 V/22 A commercially available SiC planar power MOSFET are characterized in the wide scope of high current bias conditions achieved by a Keysight B1505A curve tracer. Measurements are carried out at different junction temperatures ranging from 25 °C to 50 °C. Results show an acute non-linearity of the intrinsic capacitances of the SiC power MOSFET in the high current linear and saturation region, as well as a substantial impact of temperature on these, that correlate with the dynamic behavior of SiC power MOSFETs reported in recent studies [85, 86, 87, 22].

3.1 Pulsed-bias CV characterization of power MOSFETs under high current conduction

Conventional CV characterization setups, based on impedance analyzers (ZA), make complicated the characterization of power transis-

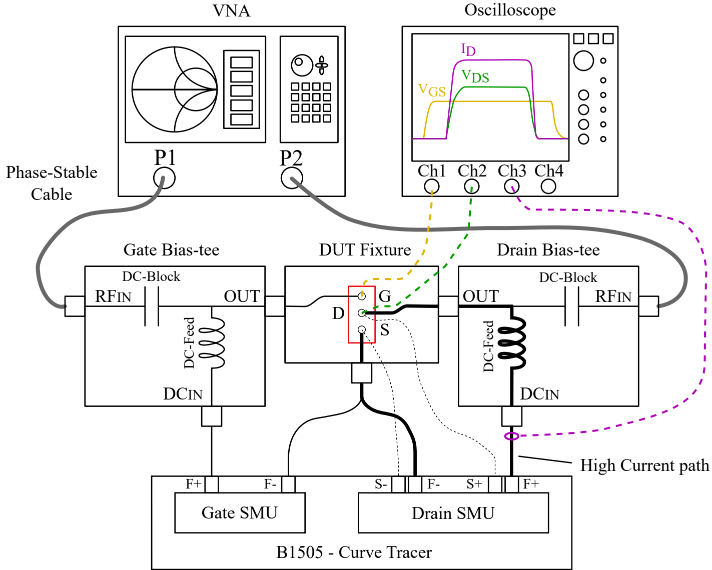


Figure 3.1: Block diagram of the proposed measurement setup

tors at bias points in which the device conducts high currents. Two are the major limiting factors: the relatively slow measurement speed of ZAs and the bypass capacitors required in the measurement fixture [31], which limit the possibility to bias the DUT inside its SOA. The measurement technique presented in chapter 2 benefits from the superior measurement speed of VNAs (section 2.1), which can realize a measurement point in just a few microseconds. This characteristic permits the extraction of an S-Parameter measurement within the short biasing pulses of a curve tracer, which can be used to characterize the intrinsic capacitances of the DUT in its high current linear and saturation operation regions.

3.1.1 Proposed measurement setup

The blocks diagram of the proposed measurement setup is depicted in fig. 3.1. A photo of this setup and a detailed view of the measurement fixture is shown in figs. 3.2a and 3.2b respectively. The measurement setup consists of:

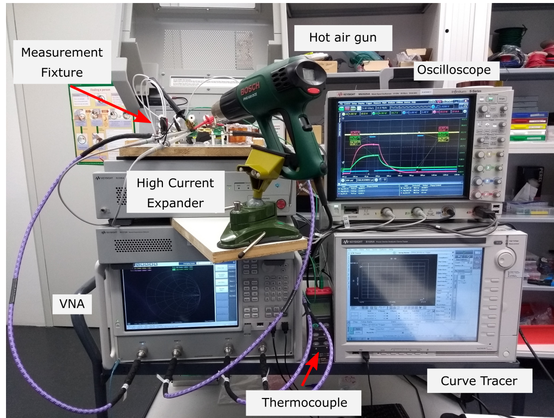
- A Keysight E5080A VNA [73] with a frequency range of 9 kHz - 9 GHz.

This VNA permits operation in constant waveform (CW) mode [70] which is necessary to achieve ultra-fast S-Parameter measurements. Two Keysight N9910X-708 3.5 mm (m) - 3.5 mm (m) rugged phase-stable cables guarantee that the measurement setup remains robust against systematic errors introduced by any possible bend in the cables.

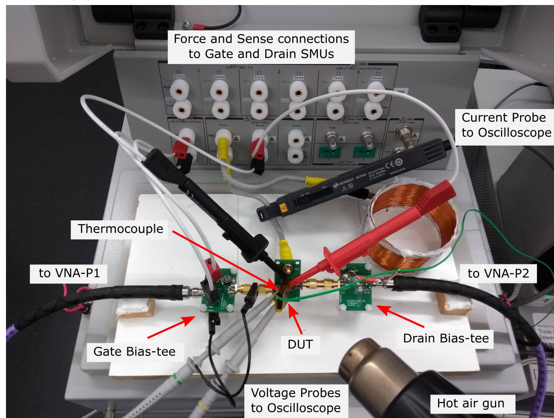
- A Keysight B1505A curve tracer [55] permits pulse-bias the DUT up to 500 A and 60 V with a max. power of 7.5 kW. Kelvin connections of the B1505A HC-SMU are connected to the pins of the DUT to compensate any voltage drop of the circuitry between the DUT and SMU arising from the series resistance of the measurement fixture and the high current pulses.
- An 2.5 GHz oscillosope Keysight MSOS254A [88] monitors the current and voltage waveforms with high time resolution for quick inspection of the bias pulse profiles.
- Two bias-tees are used to connect the gate and drain terminals of the DUT to the VNA and curve tracer. A detailed discussion on the bias-tees is provided in section section 3.1.1.
- The temperature of the DUT can be set from room temperature to 200 °C with a hot air pistol and is monitored at the case of the DUT with a Type-K thermocouple. The junction temperature of the DUT can be calculated from the thermal impedance provided by the manufacturer in the datasheet [89].

High current bias-tees

The design of high current bias-tees slightly differs from the high voltage bias-tees presented in section 2.3.1. Bias-tees for fast bias-pulsed applications require low transient setting time of the DC pulses while maintaining a high impedance path to the RF signals at the measurement frequency. In addition, the DC-path must withstand the high currents pulses required to drive the DUT in its linear and saturation region. A resistor like that of the bias-tees presented in section 2.3.1 would lead to extreme long DC set transients that impede any fast measurement. Furthermore, it would also constrain the high current biasing. An inductive DC-feed path realized with a coil solves these two problems. It permits fast DC pulses setting transients and high



(a) General view of the measurement setup



(b) Detailed view of the measurement fixture

Figure 3.2: Measurement setup and measurement fixture used in this work

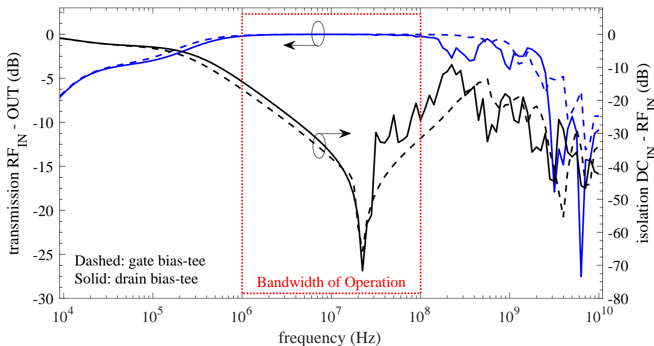


Figure 3.3: Frequency response of the gate (dashed) and drain (solid) bias-tees. The bias tees are designed to optimally operate in a frequency range of 1 MHz - 100 MHz

current supply thanks to the low DC impedance, plus it also provides a high impedance path to the RF signals.

In case of the drain bias-tee, the coil needs to present a constant impedance at any high current bias point when it is magnetized. Otherwise its impedance may change during the measurement, which complicates the de-embedding process. For this reason, an air core coil is the right choice. For the presented setup, a custom made air core coil was crafted. The geometry of the air-core coil was calculated using H. A. Wheeler formulations for circular coils [90].

In case of the gate bias-tee, no high current requirements like that of the drain bias-tee are required. Thus, an SMD ferromagnetic core coil does the work and provides a better frequency response at high frequencies.

During the fast DC bias setting transient, the coil of the bias-tee needs to quickly magnetize and demagnetize. In this process, surge voltage peaks may harness the VNA ports. To guarantee the safety of the VNA, a pair of diodes serve as transient voltage suppressor as explained in section 2.3.

The bias-tees are designed to optimally operate in the frequency range of 1 MHz to 100 MHz. The fig. 3.3 shows the frequency response and isolation achieved by the proposed drain and gate bias-tees.

IF Bandwidth	1-port meas.	2-port meas.
100 Hz	9.6 ms	20 ms
1 kHz	970 µs	2.6 ms
10 kHz	100 µs	930 µs
100 kHz	22 µs	760 µs
1 MHz	13 µs	750 µs

Table 3.1: Minimum time required by a Keysight E5080A to complete one point measurement with correction at different IF-BW

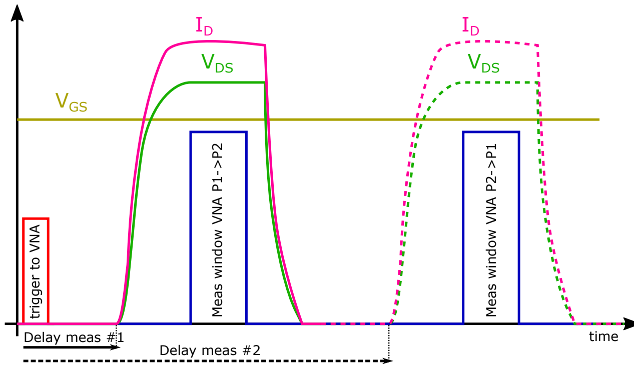


Figure 3.4: Time diagram of the proposed measurement setup. The delay of the V_{DS} pulse is adjusted to get it aligned with the measurement windows of the VNA

Measurement speed considerations

The measurement speed per point achieved by the measurement setup is critical. This needs to be as short as possible to accomplish at least one measurement point with correction within the short bias pulses of the curve tracer. Moreover, it must minimize the self-heating of the DUT when this is measured at very high currents.

The IF-BW of the VNA drastically affects the measurement speed per point of the VNA [71]. For the specific case of the VNA used in this work, a Keysight E5080A, the time required to accomplish a single frequency S-Parameter measurement in CW-mode at different IF-BW was measured in an oscilloscope. Results for 1- and 2-port corrected measurements are summarized in table 3.1.

Power transistors often require measurement frequencies in the

range of 1 MHz (see section 2.2.6). At these measurement frequencies, an IF-BW of min. 10 kHz is required to ensure a good accuracy of the measurement setup (see section 2.2.5). According to table 3.1 a corrected 2-port measurement would require 930 µs which is restrictive for the characterization of high power devices. First, the high energy dissipated in the transistor after this time will lead to excessive self-heating in the measurements. Second, the curve tracer is close to the 1 ms max. pulse width that it can supply. Therefore, a way to increase the measurement speed is required.

One way to tackle this problem consists of performing two alternated 1-port measurements instead of one single 2-port measurement. This idea is sketched in the time diagram of fig. 3.4. Instead of trying to fit an excessively long bias pulse that covers the measurement windows of both port 1 and port 2 of the VNA with its respective delay, the measurement can be segmented into two narrow measurements for port-1 and for port-2 with identical bias conditions. This can be realized by adjusting the delay of the V_{DS} pulse to align it with measurement widows of port-1 and port-2. Thus, a 2-port effective S-Parameter matrix can be obtained by merging accordingly the 2 touchstone files extracted from these independent measurement the same bias conditions.

Furthermore, the effective IF-BW of the measurements can also be reduced by averaging measurement samples [71] thus achieving a higher accuracy in the measurements (see section 2.2.5).

With these two considerations, at a measurement frequency of 1 MHz, IF-BW of 10 kHz and averaging N = 10 samples, power transistors can be characterized within bias pulses as short as 22 µs using a Keysight E5080A VNA or a similar instrument.

3.2 Capacitances of a SiC power MOSFET in high current linear and saturation operation

The intrinsic capacitances of a 1200 V / 22 A SiC planar power MOSFET [89] have been characterized up to its linear and saturation operation mode. For that, the measurement setup described in section 3.1.1 has been configured as follows:

- The bias pulses of the curve tracer are set to the minimum pulse

width of 200 µs. This minimizes self-heating in the DUT and permits the acquisition of iso-thermal measurements.

- The VNA is configured to obtain 2-port measurements in CW mode with an IF-BW of 10 kHz at a measurement frequency of 1 MHz and average N = 10 samples per measurement point (see section 3.1.1).

- All measurements are extracted at junction temperatures ranging from 25 °C to 150 °C. The junction temperature has been calculated from the thermal network provided by the manufacturer in the datasheet [89] and the temperature measured in the case of the transistor.

The intrinsic capacitances of the SiC power transistor have been extracted using the methodology provided in section 2.4. C_{DS} could not be completely characterized since this is bypassed by the low impedance $R_{\mathrm{DS_ON}}$ of the DUT at bias points beyond its threshold voltage (see section 2.2.6). The extracted IV and CV characteristics of the DUT at different temperatures are plotted in fig. 3.5.

The results of these measurements show how the non-linearity of the intrinsic capacitances of the DUT extends beyond the bias scope contemplated by conventional CV characterization solutions (i.e. zero-current bias conditions), up to the high current linear and saturation region. Furthermore, C_{GS} and C_{GD} present a strong dependence of the junction temperature of the DUT. Both effects can be appreciated more in detail in fig. 3.6.

From these results, the following observations can be summarized:

- The intrinsic capacitances C_{GS} and C_{GD} of the DUT present a non-linear behavior function of V_{DS} and V_{GS}. Both capacitances present a higher value in weak and strong inversion mode compared to their value in depletion mode. This effect is attributed to the corresponding growth of the inversion layer which acts as an electrode under the oxide layer.

- As V_{DS} increases, the depletion or space charge region (SCR) of the MOSFET expands down toward the drain terminal, resulting in a reduction of C_{GD}. C_{GS} on the contrary experiences an increase of its value as V_{DS} increases. Both effects are more prominent as the temperature increases.

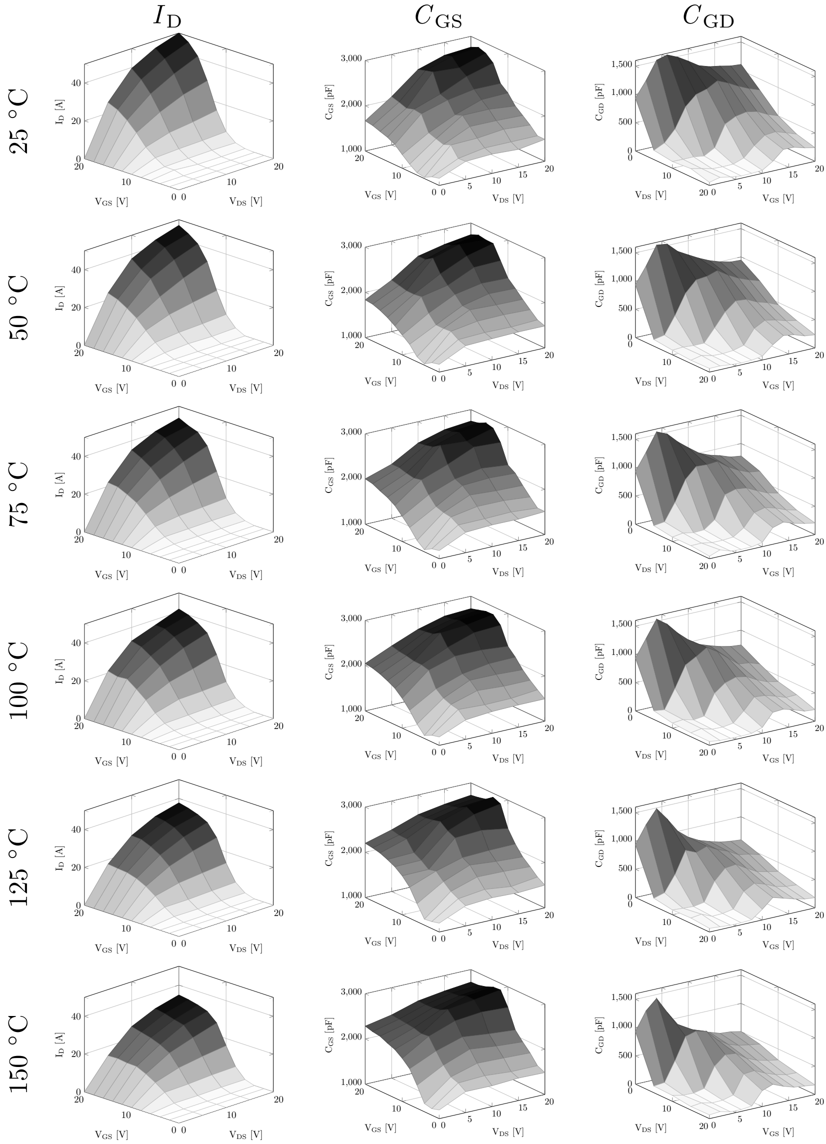


Figure 3.5: IV and CV characteristics of the SiC power MOSFET SCT2160KE at different temperatures. The capacitance values were extracted at a measurement frequency of 1 MHz

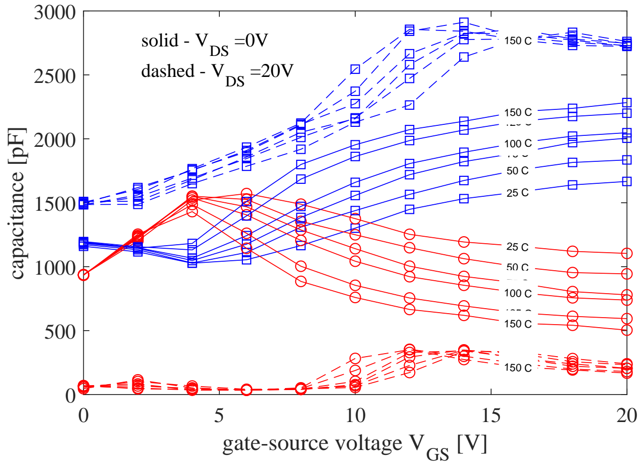


Figure 3.6: Gate-drain capacitance C_{GD} (red) and gate-source capacitance C_{GS} (blue) versus V_{GS} at junction temperatures ranging from 25 °C to 150 °C measured at $V_{DS} = 0$ V (solid) and $V_{DS} = 20$ V (dashed)

- Temperature has an impact on the measured CV characteristics of the SiC power MOSFET when operating in weak and strong inversion. This impact is more acute at low V_{DS} voltages and leads to an increase of C_{GS} and a decrease of C_{GD} proportional to the temperature.

- The impact of temperature in the threshold voltage of the SiC device displaces the voltage boundaries between operation modes (i.e. depletion, weak inversion and strong inversion) [22]. As a result, C_{GS} and C_{GD} experience a horizontal displacement towards lower V_{GS} values as the temperature increases. Furthermore, the temperature coefficients of the drift resistance and the channel mobility determine the effective intrinsic voltage drop across the SCR and channel and thus the effective capacitance values C_{GD} and C_{GS}.

Based on the summarized observations, the dynamic behavior of this particular SiC power switch in the application might be affected in the following manner:

- The turn-off voltage commutation speed of this particular SiC power MOSFET must be faster at high temperatures and high V_{DS} voltages.

- The turn-on voltage commutation speed might not be affected by the junction temperature as much as the turn-off voltage commutation speed is.

These measurement results correlate well with the dynamic behavior of comparable SiC power MOSFETs reported in recent publications [20, 85, 86, 87, 22, 30].

In [87] the gate current I_G of two SiC power MOSFETs are plotted at different temperature values. During turn-on event, I_G doesn't change much with temperature. This effect correlates well with the behavior of C_{GS} and C_{GD} shown in figs. 3.5 and 3.6. At the beginning of the turn-on transient, V_{DS} is large and temperature dependence in C_{GD} and C_{GS} is negligible (as shown in fig. 3.6). However, during the turn-off event, I_G increases with temperature. This effect correlates with the increase of C_{GS} shown in the measurements presented in fig. 3.6. At the beginning of a turn-off event, V_{DS} is low and capacitances show a high temperature dependence. At high temperatures

and low V_{DS} voltages the increased value of C_{GD} results in a longer voltage commutation process and an increase of I_{G}.

In [20] the Miller capacitance (C_{GD}) of a transistor model is fitted by applying an amplification factor to the CV measurements to account for a supposed increase of C_{GD} in the turn-off characteristics, which can not be accurately characterized with conventional CV measurements extracted at zero-current conditions. The amplification factor, adjusted by fitting the transient behavior of simulations with measurements, represents the increase of C_{GD} shown in fig. 3.6. The measurement technique presented in this chapter might help to improve the accuracy of the dynamic behavior of SiC power MOSFET transistor simulation models. A more extended discussion of this topic is provided in section 3.2.2.

It must be remarked, that the effects summarized in this section are characteristic of the specific DUT used in the presented measurements and thus can not be generalized for all SiC power MOSFETs. A device with a different process technology may behave in a different way. Though can be characterized in a similar manner using the proposed measurement technique.

3.2.1 Important considerations on the Miller Ratio

The Miller ratio, calculated as $C_{\mathrm{GS}}/C_{\mathrm{GD}}$, gives a hint on how prone a transistor is to parasitic turn-on (PTO) and oscillations in the gate terminal during a fast voltage commutation (V_{DS}) due to the voltage divider created by the intrinsic capacitances C_{GS} and C_{GD} [91, 92]. This value is often calculated from CV values provided in the datasheet, which are extracted at $V_{\mathrm{GS}} = 0$ V. In application, during the V_{DS} voltage commutation, the gate of the transistor is biased at the plateau voltage V_{Plateau} beyond the threshold voltage of the switch ($V_{\mathrm{Plateau}} > 0$). The non-linearity and temperature dependence of C_{GS} and C_{GD} presented in fig. 3.6 imply a dependence of the Miller ratio of V_{GS} and temperature. This can be seen in the values calculated and plotted in fig. 3.7.

In the hypothetical case high currents are switched (large V_{Plateau}) the Miller ratio is smaller than the value calculated at $V_{\mathrm{GS}} = 0$ V. Thus the transistor has in reality a worse PTO robustness compared to the value extracted from the datasheet at $V_{\mathrm{GS}} = 0$ V. In the specific case of the device here analyzed this difference is as large as

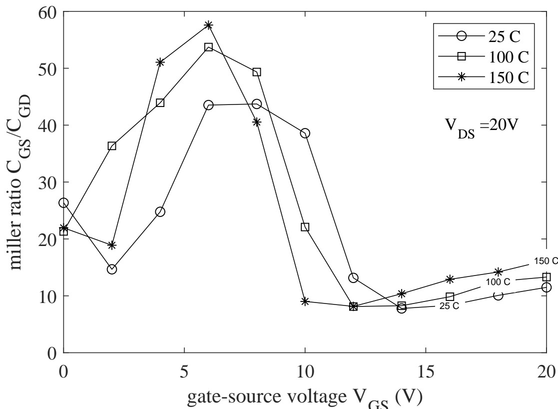


Figure 3.7: Effect of V_{GS} and temperature on the Miller ratio at $V_{\text{DS}} = 20$ V

V_{DG}	V_{GS}	V_{DS}	I_{D}	C_{GD}	Operation Mode
−3 V	3 V	0 V	0 A	1200 pF	depletion
−3 V	10 V	7 V	9 A	650 pF	strong inversion
−3 V	20 V	17 V	45 A	180 pF	strong inversion

Table 3.2: C_{GD} values and operation modes at different bias points with same V_{DG} = -3 V at T_{J} = 25 °C

50 %, what may lead to unexpected PTO in the application. At low switching currents V_{Plateau} lies in the hump situated between 5 and 10 V. In such case, the Miller ratio gets better, resulting in a higher robustness against PTO. In both cases, higher temperature lead to a higher Miller ratio, what suggests that, despite the fact that the transistor voltage commutation is faster at high temperatures (as explained in section 3.2), the robustness against PTO is also higher.

3.2.2 Important considerations on C_{GD} for transistor modeling

The gate-drain capacitance C_{GD} determines the behavior of a power MOSFET during the voltage commutation interval. This capacitance is formed by the series construction of part of the gate oxide capa-

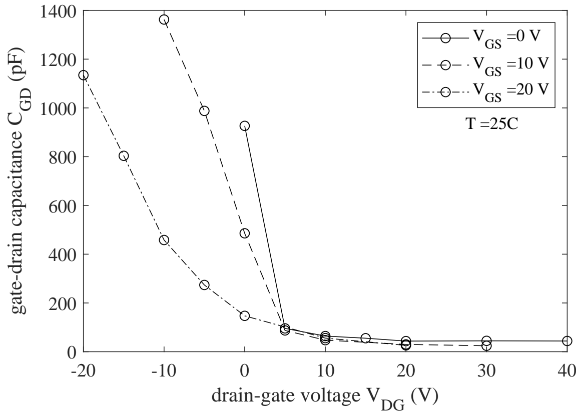


Figure 3.8: C_{GD} plotted versus V_{DG} at different V_{GS} bias points and $T_{\mathrm{J}} = 25\ ^{\circ}\mathrm{C}$. An accurate modelling approach of C_{GD} should consider this as function of V_{DS} and V_{GS} instead of a function of V_{DG}

citance and the MOS capacitance created in the drift region of the transistor under the oxide. In general, the latter is much smaller and dominates the total capacitance C_{GD} in the series construction. Large drain-gate voltages contribute to an expansion of the depletion region of this MOS capacitance and to a decrease of its value.

C_{GD} is commonly modeled as a function of its terminal voltage V_{DG}. Its non-linearity is modeled only for positive V_{DG} values whereas at negative V_{DG} values the capacitance is extrapolated constant [30]. This arises from the limitations of conventional characterization methods which only permit zero-current bias conditions. Recent publications discussed on the behavior of C_{GD} in the negative V_{DG} operation region. In [37] C_{GD} was extracted from a DPT at application switching conditions, showing a continue increase of its value at negative V_{DG} values. In [93] C_{GD} was characterized at negative V_{DG} values in depletion mode at zero-current bias conditions showing a slight increase of its value. A transistor model with C_{GD} fitted from these measurements showed a substantial gain in the accuracy and convergence robustness of transient simulations.

An accurate and continuous C_{GD} capacitance modeling is necessary to achieve accurate simulations of power circuits. However,

modeling C_{GD} as dependent on a single terminal voltage V_{DG} may be an oversimplification that constrains accuracy of modern transistor models, since a V_{DG} voltage, either positive or negative, does not necessarily define an operation mode. In the measurements shown in section 3.2 C_{GD} and C_{GS} are highly dependent on the operation mode (accumulation, depletion or inversion) defined by a combination of V_{GS} and V_{DS}. Two different combinations of these voltages may lead to the same V_{DG} value, despite the fact that the capacitances are different and the MOSFET operates in different modes. This can be seen in table 3.2 where C_{GD} takes different values for the same V_{DG} extracted at different combinations of V_{DS} and V_{GS}. The measurements plotted in fig. 3.8 represent graphically the same idea. Based on these observations, a more appropriate and accurate C_{GD} modeling approach should be implemented as a function of both V_{GS} and V_{DS} separate values and not as a single V_{GD} value.

3.3 Gate charge partition in SiC power MOSFETs

The study of the dynamic behavior of power MOSFETs requires their evaluation in dynamic test fixtures such as double pulse testers [94, 95, 96]. These, among others, permit the extraction of $Q_G - V_{GS}$ graphs [32, 41, 35] which are often used as benchmark to evaluate the dynamic behavior of power switches. They are extracted under application switching conditions and provide a more accurate view of the dynamic characteristics of the power switch than the typical CV graphs extracted by conventional measurement techniques at zero-current biasing conditions.

The literature [35, 4] assumes a flat gate-source voltage during the plateau interval to calculate Q_{GD} from $Q_G - V_{GS}$ graphs. The JESD24-2 characterization standard [33] relies on this assumption too. This assumption might not always hold valid for some devices which present a peculiar slow-saturating output characteristic. In such cases, V_{GS} might still change during the voltage commutation phase leading to a slope of $Q_G - V_{GS}$ graphs where a plateau is often assumed. Such phenomena do not permit a clear distinction of Q_{GD} and Q_{GS} from the total gate charge Q_G as assumed by theory. To estimate a better value of Q_{GD}, some manufacturers calculate it as the charge injected in the gate during the 97-10% of the volt-

age commutation interval [41]. However, none of the aforementioned methods permit an accurate separation of Q_{GD} and Q_{GS} from the total measured gate charge Q_{G} during a switching transient.

3.3.1 A versatile method to extract $Q_{\mathbf{G}} - V_{\mathbf{GS}}$ from static IV and CV characteristics

Available methods to extract $Q_{\mathbf{G}} - V_{\mathbf{GS}}$

The JEDEC defines the standard JESD24-2 [33, 34] to extract the $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ characteristics of power MOSFETs. This standard calculates the slope of the first and the last sections of the $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graph from the switching waveforms of two separate measurements, one at high-current/low-voltage and the other at high-voltage/low-current switching conditions. Q_{GD} is not directly measured but extrapolated assuming a flat plateau region. This assumption may not be true for some devices (as discussed in chapter 4) and can lead to innacurate extraction of Q_{GD} with these devices.

Alternatively, the gate charge graphs of a power MOSFET can be directly extracted from a dynamic test such as a DPT by integrating the current injected in the gate with respect to time and plotting it against the instantaneous gate-source voltage V_{GS} measured at the DUT terminals.

Both methods are based on dynamic measurements and can thus be affected by the parasitics of the test circuitry. Slow switching of the device may help reducing the effect of parasitics in the measurements at the cost of added self-heating.

Proposed method to extract $Q_{\mathbf{G}} - V_{\mathbf{GS}}$

The measurement technique proposed in section 3.1 permits the characterization of the intrinsic capacitances of a power MOSFET at high current conduction bias conditions. With this technique, the C_{GS}, C_{GD} and I_{D} surfaces of fig. 3.5 were extracted. Having separate C_{GS} and C_{GD} capacitors and their V_{GS} and V_{DS} voltage dependence permits the calculation of the charge stored in these capacitances corresponding to each bias point. These, in turn, can be used to calculate the gate charge characteristics $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ of a power MOSFET without the need of a dynamic tester, hence free of parasitic effects or self-heating.

The cumulative gate-source and gate-drain and total gate charges at an instant time t can be calculated as:

$$Q_{\mathrm{GS}}(t) = \int_{t_0}^{t} C_{\mathrm{GS}}(V_{\mathrm{GS}}(t), V_{\mathrm{DS}}(t)) \cdot V_{\mathrm{GS}}(t) \cdot dt \tag{3.1}$$

$$Q_{\mathrm{GD}}(t) = \int_{t_0}^{t} C_{\mathrm{GD}}(V_{\mathrm{GS}}(t), V_{\mathrm{DS}}(t)) \cdot V_{\mathrm{GD}}(t) \cdot dt \tag{3.2}$$

$$Q_{\mathrm{G}}(t) = Q_{\mathrm{GS}}(t) + Q_{\mathrm{GD}}(t) \tag{3.3}$$

Both eqs. (3.1) and (3.2) can be applied in combination with the IV and CV waveforms of fig. 3.5 to calculate the charges Q_{GS} and Q_{GD} of an inductive load switching transient, at generic switching conditions I_{SW} and V_{SW}, using the following numerical integration algorithm:

1. Surf the IV characteristics along a constant $V_{\mathrm{DS}} = V_{\mathrm{SW}}$ until I_{SW} is reached.

2. Then surf the IV characteristics of the DUT along a constant value I_{SW} until V_{GSmax} is reached.

The proposed algorithm has been applied to the IV and CV measurements presented in section 3.2. These belong to a SiC power MOSFET [89] and were extracted up to $V_{\mathrm{DS}} = 40$ V and $V_{\mathrm{GS}} = 20$ V at different temperatures (See fig. 3.5). An approximation of the IV and CV characteristics at higher V_{DS} voltages have been extrapolated constant. The error introduced by this extrapolation is discussed at the end of the section.

In fig. 3.9 the switching trajectory of a SiC power MOSFET is plotted in the V_{DS} - V_{GS} plane together with the integration path followed by the proposed algorithm.

The $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graph extracted with the proposed technique is plotted in fig. 3.10 and compared with that provided in the datasheet and that extracted from a DPT measurement at the switching conditions of 400 V and 7 A.

Results are graphically compared in fig. 3.10 and numerically contrasted in table 3.3. The $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graph extracted with the proposed method accurately reproduce the measurement extracted from the DPT measurements, which are considered as a reference. The resemblance between both graphs speaks for the accuracy of the measurement technique presented in section 3.1 and validates the algorithm

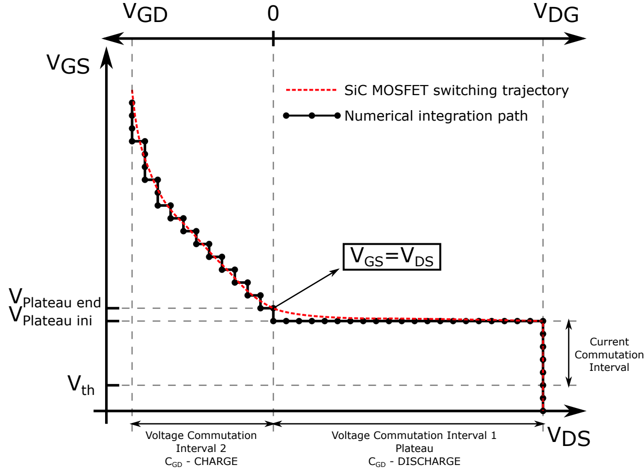


Figure 3.9: Bias trajectory of a SiC power MOSFET plotted in a V_{GS} vs V_{DS} plane and numerical integration path of the proposed algorithm to calculate its $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graphs

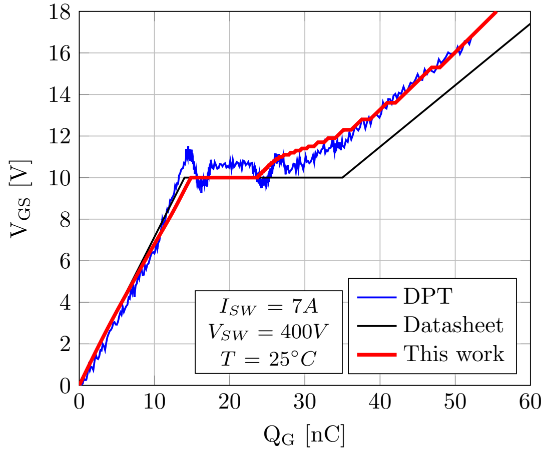


Figure 3.10: Comparison of $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ graphs extracted with the proposed method (red), datasheet (black) and a DPT (blue). The proposed method reproduces the measurements extracted from a DPT

	V_{Plateau}	$Q_{V_{\text{Plateau}}}$	$Q_{\mathbf{GD}}$	Q_{Gtot}
DPT (reference)	10.4 V	11.8 nC	16 nC	50 nC
This work	10 V	12 nC	15 nC	50 nC
Datasheet(JEDS24-2)	10.1 V	12 nC	36 nC	55 nC

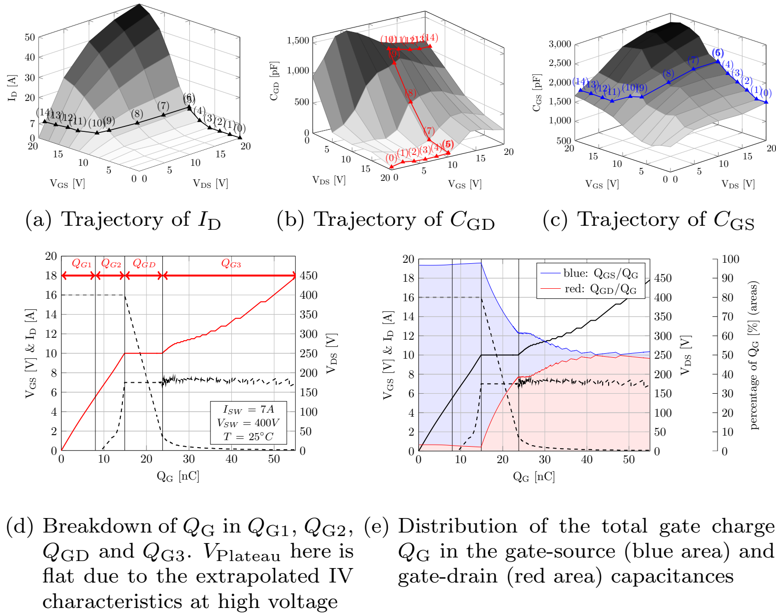
Table 3.3: Comparison of the plateau voltage (V_{Plateau}), the gate charge to reach the plateau voltage ($Q_{V_{Plateau}}$), the gate-drain charge Q_{GD} and the total gate charge Q_{Gtot} extracted with the proposed technique and that measured in a DPT

to extract gate-charge proposed in this section. The error introduced by the extrapolation of constant values at $V_{\text{DS}} > 40V$ seems to be negligible. The values provided by the manufacturer in the datasheet are probably extracted according to the JESD24-2 standard. The error introduced by the JESD24-2 standard is attributed to the fact that the Q_{GD} value is not directly measured, but extrapolated from two measurements assuming a perfectly flat plateau region. The difference in Q_{Gtot} is attributed to the tolerance of the device. One advantage of the method here presented versus measurements extracted from a DPT is that the $Q_{\text{G}} - V_{\text{GS}}$ graphs can be quickly computed for any switching conditions without the need of dynamic measurements susceptible of self-heating and the effect of parasitics innate in the measurement circuitry. This permits a fair benchmark between different devices independent on the surrounding circuitry.

3.3.2 A charge-based interpretation of the switching dynamics of a SiC power MOSFET

Applying eqs. (3.1) to (3.3) in combination with the algorithm proposed in section 3.3.1 permits an in-depth analysis of the charge distribution between the gate-source and gate-drain terminals of a power MOSFET during a switching transient. The turn-on trajectories of I_{D}, C_{GS} and C_{GD} of the DUT computed by the proposed algorithm during an inductive switching at 7 A and 400 V are plotted in figs. 3.11a, 3.11c and 3.12a respectively. The values of C_{GS} and C_{GD} are extrapolated constant at $V_{\text{DS}} > 40V$ as discussed in section 3.3.1 with a negligible error introduction.

The computed $Q_{\text{G}} - V_{\text{GS}}$ graph for these switching conditions is plotted together with V_{DS} and I_{D} in fig. 3.11d. The total gate charge distribution Q_{G} is plotted in fig. 3.11e together with the individual



(a) Trajectory of I_D

(b) Trajectory of C_{GD}

(c) Trajectory of C_{GS}

(d) Breakdown of Q_G in Q_{G1}, Q_{G2}, Q_{GD} and Q_{G3}. $V_{Plateau}$ here is flat due to the extrapolated IV characteristics at high voltage

(e) Distribution of the total gate charge Q_G in the gate-source (blue area) and gate-drain (red area) capacitances

Figure 3.11: $Q_G - V_{GS}$ extraction from pulsed-IV and -CV measurements. The values of I_D, C_{GS} and C_{GD} are extrapolated constant at high voltage values. This technique enables the computation and analysis of the dynamic behavior and charge distribution of a power MOSFET from static measurements at any switching conditions.

contribution to it of the gate-source and gate-drain charges Q_{GS} and Q_{GD} respectively.

These results permit to conclude the following analysis of the switching transient of a SiC power MOSFET and how the charge injected in the gate during the process dynamically distributes along the MOSFET structure.

1. First V_{GS} increases, V_{DS} remains constant and $I_D = 0$. Q_{G1} is the amount of charge required to charge the input capacitance C_{ISS} to reach the threshold voltage of the device V_{th}. During this process, V_{DS} does not change and only V_{GS} increases. This means, the current injected in the gate of the transistor charges C_{GS} and discharges C_{GD}. Since C_{GD} is very small compared to C_{GS}, most of the charge injected in the gate is stored in C_{GS} (see fig. 3.11e). In case of the device here analyzed and the analyzed switching conditions, 98% of the injected gate charge charge flows into charging C_{GS} and only 2% in discharging C_{GD}.

2. When the gate reaches the threshold voltage V_{th}, the transistor starts operating in inversion mode and the drain current I_{D} increases. Here starts the current commutation process. During this time interval V_{DS} remains constant due to a clamped switching node. Q_{G2} is the amount of charge required to charge the input capacitance to increase V_{GS} from V_{th} to value that permits the MOSFET to conduct the load current I_{SW}, this value is known as the plateau voltage V_{Plateau}. This time instant concludes the current commutation interval. Until this point, the current injected in the gate of the transistor charged C_{GS} and discharged C_{GD}. In this time interval, when the transistor operates in inversion mode, C_{GS} drastically increases and C_{GS} slightly decreases (see figs. 3.11c and 3.12a). As a result of this, most of the charge injected in the gate of the transistor is accumulated in C_{GS} between the gate and source terminals (see fig. 3.11e). The distribution of the gate charge injected in the gate between C_{GS} and C_{GD} doesn't change much with respect to the previous interval and still remains at approximately 98% in C_{GS} and 2% in C_{GD}.

3. The end of the current commutation interval gives rise to the beginning of the voltage commutation process. From here on, the so-called plateau or Miller effect occurs. During this process, assuming an ideal load, I_{D} remains constant and V_{DS} can

start decreasing. The pace at which V_{DS} decreases is mainly determined by the discharge process of C_{GD}, and Q_{GD} is the amount of charge required to complete the voltage commutation process.

It is important to mention that C_{GS} is not constant, indeed it gets smaller as V_{DS} decreases (fig. 3.11c). As a result, C_{GS} might inject current to C_{GD}, in addition to that injected from the gate driver, which aids the discharge of C_{GD} and so the completion of the voltage commutation process. This signifies that the non-linearity of C_{GS} affects the dynamic behavior of the power MOSFET during the voltage commutation process. From fig. 3.11e it can be seen that during the plateau interval C_{GD} a at the end of the plateau interval 40% of the total gate-charge has been injected into the discharge process of C_{GD}.

4. During the last part of the switching process the input capacitance charges further until V_{GS} reaches its maximum value. The gate-drain capacitance C_{GD} reverses its polarity and starts charging in conjunction with C_{GS}. Q_{G3} is the charge required to charge the input capacitance from $V_{\mathrm{DG}} = 0$ V until $V_{\mathrm{GS}} = V_{\mathrm{GS_max}}$. At the end of the turn-on process, the charge balance between the gate-source and gate-drain capacitances is around 50-50 % in case of this DUT and under the assumed switching conditions(fig. 3.11e).

The gate charge balance between C_{GS} and C_{GD} during a turn-on process ($\%Q_{GS} - \%Q_{GD}$) changes from 2-98 % a the beginning of the turn-on event to a 50-50 % at the end of it for the switching conditions plotted in fig. 3.11e. The dynamic distribution of the gate charge balancing between gate-source and gate-drain terminals has a direct application in the optimization of the MOSFET structure or in the extraction of charge-based compact models.

3.3.3 Effect of switching current in C_{GD} and overall switching speed of a SiC power MOSFET

As discussed in section 3.3.2, the Miller effect arising from discharging/charging C_{GD} in a turn-on/-off commutation event defines most of the switching losses of a high voltage power MOSFET. To complete the voltage commutation process, in the specific case of a turn-on event, C_{GD} needs to be discharged a total charge Q_{GD} to reduce the

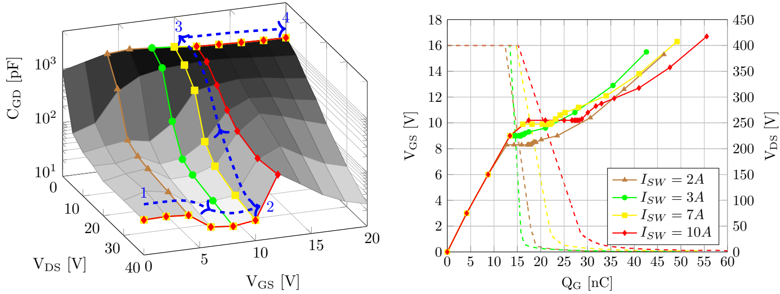
voltage $V_{DG} = V_{DS} - V_{Plateau} \rightarrow 0V$ (see fig. 3.11d). C_{GD} suffers from an acute non-linearity function of V_{DS} and V_{GS} (see fig. 3.6). Hence, the plateau voltage V_{Plateau}, determined by the switching current I_{SW}, has a strong influence on the bias trajectory in C_{GD} during a commutation transient. Therefore, the complex non-linearity of C_{GD} results into the existence of optimal and critical switching conditions in the power MOSFET.

To illustrate this effect the $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ curves of the DUT were computed (section 3.3.1) for different switching currents I_{SW} leading to different plateau voltages V_{Plateau}. Results are plotted in fig. 3.12. The gate charge breakdown into Q_{G1}, Q_{G2}, Q_{GD}, Q_{G3} and Q_{Gtot} (see fig. 3.11d) calculated at switching currents I_{SW} of 2, 3, 7 and 10 A is compared in table 3.4.

In the specific case of this device, the fastest switching conditions are reached at V_{Plateau} of 9 V (green trace with circle markers in fig. 3.12). This corresponds to a switching current of 3 A. The total charge required to complete a voltage commutation event is $Q_{\mathrm{GD}} = 3.5$ nC. In contrast, switching a current of $I_{\mathrm{SW}} = 7$ A (yellow trace with square markers in fig. 3.12), sets the plateau voltage of the device to $V_{\mathrm{Plateau}} = 10$ V. What results in a $Q_{\mathrm{GD}} = 6.5$ nC. This small variation of 0.8 V in V_{Plateau} requires almost double the charge required to switch 3 A of current.

The worst case switching condition in this device is identified at $V_{\mathrm{Plateau}} = 10.3$ V, which corresponds to a switching current of 10 A. The bias trajectory of C_{GD} during the voltage commutation travels the C_{GD} hump (red trace with diamond markers in fig. 3.12). As a result of the increased C_{GD}, a charge of $Q_{\mathrm{GD}} = 11$ nC is required to complete the voltage commutation, what makes the device extremely slow in comparison to other switching conditions.

This study demonstrates the sensitivity of the switching characteristics of a SiC power MOSFET to slight V_{GS} variations. This may have a huge impact in reliability and life degradation of SiC power switches if neglected. The topic gains even more complexity if temperature is considered. For sake of simplicity, a constant temperature of $T = 25$ °C has been considered in this analysis. However, the switching speed of the power switch, conditioned by C_{GD}, may lead to self-heating or changes in the junction temperature of the device, which might dynamically displace both its CV and IV characteristics. Such a complex analysis has not yet been carried out, but could be accordingly performed computing all the measurements presented in



(a) Approximated bias trajectory of C_{GD} sketched at different switching currents I_{SW}. V_{Plateau} is assumed constant in this representation.

(b) Extracted $Q_{\text{G}} - V_{\text{GS}}$ graphs computed for different switching currents I_{SW} i.e. different plateau voltages V_{Plateau}

Figure 3.12: Impact of C_{GD} non-linearity in the dynamic behavior of a SiC power MOSFET computed at $V_{\text{SW}} = 400$ V and $T = 25$ °C. The plateau voltage V_{Plateau} at a switching current $I_{\text{SW}} = 10$ A meets a C_{GD} hump that leads to a larger amount of Q_{GD} to accomplish the voltage commutation process

fig. 3.5 for certain switching conditions with the aim of optimizing the MOSFET structure or in seek for realistic worst-case analysis.

3.4 Conclusions of this chapter

One of the limitations of conventional CV-characterization techniques is that they can not handle high current operating conditions. This limitation restricts the range of the bias conditions in which the CV characteristics of a power MOSFET can be characterized. This chapter proposed a CV-measurement technique that permits the characterization of the intrinsic capacitances of a power MOSFET up to high-current bias conditions, i.e. in the linear and saturation region of the power MOSFET. Such characteristic extends the bias range in which the voltage non-linearity of the intrisic capacitances of a power MOSFET can be measured.

Using the proposed CV-characterization technique, the inter-electrode capacitances of a commercially available SiC power MOSFET were measured at operation modes ranging from depletion to strong inversion in a combination of bias points ranging from $V_{\text{GS}} = 0$ - 20 V and

I_{SW}	$V_{Plateau}$	$Q_{G1}+Q_{G2}$	Q_{GD}	Q_{G3}	Q_{Gtot}*
2 A	8.2 V	12 nC	6 nC	30 nC	48 nC
3 A	9 V	13 nC	3.5 nC	27.5 nC	44 nC
7 A	9.8 V	16 nC	6.5 nC	25.5 nC	48 nC
10 A	10.3 V	17 nC	11 nC	25 nC	53 nC

Table 3.4: Impact of the switching current I_{SW} in the gate-charge characteristics of the SiC DUT [89] at V_{DS} = 400 V and T = 25 °C switching conditions. *Q_{Gtot} is the total gate charge to reach V_{GS} = 16 V

V_{DS} = 0 - 40 V up to I_D = 50 A of current. The experiments were carried out at junction temperatures T_J ranging from 25 °C to 150 °C.

Additional to the well known drain-source voltage V_{DS} dependence of the intrinsic capacitances, the gate-source voltage V_{GS} turned to have a strong impact in the values of C_{GS} and C_{GD}, which experienced a substantial increase in their value in strong inversion compared to their value in depletion mode. Furthermore, the interelectrode capacitances of the SiC power MOSFET showed a dependence on the junction temperature. This was more accused in the weak and strong inversion operation modes. More precisely, C_{GD} and C_{GS} presented negative and positive temperature coefficients respectively.

Built upon the proposed CV characterization technique, a numerical integration algorithm was proposed that permitted the computation of gate-charge $Q_G - V_{GS}$ characteristics of power MOSFETs at any switching condition without the need of a dynamic test. This method provided high accuracy results and permitted an in-depth analysis of the gate-charge distribution between gate-source and gate-drain terminals during a turn-on switching event.

The measurement results presented in this work point to the following conclusions about the dynamic behavior of SiC power MOSFETs in the application:

First, the measured temperature dependence of the intrinsic capacitances C_{GD} and C_{GS} suggest that high temperatures result in slower voltage commutation speeds of a SiC power MOSFET during a turn-off event. The voltage commutation speed during a turn-on event is barely affected by temperature though.

Second, the non-linearity presented by C_{GD} as a function of V_{DS}

and V_{GS} of the analyzed SiC power MOSFET implies that the voltage commutation speed of a SiC power MOSFET may be strongly affected by the plateau voltage V_{Plateau} or, in other words, the switched load current. Results reveled optimal and critical switching conditions which might help further optimize the performance of SiC power MOSFETs in power converter designs.

The measured carried out in this work show an impact of temperature and the V_{GS} terminal voltage in the intrinsic capacitances of SiC power MOSFETs. These are not contemplated by literature, datahseets and transistor models, which may lead to an oversimplification in the prediction and simulation of the dynamic characteristics of SiC power MOSFETs.

Chapter 4

Extended IV characterization of SiC power MOSFETs

The locus described by the switching trajectory of a power MOSFET when switching a clamped inductive load crosses the high power region of its IV characteristics, where the switch withstands instantaneous high current and high voltage values. The dynamic behavior of a power switch is therefore partly determined by the shape of its IV characteristics in the high voltage region, more specifically its transconductance G_{m} at the switching voltage.

Curve traces (CT) are the standard measurement instruments used to characterize the IV characteristics of power devices. Their measurement principle consists of biasing the DUT terminals with high power pulses within which the current and voltage of the DUT are measured. The temperature increase of the DUT during the measurement (self-heating) can alter the extracted IV characteristics though [97]. Short bias pulses are best to diminish this problem. However, the limited slew rate of the CT makes self-heating unavoidable beyond certain biasing power levels. Such cases require complex calibration methods to extract the isothermal electrical characteristics of the DUT [98]. Additionally, commercially available CTs are limited to power levels below those reached by modern SiC power MOSFETs in the application [55, 99, 100]. Alternative measurement instruments such as transmission line pulse (TLP) systems [26, 27] can reach higher biasing power levels than CTs. However, these are tailored for reliability studies, rather than IV characterization, and introduce excessive energy losses and self-heating in the measurements.

The power limitation of CTs may not be a big problem for the IV characterization of power devices which IV characteristics saturate at relatively low voltage levels since the IV characteristics can be linearly extrapolated to the high voltage saturation region. However, some power devices reach the saturation at relatively large drain voltages or even do not extend linearly in their saturation region [32]. These effects, common in SiC power devices, arise from the short-channel lengths required to compensate the poor mobility of SiC inversion layers, and necessary to achieve low on-resistances [101]. In addition, the lower intrinsic concentration of SiC compared to Si [4], and the existence of positive charge-traps in the SiO_2/SiC interface [23], make the electrical parameters of SiC power MOSFETs very sensitive to temperature variations [21]. As a result, SiC power MOSFETs require accurate measurement methodologies with minimal self-heating in order to achieve reliable isothermal measurements.

To tackle these problems, new characterization approaches need to be investigated that permit to extend the IV measurement range of these devices to application power levels while maintaining negligible self-heating.

In [25] a custom high power curve tracer system permitted the IV characterization of SiC power MOSFETs up to 200 V and 12 A with pulse widths as short as 10 µs. A transistor model fitted to the extended IV characteristics of the SiC power MOSFET, led to a substantial improvement in the accuracy with which the current commutation of the device was simulated [102]. However, the measurement range of this CT still lags behind the power levels of modern SiC power MOSFETs which operate at voltage levels above 600 V.

In [20] the authors suggested for the first time the idea of extracting the high-voltage transconductance of a SiC power MOSFET from dynamic measurements at application conditions. This idea was further developed in [29, 30] and patented in [103] where the authors use the dynamic waveforms extracted during a switching transient in a DPT, more specifically the voltage commutation interval, to extract the static IV characteristics of a SiC power MOSFET at application power levels. These techniques suffer from accuracy limitations due to excessive self-heating and parasitic artifacts arising from the surrounding circuitry though. A detailed explanation follows in the chapter.

Based on the idea of using a dynamic tester to extract static IV characteristics of a power switch, this chapter presents an alterna-

tive measurement methodology which permits the characterization of power MOSFETs with negligible self-heating in the complete bias range of operation. The measurement technique has been published in [104]. Isothermal static IV characteristics of a modern commercially available SiC power MOSFET are measured up to instantaneous 50 A and 800 V at operating temperatures ranging from 25 °C to 175 °C . The results of these measurements foresee the impact of temperature and short-channel effects in the dynamic behavior of SiC power MOSFETs.

4.1 Extended IV characterization from dynamic tests

A DPT permit the characterization of the dynamic behavior of power devices when switching a clamped inductive load [94, 95, 96]. The schematic of a DPT circuit is depicted in fig. 4.5. When switching a clamped inductive load, the DUT operates for short time in its high power operation region, beyond the limits CTs can measure (see fig. 4.1). The transient current and voltage waveforms of the DUT measured from a DPT can be used to infer information about the static IV characteristics of the DUT at high power levels (i.e. instantaneous high voltage and high current). A measurement setup and the methodology to achieve that are presented in the following sections. As nomenclature in this chapter, the time-varying entities are represented with small letters and time-constant entities with capital letters. For example the time-varying gate-source voltage $v_{\mathrm{GS}}(t)$ is simply written as v_{GS} and a specific steady DC gate-source voltage as V_{GS}.

4.1.1 Proposed measurement setup

Two photos of the proposed measurement setup are shown in fig. 4.2. This consists of the following components:

- A commercially available evaluation board [105] is used in a double pulse test configuration. The evaluation board features a half-bridge configuration with a DC-Link capacitor and gate driver stage. The place of the high side switch is populated with a SiC free wheeling diode (FWD). The place of the low side switch is populated with the DUT.

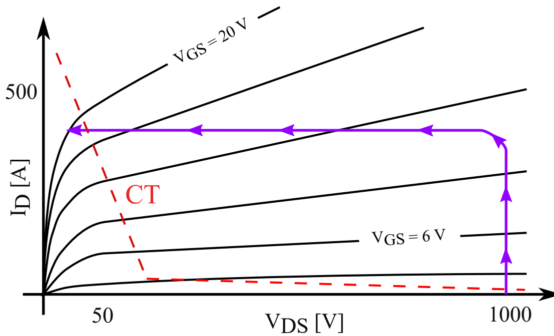


Figure 4.1: IV characteristics of a generic SiC power MOSFET and the ideal switching trajectory of a turn-on event (magenta arrows). The power limitation of curve tracers (dashed red line) does not permit a complete characterization of the IV characteristics of a power switch in its full range of operation. Numeric values depicted in the plot axes are just illustrative

- A low inductive 5 mΩ, 2 GHz bandwidth coaxial shunt from T&M [106] is mounted on the evaluation board to measure the current flowing in the power loop of the DPT with high bandwidth. This is connected in series with the source electrode of the DUT as in [96].
- A 2 GHz, 10bit resolution oscillosope Keysight MSOS254A [88] monitors the current and voltage waveforms with high bandwidth and resolution. The 5 mΩ coaxial shunt is connected with a 50 Ω coaxial cable through a 50 Ω Feed-Through terminal for protection and impedance matching at the port of the oscilloscope.
- A Keysight 33500B waveform generator [107] generates a PWM signal which is fed into the input of the gate driver circuitry of the low side transistor (DUT). A discussion on the PWM signal time profile is provided in section 4.1.2.
- A Keithley 2260B-800-4 power supply [108] provides a high voltage input source up to 800 V.
- The temperature at the case of the DUT can be adjusted with a heat gun and is monitored with a type-K thermocouple attached to the thermal pad of the package of the DUT.

- A custom made air core coil is connected as load to the test fixture. More information on how its value is selected is provided in section 4.1.2.
- Deskew of the V and I waveforms in the oscilloscope was applied as explained in [109, 96].

4.1.2 Pulse width and self-heating considerations

In a DPT the DUT charge the coil to a desired current during the first pulse. This, depending on the voltage and current levels and the inductance of the coil, may lead to excessive energy dissipation in the DUT and an increase of its junction temperature. To obtain isothermal measurements from a DPT, it is important to consider the time profile of the PWM signal that controls the charging cycle of the coil.

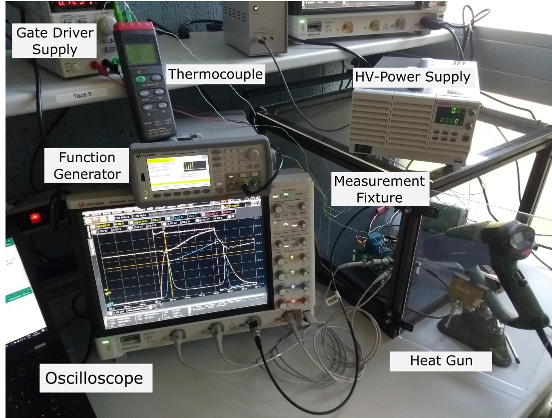
To minimize self-heating during the charging phase, the time diagram of fig. 4.3 is proposed. The charging pulse is divided in N equi-spaced pulses of duration Δt as

$$\Delta t = \frac{L_{\mathrm{COIL}} \cdot I_{\mathrm{MEAS}}}{(N-1) \cdot V_{\mathrm{IN}}} \tag{4.1}$$

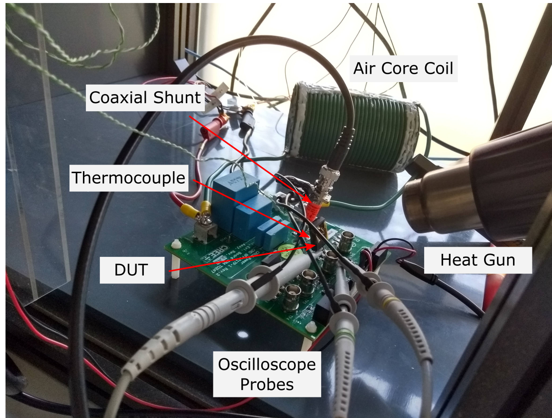
By selecting an appropriate N value and separating the charging pulses enough in time ($t_{\text{cool-down}}$), the self-heating of the DUT during the coil charging phase can be minimized.

The inductance value of the coil L_{COIL} must be carefully selected. On the one hand, low V_{SW} voltage operation points may require large charging times if L_{COIL} is too large. Hence, a coil with small inductance will lead to a faster charging phase and less self-heating. On the other hand, if L_{COIL} is selected too small, the coil will quickly loose its energy due to the losses of the FWD during the cool-down intervals ($t_{\text{cool-down}}$). Therefore, a trade-off between the time-spacing of the charging pulses $t_{\text{cool-down}}$ and the Δt charging times has the be found. A parallelization of SiC diodes or the use of a SiC MOSFET in its third quadrant operation as FWD (low series resistance) may help extending the max. time interval $t_{\text{cool-down}}$ that can be configured in the setup.

The measurement of the turn-on switching waveforms at the targeted current value I_{MEAS} is carried out at the beginning of the Nth pulse. It is important to configure the oscilloscope with the highest time resolution possible in this time interval.



(a) General view of the measurement setup



(b) Detailed view of the measurement fixture

Figure 4.2: Photos of the proposed measurement setup

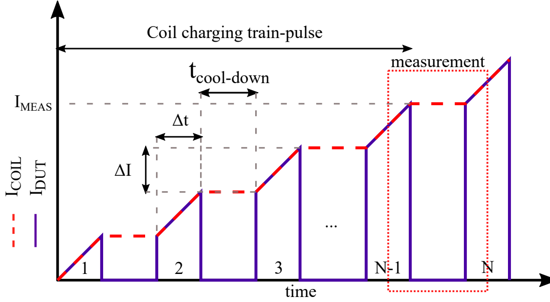


Figure 4.3: Proposed time diagram for DPT measurements to minimize self-heating

4.1.3 Measurement time interval selection

The current and voltage commutation intervals of a hard-switched inductive load turn-on event, typical of a DPT, are shown in fig. 4.4. The current and voltage waveforms overlap creating a characteristic scalene acute triangular shape.

The time between $t_1 - t_2$ corresponds to the current commutation interval. The drain current i_{D} increases from zero to the coil current at a pace (di/dt) defined by the transconductance G_{m} of the transistor and the max i_{G} supplied by the gate driver. This in turn, charges the voltage dependent input capacitance of the device $C_{\mathrm{GS}}(V_{\mathrm{DS}}, V_{\mathrm{GS}})$ throughout the series resistance $R_{\mathrm{DRIVE}}+R_{\mathrm{G}}$. As for the voltage V_{DS}, it remains constant during this time interval.

The time interval $t_2 - t_3$ corresponds to the voltage commutation interval. Once the coil current has fully commuted from the FWD to the DUT, the FWD releases the until-now-clamped switching node and V_{DS} decreases down to the on-voltage of the DUT $V_{\mathrm{DS_ON}}$. The duration of this interval (dv/dt) is mainly defined by the discharge process of the gate-drain capacitance of the power MOSFET C_{GD} (see section 3.3.2 for a detailed analysis) and is independent its IV characteristics.

Generally speaking, in a turn-on event the current commutation interval $(t_1 - t_2)$ is highly dominated by the IV characteristics of the MOSFET and C_{ISS}, whereas the voltage commutation interval $(t_2 - t_3)$ is governed mainly by the C_{GD} capacitance discharge.

Recent works have already use dynamic tests to study the IV characteristics of power MOSFETs responsible for its dynamic behavior.

In [20] the current and voltage waveforms measured in a DPT were used to study the transfer characteristics of a SiC power MOSFET at high voltages. To avoid the effect of parasitics in the measurements, the authors suggest to switch the device slowly. However, this leads to excessive self-heating of the DUT during the measurements.

In [103, 29] the Miller effect during the voltage commutation interval ($t_2 - t_3$) was used to extract the IV characteristics of a SiC power MOSFET at high voltage. This technique, however, suffers from the following drawbacks:

- The current peak arising from reverse-recovery and switching node capacitance discharge is added to the DUT channel current in the power loop. This leads to a wrong i_{D} measurement of the DUT in the coaxial shunt of the measurement fixture.
- SiC power transistors present a characteristic non-flat plateau. By assuming a constant plateau voltage, the proposed technique introduces a significant error in the calculation of the static IV characteristics.
- The energy dissipated during the voltage commutation interval, specially when switched slowly to reduce the effect of PCB-parasitics, make difficult the extraction of isothermal measurements due to self-heating.

By using the current commutation interval ($t_1 - t_2$) instead, these problems can be avoided, plus the following benefits are gained:

- The current measured in the resistive coaxial shunt in this time interval fully corresponds to that of the transistor channel. No reverse-recovery or capacitive parasitic discharge are added to the measured current.
- Since the current commutation interval happens at the beginning of the commutation process, almost no energy is dissipated in the DUT. As a result, measurements can be extracted with negligible self-heating.
- The voltage drop due to di/dt in the extrinsic parasitic inductances L_{D} and L_{S} is negligible compared to the high blocking voltage V_{DS} set in the DUT during this interval. Nevertheless, it can be subtracted as explained in section 4.1.4 to achieve the highest accuracy.

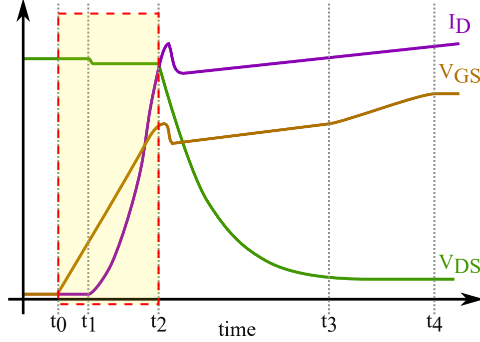


Figure 4.4: Sketched IV waveforms of power MOSFET in a DPT during a turn-on switching transient. Highlighted, the time interval proposed to extract the static IV characteristics of the DUT

As a result of the summarized points, the current commutation interval is proposed in this work as the best time window to extract the extended IV characteristics of a power MOSFET with the highest accuracy.

4.1.4 Calculation of the intrinsic voltages from dynamic measurements

The current and voltage waveforms measured in the terminals of the DUT in a dynamic test such as a DPT are time-varying waveforms. Time-varying voltage and current waveforms charge and discharge L and C parasitic components such as parasitic series inductances of the surrounding circuitry or the intrinsic capacitances of the power switch. As a result of this, the extrinsic time-varying voltages measured in the terminals of the DUT in an oscilloscope differ from the intrinsic voltages controlling the IV characteristics of the MOSFET.

To extract the intrinsic IV characteristics of the DUT from dynamic measurements the non-static model of the DUT and surrounding circuitry, shown in fig. 4.5, needs to be considered. As nomenclature, the time-varying entities are represented with small letters and time-constant entities with capital letters. For example the time-varying gate-source voltage $v_{\mathrm{GS}}(t)$ is simply written as v_{GS} and a specific steady DC gate-source voltage as V_{GS}.

During a turn-on switching transient, the current injected in the

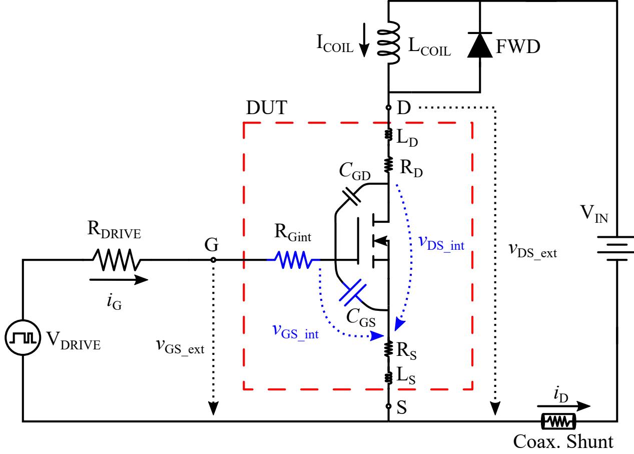


Figure 4.5: Equivalent circuit of the proposed DPT measurement fixture. The dashed contour depicts the DUT and the parasitic components R_{Gint} and C_{GS} which can be used to infer V_{GSint} from dynamic measurements

gate of the transistor charges the input capacitance. This current creates a voltage drop across the gate resistance R_{Gint} and the source resistance R_{S} that shifts the measured $v_{\text{GS_ext}}$ from the $v_{\text{GS_int}}$ voltage that defines the IV characteristics of the DUT.

Additionally, the variation of the current in time (di/dt) creates a voltage drop across the parasitic series inductances L_{D} and L_{S} that displaces the extrinsic drain-source voltage $v_{\text{DS_ext}}$ from the intrinsic one $v_{\text{DS_int}}$.

As explained in section 4.1.3, the current i_{D} measured during the current commutation interval corresponds exclusively to the current flowing through the transistor channel.

Assuming the equivalent circuit of fig. 4.5, the intrinsic time-varying drain-source voltage of the DUT during the current commutation interval can be calculated as

$$v_{\text{DS_int}} = v_{\text{DS_ext}} - i_{\text{D}} \cdot (R_{\text{D}} + R_{\text{S}}) - (L_{\text{D}} + L_{\text{S}}) \cdot \frac{di_{\text{D}}}{dt} \tag{4.2}$$

Where $v_{\text{DS_ext}}$ is the voltage measured in the terminals of the DUT and R_{D}, L_{D}, L_{S} and R_{S} are the parasitic series inductances

and resistances in the drain and source terminals respectively.

The parasitic inductances and resistances of the transistor package can be extracted using the methodology provided in section 2.4. However, if a low parasitic measurement fixture and package of the DUT are used, the first term of eq. (4.2) dominates over the second and third terms and these can be neglected.

The calculation of $v_{\mathrm{GS_int}}$ is more sensitive though and can be accomplished in different ways, as will be discussed in the next section.

Calculation of $v_{\mathrm{GS_int}}$ based on the gate resistance R_{Gint}

The time-varying gate current injected in the gate of the MOSFET during the switching transient i_{G} can be calculated applying Ohm's law on the resistor R_{DRIVE} known the voltage drop across it. With that, the time-varying intrinsic gate-source voltage $v_{\mathrm{GS_int}}$ can be calculated as

$$v_{\mathrm{GS_int}} = v_{\mathrm{GS_ext}} - i_{\mathrm{G}} \cdot (R_{\mathrm{Gint}} + R_{\mathrm{S}}) - L_{\mathrm{G}} \cdot \frac{di_{\mathrm{G}}}{dt} - L_{\mathrm{S}} \cdot \frac{di_{\mathrm{D}}}{dt} \quad (4.3)$$

Where $v_{\mathrm{GS_ext}}$ is the extrinsic gate-source voltage measured in the pins of the DUT, R_{Gint} is the internal gate resistance of the DUT, R_{S} is the source resistance of the DUT and fixture, and L_{G} and L_{S} are the parasitic series inductances corresponding to DUT package and PCB traces connected to the gate and source terminals of the DUT. The contribution of the DUT package to the parasitic series inductances L_{G} and L_{S} and resistance R_{S} can be extracted with the measurement technique described in section 2.4. These components can be zeroed-out by forcing a slow switching. In such case, eq. (4.4) can be simplified to

$$v_{\mathrm{GS_int}} = v_{\mathrm{GS_ext}} - i_{\mathrm{G}} \cdot R_{\mathrm{Gint}} \quad (4.4)$$

However, it is always preferred to switch the device fast to avoid self-heating (see section 4.1.2). For fast switching devices such as SiC power MOSFETs, this method is prone to suffer from poor accuracy due to its sensitivity to the parasitic components R_{S}, L_{S} and L_{D}. Furthermore, the temperature dependence of R_{S} may lead to accuracy errors when measurements are extracted at different temperatures.

Calculation of $v_{\mathrm{GS_int}}$ based on the input capacitance C_{ISS}

An alternative method to calculate $v_{\mathrm{GS_int}}$ consist in calculating the voltage drop across the intrinsic gate-source capacitance of the DUT C_{GS}. In section 2.4 the methodology to characterize the small signal circuit of a power MOSFET with S-Parameters was provided. In chapter 3 this methodology was used to calculate the intrinsic capacitances of power MOSFETs and its dependence with the gate-source and drain-source voltages $C_{\mathrm{GS}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$. The characterization of $C_{\mathrm{GS}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$ of the DUT used in this work were presented in section 3.2 and a 3D plot of this capacitance is plotted in fig. 3.5.

During the turn-on current commutation interval ($t2-t3$ in fig. 4.4) the current injected in the gate of the DUT (i_{G}) charges and discharges the gate-source and gate-drain capacitances respectively. These in turn are also dependent on the time-varying terminal voltages of the power MOSFET. Thus, i_{G} can be written as a function of the time-varying interelectrode capacitances c_{GS} and c_{GD} as

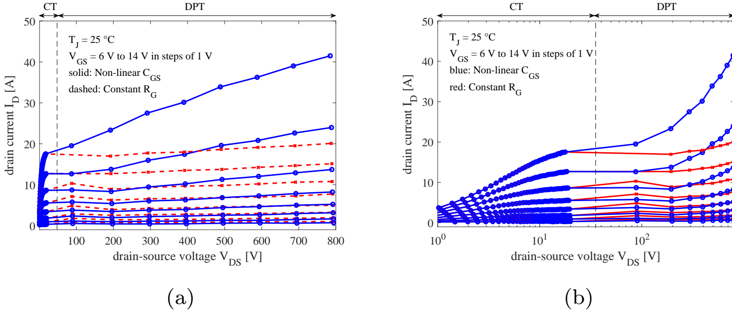
$$i_{\mathrm{G}} = c_{\mathrm{GS}} \cdot \frac{dv_{\mathrm{GS}}}{dt} + c_{\mathrm{GD}} \cdot \frac{dv_{\mathrm{GD}}}{dt} \tag{4.5}$$

Compared to C_{GS}, C_{GD} is generally speaking very small at large V_{DS} values (see fig. 3.11e). In addition, V_{DS} remains constant during the current commutation time interval. As a result, the second term of eq. (4.5) can be zeroed-out and it can be assumed that the current injected in the gate of the power MOSFET i_{G} exclusively charges the gate-source capacitance C_{GS}. Thus, the intrinsic gate-source voltage $v_{\mathrm{GS_int}}$ can be calculated as the voltage drop across the gate-source capacitance applying numerical integration as

$$v_{\mathrm{GS_int}} = V_{\mathrm{GS_ext}}(t_0) + \int \frac{i_{\mathrm{G}}}{c_{\mathrm{GS}}} \cdot dt \tag{4.6}$$

One of the benefits of this method is clear from inspecting eq. (4.6): this method is independent of the parasitic series inductances and resistances R_{S}, L_{S} in contrast with that of eq. (4.4). This means the method does not require a characterization of the measurement fixture and, in addition, the accuracy of $v_{\mathrm{GS_int}}$ calculation is not affected by the switching speed or oscillations at all.

As comparison, the IV characteristics of a SiC power MOSFET extracted with eq. (4.4) and eq. (4.6) are plotted in fig. 4.6 in blue-solid lines and red-dashed lines respectively. The low voltage IV values extracted with a curve tracer are also plotted in the figure.



(a) (b)

Figure 4.6: Comparison of the IV characteristics of a SiC power MOSFET extracted from R_{G} (dashed) and C_{GS} (solid) plotted in linear (a) and logarithmic scale (b). The latter method is not affected by the voltage drop in R_{S} and reproduces more accurately the IV characteristics of the DUT

Whereas the transition between the CT measurements and the measurements extracted from a DPT are in both cases smooth and continuous, the IV characteristics extracted using both methods seem to differ above $I_{\mathrm{D}} = 7\,\mathrm{A}$. This difference is attributed to the voltage shift in $V_{\mathrm{GS_int}}$ arising from the voltage drop across the parasitic source resistance R_{S} at high currents, which has been neglected in eq. (4.4) since it was not possible to characterize it. In contrast, the method based on the calculation of the intrinsic voltage from C_{GS}, eq. (4.6), is independent of the effect of R_{S}, providing more accurate results at high currents. Due to its superior accuracy and robustness against the effect of surrounding parasitics, the method using eq. (4.6) is preferred to calculate $v_{\mathrm{GS_int}}$ and will be used in following calculations in this work.

4.2 Extended IV characteristics of SiC power MOSFETs

The measurement methodology explained in section 4.1 was used to extract the extended IV characteristics of a 1200 V, 22 A vertical planar SiC power MOSFET [89] (same DUT as in chapter 3) up to 50 A current and 800 V voltage (i.e. 40 kW power).

The measurement setup (see section 4.1.1) was configured to ac-

quire 8 measurements of the turn-on transients at voltages ranging from 100 V up to 800 V. This was sufficient to map the complete IV characteristics of the DUT up to 50 A, beyond the rated operating conditions of this device. An 24 µH air core coil was selected for the measurement setup following the indications provided in 4.1.2. The waveform generator was configured with a PWM signal in burst mode with $N = 5$ pulses of duty cycle DC. By varying DC, the pulse train (see fig. 4.3) could be adapted to the different switching voltages to reach a maximum current of 50 A with negligible self-heating. All measurements were averaged in the oscilloscope with $N_{\text{avg}} = 10$ measurements to reduce noise introduced by the measurement setup and quantization noise of the oscilloscope.

To extract the intrinsic IV characteristics of the DUT, the current commutation time interval was selected as explained in section 4.1.3. The intrinsic voltages at the terminals of the DUT are calculated directly from the oscilloscope waveforms. $V_{\text{DS_int}}$ was calculated using eq. (4.2) and $V_{\text{GS_int}}$ as the voltage drop across the intrinsic gate-source capacitance applying numerical integration using eq. (4.6) as explained in section 4.1.4.

The measurements were carried out at case temperatures T_{C} of 25 °C and 175 °C by streaming air over the DUT with a heat gun. The temperature in the case T_{C} was measured with a type-K thermocouple attached to the thermal pad of the DUT.

The complete IV characteristics extracted from the measurements are plotted in figs. 4.7 and 4.8. From $V_{\text{DS}} = 0$ V to $V_{\text{DS}} = 20$ V the measurements are carried out with a B1505A curve tracer. Above $V_{\text{DS}} = 100$ V the measurements are extracted with the proposed measurement technique. The combination of both measurement sets maps the complete static IV characteristics of the SiC power MOSFET from the linear to the high voltage saturation region.

4.2.1 Estimation of self-heating

The maximum junction temperature of the DUT during the measurements was simulated with the electrical and thermal SPICE models provided by the manufacturer [89]. At the DUT rated current of 22 A the simulated, self-heating was negligible both at 25 °C and 175 °C. The worst case simulation results are summarized in table 4.1 with a peak self-heating of 16 °C reached at the highest switching voltage, 800 V.

V_{SW}	T_{C}	Period (T)	Duty Cycle (DC)	max $T_{\mathrm{J_sim}}$
100 V	25 °C	1 µs	15 %	35 °C
800 V	25 °C	1 µs	1.65 %	41 °C

Table 4.1: Maximum junction temperatures reached during the coil charging phase up to 50 A calculated from simulations of the measurement setup using the thermal and electrical SPICE models provided by the manufacturer [89]

4.2.2 Short channel effects and effect of temperature in SiC power MOSFETs

The output characteristics of the DUT at 25 °C are plotted in figs. 4.7a and 4.7b in linear and logarithmic scale respectively. These results have been published in [104]. The non-saturating nature of the IV characteristics of the SiC power MOSFET extends up to the high-voltage V_{DS} region. This effect is attributed to short channel effects (SCE) [18, 19, 110, 82, 111] in the following manner.

Firstly, at high V_{DS} voltages, the effective length of the inversion layer shrinks due to channel length modulation (CLM). As a result, the current I_{D} at a fixed V_{DS} increases proportional to V_{DS}. Secondly, the threshold voltage of the device decreases at high V_{DS} voltages, as seen in fig. 4.8b. This effect is known as drain induced barrier lowering (DIBL) and contributes to an increase of I_{D} proportional to V_{DS}. Both CLM and DIBL add to an increase of the drain current I_{D} in the high voltage saturation region proportional to V_{DS} that explains the resulting non-flat IV characteristics shown in the measurements.

SCEs have a huge impact in the transcoductance of SiC power MOFETs which, in case of the DUT here analyzed, increases at high V_{DS} voltages for V_{GS} voltages above 10 V (fig. 4.8d). This may lead to unexpectedly high di/dt at the end of the current commutation interval if the device switches current values that set a plateau voltage above 10 V.

The effect of temperature in the IV characteristics of the SiC power MOSFET can be analyzed from the plots in fig. 4.8. At a first glance, a different temperature behavior is observed depending on the operation region: In the linear mode the drift resistance R_{Drift} dominates the total on-resistance of the MOSFET [21]. Thus, the degradation in the carrier mobility of the drift layer at high temperatures leads to an increase of the on-resistance of the device and the

corresponding drain current degradation [112]. Contrary to this, in the high V_{DS} voltage operating region, the current of the SiC MOSFET experiences an increase of its value proportional to the junction temperature. The IV characteristic of the device is governed by the mobility of minority carriers in the inversion layer of the MOSFET structure. This is degraded by different scattering phenomena (mainly Coulomb scattering and surface phonon scattering) [101] and enhanced by the density of traps in the SiO_2/SiC interface (Dit) [23, 113]. Below 200 °C Coulomb scattering is the dominant scattering mechanism [28]. However, in the specific case of this DUT, the increase of Dit results in an overall improvement of the inversion layer mobility which dominates over scattering phenomena and leads to an overall increase of the drain current at high temperatures. This can be appreciated in the negative temperature coefficient (NTC) of the threshold voltage shown in fig. 4.8c. The limitations of the measurement setup did not permit the extraction of measurements at higher temperatures. However, beyond 200 °C a degradation of the inversion layer mobility, due to dominant phonon scattering, is expected, which should result in a reduction of the drain current of the device though [28]. The slightly increase of DIBL at high temperature seen in fig. 4.8c points to the conclusion that the density of interface traps is not affected by high V_{DS} voltages.

At this point it is important to remark, that the temperature behavior of the DUT here analyzed can not be generalized for all SiC power devices. Indeed, as the quality of the SiO_2/SiC interface gets better in the coming years due to technology maturity, Dit should be reduced to an extent that scattering phenomena always dominates the mobility of the channel, thus leading to an always less-conductive MOSFET in the high voltage saturation region as the temperature increases.

The effect of temperature and SCEs in the IV characteristics of a SiC power MOSFET can be summarized in the following conclusions (assuming $T_J < 200$ °C):

1. The transconductance G_m of this DUT increases proportional to V_{DS} and has a positive temperature coefficient (PTC) in the high voltage saturation region.

2. The threshold voltage V_{th} decreases proportional to V_{DS} and has a negative temperature coefficient (NTC).

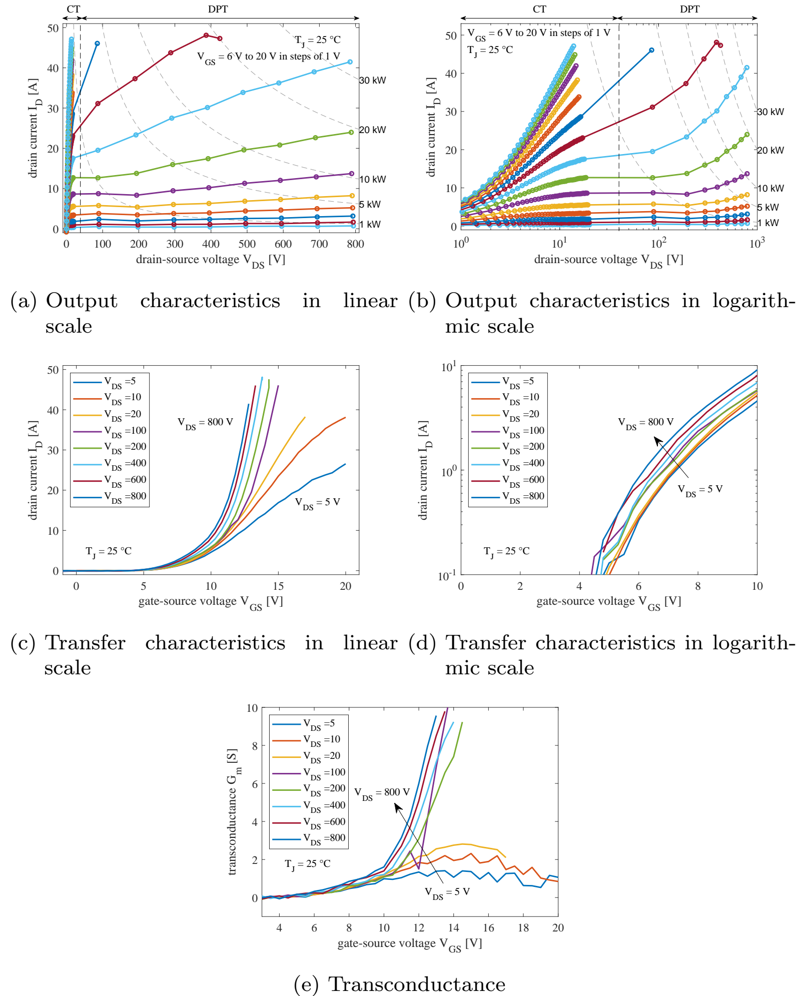
These effects explain the impact of V_{DS} and temperature in the

dynamic behavior of SiC power MOSFETs reported in recent publications [85, 86, 87, 22]. Higher V_{DS} and temperature values lead to an increase of G_{m} which results in a negative shift of the plateau voltage V_{Plateau}. As a result, the current commutation speed (di/dt) during turn-on and turn-off events increases and decreases respectively proportional to V_{DS} and temperature.

4.3 Conclusions of this chapter

The dynamic behavior of a power MOSFET under clamped inductive load switching conditions is strongly determined by its IV characteristics in the high voltage saturation region. In this region of the IV-characteristic the power MOSFET reaches dozens of kW power. Available characterization solutions rely on measurement techniques which suffer from either power limitations or excessive self-heating. As a result of this, the IV characteristics of power MOSFETs can not be characterized in the whole range of bias conditions experienced during the operation in a power circuit. This chapter provided a measurement methodology that extends the power range in which the IV characteristics of a power MOSFET can be measured. The technique relies on the current and voltage waveforms measurements from a double pulse tester, which adequately post-processed can be used to extract the static IV characteristics of the power switch up to dozens of kW power. Different methods were contrasted and evaluated in the chapter, concluding that the lowest self-heating and highest accuracy is achieved from measurements in the current commutation interval and calculating the intrinsic gate-source voltage as the voltage drop across the gate-source capacitance of the MOSFET.

The proposed measurement methodology was used to extract the static iso-thermal IV characteristics of a commercially available SiC planar power MOSFET up to instantaneous 800 V and 50 A at temperatures ranging from 25 °C to 175 °C. Results of the measurements of this specific device revealed non-saturating IV characteristic that extended up to the high voltage operation region of the power device. Furthermore, the current of the SiC power MOSFET experienced a PTC in the high voltage operation region in the temperature range of 25 °C to 175 °C. These effects were attributed to the presence of short-channel effects and the temperature dependence of the density of traps in the SiO_2/SiC interface respectively.



(a) Output characteristics in linear scale

(b) Output characteristics in logarithmic scale

(c) Transfer characteristics in linear scale

(d) Transfer characteristics in logarithmic scale

(e) Transconductance

Figure 4.7: IV characteristics of the SiC power MOSFET at T_J = 25 °C. The measurements at low V_{DS} voltages are extracted from a CT. The high V_{DS} voltage measurements are extracted from the transient waveforms of a DPT applying the proposed measurement technique

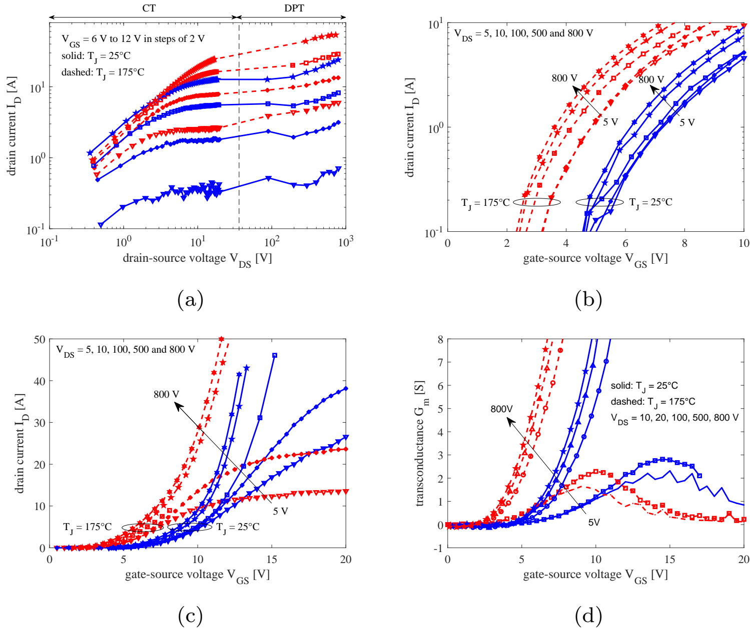


Figure 4.8: Effect of temperature (solid-blue: $T_{\mathrm{J}} = 25\ ^{\circ}\mathrm{C}$, dashed-red: $T_{\mathrm{J}} = 175\ ^{\circ}\mathrm{C}$) in the output characteristics (a), the threshold voltage (b), transfer characteristics (c) and the transconductance (d) of the SiC power MOSFET.

The impact of these effects in the dynamic behavior of this specific SiC power MOSFET in the application were discussed and correlated with the dynamic measurements of similar SiC power MOSFETs reported in recent publications.

Chapter 5

Conclusions

Emerging SiC power semiconductor devices feature superior electrical characteristics and ultra-fast switching speeds that are the key to develop the next generation of high efficient power conversion circuits. The dynamic behavior of these promising devices is still unexplored and leads to manifold challenges to unlock their full potential in the design of efficient power converters. Classical characterization solutions, mainly tailored for Si power devices, are not sufficient to describe the behavior SiC power MOSFETs. As a result, datasheets and simulation models of SiC power MOSFETS may not be descriptive enough and miss information which might be relevant to the circuit designer.

This work proposed novel measurement methodologies that broaden the bias conditions at which the static IV and CV characteristics of power MOSFETs can be characterized. The different measurement techniques are summarized in the structure of this work as follows.

In Chapter 2, S-Parameter theory was tailored to carry out network analysis of the equivalent circuit of vertical power MOSFETs using a network analyzer as measurement instrument. This included the characterization of the voltage-dependent inter-electrode capacitances, the extraction of parasitic series inductances and resistances and the individual characterization of the channel- and drift-resistances that add to the total on-resistance of the power semiconductor device. Whereas conventional characterization solutions require the use of different measurement fixtures for that, the proposed characterization technique requires only one, thus reducing the complexity of the measurement setup and the overall characterization time. The accuracy of the proposed measurement technique was in-depth ana-

lyzed showing satisfactory results for the characterization of modern SiC power MOSFETs.

Chapter 3 proposed a measurement setup that enables the CV-characterization of a power MOSFET up to its high-current linear and saturation region. The proposed technique broaden the measurement scope of conventional solutions, which are restricted to zero-current bias conditions, to application operating conditions. CV measurements of a modern SiC power MOSFET at combined bias voltages ranging from $V_{\mathrm{DS}} = 0$ - 40 V and $V_{\mathrm{GS}} = 0$ - 20 V permitted mapping the complete CV characteristics of the SiC power device in its full operating range of bias conditions up to $I_{\mathrm{D}} = 50$ A current. Both C_{GS} and C_{GD} showed a strong non-linearity as a function of the terminal voltages V_{GS} and V_{DS}, these being measured higher in linear and saturation region compared to their value measured at zero-current bias conditions. The junction temperature also showed a strong impact in the measured value of the inter-electrode capacitances in linear and saturation region. The revealed V_{GS} voltage and temperature dependence are often neglected in literature, circuit design and simulation models, but imply to have a strong impact in the switching characteristics of SiC power MOSFETs. Furthermore, a methodology to extract the gate-charge $Q_{\mathrm{G}} - V_{\mathrm{GS}}$ characteristics of SiC power MOSFET was presented. This technique relies on the numerical integration of the extended CV characteristics of the power MOSFET, what permits a clear separation of the gate charge distribution between the drain and source electrodes of SiC power MOSFETs and. The results of the gate charge values computed with the proposed technique were contrasted with those extracted using the JESD24-2 standard providing higher accuracy and versatility.

Chapter 4 presented a novel measurement technique to characterize the IV characteristics of power MOSFETs beyond the power limits of conventional measurement instruments. The IV characteristics of a commercially available SiC power MOSFET was measured up to application power levels (instantaneous 50 A and 800 V) with negligible self-heating. The extracted IV characteristics of the SiC power MOSFET revealed the presence of short-channel effects that affect the dynamic characteristics of the power device. The output conductance of SiC power MOSFETs in the high voltage saturation region might be modulated by large V_{DS} values what leads to a pronounced non-saturating slope of the IV characteristics. The effect of temperature in the IV characteristics of the SiC power MOSFET

was also analyzed in the temperature range from 25 °C to 175 °C. A positive temperature coefficient of the drain current in the high voltage saturation region was measured. This effect is associated to the strong temperature dependence of the density of traps in the SiO_2/SiC interface, which shifts the threshold voltage of the device to lower values and enhances the conductivity of the MOSFET channel.

The characterization techniques collected in this work revealed important insights concerning the dynamic behavior of SiC power MOSFETs through their extended IV and CV characteristics. These may be unknown to a circuit designer that relies on classical characterization methods. The proposed characterization techniques enable new possibilities for the improvement of SiC power MOSFET technology processes and compact device modeling which might contribute to achieve a higher grade of optimization in the development of more efficient and reliable SiC-based power converters.

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