Design of Frequency-Converting Monolithic Integrated Circuits for Millimeter-Wave Applications

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Executive Summary

The fifth generation of cellular systems or, short, 5G, will be the fastest deployed mobile communication technology in history. Although, in the year 2021, we are still in the middle of its roll-out, the definition of the successor generation, 6G, is eagerly discussed. What are the performance requirements for a 6G connection? What are the key applications, that will drive the development? And what are the key technologies that make 6G possible in the first place?
One technology in particular is treated to "become the potential force of future wireless communications": the terahertz technology. The possible employment scenarios for terahertz bands in 6G are manifold, from long range use cases like backhauling, to mid-range indoor wireless personal area networks, to short range intra-device communication and so-called data-showers. But not only communication systems benefit from the progress made in terahertz technologies. Terahertz radiation can also be employed for medical reason, e.g. detection of cancerous tissue, in security applications as ultra-high resolution imaging helps to detect hidden weapons or explosive or in material analysis and testing, where an accuracy in the range of millimeters is necessary.
Besides giving a broad overview on the questions mentioned above, this thesis focuses on how to efficiently utilize the low terahertz spectrum in the frequency range from 220 to 325 GHz, also called H-band. This work presents an introduction on several techniques necessary for designing frequency-converting monolithic millimeter-wave integrated circuits for this frequency range. A special focus is put on a new approach to assess stability in such circuits that eliminates shortcomings of the conventional procedures.
Furthermore, six different frequency-converter MMICs in a 35 nm gate-length InGaAs mHEMT technology are presented: a nonlinear resistance up- and down-converter, a dual-gate up- and down-converter, a gate-pumped transconductance up-converter and a half Gilbert cell up-converter. To the author's best knowledge, the last three architectures have never been analyzed before for the H-band frequency range using that technology. Additionally, three of these MMICs were fabricated in different versions in order to optimize their performance. Each design is explained in detail, their advantages and their disadvantages are evaluated. The measurement results of the MMICs either match the state of the art or in particular regarding the active versions even outperform it. Thus allowing them to be considered for integration in future MMIC designs using this technology.
Finally, three examples will be given where a selection of the discussed frequency-converter architectures are integrated with other functional stages like frequency multipliers and amplifiers to form a millimeter-wave transceiver: a highly linear FMCW radar receiver with a 50 GHz bandwidth, a heterodyne communication receiver facilitating multi-channel transmissions with carrier aggregation at W-band and a homodyne communication receiver with an integrated antenna for low-cost assembly on a PCB. All of these circuits operate in H-band. By integrating the frequency-converters with other functional stages a better assessment of their performance in a real-life environment can be deduced. The designs and

the target applications are thoroughly described and the corresponding measurement results are presented, analyzed and compared to state-of-the-art circuits for the same or at least a similar application. Especially designs employing the active frequency-converters outperform their passive counterparts in terms of efficiency by allowing strongly reduced footprints of transceivers MMICs of up to 42 % and reducing the necessary DC power by up to 70 %. Thereby, this thesis provides insight into the design considerations of terahertz frequency-converters, the trade-off of different circuit architectures and topologies for certain applications, the obstacles that can occur during their development and approaches to overcome them.

Zusammenfassung

Die fünfte Mobilfunkgeneration, kurz 5G, wird die am schnellsten bereitgestellte Mobilfunktechnologie in der Geschichte sein. Und obwohl sich 5G im Jahr 2021 noch mitten im Aufbau befindet, wird bereits über die Definition des Nachfolgers, 6G, diskutiert. Welche Anforderungen muss 6G erfüllen können? Was sind die Schlüsselanwendungen, die die Entwicklung von 6G vorantreiben und welche Technologien kommen in Frage, um diese Ziele erreichen zu können.
Insbesondere eine Technologie ist wegweisend und gilt als die treibende Kraft für zukünftige drahtlose Kommunikation, die Terahertz Technologie. Die Einsatzmöglichkeiten für Terahertzbänder in 6G sind vielfältig und reichen von Übertragungen über lange Strecken, wie "back-hauling", über mittlere Entfernungen, zum Beispiel sogennante kabellose personal area networksßu geräteinterner Kommunikation und Datenkiosken, die nur sehr kurze Distanzen überbrücken müssen. Jenseits der Kommunikationsanwendungen bietet Terahertzstrahlung aber auch einen Mehrwert für medizinische Anwednungen, bspw. in der Detektion von Krebgewebe, bei Sicherheitsanwendungen oder in der zerstörungsfreien Werkstoffprüfung, wo sie ultrahochauflösende Bildgebung ermöglicht.
Neben einem Überblick über mögliche Antworten auf die eingangs angeführten Fragen, beschäftigt sich diese Arbeit vor allem mit der effizienten Nutzbarmachung des unteren Terahertzspektrums von 220 bis 325 GHz, welches auch H-Band gennant wird. Es werden verschiedene Techniken vorgestellt, die notwendig sind um monolithisch integrierte, frequenzumsetzende Millimeterwellen-Schaltungen in diesem Frequenzbereich zu entwerfen. Ein besonderes Augenmerk liegt dabei auf einem neuen Ansatz zur Stabilitätsanalyse, der bestimmte Mängel von konventionellen Herangehensweisen behebt.
Des Weiteren werden sechs verschiedene frequenzumsetzende MMICs in einer InGaAs mHEMT Technologie mit einer Gatelänge von 35 nm vorgestellt: ein resisitver Auf- und Abwärtsmischer, ein dual-gate Auf- und Abwärtsmischer, ein Transkonduktanzaufwärtsmischer sowie eine halbe Gilbertzelle als Aufwärtsmischer ausgeführt. Drei dieser MMICs wurden in verschiedenen Ausführungen produziert, um Möglichkeiten zur Optimierung zu untersuchen. Jedes Design wird im Detail vorgestellt und die Vor- und Nachteile ausführlich diskutiert. Die Messergebnisse der MMICs entsprechen dabei entweder dem Stand der Technik oder übertreffen diesen. Deswegen können sie in zukünftigen Funkkommunikationssystem als echte Alternative zu konventionellen Verfahren betrachtet werden.
Abschließend werden noch drei Anwendungsbeispiele vorgestellt, bei denen die frequenzumsetzenden Schaltungen mit anderen funktionalen Stufen, wie zum Beispiel Frequenzvervielfacher oder Verstärker, in einem Millimeterwellen-Transceiver integriert werden: ein hoch linearer FMCW Radarempfänger mit einer Bandbreite von 50 GHz, ein Heterodynempfänger für kabellose Kommunikation, der eine Mehrkanalübertragung mittels Carrier Aggregation im W-Band ermöglicht, sowie ein Homodynkommunikationsempfänger mit integrierter Antenne für einen kostengünstigen Aufbau auf einem PCB. Alle diese Schaltungen sind für das H-Band ausgelegt und durch die Integration mit anderen Stufen kann eine realitätsgetreuere Beur-

teilung der Leistungsfähigkeit der frequenzumsetzenden Schaltungen erfolgen. Die Designs und die Zielanwendungen werden ausführlich beschrieben, die zugehörigen Messergebnisse vorgestellt, analysiert und mit dem Stand der Technik verglichen. Insbesondere die integrierten Schaltungen bei denen aktive Mischer eingesetzt werden, zeigen eine deutlich bessere Effizienz im Gegensatz zu jenen mit passiven. Die notwendige Chipfläche konnte hierdurch um bis zu 42% reduziert werden und die DC Stromaufnahme sogar um bis zu 70%.
Diese Arbeit liefert damit wertvolle Erkenntnisse über Abwägungen, die während des Designprozesses für frequenzumsetzende Schaltungen im unteren Terahertzspektrum getroffen werden müssen, die Vor- und Nachteile verschiedener Schaltungsarchitekturen und Topologien für bestimmte Anwendungen sowie über Hindernisse, die während der Entwicklung auftreten können und Mittel und Wege sie zu beheben.

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Contents

Abbreviations

3GPP 3rd Generation Partnership Project

ADC analog-to-digital converter

AI artificial intelligence

Au gold

AR augmented reality

BB baseband

BCB benzo-cyclo-butene

BW bandwidth

CG conversion gain

CS common-source

CPWG grounded coplanar waveguide

DAC digital-to-analog converter

DC direct current

DuT device under test

FCC Federal Communications Commission

FEM finite element method

FEOL front-end-of-line

FET field effect transistor

FMCW frequency modulated continuous wave

GaAs Gallium Arsenide

IAF Fraunhofer Institute for Applied Solid State Physics IAF

ICC integrated conversion cell

IEEE Institute of Electrical and Electronics Engineers

IF intermediate frequency

InGaAs Indium Gallium Arsenide

IoE internet of everything

IoT internet of things

IP_{1dB} input-referred 1-dB compression point

ITU International Telecommunication Union

LIS large intelligent surface

LNA low-nose amplifier

LO local oscillator

LSB lower sideband

M2M machine-to-machine

mHEMT metamorphic high electron mobility transistor

MIM metal-insulator-metal

MIMO multiple-input and multiple-output

MMIC millimeter-wave monolithic integrated circuit

mmW millimeter-wave

MR mixed reality

NF noise figure

NiCr Nickel-Chromium

OP_{1dB} output-referred 1-dB compression point

PA power amplifier

PCB printed circuit board

PRBS pseudorandom binary sequence

RF radio frequency

PSK phase shift keying

QAM quadrature amplitude modulation

RAN radio access network

Rx receiver

SCC separated conversion cell

SiN Silicon Nitride

TFMSL thin film microstrip line

TIA transimpedance amplifier

Tx transmitter

USB upper sideband

VLC visible light communications

VR virtual reality

XR extended reality

1. Introduction

5 016 000 000 000 000 000 000 Byte or 5 ZByte per month is the global traffic volume predicted by the International Telecommunication Union (ITU) for the year 2030 [Int15]. To visualize this massive amount of data, it corresponds to the data capacity of 1 trillion single layer DVDs. Stacked on top of each other, this will create a tower of 1 270 000 km height or more than three stacks of DVDs each reaching the moon as visualized in Fig. 1.1.
In the year 2020 the global traffic was only 62 EByte. This would be an increase of 8000 %. At the same time, the number of connected devices is estimated to reach 500 billion. This corresponds to 59 devices per person for a population of 8.5 billion in 2030 [Uni15]. Especially the internet of things (IoT) is a big driver for this growth. Home applications, from home automation, home security and video surveillance to the so-called white goods, washing machines, dryers refrigerators and stoves to tracking applications will represent nearly half of the machine-to-machine (M2M) connections by 2023. The fastest growing sector will be connected car applications like fleet management, navigation, in-vehicle entertainment systems, emergency calling etc. Connected car is followed by connected cities applications. [Cis20] As a consequence, the predicted M2M traffic volume for 2030 alone will be ten times higher than the total data traffic today. Many of these applications can already be bought of the shelve and many more will be available in the near future with the progressing of the fifth generation of cellular systems or better known short as 5G. Although 2019 only 5 % of the world's population had access to 5G coverage, according to [Eri20] this number is estimated to grow up to 55 to 65 % for the year 2025. This would make 5G the fastest deployed mobile communication technology in history.
But even though we are just in the middle of its roll-out, it is already clear, that 5G will not

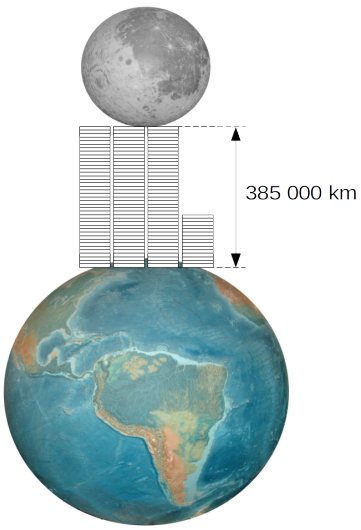


Figure 1.1.: The amount of monthly data traffic volume predicted for 2030 visualized by stacks of DVDs.

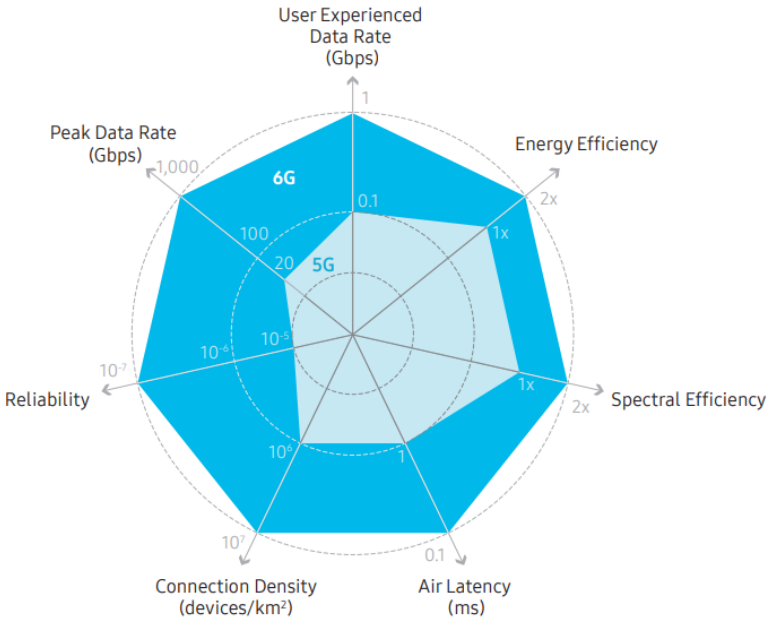


Figure 1.2.: Estimated performance requirements for 6G in comparison to 5G [Sam20].

be able to fulfill the demands of a future data-centric, data-dependent and automated society [GPM+20]. Therefore, the foundation for the next generation, 6G, is laid today to address requirements and expectations 5G cannot meet. Fig. 1.2 shows the predicted, necessary enhancements for 6G compared to 5G according to [Sam20].
But what are the applications that will require peak data rates up to 1000 Gbps, a 100 times higher reliability with an incredibly low error rate of $< 10^{-7}$ or an end-to-end latency of less than 1 ms? Academia, research communities and industry are working eagerly to identify the mega trends that will drive 6G and the key technologies capable of making it possible.
Since there are no limits to imagination, there are manifold visions of 6G and what might be the key services that will drive it. However, it is possible to identify some recurring themes which will be presented in the following. Some are further developments of 5G services and some are completely new emerging technologies.

1.1. Key Applications

Immersive extended reality is one of the top so-called killer applications that appear in almost all publications regarding 6G. Extended reality (XR) describes a combination of virtual reality (VR), augmented reality (AR) and mixed reality (MR). Often the speech is of a "truly immersive XR" experience, meaning that all five sensory inputs (sight, hearing, touch, smell and taste) are captured and real-time user interaction is provided [RAB+20]. Because of the five senses, XR is sometimes also referred to as five dimensions (5D) communications and services [CSBGJ+19]. There are various fields that will benefit highly from XR technology such as science, education, manufacturing industries, medicine and entertainment [Sam20]. But, to enable real-time user interaction in this truly immersive environment, XR cannot be compressed since coding and decoding is a time-consuming process. To transmit uncompressed

data, a very high system capacity ($>$1 Tbps), a very high per-user data rate ($>$1 Gbps) and a very low latency ($<$1 ms) are required [GPM+20]. To visualize the demands: Current AR technology requires 55.3 Mbps to support an 8K display. XR is predicted to have similar demands as 16K ultra-high definition quality video streaming that, even with compression, requires 0.9 Gbps throughput [Sam20]. This can clearly not be provided by the targeted 100 Mbps for 5G.

Holographic telepresence describes the possibility to render media for 3D hologram displays. Real-time capture, transmission and 3D rendering techniques are employed to obtain the holographically displayable content [Sam20]. In [XPLL11] a calculation of the required data rate for a 3D holographic display is performed. A colored, uncompressed hologram with a frame rate of 30 frames per second would require 4.32 Tbps and sub-millisecond latencies. With a peak data rate of 20 Gbps and a latency of $>$1 ms holographic communications cannot be supported by 5G [CSBGJ+19].

Unmanned mobility was initiated in 5G but will experience drastic improvements moving towards 6G. As previously mentioned, connected car applications are predicted to be the fastest growing sector in M2M communication. Fully autonomous vehicles promise safer traveling, improved traffic management and more comfort. But to realize this the density of sensors in vehicles has to be further increased. More sensors and more connectivity demand an increase in data rate up to terabytes per driving hour [CVGP+16] and unprecedented levels of reliability of more than 99.999 99 % [RAB+20]. Moreover these prerequisites have still to be fulfilled in high mobility scenarios up to 1000 km/h [GPM+20]. These are requirements that are impossible to meet with existing technology.

Industry 4.0 in connection with artificial intelligence (AI) will help to achieve full automatic control of processes, devices and systems. Started with IoT systems in 5G, the integration of more and more cyber physical systems will help to lift the boundaries between the real factory and a "cyber computational space" [LBK15] to create a smart factory. The need for human intervention will be reduced to a minimum. But, the prerequisites are not easy to fulfill. For high-precision manufacturing a high reliability up to the order of 10^{-9} and a low latency of 0.1 ms is necessary [BMRM19]. 5G is unable to fulfill these requirements of high precision real-time communication.

Pervasive connectivity means connectivity everywhere and always. As presented in the first section of the introduction, the number of subscribers will increase exponentially. The estimated number of device per km^2 for 5G is 1 million in dense areas. For 6G this is expected to multiply ten-fold to 10^7 devices per km^2 [ZXM+19]. In 5G the focus is on connecting machines with machines and letting cars communicate to other cars or the surrounding infrastructure (car-to-X). In 6G everything will be connected. This leads to a transformation of the IoT to a true internet of everything (IoE). IoE, a "seamless interconnection and autonomous coordination of massive number of computing elements and sensors, inanimate and living entities, people, processes and data through the internet infrastructure, is an emerging research and development towards enabling the connected universe from molecular sensors to vehicles and people." [The19]. The 5G infrastructure and technology is not build

to support this kind of pervasive connectivity.
Another aspect of the omnipresent connectivity and the ever-growing number of devices is the impact on our environment. Hundreds of billions of devices have to be supplied with power. To diminish the negative consequences for our ecosystem, we have to increase the energy efficiency by 10 to 100x with respect to 5G [ZXM+19, GPM+20]. If implemented properly the new generations of mobile communication can even help to reduce greenhouse gas emission by up to 15 % by 2030 [FGF+19].

1.2. Key Technologies

But, to tap the potential of 6G several challenges have to be overcome. So, what are the enabling technologies for the discussed 6G applications and scenarios? As always, when trying to predict the future there are many different opinions. Therefore, the list of the most promising candidates that will be presented in this section, is a snapshot of the technologies mentioned the most in recent publications concerning roadmaps to 6G

Novel Antenna Technologies already played an immense role especially in the form of massive multiple-input and multiple-output (MIMO) in the development of 5G to achieve higher spectral and energy efficiency and higher data rates at increased carrier frequencies. For 6G the progress has to continue to cope with the increasing free space path loss that comes with the necessary increase in carrier frequencies. Especially, so-called metamaterials are a promising technology to fuel antenna advancements as for example demonstrated in [ZQL+15].
Large intelligent surface (LIS) is an enhancement of massive MIMO and will facilitate the innovative ways for communication as presented before. [SBC20] Metasurface lenses and metamaterial antennas to realize beamsteering [ZE06, Pen00] or reconfigurable intelligent surfaces, that establish a propagation path in case a line of sight is not available [HZA+19, YYK20, DRC+20], are some examples for LIS implementation and its potential for 6G.

AI is omnipresent in all discussions about future technological developments. So, it is not surprising that AI in combination with machine learning also offers a great potential for the future of mobile communication. From user equipment, e.g. the cell phone, to the base station, to the underlying core network and application servers, there is no area that is not supposed to benefit from AI. It can optimize modulation, channel and source coding [KLL+18, OH17], the radio resource management, for example the allocation of bands and powers [AKA+20], and help to improve the network management and orchestration [MYLD20]. A standardization process of the 3rd Generation Partnership Project (3GPP) was successfully completed to support the introduction of AI in wireless networks [3GP19] and in 2018 leading mobile operators founded the O-RAN Alliance to enable AI technology in an open and efficient radio access network (RAN) [O-R18]. This recognition is a huge step towards the native support of AI in future 6G networks.

Network topology has to change to support the data-hungry applications mentioned before and to overcome the increased path loss for the millimeter-wave (mmW) range. The conventional cellular basestations have been static. But to meet the requirements of increased

data traffic and to fill the holes in coverage, flexible network deployment concepts have to be considered. For example, a self-moving network entity that itself in turn connects wirelessly to a static cellular network. Such a self-moving network could be a bus or a train that provides not only the passengers but also people in the vicinity on the outside with a network connection [Sam20]. This will lead to a highly dense employment of "tiny cells" [SBC20].
To further optimize the coverage and efficiency, user localization and mapping will be integrated in a 6G network helping to reduce interference, shape beamforming patterns and predict handovers.[GPM+20]
The incorporation of airborne and satellite radio access points falls also under the topic of network topology. For example, drones or high altitude platform stations flying at 20 km height and low Earth orbit satellite constellations at an altitude of several hundreds of kilometers can help to provide flexible network connection in case of spontaneous mass gatherings of people or to temporarily connect remote areas in case of a catastrophic event [CSBGJ+19].

Visible light communication To achieve peak data rates of 1000 Gbps and to enable the power hungry applications such as holographic communications, the 5G frequency spectrum is not sufficient. Therefore, the bandwidth has to be increased. One option is to exploit the visible light spectrum. Under good conditions visible light communication can achieve ultra high data rates, low latencies and secure communications. However, visible light links suffer from a limited coverage range, from noise introduced by other light sources, e.g. the sun, and a significant sensitivity to weather conditions since fog, rain, snow, haze etc. can block the signal beam [CHIJ18, GPM+20]. However, for indoor applications visible light communications (VLC) is a promising technology. This is especially of interest regarding the drastically growing number of M2M communication platforms that are based indoors.

Terahertz Technologies The ITU considers the upper end of the H-band (220 to 325 GHz) to "become the potential force of future wireless communications" [IR15]. Hence, in order to fuel the development of new wireless communication technologies, in 2019, the Federal Communications Commission (FCC) opened the spectrum between 95 GHz and 3000 GHz for experimental use and unlicensed applications [New19] and the Institute of Electrical and Electronics Engineers (IEEE) acknowledged the importance of THz communication in the standard IEEE Std. 802.15.3d-2017 [IEE17a].
The lower THz band offers huge available bandwidths that facilitate data transmissions in the hundreds of Gbps, higher link directivity, smaller component footprints and possesses higher resilience to eavesdropping [SSANA20].
Furthermore, the terahertz spectrum does not suffer from the same drastic limitations as the VLC. For example fog and haze are transparent for THz radiation, and successful transmissions can even be achieved when it is raining. [FMM16] states that "this makes THz links a promising candidate as reliable communication technology under most weather conditions."
THz communication applications cover link distances from cm to km, from intra-device communication [IR15], to so-called kiosk download or data showers [SKH+16, SSANA20], to indoor wireless personal area networks [SN15] and wireless links in data centers [KHD+15] to backhaul and fronthaul links [IEE17a].
Also other applications benefit from the progress in the utilization of the THz band, for example, ultra high resolution imaging in the security [CSW+14] and medical field [KVM+16],

accurate ranging with millimeter accuracy for material testing [MMW+19] and material analysis [GSHP14].
But, of course, there are still several issues to address in the future, from the low efficiency in power and frequency generation and frequency conversion, to lossy and noisy components and packaging as well as the high power consumption of Tbps digital data transfer and of baseband components, such as analog-to-digital converter (ADC)s, digital-to-analog converter (DAC)s [Sam20].
However unclear the exact form of 6G and its applications might be, according to the vast majority of publications, THz communication will loom large. Therefore, addressing the challenges is a big step towards the realization of 6G. And, this is exactly where this work ties in. It addresses circuit design for the utilization of the lower terahertz band, especially the frequency range from 220 to 325 GHz, also called H-band.

1.3. Thesis Outline and Goal

The goal of this thesis is to investigate the design of different mixer architectures and topologies for terahertz frequencies, to analyze their advantages and disadvantages and to discuss challenges in the design and how they can be overcome to optimize the performance in the future. Eventually, the presented results are supposed to provide a guideline for choosing and designing the best suited frequency converter architecture based on the system's or application's requirements. The work has the following outline:

Chapter 2 gives some background information on the functionality of the different types of frequency converters presented later. Furthermore, the principles of why and how single-ended mixers can be combined to form quadrature or balanced topologies are explained using a visual approach. Altogether, the chapter gives a basic understanding and an easy access to the main content of the work.

Chapter 3 focuses on simulation techniques and provides hands-on explanations on how crucial simulation for nonlinear designs can be conducted. The topic of stability analysis is discussed in more detail. A new approach also suitable for large signal simulations and its underlying theory is presented.

Chapter 4 gives an overview of the technology employed in this work: the 35 nm Indium Gallium Arsenide (InGaAs) metamorphic high electron mobility transistor (mHEMT) technology of the Fraunhofer Institute for Applied Solid State Physics IAF (IAF).

Chapter 5 discusses several frequency converter designs for terahertz frequencies. The chapter is divided in an up- and a down-converter section. For each mixer, design decisions that were made are discussed in detail and the corresponding measurement results presented. Eventually, the designs are compared among themselves as well as to the state of the art.

Chapter 6 presents three complex millimeter-wave monolithic integrated circuits (MMICs) for radar and communication applications integrating mixer stages that were presented in

chapter 5. The MMICs and their applications are fully described and the reasons for the choice of the employed frequency converter architecture is highlighted. Each section concludes by discussing the measurement results of the systems and how they compare to state-of-the-art MMICs for the same application.

2. Frequency Converter Fundamentals

This chapter gives a short overview of the architectures and topologies of frequency converters, that will be presented in the course of this work. Since these fundamentals are well-established and already described in various text books such as [Poz05, Ell08, Maa03, Voi13], the purpose of this chapter is to provide a short description on how the devices operate and facilitate an easy access to the content presented later.

2.1. Frequency Converter Architectures

2.1.1. Resistive Mixer

Fig. 2.1 depicts a basic resistive mixer schematic. The large signal is applied to the gate of the transistor, the intermediate frequency (IF) and radio frequency (RF) are connected to the drain. In this configuration, the resistive mixer can be used either as an up-converter or as a down-converter without changing the design. Here, the gate bias is applied through the gate's matching network. Conventionally, the RF is decoupled from the direct current (DC) supply network by using a $\lambda/4$ stub in series with a capacitor. This way the electrical short, that is presented by the capacitor at RF frequencies, is transformed into an electrical open. For lower frequencies, where the parasitics are not as dominant, also inductors can be employed to present a low-pass filter. Important to note is the absence of any drain voltage. This is one of the fundamentals in designing a resistive FET mixer [Maa03]. That means, that depending on the application the drain is either floating, which can be preferred for example for a zero IF mixer, or it can be connected to ground via a inductor and/or resistor to have a defined 0 V DC potential. The IF and RF matching networks also operate as filters to prevent the IF signal from flowing into the RF port and vice versa. Typically, the resistive FET mixer is biased around the threshold voltage of the transistor for minimum local oscillator (LO) power requirements.

The resistive mixer uses the variation of the transistor's channel resistance to produce intermodulation products. That means the transistor behaves like a time-varying resistance. An illustration of a typical characteristic curve of the channel resistance in dependency of the gate voltage is shown in Fig. 2.2, left. Since there is no drain voltage applied, the larger the input signal at the gate is, the larger is the variation of the channel resistance. This can be deduced from the black and blue curve in Fig. 2.2, right, which represent the channel resistance over time for a sine wave with three different amplitudes.

When the voltage swing is large enough to drive the gate voltage below the threshold voltage, where the channel presents an open circuit, and above the maximum gate voltage, were the channel is close to a short, the variation in channel resistance has reached a maximum. In this state the mixer can be represented by a time-varying switch, that switches the channel resistance between $R_{DS,on}$ and $R_{DS,off}$. In order to achieve maximum conversion gain, the

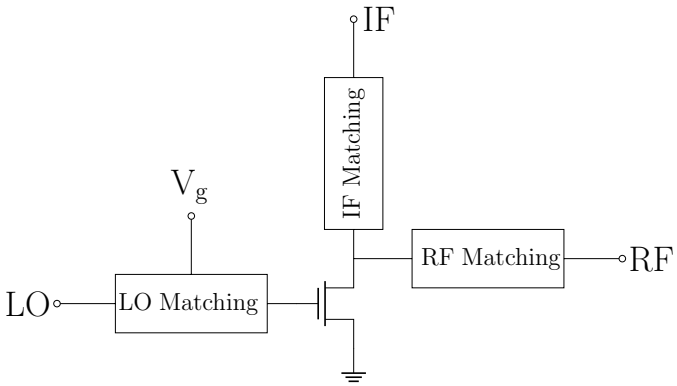


Figure 2.1.: Simplified schematic of a resistive field effect transistor (FET) mixer.

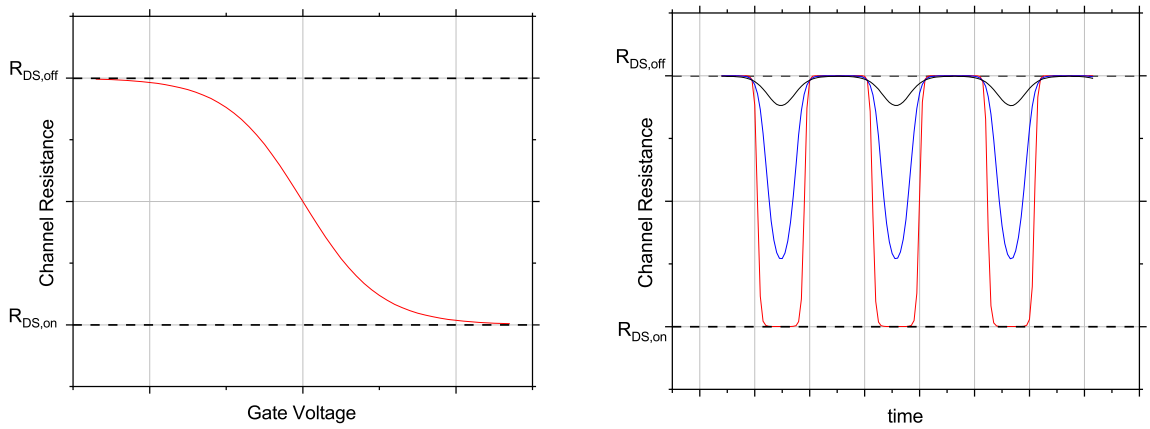


Figure 2.2.: Dependency of the channel resistance from the applied gate voltage (left) and over time when a sine wave with three different amplitudes (black, blue and red) is fed to the gate (right).

voltage swing has to be large enough to maximize the change in the channel resistance. This is why a resistive mixer needs a high LO drive power [Voi13]. But, as soon as the mixer has started to operate as a switch, a further increase in LO power will not result in a higher conversion gain anymore. The mixer is saturated with respect to LO power.

2.1.2. Nonlinear Transconductance Mixer

The underlying principle of a nonlinear transconductance mixer is using the large LO signal to vary the transconductance of a transistor over time. This variation results in the generation of the nonlinearities required to form intermodulation products.
There are two common ways to realize a transconductance mixer depending on the terminal of the transistor to which the LO is applied: the gate-pumped and the drain-pumped transconductance mixer. Only a design of the first kind will be presented in this work, therefore only a short introduction of the gate-pumped transconductance mixer will be given.
For an up-converter the two input signals, the LO and the IF, are fed to the gate of the FET and the RF gets extracted from the drain. A simplified schematic is given in Fig. 2.3.
The DC supply voltage will be fed to the drain and the gate via the matching networks. The LO matching network operates also as filter for the IF and vice versa. Hereby, a separation of the two input signals can be assured. The operating principle of a gate-pumped

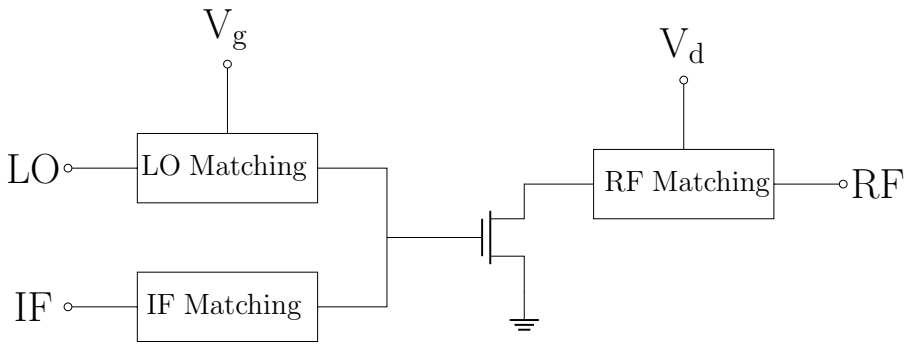


Figure 2.3.: Simplified schematic of a nonlinear gate-pumped transconductance up-converter.

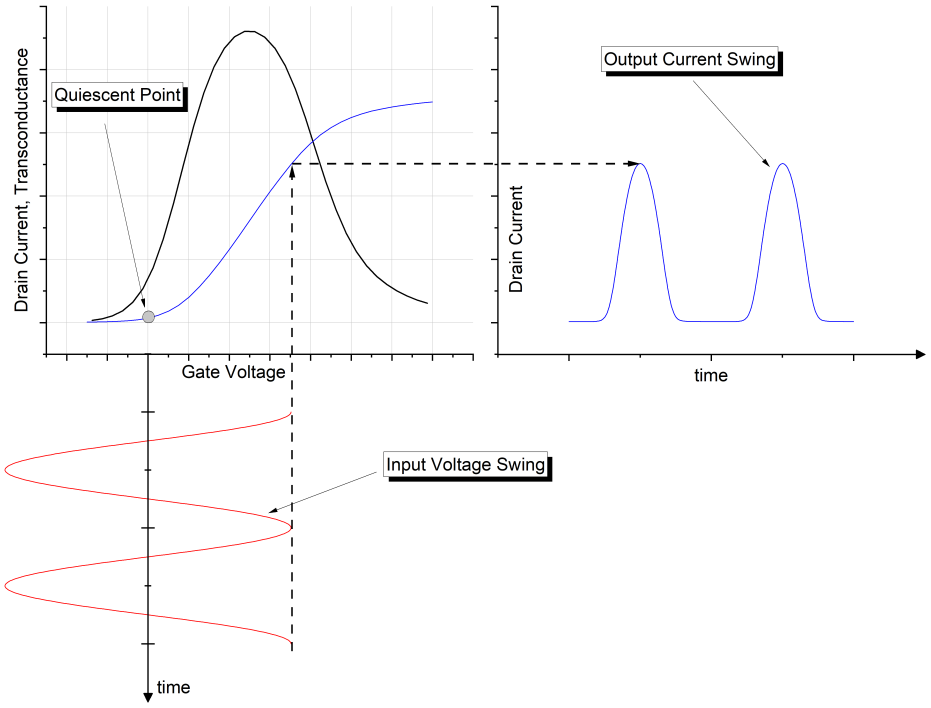


Figure 2.4.: Visualization of the underlying operating principle of the gate-pumped transconductance mixer.

transconductance mixer is depicted in Fig. 2.4.
Typically, the gate-pumped transconductance mixer is biased in a class B mode of operation. That means, the gate bias voltage is set to the transistor's threshold voltage. Applying a large sine signal (the LO) to the gate, leads to a change of the transistor's gate voltage over time. For the negative sine wave, the output current is ideally 0, since the transistor is operating below the threshold voltage. For the positive half wave of the sine, an output current is generated. The magnitude of the output current is depending on the transconductance of the device, g_m. As can be seen in Fig. 2.4, the transconductance changes with the applied gate voltage, which itself changes over time due to the LO signal. This leads to a time-dependent change of the transconductance of the device, which generates nonlinearities in the output, hence the name "nonlinear transconductance mixer".

2.1.3. Dual-Gate Mixer

Another type of active FET mixer is the dual-gate mixer which is also a transconductance mixer. Fig. 2.5 shows a simplified schematic of a dual-gate down-converter.

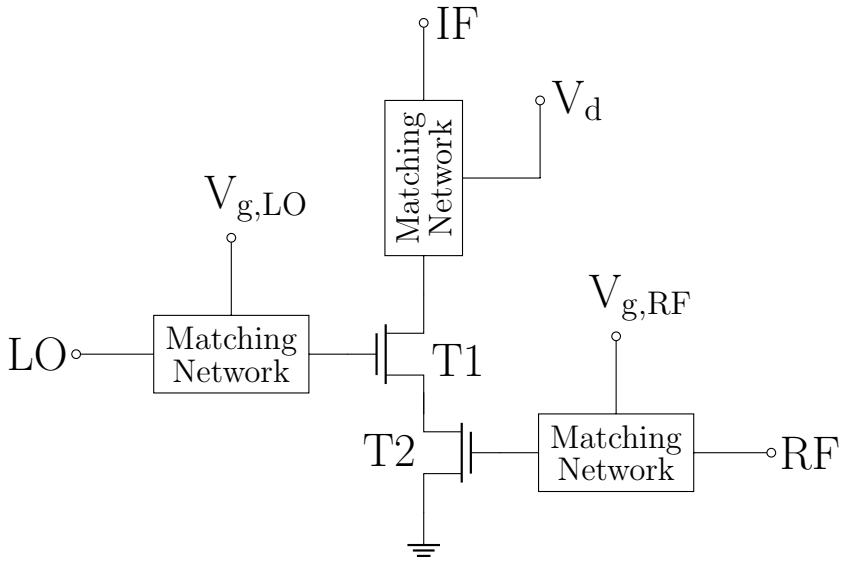


Figure 2.5.: Simplified schematic of an dual-gate down-conversion mixer.

The core of a dual-gate mixer is formed by the two transistors T1 and T2. The source of T1 is connected to the drain of T2. In case of a down-converter configuration, the IF is extracted at the drain of T1. The large signal is applied to the gate of T1 and the RF to the gate of T2. To match the input and outputs, matching networks are introduced at the ports. These matching networks can also be used to apply the bias voltages to the circuit. Since the RF and the LO are fed to separate gates, the LO-to-RF isolation of the device is better than in a single transistor architecture. This makes the dual-gate mixer suitable for applications where otherwise a balanced mixer would be needed. [Maa03]
As already mentioned, the dual-gate mixer also uses a variation of transconductance to generate harmonics and intermodulation products. The drain voltage V_d is divided between the channels of the two transistors T1 and T2: $V_d = V_{d,T1} + V_{d,T2}$. Since the large signal at the gate of the transistor T1 changes the channel resistance over time in the same way as described for resistive mixer, the drain voltage drop over T1's channel also changes over time which leads to a time dependent drain voltage variation at T2 as shown in Fig. 2.6. Fig 2.7 depicts the effect that the changing drain voltage of T2 has on the transconductance of the transistor. The transconductance describes the relationship between gate voltage and drain current of the transistor. The signal applied to the gate of T2 is the RF signal. Therefore, by modulating the transconductance of T2, also the input signal will be modulated, thus generating the desired mixing products. If the gate of T1 is biased properly, already a small change in the gate voltage, that means a small LO signal, can have a large impact on the transconductance of T2 [Maa03].

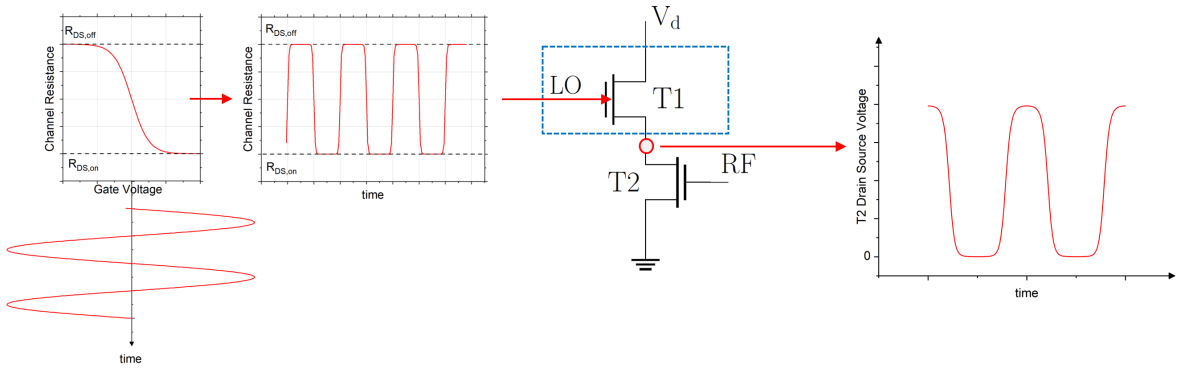


Figure 2.6.: Depiction of how a time variant large signal at T1 of the dual-gate mixer will result in a time varying drain voltage of T2.

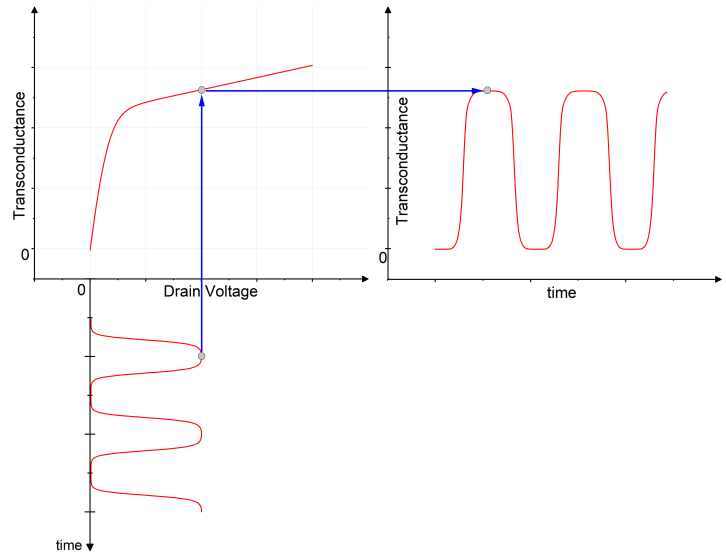


Figure 2.7.: Visualization of the influence of a time varying drain voltage on the transconductance.

2.1.4. Differential Pair and Gilbert Cell Mixer

A differential FET mixer or half Gilbert cell consists of two FETs in a differential balanced configuration. Fig. 2.8, left, shows the simplified schematic of the mixer. It is similar to the dual-gate architecture. However, due to the differential input, the LO consists of two signals with a 180° phase shift. These two signals are fed to two separate transistors: T1 and $\mathrm{T1_{diff}}$. The source of both transistors is connected. The output at the drains of T1 and $\mathrm{T1_{diff}}$ is consequently also differential. The gate of the bottom transistor, T2, is still used as port for the RF signal.

The underlying principle for mixing is to use T1 and $\mathrm{T1_{diff}}$ as switches. They are biased in a class-B mode of operation and are turned on and off by the large LO voltage swing. During the positive half-wave T1 is conducting, during the negative half-wave $\mathrm{T1_{diff}}$. Thus, during the whole duty cycle of the LO one of the transistors is always conducting and the source connection of T1 and $\mathrm{T1_{diff}}$ is a virtual ground. If the voltage swing is large enough, the transistors behave like switches with only two states: on and off. The simplified equivalent circuit is depicted in Fig. 2.8, right, where the transistors are symbolically replaced by switches. T2 on the other hand conventionally operates as an amplifier biased for maximum gain.

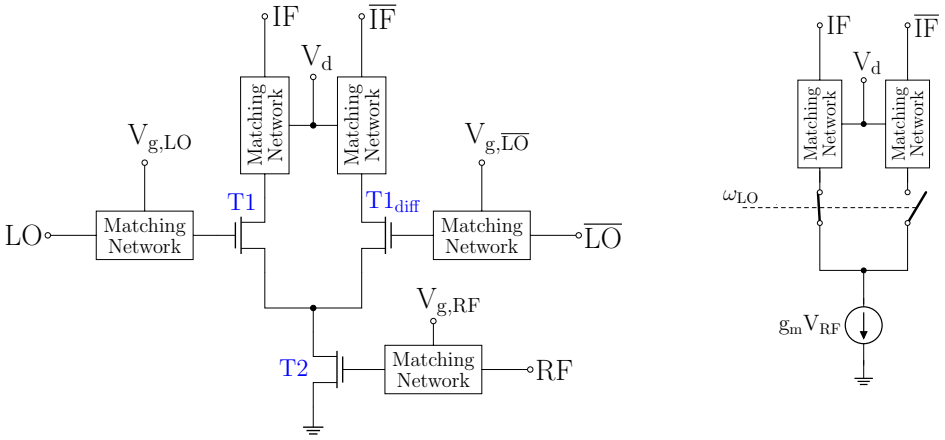


Figure 2.8.: The simplified schematic of a single balanced differential FET mixer (left) and a corresponding equivalent representation for large LO voltage swings.

Hence the output of the RF amplifier, the drain of T2, becomes modulated by the switching function of T1 and $\mathrm{T1_{diff}}$. Thereby, the intermodulation products are generated. Typical but not essential is a source degeneration or current source implemented additionally at the source of T2 [Poz05].
If two differential FET mixers are also fed with a differential RF signal, a so-called Gilbert cell mixer is created. Fig. 2.9 shows the corresponding schematic. Now it becomes clear why the differential FET mixer is sometimes also called half Gilbert cell mixer.

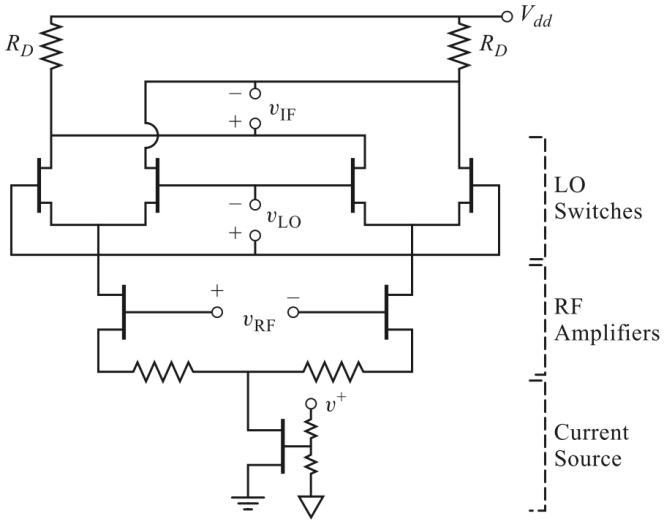


Figure 2.9.: The simplified schematic of a Gilbert cell mixer with the labeling of its main components [Poz05].

The architecture is now a double-balanced design. That means, all ports, IF, LO and RF are operated with differential signals. Hereby, the LO and the RF signal can be suppressed at the IF output. The overall operating principle is identical to the differential FET mixer. Also, included in Fig. 2.9 is the often integrated current source at the source of the RF amplifiers which can help with setting the mixer's bias [Maa03].

2.2. Frequency Converter Topologies

2.2.1. Balanced Mixers

Balancing, as for example used in the Gilbert cell architecture, is used to suppress the fundamental or unwanted intermodulation products at input and output ports of a circuit. Especially in nonlinear devices, where generation of harmonics and intermodulation products is inherent, balancing might be crucial for the functionality of the whole system. Unwanted frequency components can lead to several impairments. A selection of the most prominent ones is given below:

- Saturation of subsequent stages, like the power amplifier in a transmitter (Tx)
- Self-mixing due to an outgoing wave that gets reflected back to the mixer
- Interchannel interference in multi-channel systems due to mixing with harmonics of the LO

Conventionally, to suppress undesired intermodulation products, a destructive interference of two signals is used. For example, in-phase combining of a differential signal would lead to the extinction of that signal. However, the desired signal must not be influenced.
For this process hybrid couplers and power combiners are employed. Most commonly, components that either transform a single-ended signal to a differential one or vice versa, or, circuits, that exhibit a single-ended input and a quadrature output. Examples for the first category are Marchand baluns or rat-race couplers, for the latter one, Lange or TandemX-couplers [MBBH07].
Two possible balanced topologies will be presented in this chapter. A balanced design using two quadrature hybrid couplers and one using a 180° hybrid in combination with a power combiner. In the following the functionality of the topology is explained step by step. For this detailed analysis a closer look at the signals at certain nodes is helpful. These nodes are the input and output ports, LO, IF_1, IF_2 and RF and the nodes marked in Fig. 2.12 with the numbers 1 to 4. For an easier understanding, a three dimensional visualization of the frequency components and their phases is used. Conventionally, a pointer can be used to represent amplitude and phase of a sine or cosine signal as shown in Fig. 2.10. This can be done on a two dimensional plane, where the x-axis is the real and the y-axis is the imaginary part.

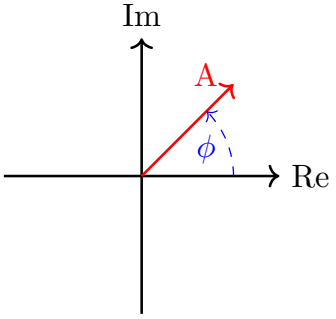


Figure 2.10.: 2D phasor representation of a sinusoidal signal.

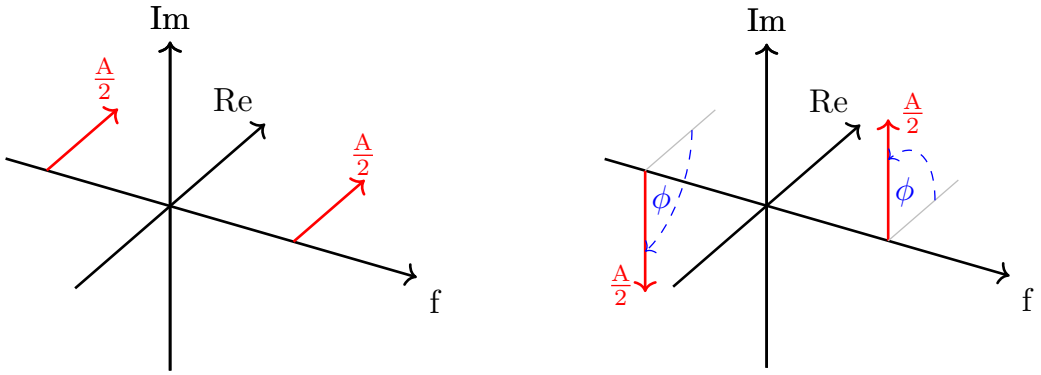


Figure 2.11.: The 3D phasor representation of a cosine (left) and the impact of a 90° phase shift (right).

But, this does not account for the frequency of the wave. Herefore, a third axis has to be added and a short mathematical detour is necessary. The underlying theory is based on Euler's identity.

$$\mathrm{e}^{\mathrm{j}\phi} = \cos(\phi) + \mathrm{j}\sin(\phi) \tag{2.1}$$

and the substitution

$$\mathrm{e}^{-\mathrm{j}\phi} = \cos(\phi) - \mathrm{j}\sin(\phi). \tag{2.2}$$

This corresponds to the phasor shown in Fig. 2.10 with an amplitude A of 1. Now, adding both these equations, the representation of a cosine is obtained:

$$\cos(\phi) = \frac{1}{2}(\mathrm{e}^{\mathrm{j}\phi} + \mathrm{e}^{-\mathrm{j}\phi}) \tag{2.3}$$

But until now, only the phase was taken into account. For the full representation, the dependency of the frequency and not only of the phase, has to be considered. Replacing ϕ with $2\pi ft + \phi$ and adding an amplitude A gives the full representation.

$$A\cos(2\pi ft + \phi) = A\frac{1}{2}(\mathrm{e}^{\mathrm{j}(2\pi ft+\phi)} + \mathrm{e}^{-\mathrm{j}(2\pi ft+\phi)}) \tag{2.4}$$

With that, a three dimensional phasor representation can be plotted. Fig. 2.11, left, shows the three-dimensional phasor representation of a cosine where $\phi = 0$. If now a phase shift is introduced, e.g. $\phi = 90°$, the cosine is transformed into a sine wave and its phasor representation is shown in Fig. 2.11, right.
The opposed rotation direction of the phasor at the positive and the negative frequency can be explained wit a closer look at Eq. 2.4. Resolving the brackets of the negative exponent $-\mathrm{j}(2\pi ft + \phi)$, leads to $-\mathrm{j}2\pi ft - \mathrm{j}\phi$. Hence, a phase shift with $\phi = 90°$ leads to phase of the negative frequency component of $-90°$, or in terms of rotation, a clockwise rotation of 90°. This phenomenon will become important in the explanations of the functionality of the topologies in the following sections.

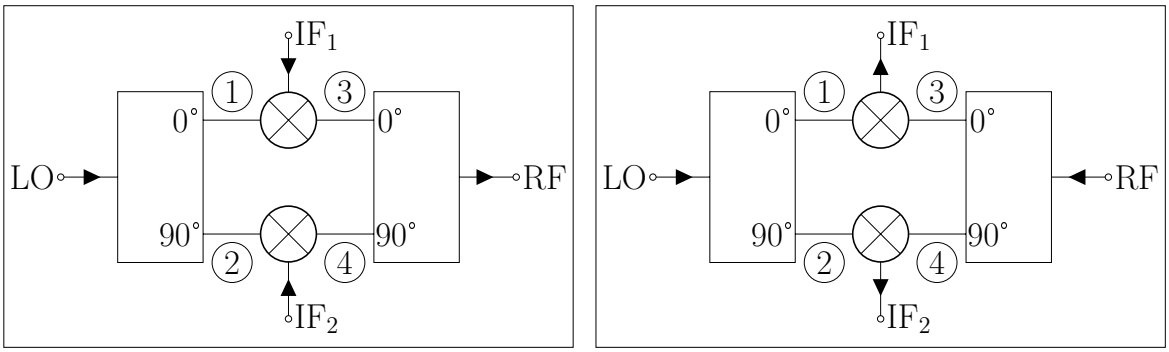


Figure 2.12.: Block diagram of a balanced up- and down-converter topology using two quadrature hybrid couplers.

2.2.1.1. Topology with two Hybrid Quadrature Couplers

Fig. 2.12 shows the block diagram of the proposed topology using two 90° hybrid couplers for balancing.
Now, for each node the frequency components and their phase can be plotted. The nodes, LO, 1 and 2, are identical for the up- and the down-converter version. If we assume, that the LO signal is a cosine, the corresponding phasor representation is the same as shown in Fig. 2.11, left. The coupler introduces a 0° and a 90° phase shift to this signal. Therefore, the signal at node 1 remains the same and at node 2, the 90° phase shift leads to counterclockwise rotation of the positive frequency component and a clockwise rotation of the negative frequency component. A visualization of the corresponding phasors for the LO, node 1 and 2 are shown in Fig. 2.13.

Up-Converter In the up-converter in the next step an IF signal is modulated onto the carrier, the LO coming from node 1 and 2, respectively. The phasor representation of IF_1 and IF_2 are depicted in Fig. 2.14.
Although the IF signal's bandwidth and shape are identical, to facilitate differentiating them, the IF_1 signal is depicted as a blue rectangle and IF_2 as a green triangle. Note, that there is

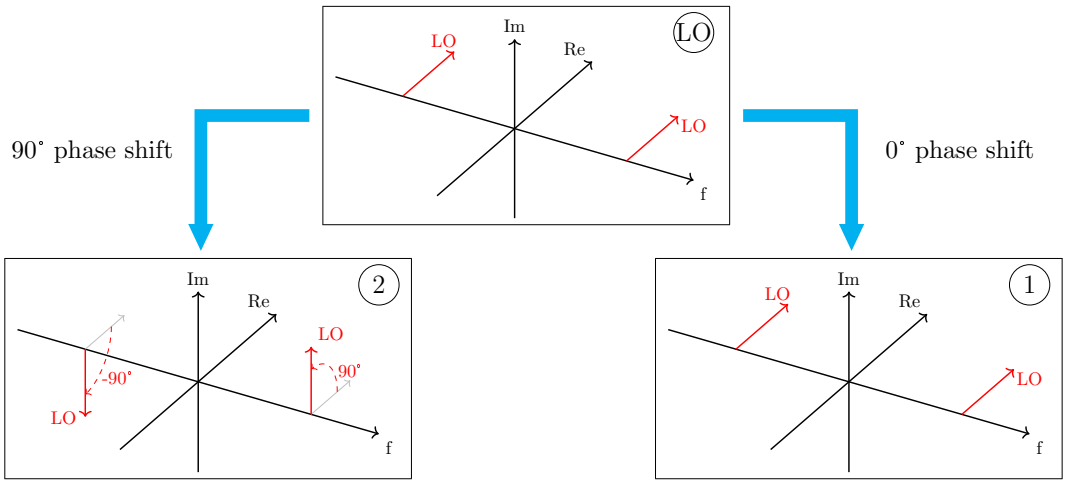


Figure 2.13.: 3D phasor representations of the signal present at the nodes LO, 1 and 2.

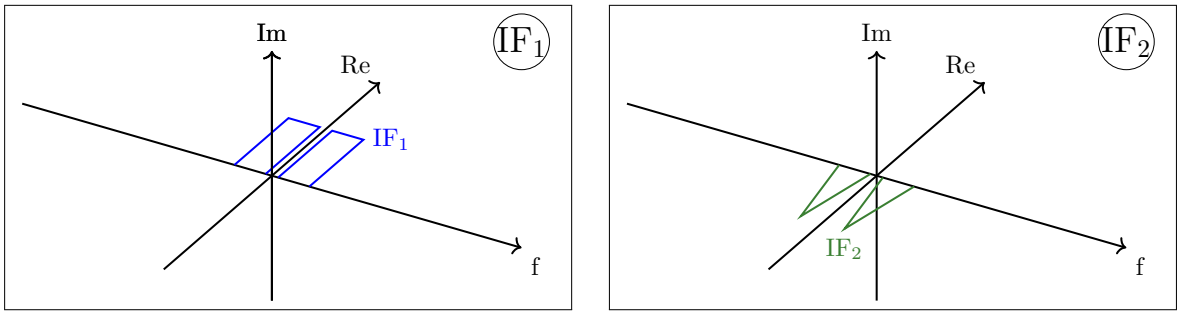


Figure 2.14.: 3D phasor representations of the input signals IF_1 and IF_2.

a phase shift of 180° between IF_1 and IF_2. This is necessary for this topology to operate properly.
Mixing the signal from node 1 and IF_1, as well as the signal at node 2 with IF_2, results in the constellation shown in Fig. 2.15.
Of course not only the desired up-converted signal $\mathrm{f_{RF}} = \mathrm{f_{IF}} + \mathrm{f_{LO}}$ will be generated, but also various intermodulation products. However, for the sake of explaining the functionality of a balanced up-converter, these unwanted intermodulation products are ignored.
When mixing, not only the frequency is summed up, but also the phase. This makes no difference for node 3, where the up-converted signal is just the baseband signal shifted in frequency. But for the signal at node 4, the phase-shifted LO leads to a phase-shifted up-converted RF signal. The negative part experiences a phase shift of -90° and the positive frequency component of +90°.
Eventually, the second 90° hybrid coupler combines both signals. Additionally, the signal coming from node 4 will be phase-shifted again by 90°. This rotates both the LO and the desired signal around the frequency axis - the components on the positive part of the frequency axis counterclockwise and the components on the negative part clockwise. Fig. 2.16 separates the combining and the phase shifting for reasons of clarity although both happen in one component. First, the phase-shifted signals are shown, then the combined signal.
Both the desired up-converted signals in RF_1 and RF_2 are in-phase. By combining them they interfere constructively. They are easily summed up. However, the LO signals coming from node 3 and 4 show a phase difference of 180° after the phase shifting. Combining these

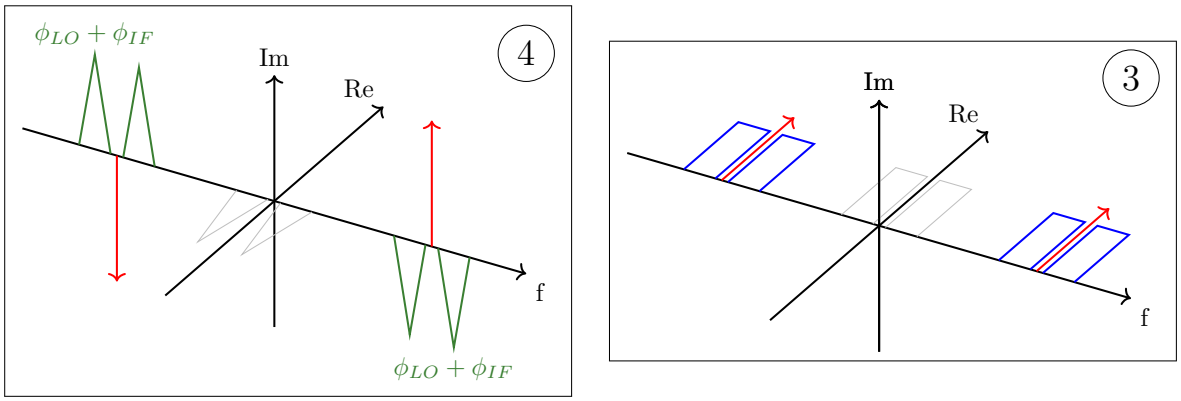


Figure 2.15.: 3D phasor representations of the signals of interest present at node 3 and 4 after mixing the signals from node 1 and 2 and the IF inputs.

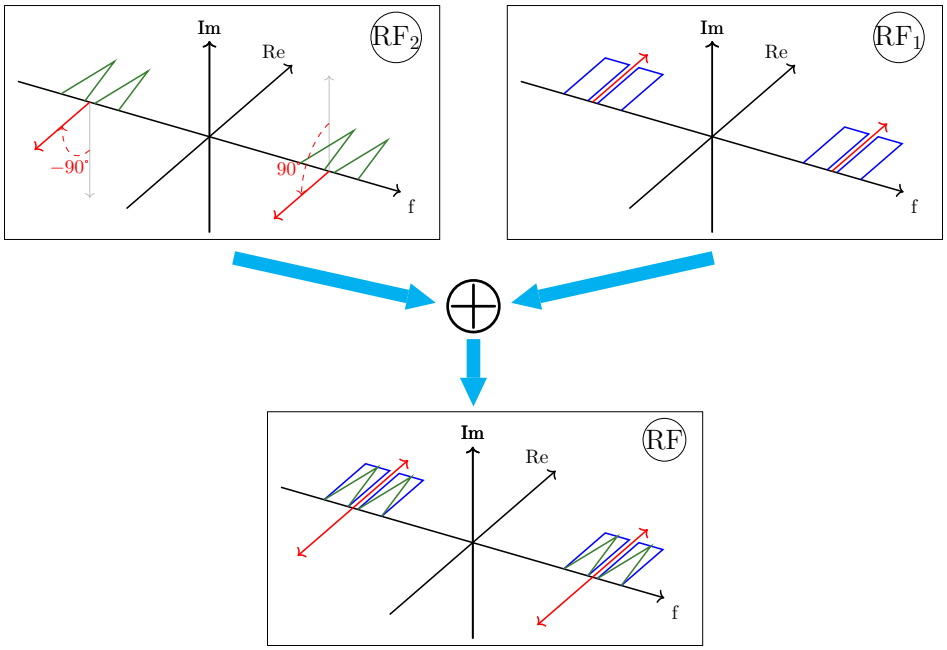


Figure 2.16.: The impact of the quadrature hybrid coupler on the signals from node 3 an 4 and the 3D phasor representation of combining them.

signals leads to a destructive interference of the LO at the output. The goal of the balanced design is accomplished: The desired signal is not influenced by the topology but the LO signal is suppressed.
One final note on the IF input signals: As mentioned, IF_1 and IF_2 exhibit a phase difference of 180°. This leads to the presented outcome. If IF_1 and IF_2 were in-phase, the up-converted signal in node 4 would be in-phase with the LO signal. In the end, this would result in the same destructive interference of the IF signals as happening to the LO signal.

Down-Converter The same way, as with the balanced up-converter, node by node, the functionality of the down-converter can be described. As already discussed, the LO input signal, as well as the signals at node 1 and 2 are identical to the down-converter. The broadband input signal at the RF port is depicted in Fig. 2.17.
This signal now gets fed to the quadrature hybrid coupler on the RF side of the down-converter. The signal is split and the two parts are phase-shifted by 0° and 90°, respectively. The signals

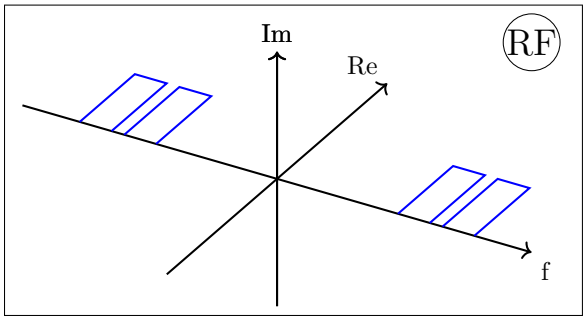


Figure 2.17.: The 3D phasor representation of the RF input signal.

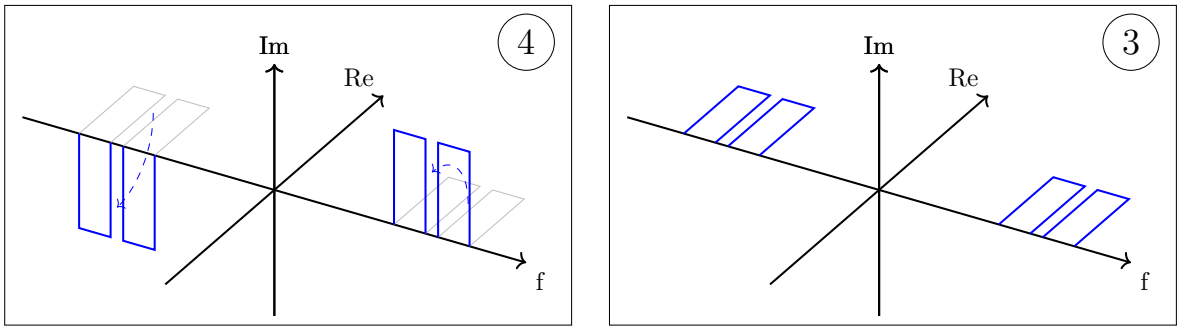


Figure 2.18.: The signals at node 3 and 4 after passing through the hybrid quadrature coupler.

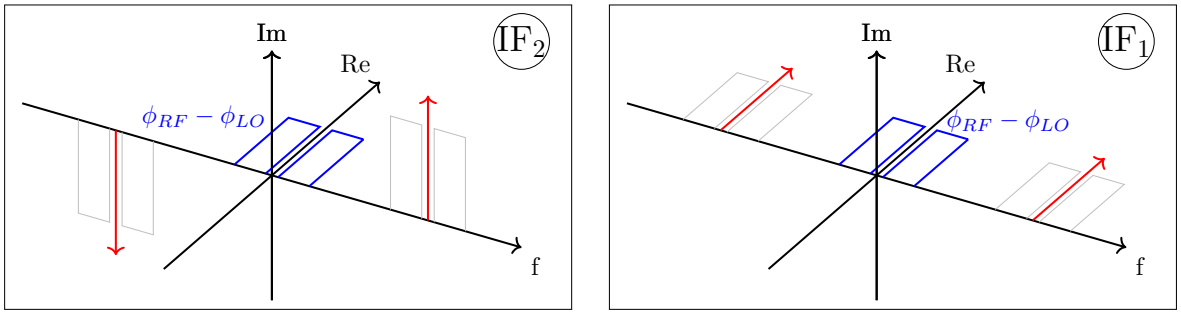


Figure 2.19.: The resulting signals at the output IF_1 and IF_2.

present at node 3 and 4 are visualized in Fig. 2.18.
Now using the LO signals at node 1 and 2, as depicted in Fig. 2.13, the signal is down-converted. Here, not only the frequency is subtracted, $\mathrm{f_{IF}} = \mathrm{f_{RF}} - \mathrm{f_{LO}}$, but also the phase: $\Phi_{\mathrm{IF}} = \Phi_{\mathrm{RF}} - \Phi_{\mathrm{LO}}$ thus leading to the phasor representation as shown in Fig. 2.19.
These two output signals can be combined without any more modification. Since the IF signals are in-phase they will interfere constructively. This represents the major difference in the design of the balanced down- and up-converter topology using two hybrid quadrature couplers: In the up-converter the IF input has to be differential whereas the output signal in the down-converter is in-phase.
Regarding the LO to RF isolation, the same transformations of the LO signal as shown for the up-converter can be applied here. That means, that the phasing of the LO for the balanced up-converter at node 3 and 4 is the same as shown in Fig. 2.15. After being applied to the quadrature hybrid coupler, it is phase-shifted in the same manner. This will result in the identical relation of the combined LO signal as presented in Fig. 2.16, thus interfering destructively. Hereby, the LO signal is suppressed at the RF input port of the balanced up-converter as well. The corresponding analytic description of the functionality of a balanced up- and- down-converter can be found in Annex A.

2.2.1.2. Topology with a 180° Hybrid Coupler and a Power Combiner

The balanced topology using a 180° hybrid coupler and a power combiner/divider can be described in the same manner. The block diagram of an up- and down-converter is shown in Fig. 2.20.

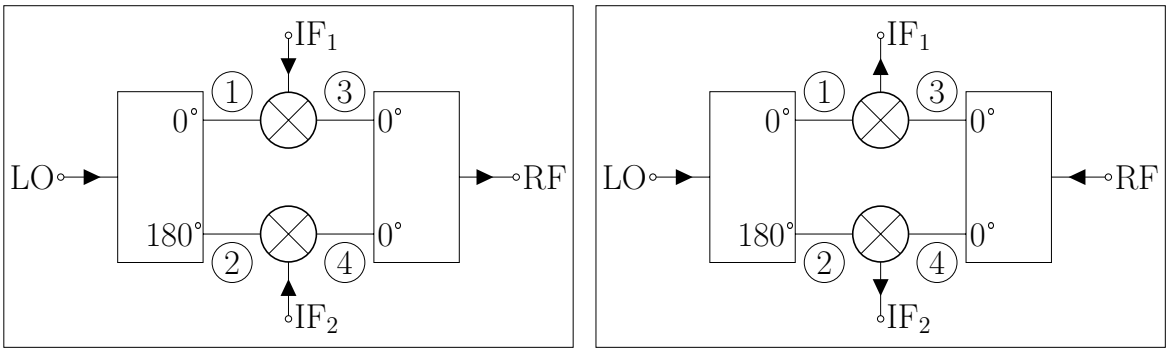


Figure 2.20.: Block diagram of a balanced up- and down-converter topology using a 180° hybrid and a power combiner/divider.

Up-Converter For the further analysis only the desired frequency components and the LO is shown. Additionally, intermodulation products will be ignored for the sake of clarity. The IF input is identical to the version with the quadrature hybrid coupler, a differential signal as shown in Fig. 2.14. IF_1 is depicted as a rectangle with a phase of 0° and IF_2 as a triangle with a phase of 180°. The complete visualization of the functionality using the phasor representation is depicted in Fig. 2.21.
Similar to the already presented version, the phasing of the LO signal at the nodes 1 and 2 are identical for both modes of operations. The cosine LO signal is fed to the balun and thereby split into two signals. The phase of the signal at node 1 is unchanged. The carrier at node 2 experiences a 180° phase shift. That leads to a rotation of the negative frequency component of $-180°$ and $+180°$ for the positive frequency component. In the next step the carrier from node 1 and 2 as well as the differential IF input signals are fed to the mixer. The up-converted desired RF signal exhibits a phase ϕ_{RF} that equals $\phi_{IF} + \phi_{LO}$. Hence, at node 3 the resulting RF phase is 0° and at node 4 $180° + 180° = 0°$. The power combiner at the output adds up the two signals to the outcome that is shown in the bottom of Fig. 2.21: The desired RF signal from node 3 and 4 are in-phase, thus interfering constructively and the LO components are 180° out-of-phase, thus interfering destructively. The LO is suppressed at the output.

Down-Converter For the down-converter version of the balanced topology employing a balun and a power splitter, the flowchart is given in Fig. 2.22. The RF input signal is a broadband double sideband signal centered around the LO frequency. The input is then fed to the power splitter. The power splitter generates two in-phase output signals, node 3 and 4. These two signals are mixed with the signals from the LO path at node 1 and 2 as depicted in Fig. 2.21. The LO exhibits a phase shift of 180° and the RF of 0°. While down-converting, not only the frequency will be subtracted but also the phase. Hence, the resulting IF signal shows a phasing of $\phi_{IF} = \phi_{RF} - \phi_{LO}$. This will lead to phasing of the desired signal at the output of IF_1 of $0° - 0° = 0°$. Correspondingly, the output signal at IF_2 has a phase of $0° - 180° = -180°$. This means, that the presented balanced down-converter topology has a differential IF output. In order to convert the output to a single-ended output, an unbal is necessary.
The LO signal will propagate from its generation at the LO node to the RF node in exactly

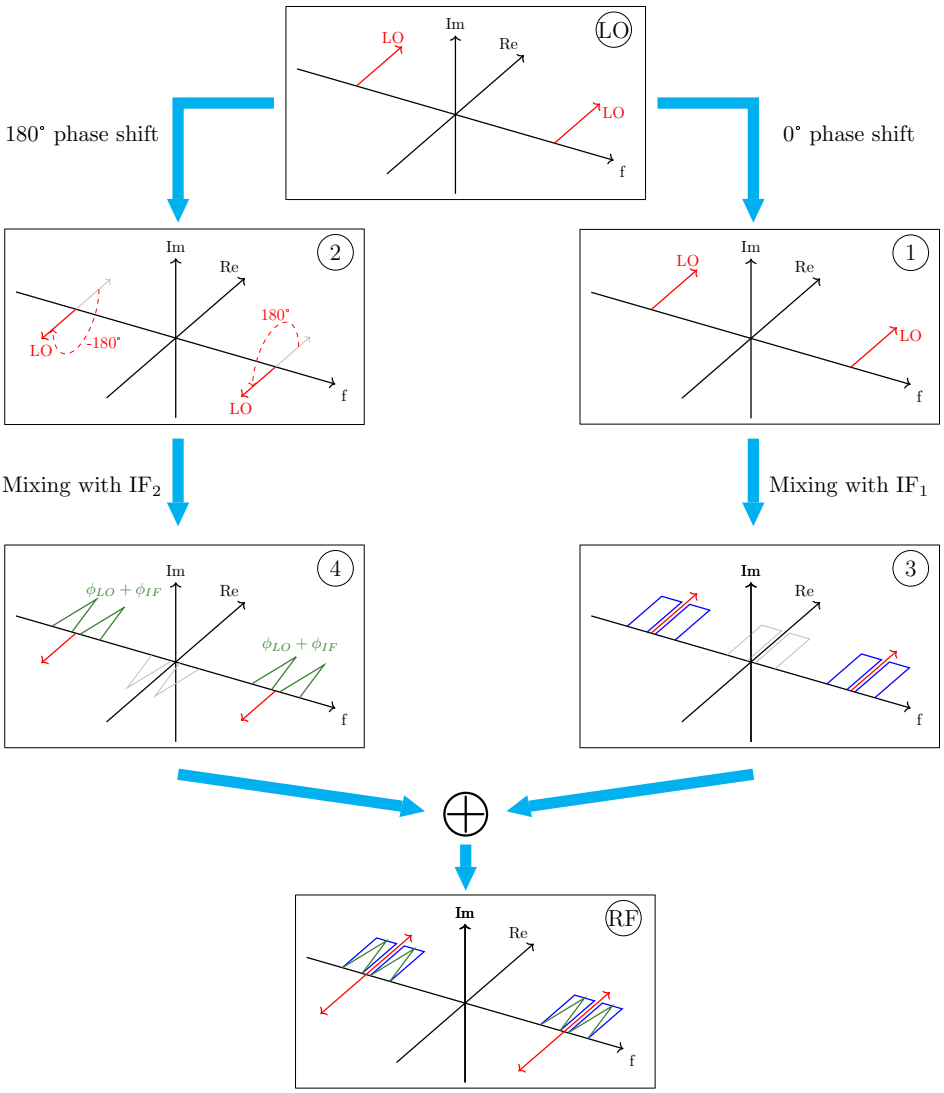


Figure 2.21.: The full chain of transformations the IF and LO input signals experience on their way to the output node RF.

the same manner as shown before in the up-converter. Hence, at the RF node it will be canceled out.

2.2.2. Quadrature Mixers

For complex modulation formats, such as phase shift keying (PSK) or quadrature amplitude modulation (QAM), the transmission requires two channels, the in-phase and the quadrature channel. These channels are combined to a single RF signal and decomposed at the receiver. Hereby, it is important, that the two channels, I and Q, do not interfere with each other and a clean separation at the receiver is feasible. Similarly to the functionality of suppressing the LO in a balanced topology, the functionality of the transmission of a quadrature signal can be explained using the graphical approach. For this purpose a simple transceiver will be used. The block diagram is shown in Fig. 2.23.
The receiver and transmitter comprise a quadrature hybrid coupler, two mixers and a power combiner/splitter. The antennas and the channel are ignored for this consideration.

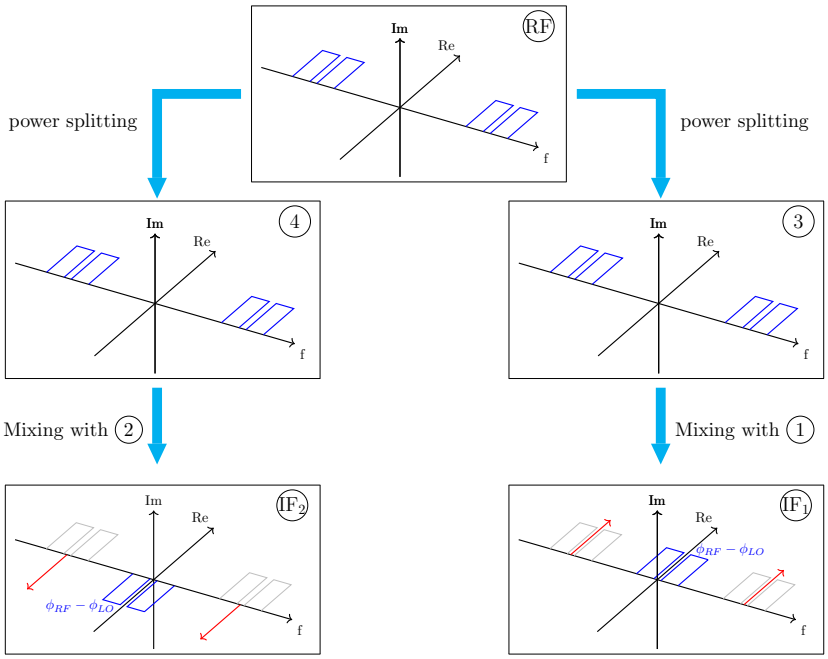


Figure 2.22.: The flowchart of a down-converter comprising a balun and a power splitter.

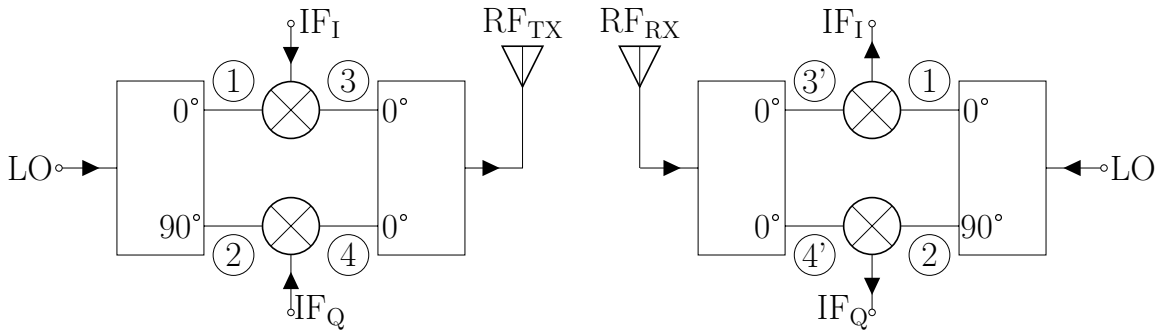


Figure 2.23.: Block diagram of a quadrature transceiver comprising a transmitter, on the left, and a receiver on the right.

Furthermore, no change in amplitude of the signals is considered, since all components are assumed to be ideal and therefore no amplitude imbalance between the paths can occur.
The LO input signal and the transformed signals at node 1 and 2 are identical for the up- and down-converter like it is shown in Fig. 2.24. The input cosine is fed to the quadrature hybrid coupler. At output 1 the signal is unchanged in terms of phase, at output 2, the positive frequency component rotates counterclockwise around the frequency axis by 90°. Correspondingly the negative part rotates clockwise which results in a phase of -90°.
The IF input signals, $\mathrm{IF_I}$ and $\mathrm{IF_Q}$, are in-phase. In Fig. 2.25, $\mathrm{IF_I}$ is depicted as blue rectangle and $\mathrm{IF_Q}$ as green triangle to help distinguishing the two signals in the course of the analysis.
The next steps from node 3 and 4, to RF, to the nodes 3' and 4' in the receiver and to the final output $\mathrm{IF_I}$ and $\mathrm{IF_Q}$ are depicted in a flow diagram in Fig. 2.26.
The IF input signals get up-converted using the LO from node 1 and 2, respectively. For node 3 this leads to no change in the phase, only in the frequency. However, $\mathrm{IF_Q}$ is phase-shifted by 90°. Again, for the negative frequencies this results in clockwise rotation and for the

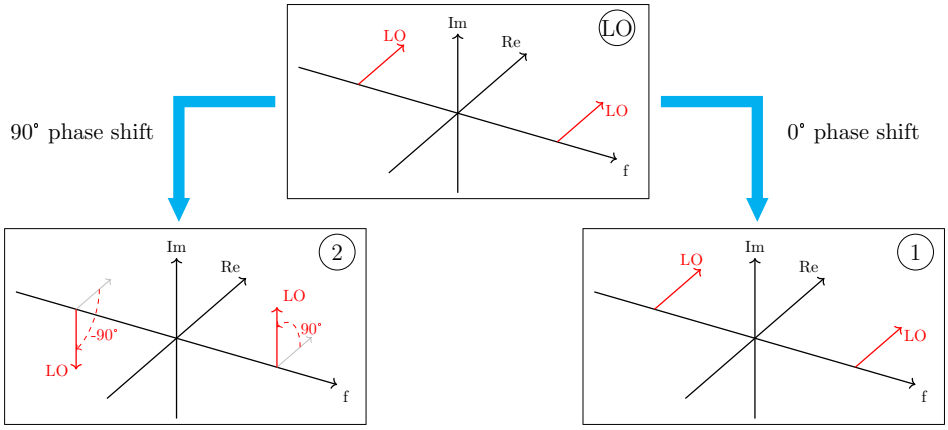


Figure 2.24.: 3D phasor representation of the LO input signal and at the nodes 1 and 2.

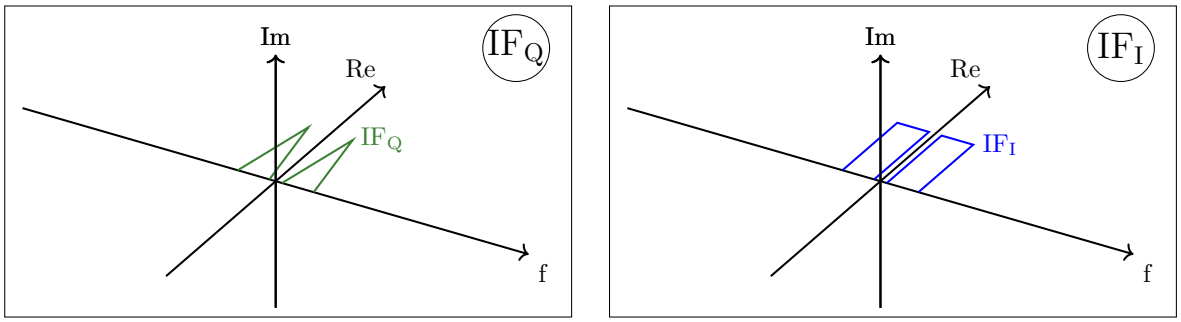


Figure 2.25.: 3D phasor representation of the IF input signals $\mathrm{IF_I}$ and $\mathrm{IF_Q}$.

positive frequencies in a counterclockwise rotation. Then, the signals are combined to a single RF signal. Here, the 90° phase shift between the signals is clearly visible, hence the name "quadrature modulation". After the signal is transmitted to the receiver, it is equally split to the nodes 3' and 4'. The signals from node 4' and 1 are fed to one of the mixers in the receiver and 5' and 2 to the other. The resulting signal at node $\mathrm{IF_I}$ is easily obtained, because neither the LO nor the RF have experienced a change in phase, meaning the down-converted phasing of the IF is identical to that at the RF. Thus, resulting in the following: The blue rectangle from the positive and the negative frequencies combine in-phase in the baseband. However, the 180° phase difference between the $\mathrm{IF_Q}$ component of the signal is maintained, leading to a destructive interference. By that, the $\mathrm{IF_Q}$ signal component is extinguished at the $\mathrm{IF_I}$ output port.
At the $\mathrm{IF_Q}$ output, phase changes have to be considered. The positive frequency components mix with the LO exhibiting a 90° phase. While down-converting, the phase of the LO is subtracted from the RF phase, thus leading to a clockwise rotation of the down-converted RF signal by 90°. On the other hand, the negative LO component shows a phase of $-90°$. Subtracting $-90°$ is equal to adding 90° to the phase of the down-converted IF signal. This leads to a counterclockwise rotation by 90°. Both $\mathrm{IF_Q}$ components are in-phase with no imaginary part. However, the $\mathrm{IF_I}$ components are 180° out of phase, thus interfering destructively and vanishing at the output port of $\mathrm{IF_Q}$.
By that, the input $\mathrm{IF_I}$ and $\mathrm{IF_Q}$ signals are completely recovered at the corresponding outputs of the receiver.

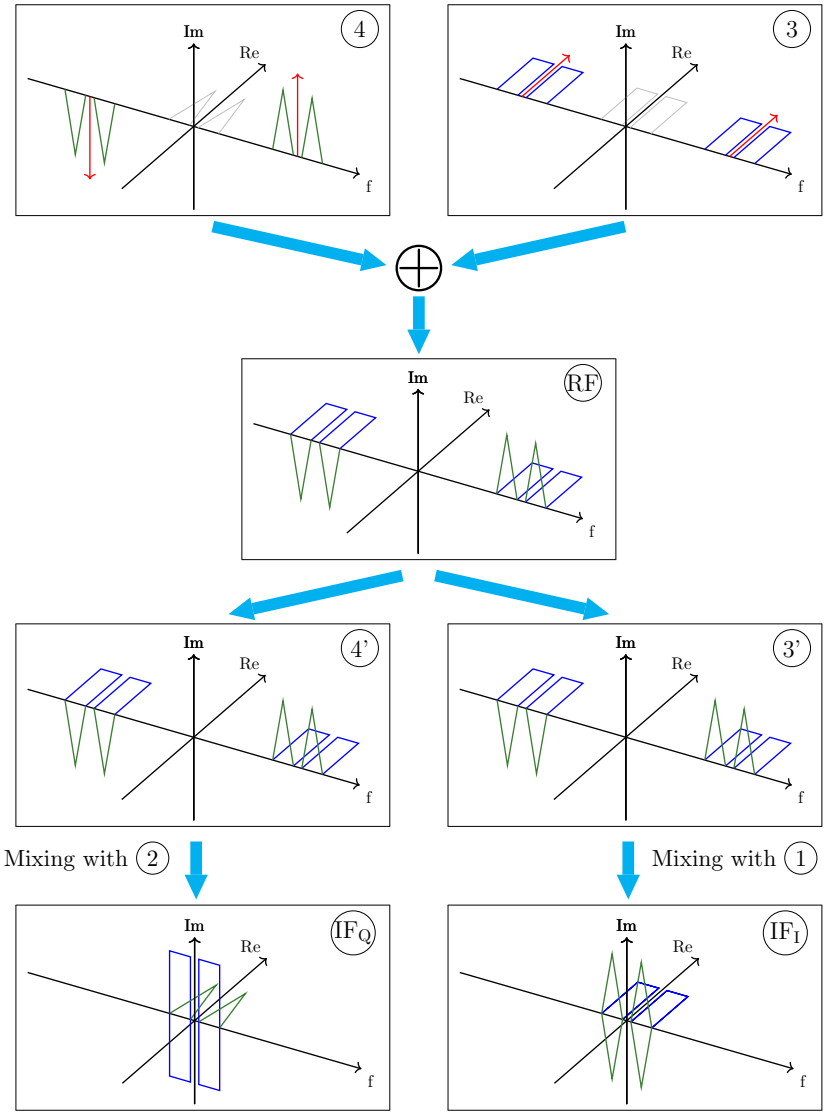


Figure 2.26.: The flowchart for the quadrature signal transmission link as depicted in Fig. 2.23 starting with the up-converted signals at node 3 and 4.

Of course, in reality, components exhibit phase and amplitude imbalances. If these are considered, there will be a leakage from the I- into the Q-channel and vice versa. Therefore, power combiners and splitters and especially couplers and baluns have to be designed carefully to obtain a result as close as possible to the presented desired outcome.

3. Simulation Techniques for Nonlinear Circuits

Simulation techniques of nonlinear circuits have been described and the theory behind it analyzed in-depth in countless textbooks like [Poz05, Mar06, Ell08, Maa03, GB03]. The purpose of this chapter is not to contribute to this canon but to add additional practical approaches for three problems a MMIC designer has to overcome: matching, load and source pull analysis and stability simulations. For the last one a new approach will be presented and the underlying theory explained in detail.

3.1. Matching

[Ell08] states that "for large-signal circuits, impedance matching is often performed by small-signal simulations in a bias point representing average characteristics. The reasons are as follows: small-signal simulations are much faster, the impedance matching is still reasonably accurate and the results can be conveniently visualized in the Smith chart."
For a power amplifier that is driven slightly in compression, this statement might be true. However, regarding nonlinear circuits, like frequency multipliers and converters which are not functional without being driven by a large signal and making use of its nonlinearity, there might be the need to reevaluate this statement.
To give an example: In the plot, Fig. 3.1, a simulation of the matching of a frequency multiplier-by-three is shown which will be presented in more detail in chapter 6.2. It was simulated both under a small and a large driving signal. The small-signal curve deviates clearly from the large signal. Therefore, in order to properly design a nonlinear circuit, the matching has to be carefully simulated under true operating conditions and an approximation by small-signal simulations is not sufficient.

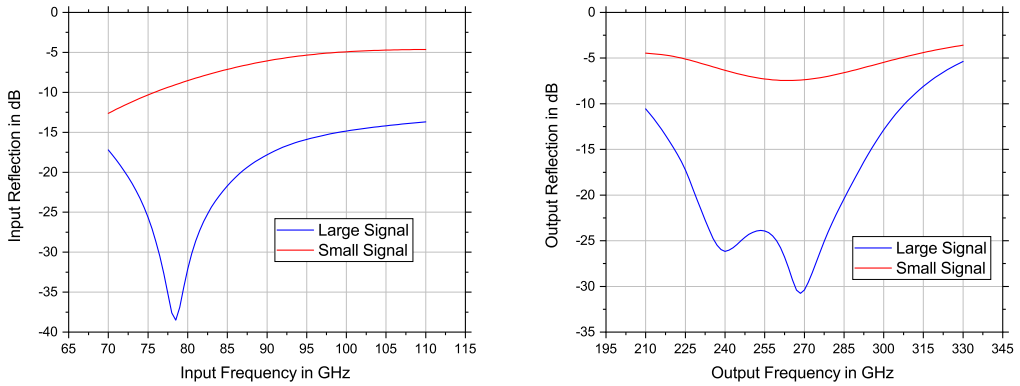
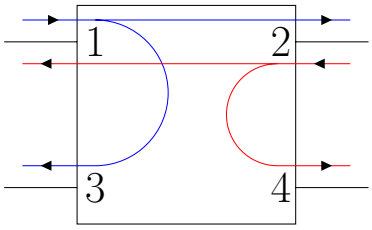


Figure 3.1.: Simulations of the input (left) and output matching (right) of a frequency H-band tripler driven by a small (red) and large signal (blue).



$$S = \begin{pmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \tag{3.1}$$

Figure 3.2.: Block diagram of the equation-based S-parameter block (left) used as ideal coupler with its S-parameter matrix (right).

The large-signal evaluation of the matching is similar to a measurement using a network analyzer. For the evaluation of the matching under large-signal excitation a harmonic balance simulator and an ideal 4-port coupler is employed. This ideal coupler is described by an equation-based S-parameter block that is available in the ADS components library [Key19]. Fig. 3.2 shows a visualization of the the equation-based S-parameter block and the corresponding S-parameter matrix. It should be noted that this coupler is not physically realizable, since it violates the energy-conservation principle. It is employed only for simulation purposes in the large-signal circuit analysis.
Port 1 is connected to a probing source and port 2 to the circuit. The signal excited at port 1 is transmitted identically to port 2 and port 3. After leaving port 2 the probing signal is fed to the circuit. In case of a mismatch, a fraction of the signal gets reflected. This reflected signal enters port 2 and gets transmitted to port 1. But at the same time, the same signal is copied to port 4. When the two output signals at port 4 and port 3 are now set in relation, $P4/P3$, the result is the corresponding input reflection coefficient.
For the port where the large signal is applied e.g. the LO port of a mixer, the large signal can be used to evaluate the incident and the reflected wave. At other ports a test signal has to be generated. It has to be small enough to avoid influencing the system, but large enough to prevent errors due to the numeric nature of the simulator. Furthermore, it must not be identical with the large signal or one of its harmonics, otherwise the reflected wave might be a superposition of the large signal and the probing signal. Fig. 3.3 shows a schematic of the principle for clarification. Here, a mixer is the device under test (DuT). The large signal is the LO. The ideal coupler is connected to either the RF or the IF port. Therefore, the DuT is driven by the large signal and is operating under real conditions. The probing

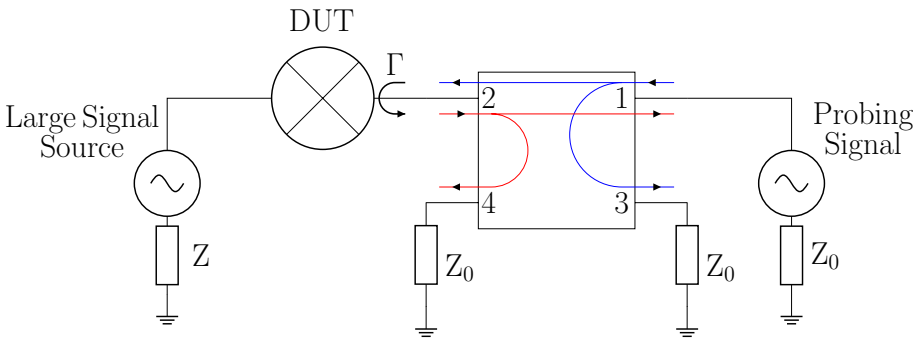


Figure 3.3.: Exemplary usage of the equation-based S-parameter block to simulate the reflection coefficient of a mixer under large-signal operation.

signal can be swept over the desired RF or IF range. To evaluate the proper reflection coefficient it is important, that the impedances of the signal source for the probing signal, the reference impedance for the S-parameter block and the termination impedances at port 3 and 4 are matched. Typically, they are 50 Ω. But, if the output port needs to be matched to a different impedance, this has to be accounted for to avoid distorting the result by introducing additional reflections.

3.2. Load/Source-Pull

Load pulling describes the technique to evaluate the performance of a device, such as an amplifier, while sweeping the load connected to the output of the device. The results are gain or output power values in dependency of a load impedance. If these values are plotted on a Smith chart, contours of equal gain or output power are created. Using this graphical approach, the designer can then chose the impedance with the best trade-off of output power versus gain. Especially in amplifier design, load pulling is performed primarily at the fundamental frequency. But regarding frequency multipliers and mixers, harmonics and intermodulation products are of more interest than the fundamental tone. Not only it is important to know, what is the optimum load impedance at the desired output frequency, but also, what is the influence of the termination at the harmonics. For example, conventionally, unwanted harmonics in a frequency multiplier are shorted. But, might it improve the device's performance if a different impedance is presented to the harmonic instead of a short? Therefore, in this chapter an accessible approach to a load pull analysis also suitable for strongly nonlinear devices is presented. The underlying idea is visualized in Fig. 3.4.
The output signal is filtered for the frequency components of interest. The filters are ideal, reflection free brick-wall filters, that present a short to one single frequency and an open for all other. Hereby, a distinguished load can be presented to a single particular frequency component. Frequencies of interest can be for example harmonics of the input frequencies or potential intermodulation products. This approach was presented in [1], where the filters were realized by equation-based S-parameter blocks, like the ones used in the previous section.
However, instead of a complex load, where a real and an imaginary part has to be swept from

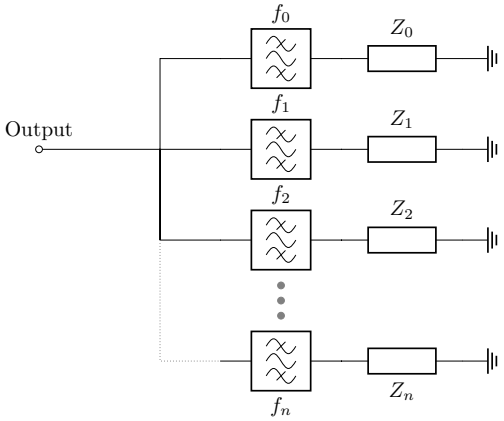


Figure 3.4.: The concept of a frequency-dependent load pull analysis illustrated by using ideal filters and load impedances.

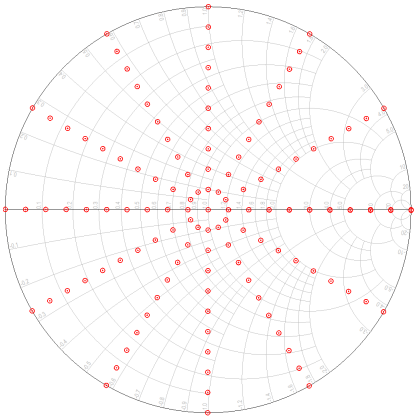


Figure 3.5.: Exemplary map of complex loads used for load pulling on a Smith chart.

0 to $+\infty$ and $-\infty$ to $+\infty$, from a simulation perspective, it is easier to work with reflection coefficients. Here the amplitude sweep will take values from 0 to 1 and the phase from 0° to 180° which is easier to setup. Also, the visualization of the load values is more accessible for an RF engineer by using a Smith chart. An example of that is shown in Fig. 3.5. Here, the phase was swept in eight steps and the amplitude in ten steps.
The most elegant way to perform the load pull analysis is to combine the filters and the loads in one component, an equation-based load. This is possible in Keysight's ADS with a 1-port equation-based S-parameter block. In this block the frequency dependence can be defined by using simple if-statements. By that, a separate load can be assigned to each frequency component. The principle is depicted in Fig. 3.6.

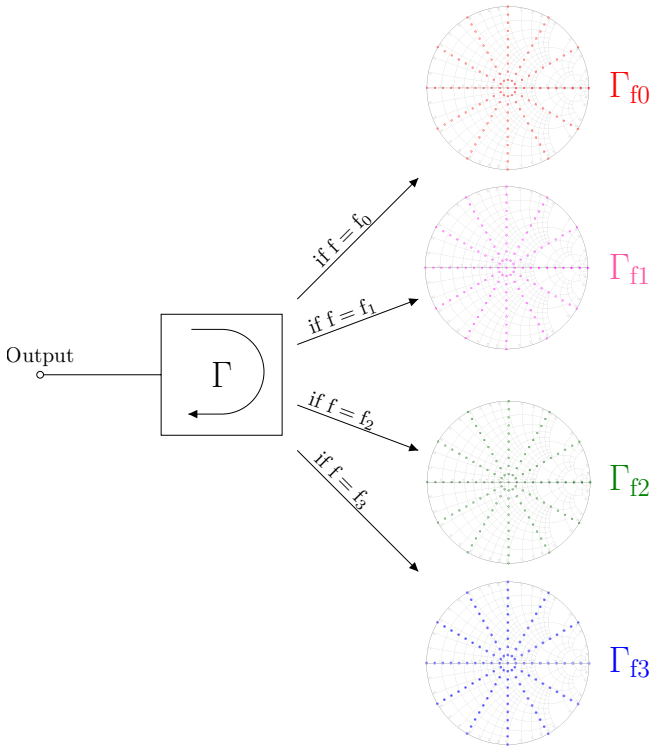


Figure 3.6.: Visualization of the load pull concept with an equation-based S-parameter block.

3.3. Stability

Instability has been and is still a major issue for a microwave circuit designer. All the effort that is put in properly composing a circuit regarding bandwidth, gain, linearity etc. can be negated by an occurring oscillation or instability. Hence, the assessment of stability is a crucial step in the process of creating a functioning component.
There are several well-known techniques to check the stability of a circuit, e.g. the Rollet stability criteria, the μ-test or graphical approaches using stability circles [Poz05]. All these approaches have in common that they only assess external stability. External stability exclusively extracts information from the ports of the device, hence the interface between the circuit and the external world. These techniques do not consider instabilities that occur inside the circuit, which might be invisible from the in- and output ports.
Internal stability on the other hand does not reduce the circuit to a N-port, where the stability is assessed from the outside but also takes into account the possibility of feedback loops in the inner circuitry and therefore presents a more holistic challenge. A method to determine the stability of a closed-loop system is the semi-graphical Nyquist criterion, where the system's behavior in dependency of frequency is investigated by drawing a plot which shows the real and imaginary part of the loop transfer function $L(j\omega)$ as ω varies from $-\infty$ to ∞. The Nyquist criterion offers several advantages like providing not only the absolute stability but also a degree of stability in form of phase and gain margins [GK09]. We define the closed-loop transfer function of a general system as depicted in Fig. 3.7 as

$$M(s) = \frac{G(s)}{1 - G(s)H(s)}. \tag{3.2}$$

where $G(s)$ is the open loop and $H(s)$ the feedback transfer function with $s = \sigma + j\omega$.
The denominator can be written as

$$\Delta(s) = 1 - G(s)H(s) = 1 - L(s) \tag{3.3}$$

where $L(s)$ is the loop transfer function. The zeros of $\Delta(s)$ are the poles of $M(s)$. Following Nyquist's definition of stability, a system is closed-loop stable if the poles of the closed-loop transfer function thus the zeros of $\Delta(s)$ are all in the left-half s-plane. $\Delta(s) = 0$ when $L(s) = (1, j0)$ therefore $(1, j0)$ in the $L(s)$-plane is called the critical point for closed-loop stability.
The number of encirclements, N, of the critical point by $L(s)$ gives the difference between the number of zeros, Z, and poles, P, of $\Delta(s)$ in the right-half s-plane:

$$N = Z - P \tag{3.4}$$

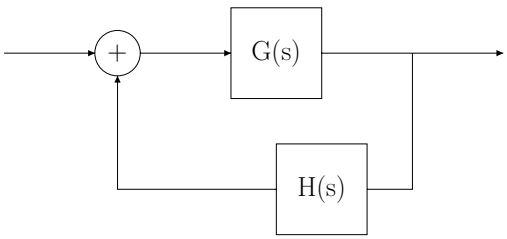


Figure 3.7.: Block diagram of a general feedback system.

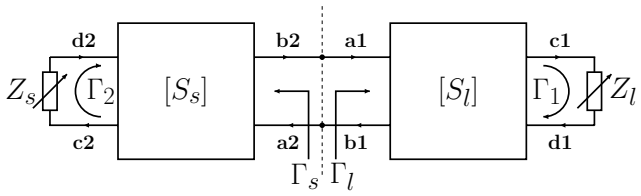


Figure 3.8.: General representation of a circuit by two 2-ports with termination impedances using incident and reflected power waves.

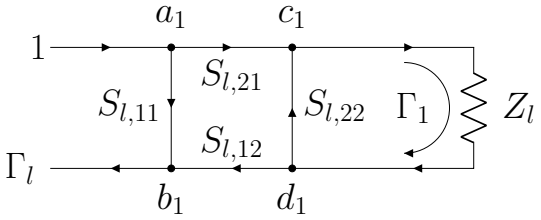


Figure 3.9.: Signal flow diagram of a 2-port with a termination impedance Z_l.

As stated before, for closed-loop stability the number of zeros of $\Delta(s)$ must equal zero leading to the condition:

$$N = -P \tag{3.5}$$

The total number of encirclements is counted as follows: Each encirclement in clockwise (CW) direction increases the number of encirclements by 1. Each encirclement in counter-clockwise (CCW) direction decreases the total number by 1.
That means, a closed-loop system is unstable when $L(s)$ encircles the critical point more often in clockwise direction than in counter-clockwise direction going from $-\infty$ to ∞. For a given transfer function of a system it is easy to determine stability by using the Nyquist criterion and counting the clockwise and counterclockwise encirclements of a critical point (typically $(1, j0)$). However in the high frequency domain it is not always easy to transform a multi-stage circuit into the form of a closed-loop feedback system. The purpose of the following discussion is to present such an approach and its implementation in a circuit simulation environment.

3.3.1. Theory

3.3.1.1. Simplified Feedback Network

In a conventional approach to check for internal stability an arbitrary point in the circuit is chosen. Herefore in the first approximation the circuit is divided into two parts, which can be represented by general 2-port networks, characterized by their scattering matrices, S_s and S_l, with arbitrary passive termination impedances, Z_s and Z_l. A depiction of the 2-port networks in terms of incident and reflected power waves is illustrated in Fig. 3.8.
If we translate the right half, the load side, of this network into a signal flow graph, fed at the probing point, this results in Fig. 3.9. From that we can calculate the reflection coefficient Γ_l:

$$\Gamma_l = \frac{b_1}{a_1} = S_{l,11} + \frac{S_{l,21}S_{l,12}\Gamma_1}{1 - S_{l,22}\Gamma_1} \tag{3.6}$$

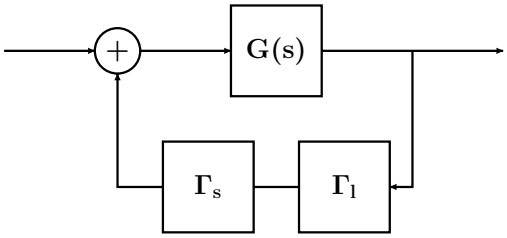


Figure 3.10.: Block diagram of a feedback system with the open loop transfer function $G(s)$ and the feedback transfer function consisting of Γ_l and Γ_s.

The left side, the source side, of the network translates the same way to a signal flow graph where Z_l is exchanged by the source impedance Z_s. The calculation of Γ_s can then be done similarly.

$$\Gamma_s = \frac{b_2}{a_2} = S_{s,11} + \frac{S_{s,21}S_{s,12}\Gamma_2}{1 - S_{s,22}\Gamma_2} \tag{3.7}$$

It is important to note that Γ_s is not considered when evaluating Γ_l since there is no source termination [Ell08] and vice versa for Γ_s.
Since at the probing point both 2-port networks are ideally connected, the reflected wave of $[S_l]$ characterized by Γ_l represents the incident wave, a_2, for the network $[S_s]$. After passing S_s a fraction, characterized by Γ_s, will again be reflected to the probing point, thus closing the loop. Fig. 3.10 shows this behavior translated into a system block diagram.
$G(s)$ is the open loop transfer function with $s = \sigma + j\omega$ and represents the transition from one 2-port network to the other. It is ideal, therefore $G(s) = 1$. The two function blocks with the reflection coefficients Γ_l and Γ_s stand for the feedback transfer function $H(s)$ leading to $H(s) = \Gamma_l\Gamma_s$. Knowing $H(s)$ and $G(s)$ we can define the characteristic equation of the system as

$$\Delta(s) = 1 - G(s)H(s) = 1 - \Gamma_l\Gamma_s. \tag{3.8}$$

After establishing the transfer function for the system, it is necessary to find a way to determine the reflection coefficients Γ_l and Γ_s.

3.3.1.2. Extended Feedback Network

In the described approach the probing point is the only connection between the two S-parameter blocks. This applies only to a limited amount of cases. For example a typical power amplifier may use parallelisation of stages to increase output power and linearity. In this case more than one feedback loop exists. Furthermore in integrated circuits bias paths of several stages are combined to reduce the number of ports for bias connections and the number of external voltage sources. Especially low frequencies tend to travel along theses bias networks which creates another feedback loop. To give a general statement on stability not only the feedback loop formed by reflections at source or load but also all other paths have to be considered.
A more accurate representation of the circuit with an additional feedback loop ($e1$ to $f2$) is therefore shown in Fig. 3.11 which can be expanded for an arbitrary number of feedbacks by extending the 3-ports to N-ports and connecting the corresponding input and output paths between the n-port blocks.

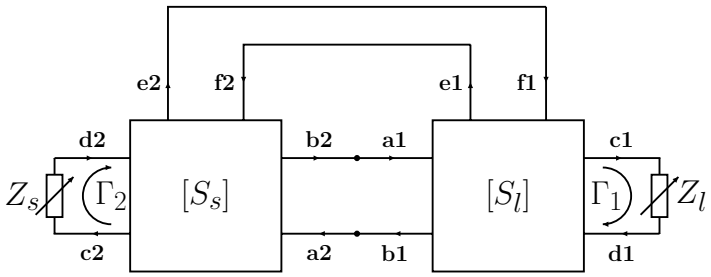


Figure 3.11.: General representation of the circuit with termination impedances and a feedback and feed-forward path using incident and reflected power waves.

Note that besides the new feedback path a forward feed is also formed by the path $e2$ to $f1$ and has to be taken into account when evaluating stability.

3.3.2. State of the Art

Eq. 3.8 is well-known especially in oscillator design where it is used to determine whether the condition for steady-state oscillation, $\Gamma_l\Gamma_s = 1$, is satisfied [EH81]. This feature is already implemented in CAD software, e.g. the "SProbe2" in Keysight's ADS [Key19] or "GPROBE2" in AWR's Microwave Office [Nat19]. Also, it was suggested for stability considerations of oscillators by [Jac92] which is still cited in more recent publications like [Maa14]. The probe is inserted into the circuit and determines the small-signal impedances looking in both directions using a S-parameter simulation. From the impedances the reflection coefficients can be calculated:

$$\Gamma_l = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{3.9}$$

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{3.10}$$

where Z_0 is an internal reference impedance by default set to 50 Ω. For an active 2-port the impedance will be negative and therefore the reflection coefficient larger than 1. In the internal calculations of the" SProbe2" a so-called "stability index" is computed: $\mathrm{StabIndex} = \mathrm{Re}(\Gamma_l\Gamma_s)$
This corresponds to the real part of $L(s)$. But introducing a reference impedance, Z_0, results in a strong dependence of $L(s)$ on the value of Z_0.
Only in case of oscillation, $\Gamma_l\Gamma_s = 1$, the result is independent of Z_0 as can be easily shown:

$$\Gamma_l\Gamma_s = 1 \tag{3.11}$$

$$\frac{Z_l - Z_0}{Z_l + Z_0}\frac{Z_s - Z_0}{Z_s + Z_0} = 1 \tag{3.12}$$

$$Z_lZ_s - Z_lZ_0 - Z_sZ_0 + Z_0^2 = Z_lZ_s + Z_lZ_0 + Z_sZ_0 + Z_0^2 \tag{3.13}$$

$$Z_l + Z_s = 0 \tag{3.14}$$

To assess stability the stability index is not suitable. To take only the real part into account is wrong as is the often quoted condition for oscillation buildup $|\Gamma_s(\omega_0) \cdot (\Gamma_l(\omega_0))| > 1$. The shortcomings of the latter are described in detail in [GB03]. For the stability index the

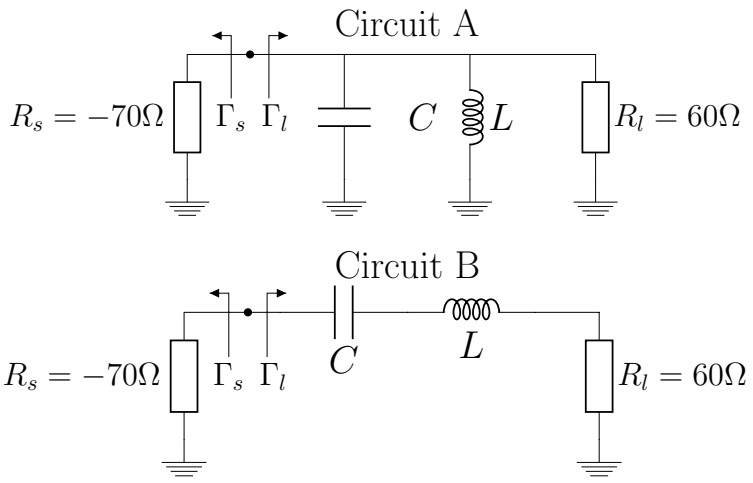


Figure 3.12.: Two simple, ideal circuits adapted from [Jac92] to prove the Nyquist stability criterion.

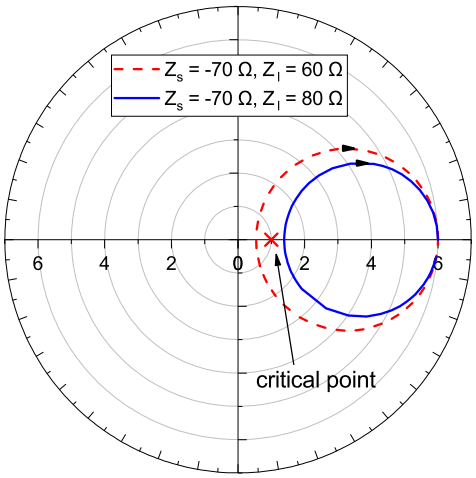


Figure 3.13.: Nyquist plot of the stable (blue, solid) and unstable (red, dashed) version of circuit B.

argumentation is similar as can be shown using the cases presented in [Jac92].
The circuits used to exemplify the dependency on the normalizing impedance are a serial and a parallel resonator, depicted in Fig. 3.12, both connected to an active part, represented by a negative resistance R_s. In case of the serial resonator the circuit is unstable, in case of the parallel resonator the circuit is stable. To stabilize the serial circuit, Circuit B, the load resistance can be changed to be larger than 70 Ω, e.g 80 Ω.
The resulting Nyquist plot is shown in Fig. 3.13. The real part of the Nyquist plot of the stabilized circuit is always larger than 1. Following the "stability index" criterion for stability, $\mathrm{Re}(\Gamma_l\Gamma_S) > 1$, this indicates instability. That however is wrong. The graphical Nyquist criterion with $\mathrm{L} = \Gamma_\mathrm{l}\Gamma_\mathrm{S}$ proves to work fine for the cases as presented in [Jac92]. For the stable circuits no encirclement of the critical point takes place. However because of the dependence on Z_0, only an absolute statement on stability can be given, but no gain or phase margin. Therefore for theses cases it is only possible to distinguish between stable and unstable but it is impossible to quantify the stability to make it comparable.

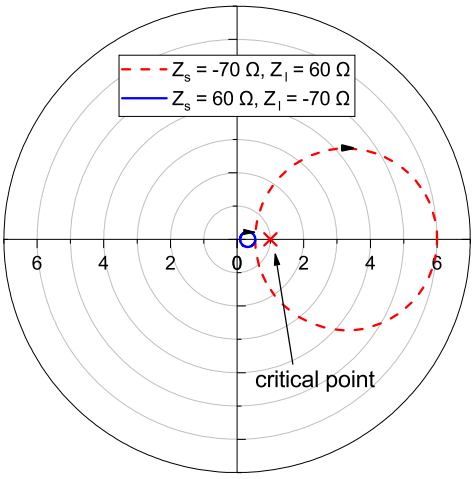


Figure 3.14.: The Nyquist plot for circuit B when source and load are exchanged, plotted in the real and imaginary plane.

3.3.3. Shortcomings of the Conventional Approach

In the presented cases the probing point is always chosen right behind the negative resistance which is the ideal case. If we change the probing point to the position behind the resonator, we get very different results. A simple example: In case the probe is located in front of the load, R_l, and the load is matched to the reference impedance of the probe, $Z_l = Z_0^*$, the reflection at the load is always 0. Therefore for each frequency the stability index will be 0, always indicating stability independent of the overall configuration of the circuit. This is obviously not true.
Another example can be derived from Fig. 3.12. Circuit B is instable. If the source and the load are exchanged, the simulation result changes, too. The circuit is now indicated to be stable although the same circuit components were used. The simulation results for both cases are shown in Fig. 3.14.
In modern professional design kits the active device i.e. the transistor is often an encrypted device and no information of the components included in the model are available. Without the knowledge of the inner circuitry of the active device, for example parasitic capacitances or inductances, surrounding the gain-producing negative resistance (e.g. the transconductance), the result of the stability simulation might be faulty.
If multiple active devices are present in form of impedances with a negative real part the statement of stability is dependent on the chosen probe impedance. For example if instead of $60\,\Omega$ in circuit B the load impedance is $-60\,\Omega$ it can be shown that the simulation indicates stability for $\mathrm{Z}_0 = 30\,\Omega$ and instability for $\mathrm{Z}_0 = 100\,\Omega$ as illustrated in Fig. 3.15. This can lead to problems when investigating devices with parallel active stages like a power amplifier.

3.3.4. Eliminating the Dependency on the Reference Impedance

To improve the statement of stability the dependence on the arbitrary internal reference impedance must be avoided. The question to be answered is: What source impedance instead of the conventional $50\,\Omega$ has to be chosen to excite the right side respectively the left side of the circuit for proper stability analysis? To achieve this, the circuit representation of Fig. 3.8 and, for more complex networks, Fig. 3.11 plays an important role. We can assume that

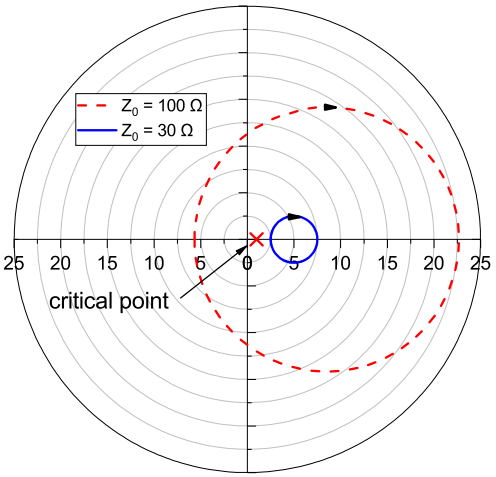


Figure 3.15.: The Nyquist plot for circuit B when source and load are arbitrary negative impedances, plotted in the real and imaginary plane for two different reference impedances, 30 Ω and 100 Ω.

for the right side part of the circuit the output impedance of the left side part represents a source and vice versa.
In case power is flowing from left to right, $Z_{s,in}$ represents a source and $Z_{l,in}$ a load. The roles are exchanged if the power flow is reversed. The determination of the input impedances of the right side respectively the left side circuit is done by using the reflection coefficient. However the calculation using Eq. 3.9 and 3.10 and Z_0 as a reference will only lead to an effective impedance for the entire load side or source side. In case of a feedback larger than 1 the real part of this effective impedance is even negative e.g. $-70\,\Omega$ in the circuits in Fig. 3.12. A negative real part of an internal source impedance is not defined, neither are Eq. 3.9 and 3.10 for a Z_0 with a negative real part. The calculated effective impedance is then not the desired input impedance for the Nyquist analysis.
To extract the proper input impedance, the S-parameter matrix will be transformed as follows. S_{11} and S_{22} of an S-parameter set can be converted to an equivalent input and output impedance, Z_{in} and Z_{out} using

$$Z_{in} = \frac{1+S_{11}}{1-S_{11}} Z_{ref} \quad \text{and} \quad Z_{out} = \frac{1+S_{22}}{1-S_{22}} Z_{ref} \tag{3.15}$$

where Z_{ref} is the reference impedance of the S-parameter set. Since the S-parameters will be extracted using Z_0 as source, $Z_{ref} = Z_0$. Then Z_{in} represents the desired input impedance. Γ_1 from Fig. 3.8 can be calculated by the mismatch between load and output impedance, Z_{out}, of the network. The new network still maintains the forward and reverse transmission coefficients, S_{21} and S_{12}, but to distinguish the converted parameters from the classical S-parameters and to avoid confusion, they will be replaced by k_{21} and k_{12}. This is comparable to an amplifier's representation by an input and output impedance and its gain and reverse isolation. In Fig. 3.16 the resulting network with the equivalent values is depicted. The next chapter describes in detail how all these parameters can be extracted from simulation and used for the assessment of stability.

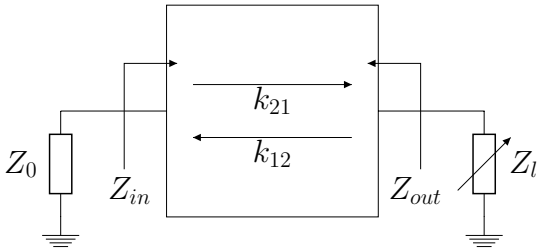


Figure 3.16.: Equivalent network using an input and output impedance, Z_{in} and Z_{out}, and forward and backward transmission coefficients, k_{21} and k_{12}.

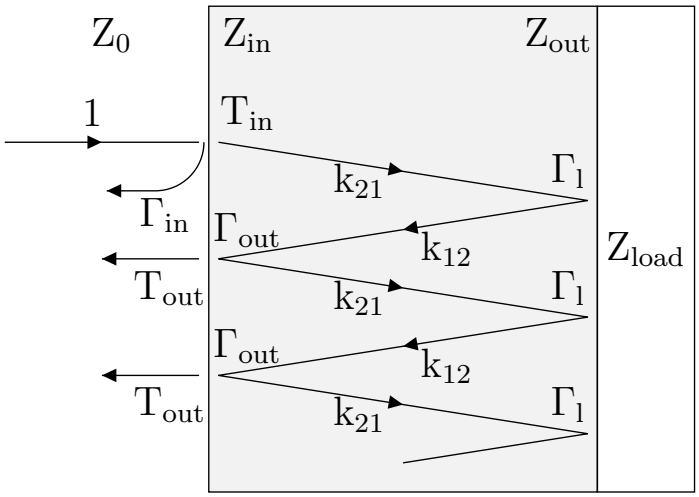


Figure 3.17.: Partial reflections and transmissions at an arbitrary network.

3.3.5. Extracting Equivalent Network Parameters

By using the equivalent impedances Z_{in} and Z_{out} instead of S_{11} and S_{22}, an equivalent network can be constructed. By introducing Z_0 also the source impedance of the probe has to be considered in the calculation in contrast to Eq. 3.6. To extract the values for theses parameters a multiple reflection analysis (compare [Poz05]) is conducted which is time domain-based. To visualize the procedure the partial reflections and transmissions, are shown in Fig. 3.17.

When we excite an incident wave by a source with the impedance Z_0, it will travel towards the network. First a part, Γ_{in}, will be reflected by the input impedance Z_{in}, the transmitted part T_{in} will continue to travel through the network and experience the effect of k_{21} which might be an amplification, attenuation and/or phase shift. At the output of the network, a part of the wave will be absorbed by the load Z_{load}. The rest will be reflected back into the network, Γ_l, gets modified by k_{12} and leaves the network. Hereby again a part gets reflected at the source. The absorbed share is T_{out}. The newly reflected part, Γ_{out}, will reenter the network and the process will continue for an infinite number of times. In the end the total

reflection can be calculated:

$$\begin{aligned}\Gamma_{total} &= \Gamma_{in} + T_{in}T_{out}k_{21}k_{12}\Gamma_l + \\ &+ T_{in}T_{out}k_{21}^2k_{12}^2\Gamma_l^2\Gamma_{out} + ... \\ &= \Gamma_{in} + T_{in}T_{out}k_{21}k_{12}\sum_{n=0}^{\infty}k_{21}^n k_{12}^n\Gamma_l^n\Gamma_{out}^n\end{aligned} \tag{3.16}$$

Using the geometric series

$$\sum_{n=0}^{\infty}x^n = \frac{1}{1-x} \quad \text{for} \quad |x| < 1 \tag{3.17}$$

Eq. 3.16 can also be expressed as

$$\Gamma_{total} = \Gamma_{in} + \frac{T_{in}T_{out}k\Gamma_l}{1 - k\Gamma_l\Gamma_{out}} \tag{3.18}$$

where

$$\begin{aligned}T_{in} &= 1 + \Gamma_{in} \\ T_{out} &= 1 + \Gamma_{out} \\ k &= k_{21}k_{12}\end{aligned} \tag{3.19}$$

For a converging series, $|x| < 1$, this leads to

$$\Gamma_{total} = \Gamma_{in} + \frac{(1+\Gamma_{in})(1+\Gamma_{out})k\Gamma_l}{1 - k\Gamma_l\Gamma_{out}} \tag{3.20}$$

where

$$\begin{aligned}\Gamma_{in} &= \frac{Z_{in} - Z_0^*}{Z_{in} + Z_0} \\ \Gamma_l &= \frac{Z_{load} - Z_{out}^*}{Z_{load} + Z_{out}} \\ \Gamma_{out} &= \frac{Z_0 - Z_{in}^*}{Z_{in} + Z_0}\end{aligned} \tag{3.21}$$

For $|x| > 1$ the series is not converging. With each partial reflection the total reflection will increase and with $n \to \infty$ also $\Gamma_{total} \to \infty$. The circuit is unstable.
But to avoid convergence problems the condition $|x| < 1$ is often considered to be always true in circuit simulators. This is the reason why the simulations as presented in chapter 3.3.2 are even possible and an effective resistance of a circuit converges against a negative resistance for an arbitrary reference impedance instead of diverging. (The exception where the total reflection is positive without diverging in Eq. 3.16 is when $Z_0 = Z_{in}^*$ and $\Gamma_l k > 1$, otherwise $k^n\Gamma_l^n\Gamma_{out}^n > 1$). This is also the reason why we are able to extract the parameters we will use to assess stability in the first place.
Eq. 3.20 leaves us with 3 unknown parameters of our network: Z_{in}, Z_{out} and k. By controlling the load impedance and changing it to three different values, three equations for Γ_{total} will be generated. This equation system can then be solved and the network is sufficiently described.
In case of a small-signal simulation the network parameters will not be influenced by a change of Z_{load} and, going along with it, a change in the reflected power. Therefore Z_{in}, Z_{out}

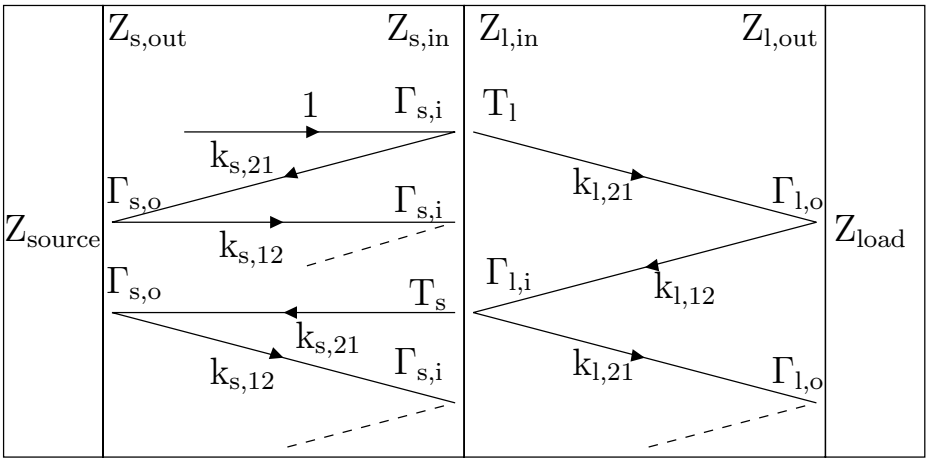


Figure 3.18.: Partial reflections and transmissions at a load and source network.

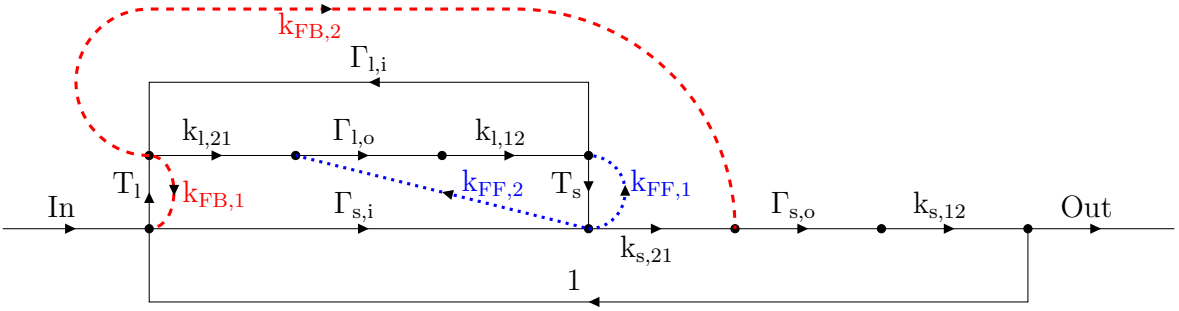


Figure 3.19.: Partial reflections and transmissions at a load and source network including feedback and feed-forward paths in dashed red and dotted blue, respectively.

and k will be constant. Using the extracted set of parameters the circuit's behavior can then be analytically analyzed for any arbitrary load or source impedance. But if a circuit is operating under a large-signal condition a change in the reflected power might also change the parameter set. Thanks to very precise circuit simulators even very small changes in the reflection coefficient can be simulated. Therefore only a slight change of the desired load impedance can be used to generate the necessary equations under the assumption that this does not influence the operating conditions of the overall circuit. In this case a new parameter extraction has to take place for each change of load or source impedance.

3.3.6. Assessing Stability

For the general case presented in Fig. 3.8 the reflected waves are not absorbed by a Z_0 but are additionally fed to the source network. Therefore the effects of the source network have also to be taken into account.
Fig. 3.18 shows the case when the source network is also considered. Each reflection at the border creates an additional partial wave traveling through the networks. To extract a transfer function from Fig. 3.18, we will transform both networks in a signal flow chart (black in Fig. 3.19). For simplification we again substitute $k_{l,12} \cdot k_{l,21}$ and $k_{s,12} \cdot k_{s,21}$ with k_l and k_s, respectively.

Ignoring the dashed red and dotted blue paths for now, there are three different loops in the system:

- $T_l \Gamma_{l,o} k_l T_s \Gamma_{s,o} k_s$
- $\Gamma_{l,o} k_l \Gamma_{l,i}$
- $\Gamma_{s,i} k_s \Gamma_{s,o}$

Extracting the denominator of the transfer function for the entire system using the present loops and Mason's rule [Mas53] leads to:

$$\begin{aligned} \Delta(s) &= 1 - L(s) \\ &= 1 - (T_l \Gamma_{l,o} k_l T_s \Gamma_{s,o} k_s + \Gamma_{l,o} k_l \Gamma_{l,i} + \Gamma_{s,i} k_s \Gamma_{s,o} \\ &\quad + \Gamma_{l,o} k_l \Gamma_{l,i} \Gamma_{s,i} k_s \Gamma_{s,o}) \end{aligned} \tag{3.22}$$

L can now be plotted and stability according to the Nyquist criterion examined.
But the system's description is not complete since the feedback/feed-forward is not considered in this equation. There are two kinds of feedback loops possible. After entering the load side, the waves travel to the source side ($e1$ in Fig. 3.11) and

- leave it again in direction of the probe ($b2$). On the way the signal gets modified by k_{FB1} (independent of Z_{source}).
- leave it in direction of the source impedance ($c2$), getting reflected by it, amplified by the reverse transmission coefficient $k_{s,12}$ and leaving the source network in direction of the probe again. The total gain coefficient is k_{FB2} (dependent of Z_{source}).

There might be an infinite number of feedback paths, but all are of the first or second kind. The only difference is the feedback gain. In signal flow theory, parallel branches from one node to another common node may be combined. Translating this to the signal flow graph, it leads to two new paths, depicted in red and dashed in Fig. 3.19. In the same way the feed-forward paths can be determined, dotted blue in Fig. 3.19. To simplify the graph further we combine the two feedback/feed-forward paths using the following equations:

$$L_{FF} = T_s k_{FF,1} + T_s k_{FF,2} \Gamma_l k_{l,12} \tag{3.23}$$

and

$$L_{FB} = T_l k_{FB,1} + T_l k_{FB,2} \Gamma_s k_{s,12} \tag{3.24}$$

The adjusted signal flow graph leads then to a new transfer function with the denominator:

$$\begin{aligned} \Delta &= 1 - L(s) \\ &= 1 - \\ &(T_l \Gamma_{l,o} k_l T_s \Gamma_{s,o} k_s + \Gamma_{l,o} k_l \Gamma_{l,i} \\ &+ k_s \Gamma_{s,o} \Gamma_{s,i} + L_{FF} + L_{FB} \\ &+ \Gamma_{l,o} k_l \Gamma_{l,i} k_s \Gamma_{s,o} \Gamma_{s,i} + L_{FF} L_{FB}) \end{aligned} \tag{3.25}$$

By exciting the load and source side with distinguishable signals, e.g. slightly different frequencies, it is possible to separate the fraction of the reflected signal that propagated through a feedback path from the one that propagated through the DUT and was reflected by the source.

3.3.7. Implementation in a Circuit Simulator

3.3.7.1. Probe Components

Fig. 3.20 shows a representation of a stability probe placed in a simplified circuit with a feedback and feed-forward path. The arrows in the probe portray the two direction in which the probe sends the probing signal: the source and the load side.

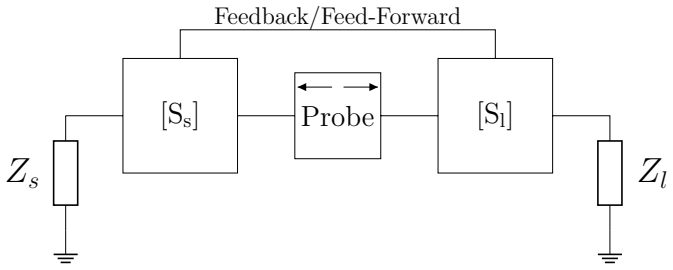


Figure 3.20.: Representation of the stability probe placed in a simplified circuit including a feedback path.

The main objectives in designing the probe are the following:

- The probe must not alter the circuit, i.e. it is non-invasive.
- The probe must detect instability in a loop independent of its placement inside the circuit.
- In case of several probes they must not influence each other.
- All feedback loops must be detected.
- The probe must work in small- and large-signal environments.

The heart of the probe is the signal generating and processing unit which is used to compute the incident and reflected waves. A representation is shown in Fig. 3.21.

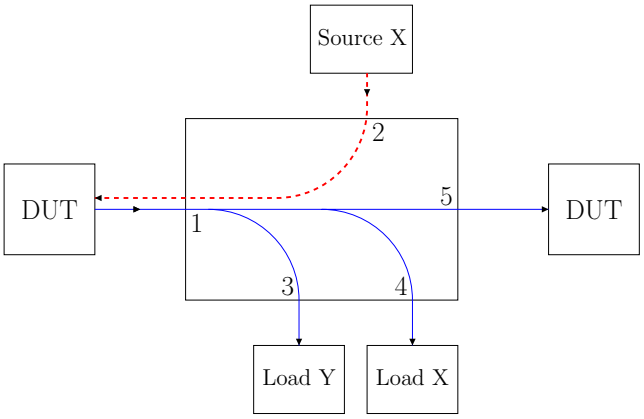


Figure 3.21.: Representation of the system block used for feeding the probing signal to the DuT including signal flow graphs. In red and dashed the excited probing frequencies, in solid blue the reflected wave.

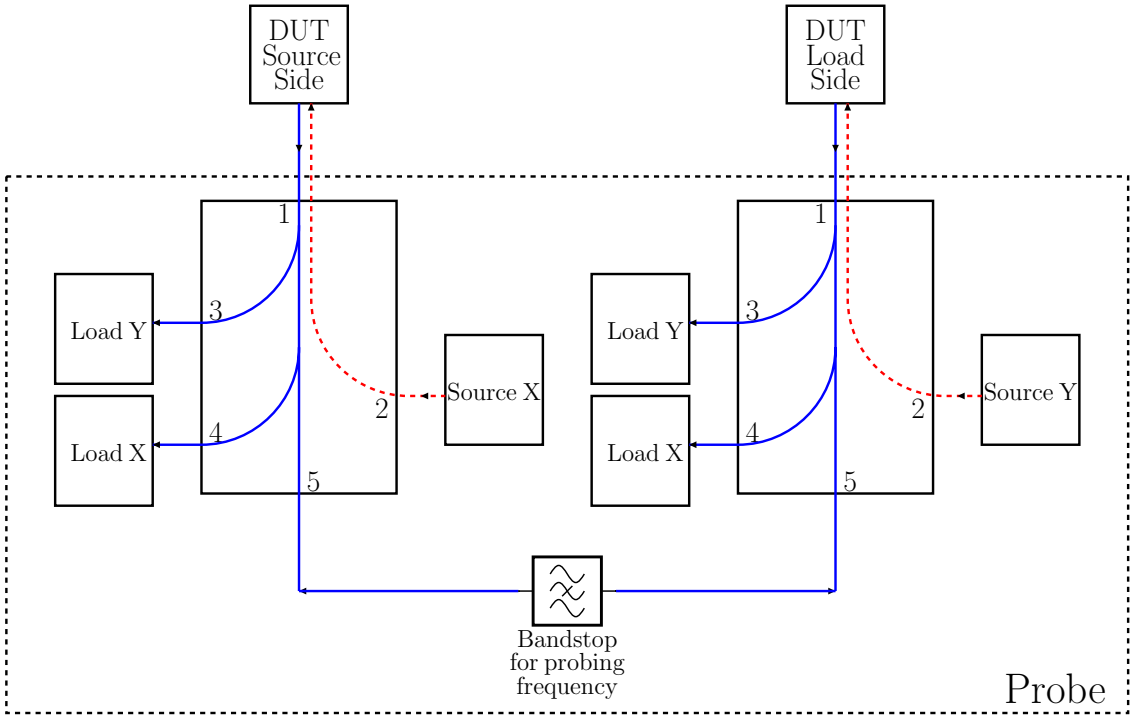


Figure 3.22.: Representation of the probe used in a circuit simulator. The left unit probes the left side (source side) of the circuit, the right unit the right side (load side). Externally excited signals can pass the probe via port 5 and the implemented notch filter.

The signals are generated by a source at port 2, fed to the circuit (port 1) and the corresponding reflections for the stability calculations are extracted at port 3 and port 4. Since the probe has to evaluate the reflection in two directions, to the load and source side, two of these units have to be implemented. The complete representation of the probe is shown in Fig. 3.22.
In order to avoid the interruption of the signal flow in the circuit from source to load side, all non-probing signals are passed from one side to the other using port 5 and a reflection-free notch filter that blocks exclusively the probing signal. That means still all AC signals, e.g. all considered harmonics and intermodulation products of a multi-tone frequency domain analysis, and all DC signals, can pass the probe. By preventing the probing signals from passing through the probe, it is assured that probing signals only enter the DuT in the desired direction and an unwanted mutual influence of the two sources in one probe is circumvented. Since the signal units use slightly different frequencies, a signal that is excited for example on the source side (Source X) can travel through the feed-forward loop and is added to the signals entering the load side. It is then fed to the corresponding load (load X) and is considered in the calculation of the total reflection. This happens vice versa for signals excited on the source side (Source Y to Load Y). Therefore all possible feedback/feed-forward loops are taken into account whilst assessing stability.
Avoiding the mutual influencing of multiple probes can be done by just manually shorting probes or implementing switches that can be controlled by an if-clause and a simple parameter sweep so that only one probe is active at the same time.

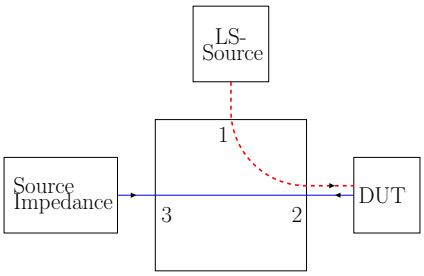


Figure 3.23.: Block diagram of the "large-signal feed"-component.

3.3.7.2. Large-Signal Probing

The fifth objective states, that the tool has to be usable not only for small signal but also for large-signal simulations. The probe as it is can be used with power sources and is created for performing harmonic balance simulations and therefore can be employed independently of signal power levels. The power of the injected probing frequencies is very low, in order to avoid creating nonlinearities in the DuT which would affect the circuit. Additionally the change in the load impedances to extract the network parameters is kept so small that the influence of the change in reflected power can be neglected.
However the large signal has to be introduced to the circuit. This is problematic because generally in stability analysis the source and load impedances are swept in magnitude and phase to determine if the circuit is conditionally or unconditionally stable and, if it is only conditionally stable, for which impedances (cp. stability circles of the Rollet approach). However, power sources often only feature real impedances, e.g. in Keysight's ADS. To avoid this problem, an additional "large-signal feed" was designed. The functionality is shown in Fig. 3.23.
The element is configured to present a through between the circuit port (DuT), port 2 and the port for the variable load, port 3. The path from the large-signal source to the circuit is a through from source to circuit (1 to 2) but an open the other way round (2 to 1). Hereby the large signal can enter the circuit but in terms of impedance termination the circuit will see the presented load at port 3.

3.3.8. Validation in Simulation

For the validation of the presented method the parallel and serial resonator circuits A and B from Fig. 3.12 will be used. They have to be adjusted to fit the requirements of the probe, in particular they have to contain a load and source impedance with a positive real part. So the negative resistance will be replaced by an equivalent S-parameter set that exhibits the same reflection coefficient, Γ_{total}, in an S-parameter simulation as the negative resistance, $\mathrm{R}_{\mathrm{eff}}$, would according to Eq. 3.9. In the test cases $\mathrm{R}_{\mathrm{eff}} < 0$ is always true. The schematic of the circuits with the different possible positions for probing is shown in Fig. 3.24. The possible probing points are between

1. negative resistance and resonator with load
2. negative resistance with capacitor and inductor with load
3. negative resistance with resonator and load

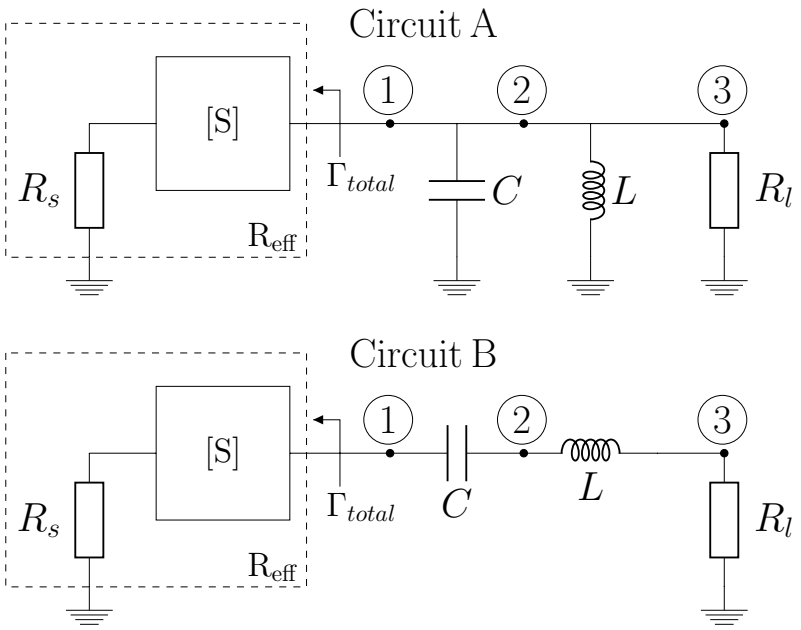


Figure 3.24.: Circuit A and B adapted from [Jac92] with the negative resistance represented by an S-parameter set and a source impedance with a positive real part.

Table 3.1 shows the resulting Nyquist plots for the three different probing positions in the circuits A and B. Additionally the effective negative resistance was changed so that its absolute value is in the first case larger than the load resistance and in the second case smaller than the load resistance. According to theory for $R_l < |R_{eff}|$ the serial resonator circuit will be unstable and for $R_l > |R_{eff}|$ stable. It is exactly the other way round for the parallel resonator circuit.
Here exclusively a real load and source impedance was chosen for reasons of comparison with the circuits presented by [Jac92]. However the presented approach is also applicable for a complex load, source or effective impedance. For the serial resonator and $R_l > |R_{eff}|$ the Nyquist plot does not encircle the critical point (1,j0) independently of the position of the probe (row 1). For $R_l < |R_{eff}|$ the critical point is encircled in clockwise direction for all positions. This means this circuit is correctly identified as unstable (row 2).
The Nyquist plots of the parallel resonator circuit has to behave in the opposite way according to theory. For $R_l < |R_{eff}|$ the critical point is not enclosed by the plot which states stability (row 3) as for $R_l > |R_{eff}|$ the plots circle the critical point and indicate instability for the circuit (row 4).
To measure the relative stability the Nyquist plot is analyzed regarding how close the curve is to the critical point $(1, j0)$ when the plot intersects the positive real axis. The corresponding frequency, ω_p, is called phase-crossover frequency [GK09]. The gain margin, GM, is then defined as

$$GM = -20log_{10}|L(j\omega_p)|dB \tag{3.26}$$

It describes the additional gain that is necessary in the loop transfer function to change the state of the circuit from stable to oscillating. Or if the circuit is unstable the reduction of gain that is necessary to stabilize the circuit.
For example the stability margin for the presented cases in Table 3.1 are -1.36 dB, 0.92 dB, 0.92 dB and -1.36 dB for row 1 to 4 respectively. The gain margin for the stable serial and

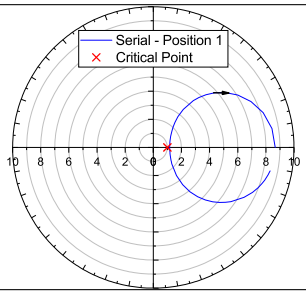
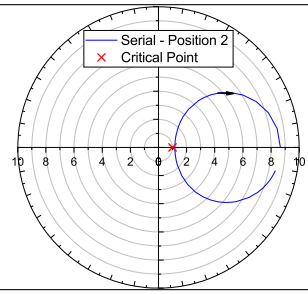
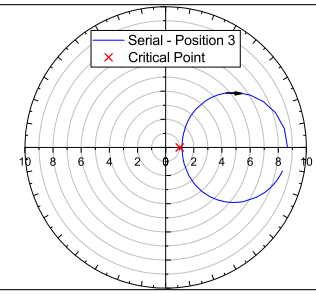
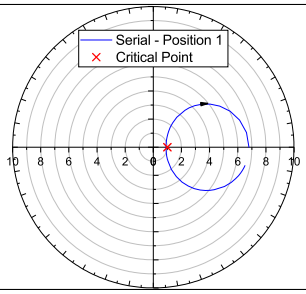
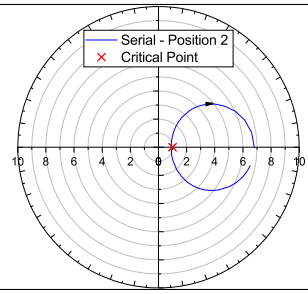
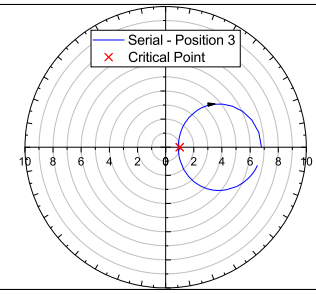
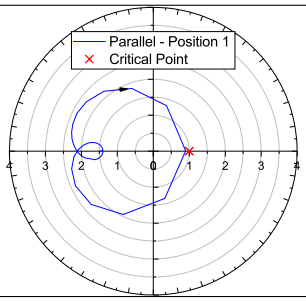
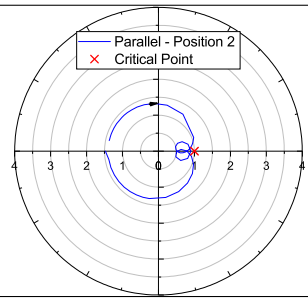
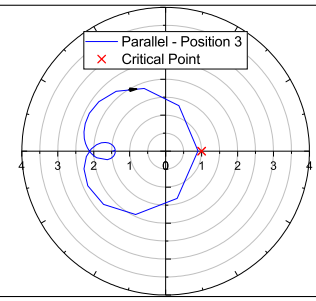
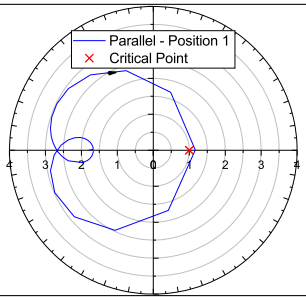
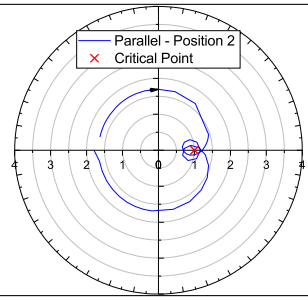
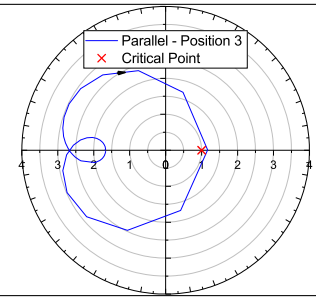
	Position 1	Position 2	Position 3
Serial Resonator	$R_l > \lvert R_{eff} \rvert$		
Stable			
Serial Resonator	$R_l < \lvert R_{eff} \rvert$		
Unstable			
Parallel Resonator	$R_l < \lvert R_{eff} \rvert$		
Stable			
Parallel Resonator	$R_l > \lvert R_{eff} \rvert$		
Unstable			

Table 3.1.: Nyquist plots for the serial and parallel resonator circuit adapted from [Jac92] for two different conditions, $R_l > |R_{eff}|$ and $R_l < |R_{eff}|$. Columns 1 to 3 represent the different positioning of the probe in the circuit.

the unstable parallel resonator circuits (row 1 and 4) is identical. The same is true for the gain margin of the unstable serial and stable parallel resonator circuit (row 2 and 3). This was predictable since the identical load and negative source resistances, R_l and R_{eff}, for these test circuits were used. Therefore also the degree of (in)stability is the same. These results give additional prove of the functionality of the probe.
This type of stability analysis was performed on all active circuits that will be presented in the following chapters. For the dual-gate down-converter the process and the results will be explained exemplarily in detail.

4. Technology Overview

The MMICs that will be presented in the following chapters are all based on the same technology, the 35 nm mHEMT technology of the IAF located in Freiburg, Germany. Since this technology with its fast transistors is the key enabler for circuits at terahertz frequencies, it will be described in this chapter.

This $\mathrm{In_{0.52}Al_{0.48}/In_{0.8}Ga_{0.2}As}$ mHEMT technology with a 35 nm gate length features a transit frequency, f_t, of above 500 GHz and a maximum oscillation frequency, f_{max}, of more than 1000 GHz. The mHEMTs are grown on Gallium Arsenide (GaAs) wafers with a 4-inch diameter which gets thinned to a final thickness of 50 µm The transistors are encapsulated in a low-k benzo-cyclo-butene (BCB) layer to reduce the parasitic gate capacitance. A maximum transconductance of 2500 mS/mm and a maximum drain current of 1600 mA/mm are achieved. [LTM+08] gives a detailed description of the front-end-of-line (FEOL) process. Fig. 4.1 shows the cross-section of the frontside process.

There are three metal layers available: MET1, MET2 and MET3. MET1 and MET2 are electron-evaporated gold (Au) layers with a thickness of 0.3 µm. Structures composed of these two layers are defined by using a lift-off process. The third metal layer is an Au layer produced by galvanic metallization in airbridge technology with a thickness of 2.7 µm. [ARCRV+18]

Several passive structures can be realized using these three metal layers. Although, recently more and more circuits in the same technology use thin film microstrip line (TFMSL) [JNT+20, ARCRV+18], the transmission line type employed for all circuits in this work is a grounded coplanar waveguide (CPWG). The coplanar transmission line exhibits lower crosstalk and lower radiation. Moreover, since the ground plane is on the same layer as

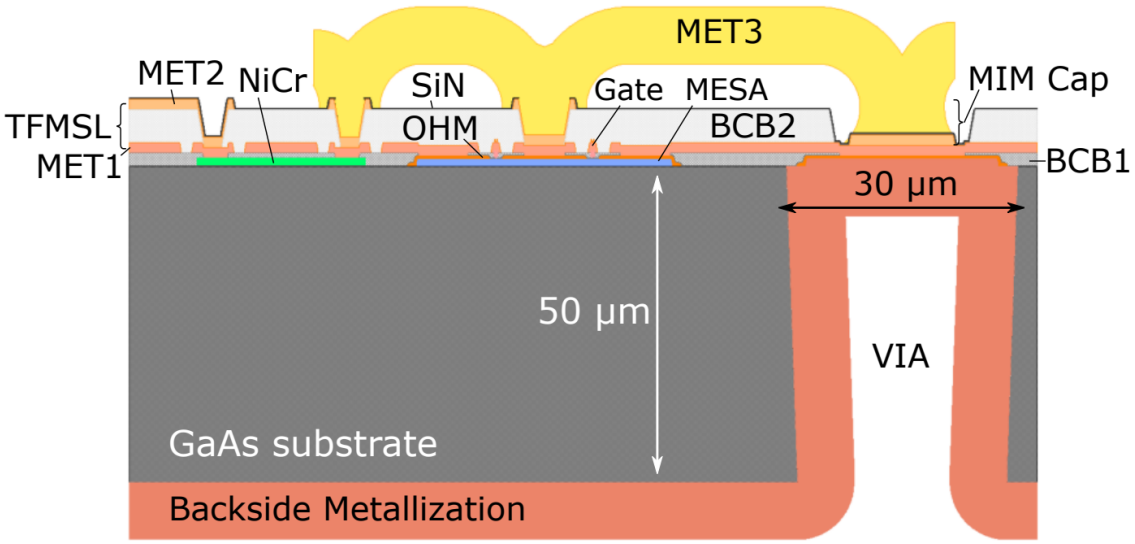


Figure 4.1.: Overview of the layer stack of the 35 nm process of the Fraunhofer IAF [JNT+20].

the signal line, it is easier to access. For example, in microstrip line environments, a via is necessary to establish a contact to the ground potential [Sim01]. The CPWG is realized with the first metal layer (MET1). A 1.4 µm thick BCB layer (BCB2) separates MET1 from MET2. In a TFMSL environmet MET2 is used as signal layer and MET1 as ground plane.
A 80 nm thick Silicon Nitride (SiN) layer is used for passivation of the circuits. The SiN can also be used to create metal-insulator-metal (MIM) capacitors. The bottom metal layer is MET2 and the top metal layer MET3. This results in a capacitance per area of $0.8\,\mathrm{fF}/\mu\mathrm{m}^2$. Series and parallel capacitors can thereby be realized.
MET3 also plays a role to suppress unwanted modes in the CPWG. Especially transmission line junctions, corners and bends are prone to excite those. Therefore, airbridges are used to connect the ground planes on either side of the signal line. Moreover, MET3 facilitates the DC routing by offering a way to cross the MET1 signal lines with a minimum level of influence. Resistors are realized with a Nickel-Chromium (NiCr) layer located below BCB with a sheet resistance of around $50\,\Omega/\square$.
Fig. 4.2 and 4.3 exemplarily show the cross-section of the CPWG and an airbridge. An additional overview of the layer stack for the the most common components is given in Appendix B, Fig. B.1 to Fig. B.3. Please note that the purpose of these visualizations is to give an impression of the layer stack and its topography. However, the drawings are not true to scale.

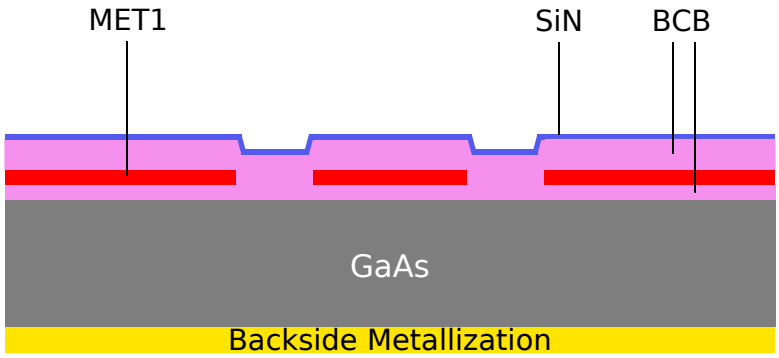


Figure 4.2.: The cross-section of a grounded coplanar waveguide.

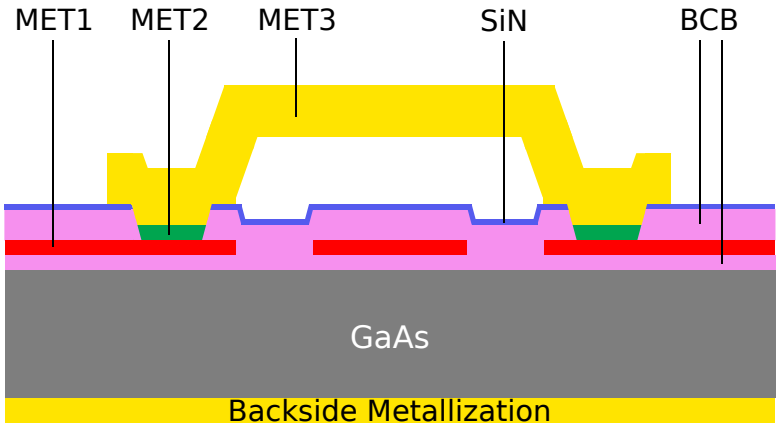


Figure 4.3.: The cross-section of a grounded coplanar waveguide, where the ground planes are connected by an airbridge.

5. Frequency Converter Architectures

In this work the terms "mixer topology" and "mixer architecture" are used to describe two different circumstances. Mixer architecture refers to the design of a single mixer cell which will be discussed in more detail in this chapter. A mixer topology is the arrangement of single mixer cells in order to achieve different functionalities in a receiver, such as a balanced, image rejection or quadrature operation. In general, the mixer topology is independent from the mixer architecture.
Various architectures for mixers are known from literature. A first separation is done by distinguishing between active and passive mixers. In a second step, subcategories are introduced based on the corresponding nonlinearity used for mixing as proposed in [Ell08]. An overview and structure is given in Fig. 5.1.
The architectures analyzed for terahertz applications in this work are differential pair, nonlinear transconductance, dual-gate and passive, nonlinear resistance. The corresponding boxes are marked in Fig. 5.1 to visualize which architectures will be presented in the course of this work and in which mode of operation, up- or down-converter or both. First the designs for down-conversion will be discussed and subsequently designs for up-conversion.

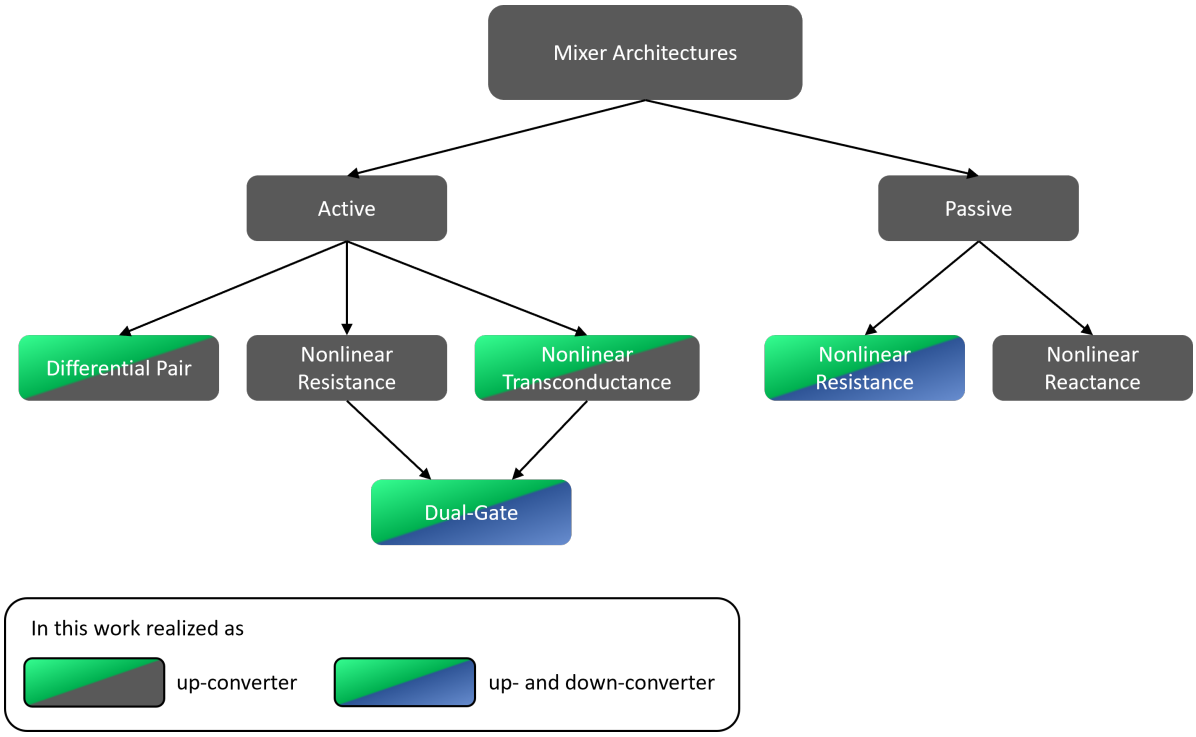


Figure 5.1.: Overview and structure of mixer architectures and the underlying source of nonlinearity.

5.1. Down-Converters

5.1.1. Dual-Gate

The content of this section has been published in [2]. It was slightly adjusted to match the layout of this work.

5.1.1.1. MMIC Design

A dual-gate mixer presents a good basis to evaluate active mixers for terahertz applications, since knowledge gained from this design can later also be used for more complex solutions like Gilbert-cell mixers. Fig. 5.2, top, shows the schematic representation of the dual-gate mixer. Two transistors each with a gate width of 19 µm and two fingers form the heart of the mixer.

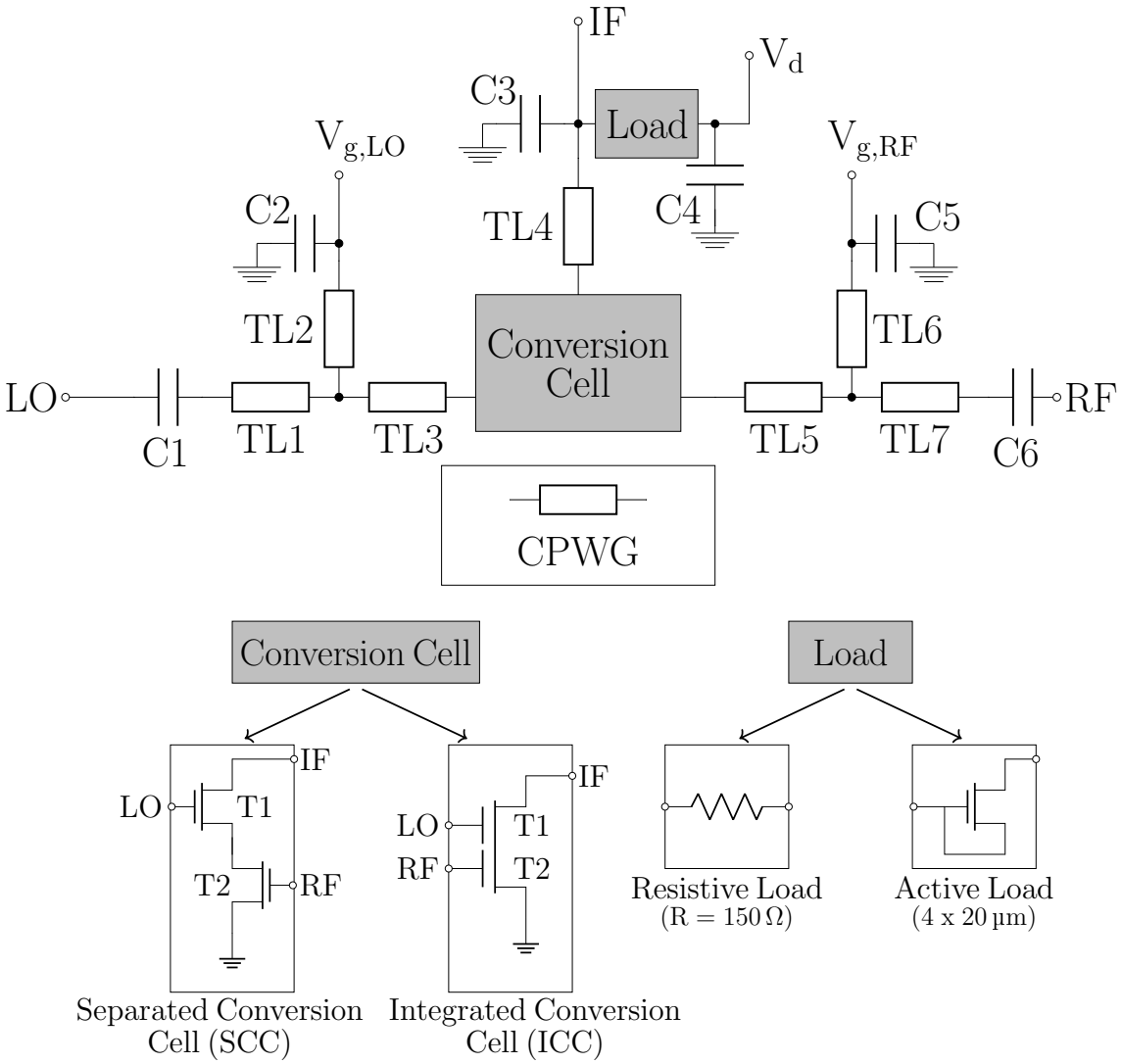


Figure 5.2.: Top: The simplified schematic of the active dual-gate down-converter. Bottom: The options for replacing the grey rectangle placeholder. The rectangle with the description "Load" is replaced by either an active or resistive load depending on the version. The rectangle labeled "Conversion Cell" will be replaced by either a separated or an integrated transistor layout.

In simulation 19 µm has shown the best compromise between conversion gain, linearity and necessary LO power for the targeted RF range of 220 to 280 GHz. Two versions of the physical implementation of the transistor cell for the dual-gate mixer were fabricated.
Fig. 5.2, bottom, shows the two versions of the layout of the transistor. In the first version the two transistor cells were kept separated, and the source of T1 is connected to the drain of T2 by a short piece of transmission line. In the second version, T1 and T2 are integrated in one multi-finger transistor cell sharing the same extrinsic device environment. For future reference, the fully integrated conversion cell will be addressed as integrated conversion cell (ICC) and the version with separated transistors as separated conversion cell (SCC). For clarification a schematic of both implementations of the transistor cells and a photograph of the section of the chip are shown in Fig. 5.3 and 5.4.

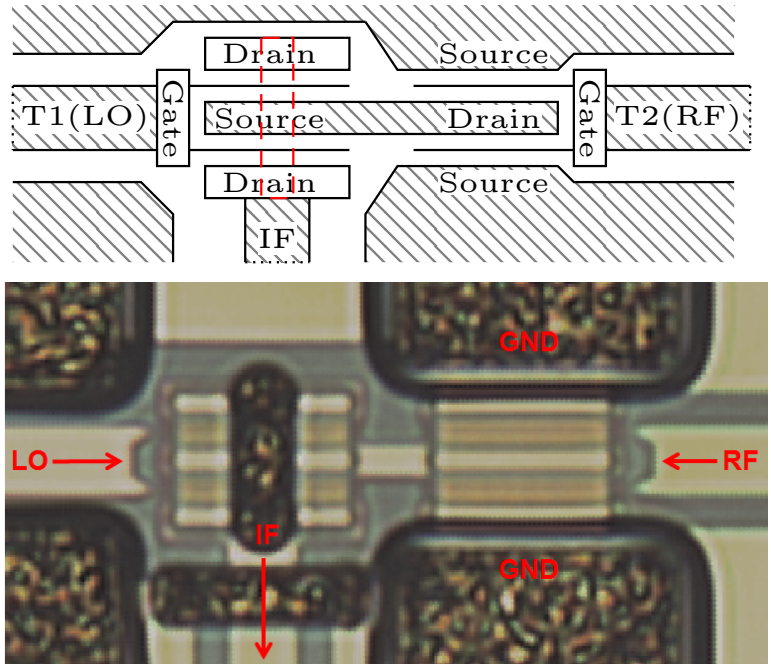


Figure 5.3.: The simplified schematic of the separated conversion cell (top) and a magnified photograph of the section of the chip (bottom). The transmission line environment is coplanar, where the center signal lines are embedded into ground planes. In dashed red is an airbridge connecting the two drain terminals of T1.

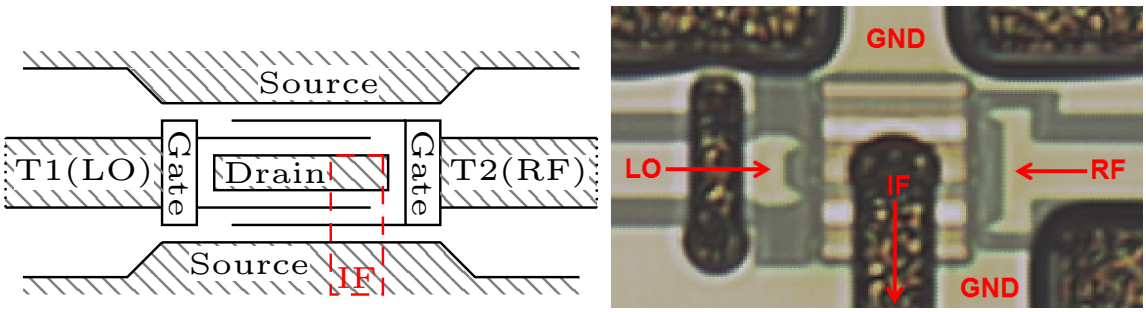


Figure 5.4.: The simplified schematic of the integrated conversion cell (left) and a magnified photograph of the section of the chip (right). Here in dashed red is the airbridge that is used to apply the IF to the drain of T1.

The LO is fed to the gate of T1. To match the LO input port to the gate impedance the transmission lines TL1, TL2 and TL3 are used. C1 operates as a decoupling capacitor and prevents DC current from flowing into the LO port. TL2 in combination with C2 also decouples the high frequency LO signal from the DC supply path for the gate bias of T1. In order to do so the length of TL2 is set to $\lambda/4$ at 240 GHz.
The RF signal is applied to the gate of transistor T2. In the same way as the LO, the RF port is matched by the transmission lines TL5 to TL7. The gate bias for T2 is fed to the circuit via TL6. TL6 in combination with C5 ensures no RF signal is flowing into the DC source. C6 is employed as a DC block. The gate bias of T1 is 0.3 V and for T2 0.18 V. The simulated current density at these bias points is around 350 mA/mm.
The IF is extracted at the drain of T1 where also the drain voltage is applied. The down-converter will be employed as a so-called zero-IF mixer meaning that the IF ranges from DC to in this case 25 GHz. 25 GHz was targeted because this is the bandwidth that is necessary to transmit 100 Gbps using a 16-QAM modulation and an idealized rectangular filter. Matching at these low frequencies is hard to accomplish on-chip using transmission lines and MIM capacitors.
Additionally, it complicates the on-chip decoupling of the IF signal path from the DC source. For transmission lines to operate properly as distributed elements for impedance transformation their length has to be $>\lambda/20$ [Bah03] which is impossible to implement on-chip for the range from DC to several tens of gigahertz.
Inductors exhibit a lowpass behavior. Hence, for the IF signal a parallel inductor in the DC supply path creates a highpass filter. The part of the baseband spectrum below the cut-off is lost due to the short presented by the DC supply. In [Raz97] a threshold is defined at which the overall data signal starts to be negatively affected by a suppression of low frequency components. According to [Raz97] the threshold lies at 0.1% of the baseband bandwidth. To minimize the cut-off frequency the size of the inductor has to be increased. However, an on-chip inductor with a cut-off frequency of less than 25 MHz would already exceed the total chip size of the mixers presented here.
Here, two different versions for IF decoupling were implemented as shown in the bottom of Fig. 5.2. Version 1 is a resistive load, a 150 Ω resistor in series with the DC supply. This is a simple, robust and frequency independent measure for decoupling. The higher the resistance is, the better the decoupling will become. But also the necessary drain voltage and the power dissipation in the resistor will increase. 150 Ω proved to be a good compromise between those parameters.
Version 2 is an active load. In the following discussion the different versions will be labeled as follows: The mixer with a resistive load and an integrated conversion cell is RL1, the version with two separated transistors (SCC) is RL2. AL1 and AL2 describe the down-converters with an active load and with an integrated or a separated transistor layout, respectively. Table 5.1 gives a summary of the nomenclature.

Table 5.1.: Overview of the nomenclature of the four fabricated H-band mixer versions.

	Integrated Conversion Cell	Separated Conversion Cell
Resistive Load	RL1	RL2
Active Load	AL1	AL2

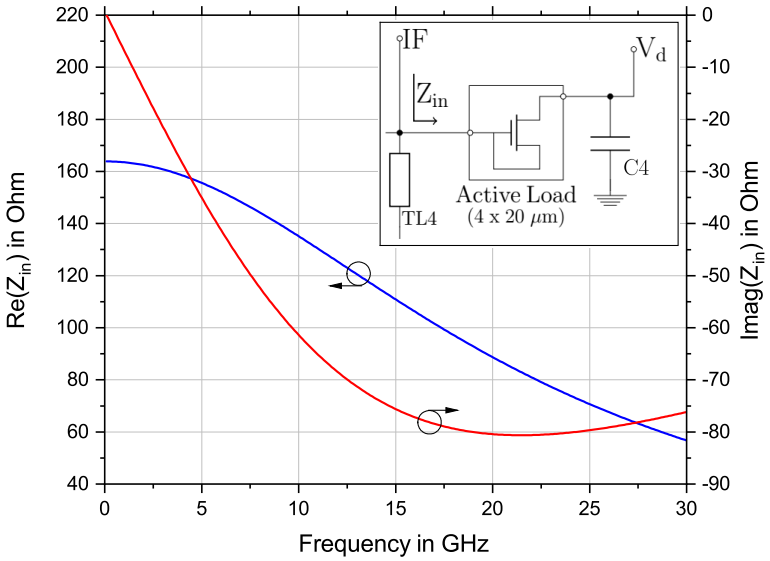


Figure 5.5.: Simulated real and imaginary part of the impedance of the active load over frequency. The schematic in the inlet visualizes the point of extracting the input impedance Z_{in} of the active load.

The active load is realized by connecting the gate of a normally-on transistor with its source. In the employed technology $\mathrm{V_{gs}} = 0$ does not represent the bias condition for maximal gain. The source is then connected to the drain of the dual-gate transistor via TL4. The drain voltage is fed to the drain of the active load. Due to its nonlinear channel resistance the active load is able to conduct the same current but creates a lower DC voltage drop. Thereby the overall necessary drain voltage can be reduced for the same drain current and the same decoupling. To match the resistive load with its 150 Ω, a 4-finger transistor with a gate width of 20 µm was chosen. The resulting real part of the input impedance, Z_{in}, presented to the circuit by the active load was extracted by an S-parameter simulation and using

$$Z_{in} = \frac{1 + S_{11}}{1 - S_{11}} \cdot Z_0 \tag{5.1}$$

where Z_0 is the reference impedance of the simulation. The results are shown in Fig. 5.5. The inlet in Fig. 5.5 visualizes the point of extraction of Z_{in} within the circuit for better understanding. A chip photograph of version AL2 is shown in Fig. 5.6.
The overall chip size is 1000 µm x 750 µm including RF and DC pads. The active area amounts to 300 µm x 400 µm including the large RF bypass capacitors. Excluding those, the active area reduces to only around 300 µm x 300 µm.
For low IF frequencies up to 10 GHz the active load shows a resistance between 140 and 160 Ω. For higher frequencies due to the parasitic capacitances the quality of the decoupling decreases to 60 Ω at 30 GHz. This affects the overall achievable bandwidth of the circuit. For the range of the LO and RF frequencies the decoupling network presents a very low resistance of 2 Ω and therefore acts like a bypass.
The overall port-matching for all four versions is similar. The simulated results for AL1 were already discussed in [3] and are shown in Fig. 5.7. The simulations of the matching were conducted following the technique introduced in chapter 3.1 using a harmonic balance simulation in a large-signal environment to mimic the real operating conditions as close as

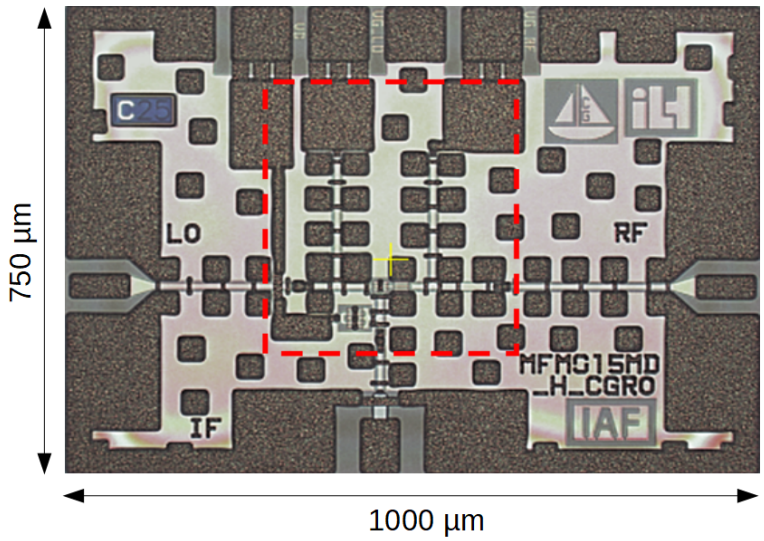


Figure 5.6.: Chip photograph of the dual-gate mixer version with active load and SCC (AL2). The chip size is 1000 µm x 750 µm with an active area of 300 µm x 400 µm (dashed red).

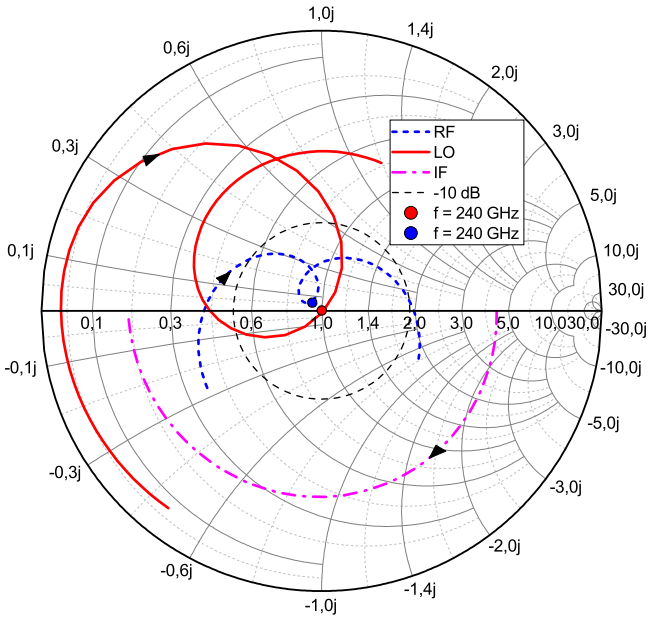


Figure 5.7.: Simulated port matching of AL1 for LO (200 - 280 GHz), RF (200 - 280 GHz) and IF (DC - 35 GHz). In dashed black the -10 dB-circle as reference [3].

possible.

For the LO and RF reflection coefficients the frequency was swept from 200 to 280 GHz, for the IF from DC to 35 GHz. The LO is matched more narrowly for a minimum reflection of less than −40 dB at 240 GHz since the LO is fixed at that frequency for the targeted application. Nonetheless, the frequency range where the LO lies below −10 dB is from 235 to 245 GHz to make the circuit more stable with respect to fabrication tolerances which might lead to a shift of the optimum in frequency. By exchanging the active load with the resistive one, the LO matching becomes more broadband and the IF matching improves by 3 dB.

Following the concept presented in chapter 3.3, a stability analysis was performed for the dual-gate down-converter. In order to do so, a probe was placed at each ungrounded terminal

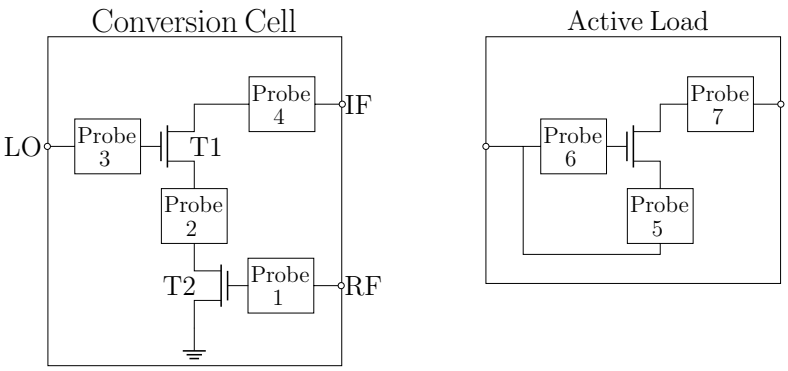


Figure 5.8.: Overview of the probe placements for the stability analysis as described in chapter 3.3.

of each transistor in the design as shown in Fig. 5.8. For the resistive load versions this amounts to four probes: two at the gates of T2 (probe 1) and T1 (probe 3), one at the source of T1 which is at the same time the drain of T2 (probe 2) and one at the drain of T1 (probe 4). For the version with the active load three additional probes are necessary at the source (probe 5), gate (probe 6) and drain (probe 7) of the load transistor. As an example, the full set of results for AL1 with 50 Ω loading is depicted in Fig. 5.9 and Fig. 5.10. For the plots where the curve is in close proximity of the critical point (probes 4, 5 and 7), versions magnifying the critical area are shown in Fig. 5.11. Since there is no encirclement of the critical point +1, the circuit is stable.

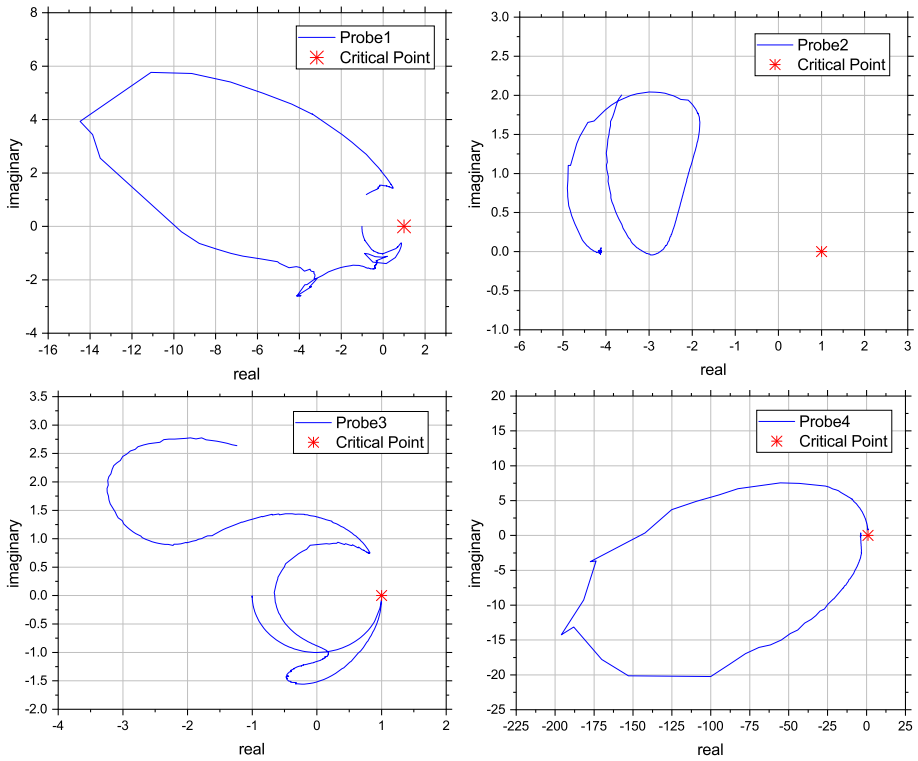


Figure 5.9.: Nyqusit plots for the probes placed at the gate of T2 (top left), the source of T1 (top right), the gate of T1 (bottom left) and drain of T1 (bottom right).

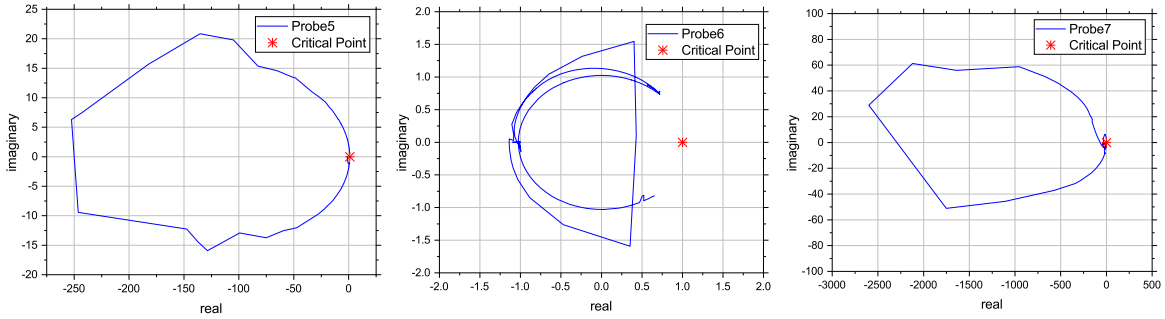


Figure 5.10.: Nyqusit plots for the probes placed at the gate (left), source (middle) and drain of the active load (right).

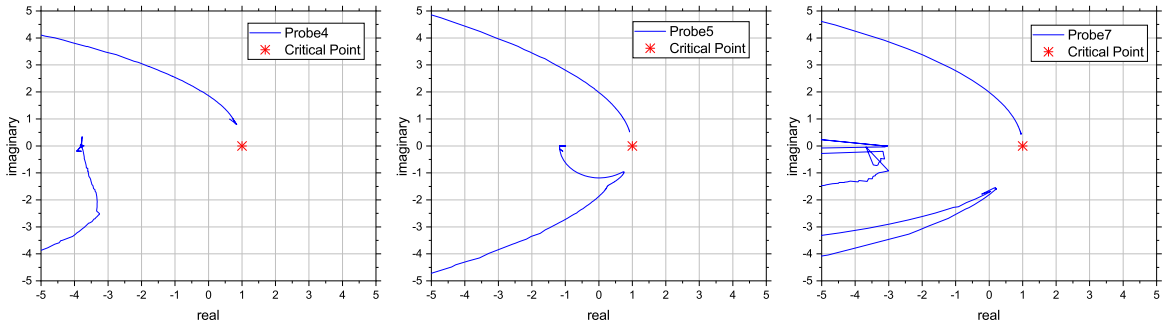


Figure 5.11.: Nyqusit plots for the probes 4 (left), 5 (middle) and 7 (right) magnifying the critical area around the critical point to enable a clearer assessment of stability.

5.1.1.2. Measurement Results

Fig. 5.12 shows the conversion gain of the four active mixer versions versus the LO input power at an LO frequency of 240 GHz and a RF frequency of 241 GHz. All measurements were conducted with a low RF power of −25 dBm to ensure linear conversion gain behavior. The maximum achieved conversion gain was −4.8 dB for RL2 at an LO input power of 0 dBm. The corresponding ICC version has a less steep gain curve therefore exhibiting higher conversion gain at lower LO input powers. Already at −10 dBm a conversion gain of −8.5 dB was achieved. The maximum lies at −5.6 dB for −3 dBm input power. The versions with the active load performed less well. They have the same gain shape as their counterparts with resistive load but show a lower conversion gain. The curve of the ICC version, AL1, is shifted by around 2 dB to lower values, and Al2, by 4 dB.
The conversion gain over RF frequency for the dual-gate mixers is compared in Fig. 5.13. For all four measurements the LO power was chosen in order to achieve maximum conversion gain, that means for RL2 and AL2 0 dBm and for RL1 and AL1 −2 dBm, respectively. The LO frequency was kept at 240 GHz and the RF power at −30 dBm.
As expected, RL2 exhibits the highest conversion gain near the carrier frequency and AL2 the lowest. For all four plots the conversion gain for the lower sideband (LSB) only decreases by around 0.5 dB in the measurement range. The upper sideband (USB) shows a steeper descent, especially for AL2. This leads to the assumption that the RF matching for the higher sideband is not as good as simulated in Fig. 5.7 and the optimum might have shifted to lower frequencies. This shift in frequency could also explain the ripple on the measured results. The calibration, that was performed, is prone to deviation caused by a mismatch

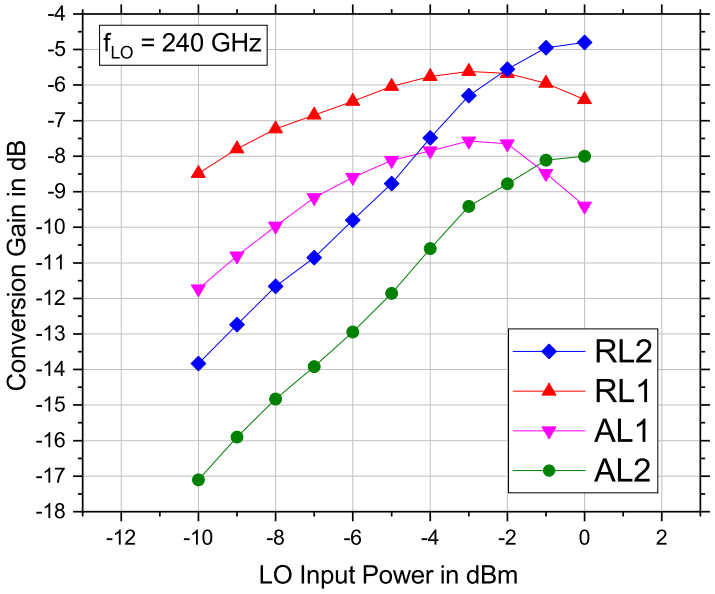


Figure 5.12.: Measured conversion gain versus LO input power at an IF frequency of 1 GHz, an RF power of −25 dBm at an LO frequency of 240 GHz for the active dual-gate down-converters.

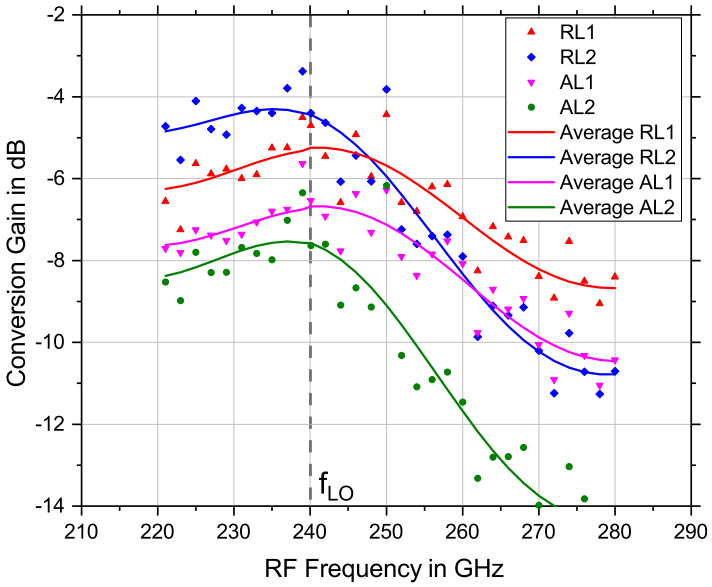


Figure 5.13.: Measured and simulated conversion gain versus RF frequency frequency at an RF power of −25 dBm at an LO frequency of 240 GHz for the active dual-gate down-converters.

between the DuT and the measurement setup. Depending on the magnitude of mismatch between setup and DuT, such a ripple on the measurement results will be the consequence. For example, a 15 dB probe match and a 10 dB return loss will lead to a ripple of ±0.5 dB. For a 15 dB probe match and a deteriorated DuT return loss of 4 dB the overall error range would be around ±1.5 dB.

Unfortunately, the measurement setup was limited to a lowest frequency of 220 GHz. This prevented the measurement of the lower corner of the 3 dB bandwidth for all four down-converters. The resulting measured 3 dB bandwidths of the four versions are given in Table 5.2.

Table 5.2.: 3 dB bandwidth for all four versions of the dual-gate mixer at an LO frequency of 240 GHz.

RL2	RL1	AL2	AL1
38 GHz	48 GHz	31 GHz	52 GHz

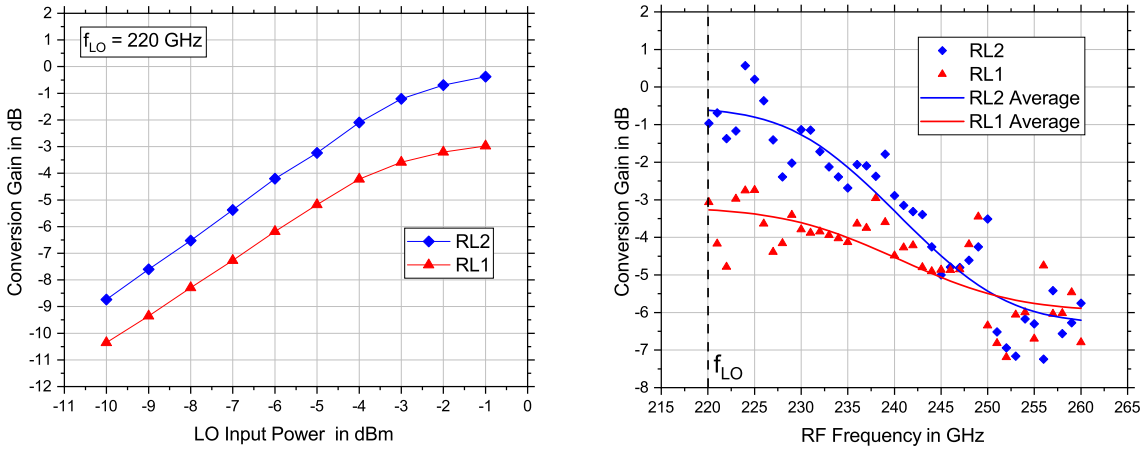


Figure 5.14.: Left: Measured conversion gain versus LO input power at an IF frequency of 1 GHz, an RF power of −25 dBm at an LO frequency of 220 GHz for the active dual-gate down-converters. Right: Measured conversion gain versus RF frequency frequency at an LO power of 0 dBm, an RF power of −25 dBm and an LO frequency of 220 GHz for the active dual-gate down-converters. An average of the curves was generated for better visualization.

Additionally, measurements of the active mixer with resistive load were conducted for a different LO frequency of 220 GHz with the same setup. Fig. 5.14, left, shows the conversion gain versus LO power. Still, RL2 exhibits the highest conversion gain. It reaches almost zero loss at an LO power of −1 dBm. RL1 achieves −3 dB at the same LO power. The effect of a declining conversion gain did not occur.
The RF frequency behavior of RL1 and RL2 for an LO of 220 GHz is shown in Fig. 5.14, right. Due to the limitation of 220 GHz as lowest RF frequency only the USB of the mixer was measured. The single sideband 3 dB bandwidth in these cases is larger than 20 GHz. For RL2 24 GHz were measured and for RL1 35 GHz.

5.1.1.3. Influence of the Transistor Layout

In Fig. 5.12, for both versions, resistive and active load, a similar behavior can be observed: For the ICC the conversion gain at lower LO input power is noticeably higher, starts to saturate earlier and hits a maximum at −3 dBm. For higher LO power the conversion gain is decreasing. As can be seen in Fig. 5.12 the SCC versions saturate at 0 dBm which is the maximum available LO input power. Therefore, no clear statement can be given if the effect will also take place in the measurements at higher LO powers for this design. Simulations shown later in this chapter will predict that it does.
The decrease of input power is unusual for a dual-gate mixer, where the operation principle is multiplicative mixing not additive mixing. In additive mixing such a behavior can be traced

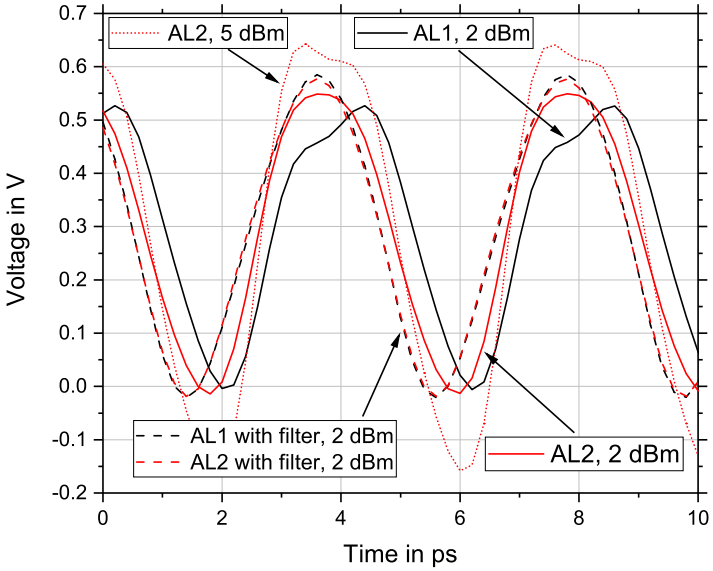


Figure 5.15.: Simulated time domain signal of the voltage at the gate of transistor T1 for AL1 and AL2 at an LO power of 2 dBm with (dashed line) and without (solid line) filtering of the fundamental at the drain of T1. Red, dotted: time domain signal of AL2 at an higher LO power level of 5 dBm.

back to a reduction of the conduction angle due to the high voltage swing of the LO signal. But for a large voltage swing the dual-gate mixer enters a quasi switching mode of operation, where the conversion gain saturates. In theory, increasing the LO power has no further influence on the conversion gain.

To answer the question why the conversion gain drops, a closer look at the differences in the layouts of the mixers and the voltages at certain nodes is necessary. Simulating and extracting the time domain voltage signal at the gate of T1, the gate where the LO is applied, is a first indication. In Fig. 5.15 the time domain voltage signals of both AL1 and AL2 are given.

Ideally, only the LO sine wave should be present. This is true for low LO power levels. But, increasing the LO power, distortions of the sine wave become visible. For example, at 2 dBm, the positive amplitude of AL1 (solid black line), decreases by around 15 % and the rising edge is "dented". Its phase is clearly shifted. However, for AL2 at 2 dBm (solid red line) the amplitude only decreases by around 5 %, but also a phase shift is visible. The gate voltage of AL1 deviates visibly more from the desired sine wave than that of AL2 . For higher LO power the time domain signal of AL2 gets distorted, too. At 5 dBm (dotted red line), it is cropped as well during the positive half wave of the sine. This is an indicator for harmonics present at the gate.

For harmonic frequency components to occur in the gate voltage a feedback of the output signal of the transistor to the gate must take place. To suppress that feedback an ideal filter is introduced directly at the drain. It presents a short exclusively to the fundamental LO frequency. Filtering out the LO at the drain leads to the disappearance of the distortion in the gate voltage of T1 (black and red dashed line).

The simulation of the conversion gain versus LO power of all four mixer versions with and without ideal filter is shown in Fig. 5.16. A visualization of the configuration with the filter is shown in the inlet.

The simulations predict a similar behavior as measured. The ICC versions AL1 and RL1, have

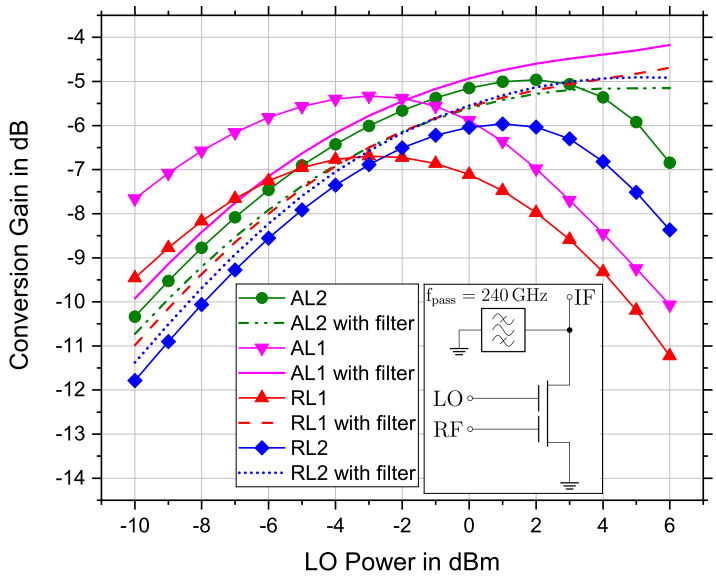


Figure 5.16.: Simulation of the conversion gain with and without LO filter at the drain for all four down-converter versions AL1, AL2, RL1 and RL2 for an LO frequency of 240 GHz and a RF power of −25 dBm. The inlet shows the configuration with band-pass filter.

a higher conversion gain for lower power levels, start to saturate earlier and then decrease. The decrease in conversion gains is also visible for the SCC versions, it starts however, at a 6 dB higher LO power. In simulations, the active load mixers, AL1 and AL2, perform better than their resistive load counterparts. In the measurements it is vice versa. Chapter 5.1.1.4 will give the reason for this.

The most important observation here is, that after introducing the filter, the behavior of the conversion gain now matches the theoretical behavior with a linear increase and a saturation for higher LO powers. No decrease in the conversion gain takes place.

The difference of AL1 and AL2, besides layout of the transistor cell, lies in the manner in which the IF is connected to the drain of T1. This can also be seen in Fig. 5.3 and Fig. 5.4. In the ICC version the IF is fed to the drain by an airbridge in comparison to the SCC version, where it is done via a coplanar wave guide. The latter one has the advantage of a better-defined characteristic impedance. Furthermore, the length from the drain of T1 to the connection of the load, depicted as TL4 in Fig. 5.2, decreases by around 10 µm from 35 µm to 25 µm. These small changes are enough to change the suppression of the fundamental and harmonics of the LO at the drain and cause a significantly different behavior of AL1 and AL2 or RL1 and RL2, respectively.

By decreasing the LO frequency, the wavelength increases. The absolute difference in length of TL4 for AL1 and AL2 or RL1 and RL2 is constant. But the relative difference in terms of electrical length of TL4 between the two version decreases. This leads to the more similar characteristic of the ICC and SCC versions at 220 GHz, Fig. 5.14, than at 240 GHz, Fig. 5.12. Therefore, for future designs a higher focus has to be put on the modeling of the IF connection. By using a load-pull analysis and an optimum termination for the fundamental and its harmonics, this effect might be used to reduce the necessary LO power even further.

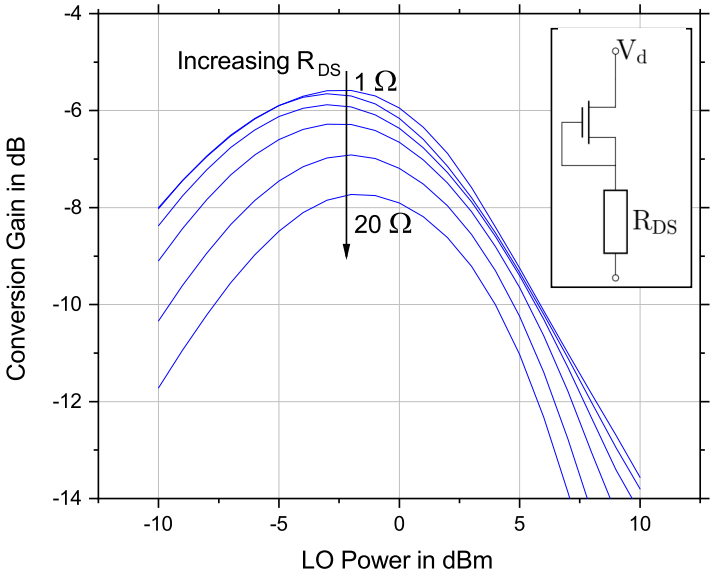


Figure 5.17.: Simulated conversion gain of the mixer AL1 versus the LO power for different serial resistances. The simplified schematic of the configuration with the serial resistor is shown in the inlet.

5.1.1.4. Influence of the Load

According to Fig. 5.12 the overall conversion gain of the circuits with an active load is lower than with a resistive load. Simulations of the circuits, as shown in Fig. 5.16, did not lead to the same result as the measurement. Since only the load was exchanged and the rest of the circuitry was kept constant, the reason for the deterioration has to be found within the active load transistor.
It was observed that the drain current decreased by around 15% by employing the active load both for the ICC and the SCC version. The active load was designed in order to maintain the same DC drain current in the active load dual-gate mixer as it was before in the resistive load version. The lower drain current is an indicator that the channel resistance of the active load, R_{DS}, is different to the simulation. A higher resistance also leads to a larger voltage drop over the active load and a lower drain voltage supplying the dual-gate mixer. To model this effect and to verify the assumption a serial resistor was introduced in the drain supply path. The resulting plot is shown in Fig. 5.17.
Although this is just a first order approximation it reproduces the effect from Fig. 5.12 quite well. While a higher resistance in the drain path could have been compensated by a higher drain voltage, this is not possible for the active load since the drain current is already saturated for the given drain voltage and does not increase linearly any more.

5.1.2. Nonlinear Resistance

5.1.2.1. MMIC Design

The schematic representation of the passive mixer is given in Fig. 5.18.
The center of the resistive mixer is formed by a two-finger transistor with a gate width of 20 µm. The LO is applied to the gate of the transistor. In order to match the LO input to 50 Ω, TL2 - TL5 as well as the capacitors C1 and C2 form an input matching network.

TL3, TL5 and TL6 in combination with C3 decouple the gate voltage supply from the high frequency path.
The IF and the RF are both connected to the drain. TL7 - TL10 with C5 and C4 form both a diplexing and matching network. That means a lowpass is presented looking in the direction of the IF port and a highpass for the RF port. The resistive mixer was designed for a 260 GHz LO frequency and a 50 GHz RF bandwidth from 235 - 285 GHz. The simulated return loss for all three ports is shown in Fig. 5.19.
The reflection coefficient of the LO port is well below −10 dB from 225 to 300 GHz. The return loss of the RF lies below −10 dB for the entire simulated frequency range from 235 to 285 GHz. Although the same problem with matching the IF due to the low frequencies is true for the resistive mixer, the intrinsic impedance presented by the drain of the mixer already shows good matching. Therefore, the IF is well matched (<−10 dB) up to 25 GHz and does not exceed −8 dB even at 35 GHz.
A photograph of the chip is shown in Fig. 5.20. The overall chip size is 1000 µm x 1000 µm. However, this includes large RF and the DC pads. The active chip size is ca. 400 µm x 400 µm.

5.1.2.2. Measurement Results

Fig. 5.21, left, shows the behavior of the conversion gain of the resistive mixer over LO power at an LO frequency of 260 GHz and an RF input power of −30 dBm. The maximum LO power of the measurement setup is not sufficient to drive the mixer in saturation. The highest measured conversion gain lies at −8.4 dB for an LO power of −4 dBm. The simulation shows a very good agreement with the measurement and predicts full saturation at 3 dBm LO input power with a conversion gain of −7.6 dB.
The resistive mixer exhibits a flat conversion gain curve over RF frequency as shown in Fig. 5.21, right. The 3 dB bandwidth exceeds the measurement range at the LSB (220 GHz). The measured 3 dB bandwidth amounts to 65 GHz ranging from 220 to 285 GHz. Fig. 5.21, left, shows the conversion gain versus LO power.
No linearity measurements were conducted for the passive, resistive design. Therefore, only simulations of the mixer will be presented. Fig. 5.22 shows the CG and IF output power versus the RF power. For the simulation the LO power level was set to 0 dBm, the LO frequency was 260 GHz and the RF 261 GHz which results in an IF of 1 GHz.

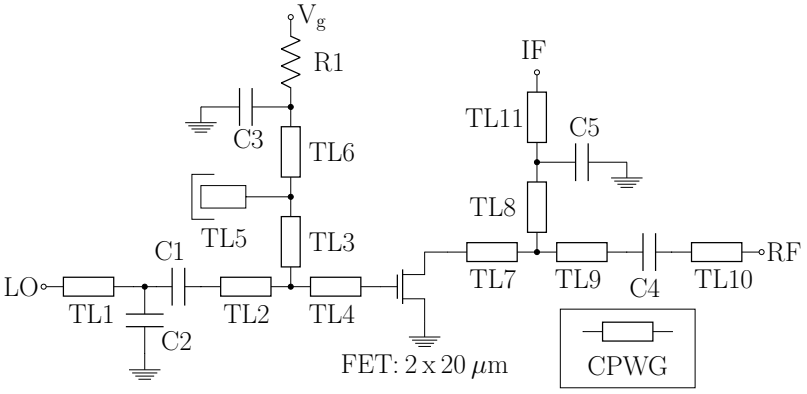


Figure 5.18.: The simplified schematic of the resistive down-converter.

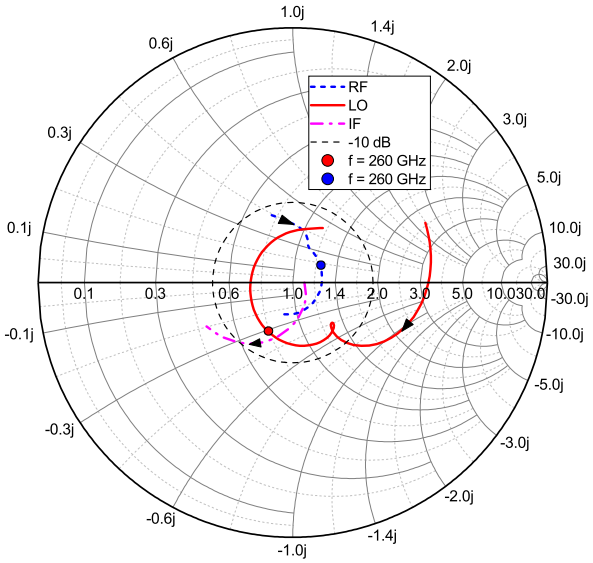


Figure 5.19.: Simulated port matching for LO (200 - 300 GHz), RF (200 - 300 GHz) and IF (DC - 35 GHz). In dashed black the -10 dB-circle as reference.

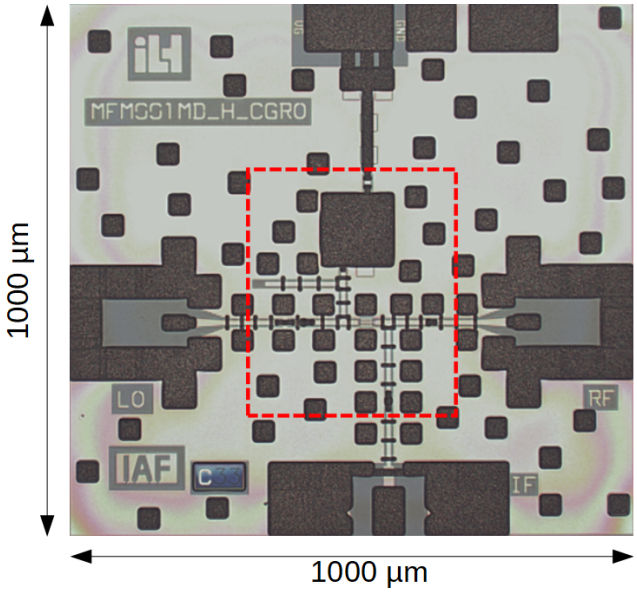


Figure 5.20.: Chip photograph of the resistive mixer. The size of the chip is 1000 µm x 1000 µm with an active area of 400 µm x 400 µm (dashed red).

The input-referred 1-dB compression point (IP_{1dB}) is found at 3 dBm. With a conversion gain of −9 dB an output-referred 1-dB compression point (OP_{1dB}) of −6 dBm is calculated.

5.1.2.3. Comparison Between Active Dual-Gate and Resistive Architecture

The content presented in this section has already been published in [2].
To generate the local oscillator signal in H-band usually frequency multiplier MMICs are used. A single stage frequency multiplier by two or three as proposed in [4] would be sufficient to drive the active mixer, RL1, and still have a higher conversion gain as the resistive mixer in saturation requiring 3 dBm of LO power as can be seen in Fig. 5.21. For the resistive mixer an

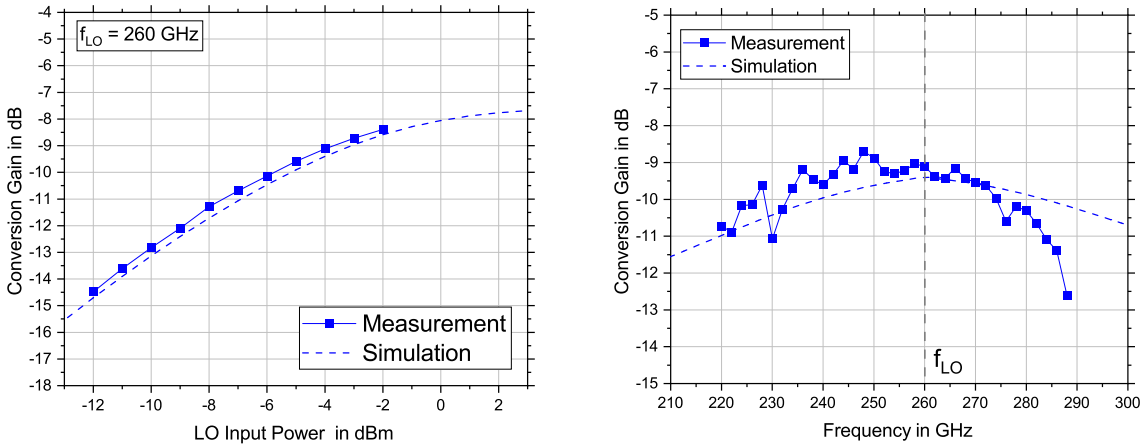


Figure 5.21.: Left: The simulated (dashed) and measured (solid) conversion gain of the resistive mixer versus LO input power (left) at an LO frequency of 260 GHz and an RF of 261 GHz. Right: The conversion gain (CG) over RF frequency at an LO power of −2 dBm, an LO frequency of 260 GHz. The RF power was set to −30 dBm in both cases.

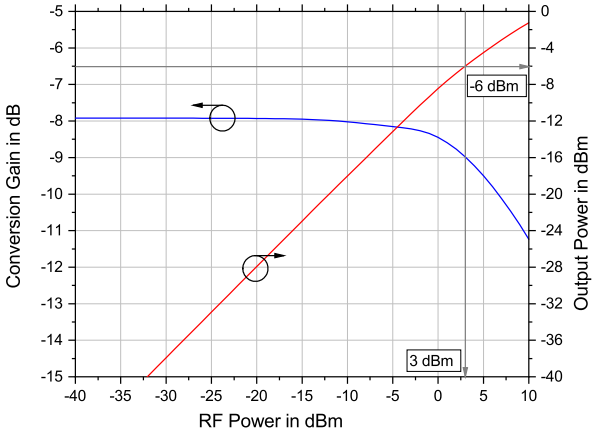


Figure 5.22.: The simulated conversion gain and output power of the resistive down-converter in dependency of the RF power at an LO frequency and power of 260 GHz and −2 dBm and an RF of 261 GHz.

additional amplification stage has to be integrated to generate the necessary LO power. The advantage of a low necessary LO power of the active mixer becomes even more impressive for more complex systems, like communication receivers, where several mixer cells are used in parallel for quadrature modulation and demodulation, and in balanced designs.
For two parallel stages a nominally 3 dB higher LO power is necessary and for four parallel even 6 dB, excluding the losses of the couplers which cannot be neglected in the mmW regime. In total, this leads to a need for large buffer stages following the frequency multiplication to drive the mixer stage, as for example presented in [5] and [6]. These drivers can occupy up to half the chip space of the entire receiver. Additionally, the buffer amplifier not only adds length to the overall chip size but might also increase its width since transistors have to be parallelized in order to achieve high output power. Altogether, large chip sizes and extreme aspect ratios lead to challenges in circuit design and the problems in mechanical chip handling and packaging as described for example in [Dix05, TLW+17].
Thus, replacing the resistive mixer in a receiver/transmitter and therefore getting rid of the

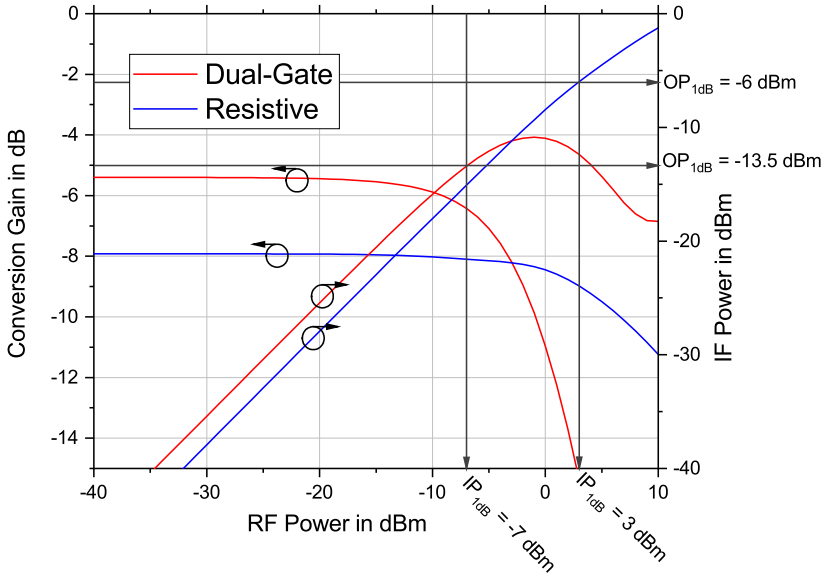


Figure 5.23.: Simulated conversion gain and IF output in dependency of RF power for the active mixer RL1 and the resistive mixer. The input and output referred 1-dB compression point are marked with grey lines in the plot.

large LO buffer stage does not only reduce the chip size and therefore the costs but also increases the efficiency of the chip.
In case of [5] in the same technology the total receiver consumes 295 mW of DC power. 200 mW fall upon the LO buffer amplifier. The active dual-gate mixer with a resistive load needs 55 mW per mixing stage so 110 mW in a quadrature receiver. By employing the mixer "RL1" in the proposed topology of [5] not only the necessary chip area can be cut in half, but also the necessary DC power.
The mixer with an active load consumes even less, only 20 mW. Therefore by changing the load to an active load the overall DC power is only a fifth compared to the resistive approach and still achieving a better conversion gain.
A valid argument for resistive mixers is the high linearity that can be achieved. Since no measurement was conducted on this matter, simulations will be used for this discussion. This approach is not unusual as can be seen later in the state of the art and is due to a lack of high power sources in H-band. For a linearity measurement not only a high LO power must be generated but additionally, a high RF power to saturate the mixer. However, the simulated values of the resistive mixer show a good resemblance to measured values from other publications with similar architectures [HFA+18, GWA+08] which supports the validity of the transistor models and the simulations.
Fig. 5.23 shows the linearity simulations for both the active dual-gate mixer and the resisitve one in one plot for an easier comparison.
For this simulation the version RL1 was chosen but the results do not change drastically for the other versions. Especially the OP_{1dB} remains constant while the IP_{1dB} shifts to higher input powers due the lower conversion gain.
The curves proof the statement of a higher linearity of the resistive down-converter. When the resistive mixer is driven in saturation with an LO power of 3 dBm, the achieved IP_{1dB} is 3 dBm, leading to a OP_{1dB} of -6 dBm.

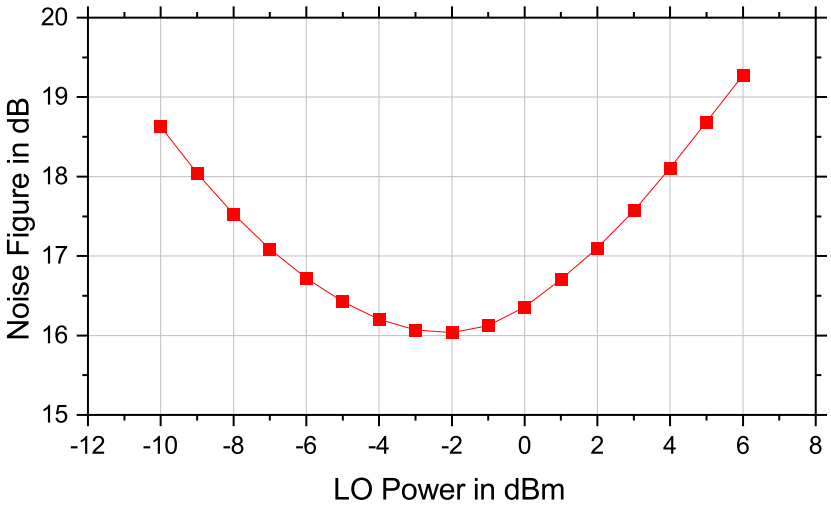


Figure 5.24.: Simulated single sideband noise figure of the mixer AL1. The NF was evaluated at the IF output at 1 GHz which corresponds to the LO and RF input frequencies of 240 GHz and 241 GHz, respectively.

The corresponding OP_{1dB} of the dual-gate mixer lies 7.5 dB below that at -13.5 dBm which corresponds to a IP_{1dB} of -7 dBm.
However, for communication receivers the prerequisites of linearity are in general more relaxed. In a transmitter the input signal is generated in baseband where high power levels are easy to achieve. In contrast, transmitted output powers in H-band are generally low as already explained in the introduction. Secondly, the large free space path loss reduces the RF power even further. Therefore, the resulting RF-input power levels, which need to be handled by the receiver, are typically very low.
Additionally, in a communication receiver the RF input signal has to be further distributed to the I and Q channel. Assuming an ideal power divider, the power per mixer cell is hereby reduced again by 3 dB. By this, the overall IP_{1dB} increases by 3 dB. Therefore an I/Q receiver with the presented active mixer and a 20 dB LNA still operates in a 10 dB back-off from the IP_{1dB} for a high input power of up to -34 dBm. This power corresponds to the received power given in [DRM+17] for an electronic transmitter with an output power of -7 dBm, operating at 300 GHz, transmitting over 0.5 m using a QPSK modulation format.
In case of systems with high receive power, for example radar systems, the lower linearity might be a concern and the resistive mixer is clearly the better choice.
Simulation showed, that the noise figure of the dual-gate mixer employing an active load is around 16 dB. This is 6 dB higher than the NF of its passive, resistive counterpart. The simulation of the single sideband NF versus the LO power is shown in Fig. 5.24. The behavior of the noise figure clearly follows the conversion gain curve. Assuming an approximately constant noise contribution of the transistors and the passive components, increasing the signal level at the output translates directly into an improvement of the NF. As can be seen in Fig. 5.24, the lowest NF is achieved where the conversion gain is at its maximum.
To improve the overall system noise figure LNAs are used. But, due to the lower linearity, the applicable gain is limited. Fig. 5.25 shows the contribution of the mixer noise figure at maximum conversion gain to the total receiver noise figure. The influence is calculated using

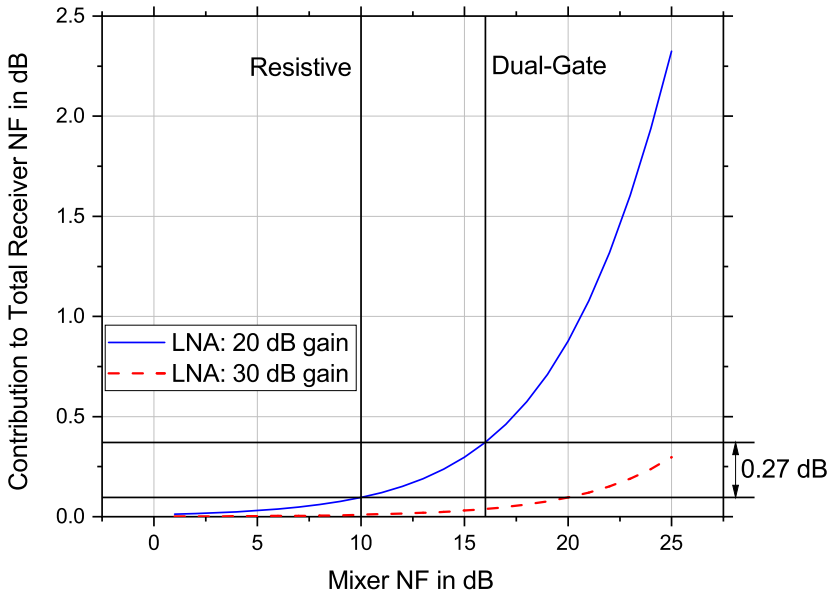


Figure 5.25.: Contribution of the mixer NF to the total receiver noise figure in dependence of the latter for two different LNAs with 20 and 30 dB gain and a 6.5 dB noise figure.

Friis' formula for noise of cascaded stages,

$$NF|_{dB} = 10 \cdot \log_{10}(F_1 + \frac{F_2 - 1}{G_1}) \tag{5.2}$$

The first term, F_1, is the contribution of the LNA to the overall noise figure. The second term reflects the influence of the mixer noise, F_2. Two LNA versions with a different gain, G_1, of 20 and 30 dB were simulated. For both a NF of 6.5 dB was assumed which is a state-of-the-art value for InGaAs-mHEMT MMICs in H-band [TLW+17].
Especially the difference between the 10 dB and the 16 dB down-converter noise figure is of interest. In simulation the load has only a very small influence on the noise of the active mixer. The delta in NF for the active and the resistive mixer is only 0.3 dB for the 20 dB LNA and even lower, 0.1 dB for $G_1 = 30$ dB. From these results it can be concluded, that the higher noise figure of the presented active mixer will have a neglectable impact on the overall noise figure of a typical receiver, at least in this particular technology.

5.1.3. Summary and Comparison to the State of the Art

In this chapter two architectures for down-converter in H-band were presented. Four versions of the active dual-gate down-converter were fabricated and the measurement results discussed. They differ in the decoupling of the IF path from drain voltage supply, an active and a passive load were employed and in the layout of the conversion cell, an integrated and a separated transistor layout. All circuits were characterized regarding necessary LO drive power, RF bandwidth and linearity and a detailed comparison of these two architectures was conducted in the subsequent section. The active dual-gate mixers exhibit a good conversion gain at low LO powers. This relaxes the requirements for the overall receiver design, since large amplifier stages are not necessary anymore. On the downside, the noise figure and the linearity are worse than for the passive, resistive FET mixer. A simple use case demonstrated, that the

higher noise figure (NF) can be easily compensated by an low-nose amplifier (LNA), but the linearity remains an issue. Especially for systems were a high RF input power is expected, the resistive architecture is the frequency converter architecture of choice. In summary, a down-converter design should be carefully selected depending on the target application and system and the expected power levels.
An overview of how the presented down-converters perform in comparison to state-of-the art mixers is shown in Table 5.3.
Unfortunately, for systems where the down-converter was integrated with amplifiers, not all figures of merit could be extracted or were given by the authors which makes a fair comparison hard to achieve. To avoid confusion, the given RF bandwidth is the bandwidth for a fixed LO with a swept RF frequency, compare Fig. 5.14 and 5.13, not a swept LO with a fixed resulting IF. For a homodyne communication system this bandwidth limits the overall possible data bandwidth and is therefore considered of more interest.
Single stage passive mixers for H-band are reported in [HFA+18] and [GWA+08]. The resistive mixer presented in this work outperforms these in terms of conversion gain, bandwidth and necessary LO power.
Even with a lower bandwidth than the presented resistive mixer, the active dual-gate mixers, RL1, RL2 and AL1, exhibit a higher bandwidth than the cited passive state of the art at a lower LO input power.
Active mixers are presented in [SKA+14], [RGS+18], [AFAS17] and [EAK+17]. The conversion gain reached by [RGS+18] and [SKA+14] is not only lower compared to the presented mixers but also the reached RF bandwidth of these circuits is limited to 12 GHz and 32 GHz. Neither a statement on linearity nor on noise figure was given in these publications. [AFAS17] and [EAK+17] present a high conversion gain at a good LO input power. However, both employ additional IF amplification without stating any gain partitioning for the stages. Unfortunately, [AFAS17] gives only a bandwidth for a swept LO with a fixed IF because the targeted application is radar. The circuit in [EAK+17] has a bandwidth of 55 GHz and is therefore slightly more broadband than the presented active circuits.
In terms of compression the presented resistive mixer performs the best. The presented active mixers are in the same range as the state of the art or slightly better.
Please note, that the DC power consumption in Table 5.3 always refers to the full topology. This might include several additional stages for LO generation which increase the overall necessary DC power. The power dissipation for a single frequency conversion stage is added in brackets if published in the reference. Since a fair comparison is hardly possible in these cases, the values for the fully integrated circuits are given for the sake of completeness and not for a comparison.

Table 5.3.: Comparison of state-of-the-art H-band mixers.

Ref.	RF BW / GHz	f_{LO} / GHz	CG / dB	P_{LO} / dBm	IP_{1dB} / dBm	OP_{1dB} / dBm	DC Power /mW	Topology	Technology
[GWA+08]	N/A	209	-8.7	1.5	0[1]	-10[2]	0	resistive mixer	100 nm mHEMT
[HFA+18]	30	270	-15	5	-1	-16	0	resistive mixer	80 nm InP-HEMT
[HKT+17]	33	290	-18	2	N/A	N/A	416[6]	buffer + x3 + resistive mixer	40 nm CMOS
[SKA+14]	30	300	-15	-5	N/A	N/A	N/A	half Gilbert cell mixer	250 nm InP HBT
[RGS+18]	12 (IF BW)	240	8[3]	5	N/A	N/A	915[6] (30.4[7])	x16 + buffer + I/Q-mixer + antenna + BB amp	130 nm SiGe HBT
[AFAS17]	N/A	240	11[3]	-16	-7[4]	3[2]	160[6]	LO amp + SH[5] Gilbert cell + IF buffer	130 nm SiGe BiCMOS
[EAK+17]	55	240	13[3]	-10	-12[4]	0[2]	500[6]	x4 + x2 + LO amp + Gilbert cell + BB amp	130 nm SiGe BiCMOS
This work									
RL1/RL2	52/38	240	-5.6/-4.8	-3/0	-7[4]	-13.5[4]	55/55	dual-gate mixer,	35 nm
	30/25 SSB	220	-3/0	-1			55/55	resistive load	mHEMT
AL1	52	240	-7	-3	-6[4]	-14[4]	20	dual-gate mixer, active load	35 nm mHEMT
Nonlinear Resistance	65	260	-8.4	-1	3[4]	-6[4]	0	resisitve mixer	35 nm mHEMT

[1]operating as up-converter, [2]calculated from IP_{1dB} and CG, [3]including IF buffers, [4]simulated, [5]subharmonic [6]total power consumption of full topology, [7]halved power consumption of I/Q down-conversion stage

5.2. Up-Converter

5.2.1. Gate-Pumped Transconductance

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5.2.1.1. MMIC Design

In a transconductance mixer, the nonlinearity used for mixing is the transconductance, g_m of the transistor. The FET operates in a common-source (CS) configuration. In general there are two ways to vary g_m, by applying a large signal to the gate or the drain of the circuit. The design presented in this work will be of the first kind, a gate-pumped transconductance mixer in an up-conversion configuration. Therefore, the large signal, the LO, and the IF are fed to the gate of the mixer and the desired RF is extracted at the drain.
The simplified schematic of the mixer is shown in Fig. 5.26.
The nonlinear component of the up-converter is the transistor. In this design a two-finger transistor with a gate width of 18 µm was chosen. The transistor determines the necessary LO power to saturate the mixer and was designed to operate at an input power of 7 dBm as shown in more detail in chapter 5.2.1.2. Both, the LO and the IF signals are fed to the MMIC separately and combined on-chip. The combined signal is then applied to the gate of the mixer - hence the nomenclature of a gate-pumped mixer. The gate bias is connected via a resistor, R1, to the IF path. The resistor assures the decoupling of DC and IF and furthermore increases the stability of the circuit. To decouple the LO path from DC a capacitor, C1, is used.
The transistor is biased slightly above the threshold voltage at $-0.1\,\mathrm{V}$. The LO varies the transconductance by changing the voltage at the gate and hereby generates intermodulation products between LO and IF at the drain of the transistor. Even small changes lead to changes in the transconductance and therefore this design is well suited for applications where LO power is hard to generate. TL1 - TL7 form the input matching network and decouple the high frequency LO from the baseband IF. At the output the drain bias path is decoupled from the RF path via TL9 and the capacitor C4 and C5. TL8 to TL12 are employed to match

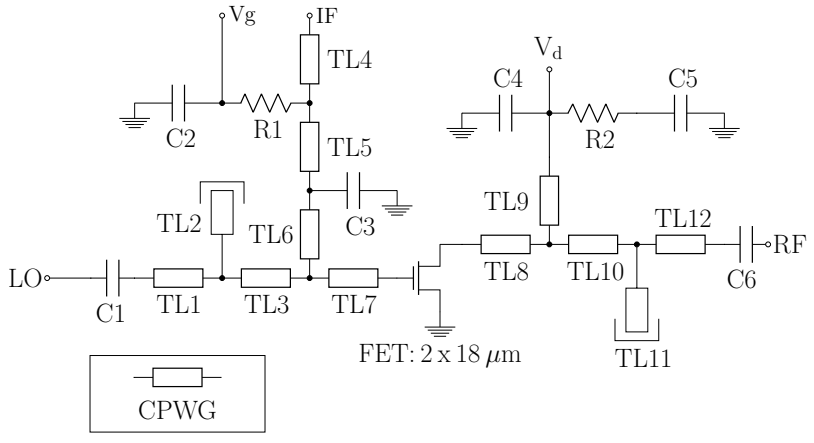

Figure 5.26.: The simplified schematic of the gate-pumped transconductance up-converter.

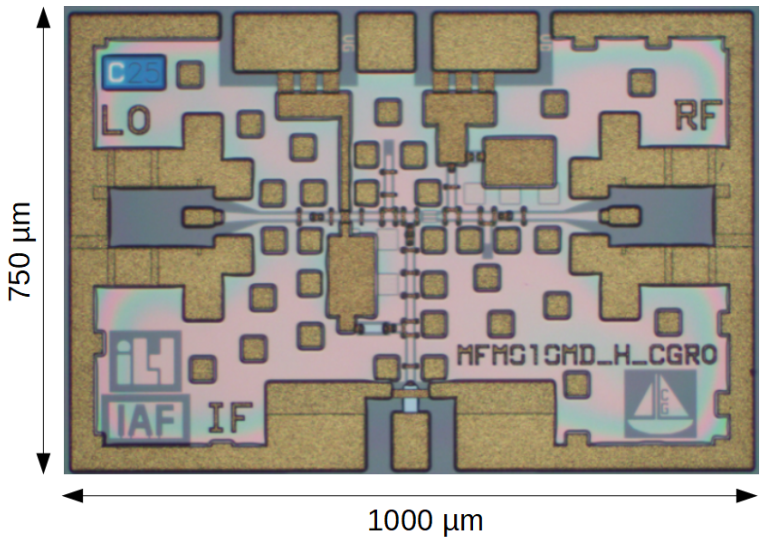

Figure 5.27.: A chip photograph of the active up-converter. Chip size is 1000 µm x 750 µm including the large pads for improved on-wafer measurement.

the RF output to 50 Ω in the desired operating range from 270 to 320 GHz. All transmission lines in the circuit are implemented as grounded coplanar waveguides. C6 decouples the RF output from the drain bias.
Fig. 5.27 shows the chip photograph of the up-converter. The chip size is 1000 µm x 750 µm including large pads for improved on-wafer measurement. The active area of the chip, the area without RF and DC pads, amounts to 300 µm x 300 µm. The overall power consumption of the circuit is 5 mW.

5.2.1.2. Measurement Results

A sweep of LO input power from −14 dBm to the maximum output power of the power amplifier stage of −3 dBm was performed. The LO frequency was set to 300 GHz and the IF frequency was kept constant at 100 MHz at a power level of −20 dBm. The results of conversion gain of the desired intermodulation products, $f_{RF} = f_{LO} + f_{IF}$ and $f_{RF} = f_{LO} - f_{IF}$ versus LO input power are shown in Fig. 5.28.
Additionally the simulation results are depicted in the same graph. As mentioned the circuit was designed to saturate at 7 dBm input power which is achieved in the simulation. For the available measurement power range the mixer is still operating in the linear region but shows a good correspondence to the simulation with a delta of 1 dB. Already at the low LO input power of −3 dBm a very good conversion of −6 dB is achieved. This value exceeds already the maximum conversion gain, typically −8 dB for the same technology and around −15 dB in InP HEMT technology [HFA+18] reached by comparable passive mixers in this frequency range in saturation. Here, the active mixer is not yet saturated and according to the simulation the conversion gain continues to increase for higher LO power levels. The power consumption at a LO input power of −3 dBm is only 5 mW.
In Fig. 5.29 the conversion gain of the presented mixer is plotted versus the output frequency. The LO power was set to the maximum possible value of −3 dBm. The IF power was kept low at −20 dBm to assure linear operation. For the measured frequencies from 270 to 313 GHz a flat conversion gain was achieved. The 3 dB bandwidth exceeds the measurement range.

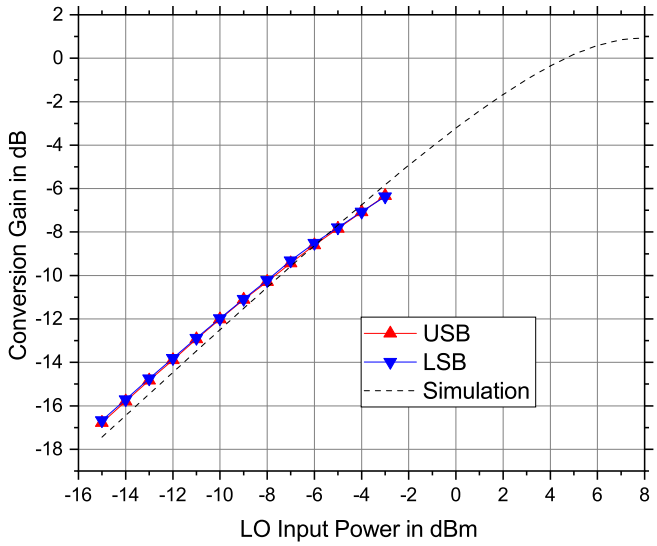

Figure 5.28.: Conversion gain of the mixer in dependency of the LO input power at an IF frequency of 100 MHz, an IF power of −20 dBm at a LO frequency of 300 GHz.

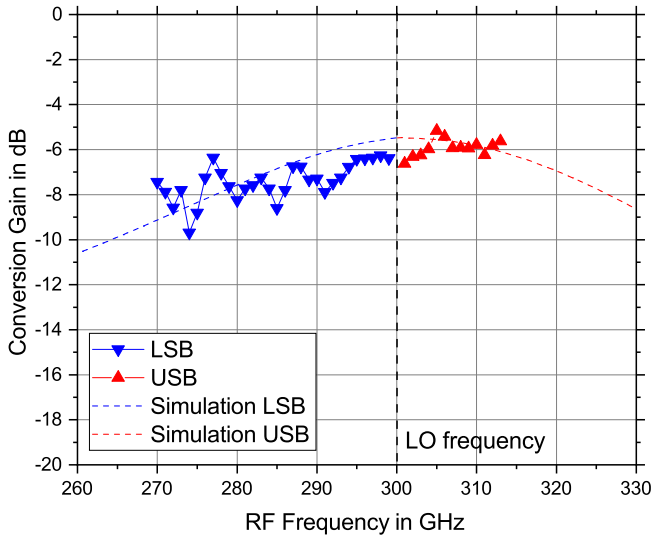

Figure 5.29.: Conversion gain of the upper sideband and lower sideband of the mixer versus the corresponding RF frequency at a LO power of −3 dBm, an IF power of −20 dBm at 300 GHz LO frequency.

To complete the fundamental characterization of the mixer the linearity with respect to the IF input power was measured. The results are shown in Fig. 5.30.
For this measurement the IF frequency was kept constant at 100 MHz and the LO power was set to −3 dBm. The mixer starts to saturate at −20 dBm and reaches its IP_{1dB} at −12 dBm. The maximum output power of the mixer was −15 dBm at −2 dBm input power. Especially for modulations including amplitude modulation like QAM this will lead to distortions in the data signal and increases the error vector magnitude and bit error rate. If referred to the output RF power, the OP_{1dB} is at −19 dBm which is comparable to the state of the art of passive mixers in saturation as will be shown at the end of this chapter. For higher LO input power the conversions gain will improve further since the mixer is not yet saturated at −3 dBm input power and therefore also the OP_{1dB} increases which then outperforms the passive devices.

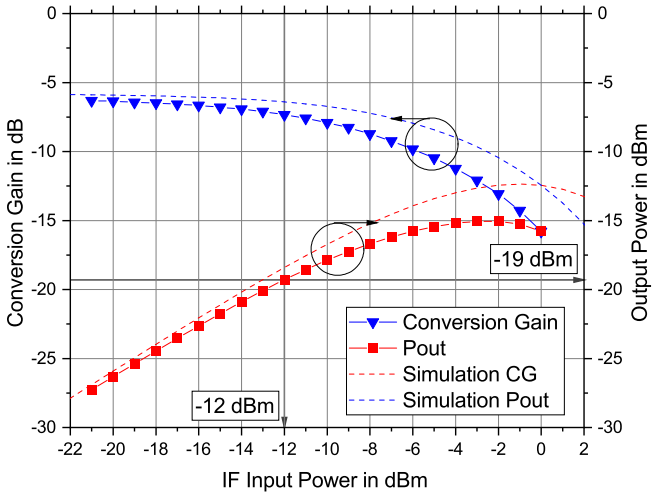

Figure 5.30.: Conversion gain and output power of the mixer in dependency of the IF input power with the 1-dB compression point.

5.2.2. Dual-Gate

5.2.2.1. MMIC Design

The dual-gate mixer as presented in chapter 5.1 can also be used as an up-converter after applying some modifications. Fig. 5.31 shows a schematic of the dual-gate up-converter. Again two versions of the up-converter were designed. One with an integrated and one with a separated conversion cell layout. Although the schematic is similar to the schematic of the down-converter, several major differences have to be pointed out. First of all, the input IF and RF ports were swapped. The IF is now fed to the gate of T2 and the RF is extracted at the drain. That means, that the function of the ports stays the same: The gates represent the input ports and the drain of T1 the output. With this exchange, the need for a resistive

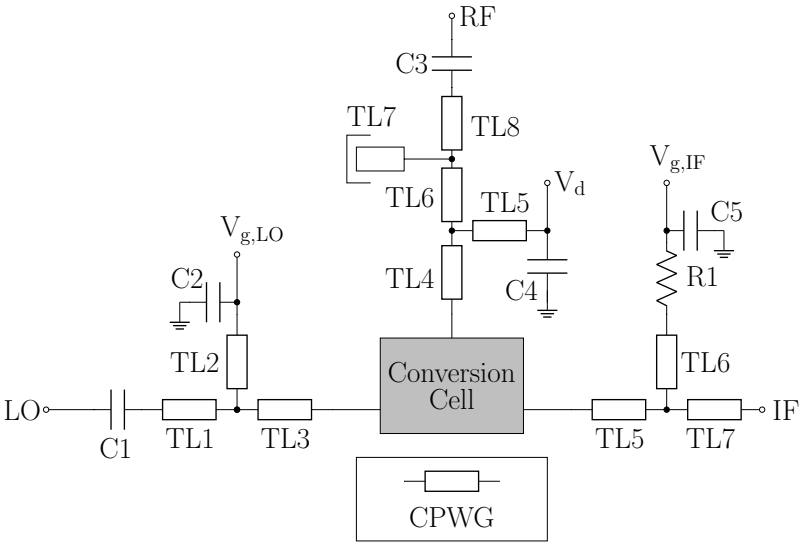

Figure 5.31.: The simplified schematic of the dual-gate up-converter. The place-holder "conversion cell" is replaced by a separated or integrated transistor layout as depicted in Fig. 5.2 in chapter 5.1

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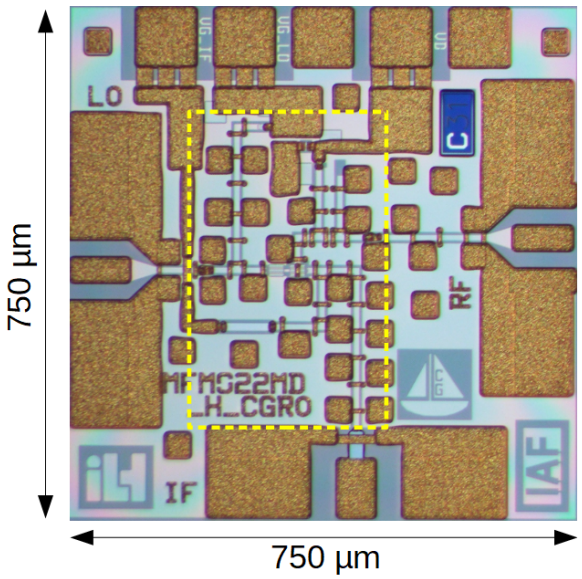

Figure 5.32.: Chip photograph of the active dual-gate up-conversion mixer. The size of the chip is 750 µm x 750 µm with an active area of 260 µm x 400 µm (dashed yellow).

or an active load to decouple the signal from the DC in the drain path is obsolete. The decoupling can be achieved by a conventional quarter wavelength transmission line, TL5, in combination with a parallel capacitor, C4. Additionally a blocking capacitor, C3, can be introduced on-chip to prevent a DC current from entering the RF path. On the other hand however, the blocking capacitor in the gate path of T2 has to be removed, since it presents a high-pass filter and it would distort the down-converted signal strongly. The implementation of an off-chip DC block with a passband as close to zero as possible is the preferred solution here. Additionally, the gate voltage has to be decoupled from the signal path. However, in the gate path, such a decoupling is much easier to establish than in the drain. Due to the low gate current flow, simply a large resistor of several hundreds of Ohms, R1, can be placed in the gate voltage path.
The remaining components have the same functionality as already described in chapter 5.1. C1 blocks the gate voltage of T1. TL1 to TL3 and TL4 to TL8 form an input respectively an output matching network. Where TL2 in combination with C2 decouple the signal path from the voltage path.
Correspondingly to the down-converter version, TL4 is only a CPWG for the SCC version. For the ICC version it is a combination of an airbridge with a CPWG. However, these differences were already discussed in detail in chapter 5.1.
The chip is designed for an LO frequency of 240 GHz, an IF frequency range from 0 to 30 GHz and the corresponding RF from 210 to 270 GHz. The drain voltage is 1 V and the optimum gate bias according to simulation is $\mathrm{V_{g,LO}} = 0.05\mathrm{V}$ and $\mathrm{V_{g,IF}} = 0.15\mathrm{V}$. The gate width of both T1 and T2 is 19 µm.
Fig. 5.32 shows the chip photograph of the active dual-gate up-converter.
The chip size is 750 µm x 750 µm. The active area, the area excluding the pads, is marked with a dashed yellow rectangle and measures 260 µm x 400 µm. The overall DC power consumption of both versions of the circuit amounts to 8 mW.

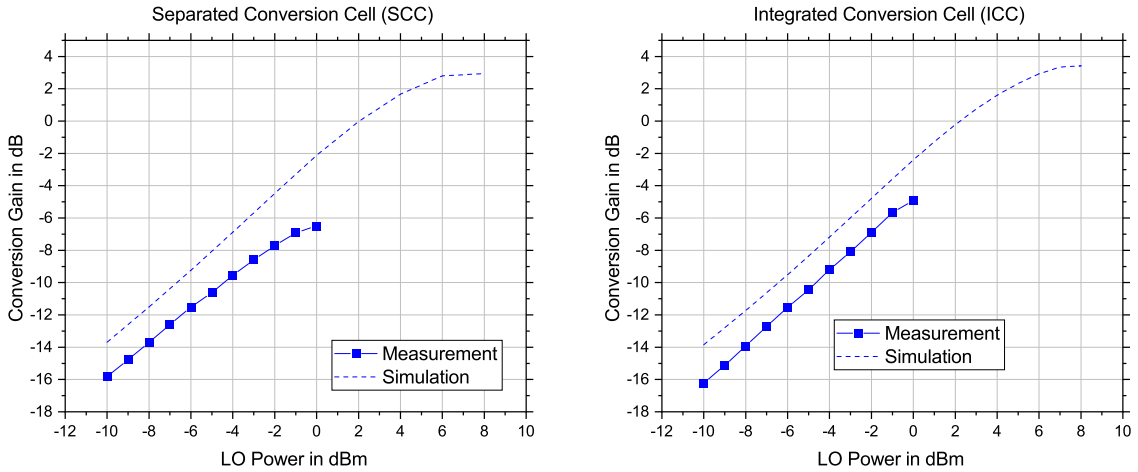

Figure 5.33.: Measured and simulated conversion gain of the two versions of the active dual-gate up-converter versus LO power at an IF power of −20 dBm, an IF frequency of 100 MHz and an LO frequency of 240 GHz.

5.2.2.2. Measurement Results

Fig. 5.33 shows the conversion gain versus the LO power for both versions of the active dual-gate up-converter. The IF frequency was set to 100 MHz and the IF power to −20 dBm to ensure linear operation. The LO frequency was kept at 240 GHz.
In both measurements the conversion gain deviates from the simulated one. Although it appears as if the SCC version, Fig. 5.33, left, deviates more than the ICC version, Fig. 5.33, right. It can be seen later, that this effect is increased by a ripple on the measurement. If another frequency would have been chosen, e.g. 1 GHz, the curves would look more alike.
Both curves start to saturate earlier than the simulation. At 0 dBm, the maximum available power in the measurement setup, a flattening has already set in, whereas the simulation shows a similar behavior not until an LO power level of 6 dBm.
For further measurements the maximum power of 0 dBm was chosen. The frequency behavior of the MMIC was determined by setting the LO to 240 GHz, the IF power to −20 dBm, the LO power to 0 dBm and sweeping the IF input frequency from o to 25 GHz. Fig. 5.34 shows the results of that measurement.
The overall conversion gain of the SCC version is around 1 dB lower than that of the ICC version. Both designs exhibit a lower CG than the simulation, which was expected from the LO power sweep. Besides that, the ICC version matches the frequency behavior of the simulation nicely. It shows a very flat gain curve and its 3 dB bandwidth exceeds the measurement bandwidth of 50 GHz. The same is true for the LSB of the SCC version. However, the USB exhibits a much steeper slope than anticipated by the simulation. This deteriorates the 3 dB bandwidth and only 34 GHz were achieved. As already discussed in chapter 5.1.1 the in- and output impedance properties of the ICC and SCC are most likely deviating due to the different conversion cell layout which can lead to a deterioration of the matching that manifests in a reduction of conversion gain. For future designs a greater emphasis has to be put on the exact modeling of the layout to predict behavior like this. Preferably, a full EM simulation of the conversion cell excluding the active part of the transistor should be conducted to extract a more realistic simulation model.
Moreover, as can be seen, both curves are distorted by small measurement ripples. For some

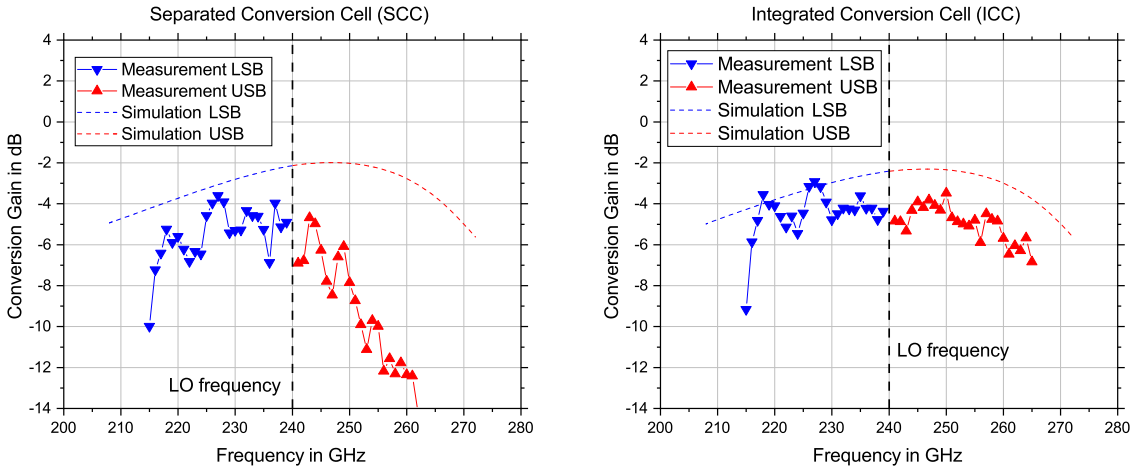

Figure 5.34.: Measured and simulated conversion gain of the two versions of the active dual-gate up-converter versus the IF frequency at an LO power of 0 dBm, an IF power of −20 dBm, and an LO frequency of 240 GHz.

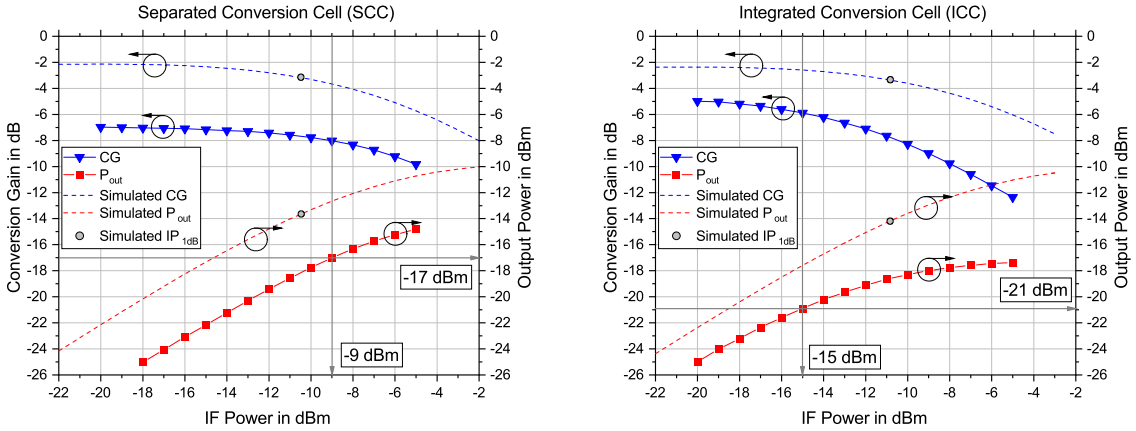

Figure 5.35.: Measured and simulated conversion gain and output power of the two versions of the active dual-gate up-converter in dependency of IF power. The IF frequency is 100 MHz, the LO frequency 240 GHz and the LO power 0 dBm.

points the peak to peak difference calculates to almost 3 dB. A similar behavior was also seen during the measurements of the dual-gate down-converter. As already explained in chapter 5.1.1 the performed calibration is prone to create such ripples due to mismatches between the DuT and the measurement setup. In particular, the frequency of 240.1 GHz lies in a minimum. This increases the difference in the measurement curves in Fig. 5.33 as already mentioned.

Eventually the linearity of both designs was determined. In order to do so, the LO frequency was set to 240 GHz, the LO power to 0 dBm and the IF to 100 MHz. Then, the IF power was swept from -20 to −5 dBm. The results are shown in 5.35.

Again visible for both designs the difference in CG. However, here the SCC version performs better than the ICC version exhibiting an IP_{1dB} of −9 dBm which is higher than the simulated IP_{1dB} at −10.5 dB. The OP_{1dB} is 3 dB lower than simulated at −17 dBm. The ICC version saturates earlier and exhibits an IP_{1dB} of −15 dBm. That corresponds to a OP_{1dB} of −21 dBm. The measured DC power consumption of both designs is very low at around 8 mW.

5.2.3. Differential Pair / Half Gilbert Cell

To evaluate whether it is feasible to use Gilbert cells in the presented InGaAs 35 nm mHEMT technology, as a first step a half Gilbert cell was designed. A full Gilbert can be formed by integrating two half Gilbert cells on one MMIC and connecting them properly. However, for an initial study, there are several advantages of designing a half Gilbert cell first. First of all, the level of complexity is lower. Only one input port, the LO port, is differential. The other input port, in case of an up-converter the IF, is single ended. This simplifies the design and reduces the necessary chip area drastically. Moreover, fewer elements lead to an easier identification of sources of impairments and it will be easier in the future to optimize the circuit accordingly.

5.2.3.1. MMIC Design

Since no measurement setup was available that comprises a way to feed a differential LO signal to the MMIC, a balun was integrated on the MMIC to convert the single ended LO signal to a differential signal. For the balun, a planar version of the Marchand topology was chosen [Mar44]. The original version converts coax to a two-conductor transmission line. The input of the balun forms a $\lambda/2$ open-ended transmission line. The output lines are shorted $\lambda/4$ lines that are coupled to the input line. To increase the coupling these $\lambda/4$ segments were put on both sides of the input line instead of conventionally on one side. The segments are connected via airbridges. Ideally, the output signals are 180° out of phase. A schematic representation and the model used for FEM simulation of the coupler are depicted in Fig. 5.36. Port 1 is the input port and port 2 and 3 are the output ports. The measured

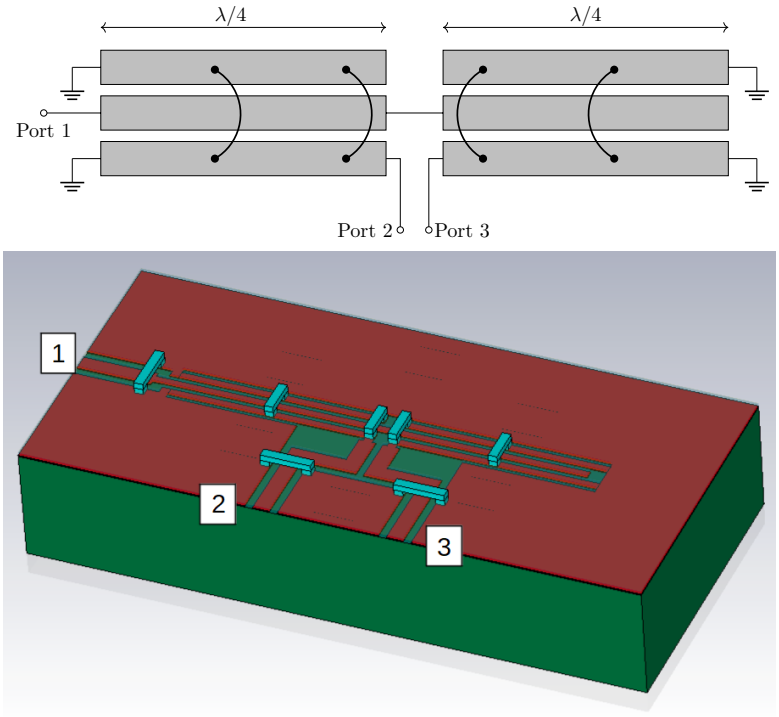

Figure 5.36.: A schematic drawing of a Marchand balun (top) and the corresponding 3D CST model for a finite element method (FEM) simulation (bottom).

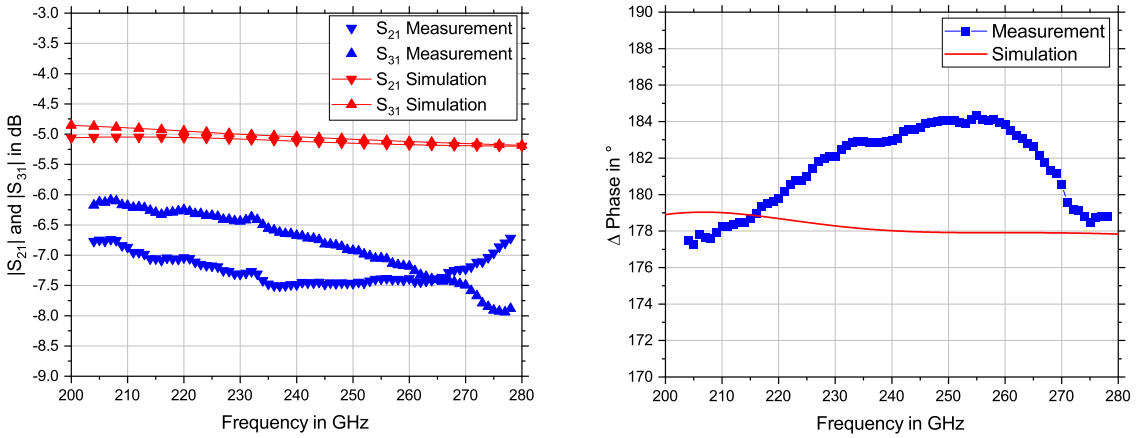

Figure 5.37.: The simulated (red) and measured transmission S-parameters S_{21} and S_{31} of the Marchand balun (left) and the phase difference of the output signals at port 2 and 3.

and simulated transmission S-parameters are depicted in Fig. 5.37, on the left the amplitude and on the right the phase. The Marchand balun is lossier than simulated and at 240 GHz S_{21} is 6.6 dB and S_{31} 7.5 dB. That means the amplitude imbalance is below 1 dB at the frequency of interest. The phase difference between the output ports is met fairly well. At 240 GHz it only shows a 3° deviation from the target value of 180°.
The schematic of the half Gilbert cell is shown in Fig. 5.38.

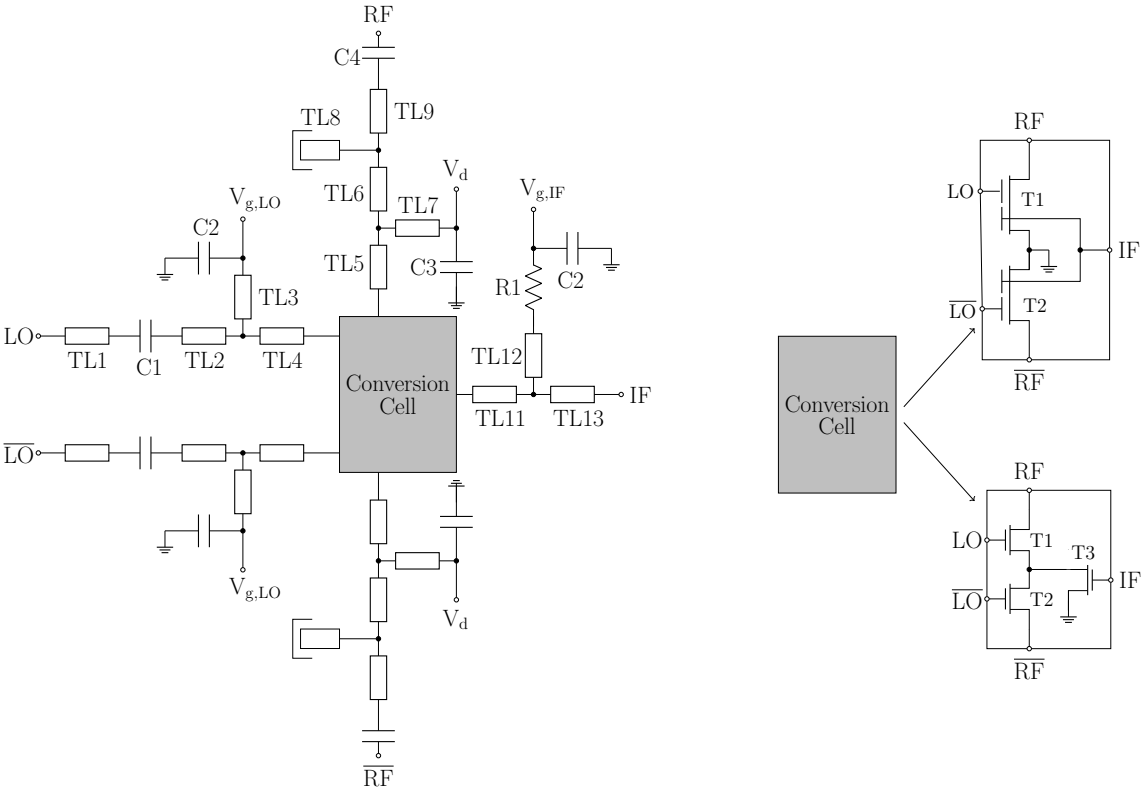

Figure 5.38.: The simplified schematic of the differential FET up-converter (left). Two versions of the mixer were realized, where the place-holder "conversion cell" is replaced by the two different transistor layouts shown on the right.

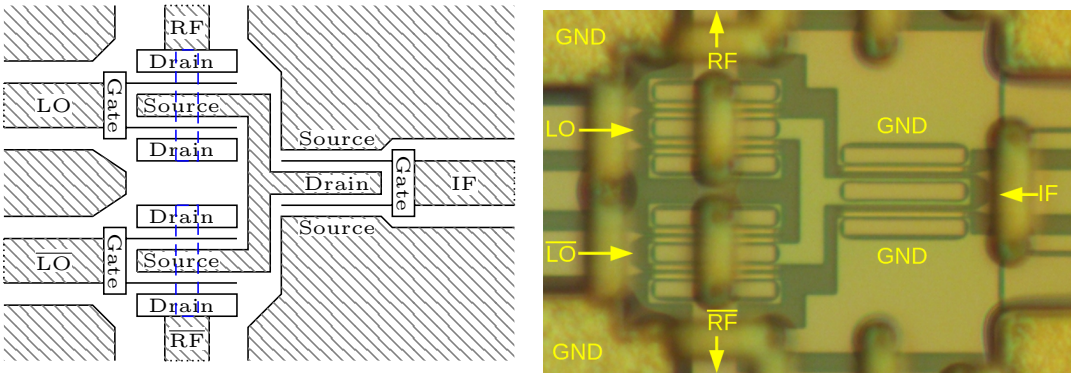

Figure 5.39.: The simplified schematic of the SCC and a magnified photograph of corresponding section of the chip. In dashed blue airbridges that connect the drain ports of the transistors.

Similar to the dual-gate mixer, the active devices, the transistors, are replaced by a "conversion cell" place-holder. Again, two different designs of the conversion cell were produced: a fully integrated transistor cell and a version where the single transistors are well separated. The same nomenclature for the conversion cells as introduced in chapter 5.1.1, ICC and SCC, will also be applied here.
The design for the LO and RF paths is completely symmetrical. Therefore, to improve clarity, only the upper part of the schematic is labeled. The passive elements in the lower part are simply a mirrored version and all the following descriptions apply to them accordingly.
TL2 to TL4 form the input matching network for the LO frequency and TL11 to TL13 for the IF frequency. The output matching at the RF frequencies is done by TL5 to TL9 in combination with an open stub TL8. C1 and C4 are decoupling capacitors, that prevent DC current from flowing into the LO or RF port or vice versa. TL3 in combination with C2, as well as TL7 in combination with C3, establish a decoupling of the high frequency paths from the DC sources by transforming the short represented by the capacitors into an open for the frequency range of operation. The decoupling of the IF signal from the gate voltage $\mathrm{V_{g,IF}}$ is realized by a 300 Ohm resistor. Similar to the dual-gate up-converters an on-chip DC block in the IF path would introduce a high-pass behavior and deteriorate the signal quality. For the proper usage of this MMIC, an external DC block is necessary. With that external DC block, no current flow at the gate is expected and therefore no voltage drop over the resistor. In the version with the separated transistors, the differential LO signal is fed to two transistors, T1 and T2, each with two gate fingers with gate width of 20 µm. The source of these transistors is connected by short piece of transmission line and then connected to the drain of T3. The gate of this transistor represents the input for the IF signal. For clarification a photograph of the transistor cell and its corresponding simplified schematic is shown in Fig. 5.39.
In the integrated version, there is one large transistor cell integrating all three transistors, that were mentioned above. In this case, the gate width of the transistors, to the gate of which the LO signal is connected, is kept the same. The transistor to which the IF is fed, is replaced by a 4-finger FET. Instead of connecting the sources of T1 and T2 and using that as a drain of T3, here, all three transistors share now the same drain and source. To maintain the same total gate width, the gate width of the 4-finger FET has to be halved. However, to achieve the same simulation results, the gate width had to be additionally varied slightly. The gate width of the 4-finger resistor is 11 µm instead of the expected 10 µm and

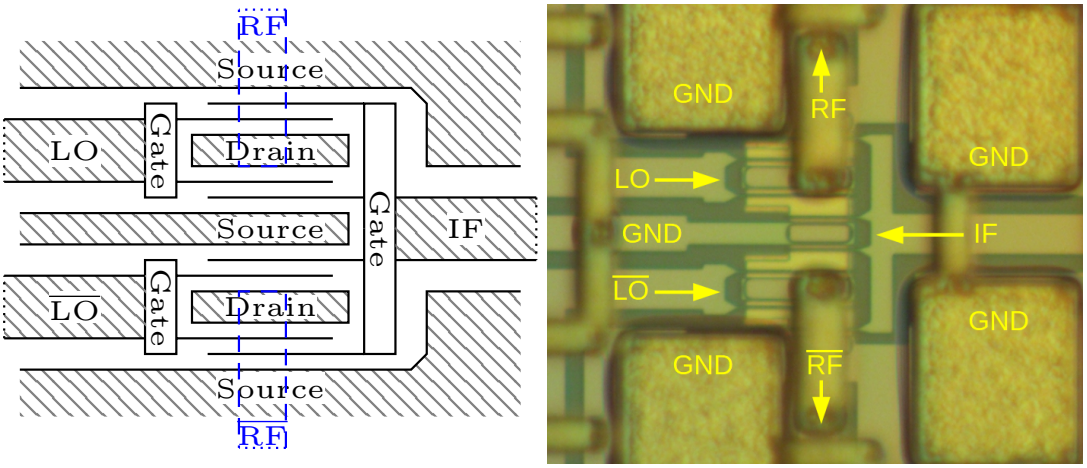

Figure 5.40.: The simplified schematic of the ICC and a magnified photograph of corresponding section of the chip. In dashed blue airbridges that connect the drain ports of the transistors to the transmission lines.

the two finger transistors were shortened by 1 µm to 19 µm A photograph of the transistor cell and its corresponding simplified schematic are shown in Fig. 5.40.
In both versions the bias voltages are the same: $V_{g,LO} = 0.25\,V$, $V_{g,IF} = 0.075\,V$ and $V_d = 1\,V$. Fig. 5.41 shows a chip photograph of the up-conversion MMIC with the integrated transistor cell. The photograph of the corresponding separated mixing cell version can be found in the Annex. The mixing cell and the Marchand balun are marked in the picture. The overall chip size is 1000 µm x 750 µm.

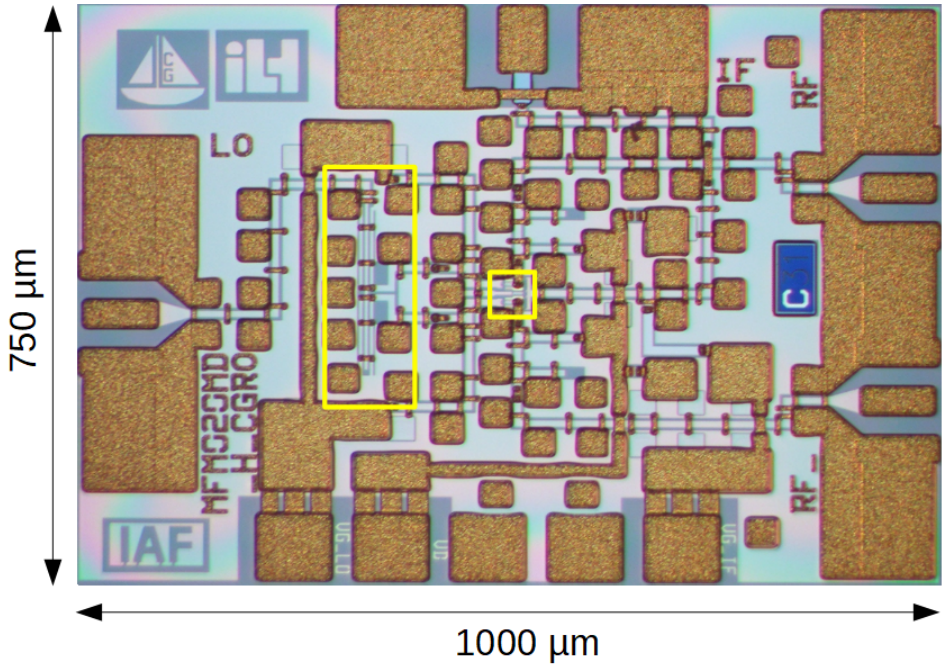

Figure 5.41.: A chip photograph of the ICC version of the half Gilbert cell MMIC. Yellow rectangles mark the positions of the Marchand balun and the conversion cell. The chip size is 1000 µm x 750 µm.

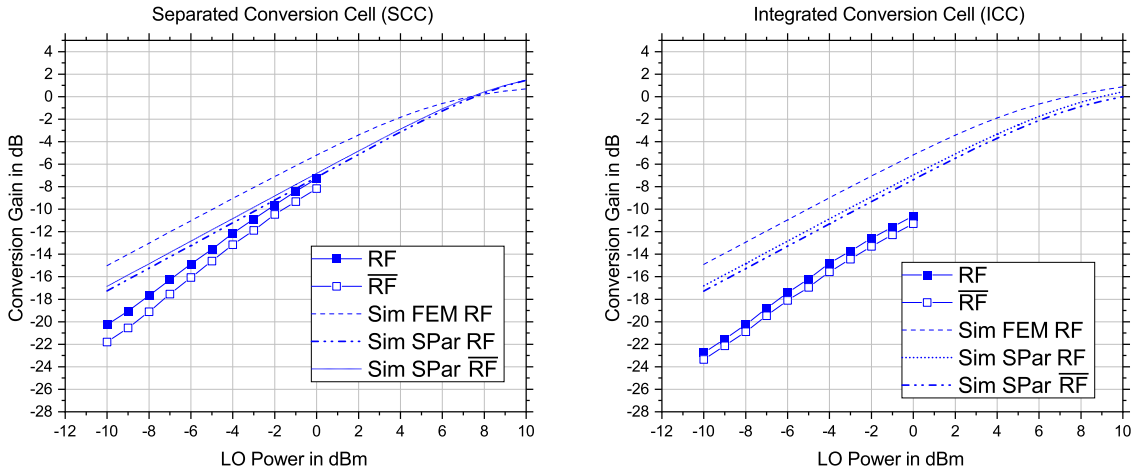

Figure 5.42.: Measured and simulated conversion gain of the two versions of the differential FET up-converter versus LO power at an IF power of −20 dBm, an IF frequency of 1 GHz and an LO frequency of 240 GHz. Simulations were conducted either with the FEM model of the Marchand balun or with the measured S-parameters.

5.2.3.2. Measurement Results

To characterize the half Gilbert cell up-converter three main characteristics were measured: the behavior of conversion gain versus LO power, versus RF frequency and the linearity, hence CG over IF power. The results for the version with the separated mixing cell and the integrated mixing cell are depicted side by side for a better comparison.
The first measurement conducted is the sweep of LO power. The results are shown in Fig. 5.42. The IF frequency is kept constant, as well as the IF power. The LO frequency for all measurements is set to 240 GHz.
The maximum available LO power of the measurement setup is 0 dBm. Neither the version with the integrated transistor cell, ICC, nor with separated mixing cell, SCC, are saturated at this power level. However, especially regarding the losses in the Marchand balun, this comes not as a surprise. When the losses are subtracted from the LO power, the power at the transistor level can be calculated. At the gate of the LO transistor at 240 GHz the power level is −6.6 dBm and at the gate of the $\overline{\mathrm{LO}}$ transistor even lower at −7.5 dBm. Even though, the LO power is very low at the mixing cell, the CG achieved is high. For SCC at the RF port the conversion gain is −7 dB and correspondingly for $\overline{\mathrm{RF}}$ it is slightly below −8 dB. The difference between the two output ports is caused by the amplitude imbalance of the Marchand balun. The total conversion gain, that means adding up the conversion gains of both output ports, calculates to −4.5 dB. This is very high for a mean LO input power of −7 dBm. In Fig. 5.42 two different simulations are shown. Firstly, a simulation using the results of the FEM simulation to model the Marchand balun and secondly, a simulation, where the S-parameters, that were extracted from an on-wafer measurement, were used. The version with the results of the electro-magnetic field simulation is overly optimistic. That roots in the lower losses predicted by the FEM simulation, compare Fig. 5.37. However, taking into account the higher losses, and using the real life measurement data, the simulation and the measurement are well in accordance.
The version with the integrated transistor cell performs less well, although the simulation predicts a very similar behavior. The conversion gain is around 3 dB lower at the maximum

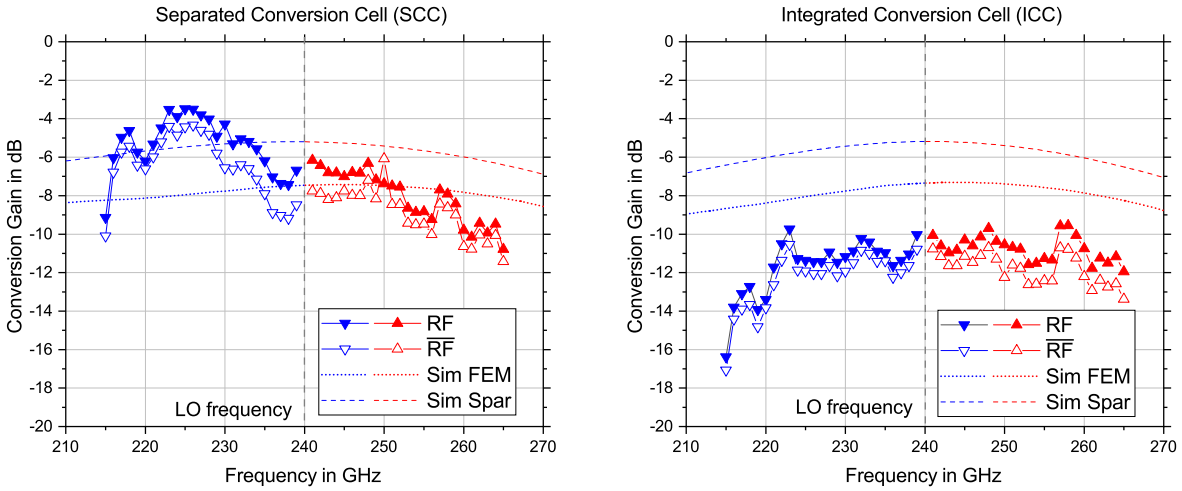

Figure 5.43.: Measured and simulated conversion gain of the two versions of the differential FET up-converter versus the IF frequency at an LO power of 0 dBm, an IF power of −20 dBm and an LO frequency of 240 GHz.

LO power, −10.5 dB at the RF port, and −11.5 dB at the $\overline{\mathrm{RF}}$ port. This combines to a total conversion gain of −8 dB for the ICC version. Although this value is lower than for SCC, it is a good result for the low LO power level at both inputs of the mixing cell.
To evaluate the usable bandwidth of the MMIC, the IF frequency was swept from 0 to 25 GHz. With the 240 GHz LO this translates to an RF frequency ranging from 215 to 265 GHz. The LO power was set to the maximum available value of 0 dBm and the IF power was kept at −20 dBm to ensure a linear mode of operation. The results are depicted in Fig. 5.43.
For SCC the USB matches the simulation very well. However, for the LSB, an unexpected increase in conversion gain occurs. It peaks at 225 GHz with −3.7 dB for the RF output and −4.3 dB, respectively for the $\overline{\mathrm{RF}}$ port. That results in a total peak conversion gain of −0.9 dB.
Taking the peak as reference, the RF 3 dB bandwidth calculates to around 33 GHz. However, if the value closest to the carrier is taken as reference, that means at 239 GHz or 241 GHz, the overall 3 dB bandwidth amounts to 45 GHz.
ICC exhibits a flatter gain curve that is more similar to the simulation. No peaking in the LSB occurs. As already discussed before, the overall conversion gain differs from the simulation by ca. 3 dB. For the USB the gain drop is lower than −3 dB. Therefore, the 3 dB bandwidth exceeds the measurement range and is at least 45 GHz.
To determine the $\mathrm{IP_{1dB}}$ and $\mathrm{OP_{1dB}}$, the IF power has to be swept. In order to do so, the IF and LO frequency were fixed at 1 GHz and 240 GHz, respectively. The LO was set to 0 dBm. The measurement results are given in Fig. 5.44.
Similar to the already presented active up-converters, the linearity differs strongly from the simulation. For SCC an $\mathrm{IP_{1dB}}$ of −16 dBm is deduced. This is 5 dB lower than predicted by simulation. −16 dBm translates to an $\mathrm{OP_{1dB}}$ of −24 dBm at the RF port and −25 dBm at the differential counterpart.
The simulated $\mathrm{IP_{1dB}}$ and $\mathrm{OP_{1dB}}$ for ICC is the same as for SCC. But, the measured $\mathrm{IP_{1dB}}$ increases to −14 dBm. Due to the lower CG this improvement can not translate to the output. Hence, only a $\mathrm{OP_{1dB}}$ of −26 dBm and−27 dBm for the both RF ports were achieved.
To compare the result to a single-ended mixer design, the two measured output powers will be

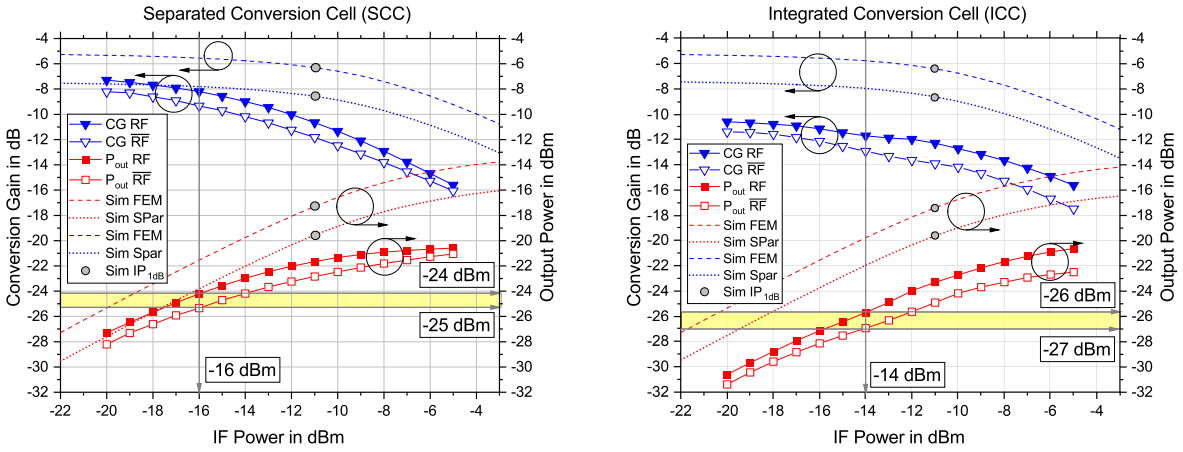

Figure 5.44.: Measured and simulated conversion gain and output power of the two versions of the differential FET up-converter in dependency of IF power. The IF frequency is 1 GHz, the LO frequency 240 GHz and the LO power 0 dBm.

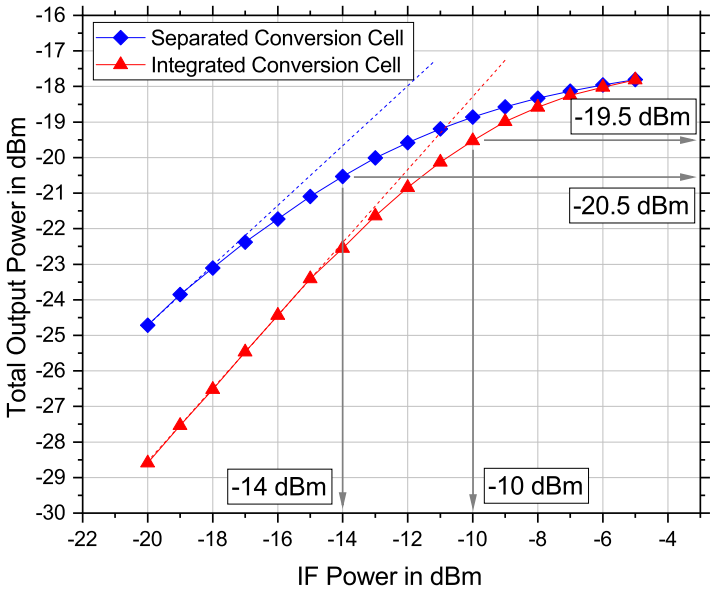

Figure 5.45.: Combined measured output power of the two RF outputs versus the IF input power. The IF frequency is 1 GHz, the LO frequency 240 GHz and the LO power 0 dBm.

combined in phase to a total output power $P_{\text{out,total}} = |P_{\text{out,RF}}| + |P_{\text{out,}\overline{\text{RF}}}|$. From that a new graph can be drawn that shows the total output power versus the IF input power, Fig. 5.45. Using the new plot a combined $\text{IP}_{\text{1dB,total}}$ and $\text{OP}_{\text{1dB,total}}$ can be derived. For the SCC, this is -14 dBm and -20.5 dBm, respectively, for ICC it results in -10 dBm and -19.5 dBm, respectively.

The power consumption of the circuits is 4.8 mW and 3 mW for SCC and ICC.

5.2.4. Nonlinear Resistance

5.2.4.1. MMIC Design

Since the resistive mixer can be used as both up and down-converter, the design of the MMIC is identical with that presented in chapter 5.1. The schematic is depicted in Fig. 5.18.

5.2.4.2. Measurement Results

All measurements of the resistive up-converter were conducted with a fixed LO of 240 GHz. First, the LO power was swept from -16 to 0 dBm and the conversion gain was measured. The IF power was set to −30 dBm and the IF frequency to 1 GHz. The results are shown in Fig. 5.46.
The CG starts to saturate at −4 dBm. At the maximum available LO input power, 0 dBm, it has reached around −10 dB. Overall, the simulation and measurement is well in accordance. However, the simulation starts to saturate slightly later and less strongly. Therefore, in simulation the CG keeps increasing to almost −8 dB at 8 dBm input power.
In comparison with the down-conversion measurement, in up-conversion mode, the mixer exhibits a slightly lower conversion gain and is less efficient especially in low power regimes. For example, at −10 dB LO power, the down-converter shows −13 dB conversion gain, whereas the up-converter version only has a CG of −20 dB at the same power level. Therefore, when designing a resistive mixer, the assumption that the efficiency for both up- and down-conversion is equal, can easily be dismissed. An extra analysis is necessary for both the modes of operation. It can even be useful, to optimize the resistive mixer for the desired operation.
In Fig. 5.47 the conversion gain over RF frequency is plotted.
The LO power was at the maximum available level of 0 dBm and the IF power at −30 dBm. The IF was varied from 0 to 25 GHz resulting in an LSB from 215 to 240 GHz and a corresponding USB from 240 to 265 GHz. The conversion gain curve is very flat over the measurement range. Only at the lower edge, starting at 218 GHz, it starts to decrease. At the maximum frequency, 265 GHz, the conversion gain has only decreased by around 1 dB

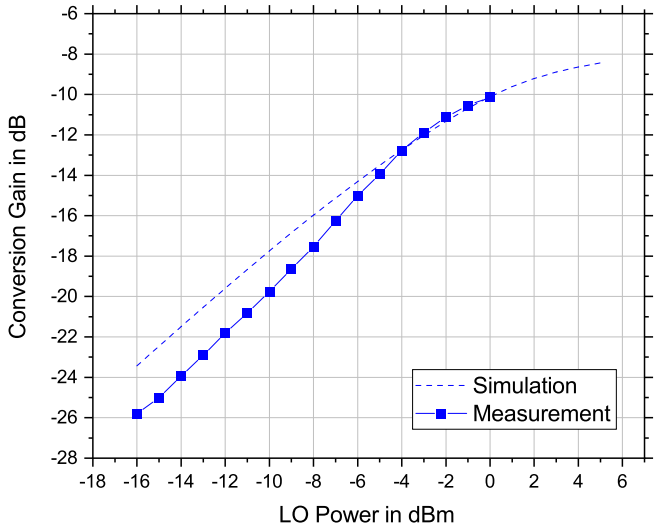

Figure 5.46.: The simulated and measured conversion gain over swept LO power at an RF frequency of 241 GHz. The LOfrequency was set to 240 GHz and the IF input power to −30 dBm.

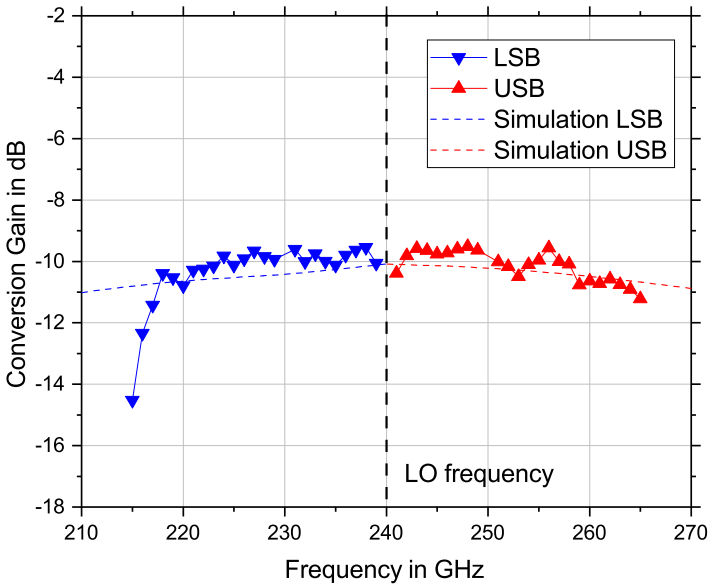

Figure 5.47.: The simulated and measured conversion gain at the resulting RF frequency for a swept IF frequency from 0 to 25 GHz. The LO power was 0 dBm, the LO frequency 240 GHz and the IF power −30 dBm.

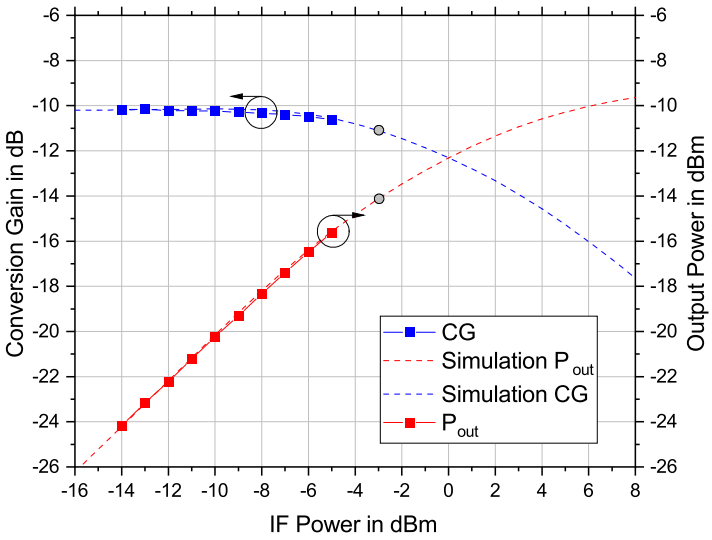

Figure 5.48.: The simulated and measured conversion gain and output power of the resistive up-converter in dependency of the IF power at an LO frequency and power of 240 GHz and 0 dBm and an RF of 241 GHz.

and therefore, the overall bandwidth exceeds the measurement range. That means, the RF bandwidth is larger than 47 GHz.

One big advantage of resistive mixers is their linearity. This can also be seen in Fig. 5.48. For measuring the linearity, the LO power was again 0 dBm, the IF frequency 1 GHz at an LO frequency of 240 GHz. The IF power was swept from −14 dBm to a maximum of −5 dBm. At this point, the IP_{1dB} has not been reached yet. The simulated IP_{1dB} is −3 dBm. Due to the excellent accordance with the measurement, the assumed real IP_{1dB} is the same. An IP_{1dB} of −3 dBm, results in a high OP_{1dB} of −14 dBm.

5.2.5. Summary and Comparison to the State of the Art

In this chapter different architectures for up-conversion mixers were presented: a gate-pumped transconductance mixer, two versions of a dual-gate up-converter and two versions of a half Gilbert cell mixer.
Similar to the dual-gate down-converter, the two variants of the dual-gate up-converter differ in the layout of the conversion cell which is either an integrated or separated transistor cell. The differential FET mixer or half Gilbert cell mixer exhibits two different versions of the conversion cell as well. On the one hand, a full integration of the three transistors in the layout into a single "integrated conversion cell", ICC, was performed. On the other hand, the transistors are spatially separated. Therefore, it was referred to as "separated conversion cell", SCC.
To the author's best knowledge, it is the first time, that both a dual-gate and a half Gilbert cell mixer were presented in that particular technology for the H-band, 220 to 320 GHz.
The design considerations of the up-converters were thoroughly described and measurements of the necessary LO power, the RF bandwidth and the linearity presented. Additionally, these results were compared to the performance predicted by simulation.
The predominant mixer architecture for H-band is the passive mixer. They show an extensive relative bandwidth combined with a high linearity as reported in [HFA+18], [ABM+14] and in this work in section 5.1.2 and 5.2.4. Furthermore the resistive FET mixer is easy to design and therefore its performance is very robust against process and bias point variations. But, to achieve even reasonable conversion loss a high LO drive power is necessary. To generate this high power is a challenge at terahertz frequencies. The herefore necessary additional amplification stages lead to a higher overall power consumption and higher requirement in terms of chip area. But even at reasonable conversion levels the advantage of high linearity is almost negated by the loss which can be seen by examining the OP_{1dB} as depicted in Table 5.4.
Active mixers offer a better conversion gain than the resistive one. At the same LO power level the dual-gate mixers exhibit up to 5 dB more conversion gain while the bandwidth of the ICC version is the highest in Table 5.4 at a very low power consumption of 8 mW.
While consuming only 5 mW, the gate-pumped transconductance mixer shows a large bandwidth as well, more than 42 GHz, and a 5 dB better conversion gain than the resistive mixer. These results were achieved at a low LO power level of only -3 dBm.
Although the two versions of the differential FET mixer do not rank highest on the first sight in any of the categories in Table 5.4, they deserve a closer look. First of all, the measured bandwidth is in a comparable range to the other presented mixers in that work and higher than any of the references [KTA+16, HFA+18, SKA+14, SGS+16, KML+08, ABM+14]. Secondly, only the passive mixer consumes less power. Thirdly, the MMIC is very compact especially since it comprises also a balun and a differential output. And, lastly, because of that, the conversion gain, the LO power level as well as the linearity, have to be considered in a revised manner. Meaning for the conversion gain and the linearity the total output power has to be taken into account and for the LO power level, the losses of the Marchand balun should be de-embedded. Especially for SCC this leads to a higher conversion gain than the other presented up-converters at a considerably lower LO power.
All active up-converters suffer from a reduced linearity compared to the resistive FET mixer. However, the mixers presented in [KTA+16, HFA+18, SKA+14] are operating at similar levels

of linearity. Although [SGS+16] achieves a very good OP_{1dB}, the reason for this is the implementation of an additional amplification stage to boost the output power.
To sum it up, all the presented mixers show a very good overall performance and their figures of merit lie in the same range or outperform the state of the art. Moreover, since this was the first design cycle of these active up-converters, there is definitely room for improvement. The results discussed in the corresponding sections offer not only a good basis for optimization, but also provide a system designer with a good repository to assess which design might suit his needs the best. Fore example, if LO power is scarce, but output power demands are low, the differential FET mixer might be a good choice. Or, if the linearity has to be high, clearly the resistive FET mixer is the way to go.

Table 5.4.: Comparison of state-of-the-art H-band mixers.

Ref.	RF BW / GHz	f_{LO} / GHz	CG / dB	IP_{1dB} / dBm	OP_{1dB} / dBm	P_{LO} / dBm	DC Power /mW	Chip Size mm^2	Topology	Technology
[KTA+16]	30	290	-12[1]	-1	-14[1]	8	1400	3x2	IF mixer+amp+cubic mixer	40 nm CMOS
[HFA+18]	30	270	-15	-1.3	-16	5	N/A	1x1	res. mixer	80 nm InP-HEMT
[SKA+14]	30	300	-15	-4	-20	-5	N/A	1.12x0.88	I/Q HGC	250 nm InP HBT
[SGS+16]	N/A	240	16[2]	-25	-10[2]	2.5	313	2.67x0.635	x16+amp+GC+amp	130 nm SiGe BiCMOS
[KML+08]	6	210	2.8	N/A	N/A	6	74	1x1.5	DG mixer	100 nm InGaAs mHEMT
[ABM+14]	40	300	-12	N/A	N/A	2	N/A	3x0.75	x3+amp+mixer+amp	35 nm InGaAs mHEMT
Transconductance	>42	300	-6	-12	-19	-3	5	1x0.75	transcond. mixer	35 nm InGaAs mHEMT
Dual-Gate 2T	>34	240	-6	-9	-17	0	8	0.75x0.75	DG mixer	35 nm InGaAs mHEMT
Dual-Gate 1T	>50	240	-5	-15	-21	0	8	0.75x0.75	DG mixer	35 nm InGaAs mHEMT
SCC	45	240	-7/-8/−4.5[4]	-16/−14[4]	-24/-25/−20.5[4]	−6.6[6]/−7.5[6]/0[5]	4.8	1x0.75	HGC	35 nm InGaAs mHEMT
ICC	>45	240	-10.5/-11.5/−8[4]	-14/−10[4]	-26/-27/−19.5[4]	−6.6[6]/−7.5[6]/0[5]	3	1x0.75	HGC	35 nm InGaAs mHEMT
Nonlinear Resistance	>47	240	-10	>-5,−3[3]	>-16,−14[3]	0	0	1x1	res. mixer	35 nm InGaAs mHEMT

[1]including 32-way power combining at RF and IF amplification, [2]including RF amplification, [3]Simulated, [4]Combined P_{out} of RF and $\overline{RF}$, [5]At LO input of MMIC, [6]Calculated level at output of balun

6. Integrated Circuits for Terahertz Applications

In this chapter three examples will be given for the integration of the presented mixer architectures in state-of-the-art millimeter-wave systems. Not only the application of the three MMICs differ, two communication chips and one radar chipset, but also the employed mixer topology ranges from a single-ended heterodyne to a quadrature to a single balanced design. The content of chapter 6.1 and 6.2 has been previously published and is reprinted with permission, by Groetsch et al. [3] ©2019 IEEE and Groetsch et al. [8] ©2020 IEEE, respectively.

6.1. Radar Front End Using a Resistive Mixer

The trend to strive for higher frequencies is not only present in communication but also in radar applications. Radar systems aim to increase the resolution of radar images by using high bandwidths (BWs). This can help e.g. with detecting errors in materials as recently demonstrated by [MZB+18] for glass fiber reinforced plastics used in wind turbines or to detect carcinoma tissue [KVM+16]. Another reason to use mmWs in radar application is the reflection behavior at these high frequencies. Clothes or cardboard can be penetrated but explosives reflect the radiation. This qualifies mmW-radar especially for security applications as presented in [CSW+14].
To monolithically generate signals in the targeted H-band region (220 - 325 GHz) there are two main options: Oscillators with an oscillation frequency directly in the desired band or a chain of multipliers fed by a low microwave frequency e.g. X-band (7 to 11.2 GHz) or W-band (75 to 110 GHz) to convert it to the desired band. In the first case the realization of such an ultra-high frequency oscillator is highly complex and not tunable over a high bandwidth as needed for radar applications. A main disadvantage is the high phase noise. Although in the second case using a multiplier chain, the phase noise generated by the low microwave oscillator will degrade by $20\log(\mathrm{n})$, where n is the multiplication factor, the overall phase noise in the desired frequency range can be lower than in the first case. The possibility to tune the oscillator in the lower frequency regime will create a high tunable bandwidth at the output of the multiplier chain. If then combined with a power amplifier (PA) to boost the output power, the frequency multiplier can act as transmitter in a frequency modulated continuous wave (FMCW) radar system. Employed in a receiver the multiplier can be used to drive the mixer which down-converts the received signal to baseband.
Especially in W-band the availability of commercial high quality components including sources has grown in the past decade which makes it a good starting point to access the millimeter- and submillimeter-wave region.
In this chapter a complete chipset for a FMCW radar with a 50 GHz bandwidth consisting of

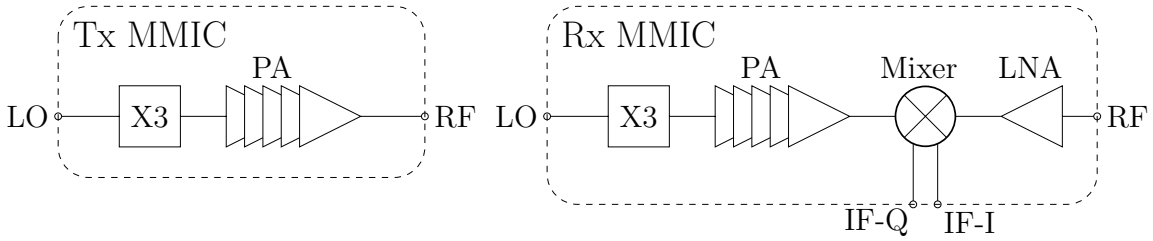

Figure 6.1.: Block diagram of the transmitter and receiver. The Tx is reused for LO generation in the Rx.

a high power transmitter and highly linear receiver is presented. The target applications are material scanners for security applications or material testing. In these cases often a high reflection occurs at the surface of the target. This reflection can saturate and desensitize the receiver and mask smaller reflections which are of interest. The chipset is realized in the 35 nm mHEMT technology described in chapter 4.

6.1.1. Transmit/Receive Chipset

The block diagrams for the Tx and the quadrature receiver (Rx) are shown in Fig. 6.1.
The transmit MMIC consists of two components, a frequency multiplier-by-three and a five-stage power amplifier. Both are designed to cover the RF range from 235 to 285 GHz corresponding to an input frequency range from 78 to 95 GHz.
The receiver comprises the same stages in the LO path to deliver enough bandwidth and to drive the mixer in saturation. A passive, resistive quadrature mixer architecture was chosen because of its high linearity regarding the RF signal. The IF channels are DC-coupled for a homodyne mode of operation. The quadrature signal enables the implementation of an image rejection topology. Additionally a highly linear low gain one-stage amplifier is used to increase the input power level and decrease the overall NF of the receiver. All four components were monolithically integrated on the receive MMIC.

6.1.1.1. Transmit MMIC

Fig. 6.2 shows the simplified schematic and the chip photograph of the transmit MMIC.
The input is called LO because typically in FMCW radars the input signal of the transmitter is identical to the LO signal driving the receive mixer. The input signal gets multiplied-by-three from W-band to H-band. The tripler operates in compressed class-A mode. The multiplier is followed by a power amplifier consisting of five stages. The first stage is a single CS stage, the second consists of two parallel branches each comprising two CS gain cells and the final stage has four parallel amplifier branches each again comprising two CS amplifiers. A more detailed description of the amplifier can be found in [STL+19].
A careful power level calibration for the on-wafer measurement was conducted using power meter measurements at the waveguide outputs feeding the measurement probes over the desired frequency range. To shift the reference plane to the tip of the probes the losses of the probes were taken from the data sheet and included in the calibration. Fig. 6.3 shows the measurement of output power versus output frequency of the Tx MMIC.
The input power was set to 8 dBm to saturate the frequency tripler. The results show a very flat gain response from 235 to 278 GHz with an output power of around 7 dBm. The

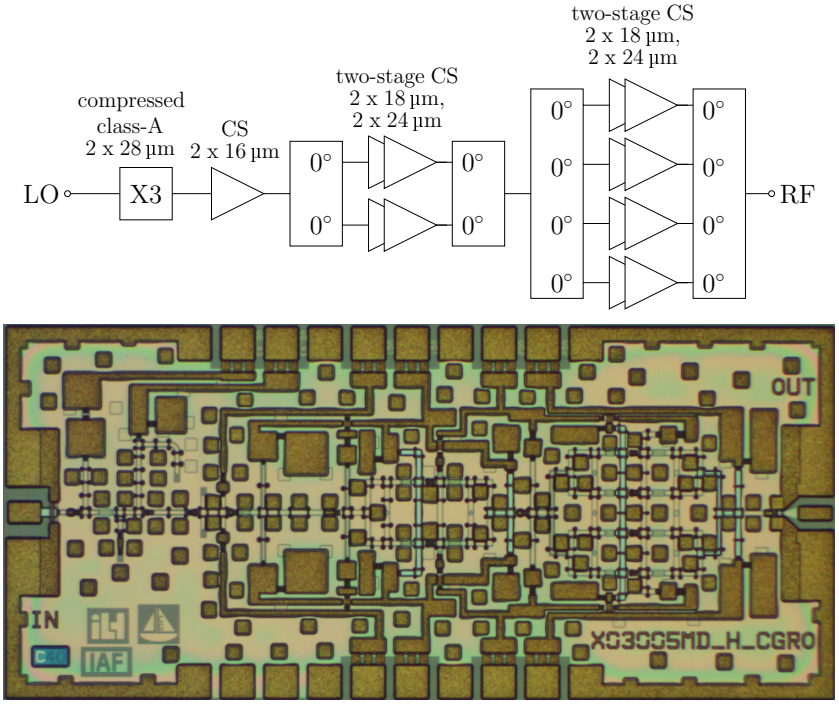

Figure 6.2.: Circuit schematic and chip photograph of the transmit MMIC. The chip size is 2 mm x 1 mm.

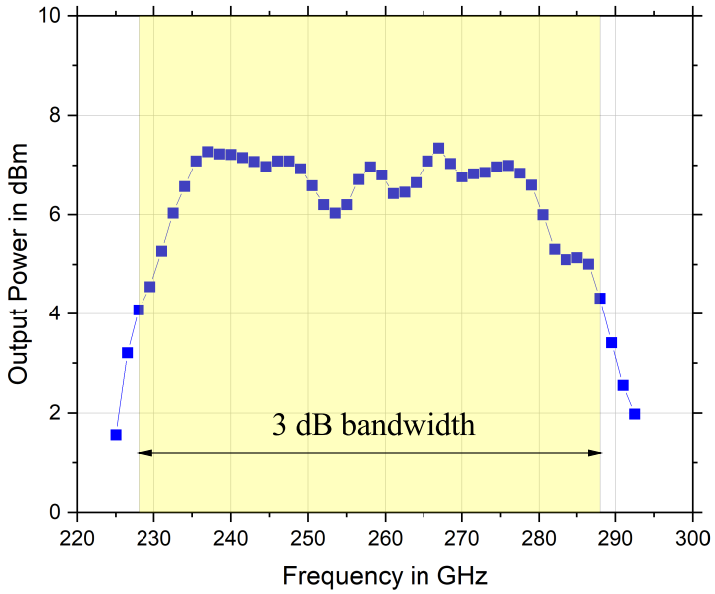

Figure 6.3.: Measured output power of the Tx versus output frequency at an input power of 8 dBm.

overall 3 dB bandwidth of the chip is 60 GHz ranging from 228 to 288 GHz. The overall power consumption of the transmitter is 235 mW at a supply voltage of 1 V.

6.1.1.2. Receive MMIC

The simplified circuit schematic and the chip photograph of the Rx MMIC is shown in Fig. 6.4. As discussed earlier the Tx was employed as LO driver stage in the receiver. The PA is followed by a quadrature mixer operating as down-converter stage. The individual mixer

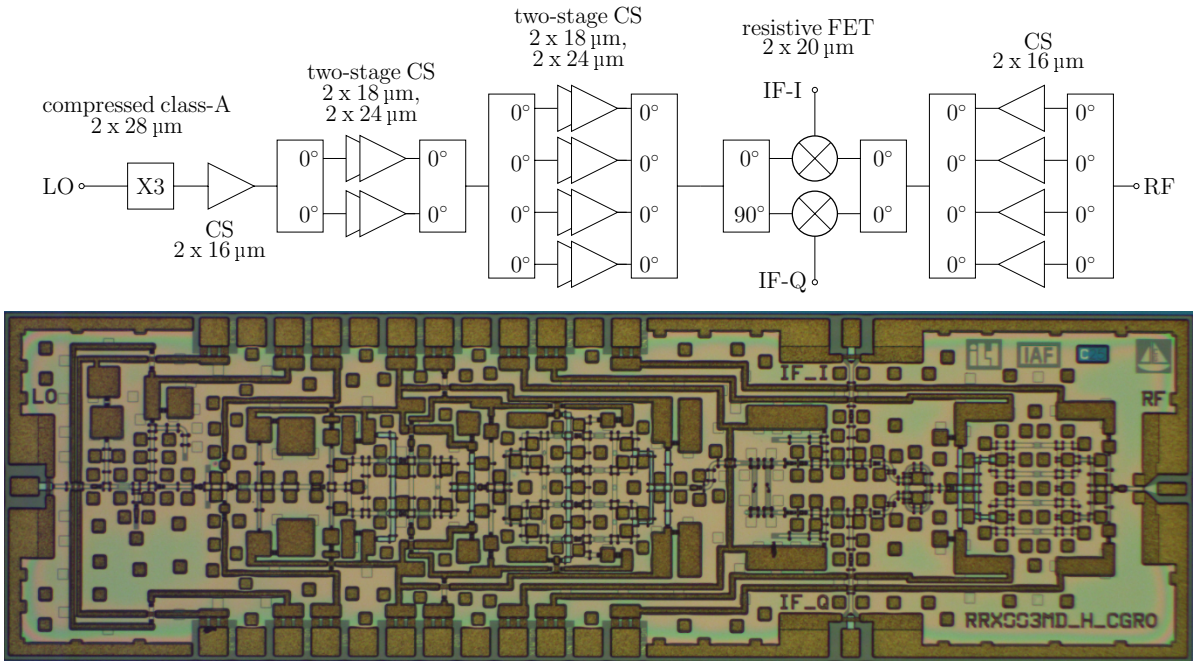

Figure 6.4.: Circuit schematic and chip photograph of the receive MMIC. The chip size is 3.25 mm x 1 mm.

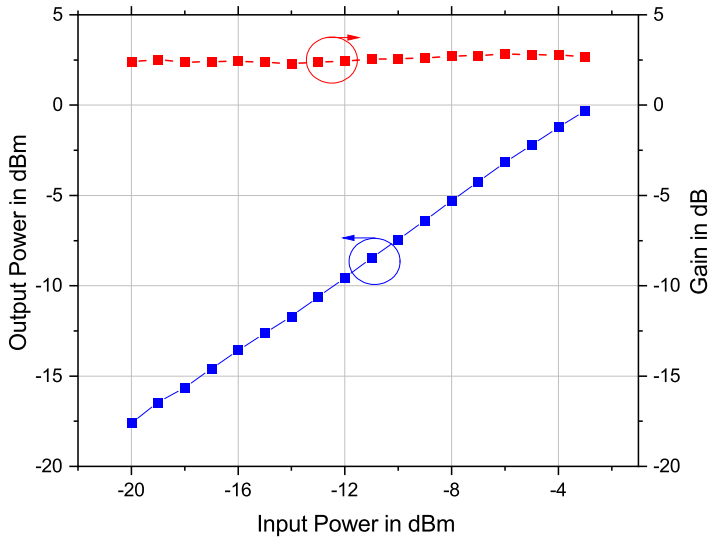

Figure 6.5.: Gain and output power of the receive amplifier in dependency of the input power. The input frequency was set to 280 GHz.

stages are realized as resistive FET mixers. The RF input signal is amplified before being fed to the mixer. The input amplifier is a single stage amplifier with four CS gain cells in parallel. The amplifier was characterized as a standalone MMIC in order to assess especially its linearity. The large-signal performance of the amplifier is depicted in Fig. 6.5.
The input frequency is 280 GHz, the average gain is around 3 dB. For lower frequencies e.g. 250 GHz a slightly higher gain of 4 dB can be reached. Up to an input power of −3 dBm no compression is occurring. This high linearity prevents saturation and desensitization in the receiver because of large unwanted input signals. These signals can for example be caused by strong reflections at a surface of a target. This takes place especially in material testing when

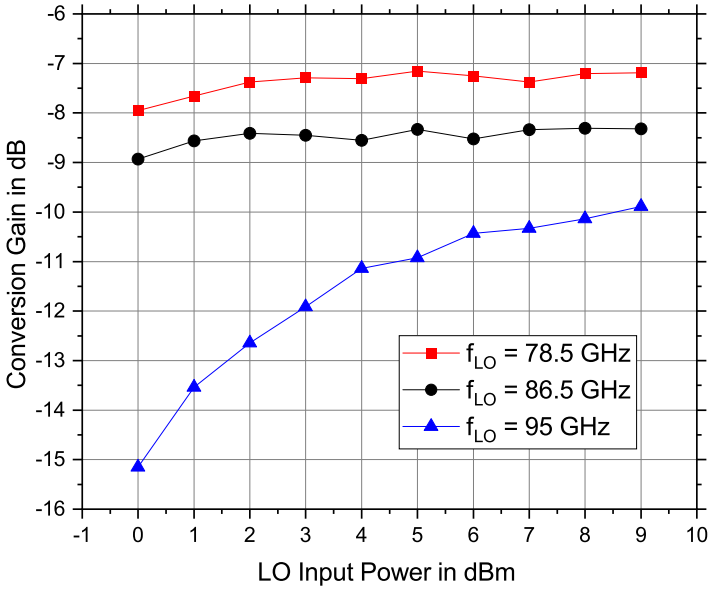

Figure 6.6.: Conversion gain of the Rx in dependency of the LO input power at an IF of 10 MHz, a RF power of -30 dBm for three different LO frequencies.

a high transmit power is necessary to penetrate the target and to compensate for propagation losses.

Although the gain of this input stage is low, it still helps to decrease the overall noise figure of the receiver calculated according to Friis formula for noise by around 3 dB from 13 dB to 10 dB using the simulated noise figures of the stand-alone mixer and amplifier.

With the high available output power of the PA it is possible to drive the mixer in saturation. The on-wafer measurement of CG versus LO input power of the Rx MMIC is shown in Fig. 6.6. Three different LO frequencies were applied, 78.5 GHz, 86.5 GHz and 95 GHz which translate after multiplying-by-three to the LO frequencies, 235.5 GHz, 259.5 GHz and 285 GHz, at the LO input port of the mixer. These frequencies represent the maximum, minimum and the center LO frequency for which the FMCW radar was designed. The RF frequency was chosen according to $\mathrm{f_{RF}} = \mathrm{f_{LO}} + \mathrm{f_{IF}}$ with a constant IF signal at 10 MHz. The RF power level was set to -30 dBm. At 8 dBm the conversion gain also for the highest frequency, 285 GHz, is saturated. So for the following measurements the LO input power was always set to 8 dBm at the W-band LO input of the MMIC.

The receiver achieves a flat conversion gain of -9 dB with a 3 dB bandwidth from 225 to 285 GHz while sweeping the LO and keeping the IF frequency constant at 10 MHz. These results are shown in Fig.6.7 for the IF-I and IF-Q channel.

The Rx conversion gain was evaluated in dependence of the RF frequency (Fig. 6.8) for the IF-I channel. Again the three different LO frequencies were applied to cover the corner cases. For a LO frequency of 259.5 GHz the RF was swept from 235 till 285 GHz. For the lower corner frequency only the USB ($\mathrm{f_{RF}} = \mathrm{f_{LO}} + \mathrm{f_{IF}}$) is of interest and accordingly for the upper corner frequency only the LSB ($\mathrm{f_{RF}} = \mathrm{f_{LO}} - \mathrm{f_{IF}}$). Therefore only those frequency sweeps were conducted up to an intermediate frequency of 25 GHz. The RF power level was set to -30 dBm.

Both measurements of IF-I and IF-Q were conducted separately because the measurement setup did not allow for a simultaneous characterization. The conversion gain for

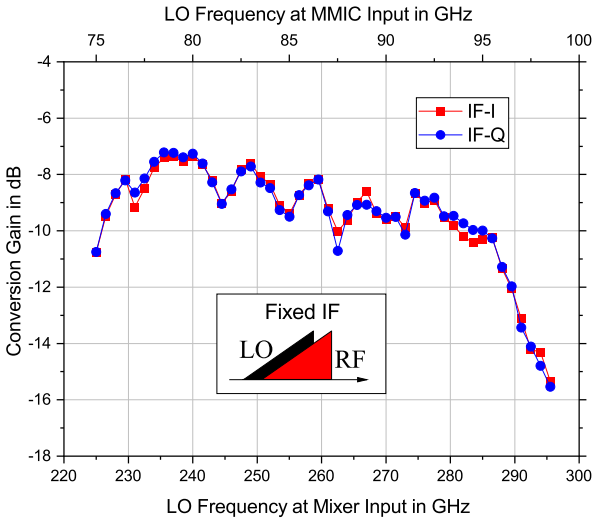

Figure 6.7.: Conversion gain for IF-I and IF-Q of the Rx versus the LO frequency at an IF frequency of 10 MHz and a RF power of -30 dBm.

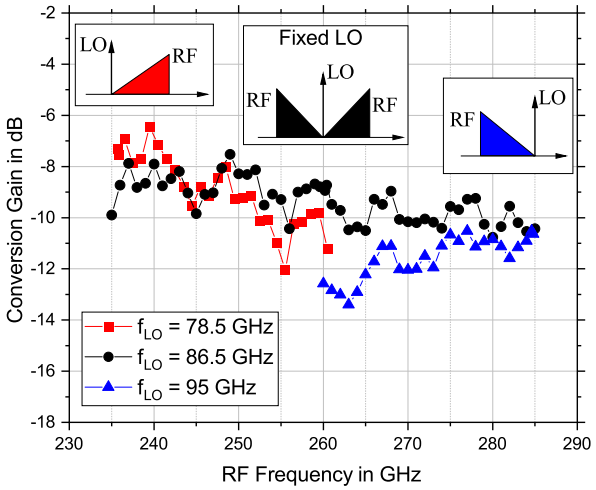

Figure 6.8.: Rx conversion gain in dependency of the RF input frequency at an RF power of -30 dBm for three different LO frequencies.

$f_{LO} = 259.5$ GHz is very flat over the whole RF band and lies at an average of -9 dB. The 3 dB bandwidth exceeds the measurement range. A similar behavior can be seen for a LO of 235 GHz. The conversion gain decreases for the maximum LO frequency. Here the average conversion gain lies at about -11 dB but also the 3 dB bandwidth is larger than the measured frequency range. The measurement results for IF-Q are very similar to IF-I. The mean values of the amplitude imbalance are shown in Table 6.1.
Not only the average I/Q-imbalance is very low over the whole frequency range for all three measured LO frequencies but also the peak values. This supports the implementation of image rejection measures.
The receiver consumes a total DC power of 295 mW at a supply voltage of 1 V.

Table 6.1.: Mean values of I/Q imbalance for different LO frequencies.

LO frequency	I/Q-Imbalance Average	I/Q-Imbalance Peak	BW
235.5 GHz	0.11 dB	0.28 dB	25 GHz
259.5 GHz	0.12 dB	0.43 dB	50 GHz
285 GHz	0.28 dB	0.58 dB	25 GHz

6.1.2. State of the Art

Table 6.2 summarizes the result of this work along with a comparison of state-of-the-art transmit and receive circuits for radar applications in similar frequency ranges.
The presented circuits deliver an outstanding output power, the largest bandwidths and a very high linearity. The low conversion gain is caused by the usage of only one amplifier stage as input buffer instead of a high gain LNA. Although no LNA was employed the Rx still exhibits a low calculated noise figure according to Friis formula for noise using simulated values.

Table 6.2.: Comparison of H-band chipsets for radar applications.

Ref.	f_{center} in GHz	P_{out} (Tx) in dBm	CG (Rx) in dB	LO BW[1] in GHz	RF BW[2] in GHz	NF in dB	Rx-P_{1dB} in dBm	DC Power in mW	Topology	Technology
[DBG+16]	340 GHz	0 dBm	−18 dB	30 GHz	N/A	N/A	N/A	N/A	x8 + x2 + x2-TRx	InGaAs pHEMT + Schottky
[TLM+13]	300 GHz	N/A	15 dB	40 GHz	N/A	N/A	N/A	N/A	PA+x3, x3+Rx MMIC	InGaAs mHEMT+Schottky
[SGS+16]	240 GHz	−6 dBm	10.5 dB	18 GHz	N/A	15 dB[3]	-18dBm	Tx: 1033 mW Rx: 866 mW	Tx MMIC, Rx MMIC	SiGe
This work	260 GHz	7 dBm	−9 dB	60 GHz	50 GHz	10 dB[3]	>−3 dBm	Tx: 235 mW Rx: 295 mW	Tx MMIC, Rx MMIC	InGaAs mHEMT

[1]LO sweep, fixed IF, [2]RF sweep, fixed LO, [3]calculated NF

6.2. Communication Front End Using a Heterodyne Dual-Gate Mixer

In recent years various terahertz communication systems were reported achieving ever higher data rates, even exceeding 100 Gbps. Different technologies and Tx and Rx architectures were employed in such transmission experiments. For example, all-electronic setups achieved 96 Gbit/s over a distance of 40 m at an LO frequency of 240 GHz [BMA+14]. [HTM+20] reports even 120 Gbit/s over 9.8 m. Applying a polarization-diversity MIMO technique in a QPSK transmission at 240 GHz facilitated a data rate of 100 Gbit/s [RVGHP20]. In [CEMS19] at a carrier of 300 GHz, 100 Gbit/s over a distance of 50 cm were shown. In CMOS technology at 300 GHz transmitters capable of a data rate of 105 Gbit/s by aggregating 6 channels were presented in [KTA+16]. By combining photonic and electronic systems the authors of [KLDA+13] showed a transmission experiment with 100 Gbit/s at an LO frequency of 240 GHz.

Most of the these systems use homodyne or zero-IF systems where the received RF is directly down-converted to a very large baseband (BB) bandwidth and evaluated in the digital domain. By exploiting the large available RF bandwidth around 300 GHz high data rates can be achieved even with simple modulation schemes. However, the large RF bandwidth also translates to a large BB bandwidth up to 25 GHz. To evaluate the baseband signal, extremely fast, high-end oscilloscopes and vector signal analyzer software are used. The transmitted data then conventionally consists of pseudorandom binary sequences (PRBSs) and not real-life data. To proof concepts and to gauge maximum transmission rates, this approach is well suited.

For real-life applications though, where real user data has to be transmitted, a different solution has to be used. Commercially available high-end modems capable of providing real-time signals can manage BB bandwidths of up to 2 GHz [Esc17]. Taking this as a basis, the obvious solution is to aggregate multiple channels, to combine them in an IF and to use one RF front end to transmit them altogether at a frequency band, where the necessary bandwidth is available, like in the H-band (220 - 325 GHz).

The work presented in [DDH+20] shows such a wireless transmission experiment where the concept of superheterodyne transmission in H-band is validated. Since no RF front end using IF frequencies higher than 30 GHz was available, the paper only shows the results for an IF system centered around 10 GHz. Even at far from ideal conditions the experiment shows the advantages of superheterodyne transmission over the zero-IF one. The quality of the transmission is improved for all modulation formats, the system is compatible with the new IEEE standard for 100 Gbit/s transmission [IEE17a] and channel aggregation is proven feasible.

The fully-integrated down-converter presented here enables a superheterodyne H-band Rx suitable for real-time terahertz communication compatible with the new IEEE 802.15.3d-2017 standard. It is designed for a large RF bandwidth, different LO frequencies and an IF between 65 and 95 GHz. Therefore components developed for 5G based on the standards IEEE 802.15.3e-2017 [IEE17b] and ETSI EN 302 217 [ETS16] can be employed in the IF. To the best of the authors' knowledge, it is the first down-converter MMIC that helps to combine the achievements in the development of 5G components for V- and W-band with the IEEE standard 802.15.3d-2017 for 100 Gbit/s wireless transmissions.

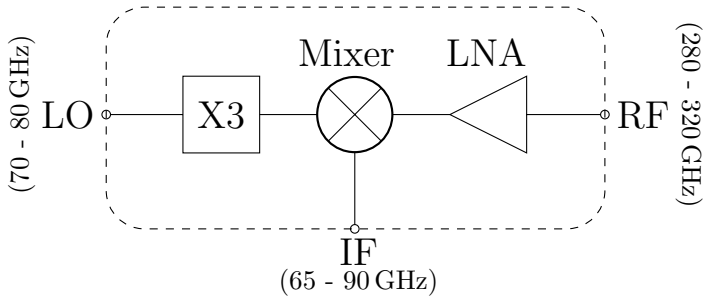

Figure 6.9.: Functional block diagram of the down-converter designed for superheterodyne communication systems.

A functional block diagram of the MMIC is shown in Fig. 6.9. By integrating an active dual-gate down-converter instead of a passive mixer the conversion gain was increased and the chip size and the power consumption were reduced drastically. To conclude, a detailed comparison with a similar down-converter comprising a resistive mixer and the necessary LO buffer stage instead of the active mixer is presented.

6.2.1. Superheterodyne Approach

The RF down-converter will be part of a superheterodyne front end. For clarification a block diagram of the complete transmit and receive front end is shown in Fig. 6.10.
Simplified, three crucial steps are necessary for the operation of a superheterodyne system. They are visualized in the bottom of Fig. 6.10. The corresponding node, where the particular step takes place, is also marked by numbers in the top of Fig. 6.10.

1. Multiple modems will provide a BB signal with a bandwidth of up to 2 GHz

2. These BB signals will be up-converted by the modems to the IF frequency range from 65 to 95 GHz. The LO applied to the IF up-converters will be slightly shifted in frequency in order to create an individual IF channel for each BB signal. Combined they yield the input signal for the RF mixer.

3. The LO used for the RF up-converter is in the range of 210 to 240 GHz. This translates to an RF output frequency from 280 to 320 GHz where the upper sideband is employed, while the lower sideband well below 200 GHz will be cut-off by the RF output amplifier and the antenna frequency range. The aggregated up-converted channels form the transmit signal.

After receiving the RF signal, the steps conducted in the transmitter are executed in the opposite direction, from 3 to 1. The RF front end down-converts the signal to an IF. IF mixers with different LOs convert the IF to the BB and feed it to the corresponding modem for analog to digital conversion and data evaluation.
A main concern for the operability of the presented system is a successful combining and separation of the channels. That includes preventing unwanted intermodulation products of one channel to interfere with another channel. Conventionally, filtering is done on a printed circuit board (PCB) or by surface/bulk acoustic filters. But at these high IF frequencies in V and W band, acoustic filters are not applicable and the transmission and packaging losses

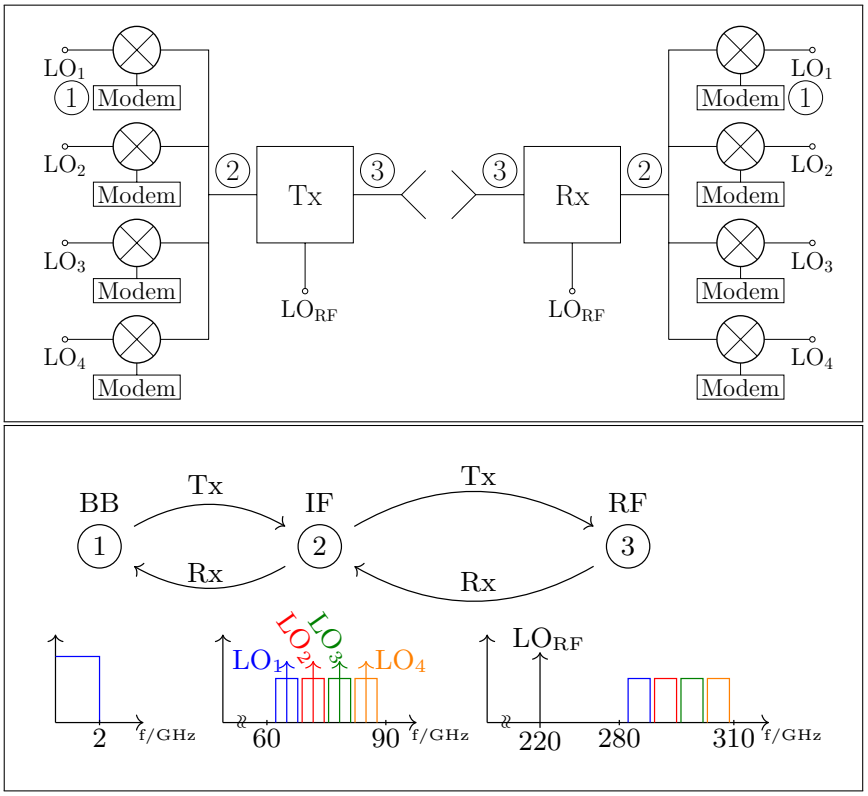

Figure 6.10.: Block diagram of exemplary superheterodyne transmit receive front end using channel aggregation in the IF.

on a PCB make this solution very inefficient. Therefore, the splitting and combining will be performed using waveguide dividers and waveguide filters. As shown in [DHK18] channel combining and separation using waveguides in W-band is feasible and efficient. To avoid images from mixing to distort other channels, it is also possible to use an image reject mixer architecture in the first mixer stage of the superheterodyne transmitter to overcome that problem.

6.2.2. Circuit Design

The down-converter consists of a frequency multiplier-by-three, an active dual-gate down-converter and an LNA. No LO buffer stage was implemented in the LO path. All chips are realized in the in-house 35 nm mHEMT technology of the IAF with cutoff frequencies f_t and f_{max} of more than 500 GHz and approximately 1000 GHz, respectively, as described in more detail in chapter 4. The LNA as a standalone circuit was presented in [6] and will therefore not be discussed in detail in this publication. It exhibits an average gain of 26 dB over a 3 dB bandwidth of 80 GHz. The noise figure was not measured but is estimated to be lower than 7 dB in the frequency band of interest, based on measurements of waveguide-packaged stand-alone LNAs in the same technology [TLW+17].
The schematic of the frequency multiplier-by-three and the dual-gate mixer is shown in Fig. 6.11. The multiplier-by-three consists of a two-finger, 28 µm CS transistor which operates in a compressed class-A mode. To match the input port to the frequency range from 70 to 80 GHz the transmission lines TL1 to TL3 are used. TL2, a quarter wavelength transmission

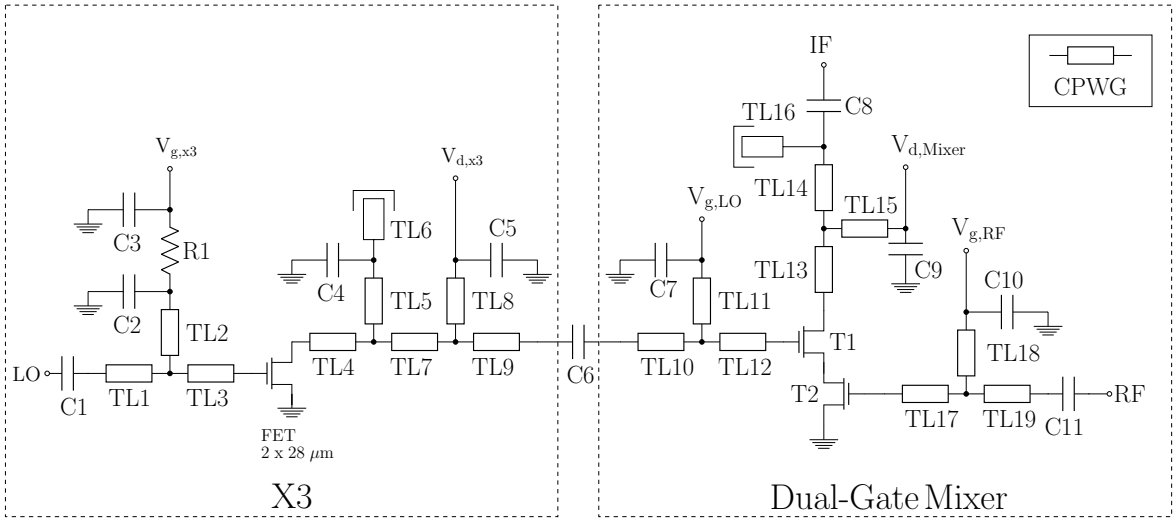

Figure 6.11.: Schematic of the multiplier-by-three integrated with the active dual-gate down-converter.

line at 75 GHz, in combination with C2, also decouples the gate bias network from the high frequency path. At the output port the matching is accomplished using the transmission lines TL4 to TL7 and the capacitively loaded open stub TL5. The drain bias is decoupled from the RF path via TL9 and C5.
The active dual-gate mixer comprises two two-finger transistors T1 and T2. T2 is a common-source stage where the drain is connected to the source of T1. Although depicted as two separate cells in the schematic, in the physical implementation they are merged together into one multi-finger transistor shell sharing the same extrinsic device environment. This type of active dual-gate mixer has been presented in chapter 5.1.1.
The gate width of T1 and T2 is 15 µm. The LO signal is fed to the gate of T1 and the RF signal to the gate of T2. TL10 to TL12 and TL17 to TL19 are used to match and decouple the LO and the RF, respectively. The IF is extracted from the drain of T1 using an airbridge and a short transmission line represented by TL13. TL14 and the open stub TL16 match the IF port to 50 Ω. In order to separate the IF signal from the drain bias, the transmission line TL15 and C9 are used. C1, C6, C8 and C11 are DC blocking capacitors.
The active dual-gate mixer was primarily selected because of the low requirement of LO power especially compared to a resistive mixer. This is due to the different mixing principles that are applied in the two mixer types as explained in detail in chapter 2.1. .

6.2.3. Measurement Setup

The receive MMIC was characterized in an on-wafer testing environment. The LO signal was generated by an analog signal generator in combination with a transmit/receive-module multiplying the frequency by a factor of 5 to reach the desired input frequency range from 70 to 80 GHz for the integrated multiplier-by-three which then translates to 210 to 240 GHz at the LO input of the mixer.
For the RF, a synthesized sweeper (10 MHz - 50 GHz) was employed. With a frequency multiplier-by-three, first a signal in W-band is generated. It is again multiplied by 3 to cover the frequency range from 280 to 320 GHz.

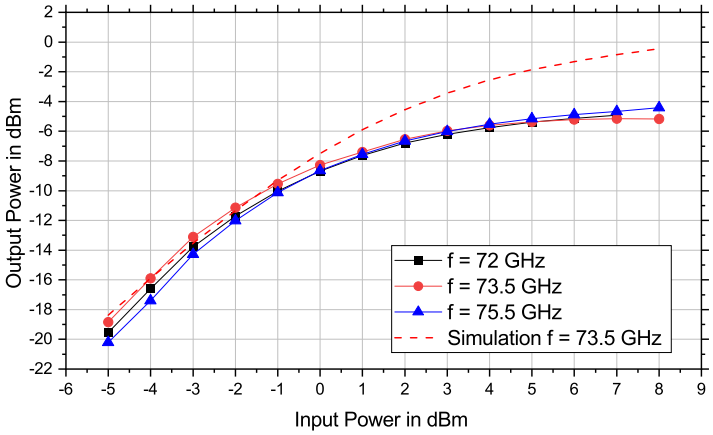

Figure 6.12.: Simulated and measured output power versus input power of the multiplier-by-three. The measurement were conducted at three different input frequencies, 72, 73.5 and 75.5 GHz.

After extracting the IF from the chip, it was fed to a broadband spectrum analyzer covering the entire frequency range from 60 to 90 GHz.
Both the RF and LO signals were applied to the device under test via H-band waveguides (WR-3) and on-wafer measurement probes. For the IF, WR-10 waveguides and probes were used. To calibrate the system, the power levels at the outputs feeding the measurement probes were determined over the frequency range of interest. By including the losses of the probes given in the datasheet in the calibration, the reference plane was shifted to the tip of the probes.

6.2.4. Measurement Results

A standalone measurement of the multiplier-by-three and of the multiplier-by-three in combination with the active down-converter as shown in Fig. 6.11 was conducted. Hereby the influence of every stage on the overall performance of the down-converter can be identified and the chip accordingly optimized in future designs.
The multiplier-by-three was designed to be able to generate an output frequency from 210 to 240 GHz which corresponds to an input frequency of 70 to 80 GHz. The comparison of simulation and measurement is presented in Fig. 6.12 and Fig. 6.13. Fig. 6.12 shows the output power of the multiplier-by-three in dependency of the input power and in Fig. 6.13 in dependency of the output and input frequency.
The simulation of output power over input power is in good accordance with the measurement at low input power levels. For input powers larger than 0 dBm, the deviation increases. The saturation effect in the simulation is weaker than in measurement. Even for input powers as high as 15 dBm, not shown for reasons of clarity, the simulated output power does not reach a plateau which is an unrealistic behavior of the transistor model. The measurement is fairly saturated at 4 dBm. Therefore, this value was chosen for the comparison of the frequency characteristic of the tripler in Fig. 6.13.
The simulation shows a peak output power of slightly above -2 dBm and a 3 dB bandwidth of more than 60 GHz. However, at the same input power of 5 dBm the measured output power level is 3 dB lower than simulated and has an average value around -5 dBm. That means that the mixer can be driven with a maximum LO power of -5 dBm.

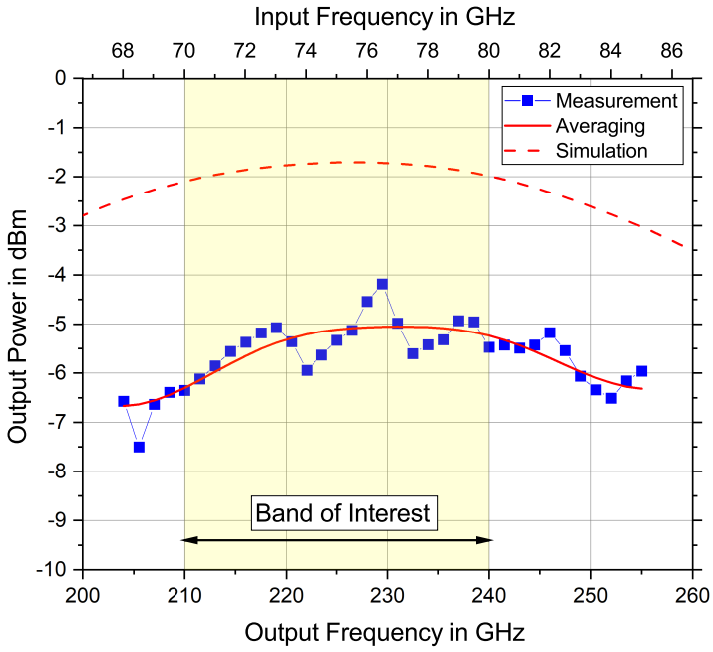

Figure 6.13.: Simulated and measured output power versus input (top x-axis) and output frequency (bottom x-axis) of the multiplier-by-three at an input power of 5 dBm.

Over the desired 30 GHz bandwidth the output varies only by around 1 dB. The overall 3 dB bandwidth of the multiplier-by-three exceeds the measurement bandwidth from 204 to 255 GHz. The desired frequency band from 70 to 80 GHz was therefore met in the measurement.

In a superheterodyne system, where the frequency range is divided into several channels for data transmission, the effect of unwanted harmonics of the frequency multiplier have to be considered.

There are mainly two ways undesired harmonics can distort the communication signal of the presented system configuration: First, the unwanted harmonic forms an intermodulation product with one channel of the received signal at H-band, that falls into another channel and generates interchannel interference. Second, a harmonic lies in the RF frequency range of the receiver. This can impair the received signal in multiple ways: The harmonic can be reflected back from the output of the LNA into the mixer and lead to self-mixing and self-biasing of the mixer. Or, the signal can travel through the LNA from output to input and after being reflected at the antenna, it adds to the receive signal and accelerates the saturation of the LNA and the mixer.

In the presented system, the fourth harmonic falls in the receive band. The lowest and highest LO frequencies at 70 GHz and 80 GHz translate exactly to the corners of the RF band: $4 \cdot 70\,\text{GHz} = 280\,\text{GHz}$ and $4 \cdot 80\,\text{GHz} = 320\,\text{GHz}$. Therefore, during the design of the frequency tripler, the output matching network was also optimized for a high suppression of the 4th harmonic. At 2 dBm input power the simulated output power of the fourth harmonic lies at -30 dBm which corresponds to a 25 dB ratio of desired carrier to unwanted harmonic. This is low enough to prevent impairments from self-mixing and to prevent saturation of the LNA.

For interchannel interference to occur, intermodulation products have to fall into the targeted

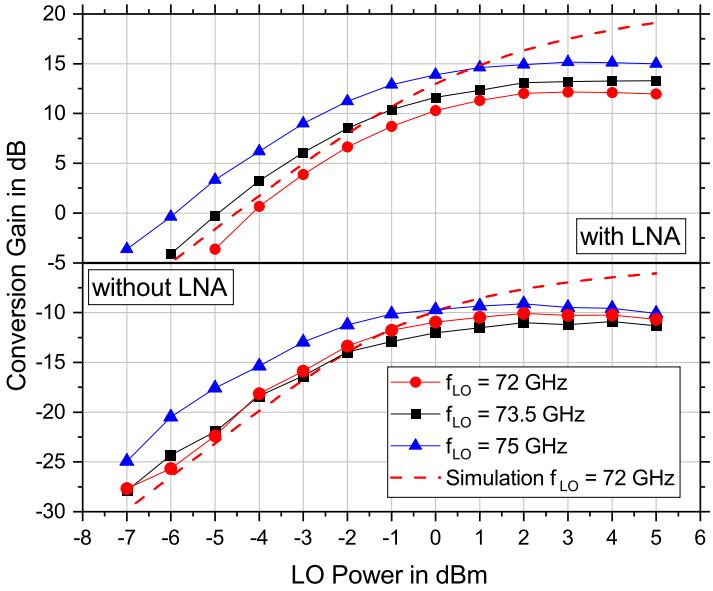

Figure 6.14.: Measured conversion gain of the down-converter over LO input power with and without integrated LNAstage. The measurements were conducted at an RF power of −45 dBm for linear operation, an IF of 80 GHz and three different LO frequencies, 72, 73.5 and 75.5 GHz.

frequency range. Due to the high LO, 70 to 80 GHz, and RF, 280 to 320 GHz, there are not many possible combinations. Using the highest second harmonic and the lowest RF leads still to a mixing product far away from the IF band: $280\,\text{GHz} - 2 \cdot 80\,\text{GHz} = 120\,\text{GHz}$. Intermodulation with the fourth harmonic leads to mixing products below the IF band since the fourth harmonic falls directly in the RF band. The closest is the lowest fourth harmonic and the highest RF signal: $320\,\text{GHz} - 4 \cdot 70\,\text{GHz} = 40\,\text{GHz}$.
But, interfering intermodulations can be caused by the 5th harmonic. For example $5 \cdot 75\,\text{GHz} - 290\,\text{GHz} = 85\,\text{GHz}$. However, according to simulation the fifth harmonic of the frequency multiplier is suppressed by 15 dB relative to the desired third harmonic at a 2 dBm input power level. The power of the mixing product of interest $5 \cdot f_{LO} - f_{RF}$ is even further decreased by the conversion loss of the mixer. The ratio of the desired intermodulation $f_{RF} - f_{LO}$ and the unwanted $5 \cdot f_{LO} - f_{RF}$ is 25 dB in simulation. Although this is low enough to avoid serious impairments, in future designs an additional filtering of the 5th harmonic after the multiplier-by-three will be considered to account for possible deviations between simulation and measurement.
Fig. 6.14 shows the conversion gain of the dual-gate down-converter integrated with the multiplier-by-three (without LNA). Furthermore the curves of the MMIC including the LNA are shown (with LNA).
Here, the plotted conversion gain is the sum of the gain of the LNA and the conversion gain of the mixer. The results are plotted over the LO power at the input of the frequency tripler. The measurement was conducted for three different LO frequencies, 72, 73.5 and 75 GHz which translates to LO input frequencies at the mixer of 216, 220.5 and 225 GHz. The RF was changed with the LO frequency in order to maintain a constant IF of 80 GHz for all three measurements.
The shape of the curves is very similar. They all start to saturate at −1 dBm of LO input power and are fully saturated at 2 dBm. For an input power of 2 dBm the output power

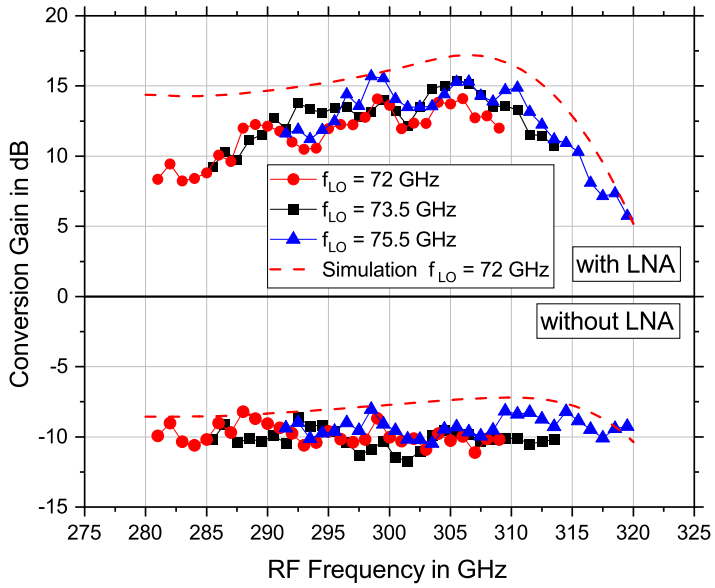

Figure 6.15.: Measured conversion gain versus RF frequency with and without integrated LNA stage at an LO input power of 2 dBm. The RF power was −45 dBm, three different LOs were applied, 72, 73.5 and 75.5 GHz while the IF was measured over the 65 to 93 GHz frequency range.

of the frequency tripler is −6.5 dBm. This means, the mixer is saturated even before the multiplier-by-three exhibits its maximum output power. Therefore, the difference of 3 dB between measurement and simulation of the output power of the frequency tripler does not affect the overall down-converter performance. Depending on the frequency the achieved conversion gain lies between -11 and −9 dB and between 12 and 15 dB, respectively for the version with the integrated LNA. The gain of the LNA can be considered constant. By increasing the LO power the conversion gain of the mixer increases and therefore the overall conversion gain of the down-converter. By using both measurements, the one with and the one without LNA, the gain of the LNA can be deduced. It lies around 24 dB which is in accordance to the results presented in [6], where the same LNA, placed as stand-alone component, reaches an average gain of around 26 dB.
For the next measurement the RF frequency was swept. Depending on the LO frequency a different range for the RF was used in order to result in the same IF range. Table 6.3 shows the corresponding frequencies for this measurement.

Table 6.3.: Overview of frequencies used for constant IF sweep.

LO	RF	IF
72	281 - 309 GHz	65 - 93 GHz
73.5	285.5 - 313.5 GHz	65 - 93 GHz
75	291.5 - 319.5 GHz	65 - 93 GHz

Fig. 6.15 shows the conversion gain versus the corresponding RF frequency for the down-converter version with and without LNA. The RF input power was kept constant at −45 dBm to assure linear operation of the down-converter. The down-converter without LNA exhibits

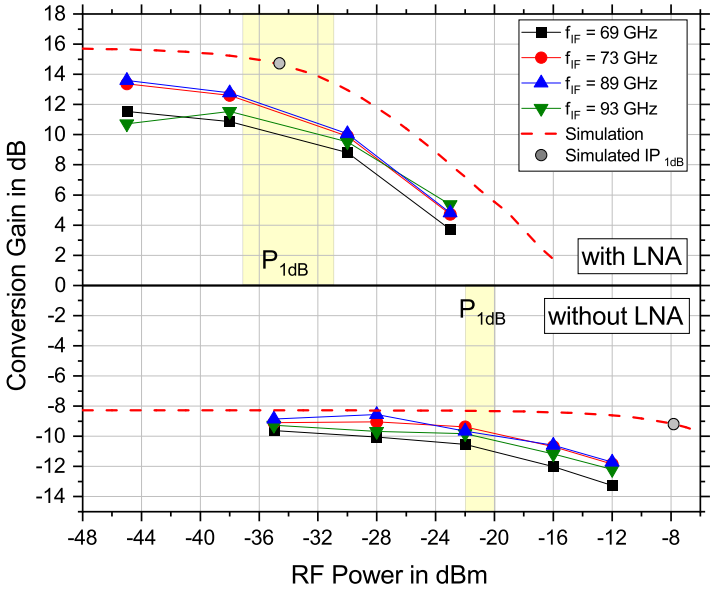

Figure 6.16.: Measured conversion gain versus RF input power with and without integrated LNA stage at an LO input power of 2 dBm and an LO frequency of 73.5 GHz. The results are plotted for four different IF frequencies, 69, 73, 89 and 93 GHz.

very flat conversion gain curves from 281 to 319 GHz of around −10 dB. The 3 dB RF bandwidth exceeds the measurement range. When the LNA is included, the curve becomes more frequency-dependent. The 3 dB bandwidth reduces to 25 GHz from 288 to 313 GHz. However, comparing this result with the measurements from [6], the decrease in gain of the LNA is due to a saddle point, meaning a local minimum, and the conversion gain is expected to increase again for lower frequencies. The achieved conversion gain in the measured region ranges between 12 dB and 15 dB.

Furthermore, the linearity of the down-converter is of interest. The conversion gain versus the RF input power is shown in Fig. 6.16.

The curve is plotted for a constant LO frequency of 75.5 GHz and different frequencies over the entire IF range. The input-referred 1-dB compression point, $\mathrm{IP}_{1\mathrm{dB}}$, for the version without LNA lies between -20 and −22 dBm. There is a clear deviation from the simulation. The simulated $\mathrm{IP}_{1\mathrm{dB}}$ is −8 dBm.

However, regarding the $\mathrm{IP}_{1\mathrm{dB}}$ of the version containing an LNA, the gap between measurement and simulation vanishes. The measured range of the $\mathrm{IP}_{1\mathrm{dB}}$ is -31 to −38 dBm. The simulated $\mathrm{IP}_{1\mathrm{dB}}$ is −35 dBm. The simulation was conducted for an IF of 85 GHz. The simulated compression point only changes marginally for other intermediate frequencies. Therefore the plotted curve is representative for the entire IF range. From the $\mathrm{IP}_{1\mathrm{dB}}$ and the conversion gain the output-referred 1-dB compression point, $\mathrm{OP}_{1\mathrm{dB}}$, can be calculated. Depending on the frequency, values between −21 dBm and −25 dBm are reached.

We can identify several effects that lead to the discrepancy between simulation and measurement without LNA as shown in Fig 6.16.

First of all, the dual-gate mixing cell consists of two transistors: T1 and T2 (Fig. 6.11), but as can be seen in Fig. 5.4, they are integrated in one common cell. There is no simulation model available for such a combined transistor cell. Therefore, the mixing cell was simulated using two single transistors, similar to the depiction of the schematic in Fig. 6.11. By that,

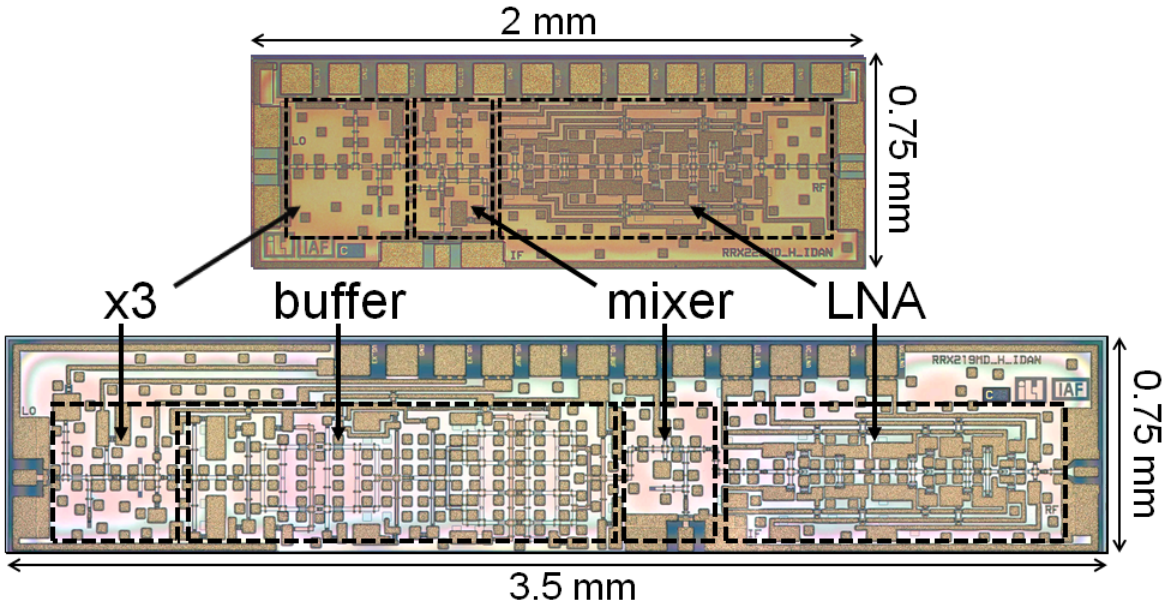

Figure 6.17.: Top: Chip photograph of the presented down-converter employing an active dual-gate mixer. Bottom: Chip photograph of an similar down-converter with an resistive mixer and the necessary LO buffer stage. The chip sizes are 3.5 mm x 0.75 mm and 2 mm x 0.75 mm.

the parasitics of the real transistor cell are not modeled according to reality. Furthermore, no coupling between the two transistors is taken into account in the simulation.
Additionally, intermodulation at frequencies around 300 GHz is very challenging to model. As can be seen in both the simulation of the frequency multiplier-by-three, Fig. 6.12 and the simulation of the mixer conversion gain versus LO power, Fig. 6.14, the transistor model is overly optimistic at large input powers for the third harmonic and the second order intermodulation product, $\mathrm{f_{RF}} - \mathrm{f_{LO}}$. That means, that in reality compression starts at lower input powers and progresses faster as in simulation. For a down-converter there are two input signals: LO and RF. For the linearity simulation the transistor is operated in an extreme condition: both signals are set to very high input powers. This leads to a superposition of the underestimated compression of both input signals.
For typical linear components, where input and output operate at the same frequency, the simulated compression curve is more accurate than for nonlinear components such as frequency multipliers or mixers. Now, when the LNA is included in the simulation, its 1-dB compression point dominates the systems $\mathrm{IP_{1dB}}$. Since the LNA's $\mathrm{IP_{1dB}}$ is modeled more accurately, the overall system simulation matches the measurement better. Although the NF was not measured, it can be calculated using Friis formula. A state-of-the-art LNA module in the same technology exhibits a NF of 6.5 dB [TLW+17]. Assuming an LNA gain of 25 dB and an NF for the active mixer from simulation of 16 dB, the overall down-converter NF calculates to 6.6 dB.
In the investigated superheterodyne system the baseband channels are in the range of a few gigahertz. Up-converted by a double-sideband mixer, a channel occupies twice the baseband channel bandwidth in the transmission band. Therefore the conversion gain over one channel, meaning a few gigahertz, is more constant than over the entire RF bandwidth. Hereby impairments introduced by gain curve flatness are reduced per channel.

The main motivation for implementing an active dual-gate down-converter was to render the large LO buffer stage for the resistive mixer obsolete while maintaining the circuit's small-signal performance. This reduces the overall chip size, power consumption and facilitates the packaging of the MMIC.
In the following, the integrated down-converter including the LNA, as shown in Fig. 6.9 will be compared to a similar down-converter comprising a resistive mixer instead of an active one. The employed LNA and x3 are identical. Additionally an LO buffer stage was integrated, since it is necessary to drive the resistive mixer. For further reference the down-converter with the resistive mixer will be addressed as RRX and the version with an active mixer as ARX.
Fig. 6.17 shows the chip photographs of both down-converters. The upper picture represents the ARX, the bottom one the RRX. The dimensions of RRX are 3.5 mm x 0.75 mm. By using an active mixer the chip size was therefore reduced by 42 % to 2 mm x 0.75 mm. There is even potential for saving more chip space for ARX by using DC pads with a smaller pitch.
The power consumption per stage is given in Table 6.4.

Table 6.4.: Power consumption per stage of ARX and RRX.

Version	x3	Buffer	Mixer	LNA	Total
ARX	27 mW	N/A	15 mW	42 mW	84 mW
RRX	27 mW	212 mW	0 mW	42 mW	281 mW

Although the resistive mixer operates without any DC power, the large buffer stage that is necessary to drive the mixer deteriorates the overall power consumption. By employing an active dual-gate mixer the DC power consumption was reduced by 70 %.
These clear advantages only count if the performance of ARX is still comparable to RRX. Since the same multiplier-by-three stage was used, the necessary input power for both circuits is the same. That leaves three important figures of merit up for comparison: The conversion gain, the bandwidth and the linearity. The same measurements as presented in chapter 6.2.4 were conducted under the same conditions regarding LO, RF and IF frequencies and LO and RF power to make the results as comparable as possible.
Fig. 6.18 shows the conversion gain versus RF frequency for both versions.
Also for RRX, three different LO frequencies were analyzed: 72, 73.5 and 75.5 GHz while the IF was swept from 65 GHz to 95 GHz. The results show that the conversion gain of ARX is around 4 dB higher over the entire band of interest. The curves of RRX are shifted to higher frequencies and peak at 310 GHz while the curves of ARX are more centered around the target frequency of 300 GHz. The 3 dB bandwidth of ARX is slightly higher than that of RRX. RRX shows a slightly more LO frequency dependent behavior, especially for $\mathrm{f_{LO}} = 72$ GHz.
The conversion gain over RF input power is shown in Fig. 6.19.
The input-referred compression behavior of RRX is better than ARX. The $\mathrm{IP_{1dB}}$ is -26 dBm which is around 10 dB higher than the $\mathrm{IP_{1dB}}$ of ARX.
But due to a lower conversion gain, this does not translate to the output. The output-referred compression point, $\mathrm{OP_{1dB}}$, calculates to around -18 dBm. The difference between RRX and ARX reduces to approximately 5 dB.
Receivers are generally designed to operate at a low input power level. Especially in the

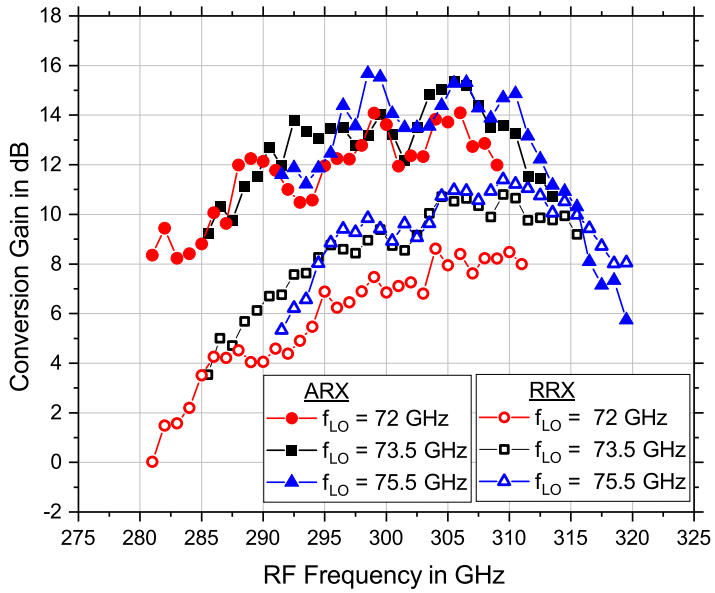

Figure 6.18.: Comparison of the measured conversion gain versus RF frequency of the presented down-converter and a reference down-converter using a resistive mixer at an LO input power of 2 dBm. The RF power was −45 dBm, three different LOs were applied, 72, 73.5 and 75.5 GHz while the IF was swept from 65 to 95 GHz.

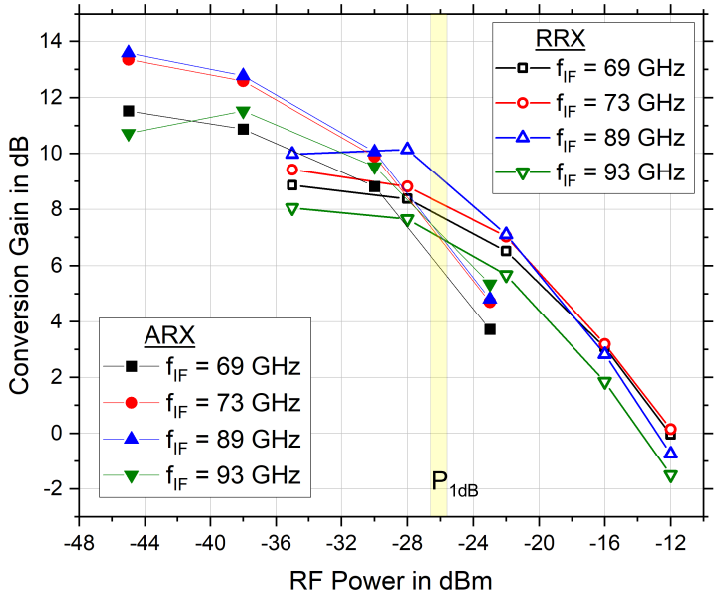

Figure 6.19.: Comparison of the measured conversion gain versus RF input power of the presented down-converter and a reference down-converter using a resistive mixer at an LO input power of 2 dBm and an LO frequency of 73.5 GHz. The results are plotted for four different IF frequencies, 69, 73, 89 and 93 GHz.

H-band the transmit power is strongly limited and the free space path loss is high. Large antennas are not practicable for short range transmissions of several meters, therefore also the antenna gain cannot be increased immensely to compensate the losses. Altogether this leads to expected input power levels at the receiver that are generally in the range of −40 dBm or lower.

A simple calculation to support the argument: Assuming a transmission at $f = 300$ GHz,

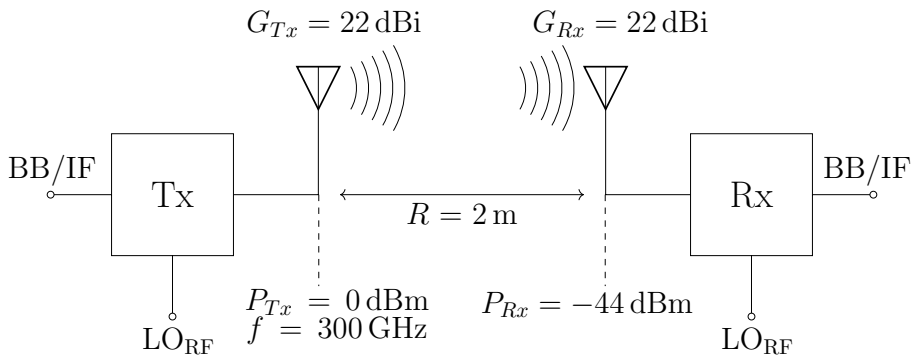

Figure 6.20.: A schematic of a wireless link transmitting at 300 GHz over 2 m employing two antennas with 22 dBi antenna gain each.

over a distance of $R = 2\,\mathrm{m}$, a transmitter output power $P_{Tx} = 0\,\mathrm{dBm}$ and two horn antennas each with a gain of $G_{Rx} = G_{Tx} = 22\,\mathrm{dB}$. A schematic of the described setup is shown in Fig. 6.20.
The received power P_{Rx} calculates as follows:

$$P_{Rx} = P_{Tx} + G_{Tx} + G_{Rx} + 20 \cdot log_{10}(\frac{c}{4\pi f R}) = -44\,\mathrm{dBm} \tag{6.1}$$

That is around 10 dB in backoff of the down-converter's $\mathrm{IP_{1dB}}$ and thereby facilitates the transmission of complex modulation formats.
Additionally, if the linearity of the down-converter is not sufficient, it is possible to reduce the gain of the LNA or implement a variable gain amplifier in the input amplifier stage.

6.2.5. State of the Art

Table 6.5 gives an overview of the state of the art of receivers and down-converters operating around 300 GHz. Not always all figures of merit were measured or were given in the referenced publications.
To avoid confusion, the given RF bandwidth is the bandwidth for a fixed LO with a swept RF frequency as shown in Fig. 6.18, not a simultaneously swept LO and RF leading to a fixed IF.
The presented down-converter exhibits the highest conversion gain and the second highest RF bandwidth. The highest measured bandwidth was reported by [6]. Similar to RRX this down-converter shows a 2.8x higher power consumption. Furthermore, the down-converter consists of two chips, taking up almost three times more die area than the presented work.
As discussed in chapter 5.1.3 the linearity is lower than compared to down-converters using resistive mixers. [6] and [HFA+18] underline this statement. The high $\mathrm{IP_{1dB}}$ of [HFA+18] is due to the lack of an input amplifier stage. Assuming an additional LNA of 25 dB, the linearity of [HFA+18] will also be in the range of RRX or [6].
The chip size of the presented MMIC is the smallest compared to all down-converters excluding [HFA+18] and [SKA+14] because in these works only single stage circuits were presented without any LO generation or additional input amplification.

Table 6.5.: Comparison of state-of-the-art receivers and down-converters at 300 GHz.

Ref.	RF BW in GHz	f_{LO} in GHz	CG in dB	P_{LO} in dBm	IP_{1dB} / OP_{1dB} in dBm	Chip Size in mm^2	DC Power in mW	Topology	Technology
[HKT+17]	33	290	-18	2	N/A	2.27	416	buffer + x3 + resistive mixer	40 nm CMOS
[HFA+18]	30	287.5	-15	5	-1[1]/-16[1]	1	N/A	resistive mixer	80 nm InP-HEMT
[SKA+14]	30	300	-15	-5	N/A	0.99	22	half Gilbert cell mixer	250 nm InP HBT
[TLW+17]	N/A	297.5	6.5	3	N/A	2.44	N/A	x3 + PA + I/Q mixer + LNA	35 nm InGaAs mHEMT
[6]	45	292.5	7	2	-26/-20	4.38	235	x4 + PA + I/Q mixer + LNA	35 nm InGaAs mHEMT
[HTM+20]	17	270	3	7.5	N/A/-17[2]	N/A	4500	individual waveguide modules	80 nm InP-HEMT
[LHY+19]	>20	266	< 5	1	N/A	11.07[3]	897	x3+mixer+I/Q mixer+4 amps	40 nm CMOS
[RVGHP20]	28	230 - 250	18	4	N/A	3.36	2850[3]	2x(x16+PA+I/Q mixer+BB amp)	130 nm SiGe HBT
This work	38	300	14	2	-35/-22	1.5	84	x3 + dual-gate mixer + LNA	35 nm InGaAs mHEMT

[1]operating as up-converter [2]estimated [3]Tx + Rx

6.3. Communication Front End Using a Homodyne Dual-Gate Mixer

To keep up with the ever-growing demand of wireless data-transfer, the low terahertz frequencies around 300 GHz have proven to be suitable. As discussed in chapter 6.2 several systems already broke the barrier of 100 Gbit/s most of them using homodyne or zero-IF topologies.
A major issue of these systems is the packaging. Conventionally, the MMICs are integrated in split-block modules. Waveguides that are nearly lossless connect the MMIC to the outside world. Especially in the mmW regime, the highest loss is introduced by the wirebonds that are used to extract or apply the signal from and to the MMIC. A transmission line on a PCB or ceramic substrate for frequencies as high as H-band is not realizable yet.
The major downside of that approach is a very high cost factor and the complexity of the assembly. Another problem are resonances in the packages due to infinite isolation or cavity modes. Especially in millimeter-wave bands, cavity resonances are a major problem [Dix05]. In order to avoid this additional measures have to be adopted, like using non-rectangular chip dies [TLW+17] and limiting its aspect ratio.
An alternative is the assembly on a low cost PCB, as for example presented in [RGS+18]. By integrating an antenna on the MMIC wirebonds as well as transmission lines on the PCB at H-band frequencies are circumvented. The highest frequency on the board is therefore the IF. Nonetheless, for a homodyne Rx operating at 300 GHz this frequency can lie at several tens of gigahertz as will be demonstrated in the following.
In this chapter an MMIC with an integrated antenna is presented. It was designed to be mounted on a low-loss RF PCB to avoid costly waveguide packaging. The overall system will comprise two MMICs, the H-band receiver and a frequency multiplier-by-twelve, a PCB with a power distribution and decoupling network, LO and IF feedlines and K-connectors that perform well up to 40 GHz. The x12 enables a low LO input frequency of 8.33 GHz and generates the 100 GHz drive signal for the receiver. A peculiarity of the design is the main beam direction of the antenna. It is designed to radiate through the MMIC and through the PCB. A lens on the backside of the PCB will then increase the directivity. Fig. 6.21 and Fig. 6.22 show a visualization of a board prototype.
The employment of an active mixer as presented in chapter 5.1.1 was key to the realization of the system since it permitted the integration of the complete receiver chain in a single MMIC. The implementation of a resistive FET mixers would have led to a much larger footprint. Therefore, similar designs, as for example published in [6], have to use multiple MMICs to achieve the same functionality even without integrating an antenna. A multi-chip assembly demands chip-to-chip wirebonds at H-band frequencies which are lossy, complex to manufacture and error-prone. This negates almost all the advantages of the PCB assembly and must therefore be avoided.

6.3.1. Receiver MMIC Design

6.3.1.1. Circuit Design

The MMIC comprises a frequency multiplier-by-three, a quadrature balanced mixer, an LNA and an antenna. The functional block diagram of the receiver MMIC is shown Fig. 6.23.

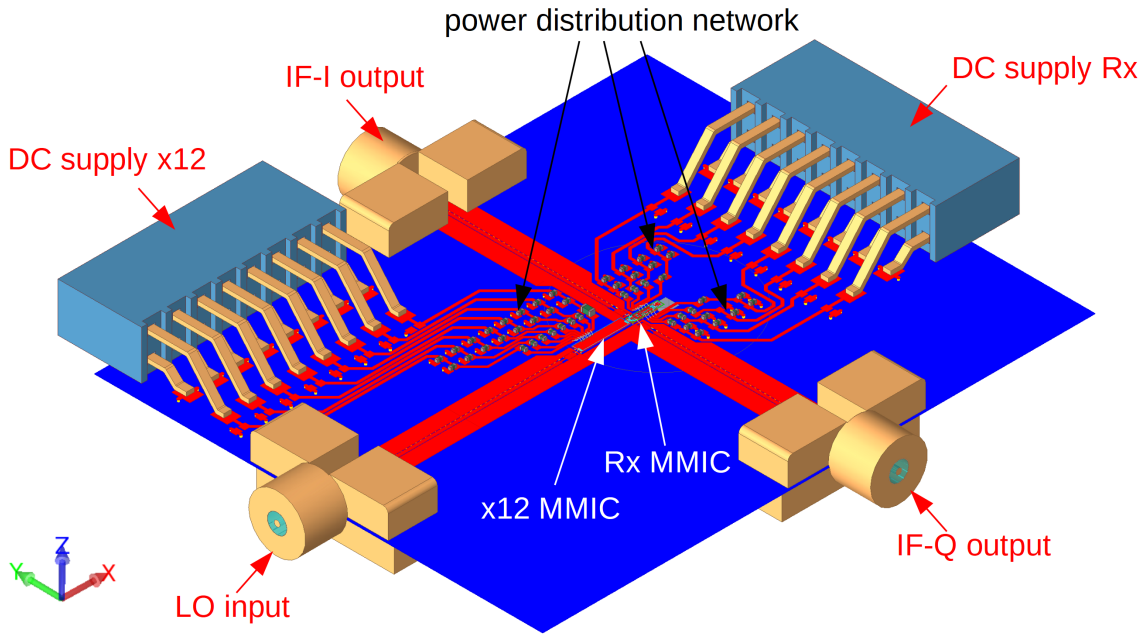

Figure 6.21.: Top view of the PCB including two DC connectors and three high frequency connectors. The MMICs are mounted in the center of the PCB and connected using bondwires.

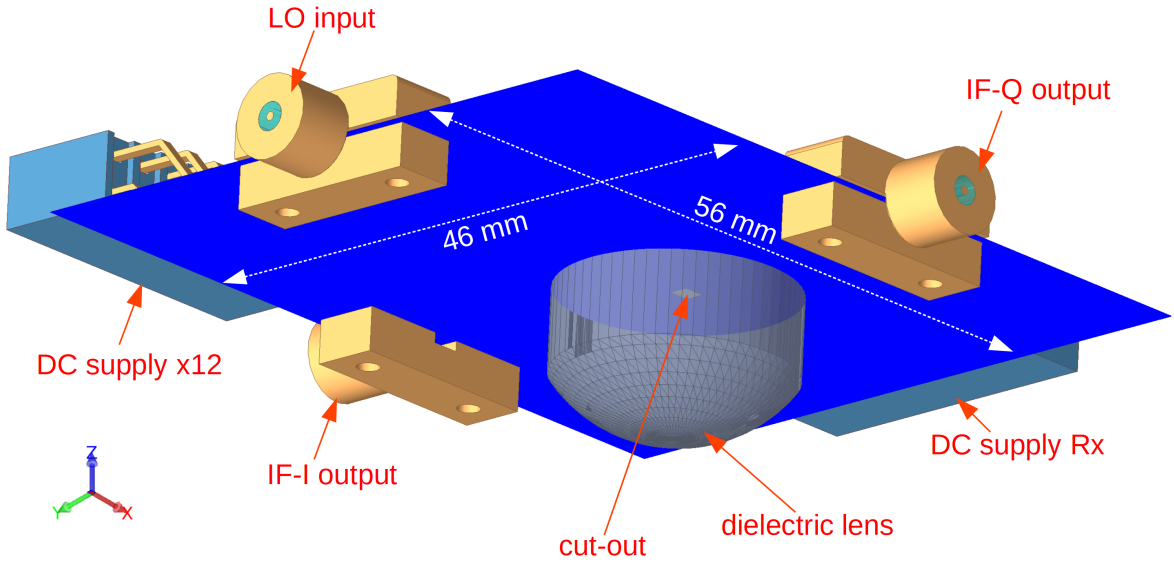

Figure 6.22.: Bottom view of the PCB. Clearly visible the lens dedicated to increase the overall antenna directivity of the receiver. A small cut-out in the bottom metal (blue) of the board allows the incoming radiation to access the antenna of the receive MMIC that is mounted on the top side. The board dimensions are 46 mm x 56 mm.

The MMIC is designed to operate at a center frequency of 300 GHz, to have an RF bandwidth of at least 50 GHz, an overall conversion gain of 10 dB and a $\mathrm{IP}_{1\mathrm{dB}}$ of -27 dBm.
The frequency tripler is similar to the design presented in chapter 6.2, but shifted in frequency to meet the center frequency of 300 GHz. No stand-alone version was fabricated, therefore no measurement results for this component can be presented. Fig 6.24 shows the simulated output power versus the input power and the output frequency.

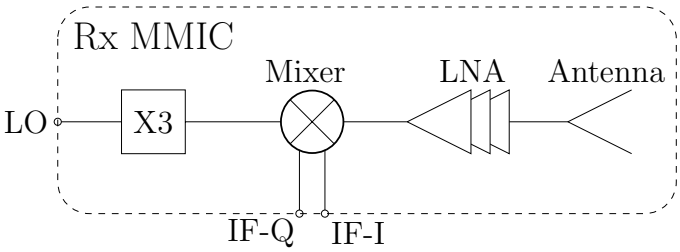

Figure 6.23.: Functional block diagram of the quadrature balanced down-converter comprising a frequency multiplier-by-three, a balanced quadrature mixer, an LNA and an integrated antenna.

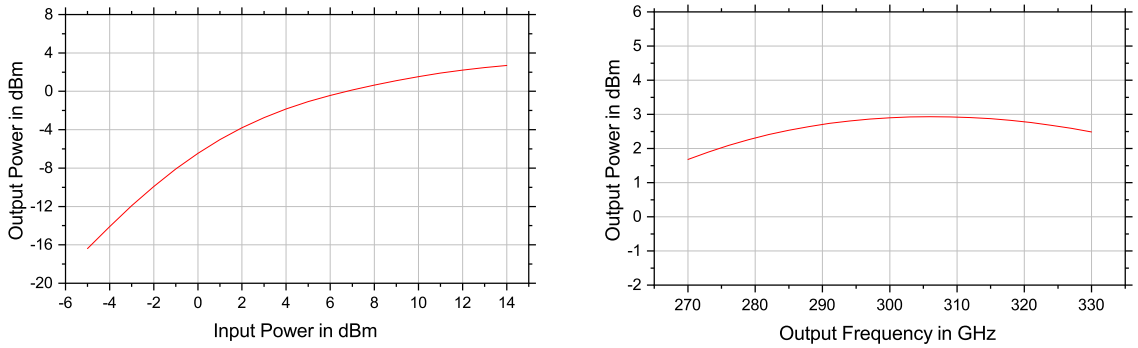

Figure 6.24.: Simulated output power versus input power (left) and versus output frequency (right) of the frequency multiplier-by-three integrated as the first stage of the quadrature balanced down-converter.

In the targeted assembly the frequency tripler will be driven by a frequency multiplier-by-twelve. The x12 provides 10 dBm output power at 100 GHz. Therefore, the input power in the frequency depended simulation was set to 10 dBm. Under these conditions, the x3 shows a very broadband behavior. The 3 dB bandwidth is wider than 60 GHz which makes it robust against process variations. The output power is around 3 dBm. A high output power is necessary because it will be distributed to four mixing cells which decreases the power per stage by 6 dB. Additionally, the loss of the couplers has to be compensated.
The mixer design is based on the ICC dual-gate down-converter with active load (AL1) presented in chapter 5.1.1 with a transistor gate width of 20 µm. However, to suppress the LO at the RF port a balanced design was employed. The topology with quadrature hybrid couplers as presented in chapter 2.2.1.1 was chosen. It was integrated in the in-phase and quadrature branch of the mixer. That means, that four dual-gate mixing cells are needed. TandemX couplers identical to those presented in [DMW+15] were used. The resulting block diagram is shown in Fig. 6.25
The design from chapter 5.1.1 was adjusted to support an LO frequency of 300 GHz. The 3 dBm output power of the tripler has to be devided by 4, hence minus 6 dB, to account for the couplers. So, ideally the LO power at each mixing stage calculates to −3 dBm. This corresponds well to the gain maximum for the dual-gate down-converter presented in chapter 5.1.1. However, taking into account the overly optimistic transistor model and losses in the couplers, a realistic power at the LO input will lie around 3 dB below that. Therefore, the mixer design was optimized to achieve maximum gain at even lower LO input power levels of around −6 dBm.

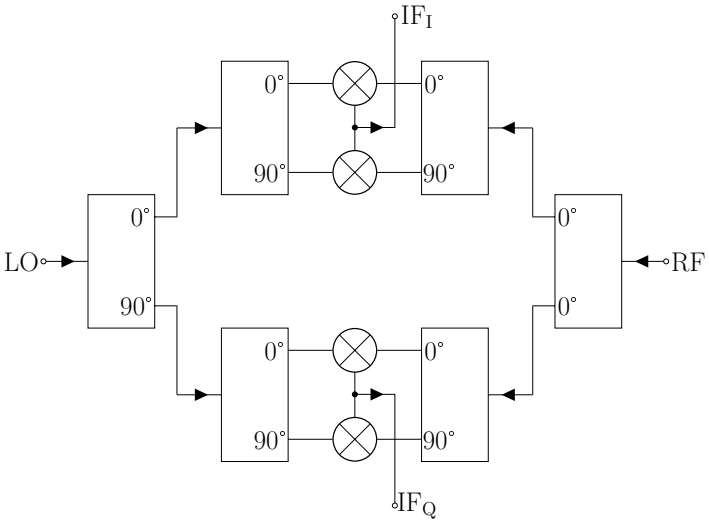

Figure 6.25.: A functional block diagram the balanced, quadrature dual-gate down-converter consisting of four mixer cells, five quadrature, hybrid couplers and a Wilkinson power splitter.

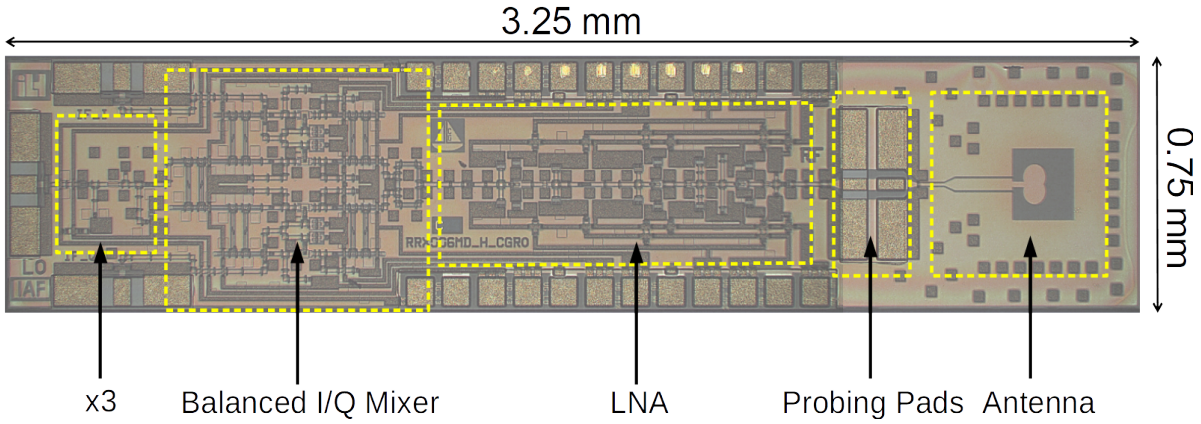

Figure 6.26.: A chip photograph of the receiver MMIC. The yellow rectangles mark the single building blocks, x3, quadrature mixer, LNA, on-wafer probing pads and the antenna. The chip size is 3250 µm x 750 µm.

To amplify the input signal and improve the noise figure of the system a 3-stage LNA was integrated. It is similar to the design presented in [6]. It exhibits a gain of around 26 dB, has a 3 dB bandwidth of 80 GHz and a $\mathrm{IP}_{1\mathrm{dB}}$ of -26 dBm.
Fig. 6.26 shows a chip photograph of the MMIC. The chip size is 3250 µm x 750 µm.
Two pads are placed between antenna and LNA. These can be used to bypass the antenna and enable an on-wafer characterization of the circuit without the need of an "over the air" measurement setup. Furthermore, they create the possibility to separate the antenna from the MMIC to perform stand-alone measurements.

6.3.1.2. Antenna Design

The antenna was designed to radiate through the GaAs substrate and the substrate of the PCB on which the chip is mounted. For that purpose, the backside metallization of the MMIC was cut out to form a window. The antenna gain was then maximized for the lower radiation hemisphere. The PCB is included in the simulation to consider its influence on

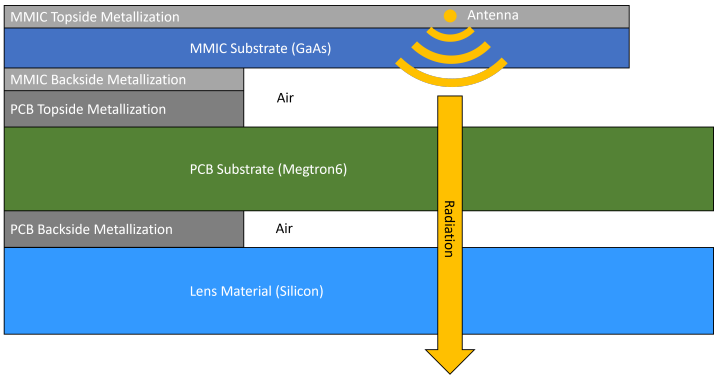

Figure 6.27.: Cross section of the layer stack used for the antenna simulation (not to scale).

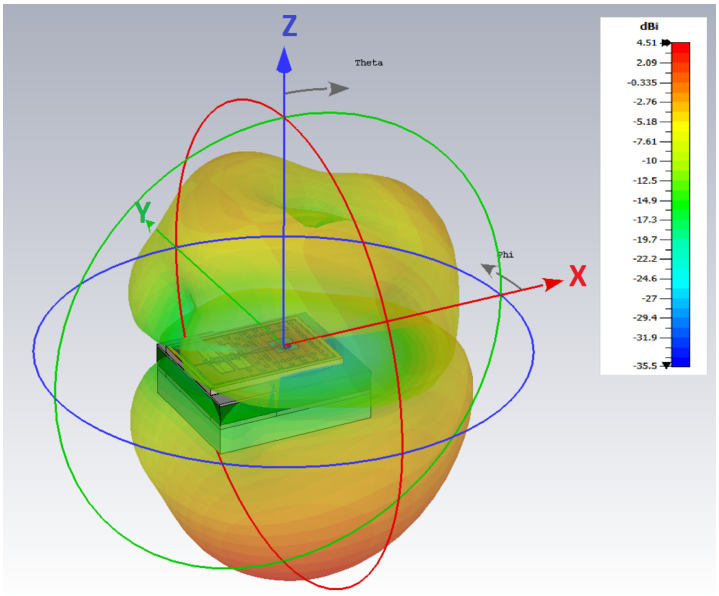

Figure 6.28.: The simulated 3D radiation pattern of the integrated antenna at 300 GHz. The maximum gain of 4.5 dBi is achieved while radiating through the MMIC and PCB substrates and a subsequent silicon layer.

the radiation properties as well. To enable high frequency transmission lines on the PCB the low loss material Megtron6 was chosen as PCB substrate. An additional silicon layer is attached to the bottom side of the PCB to model the material transition from the PCB substrate to the silicon lens that will be used to increase the directivity in the final assembly. The cross section of the layer stack used for simulating the antenna is depicted in Fig. 6.27. Fig. 6.28 shows the employed FEM model of the antenna with its simulated radiation pattern at 300 GHz. The corresponding polar plots for a constant ϕ of 180° and 90° at 300 GHz are depicted in Fig. 6.29. The antenna gain at 300 GHz is 4.5 dB. Additional radiation patterns for the frequency range from 270 to 330 GHz can be found in Annex D.
As expected, the antenna lacks directivity and the main lobe is very broad. Therefore, as described earlier and depicted in the bottom view of the PCB, Fig. 6.22, a silicon lens will be used to focus the beam in the final assembly to compensate the poor directivity, similar to the setup in [RGS+18].
In Fig. 6.30 the total efficiency for the lower hemisphere is plotted which is the ratio of the

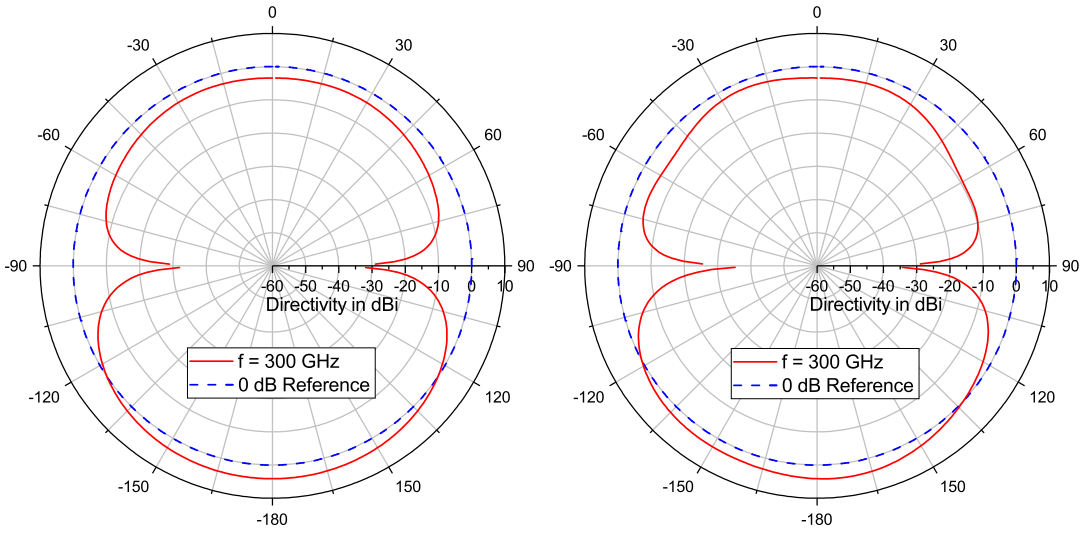

Figure 6.29.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 300 GHz.

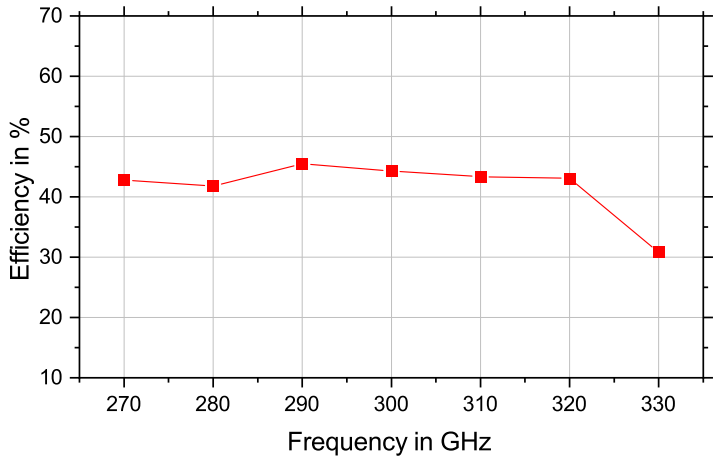

Figure 6.30.: The radiation efficiency for the lower hemisphere for the frequency range from 270 to 330 GHz.

power radiated in the lower hemisphere and the total input power:

$$\eta = \frac{P_{\text{radiated,LH}}}{P_{\text{input}}} \tag{6.2}$$

It includes circuit loss and mismatch and presents thereby a good figure of merit for the performance of the antenna. The main reduction of efficiency is due to the radiation to the upper hemisphere which is still strong as can be seen in Fig. 6.28.

6.3.2. Measurement Results

As described in chapter 6.3.1.1 pads for an RF measurement were placed between the LNA and the antenna to enable an on-wafer measurement of the circuit. Conventionally, the pad is only connected to the DuT. But, in this case the open end of the pad leads to the antenna. This introduces distortion to the circuit. Part of the signal applied to the circuit via the probe will also travel in the direction of the antenna which is designed to radiate at exactly these frequencies. Furthermore, the impedance of the pad will change which results

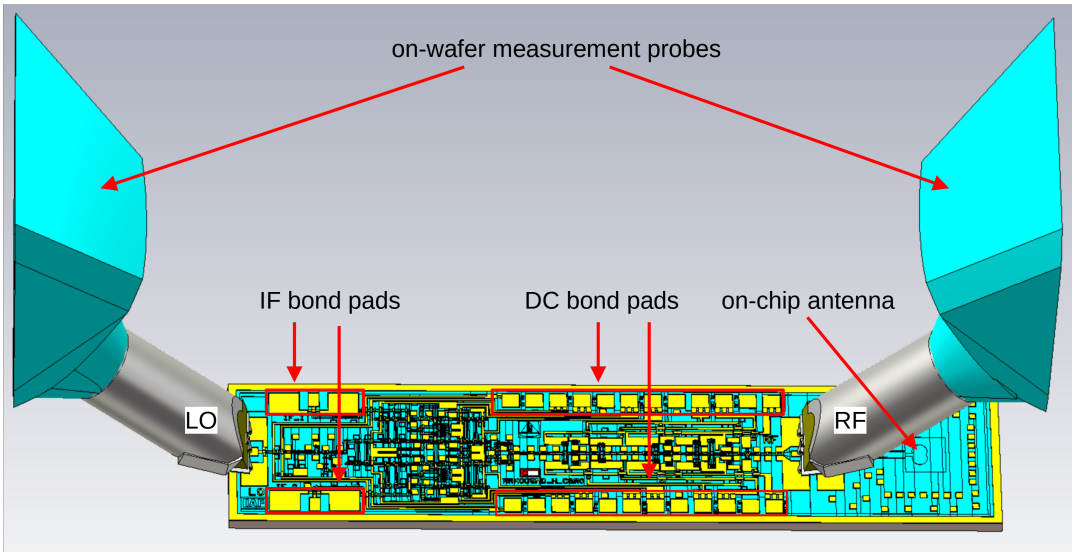

Figure 6.31.: A visualization of the measurement setup with on-wafer measurement probes.

in an increased reflection from the DuT. Additionally, to enable a separation of antenna and receiver circuit later on, two vias had to be removed from the conventional layout of the pad. As describe in detail in [Mül18], the via placement can have a noticeable impact on the on-wafer measurement. The setup of the on-wafer measurements that will be presented in the following is visualized in Fig. 6.31.
As can be seen, in the on-wafer measurement the entire receiver MMIC incl. antenna was measured . Therefore, only a certain part of the applied power will reach the circuit. This can be regarded as an additional loss, L_{setup}

$$P_{in} = P_{applied} - L_{setup} \tag{6.3}$$

Hence, values like the output power and the conversion gain will be affected by that. However, several conclusions can still be drawn from the measurements. Firstly, the overall functionality of a circuit can be proven. Secondly, figures of merit such as $\mathrm{OP}_{1\mathrm{dB}}$ and necessary LO power are still accurate. Thirdly, a relative comparison between several cells on a wafer can be conducted. Hereby, it provides a measure to pick the best cells for the assembly.
First of all the CG versus the LO power was measured. The RF frequency was set to 300.2 GHz, the LO to 100 GHz which generates an LO at the mixing cells of 300 GHz and a down-converted IF of 200 MHz. Fig. 6.32 shows the results.
The measurement setup was limited to a maximum LO power of 8 dBm, therefore the targeted 10 dBm was not reached. However, the circuit is already saturating for lower power levels, which means that the conversion gain at 10 dBm will be very similar to that at 8 dBm. A conversion gain of -11 dB was reached. This is about 22 dB below the simulated value.
For a circuit of this complexity and at these high frequencies, deviations from the simulation results are not unusual as for example also visible in the measurement results presented in chapter 5.2.3 or 6.2. However, these deviations lie more in the range of 2 to maximum 5 dB. Hence, even when taking into account overly optimistic simulation results, the difference between simulation and measurement is extremely high. As described initially in this chapter, the measurement setup was not ideal and prone to introduce additional losses. Therefore, this strong deviation is attributed to these suboptimal measurement conditions.

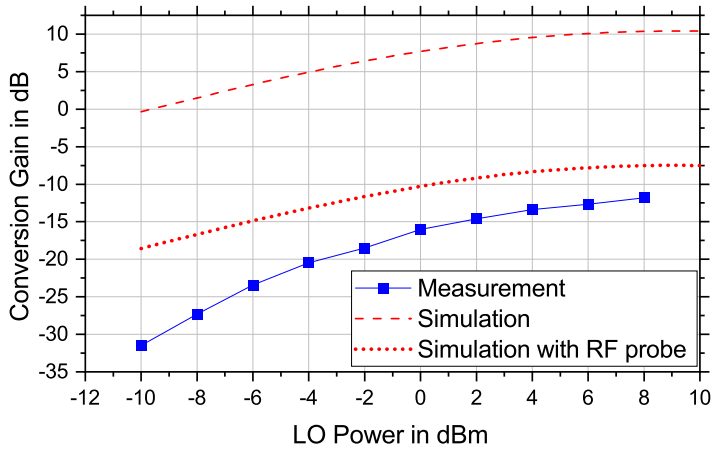

Figure 6.32.: The simulated (with and without measurement probe) and measured conversion gain of the receiver MMIC in dependency of LO power at an LO frequency of 100 GHz, an RF frequency of 300.2 GHz and a RF power of −30 dBm.

To give a rough estimation of the losses introduced by the non-ideal probing of the circuit, an additional FEM simulation was conducted. This simulation only included the part of the MMIC right of the LNA, meaning the RF contact pads, the RF measurement probe and the antenna. Moreover, the MMIC was placed on a large conductive plane to model the chuck. From this simulation the transmission from probe input to input of the LNA was extracted. These results can be used as a first order approximation of the parasitic effects introduced by the measurement setup. If these simulation results are added to the full MMIC simulation of conversion gain versus LO input power as also shown in Fig. 6.32, the deviation decreases to 4 dB which is still high but in a more realistic range of difference between measurement and simulation.

With the maximum available LO power of 8 dBm, the next measurement was performed. A sweep of the RF power for a constant LO and RF. This yields the linearity of the circuit. It is visualized in Fig. 6.33.

The circuit is linear below −27 dBm. The $\mathrm{IP}_{1\mathrm{dB}}$ is around −25.5 dBm which leads with a CG of −13.5 dB to a $\mathrm{OP}_{1\mathrm{dB}}$ of −39 dBm. The measured $\mathrm{IP}_{1\mathrm{dB}}$ matches the simulated one at −27 dBm very well. The simulated $\mathrm{OP}_{1\mathrm{dB}}$ lies around 20 dB higher at −18 dBm.

In chapter 6.2 the identical LNA and also a dual-gate down-converter were integrated in the MMIC. That receiver exhibited an $\mathrm{IP}_{1\mathrm{dB}}$ range of −31 dBm to −37 dBm, the simulated $\mathrm{IP}_{1\mathrm{dB}}$ was −35 dBm which is 10 dB lower than the $\mathrm{IP}_{1\mathrm{dB}}$ of this MMIC. However, that receiver was a single-ended version. If we consider that and we examine the $\mathrm{IP}_{1\mathrm{dB}}$ per mixing stage to have a fair comparison, the $\mathrm{IP}_{1\mathrm{dB}}$ will decrease by at least 6 dB due to the power distribution to four cells. Accounting for the coupler losses with another 2 dB, the resulting $\mathrm{IP}_{1\mathrm{dB}}$ per mixing stage results in around −33 dBm. This matches the linearity range shown in Fig. 6.16 of the single-ended stage in chapter 6.2. Moreover, if we compare the $\mathrm{OP}_{1\mathrm{dB}}$ which is calculated from the $\mathrm{IP}_{1\mathrm{dB}}$ and the CG, in chapter 6.2 −20 dBm was achieved. This is 19 dB higher than the $\mathrm{OP}_{1\mathrm{dB}}$ shown in Fig. 6.33. This corresponds to the conversion gain difference between measurement and simulation for this MMIC. That means that the linearity of the single-ended mixing cells of the MMIC presented in chapter 6.2 and in this chapter are well in accordance.

Eventually, the frequency dependent behavior was examined. The RF was swept from 280 GHz

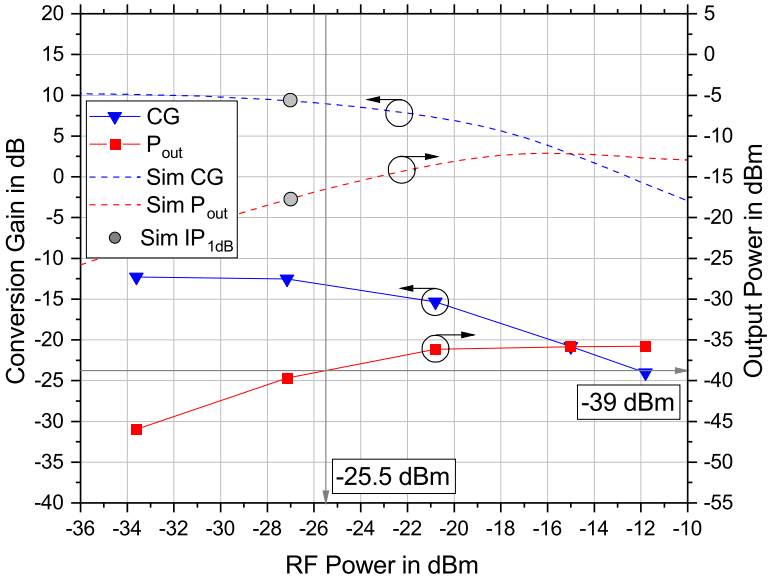

Figure 6.33.: The simulated and measured conversion gain of the receiver MMIC versus RF power at an LO frequency of 100 GHz, an RF frequency of 300.2 GHz and an LO power of 8 dBm.

to 320 GHz. The LO power level was kept at 8 dBm, the RF power level set to −35 dBm and the LO frequency was 100 GHz. The measurement result is depicted in Fig. 6.34.
As expected the overall conversion gain is very low and a clear deviation between upper sideband and lower sideband is visible. The USB has a slightly higher CG near the carrier and exhibits an overall flatter conversion gain curve. The LSB declines more steeply to lower frequencies, that translate to higher IF frequencies in the BB. The different behavior for the LSB and USB reminds of the gain curves of the ICC version presented in chapter 5.1.1, Fig. 5.13 and chapter 5.2.2, Fig. 5.34, only with the difference, that in the ICC version the USB instead of the LSB was affected. This might indicate in this case a shift of the optimal

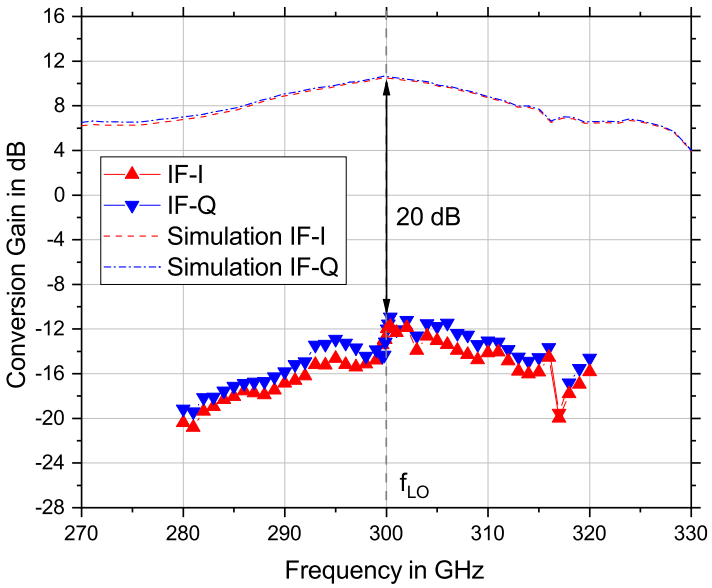

Figure 6.34.: The simulated and measured conversion gain of the receiver MMIC over the RF frequency at an LO frequency of 100 GHz, an LO power of 8 dBm and an RF power of −30 dBm.

matching to higher instead of lower frequencies. Also, the 3 dB bandwidth of the the I and Q channel are slightly different. It amounts to 20 GHz for I and to 27 GHz for Q. This is far below the bandwidth targeted for the application. However, as discussed in the beginning, the measurement setup impairs the results not only regarding the conversion gain but also in terms of frequency behavior.
Hence, assuming that the measurement setup causes the CG to drop by around $L_{setup} = 20$ dB due to mismatches and power radiated by the antenna, the results also compare well to the results presented in chapter 6.2, where the same LNA was employed and also a dual-gate ICC down-converter.
Due to the impaired measurements, a comparison with the state-of-the-art receivers that integrate an antenna will be forgone until over-the-air measurements are performed and a fair evaluation is possible.

7. Conclusion and Outlook

Following up on 5G, the sixth generation of mobile communication will have to increase the operating frequencies even further to meet future demand in data rate. The H-band has proven to be a good candidate for the usage in future communication systems by offering large bandwidths, atmospheric windows and small device sizes. Examples for these applications were discussed in chapter 6.2 and 6.3. But, not only communication systems will benefit from using higher frequencies. For radar applications terahertz frequencies will result in higher possible resolutions, but still maintain the ability to penetrate materials that appear opaque at visible light frequencies. Here, the first thing that comes to mind are security applications [CSW+14], but it can also be used for medical [KVM+16] or material testing purposes [MMW+19], as described in chapter 6.1. The list can be continued with spectroscopy, radio astronomy and many more.

This thesis focused on nonlinear components and presented in particular circuits for frequency conversion. The purpose was to discuss different mixer architectures and to evaluate their performance for future terahertz radar and communication systems. Furthermore, the integration of these architectures to form mixer topologies for different applications was picked as an additional theme. Overall, this work is supposed to provide guidance for choosing and simulating the best suited mixer design and helping to overcome occurring difficulties. From nonlinear simulation techniques in chapter 3 with a special focus on stability, to the single up- and down-conversion mixer architectures in chapter 5 to complete homo- and heterodyne communication receivers and radar systems in chapter 6. Each of these steps provide detailed information on the (circuit) design, a discussion of the achieved results and the advantages and disadvantages compared to similar state-of-the-art approaches.

Although many terahertz projects were completed and a manifold of MMICs were fabricated over the last years, to the author's best knowledge, several approaches and designs in this work were the first of their kind for terahertz frequencies in H-band (220 to 320 GHz) using that particular technology. They are highlighted in the following paragraphs.

The dual-gate mixer is an architecture that is well established in literature, however neither for up- nor for down-conversion has it been discussed before for the lower terahertz band. Not only is it analyzed in detail in this work, but also several versions of it were presented: Different DC decoupling measures were introduced, a resistive and an active load, as well as different transistor layouts. The active dual-gate mixer in a balanced, quadrature topology was eventually integrated with a frequency multiplier, an LNA and an antenna to form a homodyne receiver at 300 GHz. Furthermore, a single-ended version was adjusted to provide mixing to an IF in W-band and it was integrated into a fully functional heterodyne receiver suitable for multi-channel data transmission at 300 GHz.

The slightly more complex half Gilbert cell up-converter circuit, comprising a passive hybrid coupler and also two different transistor layouts, achieved an outstanding performance at very low LO input power levels.

The gate-pumped transconductance mixer provides an easy-to-design example for an active

up-converter exhibiting a large bandwidth, a low necessary LO driving power and a decent linearity.

The most obvious future prospect is to keep on optimizing the presented mixers. Since the passive, resistive FET mixer architecture was improved over several design cycles, its performance is already optimized. However, the presented active designs are a first generation of active mixers in the InGaAs technology presented in chapter 4. Although, the measured results are very satisfying for a first generation, they leave room for improvement: The simulation model can be refined, especially for the integrated conversion cell layouts of the active dual-gate mixer where no proper model exists yet. Extensive load pull analyses, also at the harmonics and intermodulation products, should be performed to maximize conversion gain, linearity or necessary LO drive power. Also the integration of subsequent amplifier stages like a transimpedance amplifier (TIA) could improve the performance. Moreover, the integration with an LO generation chain would extend the LO power range to saturate the mixer stages and hereby not only increase the conversion gain in many cases but also deliver a more complete behavioral description of the mixer.
The main disadvantage, as presented, is the linearity of the active frequency converters. Therefore a special focus should be put on investigating what limits the linearity of the active designs and, if and how it can be improved by using conventional linearization techniques.
Additionally, active couplers for terahertz frequencies can help to cut the losses in cascaded passive feed networks for MMICs with a high integration level, for example in the circuit presented in chapter 6.3. Eventually, the progress that is made with electro-magnetic field simulators is immense. This can be leveraged to fully simulate an entire MMIC and to help to predict the circuit's behavior more realistically.
This work provides the proper foundation to tackle all these issues and help to improve nonlinear circuit design for future terahertz applications.

A. Equation-Based Approach for Mixer Topologies

The presented visual approach to explain the functionality of the balanced up- and down-converter or quadrature mixing facilitates a quick understanding. But of course, all the steps presented in chapter 2.2 can also be described in a more abstract, analytic fashion. Therefore, for the sake of completeness, in the following, the corresponding analytic description of each step for the examples presented will be performed. Since a detailed commenting was already performed in chapter 2.2 it is considered redundant here. Furthermore, please note, since an ideal environment with total symmetry of the paths and couplers is assumed, the amplitude of the signals is neglected. When such a simplification is used, a $\Rightarrow$ replaces an $=$, for example:

$$\cos[(\omega_{LO} + \omega_{IF})t] + \cos[(\omega_{LO} + \omega_{IF})t] \Rightarrow \cos[(\omega_{LO} + \omega_{IF})t] \tag{A.1}$$

A.1. Balanced Mixers

A.1.1. Quadrature Hybrid

Up-converter The following equations correspond to the depictions in Fig. 2.13 to Fig. 2.16.

(LO) $\cos(\omega_{LO}t)$

(IF_1) $\cos(\omega_{IF}t)$

(IF_2) $\cos(\omega_{IF}t + 180°)$

(1) $\cos(\omega_{LO}t)$

(2) $\cos(\omega_{LO}t + 90°)$

(3) $\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t)$

(4) $\cos[(\omega_{LO} + \omega_{IF})t + 90° + 180°] + \cos(\omega_{LO}t + 90°)$
$= \cos[(\omega_{LO} + \omega_{IF})t + 270°] + \cos(\omega_{LO}t + 90°)$

(RF_1) $\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t)$

(RF_2) $\cos[(\omega_{LO} + \omega_{IF})t + 270° + 90°] + \cos(\omega_{LO}t + 90° + 90°)$
$= \cos[(\omega_{LO} + \omega_{IF})t + 360°] + \cos(\omega_{LO}t + 180°)$

(RF) $\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t) + \cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t + 180°)$
$= 2\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t) - \cos(\omega_{LO}t)$
$\Rightarrow \cos[(\omega_{LO} + \omega_{IF})t]$

Down-converter The following equations correspond to the depictions in Fig. 2.17 to Fig. 2.19.

(LO) $\cos(\omega_{LO}t)$

(RF) $\cos[(\omega_{LO} + \omega_{IF})t]$

(1) $\cos(\omega_{LO}t)$

(2) $\cos(\omega_{LO}t + 90°)$

(3) $\cos[(\omega_{LO} + \omega_{IF})t]$

(4) $\cos[(\omega_{LO} + \omega_{IF})t + 90°]$

(IF_1) $\cos[(\omega_{LO} + \omega_{IF} - \omega_{LO})t$
$= \cos(\omega_{IF}t)$

(IF_2) $\cos[(\omega_{LO} + \omega_{IF} - \omega_{LO})t + 90° - 90°]$
$= \cos(\omega_{IF}t)$

A.1.2. 180° Hybrid and Power Combiner

Up-converter The following equations correspond to the depiction in Fig. 2.21.

(LO) $\cos(\omega_{LO}t)$

(IF_1) $\cos(\omega_{IF}t)$

(IF_2) $\cos(\omega_{IF}t + 180°)$

(1) $\cos(\omega_{LO}t)$

(2) $\cos(\omega_{LO}t + 180°)$

(3) $\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t)$

(4) $\cos[(\omega_{LO} + \omega_{IF})t + 180° + 180°] + \cos(\omega_{LO}t + 90°)$
$= \cos[(\omega_{LO} + \omega_{IF})t + 360°] + \cos(\omega_{LO}t + 180°)$

(RF) $\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t) + \cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t + 180°)$
$= 2\cos[(\omega_{LO} + \omega_{IF})t] + \cos(\omega_{LO}t) - \cos(\omega_{LO}t)$
$\Rightarrow \cos[(\omega_{LO} + \omega_{IF})t]$

Down-converter The following equations correspond to the depiction in Fig. 2.22.

(LO) $\cos(\omega_{LO}t)$

(RF) $\cos[(\omega_{LO} + \omega_{IF})t]$

(1) $\cos(\omega_{LO}t)$

(2) $\cos(\omega_{LO}t + 180°)$

(3) $\cos[(\omega_{LO} + \omega_{IF})t]$

(4) $\cos[(\omega_{LO} + \omega_{IF})t]$

(IF_1) $\cos[(\omega_{LO} + \omega_{IF} - \omega_{LO})t$
$= \cos(\omega_{IF}t)$

(IF_2) $\cos[(\omega_{LO} + \omega_{IF} - \omega_{LO})t - 180°]$
$= -\cos(\omega_{IF}t)$

A.2. Quadrature Mixers

The following equations correspond to the depictions in Fig. 2.24 to Fig. 2.26.

(LO)
$$e^{j(\omega_{LO}t)} + e^{-j(\omega_{LO}t)}$$

(IF_I)
$$e^{j(\omega_{IF_I}t)} + e^{-j(\omega_{IF_I}t)}$$

(IF_Q)
$$e^{j(\omega_{IF_Q}t)} + e^{-j(\omega_{IF_Q}t)}$$

(1)
$$e^{j(\omega_{LO}t)} + e^{-j(\omega_{LO}t)}$$

(2)
$$e^{j(\omega_{LO}t+90°)} + e^{-j(\omega_{LO}t+90°)}$$

(3)
$$e^{j[(\omega_{LO}+\omega_{IF_I})t]} + e^{-j[(\omega_{LO}+\omega_{IF_I})t]} + e^{j[(\omega_{LO}-\omega_{IF_I})t]} + e^{-j[(\omega_{LO}-\omega_{IF_I})t]}$$

(4)
$$e^{j[(\omega_{LO}+\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}+\omega_{IF_Q})t+90°]} + e^{j[(\omega_{LO}-\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}-\omega_{IF_Q})t+90°]}$$

(RF)
$$\begin{aligned}&e^{j[(\omega_{LO}+\omega_{IF_I})t]} + e^{-j[(\omega_{LO}+\omega_{IF_I})t]} + e^{j[(\omega_{LO}-\omega_{IF_I})t]} + e^{-j[(\omega_{LO}-\omega_{IF_I})t]}\\ &+ e^{j[(\omega_{LO}+\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}+\omega_{IF_Q})t+90°]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}-\omega_{IF_Q})t+90°]}\end{aligned}$$

(3′) (4′)
$$\begin{aligned}&e^{j[(\omega_{LO}+\omega_{IF_I})t]} + e^{-j[(\omega_{LO}+\omega_{IF_I})t]} + e^{j[(\omega_{LO}-\omega_{IF_I})t]} + e^{-j[(\omega_{LO}-\omega_{IF_I})t]}\\ &+ e^{j[(\omega_{LO}+\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}+\omega_{IF_Q})t+90°]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_Q})t+90°]} + e^{-j[(\omega_{LO}-\omega_{IF_Q})t+90°]}\end{aligned}$$

(IF_I)
$$\begin{aligned}&e^{j[(\omega_{LO}+\omega_{IF_I}-\omega_{LO})t]} + e^{-j[(\omega_{LO}+\omega_{IF_I}-\omega_{LO})t]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_I}-\omega_{LO})t]} + e^{-j[(\omega_{LO}-\omega_{IF_I}-\omega_{LO})t]}\\ &+ e^{j[(\omega_{LO}+\omega_{IF_Q}-\omega_{LO})t+90°]} + e^{-j[(\omega_{LO}+\omega_{IF_Q}-\omega_{LO})t+90°]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_Q}-\omega_{LO})t+90°]} + e^{-j[(\omega_{LO}-\omega_{IF_Q}-\omega_{LO})t+90°]}\\ &= e^{j(\omega_{IF_I})t} + e^{-j(\omega_{IF_I})t} + e^{j(-\omega_{IF_I})t} + e^{-j(-\omega_{IF_I})t}\\ &+ e^{j(\omega_{IF_Q}t+90°)} + e^{-j(\omega_{IF_Q}t+90°)} + e^{j(-\omega_{IF_Q}t+90°)} + e^{-j(-\omega_{IF_Q}t+90°)}\\ &= e^{j(\omega_{IF_I})t} + e^{-j(\omega_{IF_I})t} + e^{j(\omega_{IF_I})t} + e^{-j(\omega_{IF_I})t}\\ &+ e^{j(\omega_{IF_Q}t+90°)} + e^{-j(\omega_{IF_Q}t+90°)} + e^{-j(\omega_{IF_Q}t-90°)} + e^{j(\omega_{IF_Q}t-90°)}\\ &\Rightarrow \cos(\omega_{IF_I}t) + \cos(\omega_{IF_I}t) + \cos(\omega_{IF_Q}t+90°) + \cos(\omega_{IF_I}t-90°)\\ &\Rightarrow \cos(\omega_{IF_I}t) + \sin(\omega_{IF_Q}t) - \sin(\omega_{IF_Q}t)\\ &=\cos(\omega_{IF_I}t)\end{aligned}$$

(IF_Q)
$$\begin{aligned}&e^{j[(\omega_{LO}+\omega_{IF_I}-\omega_{LO})t-90°]} + e^{-j[(\omega_{LO}+\omega_{IF_I}-\omega_{LO})t-90°]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_I}-\omega_{LO})t-90°]} + e^{-j[(\omega_{LO}-\omega_{IF_I}-\omega_{LO})t-90°]}\\ &+ e^{j[(\omega_{LO}+\omega_{IF_Q}-\omega_{LO})t+90°-90°]} + e^{-j[(\omega_{LO}+\omega_{IF_Q}-\omega_{LO})t+90°-90°]}\\ &+ e^{j[(\omega_{LO}-\omega_{IF_Q}-\omega_{LO})t+90°-90°]} + e^{-j[(\omega_{LO}-\omega_{IF_Q}-\omega_{LO})t+90°-90°]}\\ &= e^{j(\omega_{IF_I}t-90°)} + e^{-j(\omega_{IF_I}t-90°)} + e^{j(-\omega_{IF_I}t-90°)} + e^{-j(-\omega_{IF_I}t-90°)}\\ &+ e^{j(\omega_{IF_Q}t)} + e^{-j(\omega_{IF_Q}t)} + e^{j(-\omega_{IF_Q}t)} + e^{-j(-\omega_{IF_Q}t)}\\ &= e^{j(\omega_{IF_I}t-90°)} + e^{-j(\omega_{IF_I}t-90°)} + e^{-j(\omega_{IF_I}t+90°)} + e^{j(\omega_{IF_I}t+90°)}\\ &+ e^{j(\omega_{IF_Q}t)} + e^{-j(\omega_{IF_Q}t)} + e^{-j(\omega_{IF_Q}t)} + e^{j(\omega_{IF_Q}t)}\\ &\Rightarrow \cos(\omega_{IF_I}t+90°) + \cos(\omega_{IF_I}t-90°) + \cos(\omega_{IF_Q}t) + \cos(\omega_{IF_Q}t)\\ &\Rightarrow \sin(\omega_{IF_I}t) - \sin(\omega_{IF_I}t) + \cos(\omega_{IF_Q}t)\\ &=\cos(\omega_{IF_Q}t)\end{aligned}$$

B. Cross-Section of Most Commenly Used Components

The most commonly used components for the technology presented in chapter 4 are the series and parallel capacitor as well as the NiCr resistor. These components are usually embedded in the coplanar waveguide environment as shown in Fig. 4.2. However, the same section that forms the capacitance of the series capacitor, meaning the stacking of MET1, MET2, SiN and MET3 is also used to create MIM capacitors outside of the CPWG environment. An overview of the layer stack cross-sections of these components is presented in Fig. B.1 to Fig. B.3. Please note, the purpose of these visualizations is to give an impression of the layer stack and its topography and the drawings are not true to scale.

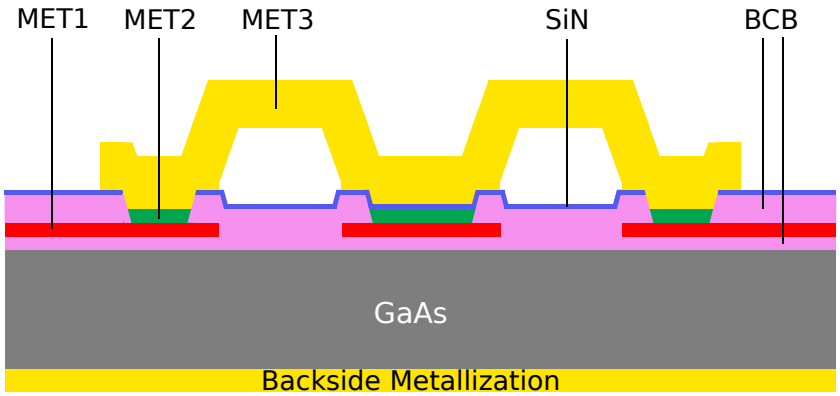

Figure B.1.: The cross-sections of a parallel capacitor embedded in a grounded coplanar waveguide.

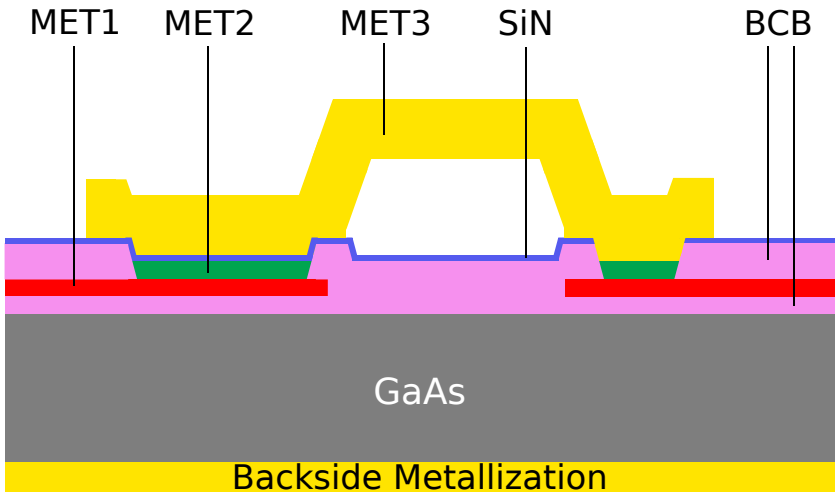

Figure B.2.: The cross-sections of a series capacitor embedded in a grounded coplanar waveguide.

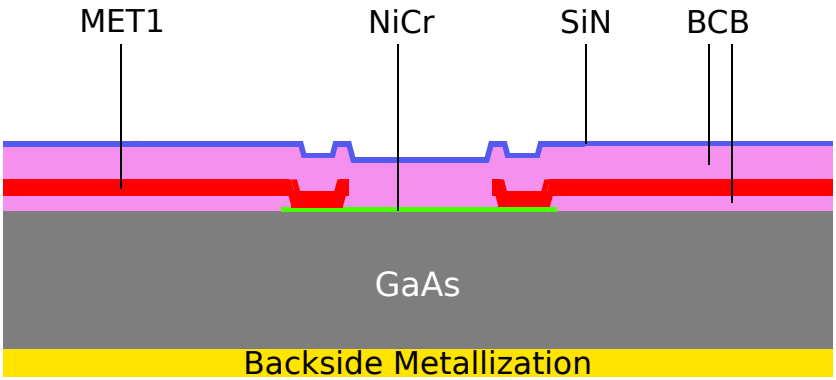

Figure B.3.: The cross-sections of a NiCr resistor.

C. Antenna Geometry

In the following the geometry of the antenna presented in chapter 6.3 is described in detail.

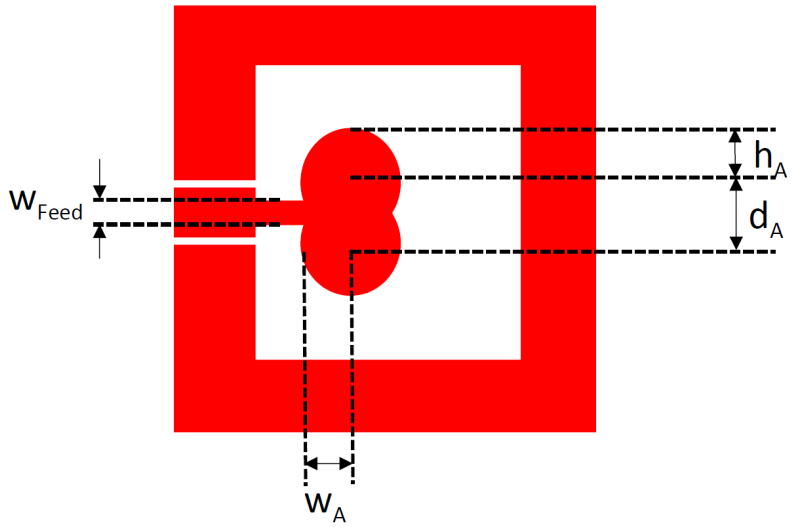

Figure C.1.: The magnified radiator of the antenna presented in chapter 6.3 with labels.

Table C.1.: Description and values of the parameters shown in Fig. C.1.

h_A	Height of antenna elipsoid	34.5 µm
w_A	Width of antenna elipsoid	32 µm
d_A	Distance between both antenna elipsoid centers	39 µm
w_{Feed}	Width of antenna feedline	61 µm

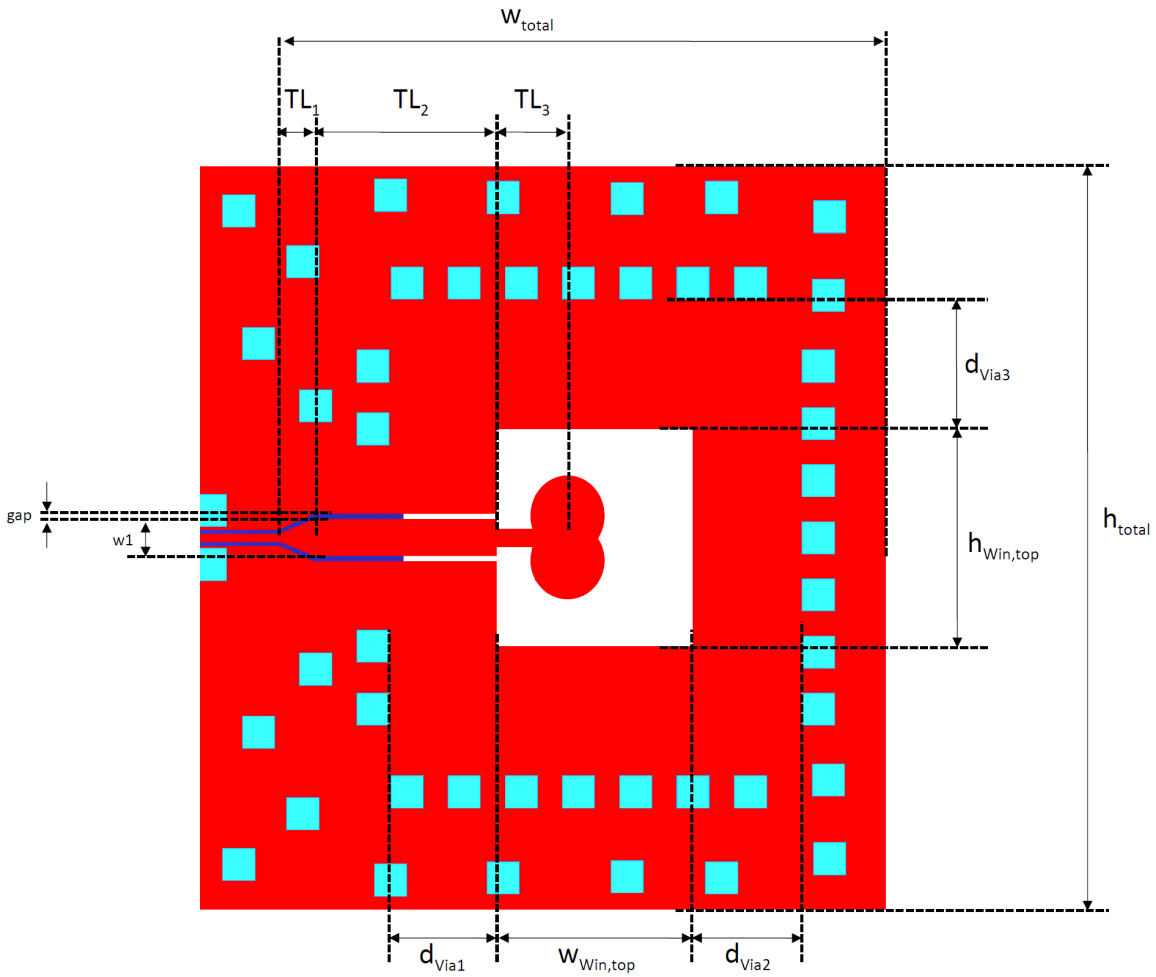

Figure C.2.: Top view of the antenna presented in chapter 6.3 with labels.

Table C.2.: Description and values of the parameters shown in Fig. C.2.

TL_1	Length of taper	30 µm
TL_2	Length of 1st section feedline	160 µm
TL_3	Length of 2nd section feedline	30.5 µm
w_{total}	Total width of structure	530 µm
gap	Width of CPWG gap	4.8 µm
w1	Width of CPWG conductor	32 µm
$h_{Win,top}$	Height of top metal layer window	190 µm
h_{total}	Total height of structure	650 µm
$w_{Win,top}$	Width of top metal layer window	171 µm
d_{Via1}	Distance to via ring	93.5 µm
d_{Via2}	Distance to via ring	95 µm
d_{Via3}	Distance to via ring	113.5 µm

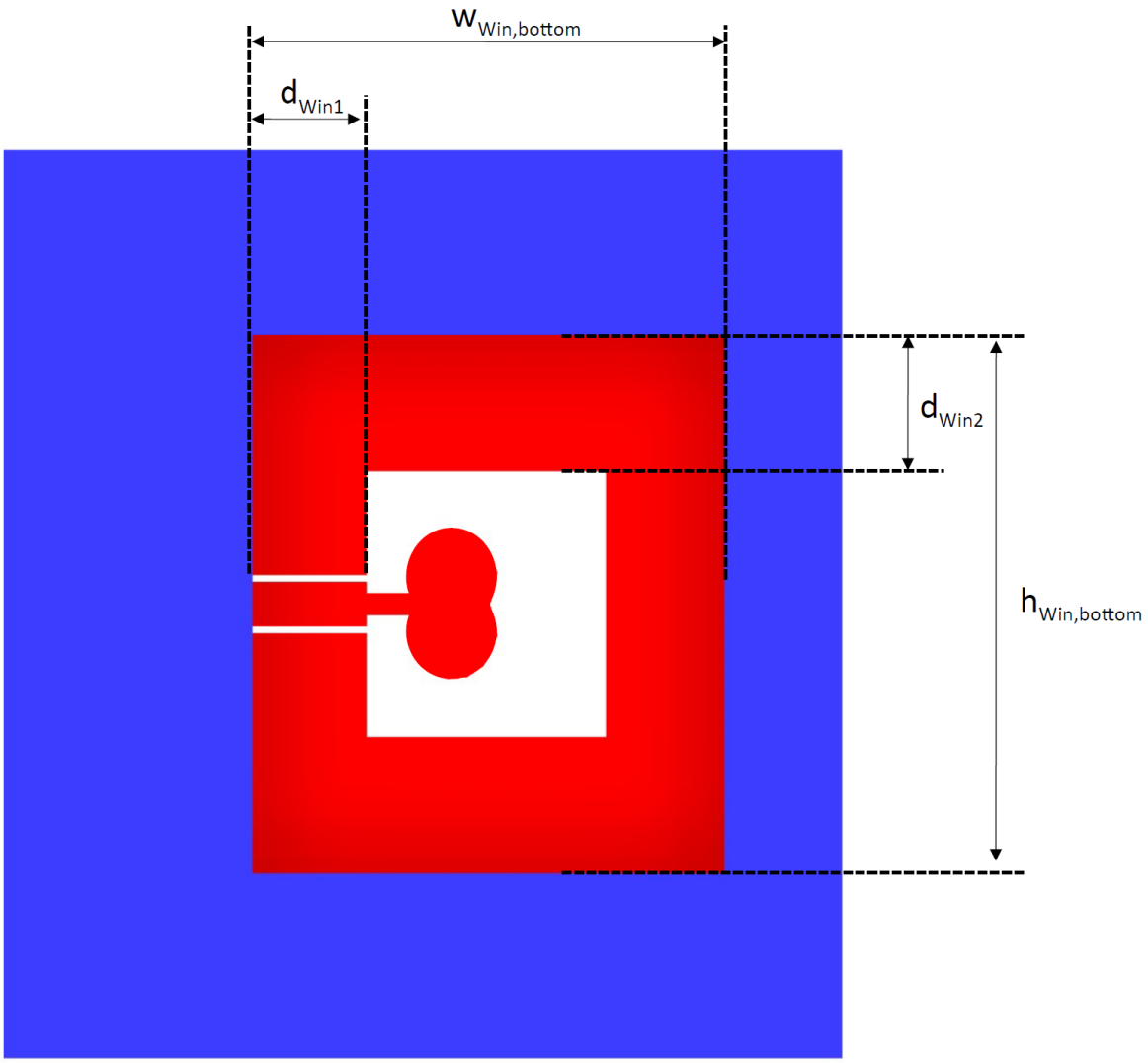

Figure C.3.: Bottom view of the antenna presented in chapter 6.3 with labels.

Table C.3.: Description and values of the parameters shown in Fig. C.3.

$h_{Win,bottom}$	Height of bottom metal layer window	385 µm
$w_{Win,bottom}$	Width of bottom metal layer window	338 µm
d_{Win1}	Distance from edge of top window to edge of bottom window	82 µm
d_{Win2}	Distance from edge of top window to edge of bottom window	97.5 µm

D. Antenna Radiation Patterns from 270 to 330 GHz

In the following the additional radiation patterns for the antenna presented in chapter 6.3 from 270 to 330 GHz in 10 GHz steps are depicted.

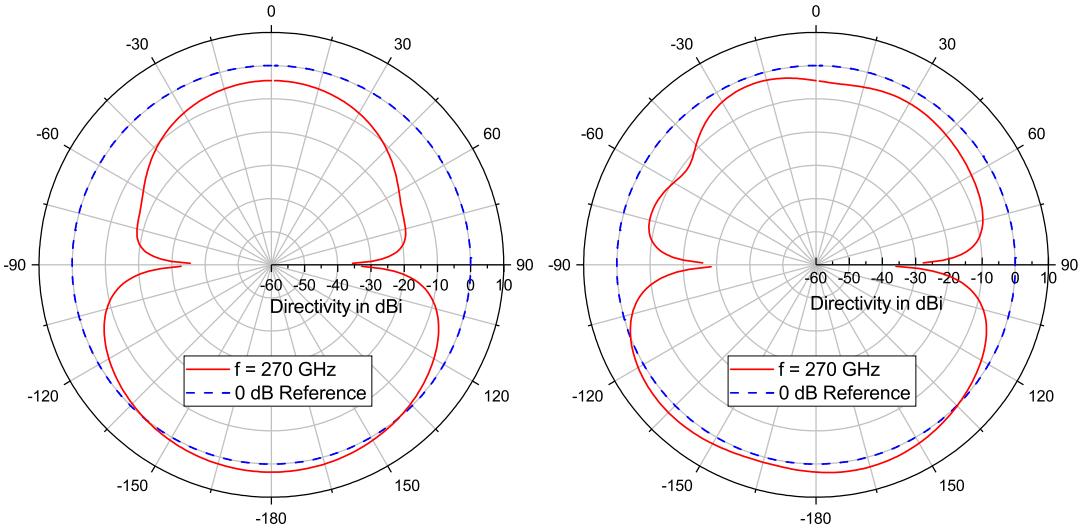

Figure D.1.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 270 GHz.

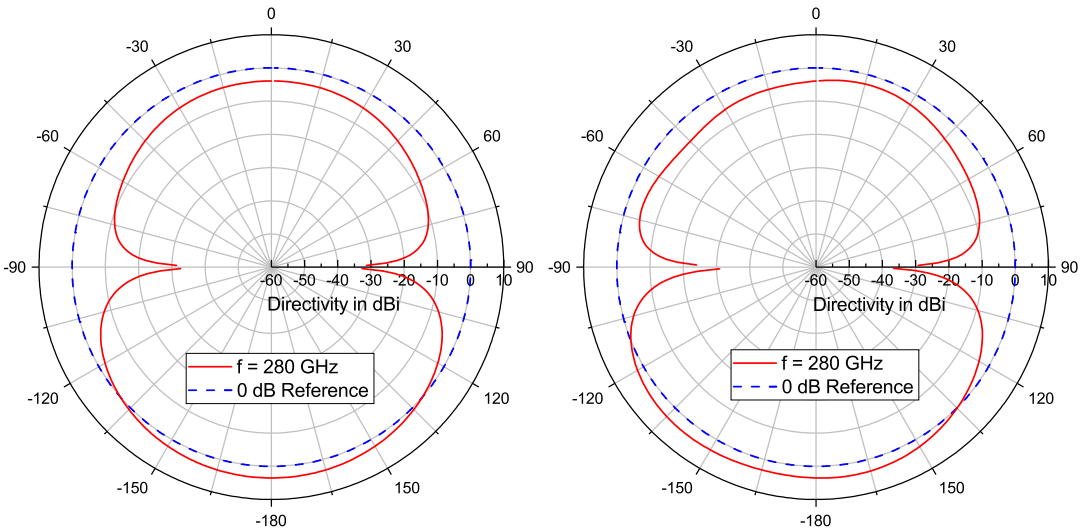

Figure D.2.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 280 GHz.

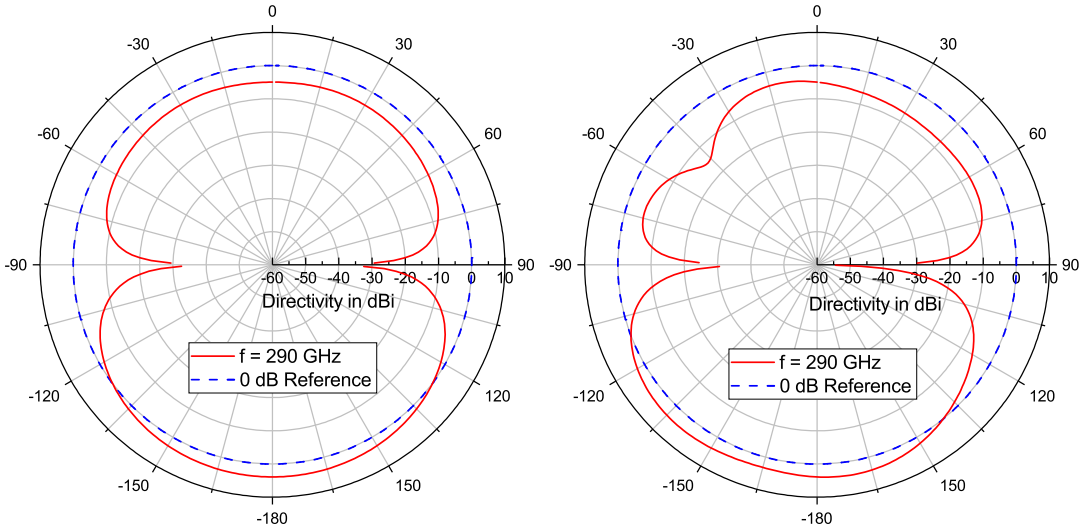

Figure D.3.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 290 GHz.

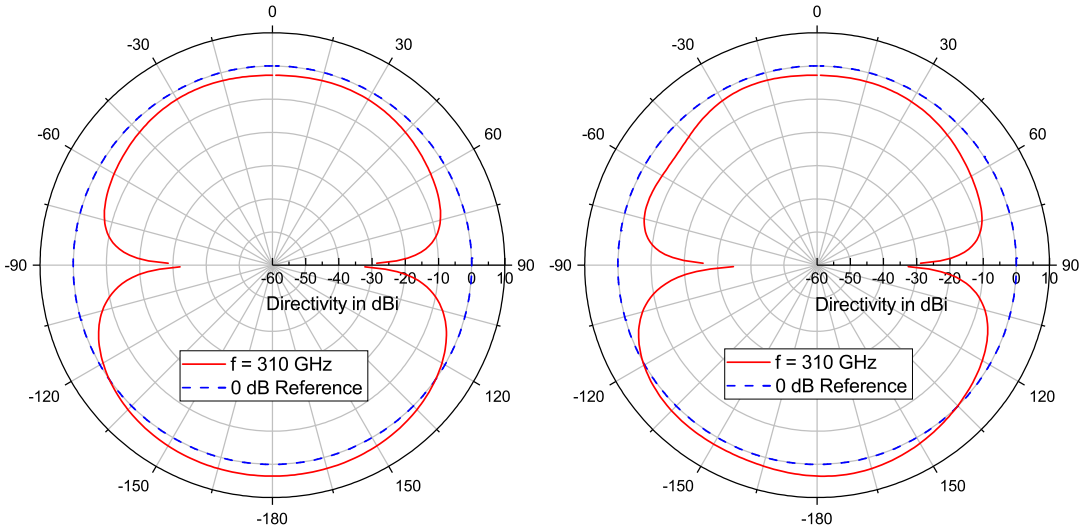

Figure D.4.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 3100 GHz.

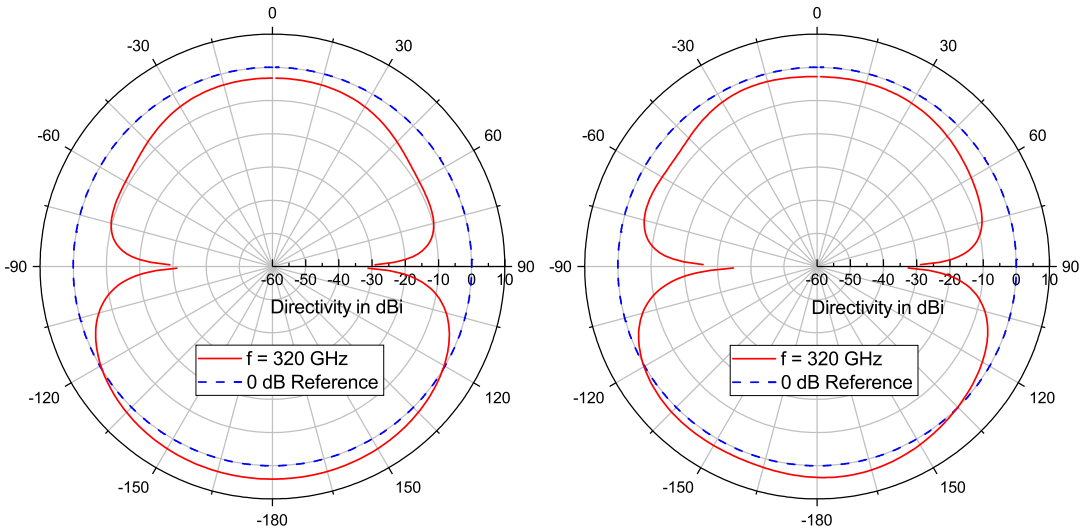

Figure D.5.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 320 GHz.

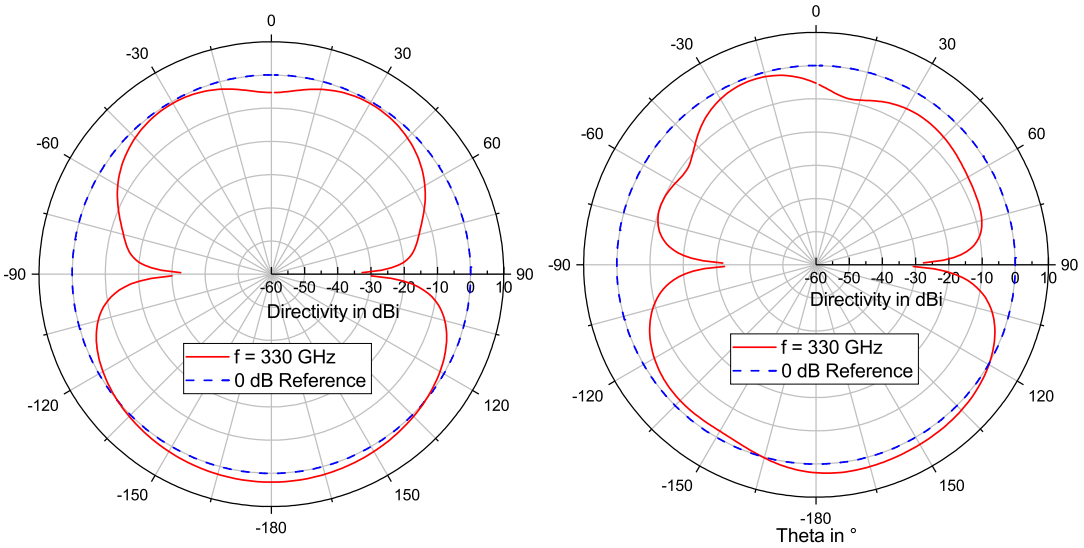

Figure D.6.: The simulated radiation pattern for $\phi = 90°$ (left) and $\phi = 180°$ (right) at 330 GHz.

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