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High-performance MEMS shutter display with metal-oxide thin-film transistors and optimized MEMS element

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Abstract
Active matrix prestressed microelectromechanical shutter displays enable outstanding optical properties as well as robust operating performance. The microelectromechanical systems (MEMS) shutter elements have been optimized for higher light outcoupling efficiency with lower operation voltage and higher pixel density. The MEMS elements have been co-fabricated with self-aligned metal-oxide thin-film transistors (TFTs). Several optimizations were required to integrate MEMS process without hampering the performance of both elements. The optimized display process requires only seven photolithographic masks with ensuring proper compatibility between MEMS shutter and metal-oxide TFT process.

KEYWORDS
MEMS shutter, metal-oxide TFT, transmissive shutter display

1 | INTRODUCTION

Microelectromechanical systems (MEMS) have advantages like reliability, fast response time, robustness, and will open doors to many applications if can be utilized in large area manufacturing processes. Among the existing display technologies, liquid crystal displays (LCDs) have become the backbone of the display industry with its maturity, but its inherent characteristics such as efficiency, contrast ratio, response time, viewing angle, and so forth made researchers to search for better technologies. Organic light-emitting diode (OLED) displays solve some of the problems of LCDs, but newer problems like lifetime and robustness against harsher environment added its attribute. MicroLEDs are superior to any other of their competitor in terms to quality, but the technology needs to be mature enough to compete with its predecessors. Several problems like mass transfer issues, suitable backplane, and manufacturing cost remain as a challenge for microLED displays.[1]

Display technology is one of the main applications of large area electronics and MEMS technology has the promise to enable efficient, responsive, and vibrant image reproduction while reducing power consumption by eliminating lossy elements and increasing robustness. Though several attempts at commercialization had failed before,[2–4] our group has successfully demonstrated highly efficient and robust vertically translating MEMS shutter display for transmissive display application.[5–7] The vertically translated MEMS shutter display technology has been further improved by integrating metal-oxide thin-film transistors (TFTs) and optimizing the structure for a high-resolution and highly efficient display.

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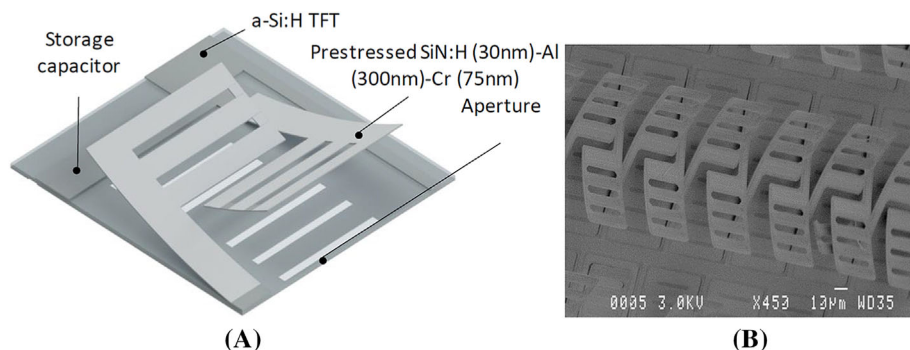

FIGURE 1 (A) Concept of prestressed microelectromechanical systems (MEMS) shutter; (B) scanning electron microscopy micrograph of prestressed MEMS Shutter. TFT, thin-film transistor.

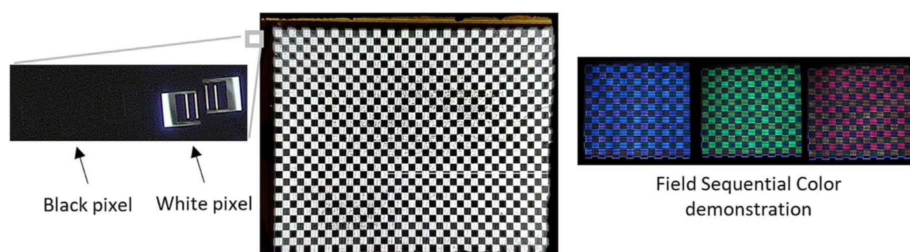

FIGURE 2 Microelectromechanical systems shutter display.

2 | PRESTRESSED MEMS SHUTTER WITH A-SI:H TFTS

2.1 | Prestressed MEMS shutter

Typical surface micromachined MEMS structures are fabricated by depositing structural layer over a sacrificial layer and the structural layer is freed by removing the sacrificial layer. For sufficient actuation range, the sacrificial layer thickness must be thick (for surface, micromachining) or the substrate must be etched (bulk micromachining). To make the MEMS process compatible with display fabrication process, the vertically translating MEMS shutter uses prestressed layer to achieve sufficient actuation range. Due to the prestress in the layer, the structures curled up into the relaxed state once the sacrificial layer is etched.

Figure 1A shows the device structure of the prestressed MEMS shutter display. In the relaxed state, the "P"-shaped structures open the patterned aperture in the bottom electrode and allow the light from the backlight pass through both direct transmission and recycled light transmission. The electrostatic MEMS shutter can be addressed with the driving voltage and can be forced to collapse over the open apertures, thus completely blocking the light from the backlight. Due to the inherent nature of electrostatic actuation, the MEMS shutters can be actuated only in collapsed and in free position and thus completely bright and completely dark state can be achieved by addressing (Figure 2). Grayscale as well as color image reproduction can be achieved by field sequential color scheme due to the fast response characteristics (around 400 μs, overdriving as well as vacuum packaging can reduce the figure) of the MEMS elements. Figure 2 also shows the demonstration of different colors with an RGB backlight through a field sequential color scheme.

2.2 | Co-fabrication with a-Si:H TFTs

The technology has advantages over previously demonstrated large area MEMS technologies as it utilizes the existing TFT layers with minimum additional layer (only sacrificial layer is added in addition[6]). The approach not only reduces the manufacturing complexity and cost but also increases manufacturing yield. The prestressed MEMS shutters operate and are modulated by their out-of-plane actuation, and the backlight must be placed on top of the substrate (Figure 1). So unlike active matrix liquid crystal displays where the bottom gate is used to protect the channel from the backlight, the MEMS shutter display requires top gate structures. Co-fabrication of prestressed MEMS elements with top gate a-Si:H TFTs had been presented before[5–7] by our group.

The top gate a-Si:H TFT process (originally proposed by Persons et al.[8]) uses selective deposition of a phosphorous doped a-Si:H layer over the molybdenum (Mo) drain/source (D/S) layer to reduce the mask count. Figure 3A shows the cross section of a co-fabricated MEMS shutter display. The D/S layer of the TFTs is shared by the MEMS elements as the bottom electrode and the top gate metal layer is shared as the structural layer. Though the process ensures lower mask count, it is susceptible to process conditions as well as the D/S metal layout variation and leads to unwanted TFT characteristics. Figure 4A shows the characteristics of top gate a-Si:H TFTs co-fabricated with MEMS shutter. Though both are deposited using same process condition, the TFT 1 has higher D/S doping than

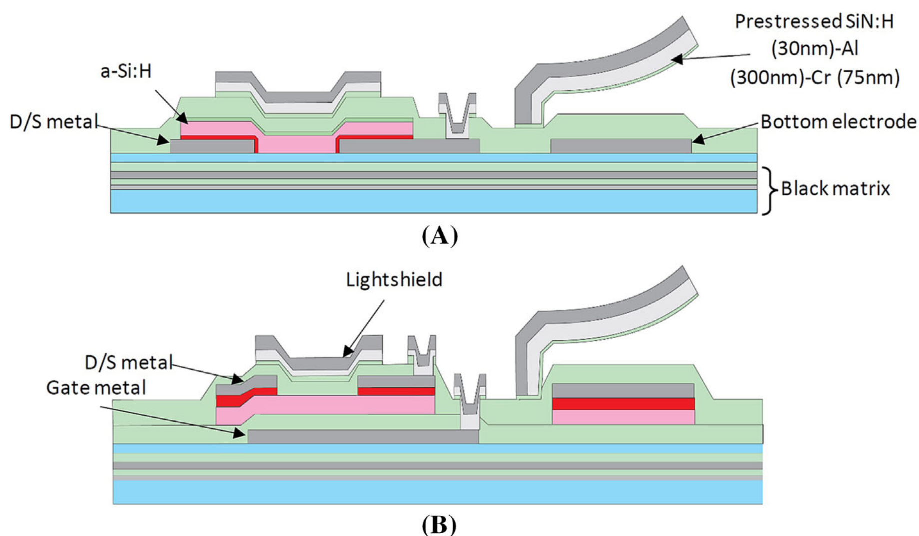

FIGURE 3 (A) Co-fabrication of microelectromechanical systems (MEMS) elements with top gate a-Si:H TFT; (B) co-fabrication of MEMS elements with bottom gate a-Si:H thin-film transistor. D/S, drain/source.

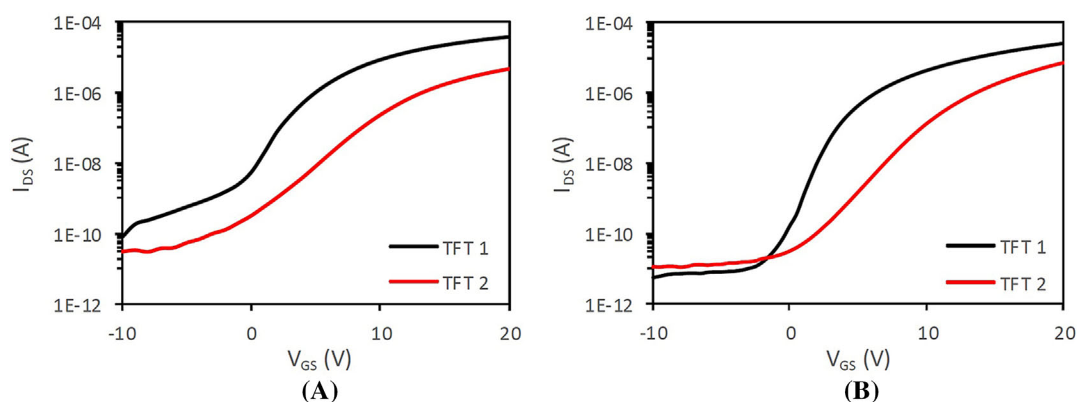

FIGURE 4 (A) Input characteristics curve of top gate a-Si:H thin-film transistors (TFTs) with different drain/source (D/S) metal content in the active matrix (W/L = 150 μm/5 μm); (B) input characteristics curve of bottom gate a-Si:H TFT with different backchannel etch conditions (W/L = 150 μm/5 μm).

TFT 2 due to the different D/S layout. The process requires thorough optimization of the a-Si:H layer deposition whenever the D/S layout is changed.

To combat these issues, co-fabrication of MEMS elements with conventional bottom gate backchannel etched a-Si:H TFTs is proposed. Our group had previously demonstrated lightshield protected bottom gate a-Si:H TFTs for high performance adaptive headlight applications.[9] A similar approach has been followed to co-fabricate MEMS elements with a-Si:H TFTs and the D/S layer has been used as the bottom electrode and the lightshield layer has been used as the structural layer of the MEMS elements (Figure 3B). Figure 4B shows the input characteristic curves of different TFTs co-fabricated with MEMS elements. Though this process requires an additional photolithographic mask (seven photolithographic masks compare to six of the top gate process) as well as additional steps like backchannel etching of the TFTs, the process is more tolerant to process condition variation. The threshold voltages as well as the field effect mobility of the TFTs can be controlled by the deposition conditions and backchannel etching time (Figure 4B) and does not depend on the display layout.

The MEMS shutter display with a-Si:H TFTs was developed as a technology demonstrator and further optimizations (e.g., faster backplanes and lower operating voltage) were needed to compete with the mainstream display technologies.

3 | OPTIMIZATION OF MEMS SHUTTER

As discussed in Al Nusayer et al.,[5] the basic principle of operation of the MEMS shutter display is the modulation of light by actuating MEMS elements in open and closed state over some apertures. Figure 5 shows the graphical representation of the principle. The prestressed shutter elements curled up in open state, and tip-displacement lets the light pass through the structured metal apertures.

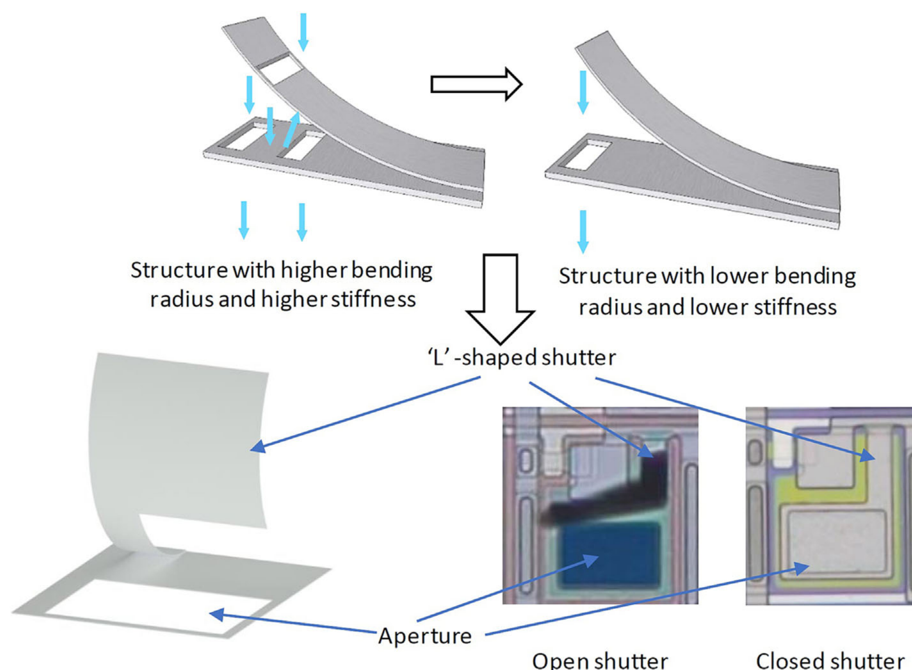

FIGURE 5 Optimization of shutter geometry for higher light outcoupling.

Multiple apertures below the curled-up element allow direct light transmission as well as recycle the reflected light to achieve much higher light outcoupling than the aperture size. One of the main features of the prestressed MEMS elements is the dependence of the actuation voltage on the bending radius of the curled-up structure. The actuation voltage also depends on the thickness of the structural layer, the stiffness of the structural layer, the overlap of the bottom electrode, and so forth, but the effect of the bending radius is more pronounced. A smaller bending radius allows higher direct transmission but requires higher voltage to actuate. Several optimizations had been performed before and the "P" structure had been proposed where the bending radius around 150 μm with actuation voltage around 35 V had been achieved.[6]

Decreasing the bending radius without increasing the actuation voltage will not only increase the light-outcoupling but also open the possibility to implement higher resolution (>250 ppi). For structures with lower bending radius (∼60–70 μm), an "L"-shaped structure (Figure 5) is more advantageous because much light can be outcoupled through direct transmission. As discussed in Al Nusayer et al.,[5,6] reduction of bending radius leads to much higher actuation voltage. The initially demonstrated MEMS technology[5] by our group had plasma-enhanced chemical vapor deposition (PECVD) deposited silicon nitride (SiN:H) bilayer (450-nm thick compressive and tensile combination) and molybdenum tantalum (MoTa) as the structural layer, which offered sufficient stiffness to prevent stiction during release at the expense of higher operating voltage (around 45 V for 200-μm bending radius). The process was optimized by reducing the stiffness of the structure by replacing the stiff SiN:H with aluminum (300 nm) and chromium (75 nm), and up to 35-V actuation could be achieved with 150-μm bending radius. The actuation voltage reached up to 60 V when the bending radius decreased to <120 μm. So to achieve structures with bending radius approximately 60 μm, optimization of the structural stiffness is necessary.

Another challenge towards achieving MEMS elements with lower actuation voltage is the release etching of the MEMS structure. The selection of the proper sacrificial layer in the MEMS elements is very important as it not only defines the MEMS structure but also the process yield is strongly dependent on the successful etching of the layer. The simplest sacrificial layer etching technique is to etch the layer with a wet etching that does not affect the surrounding layer while etching the sacrificial layer at substantially fast speed. Later, the etchant solution is rinsed and dried to release the MEMS structures for operation. Though the wet chemical etching possesses the simplicity, it also introduces yield loss due to breakage of fragile structures and surface tension-induced stiction of the MEMS structures.[10] Several techniques such as critical point drying and freeze-sublimation drying have been used to dry the release structures.[11] Dry vapor etching techniques like vapor hydrofluoric acid (HF) for silicon oxide (SiO) layer, xenon fluoride (XeF_2) for Si and Mo layer, sulfur hexa-fluoride (SF_6) plasma for Si layer, and O_2 plasma for organic layer[11] had been proposed and used in MEMS fabrication process. All these processes increase the process complexity and incompatibility with the large area microelectronic fabrication process.

Figure 6 shows the release etching procedure of the prestressed MEMS elements. To keep the process as

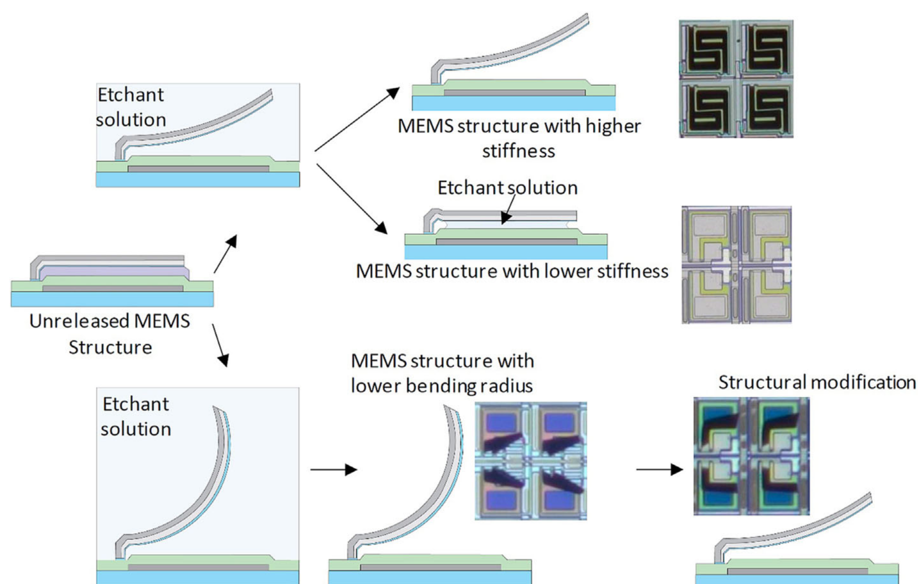

FIGURE 6 Wet-release etching of prestressed microelectromechanical systems (MEMS) structure.

simple as possible, aluminum-doped zinc oxide (AZO) was chosen as the sacrificial layer (covered with 30-nm thin SiN:H as the etch stopper layer) and etched with 1% sulfuric acid (H_2SO_4) solution upon plasma removal of the SiN:H.[6] The surface tension-induced stiction can be avoided by increasing the structural stiffness of the material, but eventually higher stiffness leads to higher voltage requirement. Experiments indicate that replacing the SiN:H with PECVD SiO and using thinner structural metal (Al–Cr or Al–MoTa) dramatically reduce the operating voltage by reducing the structural stiffness, but the structures become susceptible to stiction during release. Stiction during release can be avoided for highly bent structures (20–30 μm bending radius), but actuation voltage remains high (25–40 V) for these structures. One feasible solution to this problem could be a viable post-release structural modification to increase the bending radius and reduce the operating voltage.

As discussed before, a highly tensile stressed layer with high Young's modulus layer like Cr or MoTa is used to achieve the required prestress in the structural layer as well as bending.[5,6] The induced prestress must be homogeneous in all directions to allow the MEMS structure to bend homogeneously. Figure 7 shows the characteristics of a pass-by sputtering system where the substrate is moved in front of the target during the layer deposition, and it leads to stress inhomogeneity in different direction of the substrate. Sputter-deposited Cr layer has a high tensile stress, and by optimizing the deposition conditions, it is possible to reduce the directional stress gradient (the cantilevers in Figure 7B have different bending radii due to slightly different directional tensile stressed Cr, and Figure 7C shows shutters with homogeneous stress). The directional stress in MoTa can be tailored from highly compressive to highly tensile depending on the deposition conditions, and the directional stress gradient can lead to direction dependent bending characteristics (Figure 7D).

Aluminum is well known for its stress-relieving characteristics at elevated temperature (from 230°C) and capping layer with high Young's modulus material as well as temperature-resistant alloys had been introduced before for flat panel display manufacturing.[12] The MEMS structures with Al and homogeneously stressed Cr shows lower bending radius upon annealing over 230°C. The effect can be described by the increase of compressive stress in Al upon annealing,[12] which should increase the stress gradient inside the structure (Figure 8A). Unlike the Al–Cr structures, Al–MoTa structures with directional stress gradient shows to bend towards the opposite direction by increasing the bending radius with time (Figure 8B). The inhomogeneous stress distribution in MoTa could be responsible and prevents the Al layer to homogeneously expand (increase of compressive stress) during temperature treatment. The demonstrated MEMS structures in Figure 8B changed the bending radius from 30 to 60 μm upon 250°C temperature treatment for 15 min and the actuation voltage reduced to 15 V from 40 V. The bending radius increases more (>100 μm) upon longer annealing, and actuation voltage as low as 7 V could be achieved. For display application, a bending radius of 60 μm at 15-V actuation voltage is more practical. Though further investigations for long-term in-use case are required, the structural change with temperature has been found to be stable.

4 | INTEGRATION WITH SELF-ALIGNED INDIUM–GALIUM–ZINC–OXIDE TFTS

MEMS shutters have inherent high-speed operation capability, but the operation is limited between open and

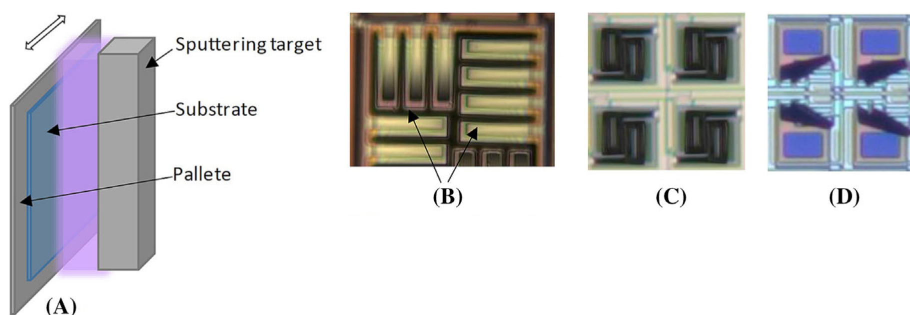

FIGURE 7 Inhomogeneous stress distribution in sputtered layer. (A) Pass-by substrate sputering system; (B) different bending radii due to inhomogeneous stress; (C) homogeneous stress distribution (Al–Cr); (D) homogeneous stress distribution (Al–MoTa).

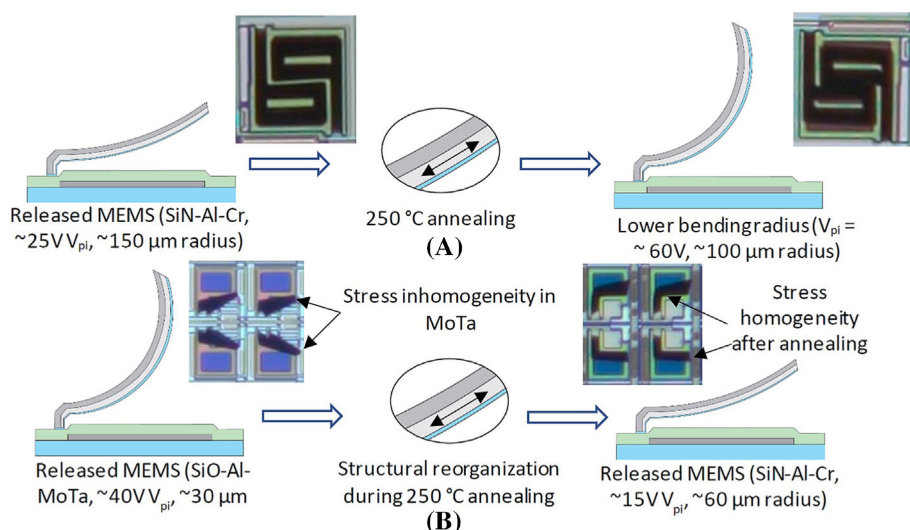

FIGURE 8 Effect of annealing on different microelectromechanical systems (MEMS) structures.

closed state. So grayscale generation during display operation can be achieved using digital field sequential driving,[13] which necessitates higher mobility TFTs such as low-temperature polycrystalline oxide (LTPS) or metal-oxide TFTs. Our group had reported the integration of large area MEMS technology with a-Si:H TFTs[5–7] as well as LTPS TFTs[14] before, and metal-oxide TFT integration has been investigated in this work.

Amorphous oxide semiconductor TFTs, especially Indium–Galium–Zinc–Oxide (IGZO) are gaining popularity due to their superior attributes like lower production cost than LTPS, higher mobility (~10 cm^2/Vs), and lower off-current than a-Si:H as well as better device uniformity. As discussed before, a top-gate (TG) variant is necessary to protect the channel from backlight during operation and a self-aligned (SA) TG variant has the benefit of smaller device footprint as well as lower parasitic capacitance. In a typical SA-TG TFT process, the semiconductor is deposited and structured first. The gate dielectric, as well as gate layer, is deposited and structured, and the structured gate/gate dielectric stack is used to define the doped and pristine semiconductor region (Figure 9). The TFT stack is then passivated, and vias are formed for metallization of D/S region.

The formation of low-resistance D/S contact with IGZO semiconductor is a major challenge towards highly uniform, reliable, and low-cost IGZO TFT production. Several methods like argon (Ar) and hydrogen (H_2) plasma treatment,[15] fluorine (F) plasma treatment,[16] and Al doping[17] have been used to achieve low D/S resistance and good device reliability. Plasma treatment with heavier Ar atoms create oxygen vacancies (V_o) in IGZO, which acts as a dopant by increasing the conductivity. Unfortunately, the generated V_o are not temperature stable, and the contact resistance degrades significantly during final annealing (250°C) of the TFTs. The H_2 plasma treatment hydrogenates the D/S region and increases the conductivity by passivating the defects with H radicals that acts as a shallow donor. Hydrogenated contacts also suffer from temperature instability, and lateral diffusion further degrades the device homogeneity. Fluorine also acts as shallow donor for IGZO, and due its similar atomic radius as oxygen, F radicals can passivate the V_o rather successfully. Moreover, fluorination using F-plasma offers better temperature stability as the metal (In, Ga, and Zn)–fluorine bonds are more stable than metal–oxygen bonds.[16] Al doping technique does not replace any atoms; rather, it acts through chemical oxidation–reduction process and generates oxygen vacancies as well as metal interstitials.[17]

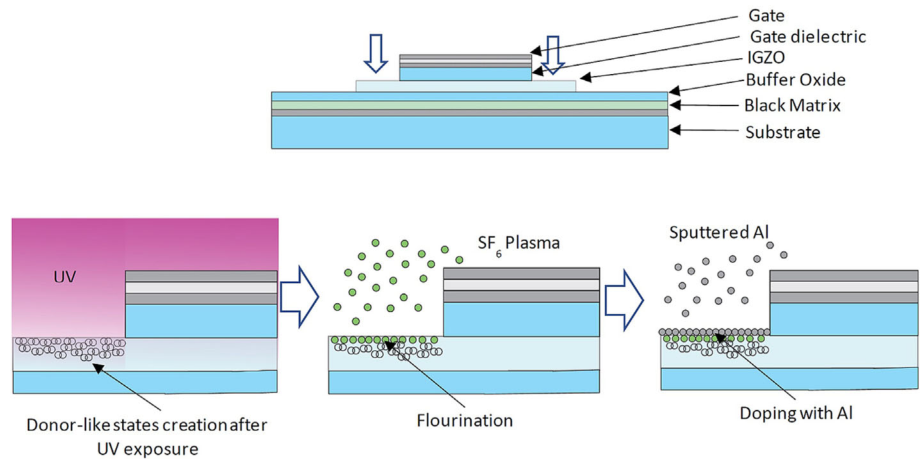

FIGURE 9 Doping of drain/source region.

4.1 | Optimization of drain-source doping

Though F-doping is reported as a stable method to dope IGZO D/S region, a proper F-doping requires relative high-quality plasma source (e.g., ICP plasma source).[16] Due to the limit of the equipment, a proper fluorination could not be achieved for this work by direct F-plasma treatment (SF_6 plasma was used) on temperature-treated (300°C) activated IGZO layer. A fresh deposited IGZO layer can be successfully doped with F-plasma treatment, but the sheet resistance remains quite high (~100 kΩ/□) to be used as the D/S contact. Since the defect density and oxygen vacancies are high in a fresh deposited sputtered IGZO layer, fluorine radicals can passivate some defects as well as act as a shallow donor to increase the conductivity.

A very thin sputtered Al layer (1–2 nm) can be deposited and activated at 250°C to successfully reduce the sheet resistance of IGZO up to 600 Ω/□. Though the method produces very good quality IGZO TFTs (μ_{FE} up to 12 cm^2/Vs, subthreshold slope as low as 250 mV/dec), the device uniformity suffers significantly. Figure 10A shows the input characteristics curves of fabricated IGZO TFTs with Al-doped D/S. As the Al doping generates oxygen vacancies and activation annealing helps the oxygen vacancies to be distributed throughout the bulk,[17] the variation of V_{th} could be an effect of the non-uniform lateral carrier diffusion and subsequent channel shortening. To mitigate the non-uniformity, a hybrid approach of Al–F co-doping is proposed. As discussed before, doping F radicals with the available equipment for this work in pristine IGZO layer requires high defect density and oxygen vacancies. UV light with sufficient energy leads to the generation of oxygen vacancy states[18] confined in the top surface of the IGZO layer, and they can be passivated with F-plasma treatment.

Figure 9 shows the doping procedure for the D/S region with Al–F doping. Several UV sources (ranging from 250 to 380 nm) have been illuminated over the D/S region for around 15 min. The generated defects and oxygen vacancies are passivated using a SF_6 plasma (40 mTorr, 750 W, capacitive coupled reactive-ion etching [RIE] plasma source) for 60 s, and the samples are annealed at 250°C for 1 h to activate the F-doping. A thin layer (1–2 nm) of Al is sputtered over the D/S region and activated at 250°C for 1 h. Figure 10B shows the input characteristic curves of produced TFTs with Al–F doping, and they show uniform behavior over a relatively large area (5 × 5 cm substrate for experimental purpose).

As discussed before, Al doping generates oxygen vacancies and indium (In) interstitials through chemical oxidation–reduction[17] to increase the conductivity of IGZO layer. The contribution of top surface fluorination before Al doping is very negligible, and the strong metal–fluorine bonds should restrict the diffusion of oxygen vacancies and prevent subsequent channel shortening. The doping effect is found to be long term as well as high-temperature stable (up to 300°C have been tested).

4.2 | Characterization of self-aligned IGZO TFTs

As discussed in the previous sections, electrostatic MEMS elements operate in a quite high-voltage regime, and the MEMS shutter presented by our group required around 35 V before the optimizations. A single pixel in the MEMS shutter display contains a single switching TFT with the source connected to the MEMS shutter element. The capacitive MEMS element needs to be charged up to its actuation voltage during addressing, where V_{DS} needs to be similar to actuation voltage and V_{GS} should be slightly higher (ideally $V_{DS} + V_{TH}$) to successfully charge the pixel.

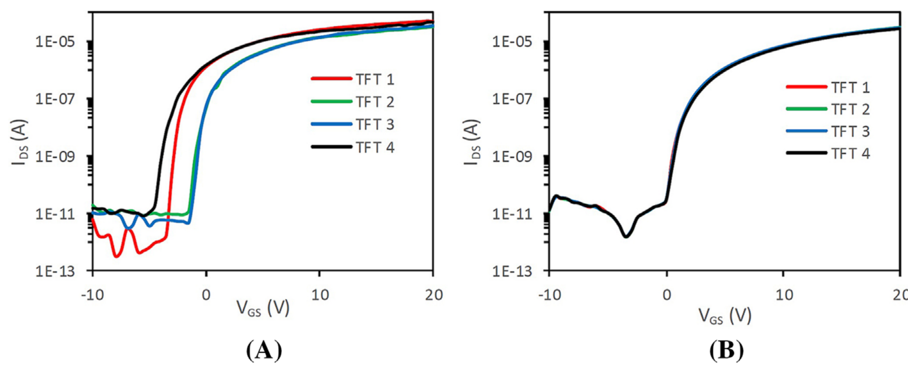

FIGURE 10 (A) Input characteristics curves of multiple Al-doped Indium–Galium–Zinc–Oxide (IGZO) thin-film transistors (TFTs) ($W/L = 20\ \mu m/10\ \mu m$, $V_{DS} = 10$ V); (B) input characteristics curves of multiple Al–F doped IGZO TFTs ($W/L = 10\ \mu m/10\ \mu m$, $V_{DS} = 10$ V).

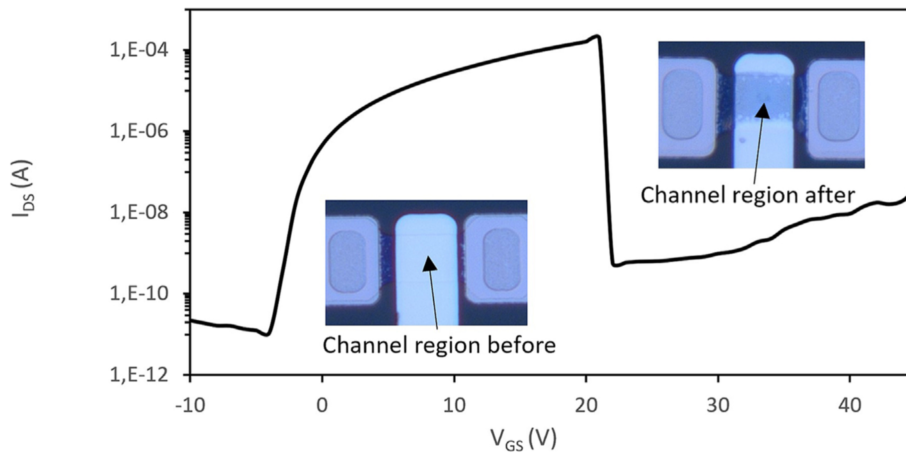

FIGURE 11 Effect of high voltage and current in Indium–Galium–Zinc–Oxide (IGZO) thin-film transistor (TFT). The micrographs show the difference between pristine IGZO TFT and the physical change afterwards.

The initial requirement for the use of IGZO TFTs along with MEMS elements was its capability to be used at least 35 V V_{DS} and V_{GS} (as the display in Figure 2 had been driven with such voltages). Figure 11 shows the input characteristics curve of IGZO TFT at 35-V V_{DS}. The TFT not only undergoes a physical change around 22 V V_{GS} but also the on current (I_{on}) reduces significantly afterwards. Initially, it was thought that the high drain voltage generates hot carriers that rupture the weak oxygen bonds and create acceptor like tail states[19] that limits the I_{on}. Later, thorough investigations confirm that the fabricated IGZO TFTs are stable and operational at high voltage (Figure 12). Figure 12A shows the standard positive bias stress curves at 10-V V_{DS} and 20-V V_{GS} of a TFT for 2700 s. The TFTs show quite stable performance and very negligible V_{th} shift even after this long stress period. Similar performance can be attained when the TFTs are stressed at 35 V V_{GS}, but limiting the V_{DS} to 0 V (and vice versa). Unfortunately, the TFTs show slight shift over time when they are stressed at 15-V V_{DS} and 20-V V_{GS} for 2700 s, and the V_{th} shifts from 1.01 to 0.03 V over this time period. This shift becomes worse when they are stressed at 20-V V_{DS} and 25-V V_{GS}, and several volts threshold shift already occurs within 90 s.

The positive bias test analysis points that Joule heating in the channel can be responsible for the behavior of the IGZO TFTs. It is evident that the V_{th} shift becomes worse with increasing power density in the 100 μm^2 ($W/L = 10\ \mu m/10\ \mu m$) IGZO channel. The threshold shift mechanism can be explained by the generation of defects and oxygen vacancies in the channel area at these quite high-power density. The channel temperature can rise more than 300°C during the on state (similar self-heating effect is discussed for LTPS TFTs in Inoue et al.[20]) which is high enough to break metal–oxygen bonds and thus generate negative V_{th} shift due to excessive amount of V_o (recoverable after 250°C annealing for 30 min). If the channel temperature rises to a certain value, that may lead to a permanent change in the channel region like depicted in Figure 11 and limit the on-state behavior of the TFTs (irrecoverable damage).

As discussed in the previous section, electrostatic MEMS shutters act as a variable capacitor in the display and require a negligible amount of current for a short amount time during operation. To simulate the compatibility with MEMS devices, the TFTs were stressed at $V_{GS} = 35$ V and $V_{DS} = 35$ V with a series capacitor (100 pF, connection similar to the MEMS pixel circuit depicted in Figure 14) where they show similar stable behavior like Figure 12A with negligible V_{th} shift. Though Joule heating can have serious impacts on IGZO TFTs depending on the applications, MEMS displays will not suffer from this problem.

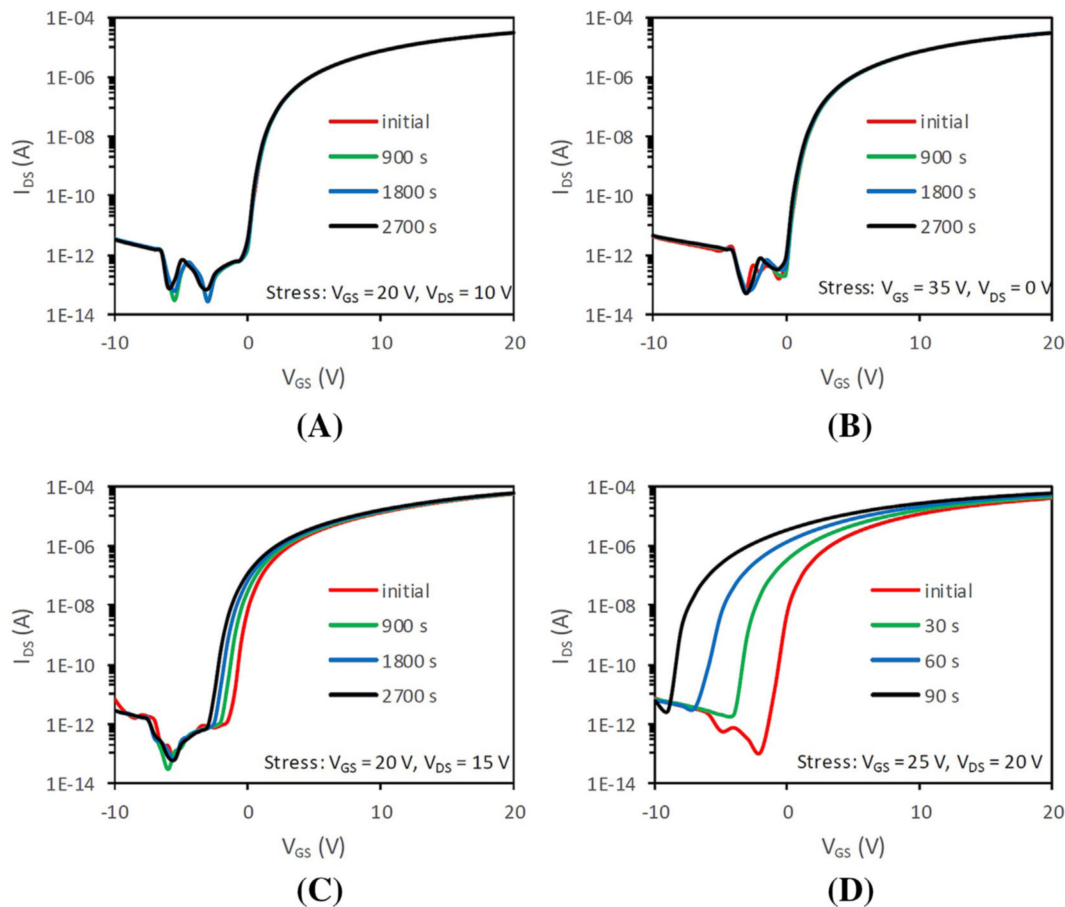

FIGURE 12 (A–D) Input characteristics curves of multiple Al–F doped Indium–Galium–Zinc–Oxide (IGZO) thin-film transistors (TFTs) (W/L = 10 μm/10 μm, V_{DS} = 10 V) after positive bias stress test.

5 | CO-FABRICATION OF MEMS SHUTTER AND SELF-ALIGNED IGZO TFTS

Unlike a-Si:H TFTs, IGZO TFTs require a final high temperature annealing step (>250°C) once the fabrication procedure is completed to ensure stability and uniformity of the TFTs. As discussed in the previous section, high temperature annealing can have adverse effects on Al-based structural layer of the MEMS elements. To manufacture the IGZO TFT-based MEMS shutter display with a minimum number of photolithographic masks as possible, a co-fabrication procedure is proposed.

The process starts with the deposition and structuring of an inorganic light-blocking layer (100-nm MoTa for experimental purpose) on the Corning XG glass substrate. The metallic light-blocking layer is then passivated by a PECVD SiN:H (150 nm)–SiO (75 nm) layer. A thin layer of aluminum oxide layer is sputtered to protect the passivation layer from subsequent F-plasma damage during the D/S doping and then covered by 50-nm PECVD deposited SiO to act as a buffer layer for IGZO. The semiconductor layer (IGZO, 1:1:1) is then deposited and structured using wet chemical etching and annealed at 300°C for 2 h. A 150-nm PECVD SiO is deposited as the gate dielectric, and a MoTa-AlNd layer is sputtered as the gate metal. The multilayer metal should offer better gas impermeability, and the top AlNd layer protects the MoTa layer from F-plasma damage during doping. The layer is then patterned to form the gate layer of the TFTs, and the dielectric below is etched with SF_6 RIE. The exposed IGZO layer in the D/S region as well as in the MEMS bottom electrode area is then doped with Al–F hybrid doping and activated (Figure 13A). The doped IGZO serves as the bottom electrode for the MEMS without the need of an additional photolithographic mask (ITO is also compatible but requires an additional mask) and offers sufficient conductivity. The stack is then passivated with an interlayer dielectric (150-nm PECVD SiO) and the sacrificial layer (80-nm aluminum-doped zinc oxide [AZO]) is deposited and structured in the MEMS area of the pixel. Since the sacrificial layer must remain intact until the end of the

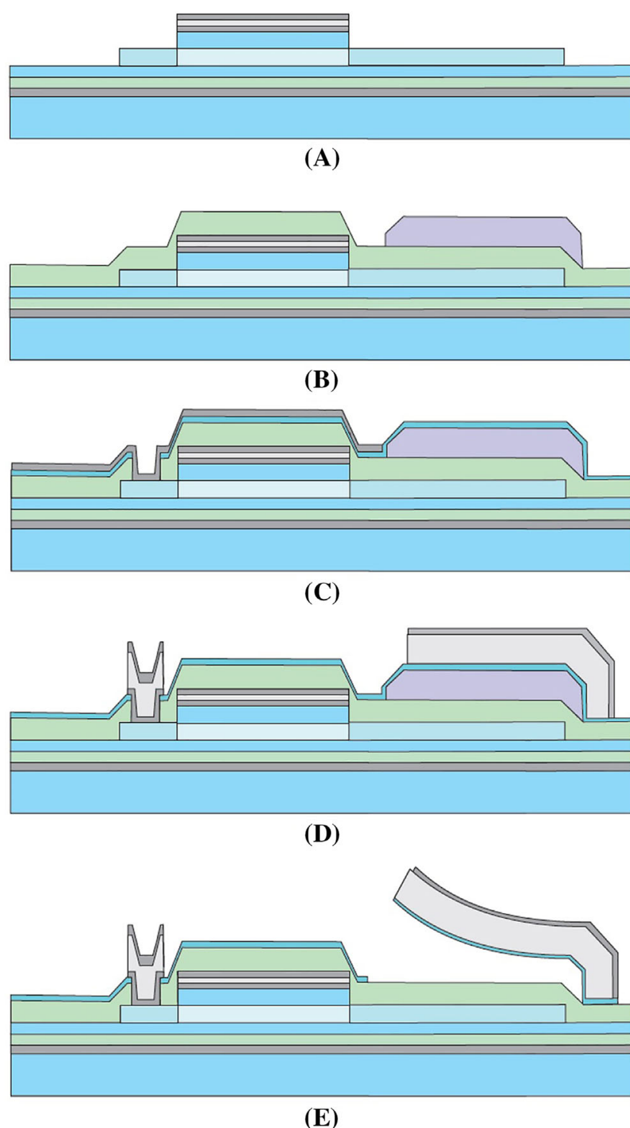

FIGURE 13 (A–E) Process flow for co-fabrication of microelectromechanical systems and Indium–Galium–Zinc–Oxide (IGZO) thin-film transistors (TFTs).

processing steps and AZO is known for its reactivity to most of the acids and bases, the whole stack is then covered with a thin layer (20 nm) of PECVD SiO. The dielectric stack is then etched to create via connections with drain and source of the TFTs as well as the metal connections in the display.

As discussed before, IGZO TFTs are annealed at 250°C for several hours at the end of the processing steps to ensure good performance. This long annealing has an adverse effect on aluminum-based structural layer of the MEMS elements. To ensure good TFTs as well as MEMS elements, the D/S metal is deposited in two steps, where the first step consists of deposition and structuring of a thin MoTa (50 nm)–AlNd (15 nm) layer all over the substrate except in the MEMS areas (Figure 13C) and then

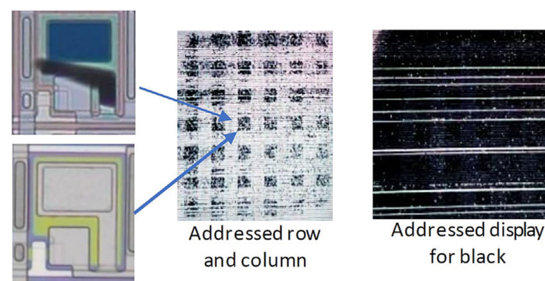

FIGURE 14 Microelectromechanical systems (MEMS) shutter display with Indium–Galium–Zinc–Oxide (IGZO) thin-film transistor (TFT).

annealed 250°C to activate the TFTs. Several annealing times from 2 to 16 h have been tested, but the difference of the TFT performance is negligible. In the second metallization step, a 70-nm Al and 60-nm MoTa is deposited and structured as the MEMS structural layer, D/S metal for the TFTs as well as the final metal connection for the display (Figure 13D). The protective SiO layer is then etched to expose the sacrificial AZO layer, which is then wet chemically etched with 1% sulfuric acid solution to release the MEMS elements. The released MEMS elements are rinsed with isopropanol solution and then dried carefully to prevent stiction and breakage. The substrates are annealed at 150°C for 1 h, which does not affect the MEMS elements. The substrates are finally annealed at 250°C for 15 min to increase the bending radius of the MEMS elements.

6 | MEMS SHUTTER DISPLAY WITH IGZO TFTS

To demonstrate the feasibility for high-performance display application, a display demonstrator has been developed. The 4-cm diagonal display consists of 320 × 320 pixels with 92 μm × 92 μm pixel size and the complete display process needs a total of seven photolithographic masks. The pixel size was limited by the technological capability during the work and can be improved to reach up to 300 ppi. Figure 14 shows the technology demonstrator as well as the micrographs of the open (bright state) and closed (dark state) pixels. The demonstrator suffered from short circuit issues due to the quality of the dielectric (both gate dielectric as well as passivation), so a fully addressable matrix was not available during the work. In addition, as full black image could not be achieved, the contrast ratio could not be measured. Further investigation is underway to improve the quality of the dielectric layer.

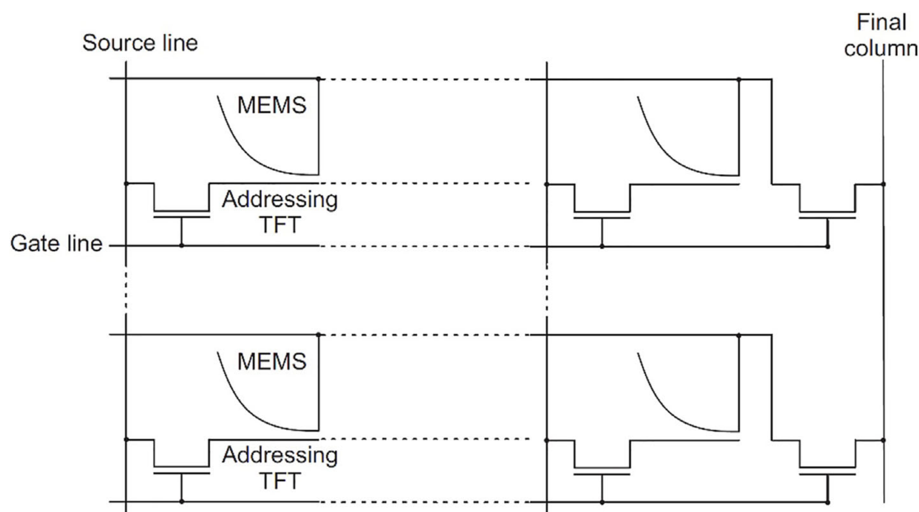

FIGURE 15 Addressing scheme for microelectromechanical systems (MEMS) shutter display. TFT, thin-film transistor.

6.1 | Addressing scheme of the MEMS shutter display

Electrostatic MEMS elements show bistable nature[2] as they can be actuated free to collapsed state for a certain voltage (known as the pull-in voltage) and another certain voltage to set them collapsed to free state (known as the hold down voltage). The hold-down voltage is slightly lower as the MEMS elements have higher capacitance in the collapsed state. Though the prestressed MEMS shutters can be actuated with a DC voltage and can have bistable nature, the effect is hard to reproduce in a large area process. Experiments suggest that the MEMS shutters return to their original state and further actuation is not possible until the actuation voltage polarity is changed. Imperfect dielectric quality can be responsible as the charged up dielectric layer can shield the electrostatic field. The limitation can be mitigated with AC voltage actuation of the MEMS elements.

Figure 15 shows the pixel circuit of the MEMS shutter display. Each pixel consists of a single TFT (W/L = 10 μm/10 μm), a capacitor and a MEMS shutter element. The final column is connected with a large TFT (W/L = 500 μm/10 μm) in each row to assist the polarity inversion during operation. In this scheme, the final column signal can be varied between actuation voltage (V_{act}) and 0 V to change the polarity of the pixel. The addressing scheme allows a two-level column driver (0 and V_{act}) as well as reduces the voltage swing of the row driver by a factor of two.

6.2 | Characteristics of the MEMS shutter display

The major improvement of the current display is the light outcoupling efficiency. Figure 16 shows the light outcoupling efficiency of the optimized display. Up to 66% light outcoupling efficiency could be achieved (with around 22% aperture ratio), where the bending radius is around 30 μm and the pull-in voltage is around 35 V. Though highly bent structures allow higher direct light transmission, the actuation voltage directly relies on the bending radius of the prestressed shutter elements. As discussed before, the bending radius can be modified with 250°C annealing and the light outcoupling efficiency reduced to around 50% when the bending radius is increased to 60 μm (actuation voltage = 15 V) as the increased bending radius hinders direct light outcoupling from the backlight.

7 | SUMMARY AND OUTLOOK

A high-performance MEMS shutter display technology has been developed that allows parallel fabrication of prestressed MEMS shutter and metal-oxide TFTs with only seven photolithographic masks. The optimized process significantly reduces the pixel size and increases light-outcoupling efficiency of the MEMS element without affecting its inherent capabilities like sub-millisecond response time, large operating temperature range (up to 140°C tested[7]).

Compared to other mainstream transmissive display technologies (e.g., the best LCD technology has less than 10% light transmittance), the MEMS shutter display offers a significant improvement in light coupling efficiency, reaching up to 66% with current optimizations. Emissive technologies such as OLED suffer from significantly higher power consumption depending on the display content (e.g., high-brightness white content). MicroLED displays are still in their infancy, and their efficiency suffers significantly with dense pixels (smaller microLED pixels).[1] In addition,

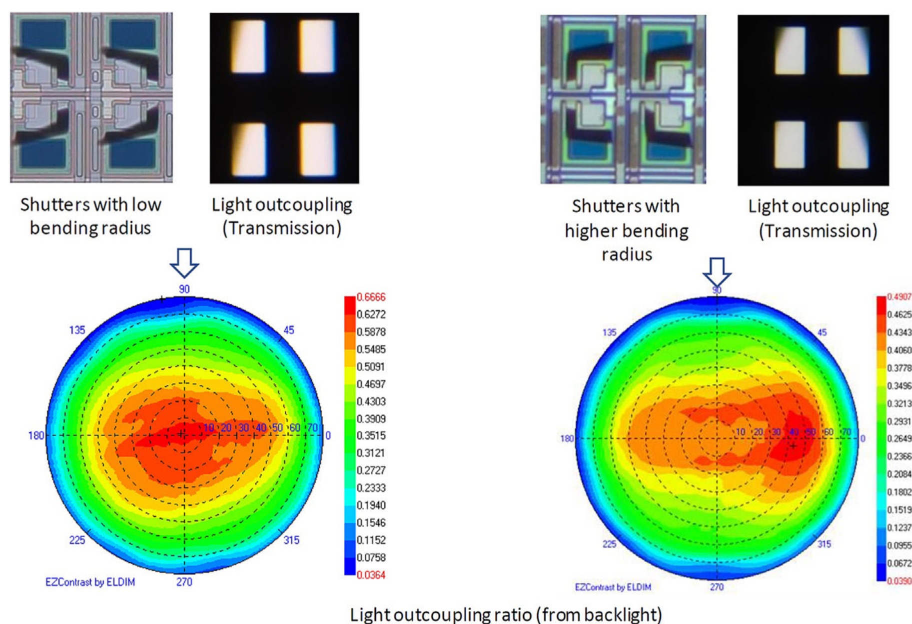

FIGURE 16 Light outcoupling characteristics of microelectromechanical systems shutter display.

approximately 30%–40% of the power dissipation of current-driven OLED pixels comes from the backplane, and the problem is worse with microLED pixels due to their lower voltage requirements.[1] The MEMS shutter display has shown better performance in this respect and still has room for future improvement.

The vertically translating structure of the MEMS shutter limits the pixel density of the display, but current optimizations already allow $92 \times 92\ \mu m$ pixels. Field sequential color technology eliminates the need for spatial color mixing (e.g., RGB pixels) and makes the pixel size already competitive with mainstream technology.

The self-aligned metal-oxide TFTs have been also optimized for parallel fabrication and characterized to ensure compatibility with MEMS elements. The MEMS shutter display demonstrator with further optimizations like vacuum packaging and better dielectric is under investigation and will be reported in the future.

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