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Monolithically Integrated GaN Power Stage for More Sustainable 48 V DC–DC Converters

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Abstract: In this article, a fully monolithically integrated GaN power stage with a half-bridge, driver, level shifter, dead time and voltage mode control for 48 V DC–DC converters is proposed and analyzed. The design of the GaN IC is presented in detail, and measurements of the single function blocks and the DC–DC converter up to 48 V are shown. Finally, considerations are given on a life cycle assessment with regard to the GaN power integration. This GaN power IC or stage demonstrates a higher level of integration, resulting in a reduced bill of materials and therefore lower climate impact.

Keywords: gallium nitride; power integrated circuits; monolithic integrated circuits; DC–DC converters; life cycle assessment; environmental factors

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1. Introduction

Power stages typically consist of power transistors (which form a topology like a half-bridge), drivers, control and protection circuity that are used as highly integrated building blocks to efficiently convert and regulate electrical power in low-voltage subsystems for data centers, telecommunications infrastructure, automotive or industrial sector, motor or battery-powered applications.

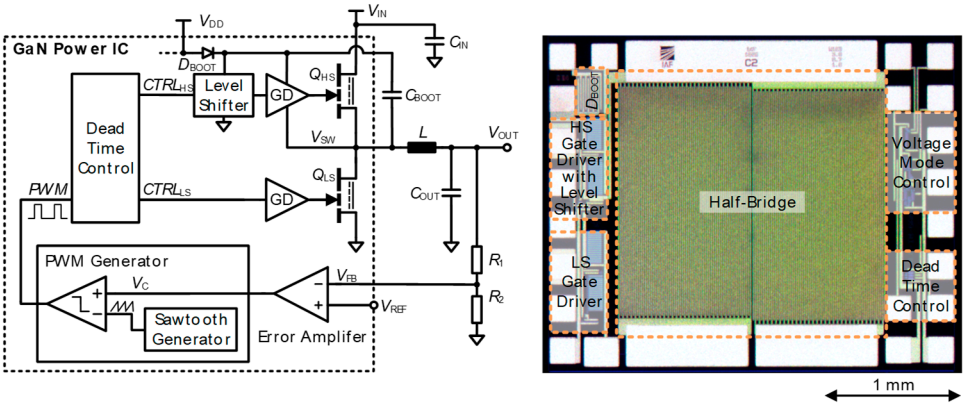
With the advent and ascent of gallium nitride (GaN) power transistors, these have been increasingly used in power stages to achieve primarily higher power density and efficiency [1,2]. In addition, the GaN technology with its lateral transistor structure (known as high electron mobility transistors, HEMTs) enables the monolithic integration of additional functions and circuits on a chip to realize cost-effective GaN power ICs [3–6] used in power converters with a reduced bill of material (BOM) and associated lower relative climate impact [7].

Commercial 80 V GaN power stages from EPC are already on the market, which integrate drivers, level shifter, logic and under-voltage lockout (UVLO) in addition to the half-bridge on a chip [8]. EPC's portfolio also includes standard monolithic low-voltage half-bridges [4], and many more are published in different voltage classes (see review in [9]) or also by the authors [10,11]. Furthermore, there is some research in the area of half-bridge driver integration including a level shifter, for example, in [12–15], and many more without level shifters. Also, a first control in GaN of the authors in [16] was shown for a half-bridge power stage.

In this article, a GaN power stage with an integrated half-bridge driver including a level shifter, dead time and voltage mode control is proposed, which are fully integrated into one die and thus can be used for highly compact DC–DC converters with reduced component effort and complexity.

Figure 1 shows the schematic and layout of the GaN power IC. The rest of this article is organized as follows. Section 2 describes the circuit implementation and operation of the proposed DC–DC converter system. Section 3 presents the measurement results

of the prototype chip, and Section 4 discusses consideration on life cycle assessments of GaN-based power stages. Finally, Section 5 concludes this article.



(**a**) (**b**)

Figure 1. GaN power stage for 48 V DC–DC converters consisting of a half-bridge with driver, level shifter, dead time control and voltage mode control. (**a**) Schematic and (**b**) chip photo.

2. Circuit Implementation

Figure 1 shows the top block diagram of the proposed GaN power IC. The power stage consists of a 48 V half-bridge, gate driver, level shifter, dead time and voltage mode control. The voltage mode control, in turn, consists of a PWM generator (sawtooth generator with comparator) and an error amplifier. The ICs are fabricated in a standard p-GaN gate power IC technology of the Fraunhofer IAF [6] with Si substrate (GaN-on-Si). In this technology, the heterojunction layers are grown on conductive 4-inch Si carrier substrates, and the circuits are manufactured in a III-V processing line based on optical stepper lithography. The total chip area is 3×2.5 mm^2. The area of the periphery is only 28.6%, while the power stage (in this case the half-bridge) is 71.4% of the chip area.

2.1. Half-Bridge

The half-bridge (HB) consists of low-side (LS) and high-side (HS) transistors with the parameter gate width ratio between the gate width of the HS and LS transistor $W_{G,HS/LS}$ given by: $k_G = W_{G,LS}/(W_{G,HS} + W_{G,LS}) = W_{G,LS}/W_{G,TOT}$. The gate width is proportional to the chip area and inversely proportional to the on-resistance R_{ON} of the power transistor. The optimal gate width ratio $k_{G,OPT}$ was analyzed and derived in [11], depending on the duty cycle of a buck converter $DC = V_{OUT}/V_{IN}$ in steady state with continuous conduction mode (CCM) or critical conduction mode (CRM) only for the conduction losses. The function is given by [11]:

$$k_{G,OPT} = \frac{\sqrt{DC - DC^2} + DC - 1}{2DC - 1} \quad (1)$$

In [17], the optimal on-resistance is calculated including conduction, switching, gate drive, reverse recovery, output capacitance charge and diode conduction loss with normalized device-specific parameters. If the optimum gate width ratio is calculated on the basis of the analysis and calculation in [17], this coincides with (1), although only the conduction losses were considered in the derivation. The realized half-bridge is symmetrical and has two identical HS/LS transistors. This results in a gate width ratio of 50% optimal for, e.g., 24-to-12 V conversions.

2.2. Gate Driver and Level Shifter

The gate driver is a single path, three stage with rail-to-rail driving based on bootstrapping. The first stage is a NOT gate (in detail, a direct-coupled FET logic inverter), and the second stage is a push–pull buffer with another NOT gate extended with a bootstrapping

circuit consisting of diode and stacked MIM capacitor with approx. 10 pF. At this point, reference is made to the design guide for monolithically integrated GaN gate drivers [18]. The driver is designed identically for HS and LS, but the HS driver has an additional protective diode. The first NOT gate stage of the HS driver is used as a level shifter, and the driver is additionally supplied with a bootstrap circuit, whereby only the bootstrap diode D_{BOOT} is integrated on the chip (see Figure 1). Further details to the design and a schematic of the HS driver can be found in [16]. The design of the level shifter is simple, although there are already more complex ones in GaN [13,15,19–21].

2.3. Dead Time Control

The dead time control is realized by two logic gates (AND and NAND) and stacked MIM capacitors to design an *RC* element. The dead time can be further increased by an external capacitor. Further dead time circuits are realized in [14,22–24].

2.4. Voltage Mode Control

The voltage mode control is based on a PWM generator consisting of a comparator and a sawtooth generator and an error amplifier with external type III compensation. The sawtooth generator is a hysteresis comparator with a charging unit. Further details on the design and a schematic of the sawtooth generator can be found in [16]. An overview of two sawtooth generators is given in [22]. The comparator consists of a differential stage with a cross-coupled latch and output stage and is similar to [25].

3. Measurement Results

The GaN IC is soldered in a DIL engineering package and then bonded. The package is plugged into an adapter located on a DC–DC converter board and is shown in Figure 2. The PCB is not designed for high power density but to provide a flexible platform for measuring the GaN IC. The GaN IC was measured step by step, from static to dynamic characterization of function blocks up to the converter system. Some highlights of the measurements are shown.

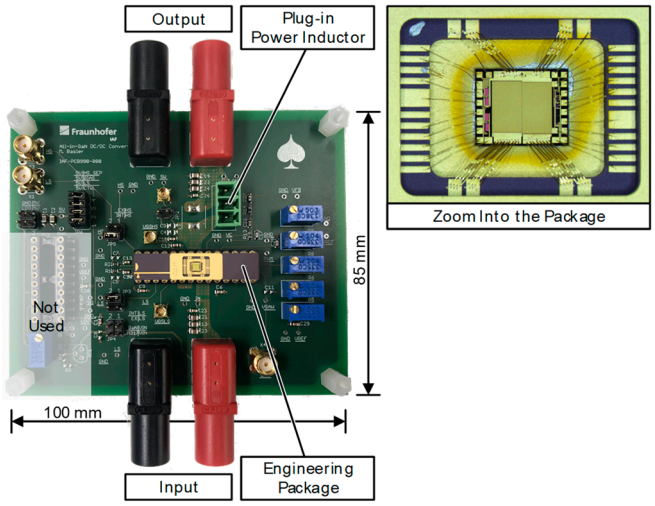


Figure 2. Experimental setup of the GaN IC (3 × 2.5 mm^2) in the DIL engineering package, which is plugged into an adapter on a DC–DC converter board. In addition, an inset is shown of the zoom into the package.

The static output and breakdown characteristics of the half-bridge are shown in Figure 3. The on-resistance is 120 mΩ, and the breakdown voltage is >80 V. Next, the HB driver including the level shifter is characterized with ext. C_{BOOT} = 100 nF. The integrated stacked MIM capacitors of the bootstrapped NOT gate are increased externally with further 1 nF, which value has not been optimized. Figure 3 shows the supply current of the driver

$I_{DD,DRV}$ as a function of the switching frequency f_{SW} with a supply voltage V_{DD} of 5/6 V. The quiescent current is 0.7/0.8 mA (f_{SW} = 0 kHz) and increases proportionally with the frequency, which is to be expected. This measurement is supplemented by a dynamic characterization with a constant input voltage V_{IN} and preset PWM signals using an arbitrary wave generator. Figure 4 shows the measurement of V_{SW}, as well as $V_{GS,HS/LS}$ with two input voltages of 24 V/48 V and three duty cycles of 10/50/90% at V_{DD} = 6 V, f_{SW} = 100 kHz, DC = 50%, t_{DEAD} = 100 ns. $V_{GS,HS}$ is not measured directly but calculated by $V_{G,H}$-V_{SW}. The high level of $V_{GS,HS}$ is reduced by the voltage drop across the bootstrap diode D_{BOOT} (see Figure 1) of 1–1.5 V. To achieve acceptable gate overdrive, the supply voltage is increased to 6 V. The half-bridge driver and level shifter are strongly influenced and slowed down by the high 2DEG sheet resistance. The driver was tested to 1 MHz and has a min. input pulse width of 25 ns.

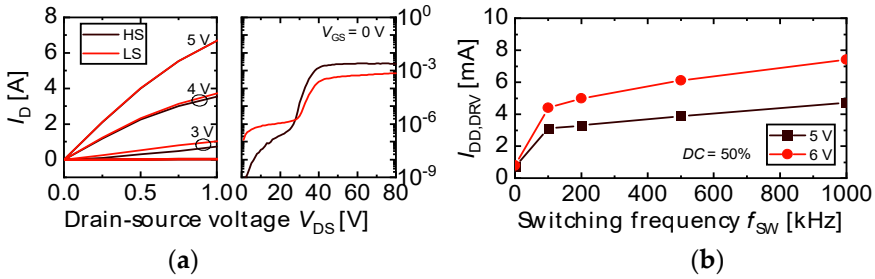


Figure 3. (**a**) Output and breakdown characteristic for HS/LS transistor and (**b**) driver current $I_{DD,DRV}$ as a function of the switching frequency with V_{DD} = 5/6 V and DC = 50%.

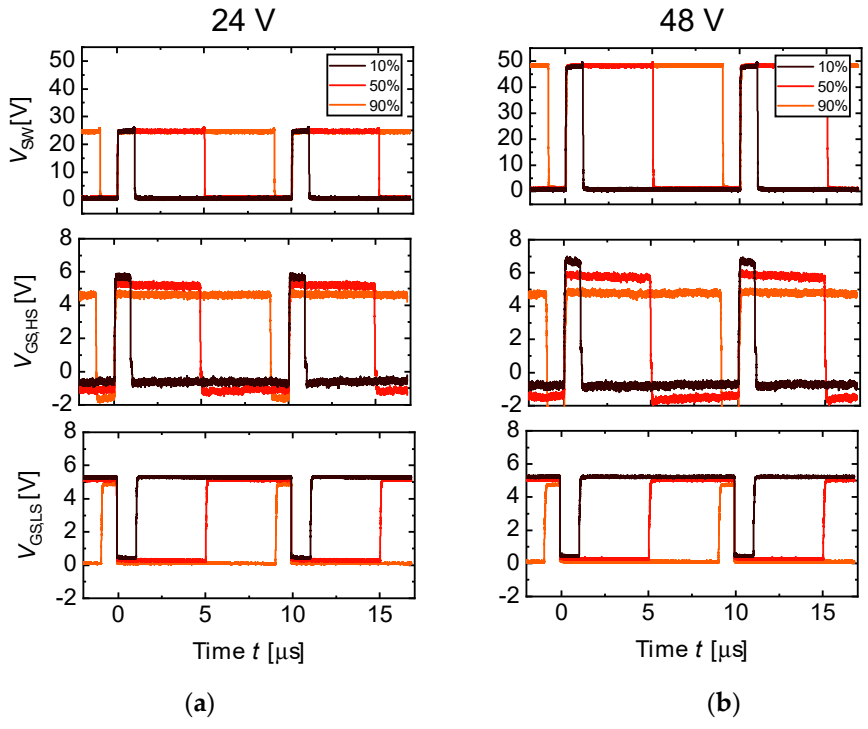


Figure 4. Switching characterization of the driver (V_{SW}, $V_{PWM,HS/LS}$) with an input voltage of (**a**) 24 V and (**b**) 48 V at V_{DD} = 6 V, f_{SW} = 100 kHz, and three different duty cycles DC = 10/50/90%.

The next step is the commissioning of the voltage mode control with the dead time control. The sawtooth carrier signal must be provided by a function generator due to a layout error on the GaN IC. The supply current is 1.5 mA at V_{DD} = 6 V. All measuring points are loaded with 3.9 pF by the passive probes. Figure 5 shows a measurement of the PWM generator with three different frequencies of the carrier signal (50/100/150 kHz) at the same operating point with the static values V_{FB} = 2.66 V and V_{REF} = 2.95 V. The driving

strength of the output stage of the comparator is not very high, as it was designed for low power consumption. In combination with the load of the probes, the rise time of the PWM signal is limited. This becomes clear from the different positive duty cycles of 23/42/51% at the same operating point with different carrier signal frequencies. The dead times for the frequency variation in Figure 5 are: $t_{DEAD,HI}$ = 278/316/326 ns (between the LS turn-off, HS turn-on) and $t_{DEAD,LO}$ = 202/171/166 ns (between the HS turn-off, LS turn-on). The output of the dead time logic is also additionally affected by the probes.

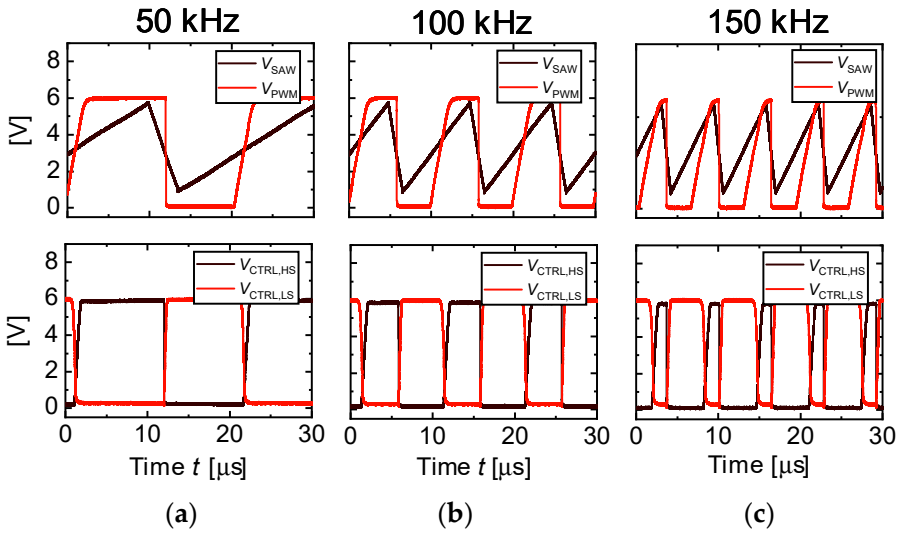


Figure 5. Measurement of the PWM generator and dead time control with the three different carrier frequencies (**a**) 50 kHz, (**b**) 100 kHz, and (**c**) 150 kHz at the same operating point (V_{FB} = 2.66 V and V_{REF} = 2.95 V).

Characterization as a synchronous buck converter is shown in Figure 6 without voltage mode control. The power inductor L has an inductance of 220 µH (component designation: WE 74437529203221). The input and output capacitance banks each have a value of 6.7 µF (3 × 2.2 µF + 0.1 µF). Figure 6 shows exemplarily two measurements at 24 V and 48 V input voltage under the same conditions (V_{DD} = 6 V, f_{SW} = 100 kHz, DC = 50%, t_{DEAD} = 100 ns, R_L = 24 Ω).

Table 1 compares this work to the state-of-the-art DC–DC synchronous buck converter with integrated power stage including a half-bridge, driver and level shifter using GaN technology.

Table 1. Comparison of GaN-based DC–DC converters with integrated power stage including a half-bridge, driver, and level shifter.

	[13]	[14]	[15]	**This Work**
Technology	GaN-on-Si	GaN-on-SOI	GaN-on-SOI	GaN-on-Si
Int. Dead Time	Yes	Yes	No	Yes
Int. Control	Yes	No	No	Yes
Die size [mm^2]	16.75	-	5.26 [1]	7.5
Power Supply [mW]	13.8	-	-	26.4
Max. V_{IN} [V]	48–400	200	50	80
Max. I_{OUT} [A]	5	10		4 [2]
Max. P_{OUT} [W]	240	223	100	≈100 [2]
f_{SW} [MHz]	≤50	0.25–0.5	≤1	≤1
η_{PEAK} [%]	94.5	98.3	96	-

[1] Estimated from chip photos, [2] Estimated from *IV* curve.

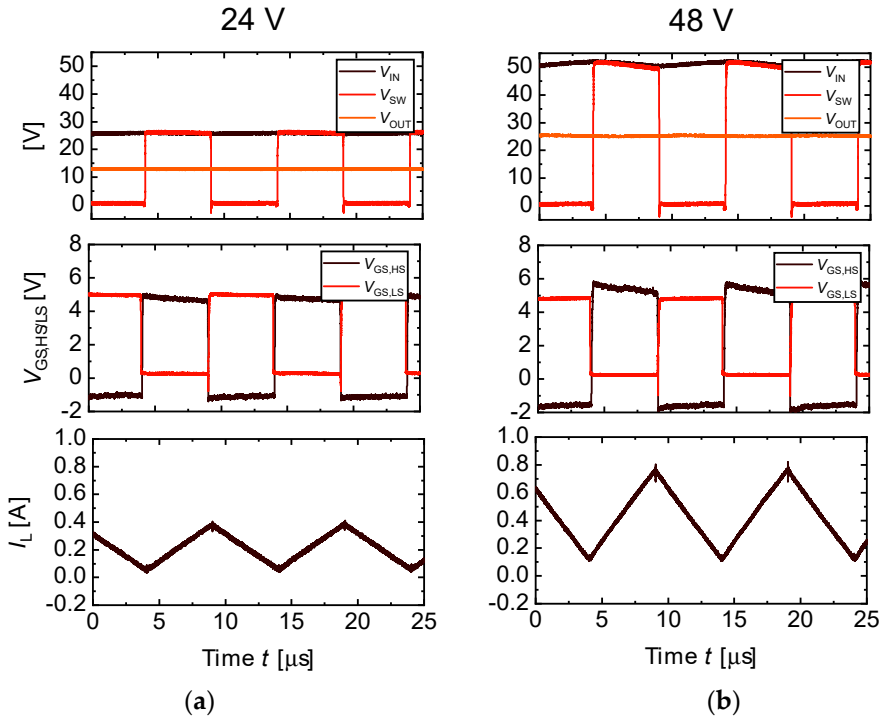


Figure 6. Switching characterization of the DC–DC converter (V_{IN}, V_{SW}, V_{OUT}, $V_{GS,HS/LS}$, I_L) with an input voltage of (**a**) 24 V and (**b**) 48 V at V_{DD} = 6 V, f_{SW} = 100 kHz, and load of 24 Ω.

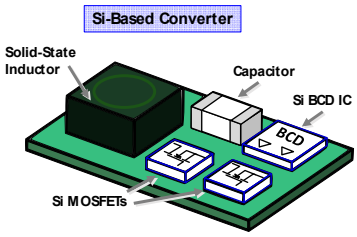
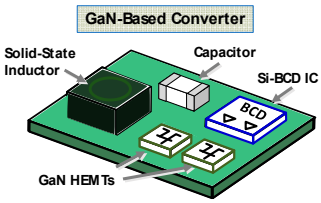
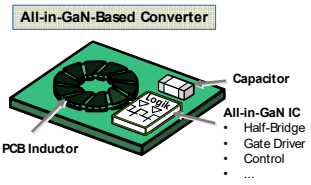
4. Considerations on Life Cycle Assessment

In the following, three different scenarios of DC–DC converters with different power stages, listed and visualized in Table 2, are compared, and considerations on life cycle assessment (LCA) are made. The most important converter parameters are V_{IN}, V_{OUT}, I_{OUT}, and f_{SW}, which are decisive for the power stage. On the converter side, efficiency is the most important parameter alongside power density, which depends on the load. In most cases, however, there are only energy efficiency requirements, e.g., from the EU, for products such as (uninterruptible) power supply units, servers, computers, etc., but not specifically for the (auxiliary) DC–DC converters used in them. There are also no weighted efficiencies as for inverters. Only the Energy Star® defines minimum required efficiencies for DC–DC converters, e.g., for rated output power $\leq$ 500 W, 70/82/89/85% (for 10/20/50/100% load level) [26]. For this reason, the peak efficiency is still a decisive evaluation criterion, and the load/user/mission profile must be known for detailed analyses.

Nevertheless, there are some figures of merit (FOMs), e.g., $R_{ON}{\cdot}A$, $R_{ON}{\cdot}Q_G$ or price$\cdot R_{ON}$ for the power semiconductors/materials used in the power stage. The FOMs for 100 V devices are listed for the three scenarios. The data are taken from [27]. The conduction and switching losses can be deduced from these FOMs. What is important for the LCA, however, is how high the CO_2 equivalent (CO_2eq) is for a device used. Table 2 lists the required electricity for semiconductor manufacturing (substrate, front-end of line, and partly back-end of line), whereby the data are taken from [28,29]. All three technologies (Si MOSFET, Si BCD/CMOS, GaN) have similar values, whereby the packaging is not taken into account here and contributes a further significant factor. This value simply has to be multiplied by the CO_2 emission per kWh. In addition, there are various environmental impacts that are categorized, e.g., climate change, ozone depletion, resource use, etc., and which must be considered in an LCA [28]. If scenario 2 is realized instead of 1, half of the semiconductor chip area can be saved and therefore also half of the CO_2eq. In addition, the Si MOSFETs require a package due to the vertical device geometry, which has a negative impact on the CO_2 footprint. Low-voltage GaN HEMTs with their lateral structure, on the other hand, also enable a chip-scale or flip-chip package solution. The low capacitances of GaN HEMTs allow a further increase in switching frequency, which miniaturizes the passive components

and reduces the amount of copper used in the inductor and the PCB size, for example. The functional integration to the power semiconductors in scenario 3 can further reduce the size required for packaging and PCB. Thus, monolithic integration in GaN has a positive effect and can reduce the use of materials and resources as well as the relative climate impact for more sustainable power stages, which is why 48 V GaN power stages are increasingly being used in data centers and motor applications like drones.

Table 2. Comparison of DC–DC converters in the context of power devices and their semiconductor material. The data are taken from [27–29].

Scenario			
Description Control and driving	Discrete half-bridge with two Si MOSFETs Si BCD/CMOS IC	Discrete half-bridge with two GaN HEMTs Si BCD/CMOS IC	Monolithic GaN half-bridge with opt. int. driver, control, etc. GaN (int. to the GaN half-bridge)
$R_{ON} \cdot A$ [mΩ·cm^2] @100 V	0.513	0.225	0.225
$R_{ON} \cdot Q_G$ [mΩ·nC] @100 V	288	31.2	31.2
Price R_{ON} [€·Ω] @100 V	1.33×10^{-2}	1.15×10^{-2}	1.15×10^{-2}
El. req. for manufacturing [kWh/cm^2] [1]	Si MOSFET: 2.45 [2] Si BCD/CMOS: 0.67–3.02	GaN: 2 [3]–2.43 Si BCD/CMOS: 0.67–3.02	GaN: 2 [3]–2.43

[1] Included substrate, front-end of line, back-end of line; packaging not included, [2] Back-end of line not included, [3] Yield not included.

5. Conclusions

This article presents a GaN IC with an integrated half-bridge, driver, level shifter, dead time and PWM generator with error amplifier to realize a voltage mode control. The half-bridge and driver with level shifter are measured up to an input voltage of 48 V also in the DC–DC converter application with inductor currents less than 1 A. The driver has a low quiescent current of less than 1 mA and also features an integrated bootstrap diode. Less than 1/3 of the chip area of the GaN IC is for the additional periphery of the power stage, which would usually have to be realized discretely in other technologies. The reduction in the BOM, PCB area, saving of additional packages, e.g., the driver, reduces the CO_2eq and thus the climate impact.

Author Contributions: Conceptualization, M.B., S.M. and R.R.; methodology, M.B.; software, M.B. and S.M.; validation, M.B.; formal analysis, M.B.; investigation, M.B.; resources, F.B.; data curation, M.B.; writing—original draft preparation, M.B.; writing—review and editing, M.B., S.M., R.R., F.B. and R.Q.; visualization, M.B.; supervision, R.R. and R.Q.; project administration, M.B.; funding acquisition, R.Q. All authors have read and agreed to the published version of the manuscript.

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