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Synergistic Dynamical Decoupling and Circuit Design for Enhanced Algorithm Performance on Near-Term Quantum Devices

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Abstract: Dynamical decoupling (DD) is a promising technique for mitigating errors in near-term quantum devices. However, its effectiveness depends on both hardware characteristics and algorithm implementation details. This paper explores the synergistic effects of dynamical decoupling and optimized circuit design in maximizing the performance and robustness of algorithms on near-term quantum devices. By utilizing eight IBM quantum devices, we analyze how hardware features and algorithm design impact the effectiveness of DD for error mitigation. Our analysis takes into account factors such as circuit fidelity, scheduling duration, and hardware-native gate set. We also examine the influence of algorithmic implementation details, including specific gate decompositions, DD sequences, and optimization levels. The results reveal an inverse relationship between the effectiveness of DD and the inherent performance of the algorithm. Furthermore, we emphasize the importance of gate directionality and circuit symmetry in improving performance. This study offers valuable insights for optimizing DD protocols and circuit designs, highlighting the significance of a holistic approach that leverages both hardware features and algorithm design for the high-quality and reliable execution of near-term quantum algorithms.

Keywords: dynamical decoupling; quantum error mitigation; quantum circuit design; near-term quantum devices

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1. Introduction

Near-term quantum (NISQ) devices [1] hold immense potential but face hurdles in accuracy and reliability due to inherent noise arising from environmental fluctuations, imperfect gate operations, and qubit interactions. Moreover, limitations in qubit count and connectivity restrict the complexity of achievable quantum circuits. Robust error mitigation techniques [2] are therefore crucial for unlocking the full potential of NISQ devices. Dynamical decoupling (DD) [3–6] stands out as a powerful approach for NISQ devices due to its simplicity and low resource overhead. It mitigates decoherence errors by applying a carefully designed sequence of control pulses during idle periods of the qubits. These pulses effectively suppress the unwanted interaction between qubits and their environment, protecting the desired quantum state. DD has been demonstrated in various quantum systems, including spins [7–12], superconducting qubits [5,13,14], and trapped ions [15]. The effectiveness of DD extends beyond decoherence suppression as it can also mitigate crosstalk [13,16–19] and coherent errors [20].

Numerous DD sequences have been developed, with prominent examples including Carr–Purcell (CP) [21], Carr–Purcell–Meiboom–Gill (CPMG) [22], XY4 [23–26], KDD [27], and Uhrig dynamical decoupling (UDD) [28]. However, the effectiveness of different sequences varies significantly [29]. Prior work has shown that the CPMG sequence outperforms the CP sequence [4]. Additionally, higher-order sequences generally outperform lower-order sequences [4,29], but optimizing pulse intervals within CPMG and XY4 sequences can achieve comparable performance [29]. In the context of the quantum approximate optimization algorithm (QAOA) [30–34], DD sequences like CP, CPMG, and XY4

significantly enhance performance, while KDD shows worse performance on IBM quantum processing units (QPUs) [35]. Combining DD sequences with pulse-level optimization in QAOAs can further improve performance [35]. While DD sequences mitigate errors, these additional control pulses can also introduce errors such as gate infidelities or crosstalk. To address this trade-off, adaptive approaches have been explored [36], which estimate the potential benefit of DD for each qubit combination and selectively apply DD to the subset that offers the most benefit. Furthermore, recent work has explored the use of empirical learning schemes for enhancing DD effectiveness on quantum processors [37], leveraging data-driven techniques to optimize the implementation of DD sequences, leading to improved error suppression capabilities.

Despite significant research on DD sequences, the interplay between their effectiveness and specific algorithm implementations on real hardware remains underexplored. This study bridges this critical gap by investigating how factors such as transpilation efficiency [38–42], circuit structure [43,44], and gate decompositions [44,45] influence DD performance on IBM QPUs. By analyzing how these implementation details interact with the chosen DD sequence, we uncover synergistic effects that enhance overall algorithm performance on hardware. This focus on codesigning hardware and software offers deeper insights than separate studies of DD or individual circuit optimization techniques. We focus on the CPMG sequence due to its established effectiveness, robustness [4], and good performance for QAOAs on IBM QPUs [35].

Our analysis of results from eight IBM QPUs demonstrates an inverse relationship between the initial performance of the algorithm without DD and the effectiveness of DD. While DD generally enhances performance and robustness, circuits with inherently higher fidelity and shorter execution times benefit less from DD than those with lower initial performance. Moreover, factors such as hardware-native gates of QPUs, the chosen gate decomposition strategy, and the optimization level can also influence the effectiveness of DD. Additionally, using gates with consistent directionality and maintaining circuit symmetry during design lead to improved performance. These findings emphasize the importance of a holistic approach that considers both hardware and software optimization for the successful execution of algorithms with DD on NISQ devices, providing valuable insights for optimizing DD protocols and designing more robust quantum algorithms.

This paper is structured as follows. Section 2 outlines the methodology, presenting the benchmark circuits and metrics used to evaluate algorithm performance. Hardware considerations and a proposed synergistic design approach combining both hardware and algorithmic factors are also described. Section 3 then analyzes the results, exploring the impact of various hardware factors, including circuit fidelity, schedule duration, and native gate sets, as well as algorithmic factors, including different implementations, DD sequences, and optimization levels. Finally, Section 4 discusses the key findings and concludes.

2. Methodology

We experimentally investigate the impact of hardware and algorithmic factors on the effectiveness of dynamical decoupling in superconducting quantum processes. Hardware factors, such as circuit fidelity, schedule duration, and native gate sets, define the fundamental capabilities of a quantum device. Conversely, algorithmic factors encompass the design choices made during algorithm implementation (specific sequence of quantum operations), error suppression strategy (selection of a DD sequence), and circuit optimization techniques. These algorithmic choices ultimately determine how efficiently the inherent capabilities of the hardware are utilized for optimal performance. Understanding these factors can potentially improve the practical implementation of algorithms on near-term quantum devices.

2.1. Benchmark Circuits and Metrics

We first present benchmark circuits used in our demonstration and metrics employed to assess algorithm performance and DD effectiveness.

2.1.1. QAOA for Portfolio Optimization

We employ QAOAs for portfolio optimization as benchmarks. The portfolio optimization problem aims to select the optimal portfolio from all available options to maximize expected returns while minimizing financial risk. The QAOA has the potential to address this challenge [46–48]. The cost Hamiltonian, which describes the portfolio optimization problem for n available assets, is expressed as [47]

$$\hat{H}_c = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} c_{i,j} \hat{Z}_i \hat{Z}_j - \sum_{i=1}^{n} k_i \hat{Z}_i. \tag{1}$$

The parameters $c_{i,j}$ and k_i in Equation (1) depend on factors specific to the portfolio optimization problem, such as the covariance matrix and the return vector. In particular, $c_{i,j} = \frac{\lambda}{2}(q\sigma_{ij} + A)$ and $k_i = \frac{\lambda}{2}\left[A(2B - n) + (1 - q)\mu_i - q\sum_{j=1}^{n} \sigma_{ij}\right]$, where λ is the global scaling factor, q is risk preference, σ_{ij} is the covariance between assets i and j, A is the penalty factor, B is the number of assets to be chosen, and μ_i is the expected return of asset i. The terms $\hat{Z}_i\hat{Z}_j$ and $\hat{Z}_i$ correspond to the ZZ interaction on qubits (i, j) and Pauli Z operator acting on qubit i, respectively. The mixer Hamiltonian is given by [30]

$$\hat{H}_m = \sum_{i=1}^{n} \hat{X}_i, \tag{2}$$

where $\hat{X}_i$ is the Pauli X operator acting on qubit i. After a QAOA depth of p, the total system evolves to $|\psi\rangle = \prod_{j=1}^{p} e^{-i\gamma_j \hat{H}_c} e^{-i\beta_j \hat{H}_m} |\psi_0\rangle$, where $|\psi_0\rangle$ is the eigenstate of the mixer Hamiltonian. The aim of the QAOA is to find $2p$ parameters $(\beta_1, ..., \beta_p, \gamma_1, ..., \gamma_p)$ that minimize the expectation value of the cost Hamiltonian $F = \langle\psi|\hat{H}_c|\psi\rangle$. We define the approximation ratio of the QAOA as

$$r = \frac{F - F_{\max}}{F_0 - F_{\max}}, \tag{3}$$

where F_0 represents the optimal value and $F_{\max}$ signifies the worst-case value.

Our study uses a QAOA with qubit numbers ranging from 3 to 12 and a depth of 1. To establish a baseline for experimental results, we present the simulation results conducted in a noise-free environment with Qiskit's Qasm simulator in Table 1. The version of Qiskit used throughout this paper is 0.45.3. All data use 30,000 circuit repetitions (shots). We observe that the approximation ratio and success probability decrease as the number of qubits increases.

Table 1. Noise-free simulation results of the quantum approximate optimization algorithm (QAOA) for portfolio optimization using Qiskit's Qasm simulator with 30,000 shots.

Number of Qubits	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
Approximation ratio	0.9751	0.4342	0.3776	0.3734	0.3589	0.3144	0.2806	0.3241	0.2933	0.3161
Success probability	0.9747	0.1536	0.1131	0.0422	0.0227	0.0124	0.0065	0.0057	0.0018	0.0006

2.1.2. Metric Definition

To quantify the impact of noise, we introduce two normalized metrics: the normalized approximation ratio (NAR) and the normalized success probability (NSP). These metrics are defined as

$$\text{NAR} = r_\epsilon / r_0, \tag{4}$$

$$\text{NSP} = p_\epsilon / p_0, \tag{5}$$

where r_ϵ and p_ϵ represent the approximation ratio and success probability obtained under noise conditions. r_0 and p_0 denote corresponding values obtained from the simulated noise-free case (Table 1). For the same problem instances, we use identical values of r_0 and p_0 for evaluation. Due to noise, the NAR and NSP typically exhibit values less than one. However, in rare instances, these metrics may exceed unity, indicating that specific noise patterns or randomness enhance performance compared to the simulated noise-free case.

Without any error mitigation being applied, the NAR and NSP for algorithms executing on real noisy quantum devices are given by

$$\mathrm{NAR_B} = r_b/r_0, \tag{6}$$
$$\mathrm{NSP_B} = p_b/p_0, \tag{7}$$

where B represents results obtained from real hardware without error mitigation. r_b and p_b represent the corresponding approximation ratio and success probability, respectively. When a specific error mitigation strategy, such as the DD sequence, is applied, the NAR and NSP are given by

$$\mathrm{NAR_{DD}} = r_d/r_0, \tag{8}$$
$$\mathrm{NSP_{DD}} = p_d/p_0, \tag{9}$$

where DD denotes the application of DD sequences. r_d and p_d represent the approximation ratio and success probability, respectively, with error mitigation. To assess DD effectiveness in error mitigation, we introduce two additional metrics: Δ_{NAR} and Δ_{NSP}. These metrics are defined as the difference between the corresponding values obtained with and without DD sequences:

$$\Delta_{\mathrm{NAR}} = \mathrm{NAR_{DD}} - \mathrm{NAR_B}, \tag{10}$$
$$\Delta_{\mathrm{NSP}} = \mathrm{NSP_{DD}} - \mathrm{NSP_B}. \tag{11}$$

A positive value for Δ_{NAR} and Δ_{NSP} indicates a successful improvement in performance resulting from the utilization of DD sequences.

We further introduce the concept of error mitigation success rate (EMSR) to quantify the robustness of an error mitigation strategy. EMSR is defined as the percentage of experimental trials where error mitigation improved the outcome compared to no mitigation. A high EMSR indicates consistent performance improvement while a low EMSR suggests limited effectiveness or potential performance degradation. We employ two EMSR metrics in this study, $\mathrm{EMSR_{AR}}$ and $\mathrm{EMSR_{SP}}$, depending on whether the approximation ratio or success probability is used. Positive values of Δ_{NAR} and Δ_{NSP} contribute to increased $\mathrm{EMSR_{AR}}$ and $\mathrm{EMSR_{SP}}$, respectively.

2.2. Hardware Considerations

This section provides information about the IBM quantum devices used in our experiments. The QPUs with 27 qubits, namely ibmq_mumbai, ibmq_kolkata, ibm_cairo, and ibmq_ehningen, operate using basis gates {CX, ID, RZ, SX, X}, where ID represents identity gate, RZ performs a single qubit rotation around the z-axis, X is the NOT gate, and SX is the square root of X. On the other hand, the QPUs with 127 qubits, specifically ibm_kyoto, ibm_cusco, ibm_brisbane, and ibm_sherbrooke, utilize basis gates {ECR, ID, RZ, SX, X}, where ECR is the echoed cross-resonance gate.

Figure 1a illustrates the schedule of a native CX gate on ibm_cairo. This implementation employs a single-pulse gate duration of 112 dt and a cross-resonance (CR) gate duration of 544 dt, leading to a total duration of 1312 dt, where dt represents the system cycle time. In contrast, Figure 1b depicts the schedule of a native ECR gate on ibm_cusco. Here, the single-pulse and CR gate durations are 88 dt and 416 dt, respectively, resulting in a shorter total duration of 920 dt. The CX gate is typically implemented using one ECR gate and multiple single-qubit gates. A further decomposition of the CX gate into ECR

and single-pulse gates at pulse level enables the elimination of single-pulse gates during circuit optimization [44]. Additionally, CX-based IBM QPUs, where CX is the native gate, support the operation of CX in two directions. On the other hand, ECR-based QPUs, where ECR is the native gate, typically only support the ECR gate in one direction. Consequently, quantum circuits designed for these latter devices need to be decomposed into sequences of gates that include only the supported direction of the ECR.

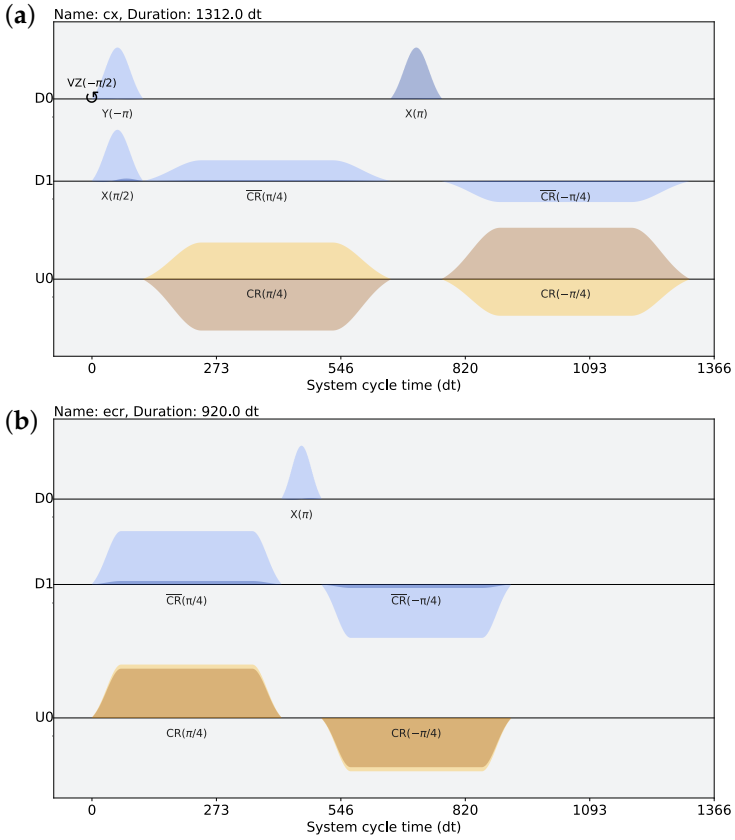


Figure 1. Schedule of hardware-native two-qubit gates: (**a**) CX gate on qubit pair (0,1) of ibm_cairo, and (**b**) echoed cross-resonance (ECR) gate on qubit pair (0,1) of ibm_cusco. The system cycle time (1 dt) is $2/9$ ns ≈ 0.22 ns in ibm_cairo, while it is 0.50 ns in ibm_cusco. D_i represents the drive channel acting on qubit i, and U_j is the control channel for a corresponding qubit pair (c, t) driving the control qubit c at the frequency of the target qubit t.

2.3. Synergistic Design Approach

This section describes a synergistic design approach for maximizing the performance and robustness of algorithms on near-term quantum devices. This approach acknowledges the critical interplay between the hardware's capabilities and the design choices made in the software implementation. The quality of algorithm implementation directly affects the performance. Key aspects include the efficiency of transpilation processes, specific gate types used, and the overall symmetry of the algorithm structure. For instance, studies have shown that the algorithm-oriented qubit mapping (AOQMAP) method [42] offers advantages in transpilation for variational quantum algorithms (VQAs) [49] compared to popular compilers such as Qiskit [50] and Tket [51] by introducing fewer two-qubit gates, maintaining a shallower circuit depth, and promoting higher symmetry [43].

In this study, we utilize the AOQMAP method [42] to efficiently map circuits onto hardware, aiming to minimize SWAP gates and circuit depth on linear topologies. Subsequently, we examine two implementations of QAOAs for portfolio optimization on CX-based IBM QPUs. These implementations differ in their choice of gate decompositions within the algorithms. The first implementation, referred to as CX implementation, directly

decomposes the gates in the QAOA into basis gates of the QPUs using Qiskit's transpiler with optimization level 3. In comparison, the second implementation, referred to as CZ implementation, initially decomposes gates in algorithms into CZ and single-qubit gates. Then, Qiskit's transpiler with optimization level 3 is used to perform optimization and decomposition into basis gates of QPUs. Previous studies have demonstrated that this CZ decomposition approach outperforms CX decomposition for ZZ and ZZ-SWAP gates in the QAOA on IBM QPUs [44]. During implementation, we also explore different optimization level settings in Qiskit and investigate their impact. To ensure consistency in evaluations, we employ identical benchmark circuits and parameters. Additionally, we consistently use 30,000 shots for each demonstration. Within the Qiskit framework, we default to using optimization level 3.

We also investigate the effectiveness of two well-established DD sequences: CPMG and XY4. As illustrated in Figure 2, the CPMG sequence applies two X pulses separated by a delay of $\frac{t}{2}$, with additional delays of $\frac{t}{4}$ at the beginning and end. The parameter t represents the time interval during which the qubit remains idle, excluding the duration of single-qubit pulses and, in the case of CPMG, two X pulses. In comparison, the XY4 sequence utilizes two X and two Y pulses, each separated by a delay of $\frac{t}{4}$, with additional delays of $\frac{t}{8}$ at the beginning and end. Additionally, the "alap" (as late as possible) scheduling method, which schedules the stop time of instructions as late as possible, is used for scheduling gates and inserting DD sequences throughout our study. Figure 3 showcases the resulting implementations of a three-qubit QAOA with a CPMG sequence on a 27-qubit QPU ibm_kolkata using both CX and CZ implementations. Compared to CX implementation, CZ implementation employs all the same directed CX gates. Additionally, we observe an X gate inserted between control qubits of CX gates in the CZ implementation, potentially suppressing idle errors and improving performance. Moreover, CZ implementation shows improved symmetry compared to CX implementation. By simultaneously optimizing both hardware and software aspects through careful algorithm design, efficient transpilation techniques, and DD sequences, it is possible to fully exploit the capabilities of near-term quantum algorithms.

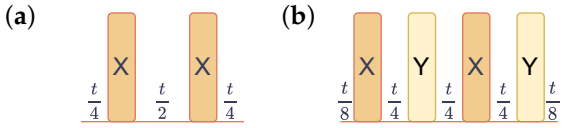


Figure 2. Two types of dynamical decoupling (DD) sequences: (**a**) Carr–Purcell–Meiboom–Gill (CPMG) and (**b**) XY4. The delay time t represents the idle time of the qubit minus the duration of the corresponding X or Y pulses.

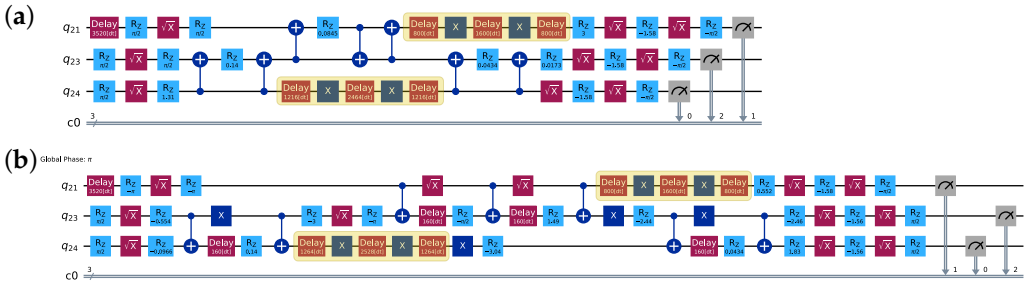


Figure 3. Two implementations of a three-qubit QAOA: (**a**) CX implementation and (**b**) CZ implementation, where both are decomposed and optimized using Qiskit's transpiler with optimization level 3. Highlighted yellow boxes represent CPMG sequences.

3. Results Analysis

This section delves into the examination of multiple factors that influence algorithm performance and DD effectiveness. These factors are classified into two main categories: hardware and algorithmic. More specifically, we thoroughly analyze the influence of circuit fidelity, schedule duration, and native gate set on the performance of DD sequences. Furthermore, we explore the impact of algorithm implementation, choice of DD sequence, and level of optimization on algorithm performance and DD effectiveness. The objective of these analyses is to provide invaluable insights into the design and optimization of algorithm implementation for achieving efficient execution on quantum devices.

3.1. Impact of Hardware Factors

Our investigation begins by examining how hardware characteristics affect algorithm performance and DD effectiveness. The CPMG sequence is chosen for our study due to its widespread adoption and relative simplicity, allowing us to gain fundamental insights. We analyze these factors using extensive datasets. The experiments involve varying the qubit counts from 3 to 12 and investigating different combinations of algorithm implementations, including the CX and CZ versions of the QAOA, as well as optimization levels 1 and 3 within the Qiskit framework. We conduct these experiments using eight QPUs, which consist of four 27-qubit devices—ibmq_mumbai, ibmq_kolkata, ibm_cairo, and ibmq_ehningen—and four 127-qubit devices: ibm_kyoto, ibm_cusco, ibm_brisbane, and ibm_sherbrooke. These extensive datasets provide a solid foundation for analyzing the impact of hardware factors on algorithm performance.

3.1.1. Circuit Fidelity

We first explore the impact of circuit fidelity on the performance. The fidelity of a circuit qc, denoted as $\mathcal{F}_{qc}$, measures the agreement between the actual operation of a quantum circuit and its ideal operation. The circuit fidelity can be mathematically represented as

$$\mathcal{F}_{qc} = \prod_{G_s \in qc} f_{G_s} \prod_{G_t \in qc} f_{G_t} \prod_{G_m \in qc} f_{G_m}, \tag{12}$$

where f_{G_s}, f_{G_t}, and f_{G_m} denote fidelities of a single-qubit gate G_s, a two-qubit gate G_t, and the measurement G_m, respectively, in the circuit. We focus on circuits with fidelities between 0.01 and 1. This broader range of fidelities establishes a solid basis for investigating the effectiveness of DD sequences under realistic noise conditions. We analyze various metrics defined in Section 2.1.2, including $\mathrm{NAR_B}$, $\mathrm{NAR_{DD}}$, $\mathrm{NSP_B}$, $\mathrm{NSP_{DD}}$, Δ_{NAR}, and Δ_{NSP}. The measured data and the corresponding circuit fidelity are fitted using a linear function. The correlation coefficient C_r and p-value are computed to assess the quality of linear approximation. C_r measures the strength and direction of the linear relationship, ranging from -1 (perfect negative correlation) to 1 (perfect positive correlation), with 0 indicating no association. The absolute value of C_r reflects the correlation strength: very strong (0.9–1.0), strong (0.7–0.9), moderate (0.4–0.7), weak (0.2–0.4), and very weak (0–0.2). It is important to note that correlation does not imply causation. The p-value is a complementary statistical measure that evaluates the strength of evidence against the null hypothesis of no correlation. A low p-value (typically below 0.05) suggests a statistically significant correlation, possibly not due to random chance. Linear fitting builds on correlation by determining the best-fit line equation, enabling predictions based on the observed relationship.

Figure 4 depicts a general trend of improved algorithm performance with increasing circuit fidelity. DD sequences enhance both the NAR and NSP on average. However, the NSP exhibits a wider range of variation for a given circuit fidelity compared to the approximation ratio, particularly at lower fidelities. Table 2 presents the average value, fitted function, correlation coefficient, and p-value for each metric. A stronger correlation is observed between NAR and circuit fidelity compared to NSP, suggesting a more pronounced dependence of NAR on fidelity. In contrast, the correlation between Δ_{NSP} and circuit fidelity is very weak, as evidenced by the low value of C_r and high p-value. This suggests that

the observed decrease in DD effectiveness might be due to random fluctuations or other factors not captured by circuit fidelity alone. The average improvement in NAR and NSP due to DD sequences is approximately 0.08. Moreover, the negative coefficients of the fitted lines for Δ_{NAR} and Δ_{NSP} suggest a potential decrease in DD effectiveness as circuit fidelity increases.

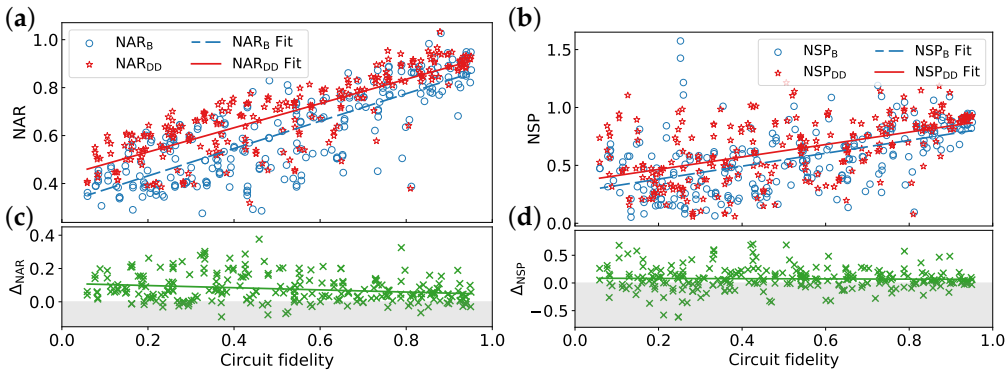


Figure 4. Impact of circuit fidelity on algorithm performance and DD effectiveness: (**a**) normalized approximation ratio (NAR), (**b**) normalized success probability (NSP), (**c**) improvement in NAR after applying DD (Δ_{NAR}), and (**d**) improvement in NSP after applying DD (Δ_{NSP}). Higher values of $\mathrm{NAR_B}$, $\mathrm{NAR_{DD}}$, $\mathrm{NSP_B}$, and $\mathrm{NSP_{DD}}$ indicate better performance on actual quantum devices. Values exceeding unity indicate that the performance achieved on the IBM quantum hardware surpasses the results obtained from the noise-free simulation. Positive values of Δ_{NAR} and Δ_{NSP} demonstrate improvements due to DD. The CPMG sequence is used for all data points. Each line in the graph represents a linear fit of the data. The reported $\mathrm{EMSR_{AR}}$ and $\mathrm{EMSR_{SP}}$ are 85.55% and 66.8%, respectively.

Table 2. Parameters derived from the analysis of Figure 4.

Metric	Mean	Fit Function	Correlation Coefficient	*p*-Value
$\mathrm{NAR_B}$	0.610	$y = 0.572x + 0.317$	0.809	0
$\mathrm{NAR_{DD}}$	0.687	$y = 0.506x + 0.430$	0.827	0
$\mathrm{NSP_B}$	0.556	$y = 0.558x + 0.270$	0.530	0
$\mathrm{NSP_{DD}}$	0.631	$y = 0.537x + 0.358$	0.521	0
Δ_{NAR}	0.077	$y = -0.065x + 0.111$	−0.209	0.00075
Δ_{NSP}	0.075	$y = -0.021x + 0.086$	−0.027	0.66997

3.1.2. Schedule Duration

We now investigate the influence of schedule duration τ and, in particular, the logarithmic transformation of schedule duration $\ln(\tau/\mathrm{dt})$ on algorithm performance and DD effectiveness. Schedule duration reflects the total time required to execute a quantum circuit and depends on the number and execution time of individual gates. Shorter durations potentially improve circuit fidelity by reducing the system's exposure to decoherence errors, but achieving them necessitates faster gates, which can be hardware-limited.

Figure 5 depicts the impact of $\ln(\tau/\mathrm{dt})$ on the defined metrics using the same datasets as in Figure 4. We observe that the algorithm performance degrades with increasing schedule duration, while DD effectiveness improves. However, Δ_{NSP} exhibits larger fluctuations for longer durations, suggesting that while DD sequences mitigate decoherence errors, potentially improving performance at longer durations, they could also introduce other error mechanisms, such as operation errors, that counteract this improvement. Table 3 summarizes corresponding parameters. The coefficients of the linear function for $\mathrm{NAR_B}$, $\mathrm{NAR_{DD}}$, $\mathrm{NSP_B}$, and $\mathrm{NSP_{DD}}$ indicate a suppressed decay in performance with increasing schedule duration by applying DD sequences. The correlation coefficients between these metrics and $\ln(\tau/\mathrm{dt})$ further support the effectiveness of DD sequences in reducing the dependence of performance (both NAR and NSP) on schedule duration. Δ_{NAR} exhibits

a statistically weak correlation with $\ln(\tau/\mathrm{dt})$, while Δ_{NSP} shows a very weak correlation. This observation aligns with the findings for circuit fidelity. However, Δ_{NSP} appears more sensitive to schedule duration compared to circuit fidelity, as indicated by a larger absolute correlation coefficient ($|C_r|$) and lower p-value.

Table 3. Parameters derived from the analysis of Figure 5.

Metric	Fit Function	Correlation Coefficient	p-Value
$\mathrm{NAR_B}$	$y = -0.238x + 3.136$	-0.731	0
$\mathrm{NAR_{DD}}$	$y = -0.196x + 2.764$	-0.691	0
$\mathrm{NSP_B}$	$y = -0.254x + 3.253$	-0.524	0
$\mathrm{NSP_{DD}}$	$y = -0.221x + 2.975$	-0.464	0
Δ_{NAR}	$y = 0.042x - 0.372$	0.295	0
Δ_{NSP}	$y = 0.033x - 0.278$	0.092	0.14281

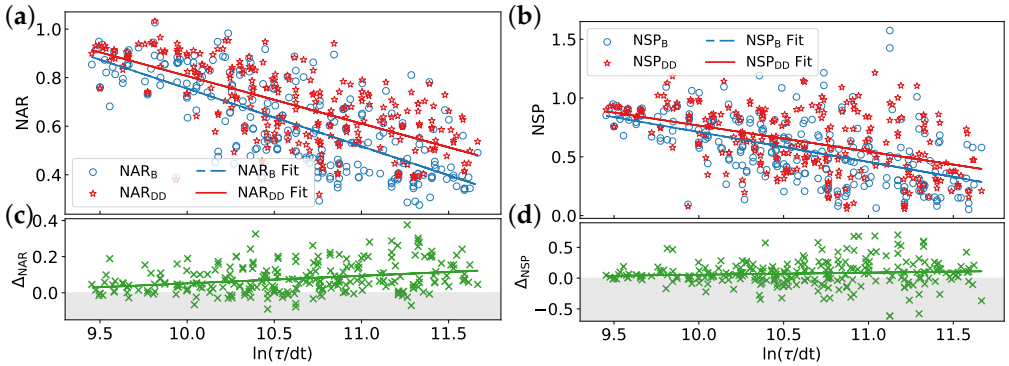


Figure 5. Influence of logarithmic transformation of circuit schedule duration ($\ln(\tau/\mathrm{dt})$) on algorithm performance and DD effectiveness with the same datasets as in Figure 4: (**a**) NAR, (**b**) NSP, (**c**) Δ_{NAR}, and (**d**) Δ_{NSP}.

Figure 6a–d illustrate the impact of circuit fidelity and schedule duration on $\mathrm{NAR_{DD}}$, $\mathrm{NSP_{DD}}$, Δ_{NAR}, and Δ_{NSP}, respectively. As observed in Figure 6a, $\mathrm{NAR_{DD}}$ exhibits degradation with increasing logarithmic schedule duration ($\ln(\tau/\mathrm{dt})$) and decreasing circuit fidelity. High performance is concentrated in the region where the schedule duration τ is below $e^{10.5}\mathrm{dt}$ and circuit fidelity surpasses 0.5. Conversely, low performance is primarily observed for τ exceeding $e^{10.5}\mathrm{dt}$ and fidelities below 0.5. A similar trend is evident for $\mathrm{NSP_{DD}}$ in Figure 6b. However, unlike $\mathrm{NAR_{DD}}$, achieving a high $\mathrm{NSP_{DD}}$ value remains feasible even for longer schedule durations and lower fidelities. This suggests that $\mathrm{NSP_{DD}}$ is less sensitive to these factors compared to $\mathrm{NAR_{DD}}$. Figure 6c,d further demonstrate the effectiveness of DD sequences, particularly at longer durations. This is potentially due to the ability of DD sequences to mitigate decoherence errors that become more prominent at these timescales.

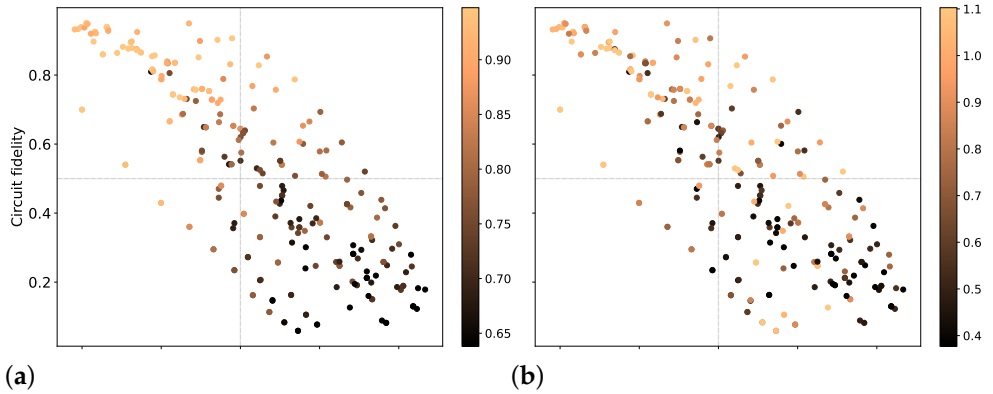
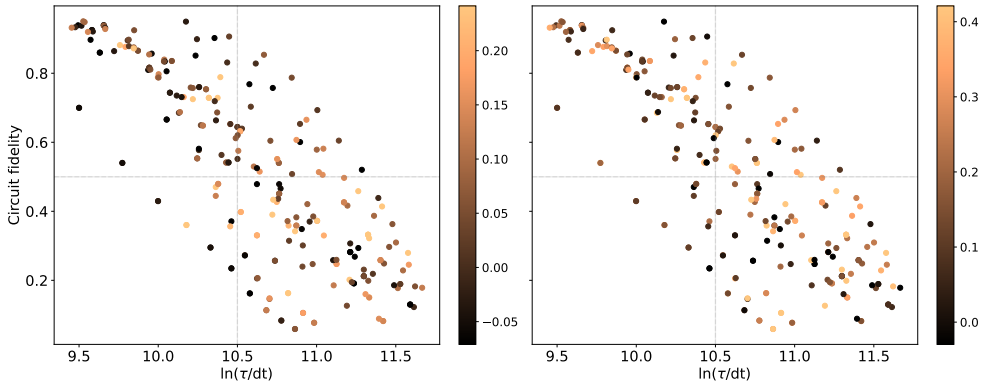


Figure 6. *Cont.*



(**c**) (**d**)

Figure 6. Influence of circuit fidelity and $\ln(\tau/\mathrm{dt})$ on algorithm performance and DD effectiveness: (**a**) $\mathrm{NAR}_{\mathrm{DD}}$, (**b**) $\mathrm{NSP}_{\mathrm{DD}}$, (**c**) Δ_{NAR}, and (**d**) Δ_{NSP}.

3.1.3. Native Gate Sets

This section explores the performance of quantum algorithms implemented on two distinct sets of IBM QPUs. The first set comprises four 27-qubit devices utilizing the CX gate as their native two-qubit gate, while the second set consists of four 127-qubit devices employing the ECR gate as their native two-qubit gate.

Benchmark results obtained from the two QPU sets are presented in Figure 7. Table 4 summarizes average values of metrics and parameters derived from the linear fits of these metrics against the number of qubits. As shown in Figure 7a,b, applying DD sequences generally improves the NAR and NSP, respectively, for both native gate sets. The highest performance is achieved with $\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{ECR}}$ and $\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{ECR}}$, which leverages ECR-based QPUs and incorporates DD sequences. Moreover, QPUs utilizing the ECR gate exhibit consistently higher baseline performance, $\mathrm{NAR}_{\mathrm{B}}^{\mathrm{ECR}}$ and $\mathrm{NSP}_{\mathrm{B}}^{\mathrm{ECR}}$, compared to those with the CX gate, $\mathrm{NAR}_{\mathrm{B}}^{\mathrm{CX}}$ and $\mathrm{NSP}_{\mathrm{B}}^{\mathrm{CX}}$, even surpassing those with DD sequences, $\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{CX}}$, and $\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{CX}}$. This observation suggests that the selection of QPUs may be more critical for achieving optimal performance than relying solely on DD techniques. As shown in Figure 7c,d, DD effectiveness improves as the qubit count increases for both gate sets. Moreover, the CX gate set exhibits higher DD effectiveness than the ECR gate set. As illustrated in Figure 7e,f, the ECR gate produces an overall higher circuit fidelity and lower schedule duration, potentially contributing to higher performance. Analyzing the proportion of positive outcomes in the experimental data presented in Figure 7c,d, we observe that the reported values of $\mathrm{EMSR}_{\mathrm{AR}}$ and $\mathrm{EMSR}_{\mathrm{SP}}$ are 92.5% and 72.5% for the CX gate, respectively, whereas the corresponding values are 75% and 62.5%, respectively, for the ECR gate, suggesting that DD sequences are more robust in mitigating errors for the CX gate set.

The correlation coefficient presented in Table 4 reveals a very strong negative correlation between $\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{ECR}}$ and the number of qubits compared to $\mathrm{NAR}_{\mathrm{B}}^{\mathrm{ECR}}$. Similarly, a very strong negative correlation is observed between circuit fidelity and qubit count for both CX and ECR gate sets, indicating a significant decrease in circuit fidelity as the number of qubits increases. Moreover, we observe a weaker correlation between NSP and qubit number compared to NAR, implying that the impact of qubit count on success probability is less pronounced than its effect on approximation ratio. Additionally, the high p-values for $\Delta_{\mathrm{NAR}}^{\mathrm{ECR}}$ and $\Delta_{\mathrm{NSP}}^{\mathrm{ECR}}$ suggest that the effectiveness of DD sequences for ECR gates is more susceptible to random fluctuations. This can be attributed to the interplay between the intended decoherence suppression capabilities of DD sequences and the additional gate errors that they introduce. As shown in Figure 7e,f, circuits utilizing ECR gates demonstrate higher fidelities while requiring shorter execution times. The inherent advantage of shorter circuits may limit the potential for further enhancement through the use of DD sequences. In such cases, incorporating extra DD pulses could even lead to a decrease in overall algorithm performance.

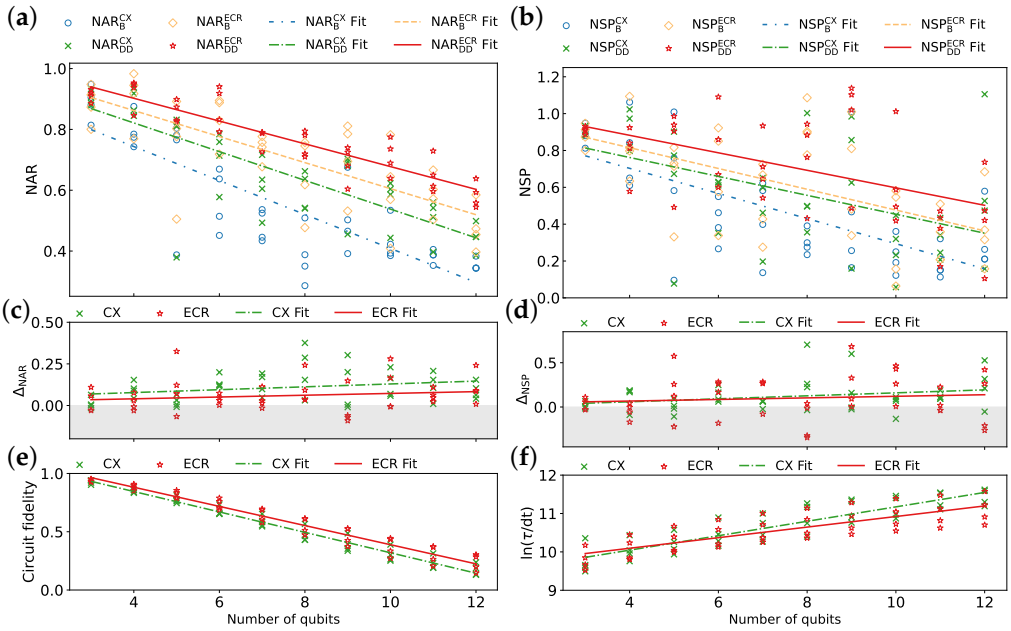


Figure 7. Comparison of two hardware-native gate sets: {CX, ID, RZ, SX, X} and {ECR, ID, RZ, SX, X}, denoted as CX and ECR gate sets, respectively. Results obtained using four 27-qubit quantum processing units (QPUs) ibmq_mumbai, ibmq_kolkata, ibm_cairo, and ibmq_ehningen for the CX gate set, and four 127-qubit QPUs ibm_kyoto, ibm_cusco, ibm_brisbane, and ibm_sherbrooke for the ECR gate set: (**a**) NAR, (**b**) NSP, (**c**) Δ_{NAR}, (**d**) Δ_{NSP}, (**e**) circuit fidelity, and (**f**) $\ln(\tau/\mathrm{dt})$. The CPMG sequence is used for all data points. Each line represents a linear fit to the corresponding data.

Table 4. Parameters derived from the analysis of Figure 7.

Metric	Mean	Fit Function	Correlation Coefficient	*p*-Value
$\mathrm{NAR}_{\mathrm{B}}^{\mathrm{CX}}$	0.548	$y = -0.056x + 0.967$	-0.832	0
$\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{CX}}$	0.656	$y = -0.047x + 1.010$	-0.812	0
$\mathrm{NAR}_{\mathrm{B}}^{\mathrm{ECR}}$	0.712	$y = -0.043x + 1.033$	-0.766	0
$\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{ECR}}$	0.771	$y = -0.037x + 1.052$	-0.911	0
$\mathrm{NSP}_{\mathrm{B}}^{\mathrm{CX}}$	0.464	$y = -0.068x + 0.976$	-0.678	0
$\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{CX}}$	0.582	$y = -0.051x + 0.967$	-0.504	0.00092
$\mathrm{NSP}_{\mathrm{B}}^{\mathrm{ECR}}$	0.618	$y = -0.056x + 1.041$	-0.579	0.00009
$\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{ECR}}$	0.716	$y = -0.047x + 1.072$	-0.529	0.00044
$\Delta_{\mathrm{NAR}}^{\mathrm{CX}}$	0.108	$y = 0.009x + 0.043$	0.27	0.09252
$\Delta_{\mathrm{NAR}}^{\mathrm{ECR}}$	0.059	$y = 0.005x + 0.019$	0.167	0.30429
$\Delta_{\mathrm{NSP}}^{\mathrm{CX}}$	0.118	$y = 0.017x - 0.008$	0.277	0.08407
$\Delta_{\mathrm{NSP}}^{\mathrm{ECR}}$	0.098	$y = 0.009x + 0.031$	0.108	0.50688
Circuit fidelity (CX)	0.539	$y = -0.088x + 1.195$	-0.984	0
Circuit fidelity (ECR)	0.594	$y = -0.082x + 1.211$	-0.975	0
$\ln(\tau/\mathrm{dt})$ (CX)	10.703	$y = 0.188x + 9.294$	0.891	0
$\ln(\tau/\mathrm{dt})$ (ECR)	10.577	$y = 0.138x + 9.543$	0.791	0

Our demonstrations on eight IBM QPUs highlight the importance of circuit fidelity, schedule duration, and DD sequences in optimizing algorithm performance. As circuit fidelity decreases and schedule duration increases, DD sequences become increasingly important for mitigating errors and identifying optimal solutions. Furthermore, the results suggest that ECR-based QPUs offer advantages over CX-based QPUs. This is primarily due to the inherently shorter schedule durations and higher circuit fidelities associated with ECR gates. However, CX-based QPUs benefit more significantly from DD sequences in terms of error mitigation.

3.2. Impact of Algorithmic Factors

This section investigates the influence of algorithmic factors on the algorithm performance and DD effectiveness. We focus on three key aspects: algorithm implementations, DD sequence types, and circuit optimization levels.

3.2.1. Algorithm Implementations

We compare the performance of CX and CZ implementations of the QAOA on four 27-qubit IBM QPUs, as detailed in Section 2.3. The CPMG sequence is consistently utilized throughout this analysis. As shown in Figure 8a,b, CZ implementation with DD sequences achieves the highest average values for both the NAR (NAR^{CZ}_{DD}) and NSP (NSP^{CZ}_{DD}). However, for the NSP at qubit counts exceeding 9, CZ implementation without DD sequences, NSP^{CZ}_{B}, outperforms that with DD sequences, NSP^{CZ}_{DD}, potentially due to the introduction of significant errors by DD sequences themselves. Furthermore, CX implementation exhibits increasing DD effectiveness as the qubit number grows (Figure 8c,d), whereas Δ_{NSP} for CZ implementation exhibits a slight decrease. Additionally, $EMSR_{AR}$ and $EMSR_{SP}$ are consistently higher for CX implementation (92.5% and 80%, respectively) compared to CZ implementation (75% and 57.5%, respectively), suggesting a higher robustness of DD sequences for CX implementation. As depicted in Figure 8e, both CX and CZ implementations exhibit comparable circuit fidelities. For a larger number of qubits, CX implementation even achieves slightly higher fidelities. Moreover, CX implementation demonstrates a consistently shorter schedule duration compared to CZ implementation (Figure 8f). This difference in schedule duration is attributed to the increased number of single-qubit gates required by CZ implementation (details in Figure 3).

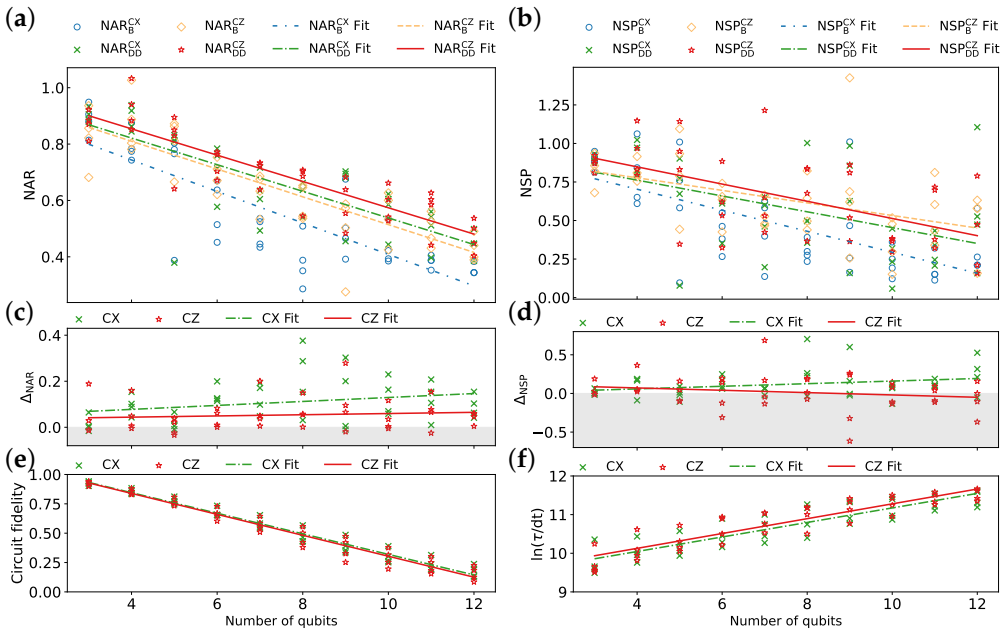


Figure 8. Comparison of CX and CZ implementations of QAOA across four 27-qubit IBM QPUs ibmq_mumbai, ibmq_kolkata, ibm_cairo, and ibmq_ehningen: (**a**) NAR, (**b**) NSP, (**c**) Δ_{NAR}, (**d**) Δ_{NSP}, (**e**) circuit fidelity, and (**f**) $\ln(\tau/dt)$. The CPMG sequence is used for all data points. Each line represents a linear fit of the data.

Table 5 summarizes the average value of each metric along with the linear fit parameters extracted from Figure 8. The negative coefficient associated with Δ^{CZ}_{NSP} suggests a decrease in DD effectiveness, as measured by success probability, with an increasing qubit count for CZ implementation. This behavior can be attributed to the intricate interplay between the optimization landscape and gate errors. As the number of qubits involved increases, the cumulative error introduced by DD sequences becomes more pronounced. This

significantly alters the optimization landscape, rendering the pre-optimized parameters of the QAOA in the noiseless case no longer suitable. Furthermore, correlation coefficients between the NAR (NAR_B and NAR_{DD}) and qubit count reveal that applying DD sequences weakens the correlation for CX implementation while strengthening it for CZ implementation. This trend is also observed for NSP_B and NSP_{DD}. An additional observation is the high p-values associated with Δ^{CZ}_{NAR} and Δ^{CZ}_{NSP}, indicating the potential dominance of random fluctuations in these metrics for CZ implementation.

Table 5. Parameters derived from the analysis of Figure 8.

Metric	Mean	Fit Function	Correlation Coefficient	p-Value
NAR^{CX}_{B}	0.548	$y = -0.056x + 0.967$	-0.832	0
NAR^{CX}_{DD}	0.656	$y = -0.047x + 1.010$	-0.812	0
NAR^{CZ}_{B}	0.638	$y = -0.049x + 1.007$	-0.850	0
NAR^{CZ}_{DD}	0.691	$y = -0.047x + 1.041$	-0.885	0
NSP^{CX}_{B}	0.464	$y = -0.068x + 0.976$	-0.678	0
NSP^{CX}_{DD}	0.582	$y = -0.051x + 0.967$	-0.504	0.00092
NSP^{CZ}_{B}	0.635	$y = -0.041x + 0.940$	-0.473	0.00208
NSP^{CZ}_{DD}	0.653	$y = -0.056x + 1.071$	-0.589	0.00006
Δ^{CX}_{NAR}	0.108	$y = 0.009x + 0.043$	0.27	0.09252
Δ^{CZ}_{NAR}	0.053	$y = 0.003x + 0.034$	0.109	0.50206
Δ^{CX}_{NSP}	0.118	$y = 0.017x - 0.008$	0.277	0.08407
Δ^{CZ}_{NSP}	0.018	$y = -0.015x + 0.132$	-0.202	0.21130
Circuit fidelity (CX)	0.539	$y = -0.088x + 1.195$	-0.984	0
Circuit fidelity (CZ)	0.527	$y = -0.089x + 1.195$	-0.977	0
$\ln(\tau/\mathrm{dt})$ (CX)	10.703	$y = 0.188x + 9.294$	0.891	0
$\ln(\tau/\mathrm{dt})$ (CZ)	10.799	$y = 0.192x + 9.360$	0.901	0

The results suggest that although CX implementation offers more advantages in terms of DD effectiveness, the higher performance of CZ implementation highlights the significance of circuit structure in executing the QAOA. In certain instances, the inherent advantage of a more symmetrical circuit structure, as exhibited by CZ implementation, can outweigh the benefits of strong DD mitigation achieved with CX implementation. However, the optimal selection of gate decomposition ultimately relies on the specific algorithm being implemented, the hardware capabilities available, and the desired balance between overhead caused by DD and potential performance gains.

3.2.2. DD Sequences

This section evaluates the performance of two DD sequences, CPMG and XY4, for mitigating decoherence errors during QAOA execution with CX implementation. The evaluation leverages data from seven IBM QPUs. XY4, which employs four single-qubit pulses, might be more effective for qubits with extended idle times than CPMG, which utilizes two single-qubit pulses. While DD sequences may introduce crosstalk errors, the use of the same transpiled circuits minimizes the impact of this potential crosstalk on our evaluation.

Figure 9a,b show that both CPMG and XY4 contribute to improved algorithm performance. While CPMG and XY4 achieve comparable NAR values, XY4 exhibits a better NSP for a larger number of qubits, but with noticeable fluctuations. CPMG and XY4 demonstrate comparable DD effectiveness for a small number of qubits (Figure 9c,d), with XY4 showing a slight advantage for larger qubit counts. However, CPMG exhibits greater robustness, as evidenced by its higher $EMSR_{AR}$ (84.29%) and $EMSR_{SP}$ (75.71%) compared to XY4's values (67.14% and 64.29%, respectively). Figure 9e,f illustrate comparable circuit fidelity and schedule duration for both CPMG and XY4. As before, the data are fitted with a linear function. The resulting parameters are summarized in Table 6. The coefficients of the linear function suggest that both CPMG and XY4 effectively suppress the decrease in NAR

and NSP as the qubit count increases. The correlation coefficients and p-values suggest a stronger correlation between $\Delta_{\mathrm{NAR}}^{\mathrm{XY4}}$ and qubit count compared to $\Delta_{\mathrm{NAR}}^{\mathrm{CPMG}}$, $\Delta_{\mathrm{NSP}}^{\mathrm{XY4}}$, and $\Delta_{\mathrm{NSP}}^{\mathrm{CPMG}}$.

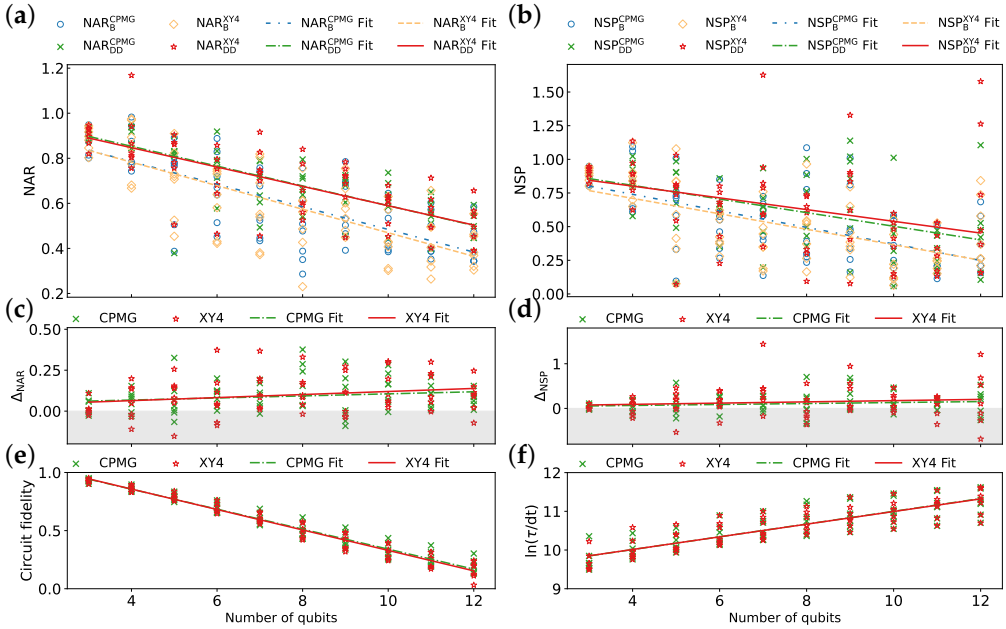


Figure 9. Comparison of CPMG and XY4 sequences across seven IBM QPUs ibmq_mumbai, ibmq_kolkata, ibm_cairo, ibmq_ehningen, ibm_kyoto, ibm_cusco, and ibm_brisbane: (**a**) NAR, (**b**) NSP, (**c**) Δ_{NAR}, (**d**) Δ_{NSP}, (**e**) circuit fidelity, and (**f**) $\ln(\tau/\mathrm{dt})$. Each line represents a linear fit of the data.

Table 6. Parameters derived from the analysis of Figure 9.

Metric	Mean	Fit Function	Correlation Coefficient	p-Value
$\mathrm{NAR}_{\mathrm{B}}^{\mathrm{CPMG}}$	0.610	$y = -0.050x + 0.986$	−0.749	0
$\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{CPMG}}$	0.699	$y = -0.044x + 1.029$	−0.802	0
$\mathrm{NAR}_{\mathrm{B}}^{\mathrm{XY4}}$	0.6	$y = -0.052x + 0.992$	−0.752	0
$\mathrm{NAR}_{\mathrm{DD}}^{\mathrm{XY4}}$	0.697	$y = -0.043x + 1.019$	−0.750	0
$\mathrm{NSP}_{\mathrm{B}}^{\mathrm{CPMG}}$	0.525	$y = -0.061x + 0.986$	−0.613	0
$\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{CPMG}}$	0.629	$y = -0.051x + 1.009$	−0.513	0.00001
$\mathrm{NSP}_{\mathrm{B}}^{\mathrm{XY4}}$	0.509	$y = -0.057x + 0.940$	−0.591	0
$\mathrm{NSP}_{\mathrm{DD}}^{\mathrm{XY4}}$	0.648	$y = -0.044x + 0.975$	−0.373	0.00148
$\Delta_{\mathrm{NAR}}^{\mathrm{CPMG}}$	0.09	$y = 0.006x + 0.042$	0.189	0.11748
$\Delta_{\mathrm{NAR}}^{\mathrm{XY4}}$	0.097	$y = 0.009x + 0.027$	0.23	0.05502
$\Delta_{\mathrm{NSP}}^{\mathrm{CPMG}}$	0.104	$y = 0.011x + 0.023$	0.144	0.23425
$\Delta_{\mathrm{NSP}}^{\mathrm{XY4}}$	0.139	$y = 0.014x + 0.035$	0.116	0.33818
Circuit fidelity (CPMG)	0.555	$y = -0.086x + 1.201$	−0.979	0
Circuit fidelity (XY4)	0.55	$y = -0.088x + 1.209$	−0.981	0
$\ln(\tau/\mathrm{dt})$ (CPMG)	10.589	$y = 0.165x + 9.354$	0.851	0
$\ln(\tau/\mathrm{dt})$ (XY4)	10.586	$y = 0.163x + 9.360$	0.858	0

The results indicate that DD sequences are generally recommended for improving circuit performance. They allow for achieving acceptable results in a wider range of circuits. For instance, the QAOA with DD can reach higher NAR values for more qubits. However, the effectiveness and robustness of DD sequences can vary. While XY4 offers slightly better performance improvements in terms of NAR and NSP, CPMG demonstrates higher robustness as measured by EMSR. This highlights the importance of considering both performance gains and mitigation robustness when choosing a DD sequence.

3.2.3. Optimization Levels

We investigate the influence of optimization levels on the performance and DD effectiveness using five IBM QPUs. Two optimization levels within Qiskit's transpiler are considered: level 1 (Opt1) and level 3 (Opt3), representing the default and highest settings, respectively. It is worth noting that different optimization levels do not affect the number of two-qubit gates in our demonstration. This is because we are considering benchmark circuits that have already undergone the AOQMAP approach [42], which effectively ensures adherence to connectivity constraints and eliminates the need for additional SWAP gates. In our case, different optimization levels influence the selected qubits for circuit execution and the count of single-qubit gates, which affects the circuit fidelity and schedule duration. The CPMG sequence and CX implementation of the QAOA are employed throughout this analysis.

Figure 10a,b demonstrate that Opt3 with DD sequences achieves the highest overall performance in terms of NAR and NSP, followed by Opt1 with DD sequences. Without error mitigation, Opt3 outperforms Opt1 for all tested qubit counts in terms of NAR, whereas, for NSP, Opt3 exhibits an advantage only for a small number of qubits, with comparable performance achieved at larger qubit counts. The average improvement in NAR due to DD (Δ_{NAR}) is generally higher for Opt1 compared to Opt3 (Figure 10c). However, for NSP, DD initially benefits Opt1 more, but this advantage shifts toward Opt3 for larger qubit counts (Figure 10d). Furthermore, the reported average $\mathrm{EMSR}_{\mathrm{AR}}$ and $\mathrm{EMSR}_{\mathrm{SP}}$ are 92% and 74% for Opt1, respectively, compared to 80% and 60% for Opt3, suggesting a higher robustness of DD for Opt1. It is important to note that Opt3 exhibits higher circuit fidelity (Figure 10e) and a shorter schedule duration (Figure 10f), which are crucial for high algorithm performance.

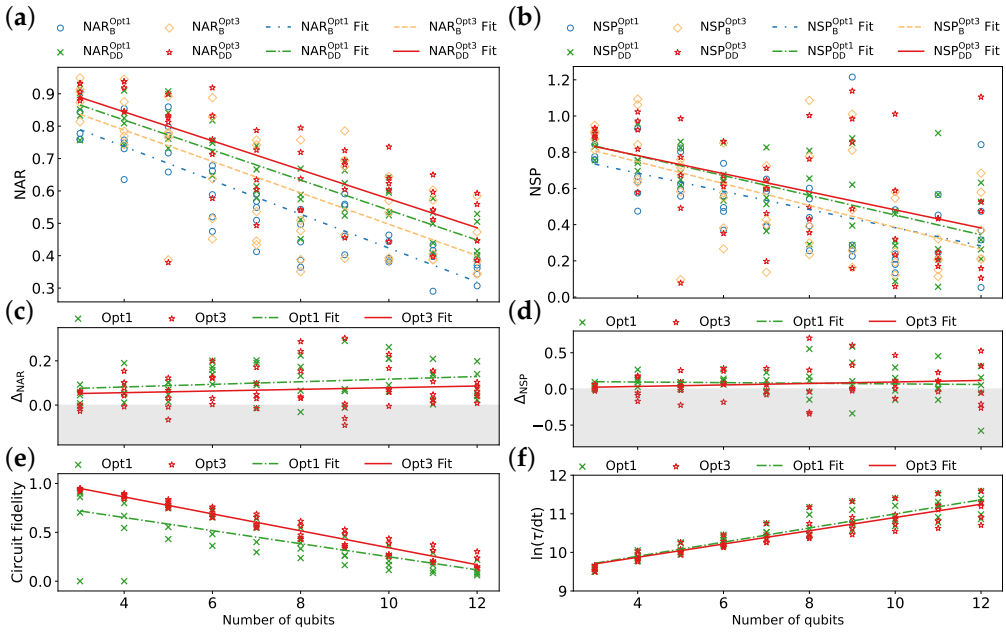


Figure 10. Comparison of optimization level 1 (Opt1) and optimization level 3 (Opt3) across five IBM QPUs ibmq_kolkata, ibm_cairo, ibmq_ehningen, ibm_cusco, and ibm_kyoto: (**a**) NAR, (**b**) NSP, (**c**) Δ_{NAR}, (**d**) Δ_{NSP}, (**e**) circuit fidelity, and (**f**) $\ln(\tau/\mathrm{dt})$. The CPMG sequence is used for all data points. Each line represents a linear fit of the data.

The detailed linear fit parameters for the optimization levels are provided in Table 7. While DD effectively mitigates the decrease in NAR for both Opt1 and Opt3 with increasing qubits, its impact on NSP differs. For Opt3, DD suppresses the decrease in NSP, whereas, for Opt1, it appears to exacerbate the decay. The correlation between NSP and qubit count for Opt1 is very weak (low C_r and high p-value), suggesting minimal influence from qubit count on NSP for this optimization level. In contrast, Opt1 prioritizes schedule duration,

exhibiting a stronger correlation with qubit count, while Opt3 prioritizes circuit fidelity, showing a stronger correlation between fidelity and qubit count.

Table 7. Parameters derived from the analysis of Figure 10.

Metric	Mean	Fit Function	Correlation Coefficient	*p*-Value
NAR_B^{Opt1}	0.554	$y = -0.052x + 0.946$	−0.891	0
NAR_{DD}^{Opt1}	0.657	$y = -0.046x + 1.004$	−0.886	0
NAR_B^{Opt3}	0.618	$y = -0.048 + 0.982$	−0.720	0
NAR_{DD}^{Opt3}	0.688	$y = -0.045x + 1.023$	−0.770	0
NSP_B^{Opt1}	0.509	$y = -0.050x + 0.885$	−0.596	0
NSP_{DD}^{Opt1}	0.589	$y = -0.055x + 0.998$	−0.667	0
NSP_B^{Opt3}	0.536	$y = -0.060x + 0.988$	−0.586	0.00001
NSP_{DD}^{Opt3}	0.606	$y = -0.050x + 0.981$	−0.471	0.00056
Δ_{NAR}^{Opt1}	0.103	$y = 0.006x + 0.058$	0.218	0.12785
Δ_{NAR}^{Opt3}	0.069	$y = 0.004x + 0.041$	0.126	0.38513
Δ_{NSP}^{Opt1}	0.08	$y = -0.004x + 0.113$	−0.065	0.65396
Δ_{NSP}^{Opt3}	0.07	$y = 0.010x - 0.007$	0.136	0.34466
Circuit fidelity (Opt1)	0.417	$y = -0.067x + 0.919$	−0.729	0
Circuit fidelity (Opt3)	0.559	$y = -0.087x + 1.209$	−0.973	0
$\ln(\tau/dt)$ (Opt1)	10.540	$y = 0.183x + 9.168$	0.919	0
$\ln(\tau/dt)$ (Opt3)	10.475	$y = 0.172x + 9.186$	0.901	0

This analysis demonstrates a trade-off between the optimization level and DD effectiveness. While Opt3 offers superior overall performance with DD sequences, Opt1 exhibits higher DD effectiveness. Furthermore, DD sequences become increasingly beneficial for Opt3 at larger qubit counts for finding optimal solutions.

4. Discussion and Conclusions

Our comprehensive study, conducted on eight IBM quantum devices, reveals that the application of dynamical decoupling (DD) sequences can significantly enhance the performance and robustness of algorithms on near-term quantum devices. However, the effectiveness of DD sequences varies depending on hardware and algorithmic factors. A key finding is the observed inverse relationship between DD effectiveness and the original performance of algorithms without error mitigation. This implies that algorithms with higher inherent performance (measured without DD sequences) exhibit lower DD effectiveness. For instance, ECR-based QPUs offer superior native performance but reduced DD effectiveness compared to CX-based QPUs. Similarly, the CZ implementation of a QAOA exhibits higher native algorithm performance but lower average DD effectiveness compared to CX implementation. Moreover, optimization level 3 produces higher algorithm performance, but level 1 exhibits higher DD effectiveness. This inverse behavior can be attributed to the fact that algorithms with high performance typically have a lower intrinsic error rate, including the decoherence errors targeted by DD sequences. Furthermore, the introduction of DD pulse sequences can lead to new gate operation errors that decrease algorithm performance and potentially limit their effectiveness for certain algorithms.

DD sequences are typically more effective for algorithms with lower fidelity and a longer schedule duration, but their impact on approximation ratio and success probability differs. The results indicate that while algorithms with lower circuit fidelity struggle to achieve high approximation ratio values, the application of DD sequences allows for achieving the simulated success probability. This finding suggests a potential methodology for obtaining the desired probabilities by studying different algorithm implementations and DD sequences and selecting the measure that minimizes system energy.

Table 8 summarizes the observed effects of investigated hardware and algorithm factors on the effectiveness and robustness of DD. Without error mitigation, the ECR native gate set achieves the highest average value of normalized approximation ratio (NAR_B),

while the CZ implementation of the QAOA exhibits the highest normalized success probability (NSP_B). However, when applying DD error mitigation, the CX native gate set and CX implementation of the QAOA demonstrate the greatest increase in NAR, while the XY4 sequence leads to the most significant NSP improvement. Additionally, the linear fit slope coefficients suggest that circuit fidelity has a stronger influence on approximation ratio, whereas schedule duration more significantly impacts success probability. Furthermore, as the qubit count increases, the CX gate set, CX implementation, and XY4 sequence benefit more from DD mitigation compared to the ECR gate set, CZ implementation, and CPMG sequence. Notably, the CX implementation exhibits the highest overall robustness for the DD strategy, followed by the CX gate set and circuit optimization level 1 (Opt1).

Table 8. Impact of hardware and algorithm factors on DD effectiveness and robustness.

Factor	Mean				Slope Coefficient		EMSR	
	NAR_B	Δ_{NAR}	NSP_B	Δ_{NSP}	Δ_{NAR}	Δ_{NSP}	$EMSR_{AR}$	$EMSR_{SP}$
Circuit fidelity Schedule duration	0.610	0.077	0.556	0.075	−0.065 0.042	−0.021 0.033	85.55%	66.80%
CX gate set	0.548	0.108	0.464	0.118	0.009	0.017	92.50%	72.50%
ECR gate set	0.712	0.059	0.618	0.098	0.005	0.009	75.00%	62.50%
CX implementation	0.548	0.108	0.464	0.118	0.009	0.017	92.50%	80.00%
CZ implementation	0.638	0.053	0.635	0.018	0.003	−0.015	75.00%	57.50%
CPMG sequence	0.610	0.090	0.525	0.104	0.006	0.011	84.29%	75.71%
XY4 sequence	0.600	0.097	0.509	0.139	0.009	0.014	67.14%	64.29%
Opt1	0.554	0.103	0.509	0.080	0.006	−0.004	92.00%	74.00%
Opt3	0.618	0.069	0.536	0.070	0.004	0.010	80.00%	60.00%

One significant reason for the higher performance of algorithms on ECR-based QPUs is the inherently higher circuit fidelity and shorter schedule duration. However, another potential factor could be the inherent advantages of ECR gates. In these devices, ECR gates are only allowed for one direction, meaning that any two-qubit gate is directly decomposed into ECR gates with the same direction on the qubit pair. While the hardware-native CX gate also has a native direction, the reverse direction is supported, requiring additional single-qubit gates and the hardware-native CX gate for implementation. Directly decomposing algorithms into one-directional ECR gates could be more advantageous than using CX gates with bidirectional capability at the gate level and then transforming them into native CX gates at the hardware pulse level. A similar trend is observed for CZ implementation, which produces a higher algorithm performance than CX implementation. The CX gate is directed, whereas the CZ gate is undirected, allowing for the decomposition of all two-qubit gates with one directed CZ gate on one or more qubit pairs. Utilizing gates in the same direction could lead to a higher symmetry in the circuit, both in terms of single- and two-qubit gates, potentially contributing to error suppression and improved algorithmic performance. This highlights the importance of considering native gate properties at the pulse level and maintaining circuit structure symmetry during algorithm design. Our findings hold broad applicability across various quantum algorithms, including the variational quantum eigensolver (VQE) [52,53]. Prioritizing native gates and maintaining circuit symmetry during VQE and other quantum algorithm executions can enhance performance and mitigate errors across diverse quantum computing platforms.

In conclusion, this study demonstrates the significant impact of several factors on algorithm performance and the effectiveness of error mitigation across eight IBM QPUs. These factors include circuit fidelity, schedule duration, choice of hardware-native gates, algorithm implementations, types of DD sequences, and optimization levels. Despite minimal performance variations between Carr–Purcell–Meiboom–Gill (CPMG) and XY4 sequences, XY4 exhibits a slight advantage in success probability for larger qubit counts. However, CPMG achieves a higher overall error mitigation success rate, suggesting potentially greater robustness. While the results highlight the general enhancement of algorithm performance and robustness through the use of DD sequences, achieving significantly

improved performance relies more critically on factors such as high-quality native gates of QPUs, symmetric algorithm implementation, and effective circuit optimization techniques. Therefore, a holistic approach that considers both hardware characteristics and software optimization strategies is important when designing quantum algorithms to maximize reliability and efficacy. This study underscores the importance of hardware considerations and circuit design in enhancing algorithm performance and robustness using DD sequences. These insights guide the development and optimization of other quantum applications. Future research directions include investigating the interplay between these factors when combining DD sequences with other error mitigation strategies, such as zero-noise extrapolation [54,55]. Additionally, exploring the relationship between circuit symmetry and its effectiveness in suppressing errors could provide valuable insights. Extending this analysis to other quantum algorithms, such as the VQE and protocols for preparing Greenberger–Horne–Zeilinger (GHZ) states, holds promise for revealing the broader applicability of these findings.

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