Porous Silicon for Thin Solar Cell Fabrication

Von der Fakultät Informatik, Elektrotechnik und Informationstechnik
der Universität Stuttgart zur Erlangung der Würde eines
Doktor-Ingenieurs (Dr.-Ing.) genehmigte Abhandlung

Vorgelegt von

Osama Tobail

geboren in Alexandria

Hauptberichter: Prof. Dr. rer. nat. habil. J. H. Werner
Mitberichter: Prof. Dr. H. Föll

Tag der Einreichung: 21.05.2008
Tag der mündlichen Prüfung: 05.12.2008

Institut für Physikalische Elektronik der Universität Stuttgart
2008

Contents

Summary

The thesis on hand considers the preparation and the characterization of porous silicon for the fabrication of monocrystalline silicon thin layers and solar cells. The reduction of the solar cell thickness decreases the material consumption, offers the fabrication of mechanically flexible cells, and enhances the physical properties of solar cells. Therefore, the goal of this work is to fabricate free-standing thin monocrystalline silicon solar cells. The layer transfer process provides an economical production of thin film silicon solar cells with thicknesses d between $d = 20$ and $d = 50$ μm on foreign superstrates. An epoxy resin attaches the solar cell onto a foreign superstrate. The layer transfer process allows the fabrication of 50 μm thin silicon solar cell on glass with an efficiency $\eta = 16.9$ %[1] by means of a complex low temperature back side process and with $\eta = 16.6$ %[2] by means of a full area aluminium back contact. The transfer process requires a double layer porous silicon on a silicon wafer, namely a low porosity upper layer on a buried high porosity layer. During a heat treatment, the upper low porosity layer forms a quasi-monocrystalline silicon layer, which is suitable for high quality epitaxial growth. The buried high porosity layer forms a separation layer, which is mechanically weak and allows the separation of the epitaxy layer from the host wafer. The mechanical properties of the separation layer has to be fine-adjusted to provide a mechanical stability during the device fabrication process but to allow an easy separation of the device from the host wafer as well.

Unfortunately, the layer transfer process has the following drawbacks: i) The glass on top of the solar cells complicates the series connection of cells to build modules, as the front side contact is beneath the glass. ii) The separation layer adjustment is difficult due to the very narrow process window, and hence the process yield is very low. iii) The epoxy resin limits the cell performance due to its high absorption in the low wavelength radiation regime. It also limits the back side processing temperature because its optical properties degrade at high temperatures.

The present thesis approaches the three drawbacks of the transfer process from three

[1]Independently confirmed by ISE CalLab, Germany and presented by Brendle in his PhD thesis [1]

[2]Independently confirmed by ISE CalLab, see Ref. [2]

sides: First, it develops a new technique for the integrated module connection from transfer cells. Second, it enhances the homogeneity of porous silicon and hence the layer transfer process yield by means of a new etching setup for porous silicon formation. Third, it introduces a new technique, which fabricates thin free-standing monocrystalline silicon layers and solar cells.

The first approach develops a new technique of a mini-module connection from transfer cells. The technique uses the laser machining to fabricate an integrated mini-module from cells, which are transferred onto a single glass superstrate. The resulting module shows a silicon utility $U_{\mathrm{Si}} = 0.74$ W/g, which is double the silicon utility of a wafer based high efficiency module.

The second approach enhances the layer transfer process by investigating porous silicon. As the transfer process quality depends mainly on porous silicon structural properties, a non-destructive determination of porosity and layer thickness is necessary. This work presents a new non-destructive method to estimate the porosity of single as well as multi layer porous silicon systems. A comparison between the white-light-interferometry results and and an independent scanning electron microscope measurement of shows deviations lower than 2 %. This thesis applies the new method in two applications: The first application is the study of the dissolution mechanism of silicon in hydrofluoric acid during anodization. The study shows that heavily doped p^+-type wafers consume three holes, while lightly doped p-type wafers consume only two holes during porous silicon formation to dissolve one silicon atom. The number of consumed holes indicates the kind of the electrochemical reaction, by which silicon atoms dissolve during the anodization. The second application is the enhancement of the lateral homogeneity of porous silicon on 6" wafer to increase the yield of the layer transfer process. The measurements agree with the two dimensional conductive medium simulation of the etching cell. The experiment together with the simulation result in a new etching setup for porous silicon production. The new setup enhances the porous silicon lateral homogeneity by about 10 % and also increases the yield Y of the layer transfer process from $Y \approx 30$ % to $Y \geq 70$ %.

The third approach introduces a new technique, which produces free-standing monocrystalline silicon thin-films. This technique uses the selective formation of porous silicon on different doped silicon. Porous silicon forms on p-type regions, while n-type regions on the same wafer act as a masking layer against the electrochemical reaction. Modeling the Si/electrolyte interface shows that n-type doped islands need a higher potential than p-type silicon to flow a certain current, and hence n-type regions act as a mask during porous silicon formation. Laser doping technique enables the simple pattern-

ing of different doped regions without the need of masking or high temperature annealing steps. The optimization of laser power minimizes the under-etching length and the defects in the n-type region. This technique produces patterned buried continuous cavities beneath the epitaxy layer. Each cavity stops at the edges, where the n-type regions exist, and hence, the epitaxy layer is only connected at the n-type doped regions with the host wafer. Separation takes place by cutting the epitaxy layer at the cavity edges. The handling system used at *ipe* allows the further processing of free-standing 50 μm thin solar cells. A free-standing 47.6 μm thin solar cell with efficiency $\eta = 17.0$ %[3] and an area $A = 1.1$ cm^2 is achieved by a simple back side metallization on a back surface field layer. The fabrication of free-standing solar cells eliminates the performance limitation due to the epoxy resin used in the transfer process.

This work deepens the understanding of porous silicon formation mechanisms and offers a new characterization method of its structural properties. A comprehensive study of the well established layer transfer process and its disadvantages leads to a new technique producing free-standing thin monocrystalline silicon layers and solar cells.

[3]Measured at *ipe* under an illumination similar to AM1.5G and presented by M. Reuter [3]

Zusammenfassung

Die vorliegende Arbeit behandelt die Erzeugung und die Charakterisierung von porösem Silizium, um dünne monokristalline Silizium-Schichten und Solarzellen herzustellen. Die Reduzierung der Solarzellendicke spart Material, ermöglicht die Herstellung flexibler Solarzellen und verbessert darüberhinaus die physikalischen Eigenschaften der Solarzelle. Deshalb ist der Hauptziel dieser Dissertation die Herstellung von freistehenden dünnen Silizium-Solarzellen. Der am *ipe* entwickelte Transferprozess bietet eine ökonomische Produktion dünner Solarzellen mit einer Dicke d zwischen $d = 20$ μm und $d = 50$ μm. Dabei haftet die Solarzelle durch ein Epoxidharz am Fremdsuperstrat. Der Transferprozess ermöglicht die Herstellung von 50 μm dünnen Silizium-Solarzellen auf Glas mit einem Wirkungsgrad $\eta = 16.9$ % mittels eines komplizierten Niedertemperatur Rückseiten-Prozesses und $\eta = 16.6$ % mittels eines ganzflächigem Aluminium-Rückseitenkontakts. Der Transferprozess basiert auf einem Zweischichtsystem aus porösem Silizium, welches aus einer niedrigporösen oberen Schicht und einer darunter befindlichen hochporösen Schicht besteht. Durch einen Temperaturbehandlungsschritt bildet sich aus der niedrigporösen Schicht eine quasi-monokristalline Silizium-Schicht, die sich für epitaktisches Aufwachsen einer monokristallinen Silizium-Schicht mit hoher Qualität eignet. Die untere, hochporöse Schicht wandelt sich in eine Trennschicht um, die mechanisch instabil ist und die Trennung der Epitaxieschicht vom Host-Wafer erlaubt. Die mechanischen Eigenschaften der Trennschicht müssen genau abgestimmt werden, um zum einem die mechanische Stabilität während des Herstellungsprozesses aber auch ein leichtes Abtrennen des Bauelementes vom Host-Wafer zu gewährlisten.

Der Transferprozess hat drei Nachteile: i) Das auf der Zelle befestigte Glassuperstrat erschwert die Modulverschaltung, da die Vorderseitenkontakte unter dem Glas verborgen sind. ii) Die Anpassung der Trennschicht ist auf Grund des engen Prozessfenster kompliziert und dadurch ist die Prozessausbeute sehr niedrig. iii) Das Epoxidharz absorbiert stark im langwelligen Wellenlängenbereich und begrenzt dadurch die Leistung der Zelle.

Außerdem begrenzt das Epoxidharz die Prozesstemperatur der Rückseite, da sich seine optischen Eigenschaften bei hohen Temperaturen verschlechtern.

Diese Dissertation tritt diesen Nachteile auf drei Ebenen entgegen: Die erste Ebene entwickelt eine Technik für eine integrierte Serienverschaltung für Transferzellen-Module. Die zweite Ebene verbessert die Homogenität des porösen Siliziums und steigert die Transferprozess-Ausbeute mit Hilfe einer neuen Ätzvorrichtung zur Herstellung von porösem Silizium. Der dritte Ebene stellt ein neues Verfahren zur Herstellung von dünnen freistehenden monokristallinen Silizium-Schichten und Solarzellen vor.

Die erste Ebene einwickelt eine neue Technik zur Minimodul-Verschaltung aus Transfer-Solarzellen. Diese Technik benutzt Laserbearbeitungschritte zur Herstellung eines integrierten Minimodules aus Zellen, die auf ein einzelnes Glassuperstrat übertragen werden. Das dabei enstehende Modul zeigt Siliziumausnutzung U_{Si}, was einer Verdopplung der Siliziumausnutzung von Wafer-basierten Hocheffizienzmodulen entspricht.

Die zweite Ebene verbessert den Transferprozess durch Untersuchungen am porösen Silizium. Da die Qualität des Transferprozesses hauptsächlich von den strukturellen Eigenschaften des porösen Siliziums abhängt, ist eine zerstörungsfreie Bestimmung der Porösität und Schichtdicke notwendig. Diese Arbeit präsentiert eine neue zerstörungsfreie Methode um die Porosität von sowohl einzelner poröser Schichten als auch von mehreren aufeinander liegenden porösen Schichten zu ermitteln. Die Methode misst und wertet die Weißlichtinterferometrie aus, die von porösem Silizium auf Silizium-Wafer reflektiert wird. Das Vergleichen von der Weißlichtinterferometer-Ergebniße mit einer unabhängigen Rasterelektronenmikroskopischen Messungen zeigt Abweichungen kleiner als 2 %. Diese Dissertation setze die entwickelte Methode nach zwei Anwendungen ein: Die erste Anwendung untersucht den Auflösungsmechanismus von Silizium während der Anodisation in Flusssäure. Die Untersuchung zeigt dass während der Ausbildung des porösen Siliziums der hoch dotierte p^+-Typ Wafer drei Defektelektronen (Löcher) und bei einem niedrig dotierten p-Typ Wafer nur zwei Löcher pro gelösten Silizium-Atom verbrauchen. Die Zahl der verbrauchten Löcher kennzeichnet die Art der elektrochemischen Reaktion, mit der sich die Silizium-Atome während der Anodisation auflösen. Die zweite Anwendung benutzt die Porositätsbestimmung-Methode zur Ermittlung der lateralen Homogenität von porösem Silizium auf 6" Wafer. Die Messungen stimmen mit der zweidimmensionalen Simulation der Ätzzelle als leitendes Medium überein. Dieses Experiment führt zum Bau einer neuen Ätzvorrichtung. Die neue Ätzvorrichtung verbessert die laterale Homogenität des porösen Siliziums um 10 %. Außerdem steigt die Ausbeute Y des Transferprozesses mit der neuen Ätzvorrichtung von $Y \approx 30$ % auf $Y \geq 70$ %.

Die dritte Ebene stellt ein neues Verfahren zur Herstellung freistehender monokristalliner Silizium-Dünnschichten vor. Dieses Verfahren nutzt die selektive Ausbildung von porösem Silizium auf unterschiedlich dotierten Silizium. Poröses Silizium bildet sich auf p-Typ Bereichen, während n-Typ Regionen auf dem selben Wafer als Maske gegen die elektrochemische Reaktion agieren. Die Modellierung der Grenzfläche zwischen Silizium und Elektrolyt zeigt dass n-dotierte Inseln eine höhere Spannung als p-dotiertes Silizium benötigt, um eine bestimmte Stromdichte zur Bildung von porösem Silizium fließen zu lassen. Laserdotierung ermöglicht die einfache Strukturierung von unterschiedlich dotierten Regionen ohne eine Maskierung oder Hochtemperatur-Tempern zu benötigen. Die Optimierung der Laserleistung minimiert sowohl das Unterätzen als auch die Defekte in der n-Typ Region. Dieses Verfahren erzeugt strukturierter verborgener durchgängiger Hohlraum unter der Epitaxieschicht. Jeder Hohlraum endet nur an den n-Typ Regionen. Dadurch ist die Epitaxieschicht nur über die n-Typ Bereiche mit dem Host-Wafer verbunden. Die Abtrennung erfolgt durch Herausschneiden der Epitaxieschicht an den Hohlraumkanten. Das am *ipe* benutzte Handhabungssystem ermöglicht eine Weiterprozessierung von freistehenden 50 μm dünnen Solarzellen. Mit einem einfachen Rückseiten-Prozess erreichen die freistehenden 47.6 μm dünne Solarzelle einen Wirkungsgrad $\eta = 17.0$ % und eine Fläche $A = 1.1$ cm^2. Die freistehenden Zellen besitzen nicht mehr die Leistungbegrenzung durch das Epoxidhartz wie im Fall des konventionellen Transferprozesses.

Diese Dissertation vertieft das Verständnis der Ausbildungsmechanismen des porösen Siliziums und bietet eine neue Methode, um die strukturelle Eigenschaften des porösen Siliziums zu bestimmen. Eine umfassende Untersuchung des am *ipe* bestehenden Transferprozesses und seine Nachteile führt zu einem neuen Verfahren zur Herstellung von freistehenden monokristallinen dünnen Silizium-Schichten und Solarzellen.

Chapter 1

Introduction

1.1 Motivation

The reduction of the solar cell thickness, on the one hand, reduces the material consumption and hence enhances the material utility and, on the other hand, offers the fabrication of mechanically flexible cells. For example, a 25 % efficient laboratory wafer based silicon solar cells with a thickness $d = 250$ μm has the same silicon utility $U_{\mathrm{Si}} = 0.43$ W/g as an 18 % efficient industrial wafer based solar cells with a thickness $d = 180$ μm. A 50 μm thin efficient silicon solar cell with an efficiency $\eta = 17$ % enhances the silicon utility $U_{\mathrm{Si}} = 1.46$ W/g by more than three times. In addition, decreasing the solar cell thickness enhances its charge carrier collection efficiency, provided that the recombination rates at surfaces are suppressed or minimized.

Obviously, neither wafer thinning by chemical etching nor the slicing of thinner wafers is suitable to decrease the material use. Therefore, the *ipe* has developed the layer transfer process. It is based on the epitaxial growth of a high quality monocrystalline Si layer on porous silicon after a high temperature annealing step and a subsequent lifting off the epitaxy layer. The transfer process requires a double layer porous silicon on a silicon wafer, namely a low porous upper layer on a high porous buried layer. After the heat treatment, the upper low porosity layer forms a quasi-monocrystalline silicon (QMS) layer, which is suitable for high quality epitaxial growth. The buried high porosity layer forms a separation layer, which is mechanically weak and allows the separation of the epitaxy layer from the host wafer. The structure of the separation layer has to be well adjusted to fulfill two conditions: a) Mechanical stability during the device fabrication and b)

capability to separate the fabricated device from the wafer. Therefore, adjustment of the porous silicon formation parameters is not simple.

In the conventional transfer process, after the fabrication of solar cells on the epitaxy layer, a glass superstrate is attached on the top of the cell by an epoxy resin and the cell is then separated by applying a mechanical force. After transferring the solar cells onto glass substrates, the back side contact has to be formed at low temperature to avoid the change of the optical properties of the epoxy resin.

Unfortunately, the layer transfer process has some drawbacks:

1. The separation layer has to be adjusted to fulfil two conditions:
   i) It has to be mechanically stable enough to fix the epitaxy layer during device processing.
   ii) At the same time, it has to be mechanically weak to allow the separation of cells after fabrication.
   Hence, the process window is very narrow and requires long experimental optimization. Therefore, the layer transfer process has a low yield $Y \approx 30$ %.

2. The glass on top of the solar cells complicates the series connection of cells to build modules, as the front side contact is beneath the glass.

3. The epoxy resin limits the cell performance due to its high absorption in the blue light regime.

4. The epoxy limits also the back side processing temperature $T \leq 220$ °C, because its optical properties degrade at higher temperatures.

The transfer process allowed the fabrication of 16.9 % efficient 50 μm thin silicon solar cell on glass with a low temperature complex back side process [1].

1.2 Objectives

The first aim of the present work is to quantify the evaluation of the transfer process. As the transfer process reproducibility mainly depends on the porous silicon properties, a non-destructive quantitative characterization of porous silicon is necessary. The evaluation of the local porosity and the thickness of porous silicon allows the estimation of the lateral homogeneity of formed porous silicon and hence its effect on the transfer process quality.

The second aim is to overcome the difficulty of module connection of transfer cells. This work presents a new method to connect transfer cells into integrated mini-modules. The method uses laser machining to electrically isolate cells after transferring them onto one glass substrate. In addition, the laser drills holes to reach the front contacts from the back side and then to connect cells in series. The resulting module shows a silicon utility $U_{\mathrm{Si}} = 0.74$ W/g, twice that of a wafer based high efficiency module.

The third aim of this thesis is to develop a new method, which fabricates free-standing silicon thin-films to avoid the epoxy resin drawbacks. The method is based on the local formation of a cavity beneath the silicon thin film. Local formation of buried cavities requires local formation of porous silicon. Therefore, the study of the electrochemical selectivity and the doping dependent anodization is a main part of this work.

The present work results in the fabrication of a free-standing solar cell with a silicon utility $U_{\mathrm{Si}} = 1.46$ W/g. The handling system used at *ipe* enables processing of free-standing 50 μm thin solar cells. A free-standing 47.6 μm thin solar cells with efficiency $\eta = 17.0$ % is achieved by a simple back side metallization on a back surface field layer. The free-standing cells avoid the performance limitation due to the epoxy resin used in the transfer process.

1.3 Structure

In order to approach the goals defined above, this thesis is structured in the following way:

Chapter 2 describes the basic properties of porous silicon. In particular, it introduces the basics and the formation conditions of porous silicon. It review the basic electrochemistry properties of silicon in hydrofluoric acid (HF), porous silicon samples used in this thesis are prepared by electrochemical etching of silicon in HF. In addition, this chapter addresses the basics of solar cells. First, it describes the theory of operation of solar cells, then the characterization methods. Second, it reviews the two solar cell characterization methods, which are used in this thesis. These methods are the quantum efficiency and the current/voltage data analysis.

Chapter 3 gives a overview on porous silicon technology at *ipe* and its applications. The *ipe* fabricates porous silicon for several purposes. The most important one is for the fabrication of thin silicon solar cells by the layer transfer process. In addition, porous silicon is the base of other research fields at *ipe* such as photoluminescence and germanium on porous silicon (GOPS). This chapter has two important conclusions: (i) It is necessary

to be able to form porous silicon on lightly doped wafers for photoluminescence, as the double-champer etching setup at *ipe* is suitable only for anodizing only heavily doped wafers for the transfer process. (ii) Free-standing silicon thin-film solar cells overcome the present drawbacks of the conventional layer transfer process.

Chapter 4 focusses on the optical characterization of porous silicon. A new non-destructive method evaluates the porosity and layer thickness of single- as well as multiple-layer porous silicon systems. The method is based on white light interferometry of thin porous silicon layers on a silicon substrate. This chapter evaluates also the number of holes consumed to dissolve one silicon atom during porous silicon formation. This number is termed as the dissolution valence n_{dv}. The dissolution valence $n_{\mathrm{dv}} = 3$ of heavily doped wafers is larger than $n_{\mathrm{dv}} = 2$ of lightly doped wafers. The values $n_{\mathrm{dv}} > 2$ stems from a total electrochemical reaction, in which the hydrogen evolution rate is not equivalent to the silicon atom dissolution rate.

Chapter 5 uses the method developed in chapter 4, which determines the porosity of multiple porous silicon systems, to evaluate the homogeneity of porous silicon on 6" wafers. The experimentally determined homogeneity profiles agree with those, which are calculated from the two dimensional conductive medium simulation of the etching setup. A new setup during the electrochemical etching enhances the lateral homogeneity by about 10 % and increases also the yield Y of the layer transfer process from $Y \approx 30$ % to $Y \geq 70$ %.

Chapter 6 experimentally and theoretically studies the effect of the substrate doping on the electrochemical reaction. It describes the behavior of both the front and back side of the wafer when immersed in HF under bias by modeling the Si/HF interface as a Schottky junction. Finally, It explains the electrochemical reaction selectivity. The higher selectivity means that lower voltage is required to flow a certain current density across Si/HF interface. In the case of p-type silicon, the surface potential controls the flow of holes. Therefore, p-type silicon has a higher selectivity than p^+-type silicon, because the surface potential at a p-type Si/HF is lower than the surface potential at a p^+-type Si/HF interface. In contrast, in the case of n-type doped islands on the surface of a p-type wafer, the pn-junction potential controls the hole flow and not the surface potential. Therefore, p-type region has a higher selectivity in the dark than n-type doped regions. The model explains the experimental results of the recorded current density and voltage during electrochemically etching samples with different doping concentrations.

Chapter 7 introduces a new technique, which produces free-standing silicon thin-films. The technique forms porous silicon selectively on p-type doped wafer, while n-type regions

act as a mask against the electrochemical reaction. Laser doping serves to form the etch stop n-type doped regions, enabling a simple patterning of doped regions without the need of lithographical masking or annealing steps. Optimization of the laser power minimizes the under-etching length and the defects in the n-type doped region. This chapter describes the handling techniques used at *ipe* which allow the processing of free-standing 50 μm thin solar cells.

Chapter 8, finally, presents the results of the prepared thin-film silicon solar cells and modules. A new method of mini-module connection allows the fabrication of an 8.1 % efficient module. The method uses laser machining to fabricate integrated mini-modules from cells, which are transferred onto a single glass substrate. The resulting module shows a silicon utility $U_{\mathrm{Si}} = 0.74$ W/g that doubles the value U_{Si} of a wafer based high efficiency module. This chapter presents also a free-standing 47.6 μm thin solar cells with an efficiency $\eta = 17.0$ %. This efficiency is slightly higher than the best transfer cell with a complicated back side processing, in which the QMS is removed by chemical etching and the back side is passivated by a-Si:H [1].

Chapter 2

Fundamentals

The present chapter addresses the most important fundamentals of porous Si as well as a solar cell. The first part of the chapter gives a historical outline of porous Si since its discovery in 1956 till latest investigations on porous Si and its properties. Porous Si forms by electrochemically etching a Si wafer in HF containing electrolyte. Therefore, I start with a review of the electrochemistry basics of semiconductors, which are necessary to understand the current flow mechanisms. This chapter discusses also the dissolution reactions, formation models, and the influence of the formation condition on the morphology and finally basic properties of porous Si.

The second part of this chapter briefly reviews the fundamentals of solar cells. First, it introduces the theory of operation of solar cells. Then, it gives a an overview of solar cell characterization methods applied in this thesis, namely the characterization of the current density/voltage curve and the quantum efficiency data.

2.1 Porous Silicon

Porous Si is not a new material, but it is only recently under investigation due to its surprising properties. The formation of porous Si was first reported in 1956 by Uhlir [4] at Bell Labs in USA during studies on electropolishing of Si in HF-based solutions. It was reported that a matte black, brown or red deposit is observed sometimes during the electropolishing of Si. One year after the observation of Uhlir [4], Fuller and Ditzenberger [5] reported about similar films chemically deposits on Si during immersing Si in HF-HNO_3 solution. In 1958, Turner [6] studied for the first time electrochemically prepared porous Si, which he termed as anodized porous Si layer. Chemically prepared films were studied by Archer [7] in 1960. These films were not recognized as porous Si until Watanabe *et al*, [8, 9] first reported their porous nature and the fast oxidation of thick porous Si films [10–12].

In the 1970, the porous Si was utilized for dielectric trench isolation of active Si devices [13–15]. The interest in porous Si has dramatically increased after the proposal of Canham [16] in 1990, that efficient visible light emission from high porosity structures arises from quantum confinement effects. The main advantage of porous Si light emitting diode (LED) is that it promises the integration of optoelectronics into the Si microchips [10]. Lehman and Goesele [17] reported in 1991 that porous Si exhibit a band gap increase compared with bulk Si. The band gap increase explains the observed visible luminescence from porous Si [18].

This work limits itself to electrochemically prepared porous Si and its properties. The formation process has intricate dependence on many factors such as HF concentration [19–24], doping type and doping concentration [11, 23, 25–31] of the Si wafer, etching current density [23, 32–35], and illumination intensity [36]. The rest of this chapter reviews the basic terms of porous Si and its formation. It addresses also the origin of the typical current/voltage characteristic of Si anodization in terms of electrochemistry. Also, the present models of porous Si formation are introduced. Finally, the optical properties of porous Si are reviewed.

2.1.1 Basics

Anodization of monocrystalline Si wafer in an aqueous HF solution as an electrolyte results in the formation of porous Si layers. Therefore, porous Si is monocrystalline Si, which contains pores with an average diameter d_{p}. The morphology of porous Si depends on the spatial distribution of silicon. Porous Si has an extremely rich morphological structure, which is characterized by many aspects. The most important aspects are the pore shape and size, the pore orientation, the shape of pores' bottom, and their branching [11]. Porous Si is roughly classified by the pore size d_{p} into micro- meso- and macropores [37]. Table 2.1 lists the ranges of the pore size of each class, according to the classification of the International Union of Pure and Applied Chemistry (IUPAC) [37].

Table 2.1: *Classification of porous Si by the structure size.*

Type of porous Si	pore size d_{p} [nm]
Microporous silicon	$d_{\mathrm{p}} \leq 2$
Mesoporous silicon	$2 < d_{\mathrm{p}} \leq 50$
Macroporous silicon	$d_{\mathrm{p}} > 50$

To form porous Si, the Si wafer is mounted in an etching cell in a way that at least one side has a contact with HF. A current flowing across the surface of the wafer into the electrolyte leads to the electrochemical dissolution of Si. The current preferentially flows at positions on the wafer surface, which have defects [11], due to the local increase of the electric field strength [35]. Hence, the dissolution takes place at any perturbation of the wafer surface until tips or cavities become marked enough to trap charge carriers [38].

The dissolution reaction between Si and species in the electrolyte requires holes as charge carriers [11, 12]. The required number of holes to dissolve one Si atom is termed as the dissolution valence n_{dv} of the reaction [39]. The dissolution valence n_{dv} has a value between $n_{\mathrm{dv}} = 2$ and $n_{\mathrm{dv}} = 4$ [11, 12, 36, 40]. Evolution of hydrogen gas is observed during porous Si formation, but not during electrochemical polishing [41]. Hydrogen evolution corresponds to a dissolution valence $n_{\mathrm{dv}} = 2$ [17, 39].

All pores in the bulk material inhibit a Si/ambient interface, thus one of the main structural characteristics of porous Si is its huge surface-to-volume ratio, which can be as high as 230 $\mathrm{m}^2/\mathrm{cm}^3$ [42, 43]. Directly after etching, hydrogen terminates the dangling bonds on this huge surface [17]. The hydrogen termination may change due to further processing or after a certain time causing a degradation of the porous Si properties. Therefore, low temperature passivation of porous Si [44] is an interesting point, where high temperature processes change the structure of porous Si [45].

The ratio of the dissolved pore volume V_{p} and the macroscopic volume of the whole layer V_{g} defines the porosity

$$p = \frac{V_{\mathrm{p}}}{V_{\mathrm{g}}}. \tag{2.1}$$

The conventional porosity determination method [23, 42] calculates the porosity

$$p = \frac{m_1 - m_2}{m_1 - m_3} \tag{2.2}$$

from the mass m_1 of the wafer before anodic etching, the mass m_2 after anodization, and the mass m_3 after removal of the porous layer by NaOH or KOH.

Tanaka *et al.* developed a nondestructive method which determines the porosity from the hydrogen gas evolved at the cathode during the electrochemical etching [26]. The method assumes implicitly that all silicon atoms are dissolved in a process which generate hydrogen. Calculations based on the assumption that all Si atoms dissolve with evolution of hydrogen [26] result in a dissolution valence $n_{\mathrm{dv}} = 2$ to $n_{\mathrm{dv}} = 2.67$ for formation of stable porous Si. However, porous Si formation was also observed at dissolution valences in the range $2 \leq n_{\mathrm{dv}} < 4$ [11, 12, 46]. Therefore, it is necessary to understand the

details of the dissolution reactions leading to porous Si formation, which is based of the electrochemistry of Si.

2.1.2 Electrochemistry

This chapter describes the basic aspects of semiconductor electrochemistry [11, 12, 47–51], which provide the base for understanding the Si/HF electrochemical interaction. The analogy between electrolyte energy levels [11] and semiconductor energy levels [52] simplifies the modeling of the interface between them in the form of energy band diagram.

Similar to the Fermi level E_{F} in semiconductors, the energy levels of electrons in electrolytes associated with ions are characterized by the redox potential E_{redox}. The redox potential E_{redox} describes the tendency of the species in the electrolyte to give up or accept electrons and is considered as the effective Fermi level of the solution.

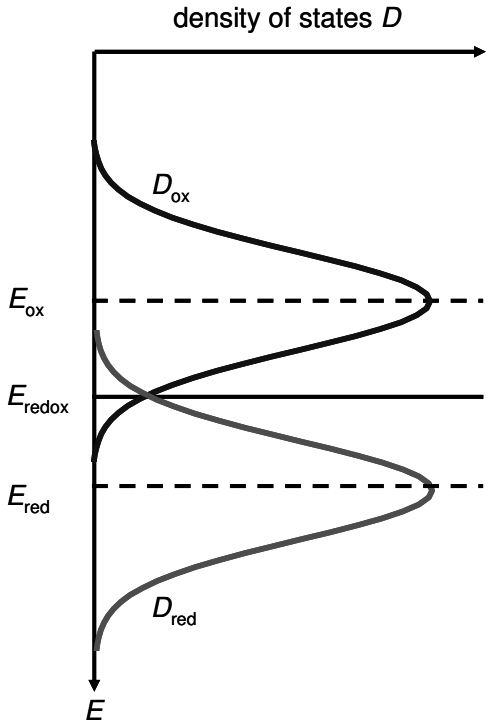

Figure 2.1: *The different energy levels and the density of states in the electrolyte. The redox potential E_{redox} = (E_{ox} + E_{red})/2 is the mathematical mean of the energy levels E_{ox} of the oxidized species and E_{red} of reduced species. D_{ox} describes the density of empty states and D_{red} describes the density of occupied states.*

Figure 2.1 illustrates the different energy levels and the density of states in the electrolyte. The redox potential E_{redox} is the mathematical mean of the energy level of the

oxidized species E_{ox} and that of the reduced species E_{red}. The density of empty states

$$D_{\mathrm{ox}} = D^0_{\mathrm{ox}} \exp\left[-\frac{(E - E_{\mathrm{ox}})^2}{2(E_{\mathrm{ox}} - E_{\mathrm{red}})}\right] \tag{2.3}$$

has a Gaussian distribution around the energy level of the oxidized species E_{ox} and the density of occupied states

$$D_{\mathrm{red}} = D^0_{\mathrm{red}} \exp\left[-\frac{(E - E_{\mathrm{red}})^2}{2(E_{\mathrm{ox}} - E_{\mathrm{red}})}\right] \tag{2.4}$$

has also a Gaussian distribution around the energy level of the reduced species E_{red}, where D^0_{ox} and D^0_{red} are normalization factors [11].

When a semiconductor is brought in contact with an electrolyte, thermodynamic equilibrium requires that $E_{\mathrm{F}} = E_{\mathrm{redox}}$ holds at the interface. This equilibrium is attained by charge transfer across the interface. In the case of an n-type semiconductor, electrons flow from the semiconductor to the electrolyte. In the case of a p-type semiconductor, the equilibrium requires the transfer of electrons from the electrolyte to the semiconductor.

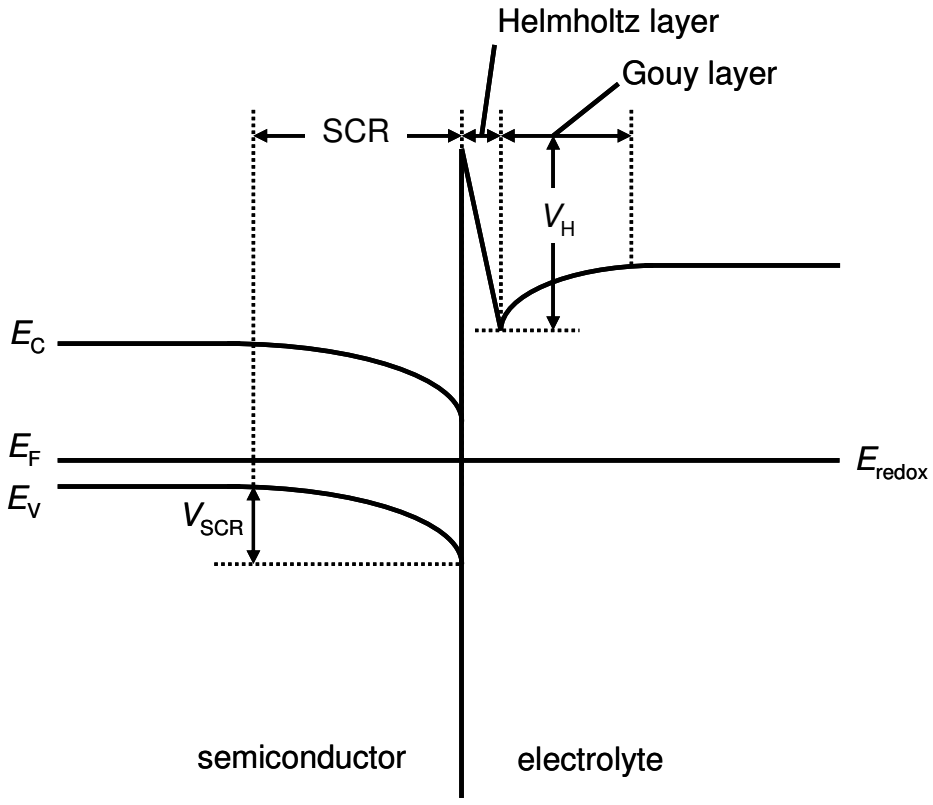

Figure 2.2: *The three charged layers in the interface between the semiconductor and the electrolyte.*

Figure 2.2 describes the three charged layers in the interface between the semiconductor and the electrolyte. The semiconductor band bending results in the formation

of the space charge region (SCR) in the semiconductor side. On the electrolyte side of the interface, an ionic layer called the Helmholtz layer forms. The Helmholtz layer has a typical thickness $d_{\mathrm{H}} \approx 3$ Å. A diffused ionic layer, called Gouy layer, forms deeper in the solution and extends up to 300 Å. In highly concentrated solutions, the contribution of the Gouy layer to the potential drop is negligible and only the space charge layer and the Helmholtz layer are considered [11]. However, some groups showed that the voltage drop across the Helmholtz layer can be also neglected with respect to the semiconductor surface potential [11, 33, 53].

Electrochemical reactions at a semiconductor electrode involve charge transfer between the species in the solution and charge carriers in the semiconductor. Gerischer [54] assumed in his theory that charge carrier transfer in an electrochemical reaction is most probable when the energy levels of the initial and final states of the system coincide. The anodic current is defined as the electron transfer from the molecules of the electrolyte to the electrode, while the cathodic current involves an electron transfer from the electrode to the electrolyte [11, 54].

Figure 2.3 depicts the anodic and the cathodic currents via the conduction and valence bands. The magnitude of the currents depends on the overlap between the levels in the semiconductor bands and those in the electrolyte. As the anodic current involves an electron transfer from the electrolyte to the semiconductor, it depends mainly on the density D_{red} of occupied states in the electrolytes. Moreover, it depends on the empty states in the semiconductor. On the one hand, the empty states in the conduction band are expressed as the effective density of states N_{C} in the conduction band. The conduction band component of the anodic current $I_{\mathrm{a,c}}$ is bias independent, as N_{C} is constant. On the other hand, electron transfer from the electrolyte to the valence band of the semiconductor takes place only if holes are present at the semiconductor surface. This means the density of empty states is equal to the surface hole density p_{s}, which depends on the band bending at the surface and hence on the doping concentration as well as on the bias voltage. Therefore, the valence band component of the anodic current $I_{\mathrm{a,v}}$ is doping and bias dependent [11].

In the case of the cathodic current, electrons transfer form the semiconductor to the empty states in the electrolyte, which have a density of D_{ox}. The conduction band component of the cathodic current $I_{\mathrm{c,c}}$ requires electrons on the surface and hence depends on the electron surface concentration n_{s}. The valence band component of the cathodic current $I_{\mathrm{c,v}}$ depends on the effective density of states N_{V} in the valence band [11]. The

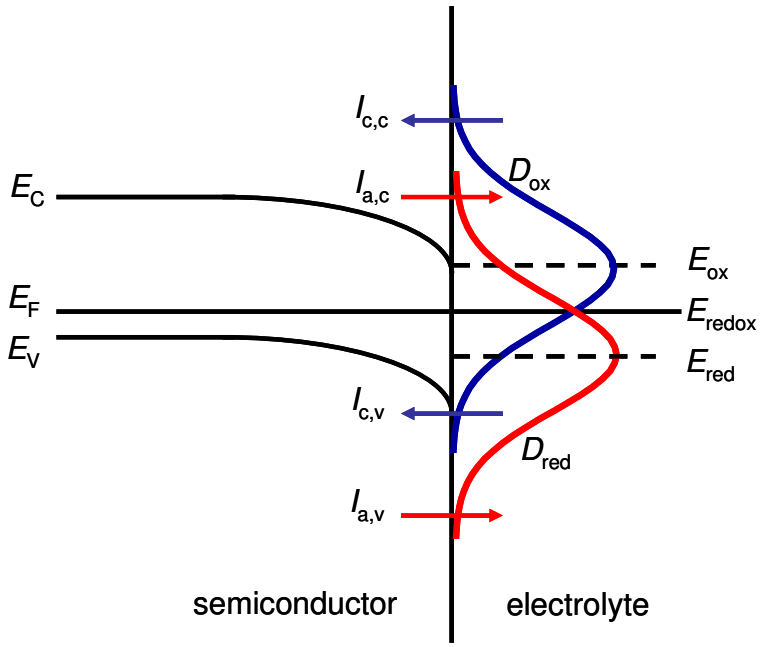

Figure 2.3: *Anodic and the cathodic currents via the conduction and valence band. The magnitude of the currents depends on the overlap between the levels in the semiconductor bands and those in the electrolyte. The anodic current consists of two current components: $I_{a,c}$ due to electron transfer from the electrolyte to the semiconductor via the conduction band and $I_{a,v}$ due to electron transfer from the electrolyte to the semiconductor via the valence band. The cathodic current also consists of two current components: $I_{c,c}$ due to electron transfer from the semiconductor to the electrolyte via the conduction band, and $I_{c,v}$ due to electron transfer from the semiconductor to the electrolyte via the valence band. The arrows represent the conventional current flow direction, i.e. electrons flow in the reverse directions of arrows.*

net current is written as

$$I = I_o \left[\exp\left(\frac{qV}{kT}\right) - 1 \right]. \tag{2.5}$$

This form resembles that for the Schottky contact [52] at a metal/semiconductor interface, which is used in literature [11, 28, 31, 34].

2.1.3 Dissolution reaction

Si atoms dissolve electrochemically in HF by two possible reaction paths [2, 11, 12, 29, 55]. The first path assumes a direct dissolution of Si atoms, whereas the second path assumes an electrochemical oxidation of the Si surface followed by the chemical dissolution of the silicon oxide due to the HF. Both reaction schemes end with the formation of the hexafluor complex (H_2SiF_6), but differ by the amount of evolved hydrogen and consumed holes.

The direct reaction

$$\mathrm{Si}+2\mathrm{F}^{-}+4\mathrm{HF}+2\mathrm{h}^{+} \rightarrow \mathrm{H_2SiF_6} + \mathrm{H_2} \uparrow \tag{2.6}$$

is called also the divalent reaction, while two holes h^{+} are consumed to dissolve one Si atom. The divalent reaction dominates at low potentials and evolves one hydrogen molecule for each dissolved Si atom [29, 35].

The indirect reaction takes place in two steps. The first step

$$\mathrm{Si}+4\mathrm{OH}^{-} + 4\mathrm{h}^{+} \rightarrow \mathrm{SiO_2}+2\mathrm{H_2O} \tag{2.7}$$

is an anodic oxidation of the surface followed by a chemical dissolution of the $\mathrm{SiO_2}$ by HF

$$\mathrm{SiO_2}+6\mathrm{HF} \rightarrow \mathrm{H_2SiF_6}+2\mathrm{H_2O}. \tag{2.8}$$

The net indirect reaction

$$\mathrm{Si}+4\mathrm{OH}^{-}+6\mathrm{HF}+4\mathrm{h}^{+} \rightarrow \mathrm{H_2SiF_6}+4\mathrm{H_2O} \tag{2.9}$$

is a tetravalent reaction and does not evolve hydrogen. It takes place at high potentials and is responsible for electrochemical polishing [12, 29].

2.1.4 Formation models

Many theories on the porous Si formation have emerged since its discovery in the late of 1950s up till present. This section presents the most famous models, which describe the porous Si formation.

Depletion layer and field intensification model

In 1984, Beale and coworkers presented the first model to explain the porous Si formation [21, 22, 56]. Because the spacing between the pores is always less than the space charge region width L_{scr}, which is formed at the Si/HF interface, they proposed that the material in porous Si is depleted of carriers during anodization. The depletion region is responsible for current localization at the pore tips, where the field is intensified. The field intensification is attributed to the large curvature at the pore tips. Hence, the current flows only at the pore tips and not across the pore walls.

For lightly doped p-type Si, the hole transfer from the bulk of Si to the Si/electrolyte interface is described by thermionic emission. The small radius of curvature at the pore tips reduces the Schottky barrier height and thus increases the current density at the

pore tips. For heavily doped materials, the current flows by tunneling, which depends on the barrier width L_{scr}. The large curvature at the pore tips reduces the barrier width L_{scr} and hence increases the current density. The initiation of porous Si formation was considered to be associated with the surface inhomogeneities, which provides the initial localized high current density at the small surface depressions.

The model provides a deeper understanding level of the current localization required for porous Si formation on different Si substrates and explains the correlation between the relative pore dimensions and the space charge region. However, the model is not able to explain the formation of micropores that evolve on the walls of the macropores in n-type Si.

Carrier diffusion model

Near the end of the 1980s, Smith *et al.* [57, 58] proposed a computer simulation model based on the diffusion of holes in the semiconductor. They assumed that the pore structure is determined by the intrinsic nature of the random walk of holes from the semiconductor bulk toward the growing pore tips. The model explains the dependence of pore density, diameter, shape and layer porosity as well as the transition from porous Si formation to the electropolishing on the etching parameters.

Although the Carrier diffusion model simulated some morphological features of porous Si, it was too general to account for the different current conduction mechanisms for different types of Si substrates. For example, for n-type Si in the dark, the current flows by electron injection into the conduction band from the surface, which cannot be explained by the carrier diffusion model. Furthermore, the Carrier diffusion model did not consider the nature of the electrochemical reaction at the interface between Si and electrolyte.

Quantum confinement model

In the early of the 1990s, Lehman and Goesele [17] postulated quantum confinement in the small crystallites of porous Si to be responsible for the formation of micropores in heavily doped p-type Si. The quantum confinement occurs due to an increase in the band gap caused by the quantum size porous structure. The quantum confinement prevents the charge carriers from entering the wall region of porous Si, and hence only the pore tips dissolve [12].

Frohnhoff *et al.* [59] extended the quantum confinement model to account for the wide distribution of pore diameters of porous Si formed on p-type Si. The model has been also adopted by many groups to explain observed luminescence from porous Si [60–62]. The

model successfully explains the formation of crystallites of a few nanometer. However, it does not provide an explanation of what determines the pore size.

Current burst model

In the late 1990s, Föll *et al.* [63–67] introduced the current burst theory. The basic hypothesis is that electrochemical reactions involved in dissolution of Si surface operate in microscopic units. These reaction units have a temporal and a spatial distribution in number and in the state of activity. The formation of pores is due to the synchronization of these operation units at a certain time and geometrical scales. The unit on any position can be silent or burst into action resulting in an increase in current density. The model assumes that the system has the following features:

1. Current flow is always spatially and temporally inhomogeneous; it occurs by local current bursts.

2. Current flow induces either direct dissolution according to reaction Eq. (2.6) or indirect dissolution as in the reaction Eq. (2.9), which consists of oxide formation according to Eq. (2.7) and chemical dissolution of the oxide by HF according to Eq.(2.8).

3. The Fermi level E_{F} is pinned in the midband gap due to the surface states. The surface tends to be terminated by hydrogen resulting in the passivation of the surface states and unpinning of the Fermi level E_{F}. As a result of hydrogen termination and de-termination, the position of the Fermi level E_{F} and thus the width of the space charge region L_{scr} oscillate with time.

4. Because the hydrogen termination process takes a considerable amount of time, it is an important element contributing to the oscillation process.

5. The rate of hydrogen termination varies with crystal orientation, is fastest on the (111) surface, and thus determines the probability of current burst on surfaces of different orientation.

Figure 2.4 illustrates a cycle of the process involving a direct dissolution, oxide formation and dissolution, hydrogen termination, and a nucleation for a reaction unit on a certain microscopic position in a growing pore tip [64]. The amount of the consumed charge of an oxidizing reaction is larger than that of a direct dissolution reaction, because the oxidizing reaction Eq. (2.7) is tetravalent where the direct dissolution reaction Eq.

(2.6) is divalent. The dissolution of the oxide is due to a chemical reaction as shown in Eq. (2.8), therefore it does not consume charge. Also the hydrogen termination and nucleation does not consume charge.

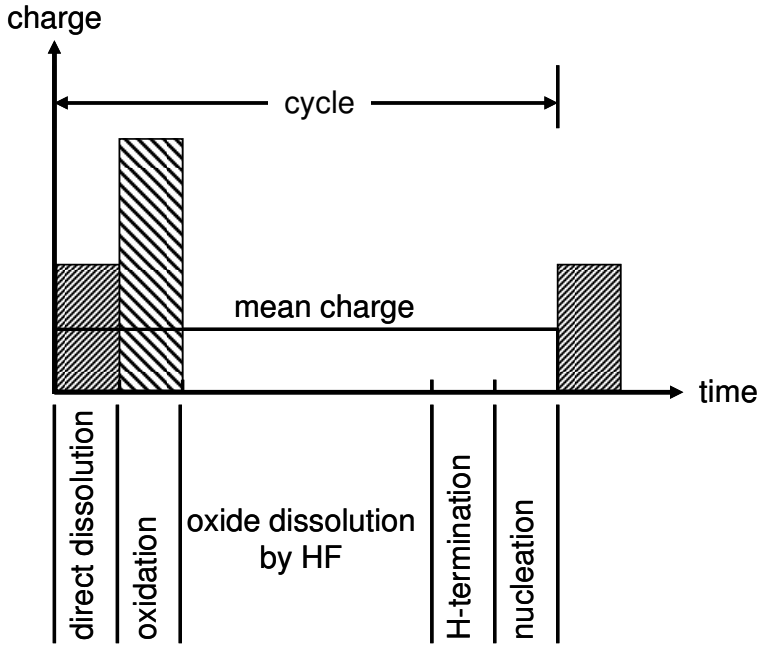

Figure 2.4: *The charge temporal distribution on a certain microscopic position in a growing pore tip. A cycle involves a direct dissolution, oxide formation and dissolution, hydrogen termination, and a nucleation. The amount of the consumed charge of an oxidizing reaction is larger than that of a direct dissolution reaction, where the hydrogen termination and the nucleation do not consume charge.*

The current burst model provides a coherent explanation of the different porous Si morphologies and their dependence on substrate doping, crystal orientation, and etching conditions. Etching conditions are the etching current density and the HF concentration. The following section describes the influence of the formation conditions on the morphology of the fabricated porous Si.

2.1.5 Influence of formation conditions

This section discusses the effect of the substrate doping, the HF concentration, and the etching current density on the porosity of the etched porous Si. The discussion is based on the presented models especially on the current burst model, which considers all formation conditions and the electrochemical reactions under these conditions.

Substrate doping

The interpore spacing d_{ips} and the pore diameter d_{p} are expected to be in the same order as the space charge region width L_{scr} [68]. The space charge region L_{scr} in the semiconductor decreases by increasing the doping concentration of the Si substrate, and vice versa. For heavily doped wafers, the small space charge region results in a small pore size. When all other conditions are unchanged, a constant dissolution rate results in a low porosity. For lightly doped wafers, the space charge region width is large. Hence, the resulted pore size and porosity are high. Therefore, the porosity is inverse proportional to the doping density.

HF concentration

SiO_2 results from the indirect dissolution reaction in Eq. (2.9). A higher HF concentration etches the oxide faster. Therefore, increased HF concentration results in faster indirect dissolution reactions. Because the oxide forms in the middle of the pore tip, where the field is enhanced, more than on the sides of the pore [11, 29], increased HF concentration results in smaller pores [11].

Current density

Increased etching current density supplies more holes and hence enhances the tetravalent indirect dissolution reactions in Eq. (2.9). In this reaction, oxide forms and then is chemically removed by HF as shown in Fig. 2.4. The oxide removal limits hence the total process because it is the slowest reaction in the process. When the oxide covers the pore tips, the current has to start to flow from the lower part of the pore walls. When the current flows across the pore walls, the pore diameter increases, and hence the porosity increases. At a certain high current density, the removal of the oxide by HF is too slow compared to the oxide growth due to current flow. Therefore, the oxide forms on the walls before it is removed from the pore bottom. This current density is the threshold value for the electropolishing.

Table 2.2 summarizes the influence of increasing each of the doping concentration N_{A}, the HF concentration c_{HF}, and the etching current density J during anodizing p-type Si on the porosity p and the porous Si growth rate

$$R_{\mathrm{g}} = \frac{d}{t}, \tag{2.10}$$

where d is porous Si thickness formed in a certain time period t.

Table 2.2: *Influence of the porous Si formation conditions on the porosity p and layer growth rate R_g. The arrow ↘ represent an inverse proportionality, while ↗ represents the direct proportionality between the column and row.*

	N_A	c_HF	J
p	↘	↘	↗
R_g	↗	↗	↗

2.1.6 Optical properties

Porous Si consists of monocrystalline Si crystallites and pore sizes in the range of a few nanometers as shown in section 2.1.1. These feature sizes are much smaller than the wavelength of light, which is in the order of hundreds of nanometers. Therefore, from the optical point of view, porous Si is a homogeneous mixture of Si and air [18, 20, 69].

To a first approximation, the optical constants of porous Si are expressed as a mixture of the optical constants of Si and the optical constants of air according to the effective medium theory [70]. The Bruggeman approximation [71] of the effective medium theory allows the determination of the complex refractive index of porous Si $\tilde{n}_\mathrm{Si}(\lambda)$ from the equation

$$p\frac{\tilde{n}^2_\mathrm{Si}(\lambda)-\tilde{n}^2(\lambda)}{\tilde{n}^2_\mathrm{Si}(\lambda)+2\tilde{n}^2(\lambda)}+(1-p)\frac{1-\tilde{n}^2(\lambda)}{1+2\tilde{n}^2(\lambda)}=0, \tag{2.11}$$

where $\tilde{n}_\mathrm{Si}(\lambda)$ is the complex refractive index of monocrystalline silicon.

The porosity dependence of the complex refractive index $\tilde{n}_\mathrm{Si}(\lambda)$ of porous Si allows the fabrication of tailored dielectric layers with desired refractive constants [72]. In addition, porous Si layers with different porosities can be etched on top of each other, as it is possible to fabricate dielectric multilayer interference filters for optoelectronics [20, 73].

The band gap widening of porous Si due to quantum confinement effect [16, 17, 60–62] leads to a decrease of the absorption coefficient of porous Si and hence makes it transparent in the whole infrared region [74]. Interference filters in the infrared range have been demonstrated with good spectral behavior due to the low absorption of porous Si. Even infrared filters are commercially available nowadays. Increasing the porosity further causes a blueshift and enables the fabrication of porous Si filters and light emitting diodes in the visible wavelength range [75, 76].

2.2 Solar Cells

This section addresses the fundamentals of solar cells. It starts with a description of the theory of operation. Then it presents the technological processes for Si solar cells. Finally, I review the most important characterization methods, which this thesis uses to characterize the fabricated solar cells.

2.2.1 Theory of operation

A solar cell is a device that directly converts light into electricity. The incident light consists of photons with energy $E_{\mathrm{ph}} = \mathrm{hc}/\lambda$, where h is Plank's constant, c is the speed of light in vacuum, and λ is the wavelength of the incident light. In the absorption process, the energy of the photon transforms an electron from its valence state to a conduction state [77, 78]. This process is called the excitation of an electron from the valence band (VB) to the conduction band (CB). In such a transition, both energy and momentum have to be conserved [77, 79]. This process is also called electron/hole generation process. The absorption of a photon depends on the photon wavelength and on the material itself. The energy of the photon has to be enough for the electron transition from the VB to the CB. Therefore, it has to be larger than the band gap of the semiconductor E_{g}. Each material is distinguished by its absorption coefficient $\alpha(\lambda)$. The absorption coefficient is the inverse of the absorption length L_α. The absorption length L_α is the distance in the semiconductor, after which the light intensity drops to 1/e of its initial value at the semiconductor surface. The number of generated electron/hole pairs per unit volume per second as a function of the depth z into the cell is termed as the generation profile $g(z)$.

The absorption of light and generation of electron/hole (e/h)pairs is not enough to generate electricity. The separation of the e/h pairs from each other and the collection of them from different electrodes before they recombine again is necessary for the generation of electrical power. The average time, in which the charge carriers live before they recombine is called the carrier lifetime τ. The minority charge carriers diffuse in a semiconductor due to the concentration gradient for a distance in a duration equals its lifetime before they recombine. This distance is defined as the minority carrier diffusion length

$$L_{\mathrm{n,p}} = \sqrt{D_{\mathrm{n,p}}\tau} \tag{2.12}$$

for electrons in p-type semiconductor and holes in n-type semiconductor respectively, with the minority carrier diffusion constant $D_{\mathrm{n,p}}$ in p-type and n-type semiconductors.

The carriers recombine more likely at the surfaces of the semiconductor, the interfaces with metals, and defects like grain boundaries. The recombination at the surface is characterized by the surface recombination velocity S. Therefore, the effective diffusion length L_{eff} depends on the diffusion length $L_{\text{n,p}}$ and the surface recombination velocity S.

Figure 2.5 pictures a pn-junction high performance Si solar cell [77, 80]. The maximum laboratory efficiency of such a cell is $\eta = 24.7$ % on FZ Si wafer [81] and $\eta = 21.5$ % cell with a thickness $d_{\text{cell}} \approx 50$ μm achieved by wafer thinning [82]. The p-type Si base with an acceptor concentration N_{A} acts as an absorber of the cell. An n-type emitter with a donor concentration N_{D} is formed by phosphorous diffusion. The junction between the n-type emitter and the p-type base forms a space charge region (SCR). The absorber absorbs the most of the incident light due to its larger thickness compared to the emitter. The light absorption results in the generation of e/h pairs. The number of the generated e/h pairs per unit volume as a function of the distance from the cell surface is called the generation profile $g(z)$.

The collection of the charge carriers depends on the material quality, where materials with low defect density have a large minority carrier diffusion length $L_{\text{n,p}}$. Also, the quality of the interfaces affect the effective diffusion length L_{eff}. Therefore, the front and back surfaces have to be passivated [83]. Passivation means the saturation of the dangling bonds on the surface, which are considered as recombination centers. Possible passivation layers are SiO_2 [84, 85], Si_3N_4 [86], or a-Si:H [1, 87]. Thermally grown SiO_2 is a perfect passivation material, but it has the drawback that it does not work as an anti-reflection coating (ARC) for encapsulated cells, because it has the same refractive index $n_{SiO_2} = 1.5$ as the encapsulation materials. Hence, a material with a higher refractive index is required. Silicon nitride has the advantage that its refractive index is adjustable by the deposition parameters. The ARC increases the coupling of light into the solar cell. The coupling of light is increased also by the texturing of the surface. The chemical etching of Si in KOH produces on the wafer surface random pyramids, which increase the path length of radiation in the cell and decrease the front surface reflectivity.

Figure 2.5 shows also a part of the front contact grid. The grid contains many fingers with a certain width, hight, and spacing connected together with a busbar (the busbar is not shown in the figure). The grid has to be optimized to minimize the shadowing losses and at the same time minimize the electrical losses due to the resistance of the grid [88].

The interface between Si and metal has the maximum surface recombination velocity $S_{\text{max}} = 10^7$ cm/s. Therefore, the metallization contact area at the back side must be minimized. However, the contact area has to be large enough to minimize the series resis-

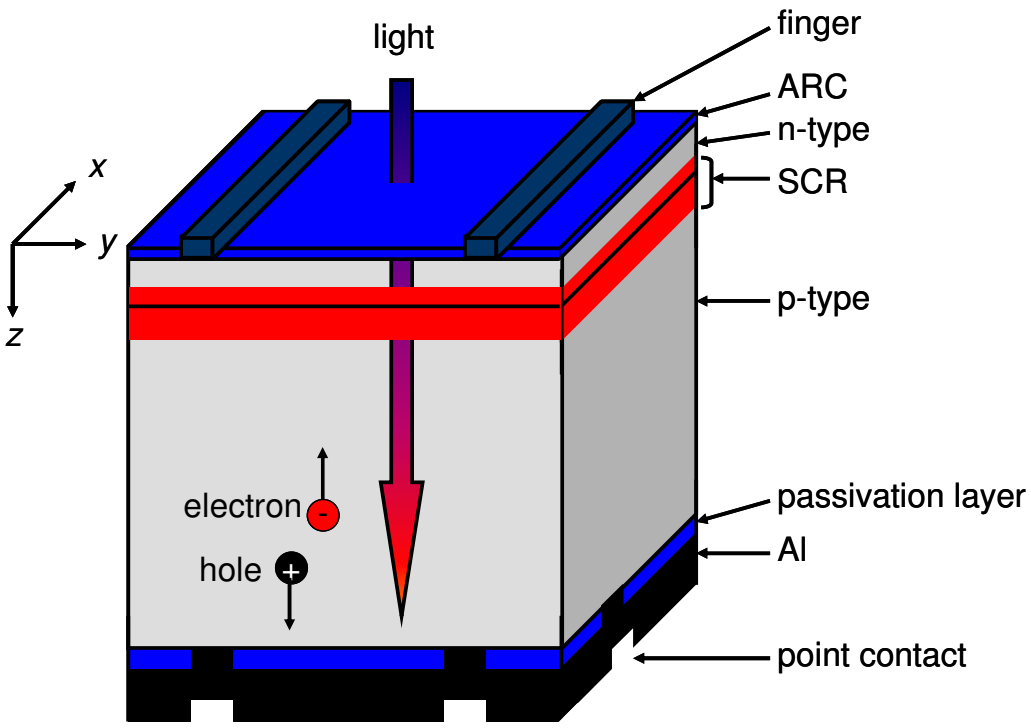

Figure 2.5: *Schema of a high performance pn-junction Si solar cell. The semiconductor absorbs the incident light generating electron/hole pairs. The generated carriers are collected by diffusion towards the junction and then conducted through the front and back contacts to the external circuit. The front side grid contains finger with certain dimensions and spacings connected together with a busbar (not shown here). The grid is designed to maximize the output. The anti-reflection coating (ARC) couples light into the cell by decreasing the front surface reflectivity. The back side structure contains a dielectric layer as a passivation layer and Al as a back contact. This structure acts also as a back reflector for radiation and the point contacts conduct the current to the external circuit.*

tance R_s. Therefore, point contacts are optimized with respect to the effective diffusion length L_{eff} together with the series resistance R_s to get a maximum power from the cell [89]. In industry, a back surface field, formed by a heavily doped diffused Al layer on the full area, reduces the effect of the back side recombination velocity S_b.

The structure of point contacts has an additional advantage. The structure of Si/dielectric/metal acts as a back reflector [90]. The back reflector reflects radiation, which is not absorbed in the first path through the cell, again into the cell and hence enhances the light trapping. The back reflector is designed to reflect the wavelengths, which are not absorbed by choosing the thickness and the refractive index of the dielectric [90].

The reciprocity theory of Donolato [91, 92] enables a simplified modeling and simulation of the functionality of the solar cell in figure 2.5. The carrier collection probability density $f_c(x, y, z)$ is the fraction of generated charge carriers at a point (x, y, z) that are

collected in the external circuit [93, 94]. The partial differential equation

$$\nabla^2 f_{\mathrm{c}}(x,y,z) = \frac{f_{\mathrm{c}}(x,y,z)}{L^2} \tag{2.13}$$

describes the collection probability $f_{\mathrm{c}}(x,\ y,\ z)$, where $L = L_{\mathrm{n}}$ in the p-type base and $L = L_{\mathrm{p}}$ in the n-type emitter. The solar cell is generally divided into three regions:

1. The emitter layer, which is a neutral n-type layer with a minority carrier diffusion length L_{p}.

2. The space charge region (SCR), which is depleted of carriers. The model assumes a 100 % collection probability of carriers generated in the SCR. Therefore $f_{\mathrm{c}}(x,\ y,\ z) = 1$ in the SCR.

3. The p-type base, which is a neutral p-type layer with a minority carrier diffusion length L_{n}.

The solution of the differential equation in Eq. (2.13) with the appropriate boundary conditions in each region provides the collection probability density function in each position in the solar cell. The boundary conditions are generally in the form

$$\nabla f_{\mathrm{c}}(x,y,z) = \frac{S_{\mathrm{f,b}}}{D_{\mathrm{n,p}}} f_{\mathrm{c}}(x,y,z), \tag{2.14}$$

where S_{f} is the effective recombination velocity at the front side and S_{b} is the effective recombination velocity at the back side. There are two approaches to solve Eq. (2.13) with the boundary conditions in Eq. (2.14). The first approach [94] is to distinguish between the boundary regions which have a contact with the passivation layer S_{f} and S_{b} and the boundary regions which have a metallic contact with $S_{\mathrm{m}} = 1{\times}10^7$ cm/s, i.e. $f_{\mathrm{c}} = 0$. This approach requires a numerical three dimensional or at least an approximated two dimensional solution [94]. The second approach is to define an effective recombination velocity of the front $S_{\mathrm{f,eff}}$ and back $S_{\mathrm{b,eff}}$ sides regardless of there structures [1, 95–97]. The second approach requires a simple one dimensional solution of Eq. (2.13) [95–97] and determines the one dimensional collection probability

$$f_{\mathrm{c}}(z) = \exp\left(-\frac{z}{L_{\mathrm{eff}}}\right), \tag{2.15}$$

where z is the coordinate, which is parallel to the radiation direction shown in figure 2.5 and $z = 0$ is at the boundary between the SCR and the neutral regions. The effective diffusion length in Eq. (2.15) is defined in the p-type base as the electron effective diffusion

length

$$L_{\mathrm{n,eff}} = L_{\mathrm{n}} \frac{\cosh\left(\frac{H_{\mathrm{b}}}{L_{\mathrm{n}}}\right) + \frac{S_{\mathrm{b,eff}} L_{\mathrm{n}}}{D_{\mathrm{n}}} \sinh\left(\frac{H_{\mathrm{b}}}{L_{\mathrm{n}}}\right)}{\sinh\left(\frac{H_{\mathrm{b}}}{L_{\mathrm{n}}}\right) + \frac{S_{\mathrm{b,eff}} L_{\mathrm{n}}}{D_{\mathrm{n}}} \cosh\left(\frac{H_{\mathrm{b}}}{L_{\mathrm{n}}}\right)}, \tag{2.16}$$

where H_{b} is the base thickness [96]. In the n-type emitter, the diffusion length in Eq. (2.15) is defined as the hole effective diffusion length

$$L_{\mathrm{p,eff}} = L_{\mathrm{p}} \frac{\cosh\left(\frac{H_{\mathrm{e}}}{L_{\mathrm{p}}}\right) + \frac{S_{\mathrm{f,eff}} L_{\mathrm{p}}}{D_{\mathrm{p}}} \sinh\left(\frac{H_{\mathrm{e}}}{L_{\mathrm{p}}}\right)}{\sinh\left(\frac{H_{\mathrm{e}}}{L_{\mathrm{p}}}\right) + \frac{S_{\mathrm{f,eff}} L_{\mathrm{p}}}{D_{\mathrm{p}}} \cosh\left(\frac{H_{\mathrm{e}}}{L_{\mathrm{p}}}\right)}, \tag{2.17}$$

where H_{e} is the emitter thickness [96].

Figure 2.6 schematically illustrates the one dimensional profiles of the generation $g(z)$ and the collection probability function $f_{\mathrm{c}}(z)$. The short circuit current density

$$J_{\mathrm{SC}} = q \int f_{\mathrm{c}}(z) g(z) dz \tag{2.18}$$

represents the total generated and collected charge carriers. The reverse saturation current density

$$J_0 = q D_{\mathrm{n}} \frac{n_{\mathrm{i}}^2}{N_{\mathrm{A}}} \frac{\mathrm{d}f_{\mathrm{c}}}{\mathrm{d}z} \mid_{z=d_{\mathrm{p}}} + q D_{\mathrm{p}} \frac{n_{\mathrm{i}}^2}{N_{\mathrm{D}}} \frac{\mathrm{d}f_{\mathrm{c}}}{\mathrm{d}z} \mid_{z=d_{\mathrm{n}}} \tag{2.19}$$

is also determined from the collection probability function [98], where n_{i} is the intrinsic carrier concentration.

2.2.2 Characterization methods

This section addresses the characterization methods used in this thesis to evaluate solar cells qualities. This work evaluates the material quality by the determination of the effective diffusion length L_{eff} from the measured internal quantum efficiency. In addition, it characterizes the current density/voltage (J/V) measured curve according the equivalent circuit of the solar cell to determine the parallel resistance R_{p}, the series resistance R_{s}, the ideality factor n_{id}, and the reverse saturation current density J_0.

Quantum efficiency

The external quantum efficiency EQE is defined as the probability of an incident photon contributing one electron to the short circuit current of the solar cell. The external quantum efficiency

$$EQE(\lambda) = \frac{\triangle j_{\mathrm{sc}}}{q \triangle \Phi_{\lambda}} \tag{2.20}$$

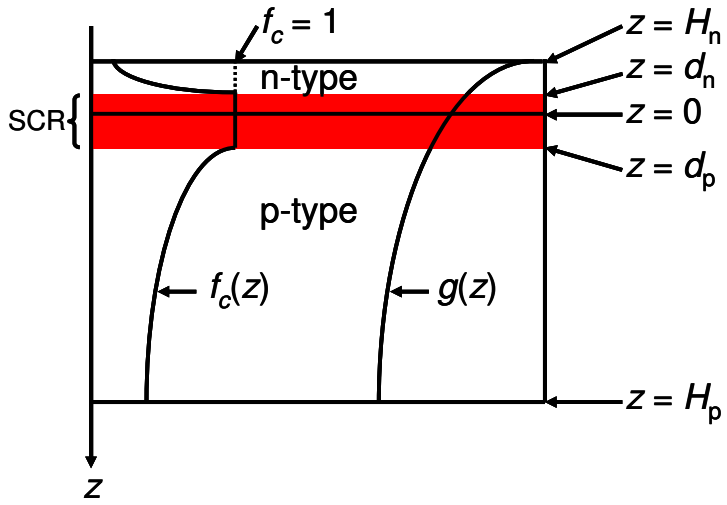

Figure 2.6: *Schema of one dimensional profiles of the generation $g(z)$ and the collection probability function $f_c(z)$. The integral of the multiplication of $f_c(z)$ and $g(z)$ determines the short circuit current density as described by Eq. (2.18). The saturation current density depends on the derivative of $f_c(z)$ at $z = d_n$ and $z = d_n$ as shown in Eq. (2.19).*

is measured as the change of the short circuit current density $\triangle j_{\mathrm{sc}}$ due to a change of the illuminating photon flux density $\triangle \Phi_\lambda$, where q denotes the elementary charge. Using monochromatic radiation provides a depth resolution in the z direction since the absorption length L_α increases monotonically with the wavelength [99].

The external quantum efficiency EQE depends on the optical properties of the cell, as radiation that does not enter the cell, does not contribute to the current. Therefore, one measures both the $EQE(\lambda)$ and the reflection $R(\lambda)$ and then calculates the internal quantum efficiency

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)}, \tag{2.21}$$

which is less dependent on the optical properties of the cell.

The most important feature of the internal quantum efficiency IQE is that the effective diffusion length $L_{\mathrm{n,eff}}$ in the base is extracted directly from it [95]. For simplicity, I denote $L_{\mathrm{n,eff}}$ as L_{eff} in the rest of the work. The plot of the inverse internal quantum efficiency IQE^{-1} versus the absorption length L_α shows two linear regions [95]. The range, in which L_α is smaller than the cell thickness, the data fits to the straight line

$$IQE^{-1} = 1 + \xi \frac{L_\alpha}{L_{\mathrm{eff}}} \tag{2.22}$$

with the factor ξ considering the longer effective path due to texture; it holds $\xi = 0.8$ for cells textured by KOH [100, 101].

Current density/voltage characteristics

Figure 2.7 illustrates the typical variation of the current density J as a function of the voltage V for a solar cell under illumination. The open circuit voltage $V_{\rm OC}$ is defined as the voltage at $J = 0$. The short circuit current density $J_{\rm SC}$ is the current density at $V = 0$ and it is approximately equals to the photogenerated current density $J_{\rm ph}$.

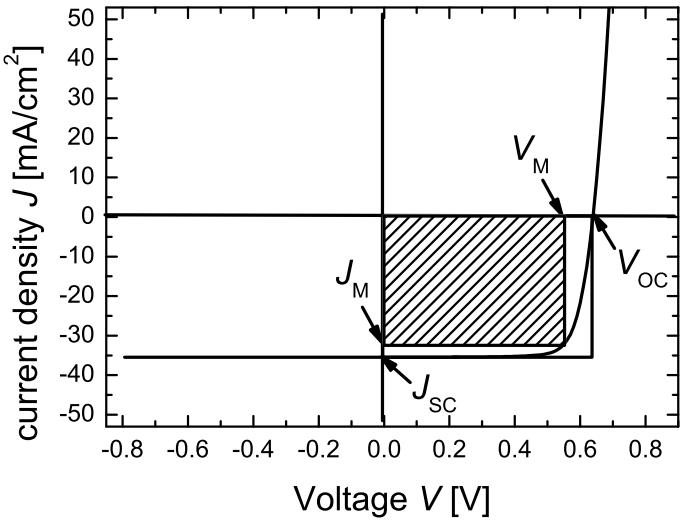

Figure 2.7: *Typical current density/voltage dependence under illumination. The small hatched square represents the maximum power $P_{\rm M}$. The large square represents the multiplication $V_{\rm OC}J_{\rm SC}$. The fill factor FF is the ratio between the small square to the large square.*

The fill factor

$$FF = \frac{P_{\rm M}}{V_{\rm OC}J_{\rm SC}} \tag{2.23}$$

is a measure of the diode form of the solar cell, where $P_{\rm M}$ is the maximum power delivered from the solar cell. The maximum power point is defined, as shown in figure 2.7, by the maximum power point voltage $V_{\rm M}$ and the maximum power point current density $J_{\rm M}$, where $P_{\rm M} = V_{\rm M}J_{\rm M}$. The efficiency η of the solar cell is defined as the ratio between the maximum power $P_{\rm M}$ and the power of the incident radiation. Assuming that the efficiency is measured under AM1.5G illumination, the efficiency

$$\eta = \frac{P_{\rm M}}{P_{\rm AM1.5G}} \tag{2.24}$$

with $P_{\rm AM1.5G} = 100$ mW/cm^2. Substituting $P_{\rm M}$ from Eq. (2.23), determines the efficiency

$$\eta = FF\frac{V_{\rm OC}J_{\rm SC}}{P_{\rm AM1.5G}} \tag{2.25}$$

Figure 2.8 shows the equivalent circuit of a solar cell. The equivalent circuit models the solar cell as a diode with an ideality factor n_{id} and reverse saturation current density J_0. The diode represents the recombination current density of the cell. The recombination in the SCR leads to a maximum ideality factor $n_{\mathrm{id}} = 2$ [52]. Therefore, the ideality factor generally lies between $n_{\mathrm{id}} = 1$ and $n_{\mathrm{id}} = 2$, regardless of some special cases, in which the ideality factor $n_{\mathrm{id}} > 2$ due to for example the inhomogeneity of a $CuInSe_2$ solar cell [101, 102]. The constant current source with a current density J_{SC} considers the photogeneration. All resistive losses such as the losses in contacts and Si bulk are modeled as a series resistance R_{s}. Finally, the parallel resistance R_{p} considers the shunts through the pn-junction.

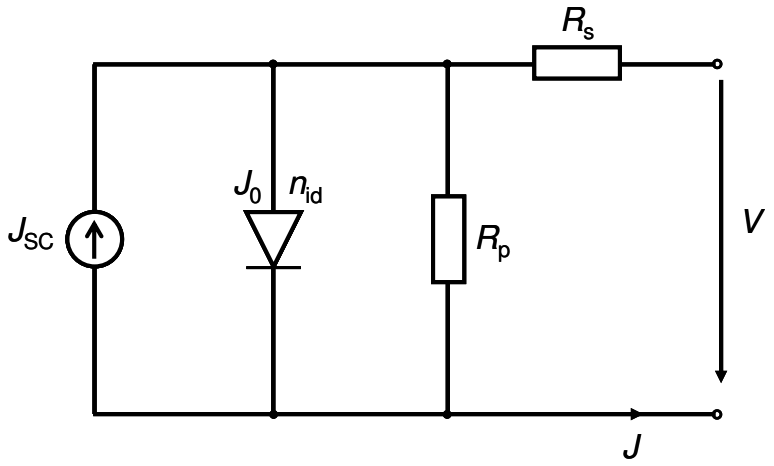

Figure 2.8: *Equivalent circuit of the solar cell. The diode with ideality factor n_{id} and reverse saturation current density J_0 represents the diode part of the cell. The constant current source with a current density J_{SC} considers the short circuit current density of the cell. The series resistance R_{s} models the resistive losses in contacts and bulk, where the parallel resistance R_{p} corresponds to the shunt through the junction.*

According to the equivalent circuit in figure 2.8, the J/V characteristics of a solar cell is described by the equation

$$J = J_0 \left[\exp\left(\frac{q(V - JR_{\mathrm{s}})}{n_{\mathrm{id}} kT} \right) - 1 \right] + \frac{V - JR_{\mathrm{s}}}{R_{\mathrm{p}}} - J_{\mathrm{SC}} \tag{2.26}$$

The series R_{s} and the parallel R_{p} resistances in Eq. (2.26) have the unit [$\Omega\mathrm{cm}^2$], where the current density J has the unit [$\mathrm{mA/cm}^2$] and the voltage V has the unit [V]. The equivalent circuit components are evaluated from the measured J/V curve as follows [103]:

1. Calculation of the parallel resistance R_{p}

$$R_{\mathrm{p}} = \left(\frac{\mathrm{d}J}{\mathrm{d}V}\right)^{-1} \tag{2.27}$$

at $V < 0$ V.

2. Correction of the current density J with parallel resistance and J_{SC} to get the corrected current density

$$J_{\mathrm{c}} = J - \frac{V}{R_{\mathrm{p}}} + J_{\mathrm{SC}}, \tag{2.28}$$

provided that $R_{\mathrm{p}} \gg R_{\mathrm{s}}$.

3. Determination of the small signal conductance

$$g(V) = \frac{\mathrm{d}J_{\mathrm{c}}}{\mathrm{d}V} \tag{2.29}$$

4. Dividing the conductance $g(V)$ by the corrected current $J_{\mathrm{c}}(V)$ and plotting $g(V)/J_{\mathrm{c}}(V)$ versus the conductance $g(V)$. This plot yields a straight line according to

$$\frac{g(V)}{J_{\mathrm{c}}(V)} = \frac{q}{n_{\mathrm{id}}kT}[1 - g(V)R_{\mathrm{s}}], \tag{2.30}$$

5. Fitting the g/I_{c} leads to a straight line. The x-axis intersection X_0 determines R_{s}, where the y-axis intersection Y_0 determines n_{id} as follows:

$$R_{\mathrm{s}} = \frac{1}{X_0} \tag{2.31}$$

and

$$n_{\mathrm{id}} = \frac{q}{kTY_0}, \tag{2.32}$$

where q is the elementary charge, k is the Boltzmann constant, and T is the temperature.

6. Determination of the reverse saturation current density J_0; The corrected current J_{c} is extrapolated in the logarithmic scale. The intersection with the y-axis determines the reverse saturation current density J_0. The saturation current density satisfies also the equation

$$J_0 = J_{\mathrm{SC}} \exp(-\frac{qV_{\mathrm{OC}}}{n_{\mathrm{id}}kT}) \tag{2.33}$$

This analysis assumes a voltage step $\triangle V \leq 10$ mV [103]. I developed a Matlab programm [102], which calculates the equivalent components (R_{p}, R_{s}, n_{id}, and J_0) from the measured J/V data according to the steps 1 to 6.

Chapter 3

Porous Silicon Technology at *ipe*

This chapter surveys the porous Si technology and its application fields at ipe. *Porous Si is the base of several activities such as the fabrication of thin-film Si solar cells by the layer transfer process, photoluminescence, and Ge on porous Si. This chapter draws two important conclusions: i) Doping variation of the anodized substrate is necessary, as the optimum doping concentration for the porous silicon used in the layer transfer process is not suitable for luminescent porous silicon fabrication. ii) Free-standing Si thin-film solar cell overcomes the drawbacks of the conventional layer transfer process. The drawbacks of the transfer process are the limited processing temperature, the light absorption in the epoxy resin, and the difficult module connection.*

3.1 Experimental Details

Figure 3.1a shows a CAD[1] drawing of the double chamber etching cell[2], which is used at *ipe* to electrochemically form porous Si. A vacuum wafer chuck enables the exposure of the full front surface area of the wafer to the electrolyte. Therefore, porous Si forms on the full surface area of the wafer. An insulating tunnel enhances the homogeneity of the current density over the wafer area [2]. As porous Si propagates perpendicular to the surface, the current density variation over the wafer is termed as the lateral homogeneity. The etching process uses hydrofluoric acid mixed with ethanol (CH_3CH_2OH) as an electrolyte. The commercially available hydrofluoric acid is an aqueous diluted HF with a concentration c_{HF} = 49 %. This thesis uses two different HF concentrations: i) A solution with c_{HF} = 40 % has a volumetric composition ratio of HF:water:ethanol = 1:1:1. ii) A solution with c_{HF} = 33 % has a volumetric composition ratio of HF:water:ethanol = 1:1:2. Hydrofluoric acid is toxic, corrosive, and hazardous to water [105]. At the used high concentrations

[1] Computer Aided Design

[2] The etching cell and the drawing are done by LOTUS Systems GmbH, Germany [104]

$c_{\mathrm{HF}} \geq 25$ %, any exposure of parts of the skin, ingestion, and inhalation of vapors are potentially deadly [105, 106]. The risk of exposure is minimized by wearing suited protective clothing, boots, gloves and face masks, and work has to be carried out in an extractor hood to prevent inhalation of vapors [2, 106]. The setup is suitable for etching both 4" an 6" wafers by replacing the wafer chuck, however, all wafers etched in this work are 6" wafers.

Chapter 5 enhances the lateral homogeneity of porous Si formation by designing a new wafer chuck, which is realized by LOTUS Systems GmbH. Figure 3.2 depicts the side view and the elevation view of the designed wafer chuck. Only a circle with a diameter smaller than the wafer diameter is exposed to HF, hence porous Si forms only on this circular area. The new chuck requires a new insulating tunnel with an opening identical to the exposed wafer area.

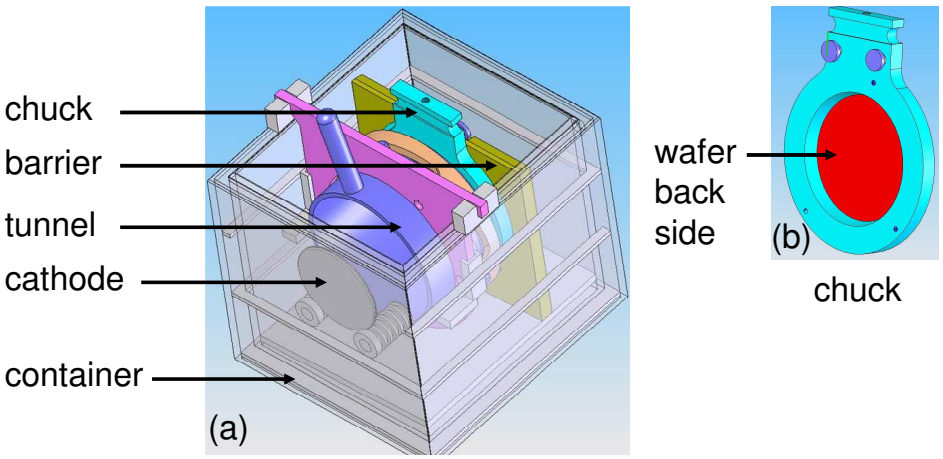

Figure 3.1: *(a) A CAD-drawing of the etching cell used to produce porous Si at* ipe. *(b) The wafer chuck from the back side. Back side is the side which faces the anode.*

3.2 Application fields

3.2.1 Transfer process

Solar cells based on monocrystalline Si wafers have power conversion efficiencies up to $\eta = 25$ % [81]. One approach to decrease the cost of photovoltaic power generation is to minimize the used material [79]. Wafer thinning to a thickness of around 50 μm still enables solar cells with an efficiency $\eta = 21.5$ % [82]. Obviously, wafer thinning is not suitable to decrease the material use. In order to enable economically viable thin Si layers, several techniques [55, 107–115] have been developed that employ transferring monocrystalline Si

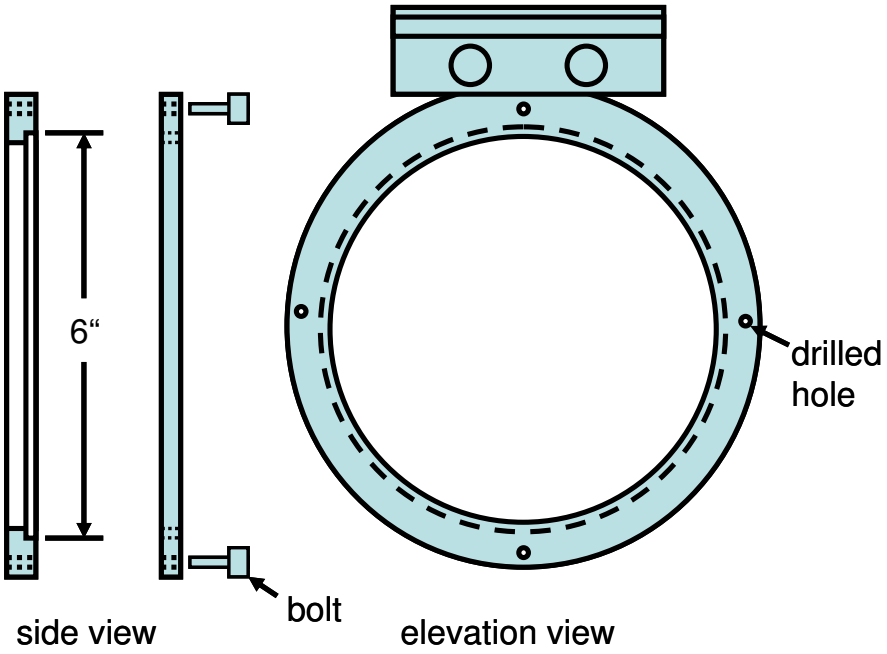

Figure 3.2: *Side and elevation views of the new wafer chuck. The new wafer chuck etches an area smaller than the wafer area, but with better lateral homogeneity compared to the old one.*

layers onto foreign substrates. A state-of-the-art transfer process, which is developed at *ipe* [114, 116, 117], enables the fabrication of about 50 μm thin Si solar cells on a glass substrate with an efficiency $\eta = 16.6$ % [118] and on flexible substrates with an efficiency $\eta =$14.6 % [2, 119]. The transfer process is based on Si epitaxy on a porous Si double layer after a high temperature treatment in H_2 atmosphere.

Figures 3.3a, b describe the structure transformation of the porous Si double layer during the heat treatment. The porous Si double layer in Fig. 3.3a forms by two-step electrochemical etching of a Si wafer in hydrofluoric acid. First, a layer with low porosity p_1 forms at a low current density J_1. Second, increasing the current density J_2 for a short time evolves a buried layer with a high porosity p_2.

Figure 3.3b depicts the structure after the heat treatment at a temperature $T = 1100$ °C. The upper low porosity Si layer recrystallizes and forms the quasi-monocrystalline Si (QMS) layer. The QMS layer allows a high quality epitaxially grown monocrystalline Si layer by chemical vapor deposition (CVD). The high electronic quality of the deposited layer is proved by the fabrication of up to 17 % efficient solar cells with a thickness $d = 47.4$ μm [3]. The buried high porosity Si layer establishes the separation layer, which contains cavities and Si-columns between the QMS layer and the host wafer. Therefore, the separation layer is mechanically weak and enables the separation of the epitaxy layer from the host wafer by applying a mechanical force. Solar

cells are fabricated on the epitaxy layer and then a glass substrate is attached to the front surface of solar cells with an epoxy resin. After the separation of the cells from the host wafer, the back side contact is applied and then the cells are measured. To reach the front side contact, a silver stripe is soldered to the pad of the front side grid before the glass attachment.

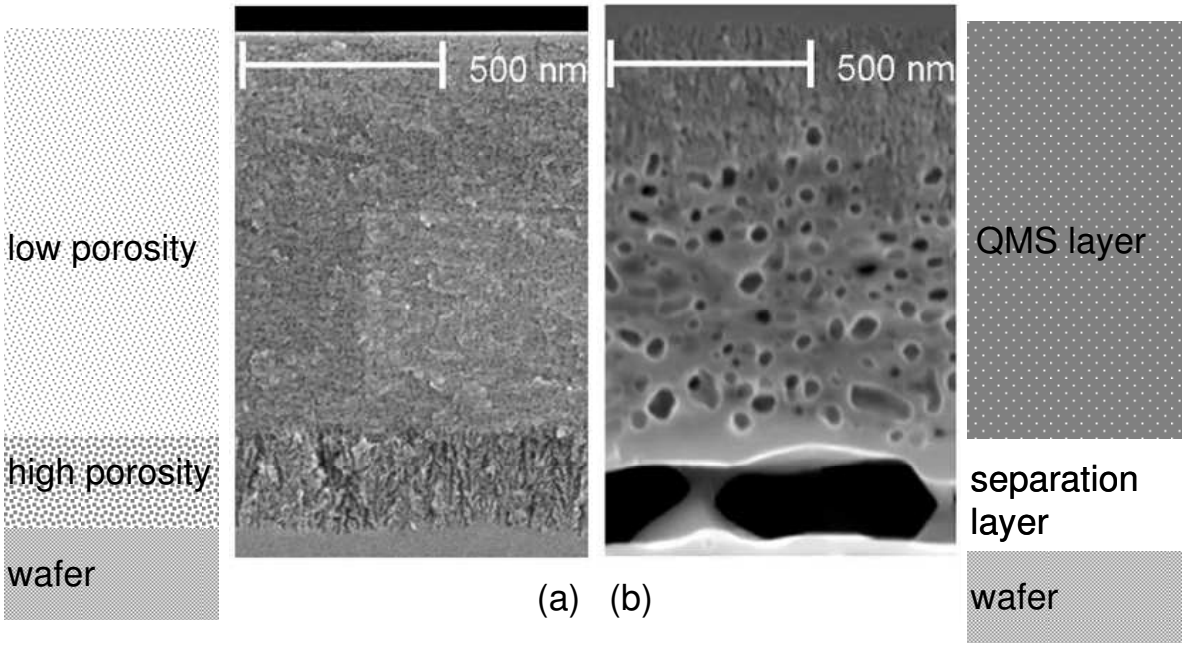

Figure 3.3: *Structure transformation of porous silicon double layer [2]. a) A buried high porosity layer forms under a low porosity layer during etching. b) Heat treatment forms a separation layer from the buried high porosity layer. The upper low porosity layer builds the quasi-monocrystalline silicon (QMS). The separation layer contains cavities and remaining Si columns. The QMS layer serves as a seed for high quality epitaxy. The separation layer is mechanically weak and hence enables the transfer of the epitaxy layer.*

Disadvantages of the transfer process

This chapter discusses the drawbacks of solar cells produced by the transfer process. The first drawback is the difficulty of the fine adjustment of the separation layer, on the one hand, firmly to fix the epitaxy layer on the host wafer during device processing and, on the other hand, to easily enable a layer separation after the device fabrication. Therefore, the reproducibility of the process depends on the first step of the process, namely the porous Si formation. Furthermore, the substrate attachment on top of the fabricated cell with an epoxy resin leads to three problems: i) The first problem is the complicated module connection of cells with glass on the top. ii) The second problem is the resin

itself, which limits the processing temperature T of the back side to $T \leq 200$ °C and hence a complicated back contact processing is required [1]. iii) In addition, the epoxy resin absorbs a significant amount of radiation and hence limits the performance of the solar cell [45].

I. Adjustment of the separation layer properties:
The structure of the separation layer has to be well adjusted to fulfill two conditions:

1. Mechanical stability during the device fabrication.

2. Capability to easily separate the device from the wafer after fabrication.

On one hand, the amount of Si-columns per cm^3 is responsible for the mechanical stability of the epitaxy layer during the device fabrication. On the other hand. the amount of cavities offers the capability to separate the epitaxy layer from the host wafer by applying mechanical force after the device fabrication. These two conditions are so correlated that a complicated experimental optimization procedure is required. Unfortunately, the structure of the separation layer changes during the device fabrication due to restructuring during the high temperature steps. Therefore, it is difficult to predict the separation capability of the fabricated device.

II. Module connection:
The transfer process results in a solar cell with a glass substrate attached on its top. Therefore, the series connection of cells and the capsulation are not straight forward processes. Chapter 8 introduces a new method, which simplifies the module connection and capsulation. In this method all connected cells are transferred onto single glass substrate, then laser machining allows to reach to the front side contact from the back side of the cell [120].

The presented method enables the fabrication of mini-modules for low power consumption applications. However, this new method is complicated and the connection of free-standing thin cells would be simpler and probably more industry compatible. Therefore, the present work concentrates mainly on the production of free-standing Si thin-films, see chapter 7. Before producing free-standing layers, the homogeneity of porous Si is optimized in chapter 5, on which the quality of the transfer process depends.

III. Back side processing:
Brendle has introduced a novel stacked back contact system in his PhD thesis [1]. The

optimized back side structure provides a low surface recombination velocity, enhancement of light trapping and a good ohmic contact. The low processing temperature $T_{\mathrm{p}} \leq 220$ °C makes the back side structure suitable for transfer solar cells on glass substrates. The back contact is fabricated as follows:

1. Removal of the QMS layer and the heavily doped back surface field by chemical etching.

2. Deposition of a thin a-Si:H layer at a temperature $T = 130$ °C. This layer provides a good passivation of the back side, which enables a back contact surface recombination velocity S_{b} as low as $S_{\mathrm{b}} = 15$ cm/s [1].

3. Deposition of a silicon nitride layer, which increases the back side reflection.

4. Evaporation of Al as a back metallization. The silicon nitride/Al system acts as a back side mirror and enhances the red region performance of the cell.

5. Laser fired contact (LFC) provides point contacts by firing the Al through the nitride layer as well as the a-Si layer to Si.

6. Annealing of the complete cell at a temperature $T = 220$ °C

This back side structure increases the series resistance R_{s} for transfer solar cells from $R_{\mathrm{s}} = 0.16\ \Omega\mathrm{cm}^2$ to $R_{\mathrm{s}} = 0.6\ \Omega\mathrm{cm}^2$ [1]. In addition, the processing is complicated compared to the conventional industrial back contact. However, it improves the electronic as well as the optical performance of the thin cell. The production of free-standing cells increases the upper limit of the processing temperature from $T_{\mathrm{lim}} = 220$ °C up to $T_{\mathrm{lim}} = 420$ °C and hence enables the application of high quality silicon nitride as well as the conventional firing.

3.2.2 Photoluminescence

The *ipe* produces porous Si for investigating photoluminescence[3] [45, 121, 122]. The goal of luminescent Si is the fabrication of Si light emitting diodes (LEDs) integrated on Si chips. The problem is that the Si energy band gab $E_{\mathrm{g}} = 1.12$ eV at room temperature causes a radiation in the infrared (IR) regime. To shift the radiative spectrum towards the blue wavelength, the band gap has to be increased. Lehman and Goesele [17] reported that porous Si exhibits a band gap increase compared with bulk Si due to the

[3]Photoluminescence measurements are performed by N. Ximello

quantum confinement in the small crystallites. Therefore, porous Si is a suitable material for the fabrication of LEDs which emits visible radiation with a designable wavelength. Unfortunately, the degradation and the low efficiency of the Si LED due to its high power consumption are the main drawbacks of Si as a LED. Therefore, the *ipe* performs experiments to increase the output signal of porous Si luminescence and maintain its level for long time. We use the passivation techniques which are successfully used at *ipe* to fabricate high efficiency solar cell. Low temperature process are preferable to avoid the thermal variation of the structural properties of porous Si.

Figure 3.4 depicts the latest results of the photoluminescent porous Si [45]. The photoluminescence (PL) peak of the porous Si layer is at $\lambda = 800$ nm. A 7 nm thin a-Si:H[4] capping layer deposited by PECVD[5] enhances the PL signal intensity of porous Si up to 10 times [45]. Annealing of the system at a temperature $T = 300$ °C decreases slightly the PL intensity, but maintain it at the same level for at least two months.

The doping variation of the p-type Si wafer results in an optimum doping density $N_A = 10^{16}$ cm^{-3} for higher PL intensity [45]. Therefore, it is necessary to anodize lightly doped p-type wafers. Chapter 4 compares the dissolution mechanisms of lightly and heavily doped Si. In addition, chapter 6 explains the etching unavailability of lightly doped wafers in the double chamber etching cell and introduces a method for etching such wafers without changing the etching setup. Lightly doped wafers have to have a heavily doped back contact to be able to form porous Si at low voltages (see chapter 6).

3.2.3 Germanium on porous silicon (GOPS)

Ge growth on Si has many applications in microelectronics [123–126]. The lattice mismatch $\delta = 4.2$ % between Si and Ge is overcome by growing a SiGe buffer layer, which is called virtual substrate [127]. The *ipe* works together with the Institut für Halbleitertechnik (IHT) to replace the conventional buffer by a porous Si layer. Therefore, study of Ge grown on porous Si (GOPS) is of high interest. Porous Si is a soft material and could accommodate at least partly the lattice mismatch [128]. This method would enable a cheap virtual substrate for Ge. In addition, it would provide a low cost Si wafer for the growth of high performance III/V solar cells [129], because Ge has the same lattice constant as GaAs.

Figure 3.5 depicts a cross-sectional scanning electron microscopic (SEM) photo of a Ge film grown on porous Si. A 1.3 μm thin porous Si layer is formed by anodizing a heavily

[4]Hydrogenated amorphous Si is deposited at *ipe* by C. Ehling

[5]Plasma Enhanced Chemical Vapor Deposition

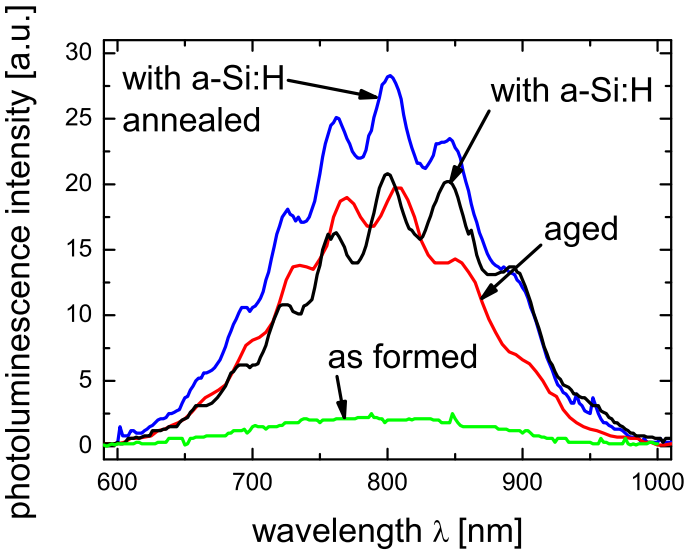

Figure 3.4: *Photoluminescence of porous Si. A 7 nm thin a-Si:H capping layer enhances the PL signal intensity of porous Si up to 10 times [45]. Annealing at $T = 300$ °C maintains the PL signal up to two months.*

doped wafer with a resistivity ρ between $\rho = 10$ to $\rho = 16$ mΩcm in HF at a current density $J = 10$ mA/cm^2 for time $t = 65$ s. Molecular beam epitaxy[6] (MBE) [130–132] serves to grow a Ge film at a temperature $T = 530$ °C. A Ge film with an average thickness $d_{\mathrm{Ge}} = 150$ nm covers the complete surface of the porous Si layer. The transmission electron microscopic[7] (TEM) investigation proves that the grown Ge layer shown in Fig. 3.5 is (100) oriented single crystalline[8] [133]. Figure 3.5 shows a complete coverage of the surface but with a large inhomogeneity.

To improve the Ge layer homogeneity, the porous Si properties have to be optimized. Therefore, controlling and measuring the porosity is a very important issue. Chapter 4 introduces a new non-destructive method for porosity estimation.

Molecular beam epitaxy is a suitable deposition method to cover porous Si completely with single crystalline Ge layer at low temperature $T = 530$ °C. The Ge layer has a large inhomogeneity probably due to a high rough surface of the porous Si. Porosity optimization requires the accurate estimation of it. Chapter 4.1 presents a new method of porosity determination by analyzing the measured reflected spectrum by a white light interferometer.

[6] MBE done by IHT

[7] Measured by F. Phillipp, Max Plank Institute, MPI, Stuttgart

[8] Explained by M. Oehme, IHT from the TEM and RAMAN spectroscopy analysis (unpublished)

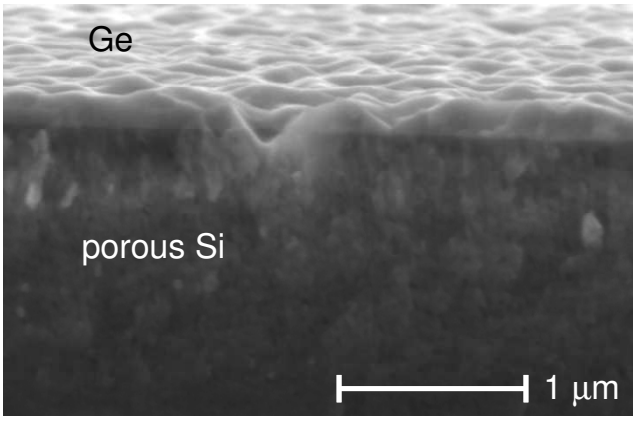

Figure 3.5: *Cross-sectional SEM photo of a Ge film grown by MBE at T = 530 °C on porous Si. Porous Si is formed by anodizing a Si wafer in HF by a current density J = 10 mA/cm^2 for duration t = 65 s. The surface is complectly covered by Ge.*

3.3 Summary and Conclusions

This chapter has reviewed the porous Si technology and its application fields at *ipe*. Porous Si is the base of many activities at *ipe* such as:

1. Fabrication of thin-film Si solar cells by the layer transfer process.
2. Photoluminescence from porous Si layers.
3. Growth of Ge on porous Si (GOPS).

This chapter has explained the drawbacks of the transfer process:

1. The difficulty of the adjustment of the separation layer in a way that it fixes the device layer during processing and enables the separation of the device layer from the host after device fabrication.
2. The complicated module connection due to the glass coverage of the front side.
3. The complex back surface processing due to the low processing temperature limit.
4. The light absorption in the epoxy resin, which attaches the glass substrate on the top of the cell.

Considering the drawbacks of the layer transfer process, the free-standing Si layers have to be produced without the need of any substrate and resin. In addition, the separation

layer has to be formed in a way that allows the separation and at the same time fixes the device layer. The mechanical stability of the layer during device fabrication as well as the capability to easily separate the layer after device fabrication correlated properties. Both of them depend on the number of Si columns per cm^3. These two properties have to be separated from each other simplify the process adjustment.

Chapter 7 presents a solution for problems of the transfer process, by introducing a new method, which produces free-standing Si thin films. The method separates the separation properties from the fixation properties by locally defined cavities, which are fabricated by selective porous Si formation.

Photoluminescence experiments require porous Si formation on lightly doped Si wafers. The double chamber etching cell at *ipe* is not suitable to etch lightly doped wafers. Therefore, chapter 6 studies doping effects of both, the front and the back side of the wafer during electrochemical etching. Lightly doped Si wafers are anodized in the double chamber etching cell after doping its back side with a high boron concentration by ion implantation.

The next chapter characterizes porous Si and introduces a non-destructive method to estimate the porosity. This method allows the characterization of the porous Si lateral homogeneity in chapter 5, and hence enhances the transfer process.

Chapter 4

Porous Silicon Characterization

The first step to controlling and enhancing the layer transfer process is to understand the porous Si formation. This chapter introduces a new non-destructive method, which estimates the porosity of both single- and multi-layer porous Si on a Si wafer by a fast white light interferometer measurement. Based on the new porosity determination method, this chapter develops a model, which determines the number of consumed holes during the porous Si formation. This number is termed as the dissolution valence. The dissolution valence $n_{dv} = 3$ of heavily doped wafers is larger than the $n_{dv} = 2$ of lightly doped wafers. According to the current knowledge of silicon electrochemical etching, there are two possible reaction paths to electrochemically dissolve silicon in hydrofluoric acid. The first reaction path has $n_{dv} = 2$ and evolves hydrogen, while the second reaction path has $n_{dv} = 4$ and does not evolve hydrogen. Proposing a total electrochemical reaction explains the dissolution valences $n_{dv} > 2$. The hydrogen evolution rate from the total reaction is not equivalent to the Si atom dissolution rate. The exact ratio between hydrogen evolution and Si dissolution is calculated directly from the determined dissolution valence.

4.1 Porosity Determination by White Light Interferometries

As reviewed in chapter 2.1.1, the conventional porosity determination method is destructive, as it is based on measuring the mass loss after porous Si formation and mass loss after the removal of the porous Si layer. This chapter presents a new nondestructive method to precisely measure and predict the porosity p of electrochemically etched silicon. The method evaluates the white light interferometer measurements of multiple porous Si layers on a Si wafer with an optical model. The model deals porous Si as a material with a refractive index, which depends on the porosity according to the effective medium theory.

Scanning electron microscopic (SEM) measurements show that the thickness prediction of the optical method is very precise, the error e is $e < 2\ \%$.

4.1.1 Experimental details

Figure 4.1 illustrates the functional principle of a white light interferometer of the type F-20[1], which serves in this work for the porosity p measurements of porous silicon. A tungsten-halogen bulb generates radiation with wavelengths λ from $\lambda = 400$ to $\lambda = 3000$ nm. A fiber-optic cable delivers the generated radiation to the sample. A two-way waveguide separates the generated and reflected beams and delivers the reflected radiation through a fiber-optic to the spectrometer. The spectrometer contains a grating to disperse radiation and an array of 512 photodiodes to measure the radiation intensity at 512 different wavelengths. The electronic signals collected from the 512 photodiodes are collected by a personal computer.

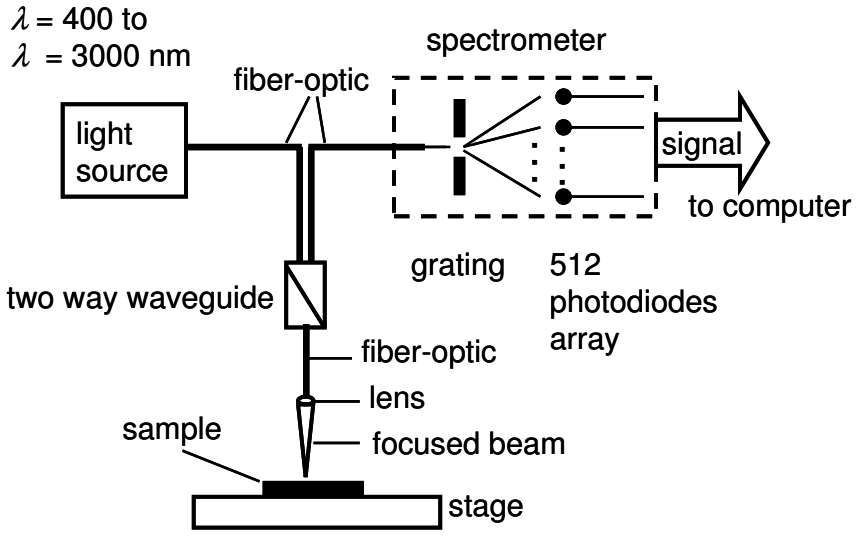

Figure 4.1: *Functional principle of white light interferometer of type F-20. Radiation is supplied by a tungsten-halogen bulb that generates radiation with wavelengths λ from $\lambda = 400$ to $\lambda = 3000$ nm. The radiation is delivered and collected from the sample through a fiber-optic cable bundle and a lens. The intensity of the reflected radiation is measured at 512 different wavelengths with a linear photodiodes array. The F-20 spectrometer uses a grating to disperse the radiation. The measured electrical signals are collected by a computer to be processed.*

A MATLAB[2] programm analyzes the collected data according to the physical model of

[1]Produced by Filmetrics, Inc. (USA), www.filmetrics.com

[2]MATLAB is a high level language and interactive medium, which enables the fast and effective calculation of technical tasks. MATLAB is produced by the MathWorks^{TM}, www.mathworks.com

radiation interferometries in the matrix formalism [72] as discussed below in section 4.1.2. The model calculates the reflectance $R_{\mathrm{c}}(\lambda)$ of the porous silicon system and compares it with the measured reflectance $R_{\mathrm{m}}(\lambda)$. The penalty function

$$F = \sum_{i=1}^{N_\lambda} [R_{\mathrm{m}}(\lambda_{\mathrm{i}}) - R_{\mathrm{c}}(\lambda_{\mathrm{i}})] \tag{4.1}$$

evaluates the error, where N_λ is the number of wavelengths.

To evaluate the presented porosity determination method, porous Si single layers formed by electrochemical etching of p-type Si 6" wafers are measured by white light interferometry. A scanning electron microscope (SEM) measures the thickness d_{SEM} of each porous sample. The wafers are etched in an aqueous hydrofluoric solution with the composition HF:CH_3CH_2OH:H_2O of 1:1:1, which corresponds to HF mass concentration $c_{\mathrm{HF}} = 40$ %. Two kind of wafers are used in this work: heavily doped p^+-type wafers with a resistivity ρ between $\rho = 10$ to $\rho = 16$ mΩcm and lightly doped p-type wafers with resistivity ρ between $\rho = 0.5$ to $\rho = 2$ Ωcm.

4.1.2 Modeling of multilayer porous Si system

Figure 4.2a gives a schema of a multilayer porous silicon system on a monocrystalline silicon substrate. Each porous silicon layer j has a porosity p_{j} and a thickness d_{j}. The layer thickness is measured by a scanning electron microscope (SEM) to decrease the number of unknown variables during the calculation of the reflectance $R_{\mathrm{c}}(\lambda)$. The reflectance

$$R_{\mathrm{c}}(\lambda) = \frac{\mathrm{R}(2,1) \cdot \mathrm{R}^*(2,1)}{\mathrm{R}(1,1) \cdot \mathrm{R}^*(1,1)} \tag{4.2}$$

is determined from the reflection transfer matrix R of the system. The system transfer matrix R determines the electric field intensity components of the incident E_0^+ and reflected E_0^- waves in air via

$$\begin{pmatrix} E_0^+ \\ E_0^- \end{pmatrix} = \mathrm{R} \begin{pmatrix} E_t \\ 0 \end{pmatrix} \tag{4.3}$$

as a function of the electric field intensity component E_{t} of the wave, which is transmitted into the Si substrate.

Figure 4.2b depicts the boundary number j between the porous layers j and $j+1$. The boundary conditions at the surface determines the boundary transfer matrix

$$\mathrm{M_j} = \frac{1}{t_{\mathrm{j}}} \begin{pmatrix} \phi_{\mathrm{j\text{-}1}}^{-1} & 0 \\ 0 & \phi_{\mathrm{j\text{-}1}} \end{pmatrix} \begin{pmatrix} 1 & r_{\mathrm{j}} \\ r_{\mathrm{j}} & 1 \end{pmatrix}, \tag{4.4}$$

which is a function of the phase shift

$$\phi_{\text{j-1}} = \exp(i\frac{2\pi}{\lambda}\tilde{n}_{\text{j-1}}d_{\text{j-1}}) \tag{4.5}$$

due to each layer , the layer reflectance

$$r_{\text{j}} = \frac{\tilde{n}_{\text{j-1}} - \tilde{n}_{\text{j}}}{\tilde{n}_{\text{j-1}} + \tilde{n}_{\text{j}}} \tag{4.6}$$

and the layer transmittance

$$t_{\text{j}} = \frac{2\tilde{n}_{\text{j-1}}}{\tilde{n}_{\text{j-1}} + \tilde{n}_{\text{j}}} \ , \tag{4.7}$$

where $\tilde{n}_{\text{j}}$ is the effective complex refractive index of the porous silicon layer and d_{j} is the layer thickness.

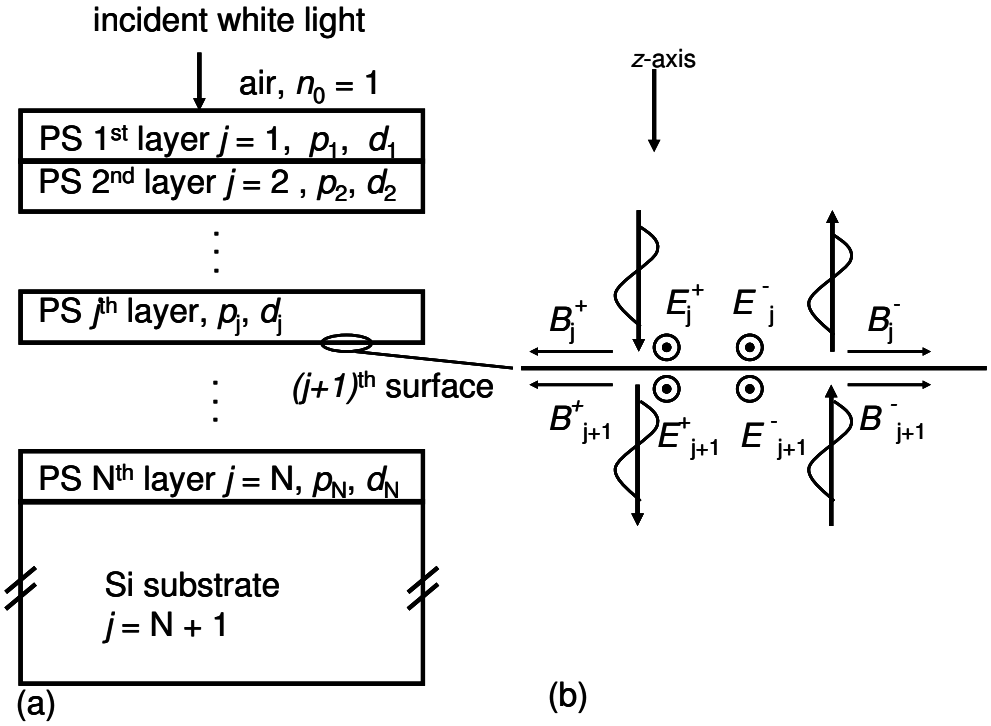

Figure 4.2: *(a) Multilayer porous silicon layers with different porosities pj and thicknesses dj on a silicon substrate. The suffix j represents the layer number of the N porous silicon layers, where j = N+1 represents the substrate. (b) The boundary j+1 between two consecutive porous silicon layers j and j+1 shows the continuity of electric field intensity E and magnetic field density B of electromagnetic waves propagating in positive z direction, with the + superscript, and in the negative z direction, with the - superscript.*

The multiplication of all boundary matrices gives the system transfer matrix

$$\text{R} = \prod_{j=1}^{N} \text{M}_{\text{j}} \ . \tag{4.8}$$

The model calculates the porous Si complex refractive index $\tilde{n}(\lambda)$ for each porous Si layer from the equation

$$p\frac{\tilde{n}_{\mathrm{Si}}^2(\lambda)-\tilde{n}^2(\lambda)}{\tilde{n}_{\mathrm{Si}}^2(\lambda)+2\tilde{n}^2(\lambda)}+(1-p)\frac{1-\tilde{n}^2(\lambda)}{1+2\tilde{n}^2(\lambda)}=0 \tag{4.9}$$

according the Bruggemann approximation [18] of the effective medium theory as described in chapter 2.1.6, where $\tilde{n}_{\mathrm{Si}}(\lambda)$ is the complex refractive index of monocrystalline silicon. Figure 4.3 shows the the calculated complex refractive index $\tilde{n}(\lambda)$ of porous Si from Eq. (4.9) at different porosities.

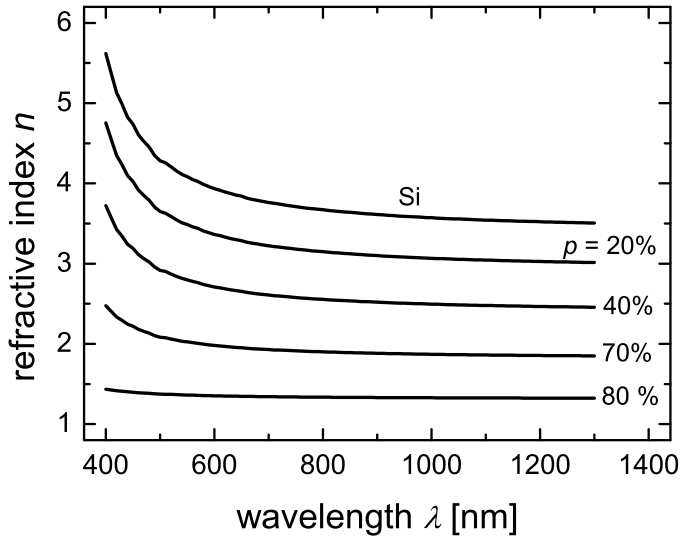

Figure 4.3: *The real part of the refractive index of porous silicon as determined from the effective medium theory [18] decreases by increasing porosity p.*

The presented model allows the calculation of the reflectance $R_{\mathrm{c}}(\lambda)$ of a porous Si system on a Si wafer as a substrate. I have developed a MATLAB program to calculate $R_{\mathrm{c}}(\lambda)$. The program compares $R_{\mathrm{c}}(\lambda)$ with the measured reflectance $R_{\mathrm{m}}(\lambda)$ from the white light interferometer and minimizes the error, which is expressed by the penalty function in Eq. (4.1) to estimate the porosities of the layers. Single layer porous Si structures as well as double layer porous Si systems are characterized by the presented program.

4.1.3 Results

This section presents the evaluation results of the white light interferometer method of the estimation of the porosity p. The evaluation methodology consists of the determination of the porous Si thickness by two independent methods. The first method is the white

light interferometer and the second method is the direct measurement of the thickness by the scanning electron microscope. The white light interferometer measurements and simulation predicts the porosity p and the optically determined thickness d_{WLI}, while the geometrical thickness d_{G} of porous Si is directly measured by the scanning electron microscope. The white light interferometer method is evaluated by the determination of the error

$$e = \frac{d_{\mathrm{WLI}} - d_{\mathrm{G}}}{d_{\mathrm{WLI}}} \times 100. \tag{4.10}$$

Figures 4.4 to 4.6 compare the measured reflectance by white light interferometer and the calculated reflectance of porous silicon layer on a heavily doped p^+-type wafer for the three samples PS1, PS2, and PS3, which are listed in Table 4.1. The measured reflected spectrum from sample PS1 in Fig. 4.4 fits very well to the calculated spectrum at a porosity $p = 30$ % and a porous layer thickness $d_{\mathrm{WLI}} = 600$ nm. Figure 4.5 shows a good fitting between the reflected spectrum and the modeled spectrum for sample PS2. The simulation results in a porosity $p = 62$ % and a porous Si layer thickness $d_{\mathrm{WLI}} = 675$ nm. Finally, Fig. 4.6 calculates the porosity $p = 63$ % and the porous Si layer thickness $d_{\mathrm{WLI}} = 1240$ nm of sample PS3 with a very good fitting.

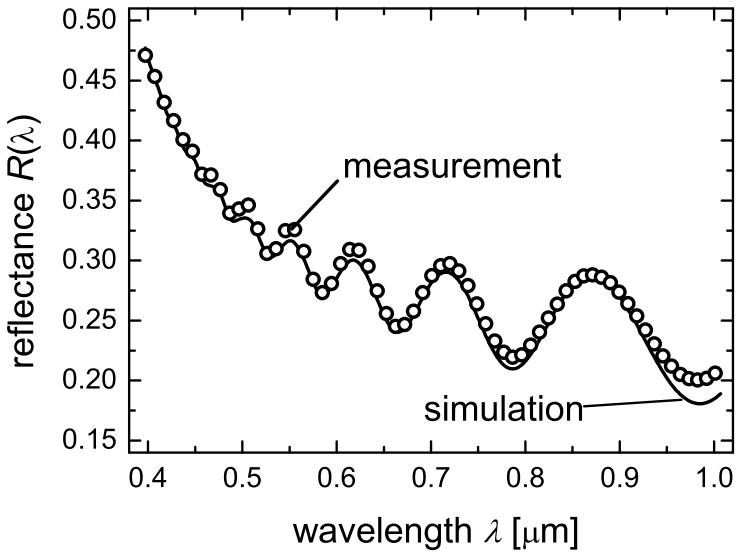

Figure 4.4: *Comparison between the measured reflectance by white light interferometer and the calculated reflectance of porous silicon layer with a thickness $d_{WLI} = 600$ nm on a heavily doped silicon wafer. The simulation determines a porosity $p = 30$ %*

.

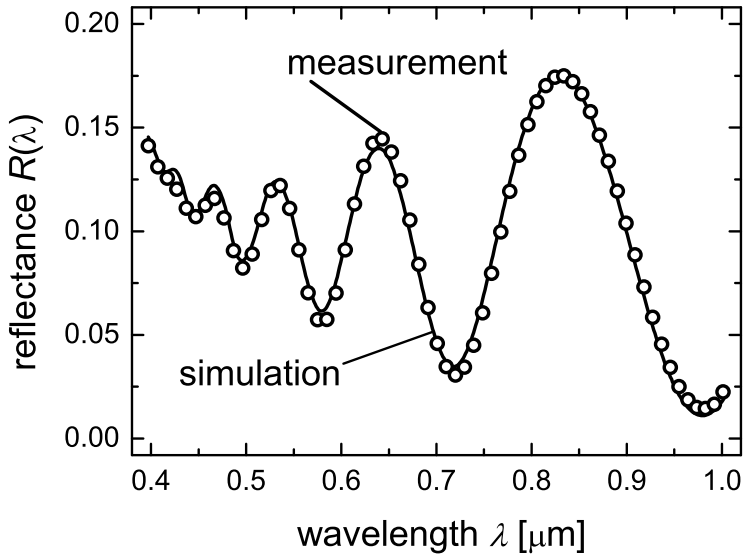

Figure 4.5: *Comparison between measured reflectance from white light interferometer and calculated reflectance of a porous silicon layer on a lightly doped silicon wafer. The model determines porosity p = 62 %, and a porous silicon layer thickness d_{WLI} = 675 nm.*

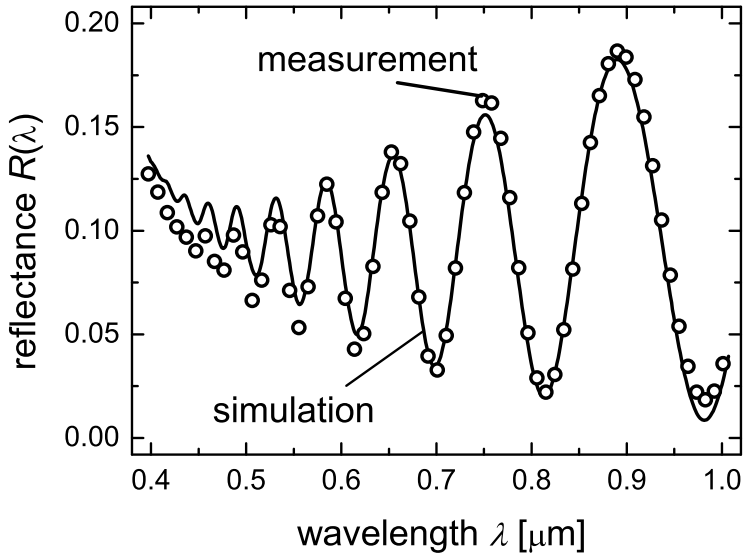

Figure 4.6: *Comparison between measured reflectance from white light interferometer and calculated reflectance of a porous silicon layer on a lightly doped silicon wafer. The modeled porosity p is p = 63 %, and the porous silicon layer thickness d_{WLI} is d_{WLI} = 1240 nm.*

Table 4.1 lists porous Si formation conditions as well as porous Si parameter, which are determined by the two independent measurement techniques. The uncertainty of the geometrical thickness determined by the SEM is estimated by measuring different five points and calculating the average thickness and its standard deviation.

Section 4.2 will use the method presented here for the determination of the dissolution valence n_{dv} during the electrochemical etching of Si wafers in HF. Heavily doped p^+-type Si shows a dissolution valence $n_{\mathrm{dv}} = 3$ during the anodization and lightly doped p-type Si has $n_{\mathrm{dv}} = 2$.

Table 4.1: *Evaluation of the white light interferometer method of porosity estimation. Porous Si forms by electrochemically etching Si wafers in HF with a mass concentration $c_{HF} = 40$ %. The etching parameters are current density J and etch duration t. The white light interferometer measurements and simulation determine the porosity p and the thickness d_{WLI}, while the geometrical thickness d_G of porous Si is directly measured by the scanning electron microscope. The heavily doped wafer PS1 has a resistivity ρ between $\rho = 10$ to $\rho = 16$ mΩcm while lightly doped p-type wafers PS2 and PS3 have a resistivity ρ between $\rho = 0.5$ to $\rho = 2\,\Omega$cm. The method optical determines the layer thickness of porous Si with an error $e < 2$ %*

Sample	J	t	p	d_{WLI}	d_{G}	e
	[mA/cm^2]	[s]	[%]	[nm]	[nm]	[%]
PS1 (p^+-type)	10	30	30	600	600 ∓ 30	0
PS2 (p-type)	10	60	62	675	663 ∓ 40	1.8
PS3 (p-type)	20	60	63	1240	1220 ∓ 50	1.6

4.2 Dissolution Mechanism

Porous silicon forms by anodic attack of silicon in an aqueous hydrofluoric acid solution as described in chapter 2.1.1. Positive charge carriers are necessary for the dissolution of Si in HF. The number of holes consumed to dissolve one Si atom is known as the dissolution valence n_{dv}. The determination of the exact dissolution valence is necessary for understanding the dissolution mechanism of porous Si formation. In addition, n_{dv} enables the expectation of the porosity [2, 26]. Tanaka *et al.* developed a nondestructive method which determines the porosity from the hydrogen gas evolved at the cathode during the electrochemical etching [26]. The method assumes implicitly that all silicon atoms are dissolved in a process which evolves hydrogen. Calculations based on the assumption

that all Si atoms dissolve with evolution of hydrogen [26] result in dissolution valences $n_{dv} = 2$ to $n_{dv} = 2.67$ for formation of stable porous Si. Some works calculate the porosity by assuming a certain value of dissolution valence, for example $n_{dv} = 2.4$ in Ref. [134], and $n_{dv} = 3.4$ in Ref. [135]. To avoid the non-physical assumption of the dissolution valence value, the exact dissolution valance has to be determined.

This chapter introduces a new method, which determines the dissolution valence n_{dv} and finds $n_{dv} = 3$ for p^+-type Si anodization regardless of the HF concentration and $n_{dv} = 2$ for p-type Si anodization. The resulted dissolution valence $n_{dv} = 3$ for p^+-type Si shows that hydrogen evolution corresponds to only a certain ratio P of the total dissolved Si atoms and not all dissolved atoms as assumed by some groups [26, 32, 33]. The method determines the exact ratio P of dissolved Si atoms with hydrogen evolution from the dissolution valence n_{dv}. In the case of heavily doped p^+-type Si, only 50 % of dissolved Si atoms corresponds to hydrogen evolution, while in the case of lightly doped p-type Si all dissolved Si atoms evolve hydrogen.

4.2.1 Experimental details

The present experiment determines the dissolution valence n_{dv} for three groups of samples. Table 4.2 summarizes the differences between the three sample groups. Group A contains heavily doped 6" Si wafers with resistivity ρ between $\rho = 10$ to $\rho = 16$ mΩcm. The wafers are etched in an aqueous hydrofluoric solution with the composition HF:CH_3CH_2OH:H_2O of 1:1:1, which corresponds to an HF mass concentration $c_{HF} = 40$ %. Group B contains also heavily doped 4" Si wafers with resistivity ρ between $\rho = 12$ to $\rho = 18$ mΩcm. Samples of group B are etched in an aqueous hydrofluoric solution with the composition HF:CH_3CH_2OH:H_2O of 1:2:1, which corresponds to HF mass concentration $c_{HF} = 33$ %. Group C contains lightly doped 6" Si wafers with resistivity ρ between $\rho = 0.5$ to $\rho = 2$ Ωcm. The wafers are etched in an aqueous hydrofluoric solution with the composition HF:CH_3CH_2OH:H_2O of 1:1:1, which corresponds to HF mass concentration $c_{HF} = 40$ %.

Tables 4.3 to 4.5 list the etching parameters, current density J and etching duration t, and the optically determined porous Si layer parameters, thickness d and porosity p, of the groups A to C. The layer thicknesses of groups A and C are determined by SEM and the porosities are then determined by the white light interferometer measurements as described in chapter 4.1. The porosity and etching parameters of group B are taken from Ref. [55]. The porosities of samples B were determined by the conventional weighing method as described in chapter 2.1.1 and Ref. [55]. The group B include a heavily

doped samples as group A, but a different HF concentration. Group C has the same HF concentration of group A, but different doping. The groups enables the study of both effects, doping and HF concentrations, with the minimum number of experiments. The next chapter develops a model which determines the dissolution valence n_{dv} from the parameters listed in tables 4.3 to 4.5 and investigates the validity of the model.

Table 4.2: *Wafer resistivity ρ and HF mass concentration c_{HF} of the three sample groups. Groups A and C are characterized by white light interferometer, while the porosity of group B is taken from the Ref. [55].*

Sample group	ρ [Ωcm]	c_{HF} [%]
A (p^+-type)	0.01-0.016	40
B (p^+-type)	0.008-0.018	33
C (p-type)	0.5-2	40

Table 4.3: *Porosity and layer thickness of single layer porous silicon etched in 40 % concentrated HF on heavily doped p^+-type silicon wafers. The layer thickness d is measured by SEM and the porosity p is determined by white light interferometry. The samples are etched with different current densities J and durations t.*

Sample	J [mA/cm^2]	t [s]	d [nm]	p [%]
A1	10	65	1220	23
A2	10	130	2400	24
A3	20	130	4510	27
A4	130	3	350	48
A5	200	65	12100	45

Table 4.4: *Porosity and layer thickness of single layer porous silicon etched etched in 33 % concentrated HF on heavily doped p^+-type silicon wafers. The layer thickness d and the porosity p The porosity and etching parameters of group B are taken from Ref. [55]. The samples are etched with different current density J and etching duration t.*

Sample	J [mA/cm^2]	t [s]	d [nm]	p [%]
B1	25	10	400	30
B2	50	10	700	33
B3	100	10	1150	35
B4	200	10	2000	40
B5	300	10	2650	50

Table 4.5: *Porosity and layer thickness of single layer porous silicon etched etched in 40 % concentrated HF on lightly doped p-type silicon wafers. The layer thickness d is measured by SEM and the porosity p is determined by white light interferometer. The samples are etched with variable current densities J and durations t.*

Sample	J [mA/cm^2]	t [s]	d [nm]	p [%]
C1	10	60	675	62
C2	20	60	1240	63
C3	50	60	2482	67
C4	50	30	1493	61
C5	50	90	3500	77
C6	50	120	5400	73

4.2.2 Silicon dissolution model

The model defines the consumed charge density

$$q_{\mathrm{c}} = \frac{It}{A} = Jt \tag{4.11}$$

to electrochemically dissolve a certain volume of Si during time t, where A is the area exposed to the electrolyte, and I is the current passing through the sample. The dissolved Si volume is normalized to the exposed surface area A and hence expressed as an effective

dissolved thickness

$$d_{\mathrm{d,eff}} = pd, \tag{4.12}$$

where d is the porous Si layer thickness. When each Si atom needs n_{dv} holes to dissolve [12], the relation between $d_{\mathrm{d,eff}}$ and q_{c} results from the balance between the number

$$N_{\mathrm{h}} = \frac{q_{\mathrm{c}}}{q} \tag{4.13}$$

of consumed holes and the number

$$N_{\mathrm{Si}} = pd\rho_{\mathrm{a,Si}} \tag{4.14}$$

of dissolved Si atoms, where q is the elementary charge and $\rho_{\mathrm{a,Si}} = 4.82{\times}10^{22}$ cm^{-3} is the atomic density of Si. The balance equation

$$N_{\mathrm{Si}} = \frac{N_{\mathrm{h}}}{n_{\mathrm{dv}}}. \tag{4.15}$$

together with Eqs. (4.11) to (4.14) gives the effective dissolution thickness

$$d_{\mathrm{d,eff}} = \frac{1}{q\rho_{\mathrm{a,Si}}n_{\mathrm{dv}}}q_{\mathrm{c}} \tag{4.16}$$

as a linear function of the consumed charge density q_{c}. Eq. (4.16) shows that the slope of the linear function $d_{\mathrm{d,eff}}(q_{\mathrm{c}})$ depends only on the dissolution valence n_{dv}.

The next section 4.2.4 determines the slope of the experimentally determined $d_{\mathrm{d,eff}}$ and q_{c} from Tables 4.3 to 4.5 in the previous section 4.2.1, and hence determines $n_{\mathrm{dv}} = 3$ for heavily doped samples and $n_{\mathrm{dv}} = 2$ for lightly doped samples. The validity of the method of dissolution valence determination is also investigated by the determination of the deviation of the slope in the logarithmic scale. The next chapter proves that this method is valid for both heavily and lightly doped samples with an accuracy $a > 97$ %.

4.2.3 Results

Figure 4.7 presents the experimentally determined effective dissolved thickness $d_{\mathrm{d,eff}}$ as a function of the consumed charge density q_{c} together with the linear fit according to Eq. (4.16). The heavily doped samples show a dissolution valence $n_{\mathrm{dv}} = 3$ regardless of the HF concentration, while the lightly doped samples have a dissolution valence $n_{\mathrm{dv}} = 2$. The dissolution valence $n_{\mathrm{dv}} = 3$ for heavily doped samples is valid for both group A which is characterized by the white light interferometer and group B which is characterized by the conventional method [55].

The present method assumes that the dissolution valence n_{dv} does not depend on the consumed charge density during the etching. The validity of the assumption and the accuracy of the determination of n_{dv} are investigated by rewriting Eq. 4.16 after taking the logarithm of both sides. The equation

$$\log(d_{\mathrm{d,eff}}) = \; -\log(q\rho_{\mathrm{a,Si}}n_{\mathrm{dv}}) + \log(q_{\mathrm{c}}) \tag{4.17}$$

shows also a straight line with a slope

$$S = \; \frac{d\log(d_{\mathrm{d,eff}})}{d\log(q_{\mathrm{c}})} = 1 \tag{4.18}$$

provided that n_{dv} does not depend on q_{c}. The unity in Eq. 4.18 proves the linearity of Eq. (4.16) and shows that the slope is constant, i.e. n_{dv} is independent on the etching parameter, J and t.

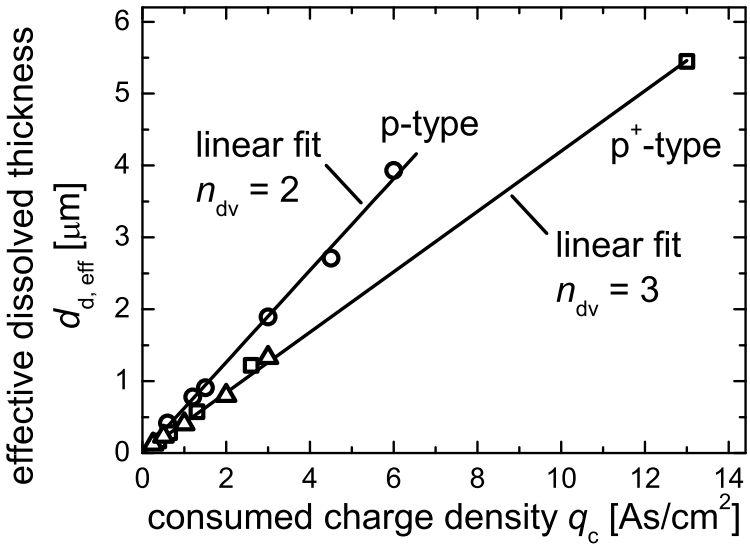

Figure 4.7: *Effective dissolved thickness $d_{d,eff}$ as calculated from geometrical porous silicon layer thickness d_G and porosity p for samples in Table 4.2. Heavily doped samples show a dissolution valence $n_{dv} = 3$, while lightly doped samples show $n_{dv} = 2$.*

Figure 4.8 illustrates the logarithmic linearity of Eq. (4.16). The slope S is very close to unity for both heavily doped, $S = 0.99$, and lightly doped, $S = 0.97$, samples. The slight deviation of the slope S from $S = 1$ shows a negligible deviation of the dissolution valences from the estimated values, namely $n_{\mathrm{dv}} = 3\pm0.03$ for p$^+$-type and $n_{\mathrm{dv}} = 2\pm0.06$ for p-type samples.

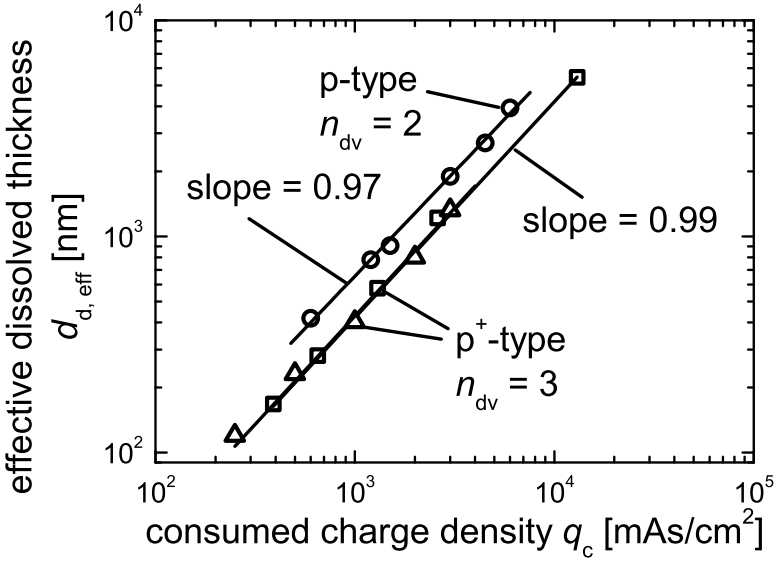

Figure 4.8: *A logarithmic presentation of the linear behavior of the effective dissolved thickness $d_{d,eff}$ on q_c. The linear behavior in the logarithmic scale with a slope S very close to $S = 1$ indicates that the dissolution valence $n_{dv} = 3$ for heavily doped samples and $n_{dv} = 2$ for lightly doped samples are do not depend on q_c.*

4.2.4 Discussion

Chapter 2.1.1 stated that there are two main reactions responsible for the electrochemical dissolution of Si in HF containing electrolyte. Some groups [26, 32, 33] assume that the direct reaction

$$\mathrm{Si+2F^-+4HF+2h^+ \rightarrow H_2SiF_6+H_2 \uparrow} \tag{4.19}$$

takes place in the porous Si formation region, while the indirect oxidizing reaction

$$\mathrm{Si+4OH^-+6HF+4h^+ \rightarrow H_2SiF_6+4H_2O} \tag{4.20}$$

should happen only in the case of electrochemical polishing. The direct reaction in Eq. (4.19) is a divalent reaction as it consumes two holes to dissolve one Si atom, i.e. $n_{\mathrm{dv}} = 2$ is expected. The indirect reaction in Eq. (4.20) is a tetravalent reaction as it consumes four holes to dissolve one Si atom, i.e. $n_{\mathrm{dv}} = 4$ is expected. The divalent reaction in Eq. 4.19, $n_{\mathrm{dv}} = 2$, evolves one hydrogen molecule for each dissolved Si atom, while the tetravalent reaction in Eq. 4.20, $n_{\mathrm{dv}} = 4$, does not evolve hydrogen at all.

The measured dissolution valence $n_{\mathrm{dv}} = 2$ for lightly doped wafers indicates that only the divalent reaction in Eq. (4.19) takes place during the electrochemical etching.

Unfortunately, a dissolution valence $n_{\mathrm{dv}} > 2$ cannot be explained only with the direct dissolution reaction in Eq. (4.19). This means, in the case of heavily doped wafers, both reactions take place, each with a certain probability. When no other reactions take place except those in Eqs. (4.19) and (4.20), then the divalent reaction takes place with a probability P and the tetravalent reaction takes place with a complementary probability (1-P). The two weighted reaction are

$$P[\mathrm{Si}+2\mathrm{F}^{-}+4\mathrm{HF}+2\mathrm{h}^{+} \rightarrow \mathrm{H_2SiF_6}+\mathrm{H_2}\uparrow] \tag{4.21}$$

and

$$(1-P)[\mathrm{Si}+4\mathrm{OH}^{-}+6\mathrm{HF}+4\mathrm{h}^{+} \rightarrow \mathrm{H_2SiF_6}+4\mathrm{H_2O}] \tag{4.22}$$

with a total effective reaction

$$\begin{aligned}\mathrm{Si}+(2P)\mathrm{F}^{-}+(6-2P)\mathrm{HF}+4(1-P)\mathrm{OH}^{-}+(4\text{-}2P)h^{+} \\ \rightarrow \mathrm{H_2SiF_6}+4(1\text{-}P)\mathrm{H_2O}+P\mathrm{H_2}\uparrow .\end{aligned} \tag{4.23}$$

The total reaction has a dissolution valence

$$n_{\mathrm{dv}} = \ 4-2P \tag{4.24}$$

which depends on the probability P of the divalent reaction. The ratio of hydrogen atoms to the dissolved Si atoms depends on the probability P. The probability

$$P = \ \frac{4-n_{\mathrm{dv}}}{2}. \tag{4.25}$$

is determined from Eq. (4.24).

This section has presented a method to determine the number of holes n_{dv} consumed in the electrochemical reaction to dissolve one Si atom. The dissolution valence $n_{\mathrm{dv}} > 2$ indicates that both reactions take place at the same time and leads to the determination of the probability P of each reaction. The probability P is necessary to estimate the correct porosity with the method [26] which depends on evaluation of the amount of evolved hydrogen, while not all dissolved Si atoms corresponds to hydrogen evolution. Only P atoms dissolve with the direct reaction and evolve hydrogen.

The silicon dissolution model in section 4.2.2 and the experimental results in section 4.2.4 indicate that the dissolution valence n_{dv} strongly depends only on the doping concentration of the etched wafer. The dissolution valence n_{dv} depends on the probability of each dissolution reaction, the divalent reaction in Eq. (4.19) and tetravalent reaction in Eq. (4.20). The probability of each reaction depends on the availability of the reactants,

i.e. the probability of the tetravalent reaction in Eq. (4.20) increases by increasing the concentration of OH^- ions. The only source of OH^- ions in the electrolyte is the water ionization, which increases at high electric field intensities near the Si/electrolyte interface, i.e. in the Helmholtz layer. Valance [33] has showed that the Helmholtz potential

$$V_{\mathrm{H}} = \frac{\epsilon_{\mathrm{Si}} d_{\mathrm{H}}}{\epsilon_{\mathrm{H}} L_{\mathrm{D}}} \sqrt{V_{\mathrm{s}}} \tag{4.26}$$

depends on the surface potential V_{s} in Si, which is calculated in chapter 6.3, where

$$L_{\mathrm{D}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}} kT}{q^2 N_{\mathrm{A}}}} \tag{4.27}$$

is the Debye length. Eqs. (4.26) and (4.27) describe the doping dependence of the Helmholtz voltage V_{H}. The electric field intensity inside the Helmholtz layer is given by $V_{\mathrm{H}}/d_{\mathrm{H}}$, where $d_{\mathrm{H}} \approx 3$ Å is the Helmholtz layer thickness.

Figure 4.9 illustrates the doping dependence of the electric field intensity inside the Helmholtz layer. The strong increase of the electric field intensity by increasing the doping concentration yields to an increase of the water ionization and hence increases the concentration of OH^- ions.

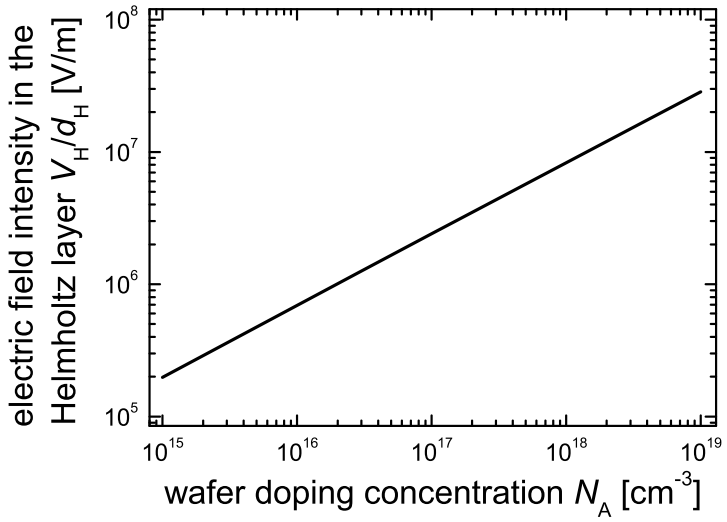

Figure 4.9: *Increasing the doping concentration strongly increases the electric field intensity inside the Helmholtz layer.*

4.3 Summary and Conclusion

This chapter has presented a new nondestructive method, which estimates the porosity of both single- and multi-layer porous Si on a Si wafer by a fast white light interferometer measurement. The method has been used characterize single layer porous Si layers on Si wafers. The dissolution mechanism of porous Si formation by electrochemically etching a heavily doped Si wafer differs from that of etching a lightly doped wafer. Lightly doped Si dissolve by a divalent reaction and evolve hydrogen with a rate equivalent to the Si atomic dissolution rate. In the case of heavily doped wafers, which are the base of the layer transfer technology, a dissolution valence $n_{\mathrm{dv}} = 3$ is observed. The atomic dissolution rate arises directly from the the hydrogen evolution rate, when the dissolution valence is known. The determination method of the dissolution valence has an accuracy $a > 97\ \%$.

Chapter 5 will use the white light interferometer measurement to determine the local porosity of double layer porous Si on a 6" Si wafer to determine the lateral homogeneity of porous Si formation. It experimentally compares the homogeneity of porous Si produced by two different etching setups. The comparison agrees with the simulation of both etching setups and leads to an enhancement of the lateral homogeneity of porous Si on 6" wafers. Therefore, the yield of the layer transfer process increases.

Chapter 5

Layer Transfer Process Enhancement

White light interferometer measurements analyze the local porosity of double layer porous Si on a 6" Si wafer and hence judge the lateral homogeneity of porous Si formation. This chapter experimentally compares the homogeneity of porous Si produced by two different etching setups. The two dimensional conductive medium simulation of both etching cells agrees with the experimentally determined porosity distribution. The new etching setup enhances lateral homogeneity of porous Si on 6" wafers by about 10 %. The lateral homogeneity enhancement of porous Si increases the yield Y of the layer transfer process from $Y < 33$ % to $Y \geq 70$ %.

5.1 Experimental Details

Figures 5.1a and b show a schematic drawing of the etching cell[1]. The cell is filled by the diluted HF solution with concentration $c_{\mathrm{HF}} = 40$ % as described in chapter 3.1. A heavily hoped 6" p-type wafer, with a resistivity ρ between $\rho = 0.01$ and $\rho = 0.016$ Ωcm, is fixed during electrochemical etching by one of two different chucks. The old chuck in Fig. 5.1a fixes the wafer only from the back side by vacuum between two sealing O-rings, thus the complete front surface and the wafer edges are anodized. The new chuck in Fig. 5.1a holds the wafer from both sides at its edges with one O-ring in each side, thus the anodized area is smaller than the wafer area. To prepare a transfer layer, a double porous Si layer is formed by a double step etching process. The resulting structure is annealed[2] at 1100 °C in hydrogen atmosphere for 30 min to form the separation layer and the QMS layers as discussed in chapter 3.2.1.

[1]The etching cell and the wafer chucks are fabricated by LOTUS Systems GmbH, Germany, www.lotus-systems.de

[2]The annealing process is performed by the Institute of Microelectronics Stuttgart (IMS) in the epitaxy champer

Figure 5.2 schematically illustrates the time dependence of the etching current density[3]. The current density time variation shows three regions [2]: In the first region, a low current density J_1 flows for a duration $\triangle t_1$. An upper low porosity p_1 layer forms in this period. The second region shows a linear increase of the current density from J_1 to J_2 in a period $\triangle t_{12}$, where the porosity increases slowly until it reaches p_2. A thin buried high porosity layer forms by holding the current density J_2 for a duration of $\triangle t_2$. The duration $\triangle t_1$ determines the thickness of the upper porous layer d_1, while $\triangle t_2$ determines the thickness of the buried porous layer d_2. Each porosity is controlled by the corresponding current density [2, 116].

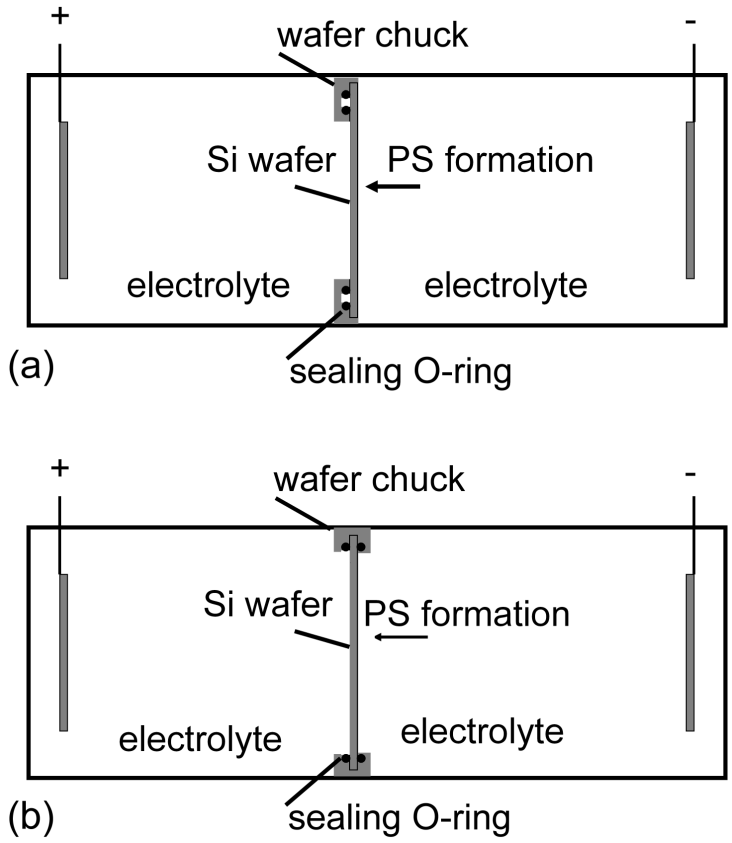

Figure 5.1: *Schema of the etching cell. (a) The old chuck holds the wafer from the back side with vacuum; hence the full front side area is etched. (b) The new chuck fixes the wafer from both sides, therefore the etched area is smaller than the wafer area.*

Table 5.1 lists the values of the current density J_2 for both samples Oi etched by the old chuck, which is in Fig. 5.1a, and samples Ni etched by the the new chuck in Fig. 5.1b, where i = 1 to 10. To analyze the effect of J_2 for both chucks, all other parameters are held constant, namely $J_1 = 10$ mA/cm^2, $\triangle t_1 = 65$ s, $\triangle t_{12} = 2$ s and $\triangle t_2 = 3$ s.

[3]This time dependence form of the etching current density was developed by C. Berge in his PhD [2]

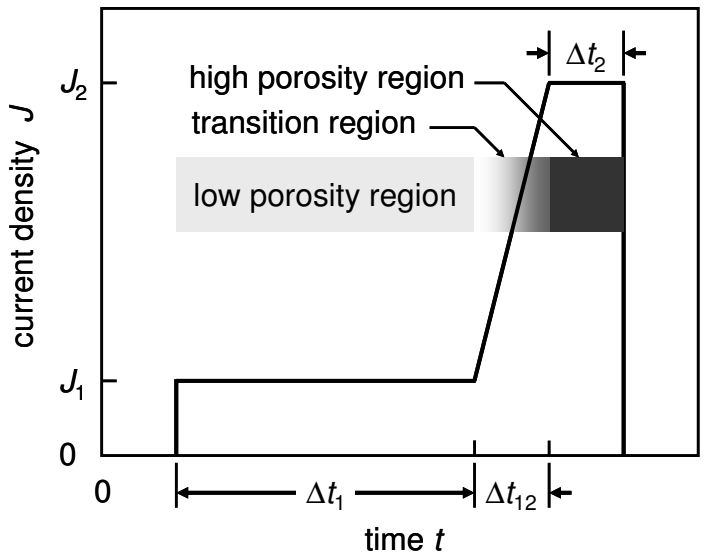

Figure 5.2: *Schema of the etching temporal current density profile.*

This chapter contains two parts: The first part compares the lateral homogeneity[4] of the double porous Si layers etched on a 6" wafer for wafers etched by both chucks. White light interferometer measurements estimate the local porosity as described in chapter 4.1. The second part investigates the effect of each chuck on the mechanical stability[5] of the layer during the different solar cell fabrication processing step. The processing steps are:

1. Epitaxial growth at temperature $T = 1100$ °C. The porous Si structure restructures for 30 min at $T = 1100$ °C, then a 47.4 μm thin Si layer epitaxially grows in about 60 min.

2. Surface texturing takes place in a mixture of KOH solution and isopropyethanol (IPA). The resulted random pyramids enhances the light trapping.

3. Standard RCA cleaning performed at temperature $T = 80$ °C for 20 min. The first standard clean consists of 25 % ammonia (NH_4OH), 30 % hydrogen peroxide (H_2O_2) and water with a volumetric ratio 1:1:5 and takes 10 min. The second standard cleaning consists of 37 % hydrochloric acid (HCL), 30 % hydro gen peroxide (H_2O_2) and water with a volumetric ratio 1:1:8 and takes 10 min.

4. Diffusion of the pn-junction from a phosphoroxidchloride ($POCL_3$) at 830 °C.

5. Phosphorous glass removal in 5 % diluted HF solution.

[4]Chapter 5.2.1 explains the 10 % enhancement of the lateral homogeneity caused by replacing the old wafer chuck by the new one

[5]Chapter 5.2.2 compares the survival capability of layers produced by both etching chucks through the different processing and presents the process yield increase from $Y < 33$ % to $Y \geq 70$ %

6. Drive-in at a temperature T = 1000 °C, which activates more phosphorous atoms of emitter and increases its depth.

Table 5.1: *Current density J_2 for both samples Oi etched by the old chuck in Fig. 5.1a and samples Ni etched by the the new chuck Fig. 5.1b, where i = 1 to 10. All other parameters have constant values, namely J_1 = 10 mA/cm^2, $\triangle t_1$ = 65 s, $\triangle t_{12}$ = 2 s and $\triangle t_2$ = 3 s.*

Sample	J_2 [mA/cm^2]	Sample	J_2 [mA/cm^2]
O1	100	N1	133
O2	120	N2	146
O3	140	N3	160
O4	160	N4	160
O5	160	N5	160
O6	165	N6	173
O7	165	N7	173
O8	170	N8	186
O9	200	N9	186
O10	200	N10	200

5.2 Results and Discussion

The lateral homogeneity of porous Si or of the etching current is the maximum percentage change in each of them along the axis of measurement. The x-axis is taken as a measurement axis and defined on the wafer surface perpendicular to the flat with the origin point in the middle of the wafer. The new chuck enhances the lateral homogeneity by about 10 % as shown in section 5.2.1 and increases the yield Y of the layer transfer process from Y < 30 % to Y > 70 % as shown in section 5.2.2 [46, 136].

5.2.1 Lateral homogeneity enhancement

Figure 5.3 compares the calculated porosities of double porous Si layers on Si wafer for two wafers etched by the different wafer chucks. The local porosity of the double layer porous Si is predicted by white light interferometer measurements as described in chapter

4.1.2. The full area of the 6" wafer A, from the old chuck in Fig. 5.1a, is exposed to the electrolyte, whereas on wafer B, from the new one 5.1b, only a circle of diameter $D = 13$ cm is exposed. Therefore, wafer B has a non-etched one cm wide edge. The heavy line in Fig. 5.3 is a guide to the eye. The lateral homogeneity is defined as the percentage change in porosity along the x axis. Figure 5.3 shows that the new chuck increases the homogeneity of the porosity laterally: The porosity of the buried layer varies by 25 % for wafer O, etched by the old chuck, and by only 15 % for wafer N, etched by the new chuck,. Thus, the new chuck enhances the lateral homogeneity of porous silicon by about 10 %. The the upper layer porosity from the new chuck is also more homogeneous than that from the old chuck.

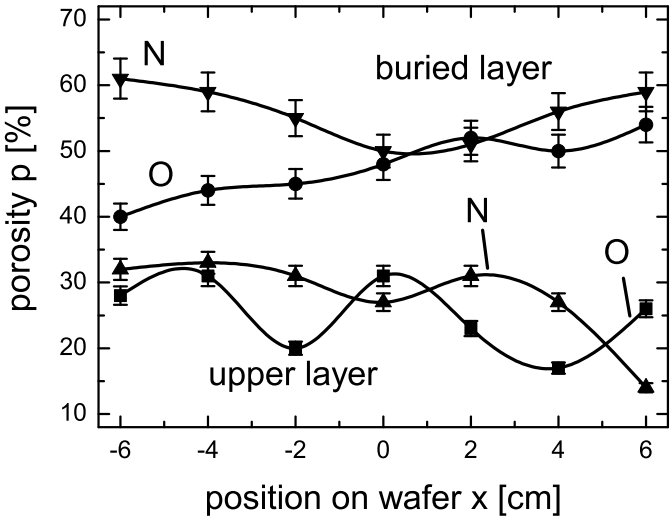

Figure 5.3: *Porosity distribution determined by white light interferometer measurement. The full area of wafer* O *is etched with the old chuck, while the radius of the etched area at wafer* N *from the new chuck is 1 cm smaller than the wafer radius. The wafer's flat is at the right hand side.*

Figure 5.3 shows a U-shape of the porosity spatial distribution for the buried porous layer etched by the new wafer chuck, while the wafer etched by the old chuck has a porosity decrease from the flat side to the opposite side. It is also observed that in some transfer experiments solar cells in the middle of the wafer need larger forces than those near to the etched edge to be removed. To understand and enhance porosity distribution, it is simulated for the old and new cases. The two dimensional conductive medium simulation programm, which is developed by Berge in his Ph.D. thesis [2] is adapted in this work to be suitable also for the new chuck structure as follows:

1. The new wafer chuck in Fig. 5.1b covers the edges of the wafer as a dielectric.

2. In the case of the old chuck in Fig. 5.1a , the wafer flat is defined as an isolation part in one side of the wafer.

The programm is based on solving the two dimensional Poisson's equation, as addressed in Appendix B, numerically by the finite element method (FEM) [137–139] with the appropriate boundary conditions in the etching cell. It calculates the normalized etching current density J_{n} distribution through the wafer diameter.

Figure 5.4 illustrates the calculated normalized etching current density J_{n} as a function of position x. Curve A in Fig. 5.4, which corresponds to curve O in Fig. 5.3 for the wafer etched by the old chuck, shows a normalized etching current density J_{n} decreasing from the flat side to the opposite side. This etching current density decrease explains the estimated buried layer porosity decrease of curve O in Fig. 5.3. Both experiment and simulation deviate from the results presented by Berge [2, 140], who calculated a symmetrical simulated current density similar to curve C in Fig. 5.4. The reason of this deviation is that curve C in Fig. 5.4 corresponds to a wafer etched by the old chuck without taking into account the effect of the wafer flat, while curve A is more realistic as the effect of the wafer flat is taken into account. Therefore, curve A in Fig. 5.4 resembles the experimentally determined porosity distribution, curve O of the buried layer in Fig. 5.3, while curve C in Fig. 5.4 does not.

The simulated current density of the etching cell with the new chuck, curve B in Fig. 5.4 shows a U-shape distribution and resembles the U-shape of curve N in Fig. 5.3. The U-shape of the porosity distribution results in a higher required separation mechanical force of cells in the middle of the wafer than those near to the edge of the etched circle. I ascribe the observed U-shaped porosity distribution of wafers etched by the new wafer chuck in Fig 5.1b to the sudden change of area at the wafer surface, where the etched area is smaller than the electrolyte bulk area.

Figure 5.5 schematically describes the insertion of an insulating tunnel in the cathode side of the etching cell. The tunnel insertion enhances the homogeneity of the etching current distribution as shown in curve D in Fig. 5.4. The new insulating tunnel is fabricated by the company LOTUS Systems GmbH [104] and used with the new chuck in all following etching processes.

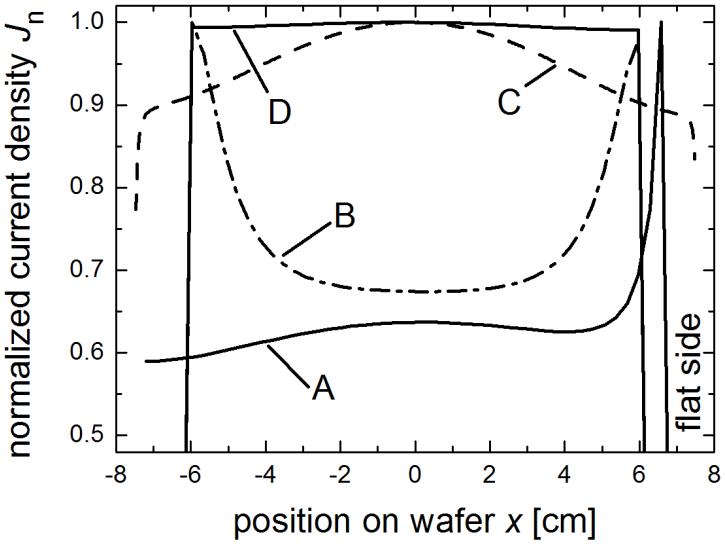

Figure 5.4: *Simulated local normalized etching current density for both old and new porous Si etching cells. Curves A and C correspond to the old chuck, which etches the full area of the cell. The effect of wafer flat is simulated only in curve A. Curves B and D correspond to the new chuck, which allows etching only a circle with a diameter D = 13 cm. Curve D simulate the etching cell with an insulating tunnel with an area equal to the area of the new wafer chuck.*

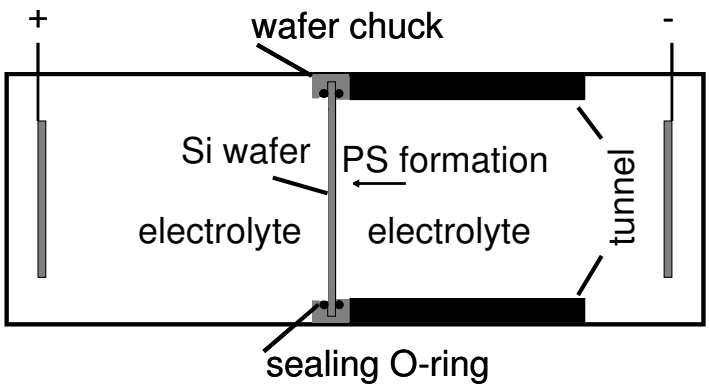

Figure 5.5: *Schema of the new etching cell with the new chuck and insulating tunnel. The new chuck fixes the wafer from both sides, therefore the etched area is smaller than the wafer area. Inserting an insulating tunnel with an area equal to the chuck opening area increases the homogeneity of the etching current density.*

Figures 5.6a, b show scanning electron micrographs of the wafer N, etched by the new chuck, cross section after the epitaxially grown Si on the recrystallized porous Si double layer. Figure 5.6a shows the cross section at the boundary between the etched and non etched areas. Some Si-columns exist between the epitaxy layer and the substrate. Figure 5.6b which is 1 cm away from the boundary in the direction of the wafer center indicates

that the separation layer there has a large cavity without any bridges. The separation layer has a thickness $d = 2.43$ μm much larger than the original thickness of the high porosity layer $d = 300$ nm. This means that the Si thin layer is totally free and only fixed at the edges, where the Si-columns exist. The free Si layer is like a membrane, therefore its separation requires just the release the membrane at its edges from the host wafer.

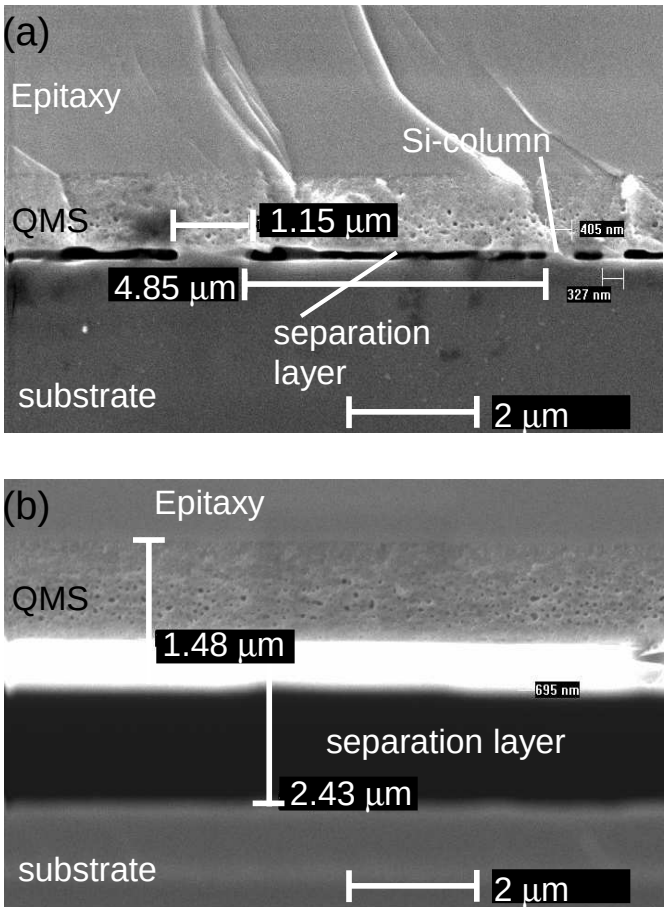

Figure 5.6: *Scanning electron microscope cross section images of wafer B after etching, annealing 30 min at 1100 °C in hydrogen atmosphere and epitaxy growth (a) at the boundary between etched and non-etched areas and (b) 1 cm away from boundary in the direction of wafer center. After heat treatment, the low porosity layer transforms into the quasi-monocrystalline silicon layer (QMS), while the high porosity buried layer transforms into the separation layer. The separation layer does not contain Si-columns throughout the wafer except at the edges of the etched area.*

5.2.2 Process yield increase

Table 5.2 demonstrates the status of each sample described in table 5.1 after each solar cell processing step. The process window is very narrow, as all samples Oi etched by the

old chuck at $J_2 \geq 160$ mA/cm^2 do not survive the solar cell fabrication process. The new chuck increases the processing window of the electrochemical etching process, while all samples Ni etched by the new chuck at $133 \leq J_2 \leq 200$ mA/cm^2 survive the solar cell fabrication process.

Table 5.2: *The status of samples* Oi *etched by the old chuck as well as samples* Ni *etched the new one, with i = 1 to 10, after each solar cell fabrication process. The letter "Y" means that the sample has survived through the process, while "N" means not. The processing window is very narrow, where all samples etched by the old chuck at $J_2 \geq 160$ mA/cm^2 do not survive the solar cell fabrication process. The new wafer chuck increases the processing window, while all samples etched by $133 \leq J_2 \leq 200$ mA/cm^2 survive the solar cell fabrication process.*

Sample	J_2 [mA/cm^2]	Etching	Epitaxy	Texture	RCA	Diffusion	HF etching	Drive-in
O1	100	Y	Y	Y	Y	Y	Y	Y
O2	120	Y	Y	Y	Y	Y	Y	Y
O3	140	Y	Y	Y	Y	Y	Y	Y
O4	160	Y	Y	Y	Y	N		
O5	160	Y	Y	Y	Y	N		
O6	165	Y	Y	N				
O7	165	Y	Y	N				
O8	170	Y	N					
O9	200	Y	N					
O10	200	Y	N					
N1	133	Y	Y	Y	Y	Y	Y	Y
N2	146	Y	Y	Y	Y	Y	Y	Y
N3	160	Y	Y	Y	Y	Y	Y	Y
N4	160	Y	Y	Y	Y	Y	Y	Y
N5	160	Y	Y	Y	Y	Y	Y	Y
N6	173	Y	Y	Y	Y	Y	Y	Y
N7	173	Y	Y	Y	Y	Y	Y	Y
N8	186	Y	Y	Y	Y	Y	Y	Y
N9	186	Y	Y	Y	Y	Y	Y	Y
N10	200	Y	Y	Y	Y	Y	Y	Y

Figure 5.7a pictures a separated 47.4 μm thin-film with a diameter $D = 13$ cm. The wafer is etched by the new wafer chuck, which enhances the lateral homogeneity by about 10 %. The thin Si layer is separated without applying any mechanical force, where the thin Si layer is like a membrane, which is fixed only at edges as shown in Fig. 5.6. Figure 5.7b shows the host 6" wafer after the separation. When I take into account the areal yield of the process, then only 75 % from the wafer are is separated. Therefore, The yield of the layer transfer process with the new chuck is $Y = 75$ % because all samples in table 5.2 survive all solar cell fabrication processes.

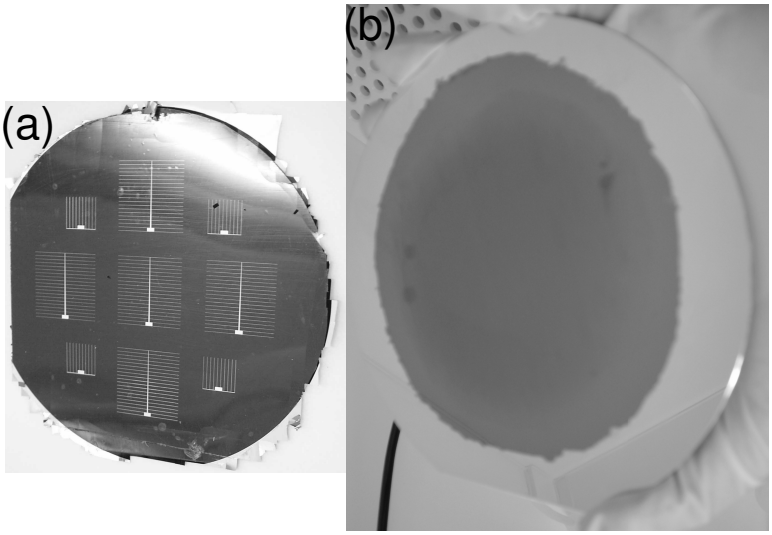

Figure 5.7: *A separated 47.4 μ m thin Si film with diameter $D = 13$ cm. The wafer is etched by the new chuck which increases the lateral homogeneity by 10 %. Scribing the edges of the layer leads to a separation without applying a mechanical force. The cells are completely grown by epitaxy and then covered by an UV−tape to protect cells surfaces during separation. (b) The host 6" wafer after separating the epitaxial layer.*

5.3 Summary and Conclusion

The present chapter introduced a new etching setup for porous Si production. It presents a comparison between the new chuck and the old etching setups from the lateral homogeneity point of view. White light interferometer measurements determine the local porosity on 6" wafers and hence the lateral porosity distribution. A new chuck enhances the lateral homogeneity of porous Si by bout 10 %. The resulted distributions of the porosity on the 6" wafer resembles the two dimensional conductive media simulation of both old and new cells. The new chuck has the disadvantage that only 75 % of the wafer

area is used, where this area is the exposed area to the electrolyte during porous Si formation. Nevertheless, the yield Y of the total layer transfer process is increased from $Y < 33$ % to $Y \geq 70$ % by replacing the wafer chuck used during porous Si formation. The 75 % area losses can be optimized by decreasing the non-etched area in the chuck. The problem is that the decrease the holding edge of the chuck affects the insulation quality O-ring sealing.

Chapter 6

Selective Porous Silicon Formation

Different Si wafers show different response when exposed to HF from both sides in an electrochemical reaction. This chapter studies experimentally as well as theoretically the effect of both the front side and the back side doping of a Si wafer immersed in HF on the electrochemical reaction. The experiment results in three important conclusions: i) Increased front surface doping decreases the voltage required for a certain current density flow. ii) Increased back side doping decreases the voltage required for flowing a certain current density. iii) Local n-type regions mask p-type wafers against porous Si formation in dark. The present chapter introduces also a model of the Si/HF surface. On one hand, the front surface interface is under forward bias and considered as a Schottky diode. On the other hand, the current flows through the back side interface by tunneling. The model agrees well with the experiment.

Finally, I explain the concept of the electrochemical reaction selectivity. The higher selectivity means lower required potential brings holes from the bulk to the interface of SI/HF. As holes are required for the electrochemical reaction, the reaction takes place where the holes are brought easier, i.e. where the selectivity is higher. In the case of p-type Si, the surface potential controls the hole flow. In contrast, in the case of an n-type doped island on the surface of a p-type wafer, the pn-junction potential controls the hole flow and not the surface potential and not the surface potential. Therefore, p-type Si has a higher electrochemical etching selectivity than p^+-type Si. In addition, a p-type region has a higher electrochemical etching selectivity in the dark than n-type doped regions.

6.1 Experimental Details

Figures 6.1a to f illustrate six different 6" wafer types. The heavily doped reference p^+-type wafers in Fig. 6.1a are standard wafers for the transfer process at *ipe* and have a resistivity between ρ between $\rho = 0.01$ and $\rho = 0.016$ Ωcm, which corresponds to boron

doping N_A between $N_A = 3.6\times10^{18}$ cm^{-3} and $N_A = 7.4\times10^{18}$ cm^{-3}. Lightly doped p-type wafers in Fig. 6.1b with a resistivity between ρ between $\rho = 0.2$ and $\rho = 0.5$ Ωcm, which corresponds to boron doping N_A between $N_A = 1\times10^{16}$ cm^{-3} and $N_A = 3\times10^{16}$ cm^{-3}. Figure 6.1c shows a lightly doped wafer with a heavily doped thin layer on the front side, while Fig. 6.1d shows the same structure but with the heavily doped layer on the back side. The heavily doped layers are produced by 30 keV ion implanted boron with a dose $D_B = 5\times10^{14}$ cm^{-2}. Figure 6.1e is a schematic for a lightly doped wafer with two heavily doped layers on both sides. Figure 6.1f is a test structure to investigate the principle of selective electrochemical etching, therefore the half of a heavily doped standard wafer is n-type doped by 30 keV ion implanted phosphorous with a dose $D_P = 10^{15}$ cm^{-2}. All doped areas in this experiment are accomplished by ion implantation due to its high homogeneity. After the ion implantation, all samples are annealed at a high temperature $T = 900$ °C for 30 min to get the final doping profile.

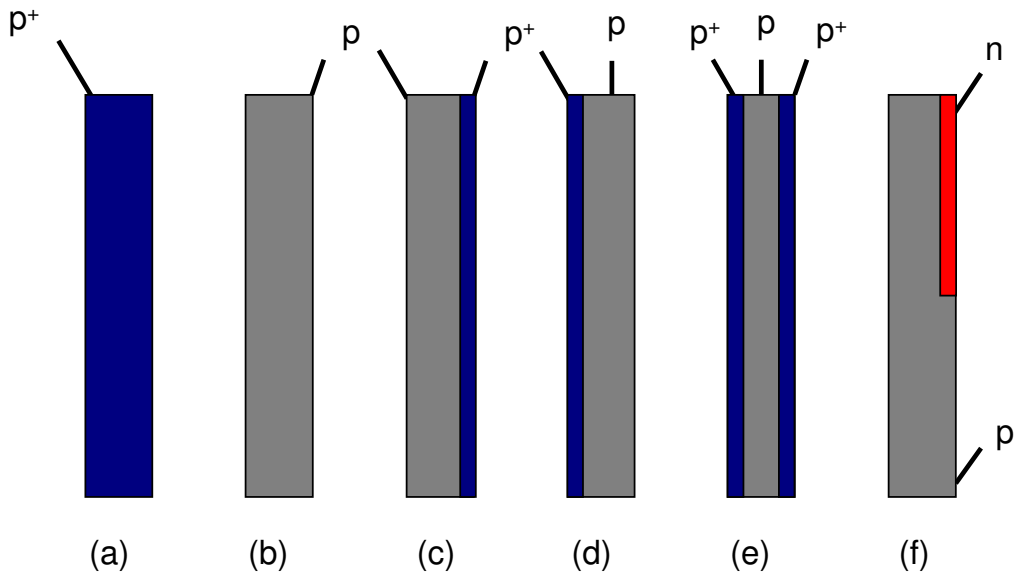

Figure 6.1: *Schema of six different sample structures, which are anodized in HF aqueous solution. The structures compare the behavior of (a) heavily doped p^+-type wafers and (b) lightly doped p-type wafers. In addition, the experiment studies also the anodization behavior of lightly doped p-type wafers with a heavily doped layer on (c) the front side. (d) the back side and (e) both sides. (f) Heavily doped p^+-type wafers with phosphorous doping on their half to study the selective porous Si formation.*

The wafers in Figs. 6.1a to f are anodized in HF with mass concentration $c_{HF} = 40.9$ % in the double-chamber etching cell described in chapter 3.2.1. The electrolyte consists of a mixture of hydrofluoric acid, water and ethanol in a volumetric proportion of 1:1:1. I recall that the front side of the wafer is the side faced by the cathode, while

the back side of the wafer is the side faced by the anode. The experiments record the electrochemical current density J and electrochemical potential V versus time t. Scanning electron microscopic (SEM) images investigate porous Si formation on wafers under different conditions.

6.2 Results and Discussion

Figures 6.2a to f depict the voltage V and current density J profiles versus time t corresponding to wafers in Figs. 6.1a to f. The current source starts to apply the set current after 5 s therefore, in all figures 6.2a to f, the first 5 s has a current density $J = 0$ and a voltage $V = 0$. Figure 6.2a shows the standard etching profile used in the conventional transfer process for heavily doped wafers in Fig. 6.1a. A current density $J = 10$ mA/cm^2 requires a voltage $V = 4.8$ V. The voltage increases slightly in the first 10 s from $V = 4.5$ V to $V = 4.8$ V due to the decrease in the surface area after porous Si formation, while the reaction takes place only at the pore tips. After 65 s the current density increases to $J = 120$ mA/cm^2 to form the high porosity layers. To flow a current density $J = 120$ mA/cm^2, the voltage increases about 4 times to $V = 16$ V.

Figures 6.2b depicts the same etching profile for the lightly doped wafer in Fig. 6.1b. Lightly doped Si requires a higher voltage $V = 25$ V to flow the same $J = 10$ mA/cm^2 than heavily doped wafers. The high current density $J = 120$ mA/cm^2 step requires also a higher voltage, where the voltage reaches its maximum limit $V_{\text{lim}} = 40$ V. Therefore, after porous Si formation, a further voltage increase is not possible, so the current density starts to decay. To understand the current density decay reason, one has to study the effect of both front and back side doping on the current density and voltage relation.

Figure 6.2c illustrates the response of the lightly doped wafer with heavily doped front side in Fig. 6.1c under a set current density $J = 120$ mA/cm^2. It is not possible to flow the $J = 120$ mA/cm^2 within the voltage limit, so a low current density $J = 22$ mA/cm^2 flows at $V = 30$ V. The voltage starts to increase after porous Si formation due to the area decrease till it reaches its limit and then the current density decreases very fast. This means, heavily doped front side requires higher voltage to flow the same current density when the back side is lightly doped.

Figure 6.2d shows the reverse of the previous case, where the back side is heavily doped and the front side is lightly doped as shown in Fig. 6.1d. Etching lightly doped surfaces at $J = 10$ mA/cm^2 requires smaller voltages $V = 5$ V than that of lightly doped back sides. In addition, the voltage limit $V_{\text{lim}} = 40$ V in this case is able to flow $J > 250$

mA/cm^2. This means, the back side must be heavily doped, regardless of the front side to be able to etch the wafer. The voltage is slightly higher than that of heavily doped wafers. To understand if this slight increase results from the surface interaction of the higher resistive substrate, lightly doped wafers with heavily doped both surfaces (Fig. 6.1e) are anodized.

Figure 6.2e investigates the voltage variation during etching the lightly doped wafer with heavily doped both sides, according to Fig. 6.1e, with constant current density J = 10 mA/cm^2. The voltage profile proves that a heavily doped reaction surface requires a higher voltage than a lightly doped surface, regardless of the bulk resistivity and the back side doping, where the voltage starts to decrease after t = 50 s as the reaction surface doping decreased.

Figure 6.3 pictures a cross-sectional SEM photo of the sample in Fig. 6.1e. However, a constant current density J = 10 mA/cm^2 flows through the wafer, a double porous Si layers forms. A low porous Si layer with a thickness d_1 = 1.6 μm forms first and then the porosity increases. The increase of the porosity with the depth y at a constant etching current density is explained only by a decrease of the boron concentration N_A. To find the correlation between porosity and doping, a secondary ion mass spectroscopy (SIMS) measurement determines the doping spatial profile.

Figure 6.4 depicts a measured SIMS profile with the depth y of the wafer from the back side, which is heavily doped by boron ion implantation. Boron segregation at the wafer surface N_A = 7.5×10^{18} cm^{-3} takes place due to the high temperature annealing step after the ion impanation process. The annealing is necessary after the ion implantation step for two reasons:

1. Restore Si crystallinity from the implantation damages.

2. Activate the dopant atoms by placing them into Si substitutional sites.

The boron concentration reaches N_A = 3.5×10^{18} cm^{-3} after 300 nm and stills constant to a depth y = 0.8 μm. N_A starts to decrease after y = 0.8 μm until it reaches N_A = 4×10^{17} cm^{-3} at y = 1.6 μm. When the doping decreases under N_A = 4×10^{17} cm^{-3}, the change of porosity becomes more clear in the SEM photo in in Fig. 6.3.

Finally, the p$^+$-type wafer in Fig. 6.1f, which has a half area n-type region investigates the electrochemical selectivity. The wafer is anodized at J = 10 mA/cm^2 for time t = 65 s. Figure 6.2f indicates that the n-type half area of the wafer does not affect the reaction, where n-type regions do not contribute to the current flow in the dark, because the

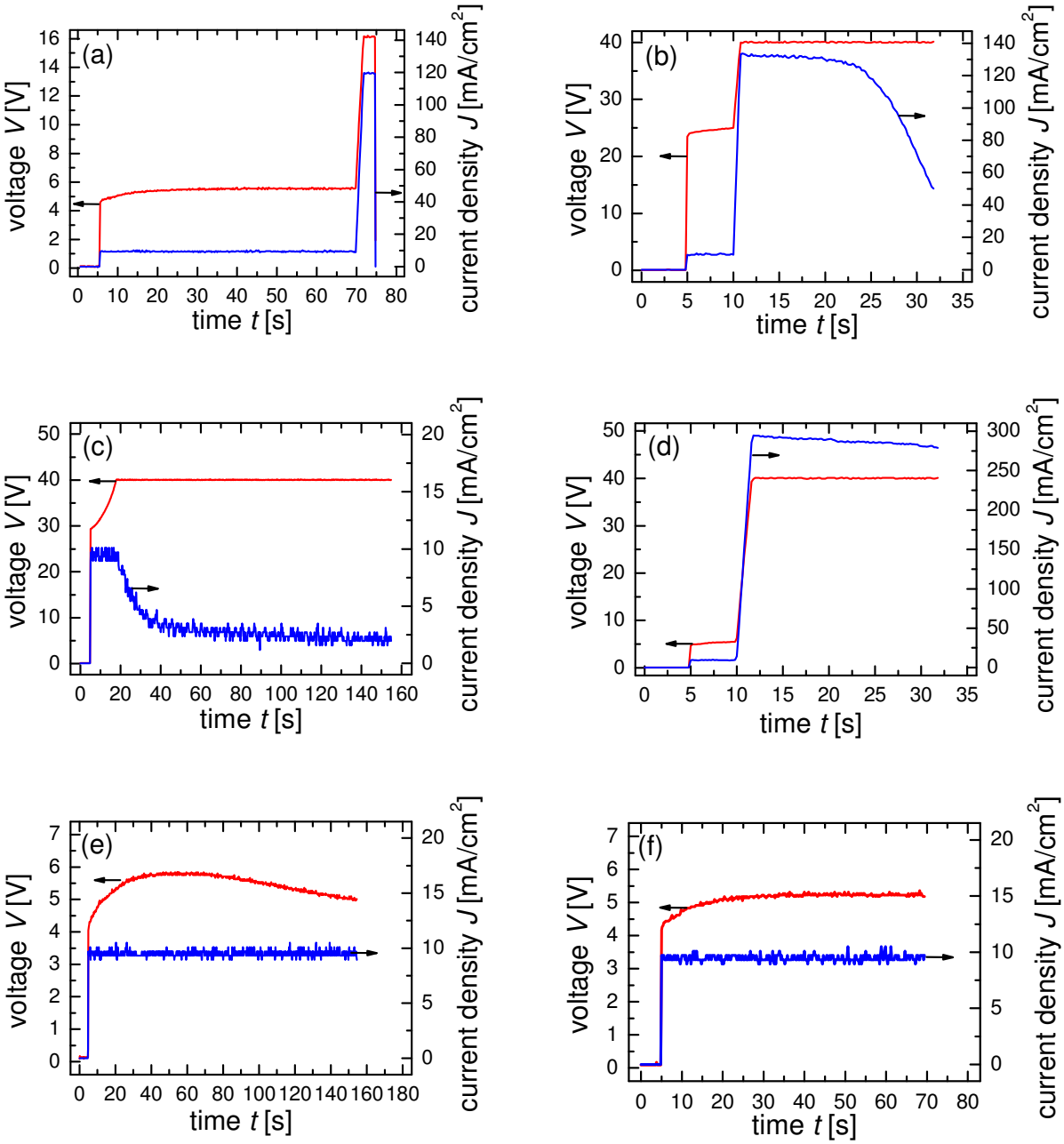

Figure 6.2: *Voltage V and current density J temporal profiles measured during anodizing (a) heavily doped p^+-type wafer, (b) lightly doped p-type wafer, (c) lightly doped doped p-type wafer with heavily doped front side, (d) lightly doped p-type wafer with heavily doped back side, (e) lightly doped p-type wafer with heavily doped both sides and (f) heavily doped p^+-type wafer with phosphorous ion implantation on its half. The maximum limit of the voltage source is $V_{\max} = 40$ V. The current density decays, when higher voltages are required. Thick porous Si layers on lightly doped wafers is only achievable with heavily doped back side.*

etching profile is similar to that of a p-type wafer. The selectivity of porous Si formation is observed, where porous Si forms only on the half p^+-type region of the wafer.

Figure 6.5 shows a cross-sectional SEM micrograph of the wafer in Fig. 6.1f at the

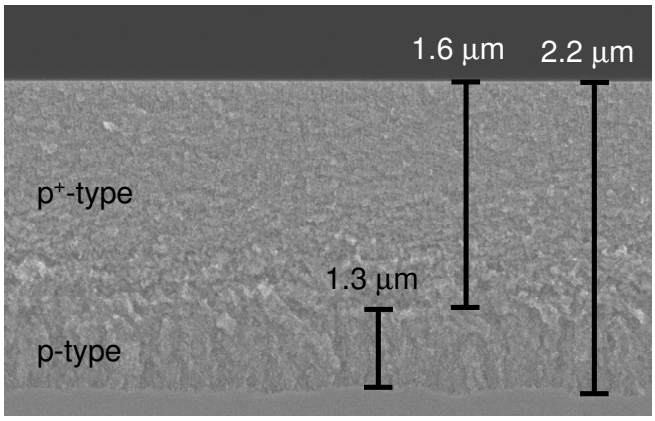

Figure 6.3: *Cross-sectional SEM micrograph of an anodized lightly doped wafer with heavily doped both sides. The wafer is etched by a constant current density $J = 10\ mA/cm^2$, however the porosity increases with depth. The porosity increase is ascribed to the decrease of the doping density of the interaction surface.*

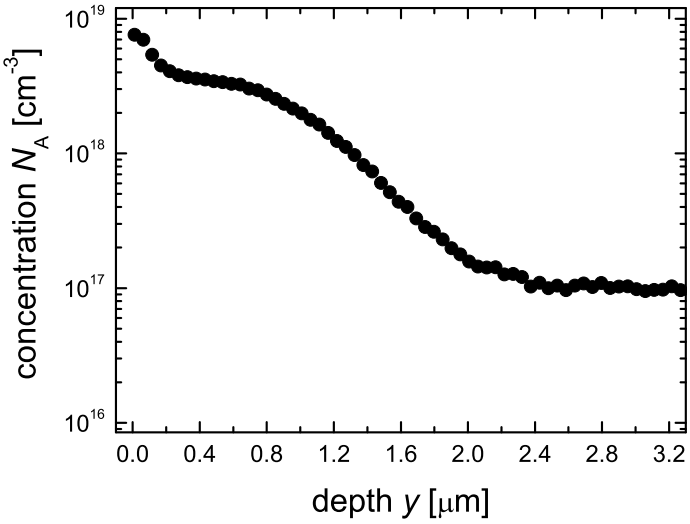

Figure 6.4: *SIMS measurement of boron ion implantation profile. The decrease of the boron concentration N_A with the depth y explains the increase of the porosity of the sample shown in Fig. 6.3.*

boundary between n-type and p^+-type regions. Porous Si forms in the p-type at the right hand side, while no porous Si forms in the n-type region at the left hand side. The n-type region does not only resist against porous Si formation, but it masks also the p^+-type bulk beneath it. Therefore, the higher electrochemical etching selectivity of p-type Si compared

to than of n-type Si in the dark enables the use of n-type doped regions as a masking layer during porous Si formation on p-type wafers. The 1.8 μm under-etching limits the minimum width of the n-type region. The depth of porous Si is significantly larger than the normal depth observed for p^+-type wafers without n-type masking. To investigate the higher rate of porous Si formation, SEM measurements are performed away from the pn-junction. At 5 mm away from the junction the porous Si layer thickness amounts to $d_{5\ \mathrm{mm}} = 3\ \mu$m. At 10 mm away from the junction the porous Si layer thickness decreases to $d_{10\ \mathrm{mm}} = 2.4\ \mu$m. The depth of porous Si decreases with the increase of the distance from the pn-junction until it reaches the usual value $d = 1.5\ \mu$m achieved always under these etching conditions. I conclude from this result that the n-type region causes additional inhomogeneities of porous Si depth due to the inhomogeneity of the hole current density. To avoid this effect, the n-type region has to be as thin as possible, but larger than the under-etching length. Therefore, chapter 7 optimizes the n-type laser doped regions, which are used to selectively form porous Si.

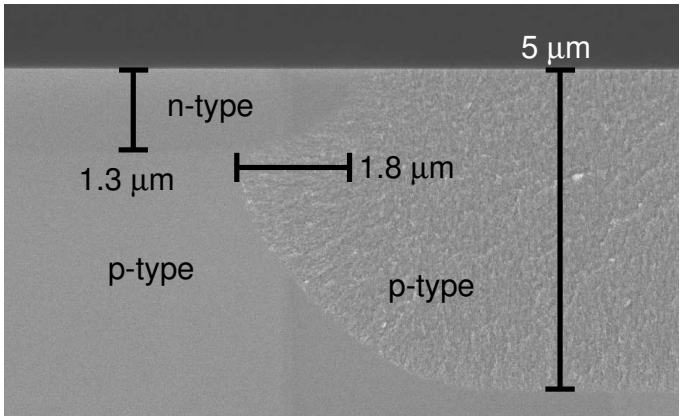

Figure 6.5: *SEM photo of n-type masking during porous Si formation on a p-type wafer. The higher electrochemical etching selectivity of p-type compared to n-type Si in the dark enables the use of n-type doped regions as a masking layer during porous Si formation on p-type wafers. Porous Si does not form neither in the n-type region nor in the p-type region, which is under the diffused n-type region. The 1.8 μm under-etching limits the minimum width of the n-type region.*

Conclusions

This experiment yields three important conclusions:

1. Increased front surface doping increases the voltage V required for a certain current density J flow.

2. Increased back surface doping decreases the voltage V required for a certain current density J flow.

3. Local n-type regions mask p-type wafers against porous Si formation in the dark.

The experiment leads also to the definition for the selectivity of porous Si formation. The higher selectivity means a lower applied voltage is needed to flow a certain current density. Therefore, p-type Si has a higher selectivity than p^+-type Si. In the case of n-type Si, hole generation is necessary to react at the surface. Hence, n-type Si does not react with the electrolyte in the dark. The next section explains the selectivity more in details based on modeling the interface between Si and HF.

6.3 Modeling the Si/HF Interface

6.3.1 p-type silicon

Figures 6.6a and b picture schematic band diagrams of p-type Si and electrolyte, HF in this case, before and after immersing Si in the solution. Si has an electron affinity χ_e = -4.05 eV is constant, while redox potential of the solution depends on the HF concentration. At zero pH the redox potential is defined as the normal hydrogen electrode with a potential of -4.5 eV with respect to vacuum [141, 142]. The redox potential

$$E_{\text{redox}} = -4.5 \text{ eV} + 0.059 \text{ pH eV} \tag{6.1}$$

shifts towards more positive values by 59 meV/pH [143].

After immersion of Si into HF the electrolyte in the dark, the Si Fermi-level E_F and the redox potential level E_{redox} at the interface are brought to the same energy level [11]. Figures 6.6b show a band bending of both the valence band edge E_V and the conduction band edge E_C to maintain the electron affinity χ_e = -4.05 eV of Si at the surface leading to a surface potential

$$V_s = \chi_e - E_{\text{redox}} - (E_c - E_f). \tag{6.2}$$

The band bending shows a potential barrier for holes coming from the Si bulk to the interface. The electrochemical reaction depends mainly on the amount of holes which are able to reach the interface. This means that the electrochemical reaction depends on the surface potential and hence the doping of the Si substrate, where the doping determines the difference between the Fermi-level and the conduction band edge in Eq. (6.2). The

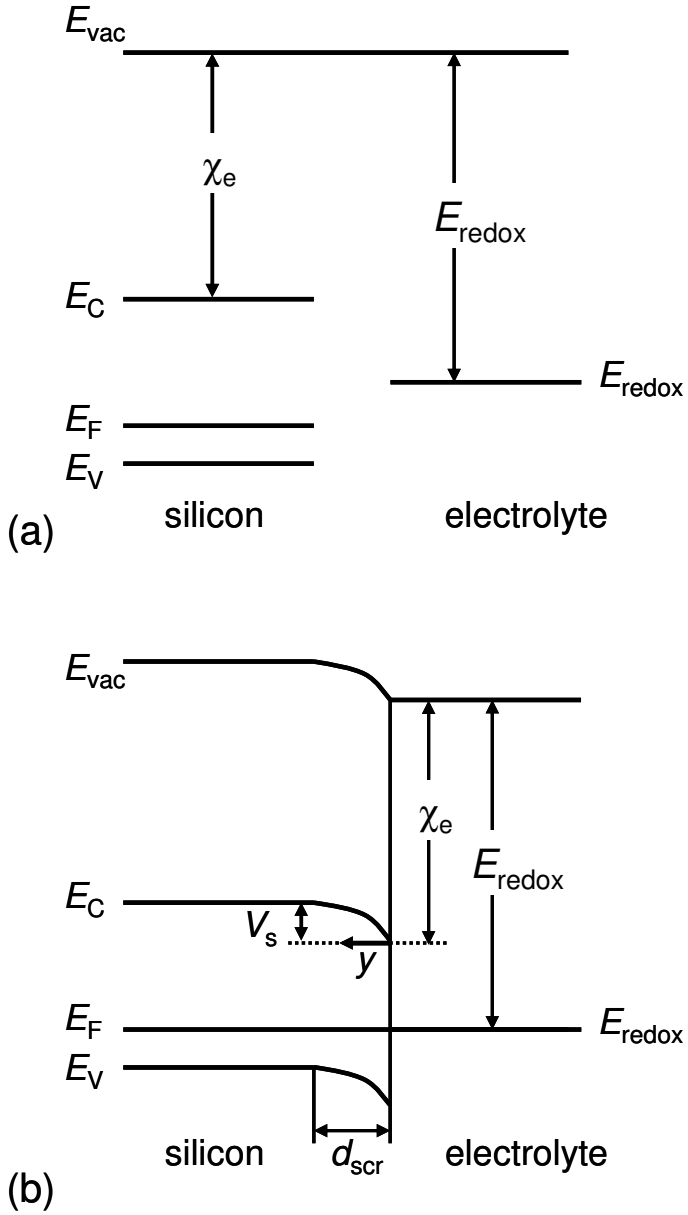

Figure 6.6: *A schematic band diagrams of p-type Si and HF. (a) Before immersing Si in HF. Si has an electron affinity χ_e = -4.05 eV, while redox potential of the solution depends on the HF concentration. At zero pH the redox potential is defined as the normal hydrogen electrode with a potential of -4.5 eV with respect to vacuum. (b) After immersing Si into HF in the dark, the Si Fermi-level E_F and the redox potential level E_{redox} have the same energy level. The electron affinity at Si surface does not change. Therefore, a band bending results in a surface potential V_s.*

HF concentration also affects the surface potential V_s, while it affects the redox potential according to Eq. (6.1).

Figure 6.7 depicts the variation of the surface potential V_s as a function of the acceptor doping N_A calculated at different pH values. The model calculates the difference between

E_C and E_F in Eq. (6.2) from the carrier concentration according to the Fermi-Dirac distribution as the Boltzmann approximation is not valid at high doping concentrations. Decreasing pH value from pH = 2.3 for pure HF [141] to pH = 0 decreases the potential barrier by about $\triangle V_s \approx 140$ meV. On one hand, if the Si electrode acts as an anode, the barrier height decreases with increased biased voltage and hence the interface works as a forward biased Schottky junction. On the other hand, if the Si electrode is connected as a cathode, the barrier height increases with applied voltage and hence the interface is modeled as a reverse biased Schottky diode. In the etching setup used at *ipe*, both cases take place at the same time during anodizing any wafer, while the wafer is conducted by HF from both sides. The front side is forward biased, while the back side is reverse biased.

Front side

During anodization of a Si wafer, the front side is forward biased and modeled as a Schottky junction [52]. Modeling the Si/HF interface at equilibrium as a Schottky junction according to the thermionic emission theory [144] leads to a saturation current density

$$J_s = A_R T^2 \exp(-\frac{qV_s}{kT}) \tag{6.3}$$

with the richardson's constant

$$A_R = \frac{4\pi q m k^2}{h^2}. \tag{6.4}$$

Higher doping concentrations N_A results in higher surface potential V_s as shown in Fig. 6.7. In addition, Eq. 6.3 shows that increased V_s decreases J_s. Lower J_s leads to a higher required voltage V to flow a certain current density J. Therefore, decreasing the doping N_A lowers the required voltage to flow the same current density with the same back side. This explains the decrease in voltage in Fig. 6.2e after etching time $t = 40$ s, while the HF starts to contact the lightly doped substrate. The model agrees with the first conclusion of the experiment in chapter 6.2, which states that the required voltage to flow a certain current increases by increasing the doping.

Back side

Now to explain the second experimental conclusion in chapter 6.2 based on the proposed model, one has to study the back side of the wafer during etching. The second conclusions states that the required voltage to flow a certain current decreases by increasing the back side doping. The back side of the wafer is reverse biased. Therefore, the barrier height

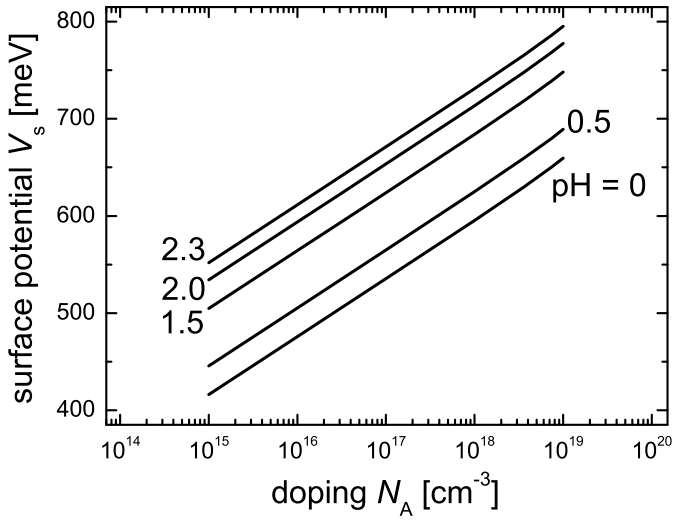

Figure 6.7: *Calculated doping dependent surface potential V_s of p-type Si in contact with HF. The model uses the Fermi-Dirac distribution as the Boltzmann approximation is not valid at high doping concentrations. Decreasing the pH value from pH = 2.3 for pure HF [141] to pH = 0 decreases the potential barrier by about $\triangle V_s \approx 140$ meV.*

increases with the applied voltage. The model assumes that the current flows through the back side by the tunneling [145, 146] mechanism. The model approximates the potential barrier as a triangular barrier with a height V_s and a width equal to the space charge region width d_{scr}. The space charge region width

$$d_{scr} = \sqrt{\frac{2\epsilon_{Si} V_s}{qN_A}} \tag{6.5}$$

results from solving Poisson equation

$$\frac{d^2V}{d^2y} = -\frac{\rho_y}{\epsilon_{Si}} \tag{6.6}$$

in the space charge region under equilibrium with charge density

$$\rho_y = qN_A. \tag{6.7}$$

The tunneling current density [145]

$$J_t = J_{t0} \exp(V_{bs}^{\frac{3}{2}}) \tag{6.8}$$

depends exponentially on the voltage drop across the back side junction V_{bs} to the power of $3/2$ with a constant

$$J_{t0} = qN_A \sqrt{\frac{kT}{2\pi m}} \exp(-\frac{4}{3}\frac{\sqrt{2qm}}{\hbar}\sqrt{\frac{2\epsilon_{Si}}{qN_A}}\ V_s). \tag{6.9}$$

The model calculates the voltage drop across the back side V_{bs} for Si wafers with variable doping density acceptor N_{A} at different set values of the current density J_{set}.

Figure 6.8 illustrates the variation of the voltage drop V_{bs} across the wafer back side in contact with HF with pH = 2.3 as a function of N_{A} at low set current density J_{set} = 10 mA/cm^2 and high current density J_{set} = 500 mA/cm^2. The difference in V_{bs} at the two set current densities is very low. Wafers with back side doping $N_{\mathrm{A}} \leq 2.2\times10^{17}$ cm^{-3} require a voltage drop across the back side $V_{\mathrm{bs}} \geq V_{\mathrm{lim}}$, where V_{lim} = 40 V is the voltage limit of the instruments. Therefore, it is not possible to etch wafers with lightly doped back side as shown in Fig. 6.2c, while the total available voltage is not enough for tunneling at the back side. This result explains the second experimental conclusion, that the back side must be heavily doped to flow current through the wafer.

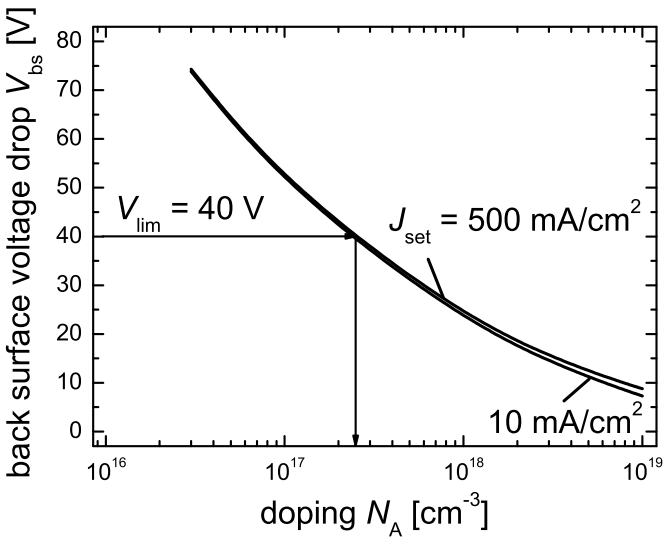

Figure 6.8: *Calculated voltage drop V_{bs} across the wafer back side in contact with HF with pH = 2.3 as a function of the boron doping N_{A} at different set current density J_{set}. It is not possible to etch wafers with back side doping $N_{\mathrm{A}} \leq 2.2\times10^{17}$ cm^{-3} because it requires voltage drop across the back side $V_{\mathrm{bs}} \geq V_{\mathrm{lim}}$.*

6.3.2 n-type silicon

This section explains the third experimental conclusion in chapter 6.2, that n-type region masks p-type wafers against electrochemical reaction. Figure 6.9 illustrates schematically the band diagram of the structure, when a thin n-type layer is inserted between the p-type substrate and the HF solution. In the case of n-type Si/HF interface, the bands bend

upwards at the interface in a way that no barrier for holes exists. In contrast with the p-type case, the band bending helps the holes to reach the interface falling down into the potential well.

Figure 6.10 shows the calculated surface potential V_s for n-type Si/HF as a function of the donor doping N_D at different pH value. While V_s does not represent a barrier, increasing of V_s increases the hole flow to the surface. Decreasing the pH value from pH = 2.3 for pure HF [141] to pH = 0 increases the absolute value of V_s by about $\triangle V_s \approx 140$ meV. This means low concentrated HF solutions would react better with n-type Si. In addition increasing the donor doping would also increase the electrochemical reactivity, where more holes reach the surface.

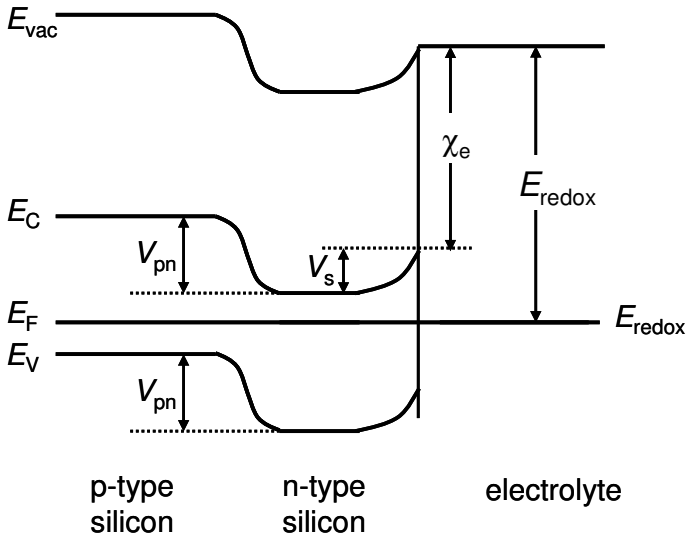

Figure 6.9: *A schematic band diagram of p/n/HF. The bands of n-type Si bend upwards at HF interface in a way that no barrier for holes form, but a well. An n-type region has a lack of holes, therefore an excitation is necessary. The excess holes are generated in the n-type region by at least one of two ways: i) Light absorption. ii) Injection from the p-type substrate under high voltage. Holes in p-type have to overcome the barrier V_{pn}. Therefore, the current flow through this structure in the dark depends on V_{pn} and not on the surface potential V_s as in the case of p-type.*

The introduced interpretation seems to be contradict with the experimental conclusion, that the n-type masked areas do not react with HF. In fact, one finds no contradiction between experiment and model, when one studies the case deeply. The electrochemical reaction requires that holes reach the interface. The band bending at the n-type Si/HF interface results in a simple flow of holes to the interface, but holes in donor doped regions are minority carriers and have a negligible concentration $p \lesssim 10^2$ cm^{-3} in heavily doped

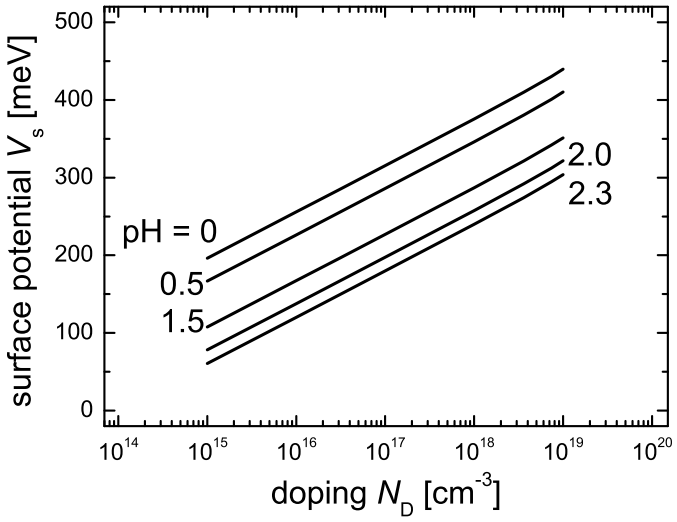

Figure 6.10: *Calculated doping dependent surface potential V_s of n-type Si in contact with HF. The model uses the Fermi-Dirac distribution as the Boltzmann approximation is not valid at high doping concentrations. The potential V_s is not a barrier for holes, but a well. Decreasing pH value from pH = 2.3 for pure HF [141] to pH = 0 increases the absolute value of V_s by about $\triangle V_s \approx 140$ meV.*

n-type regions with $N_D \geq 10^{18}$ cm^{-3}. There are only two ways to generate excess holes in the n-type region:

1. From light absorption.

2. Injection from the p-type substrate.

The first way is excluded, while all experiments in this work are done in the dark. This means, the only way for holes to reach the Si/HF interface is to come from the p-type substrate. Holes have to overcome the pn-junction potential V_{pn}, which is defined in Fig. 6.9. For example, a symmetrical abrupt pn-junction with $N_A = N_D = 10^{18}$ cm^{-3} has $V_{pn} = 970$ meV, which increases by increasing either the p-type substrate or the n-type doping density. Therefore, the potential barrier V_{pn} is the reason of the lower selectivity of an n-type island on a p-type wafer. This barrier enables the masking of a p-type wafer during electrochemical etching, as the surface potential of p-type Si in HF $V_s < 970$ meV as shown in figure 6.10.

6.3.3 Selectivity

The electrochemical reaction takes place selectively in a position, when the total potential energy needed to bring holes to this position is minimum with respect to other positions. Therefore, the selectivity of a certain region is inversely proportional to the threshold voltage V_{th} from the cathode to the anode, which has to be overcome to start the hole-current flow. For two regions on the same wafer, the back surface voltage drop V_{bs} and the voltage drop across the resistance of the electrolyte are equal. Hence, only the front side defines the selectivity of the electrochemical etching. For instance, when a heavily p-type doped Si with doping $N_{\mathrm{A}} = 10^{18}$ cm^{-3} is anodized, a surface potential $V_{\mathrm{s}} = 731.1$ meV forms at the HF interface. When a neighboring region is masked by an n-type island with a doping $N_{\mathrm{A}} = 10^{17}$ cm^{-3}, a potential of $V_{\mathrm{pn}} = 910.8$ meV forms at the pn-junction. This means, the n-type region need higher voltage to permit current flow. Thus, the p-type region will react selectively with HF, while n-type region will not react. Increasing the n-type doping concentration $N_{\mathrm{D}} \geq 3.6{\times}10^{18}$ cm^{-3} increases $V_{\mathrm{pn}} \geq 1$eV and ensures the masking property of the n-type region against the electrochemical reaction.

6.4 Summary and Conclusions

This chapter has experimentally as well as theoretically studied the doping effect of a Si wafer immersed in HF on the electrochemical reaction. The experiment results in three important conclusions: i) Increased front surface doping decreases the voltage required at a certain current density. ii) Increased back side doping decreases the voltage required at a certain current density. iii) Local n-type regions mask p-type wafers against porous Si formation in dark.

The present chapter has introduced a model of the Si/HF surface. The front surface interface is under forward bias and considered as a Schottky diode. The back side interface is under reverse bias and hence the current flows through the it by the tunneling mechanism. The model agrees well with the experimentally concluded three experimental conclusions and explains them in details.

This chapter has also explained the selective electrochemical reaction. The higher selectivity means lower required potential brings holes from bulk to the interface of SI/HF. In the case of p-type silicon, the surface potential controls the flow of holes. Therefore, p-type silicon has a higher selectivity than p^+-type silicon, because the surface potential at a p-type Si/HF is lower than the surface potential at a p^+-type Si/HF interface. In contrary, in the case of n-type doped islands on the surface of a p-type wafer, the pn-

junction potential controls the hole flow and not the surface potential. Therefore, p-type region has a higher selectivity in the dark than n-type doped regions. This means, n-type doped regions mask the wafer against the electrochemical reaction and hence no porous Si forms on and beneath them. The model explains the experimental results of the recorded current density and voltage during electrochemically etching samples with different doping concentrations.

The next chapter uses the n-type masking property to form local porous Si as well as local buried cavities. Applying the selective porous Si formation results in a new separation method, which produces free-standing Si thin-films.

Chapter 7

Free-Standing Silicon Thin-Films

The present chapter introduces a new method, which produces free-standing Si thin-films. The method makes use of the fact that porous Si forms in dark only in p-type regions, while n-type regions act as a mask against the electrochemical reaction. The selective etching is achieved by applying a laser-doped n-type masking layer on the front surface of a p^+-type wafer before the porous Si formation. This chapter experimentally optimizes the laser power for the process to get the minimum under-etching d_{ue} = 1.8 μm and minimum defects in the laser doped masking regions. During the electrochemical etching, porous Si forms only in the bulk wafer and not in the masked areas. The heat treatment results in a locally defined buried continuous cavities, which stop only at the n-type regions. Porous Si upper surface recrystallizes and forms a suitable substrate for high quality thin Si layers. Laser cuts the edges of the Si layers and separates them from the host wafer. A pick-and-place system removes the cells and places them in a holder for further processing.

7.1 Experimental Details

Figures 7.1a to f explain the concept of free-standing Si thin-film fabrication. The concept consists of the following three main processes:

1. **Laser-doped masking layer:**

   Figure 7.1a shows the laser diffusion process performed after applying a precursor layer of the front surface of the host wafer. Czochralski-grown p-type 6" wafers with resistivity ρ between ρ = 0.010 and ρ = 0.016 Ωcm are used as host wafers. Laser-doped locally defined n-type regions act as an etching stop during porous Si formation on a host p-type wafer. The present work uses two different methods of applying the precursor layer:

(i) Spin coating: The wafer front surface is covered by a phosphorous containing liquid by spin-on. Pre-backing the liquid on a hot plate at $T = 300$ °C results in a precursor layer with a thickness $d_{\mathrm{pr}} = 100$ nm.

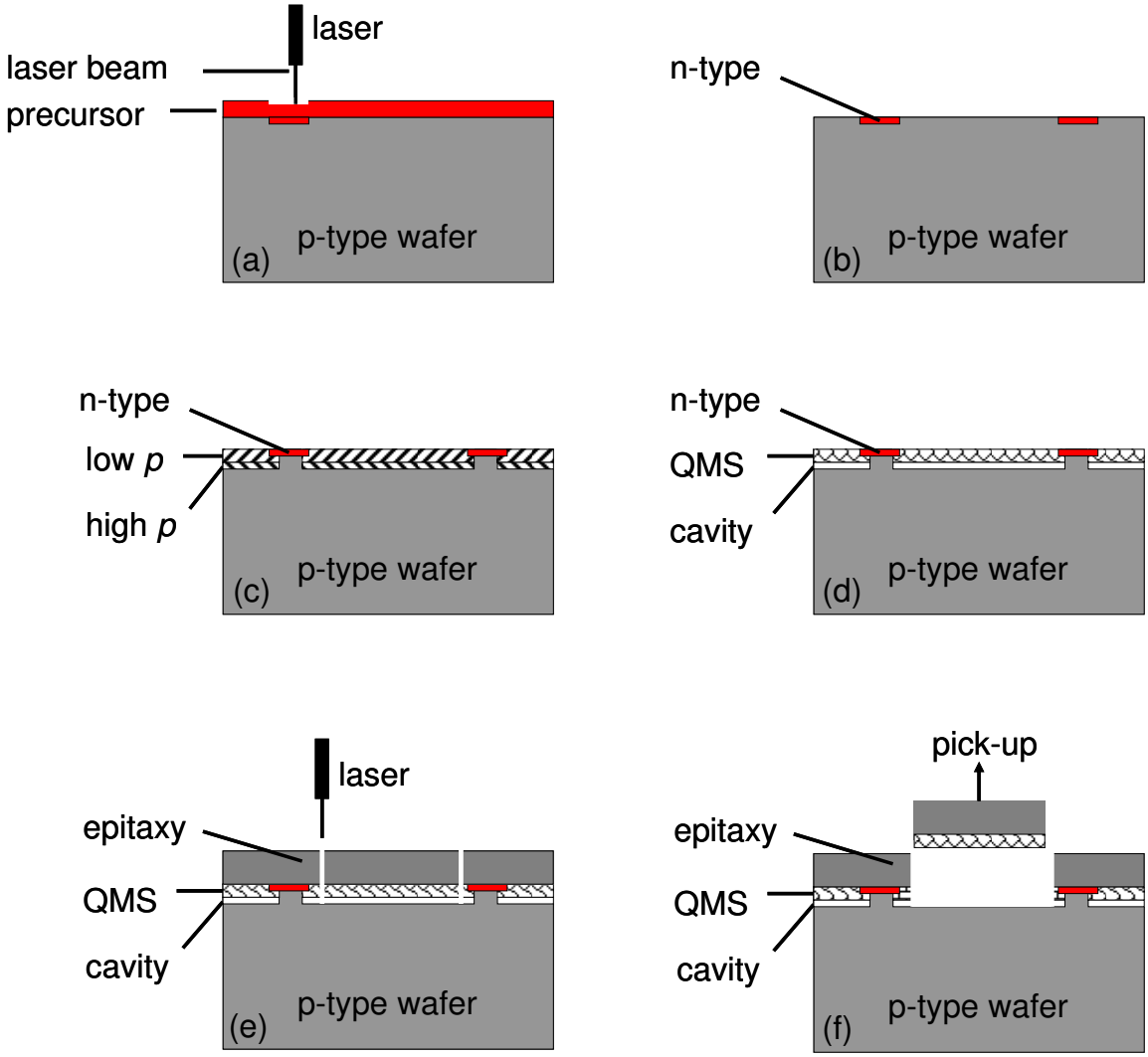

Figure 7.1: *Formation of locally defined buried continuous cavities using a laser doped n-type masking layer. a) A Nd:YVO4 pulsed laser beam structures the phosphorus containing precursor layer by local diffusions. b) After removing the precursor by HF, only the n-type patterned diffused layer remains. c) Low porosity p layer with p $\approx$ 30% is etched electrochemically at low current density J_1. Higher current density J_2 forms a buried high porosity layer with p $>$ 50%. The n-type regions act as a mask during selective etching. d) Annealing at $T = 1100$ °C for 30 min forms the QMS layer. The buried high porosity layer builds a continuous buried cavity. e) During epitaxial growth and device fabrication, the n-type regions fix the structure on the host wafer. The device layer is separated from the host wafer by laser ablations at the edges of the n-type regions. f) The device layer is lifted by a vacuum die.*

(ii) Sputtering: The intermediate target [147] sputtering method deposits phosphorous via a two step sputtering process by the magnetron plasma excitation. This method deposits phosphorous from a solid primary target on a Si wafer and uses it as a secondary target. Consequently, the precursor is sputtered from the secondary target on the host wafer with a thickness $d_{\mathrm{pr}} = 20$ nm.

The laser doping takes place by a pulsed Nd:YVO_4 laser with a wavelength $\lambda = 532$ nm and an average pulse duration of 15 ns. A lens system focuses the laser beam on the wafer surface as a line-beam with a width $w_{\mathrm{laser}} = 5$ μm and a length $l_{\mathrm{laser}} = 200$ μm. The Gaussian pulse intensity distribution results in a pulse energy density

$$E_{\mathrm{p}} = \frac{P}{f_{\mathrm{laser}} w_{\mathrm{laser}} l_{\mathrm{laser}}} \tag{7.1}$$

of the laser beam with laser power P and tuning repetition frequency f_{laser}.

Figure 7.1b depicts the n-type diffused regions after the laser doping and the removal of the rest of the precursor by HF with a mass concentration $c_{\mathrm{HF}} = 5$ %. This work uses the following laser parameters [1]: Laser frequency $f_{\mathrm{laser}} = 5$ kHz, laser beam scanning velocity $v_{\mathrm{b}} = 12$ mm/s, number of iteration $N_{\mathrm{i}} = 100$ and laser power $P = 170$ mW which corresponds, according to Eq. (7.1), to a pulse energy density $E_{\mathrm{p}} = 3.4$ J/cm^2. This chapter optimizes also the laser power to the process by changing it from $P = 160$ mW to $P = 190$ mW and finds that the optimum laser power $P_{\mathrm{opt}} = 170$ mW.

2. **Local buried cavity:**

Figures 7.1c and d describe the formation of the locally defined buried cavity on the host wafer. Figure 7.1c illustrates the electrochemical reaction selectivity effect. The porous Si double layer is formed by electrochemically etching a 6" Si wafer in electrolyte in the dark. The electrolyte consists of a mixture of hydrofluoric acid, water and ethanol in a volumetric proportion of 1:1:1. The upper porous Si layer is etched at low current density $J_1 = 8$ mA/cm^2 and has a low porosity p_1 between $p_1 = 20$ % and $p_1 = 30$ %. A buried porous Si layer with very high porosity $p_2 > 50$ % is etched by increasing the current density to J_2 mA/cm^2. Porous Si forms only in p-type regions, while n-type regions act as a masking layer during the electrochemical etching.

[1] These laser parameters are used by S. Eisele to fabricate solar cell emitters at *ipe*

Figure 7.1d pictures the effect of the high temperature treatment. After the heat treatment in a H_2 atmosphere at $T = 1100$ °C for 30 min, the buried high porosity layer forms a continuous cavity through the wafer except for the n-type laser doped regions. The upper porous layer recrystallizes and forms the so called quasi-monocrystalline Si (QMS) layer, which is a suitable substrate for a high quality epitaxial growth.

3. **Epitaxial layer separation:**

   Figure 7.1e depicts the wafer after the thin Si layer growth. Chemical vapor deposition (CVD) serves to epitaxially deposit about 50 μm thin Si layer on the QMS layer. Laser cuts at the edges of buried cavities enables the separation of the epitaxy layer from the host wafer. Figure 7.1f demonstrates the pick-up concept of the laser separated layers.

7.2 Results and Discussion

Figures 7.2a and b is a photograph of a wafer, which is masked by laser-doped n-type lines. The lines define 2.2 × 2.2 cm^2 square cells. Figure 7.2a shows the wafer after the selective electrochemical etching, where porous Si forms everywhere except at the n-type lines. Figure 7.2b pictures the wafer after an epitaxial growth of a 50 μm thin Si layer. The laser-doped lines are no longer detectable by eye, as Si grows epitaxially on the wafer surface regardless of the doping type of the substrate.

Figures 7.3a and b show scanning electron microscopic (SEM) images of the wafer after the epitaxial growth. Figures 7.3a proves that no single Si-column but a continuous cavity exist under the QMS layer. In contrast, a stable conventional separation layer requires several Si-columns per micron. Figure 7.3b shows the edge of the continuous cavity. The continuous cavity stops at the edge of the laser doped n-type regions, because no porous Si forms in n-type regions in the dark. The continuous cavity ensures the separation of the device layer after the fabrication, while only the n-type regions fix the epitaxy layer. Therefore, the method isolates the two inherently correlated properties of the separation layer (see chapter 3.2.1) from each other, namely the transfer capability on one side and the mechanical stability during the processing on the other side. Isolating the two properties from each other simplifies the optimization of the process.

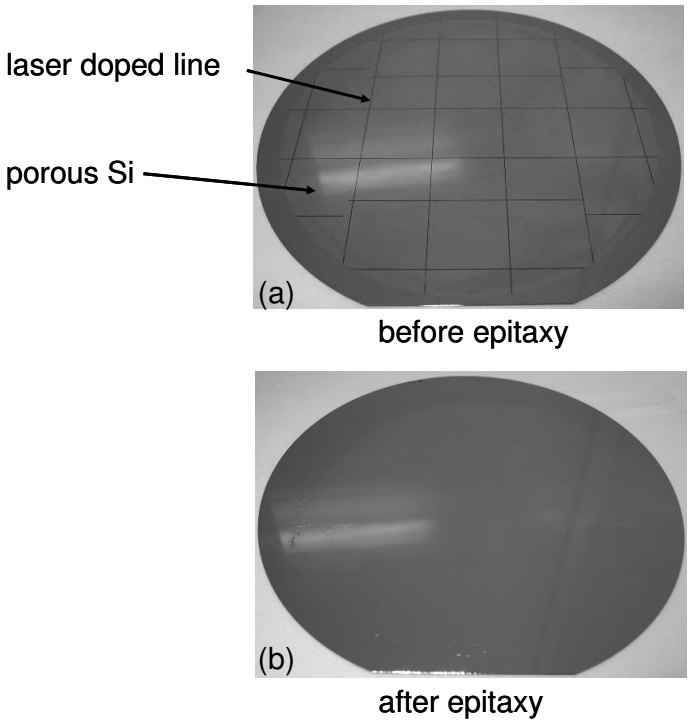

Figure 7.2: *(a) A laser-doped masked 6″ wafer after selective electrochemical etching. The lines represent 2.2 × 2.2 cm^2 patterned cells. (b) The wafer after an epitaxial growth of a 50 μm thin Si layer. The laser-doped lines are no longer visible after the epitaxial growth of about 50 μm thin Si layer.*

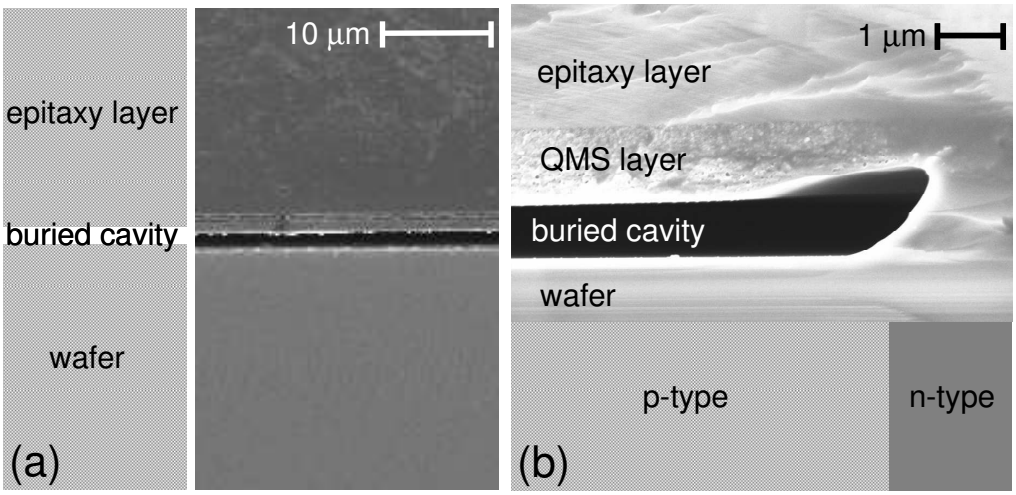

Figure 7.3: *(a)SEM cross-section illustrates the continuous buried cavity under the device layer fabricated by the process in Fig. 7.1a to f. The process fabricates stable layers with no Si columns between the n-type edges. (b) SEM cross-section at the edge of an n-type region proves that the cavity stops at this interface. A 1.2 μm thick QMS layer exists only on the surface of the p-type region, where porous Si forms. The QMS layer serves as a seed for the epitaxial growth of a high quality Si layer. The n-type region acts as a support of the Si layer from the sides during processing.*

Figure 7.3b indicates that about 1 μm under-etching exists. The under-etching is defined as the horizontal distance between the upper porous Si edge and the lower one. The following experiment studies the under-etching and its effects more accurately and optimizes laser power to the process.

7.2.1 Laser power optimization

The present experiment studies the under-etching, which takes place during electrochemical etching of p-type wafer masked with n-type regions. To detect the lateral formation of porous Si easily, a special test structure is needed. The structure consists of a cavity on a the QMS layer and another cavity under the QMS layer, As cavities are detectable by SEM more easier than QMS layers. This experiment uses wafers masked with n-type laser-doped structures with variable laser power P from $P = 160$ mW to $P = 190$ mW. As a precursor, 20 nm thin phosphorous layer is sputtered by the intermediate target method[2].

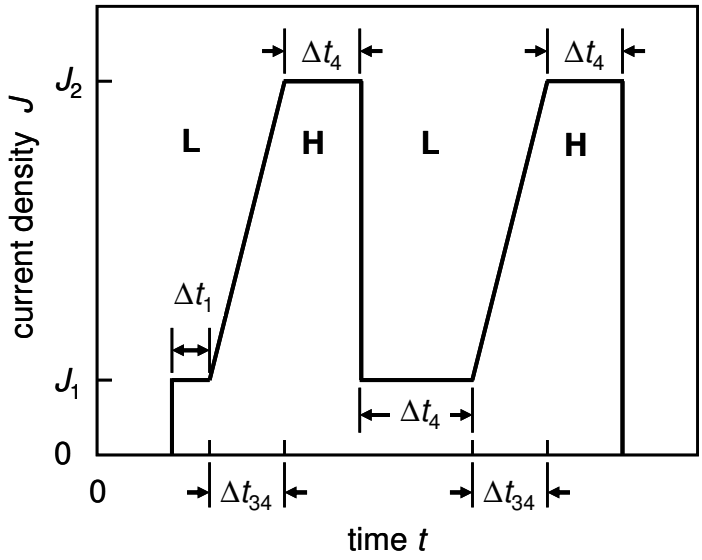

Figure 7.4: *Etching current density profile for two successive buried cavities. A topmost low porosity layer forms at J_1. Increasing the current density to J_2 forms the first high porosity buried layer. The current density decrease decreases the porosity again to form a low porosity buried layer. Increasing the density to J_2 again forms the second high porosity buried layer. Each high porosity layer forms a separate buried cavity after heat treatment.*

Figure 7.4 schematically shows the time profile of the etching current density J which results in the structure **LHLH**, where **L** stands of low porosity layer and **H** for high

[2]The sputtering is performed by S. Eisele at *ipe*

porosity layer. The current etching density $J_1 = 10$ mA/cm^2 for $\triangle t_1 = 10$ s forms a top most thin low porosity Si layer. Increasing the current density to $J_1 = 160$ mA/cm^2 for a short period $\triangle t_1 = 3$ s produces a first high porosity buried layer. The current density decrease to $J_1 = 10$ mA/cm^2 for a period $\triangle t_1 = 65$ s forms a low porosity layer beneath the first buried high porosity layer. The second buried high porosity layer forms by increasing the current density to $J_1 = 160$ mA/cm^2 for $\triangle t_1 = 3$ s again. The high porosity buried layers transform to buried cavities by the high temperature annealing. The lateral displacement of the second buried cavity with respect to the upper one expresses the under-etching during porous Si formation.

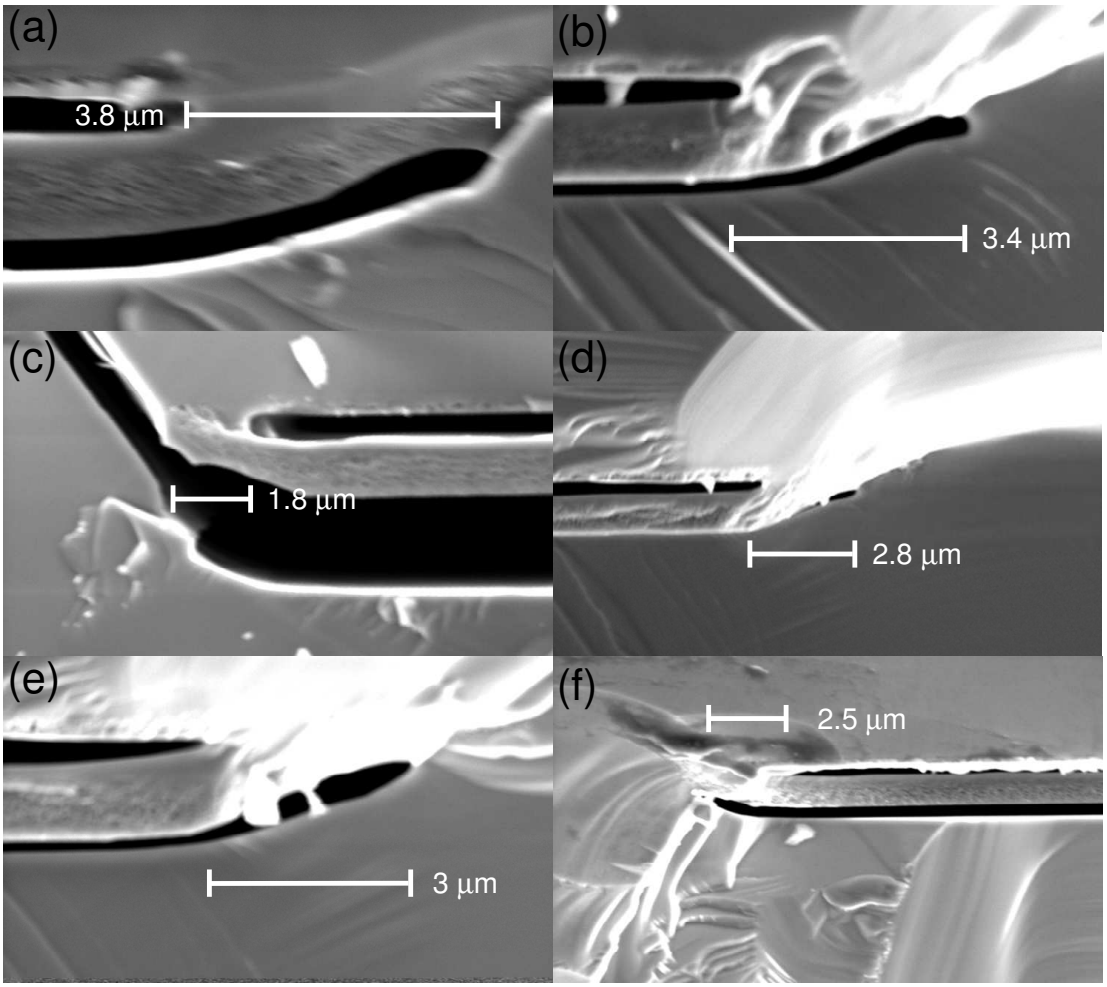

Figure 7.5: *Cross-sectional SEM photos at the boundary between n-type laser-doped region and bulk after heat treatment at $T = 1100$ °C for 30 min and 50 µm thin epitaxial growth. The n-type regions are doped at laser power P (a) $P = 160$ mW. (b) $P = 165$ mW. (c) $P = 170$ mW. (d) $P = 175$ mW. (e) $P = 180$ mW. (f) $P = 190$ mW. The two buried cavities stop at the n-type region boundary, where no porous Si forms. The lower cavity extends horizontally more than the upper one, which means that porous Si forms also horizontally with a certain rate. The cursors in (a) to (f) show the under-etching length d_{ue}.*

Figures 7.5a to f picture cross-sectional scanning electron micrographs at boundaries between n-type laser-doped masking layers and bulk p-type. Samples are processed by varying the laser power P from $P = 160$ mW to $P = 190$ mW. Porous Si forms by etching the samples by the etching current profile in Fig. 7.4. The two buried high porosity layers transforms to separated buried cavities. Both cavities must stop at the edge of the n-type laser doped region, where no porous Si forms. The lower cavity extends horizontally more than the upper one, which means that porous Si forms also horizontally with a certain rate.

The under-etching length d_{ue} is measured as the horizontal distance between the edges of the two cavities in Figs. 7.5a to f. Figure 7.5c shows the minimum under-etching length $d_{\mathrm{ue}} = 1.8$ μm at $P = 170$ mW. Understanding the under-etching effect requires studying the doping profiles of the n-type laser doped masking layers at variable laser power.

Figure 7.6 depicts the phosphorous doping profiles measured by secondary ion mass spectroscopy (SIMS)[3]. Increasing the laser power increases both the junction depth and the doping level. The intersection of each profile with the background acceptor doping of the wafer determines the junction depth d_{j}.

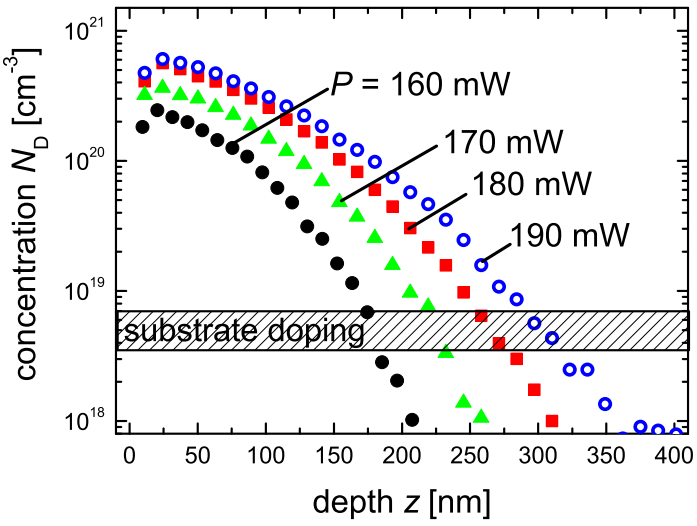

Figure 7.6: *SIMS profiles of n-type laser-doped masking layers formed by variable laser power. Increasing the laser power increases both the junction depth and the doping level.*

Figure 7.7 summarizes the effect of the laser power on both the under-etching and the junction depth. The junction depth increases monotonically by increasing the laser power. Deeper junctions mask better against porous Si formation. Therefore, the under-etching

[3]SIMS measurements done by G. Bilger at *ipe*

length decreases by increasing the laser power with a local minimum at $P = 170$ mW. To choose the optimum laser power and decide the minimum line width, mask feature, more investigations of the n-type regions are necessary. Therefore, I study the cross sections of the n-type regions itself by the scanning electron microscopy.

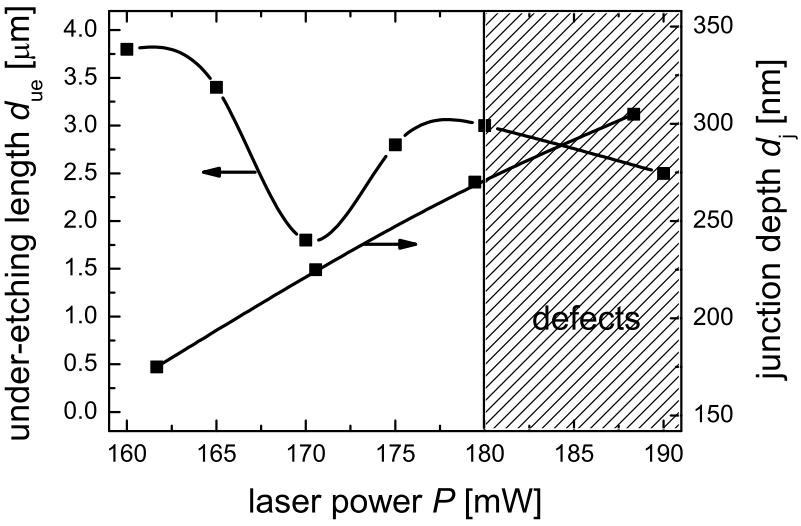

Figure 7.7: *The under-etching length d_{ue} decreases with increasing the laser power with a local minimum at $P = 170$ mW. The junction depth d_j increases by increasing the laser power. Deeper junction masks better against porous Si formation.*

Figures 7.8a and b illustrate the SEM cross sectional images of the n-type laser doped masking layers processed by laser power $P = 180$ mW and $P = 190$ mW. After the high temperature annealing at $T = 1100$ °C for 30 min and the epitaxial growth, Fig. 7.8a indicates that the n-type region at $P = 180$ °C does not mask porous Si formation. The defects in Fig. 7.8a are similar to the laser pulse, which has a width $w_{\text{laser}} = 5$ μm.

Figure 7.8b shows also small cavities in the mask region at laser power $P = 190$ mW. However, increasing the laser power increases the junction depth, and hence enhances the masking properties against porous Si formation. Increasing the laser power $P \geq 180$ mW causes defects and cavities inside the n-type masking layer. Therefore, the optimum laser power is $P = 170$ mW.

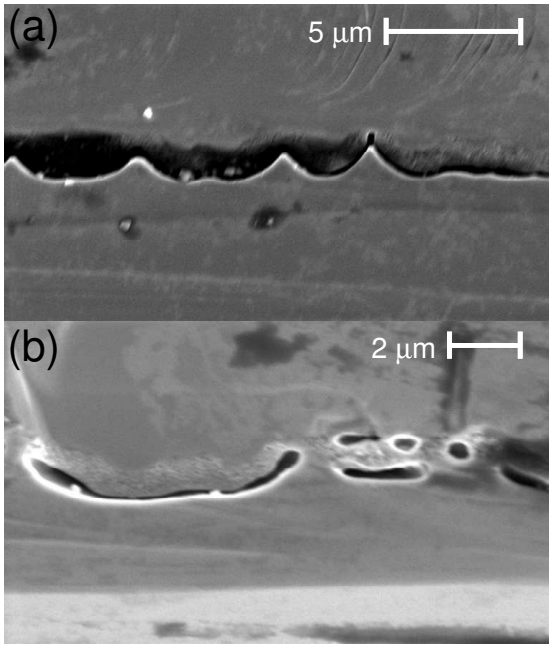

Figure 7.8: *Cross-sectional SEM photos inside the n-type laser-doped region after heat treatment at $T = 1100$ °C for 30 min and 50 µm thin epitaxial growth. Defects in the n-type masking layers are observed only in samples processed with laser power $P \geq 180$ mW. (a) $P = 180$ mW. (b) $P = 190$ mW. The Defects show formed porous Si in the masking layer.*

7.3 Handling of Free-Standing Thin Layers

In the frame of this thesis and with the cooperation with Fraunhofer Institut für Produktionstechnik und Automatisierung, IPA, a handling system[4] of free-standing Si thin-films is designed, realized and tested [148]. The handling system has two main functions:
(i) Pick-up of the cell, which is separated from the host wafer by laser cutting.
(ii) Placing of the removed cell in a holder to simplify the further processing of the cell, e.g. back contact metallization of solar cells.

Figure 7.9a schematically describes the principle of the cell picker. The picker consists of a stainless steel body filled with porous teflon and connected to a pump to generate an under-pressure. The porous teflon distributes the vacuum homogeneously on the thin-film area. In addition, a force sensor enables the measurement of the force required to separate the layer from the host wafer. After removing the thin layer, the picker places it in a magazine.

Figure 7.9b illustrates the working principle of the magazine, in which the cells are

[4]The handling system is designed and realized by Fraunhofer Institut für Produktionstechnik und Automatisierung (IPA) in Germany

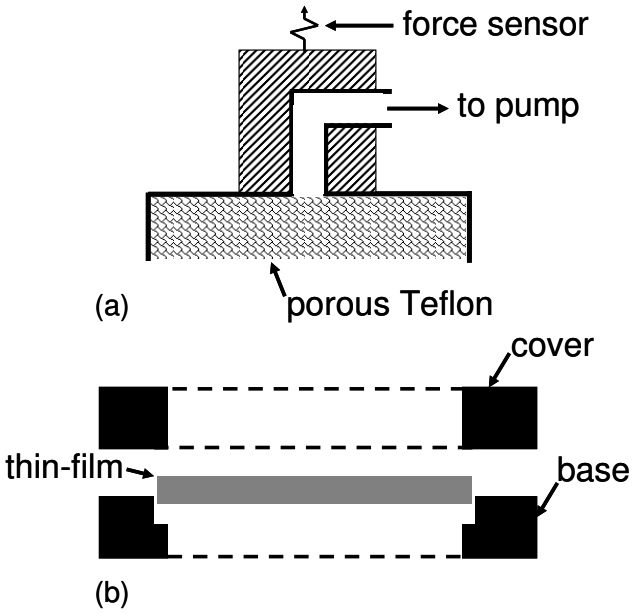

Figure 7.9: *(a) The cell picker consists of a stainless steel body filled by porous teflon. The porous teflon distributes the vacuum homogeneously on the thin-film area. A force sensor enables the measurement of the force required to separate the layer from the host wafer. (b) The Thin-film holder consists of two parts: The lower part, base, has an opening with a lip, on which the thin-film is located. The upper part, cover, has an opening which is smaller than the thin-film area. The holder enables hence the further processing of both sides of the separated thin films.*

placed after the separation and during the further processing. The magazine consists of a base and a cover. The base has an opening slightly larger than the cells and has small lips to support each cell. The upper cover holds cells and simplifies the further processing of them.

Figure 7.10a shows a photo of the realized picker system. Figure 7.10b is a photo of the real magazine with four free-standing Si thin-films placed in it. Pull forces F_p between $F_\mathrm{p} = 0.1$ N and $F_\mathrm{p} = 1.02$ N are necessary to separate 50 μm thin Si layers of area $A = 2.1{\times}2.1$ cm^2.

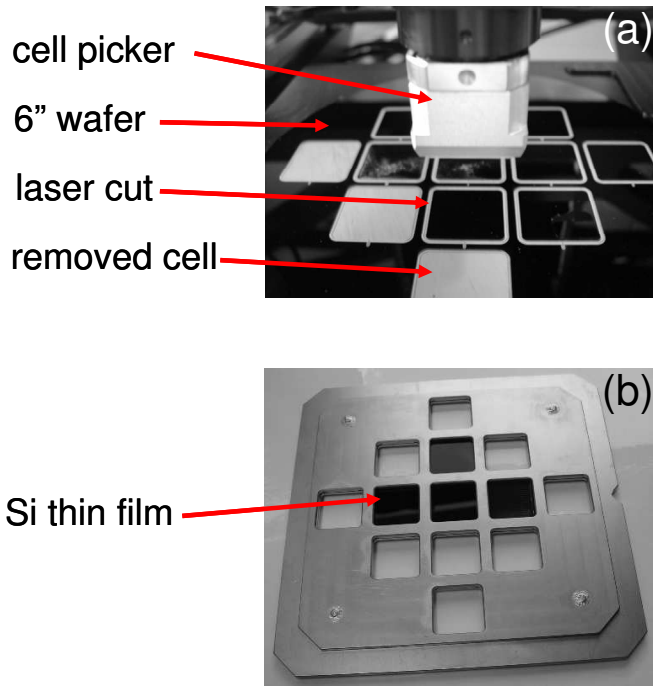

Figure 7.10: *Handling of 20 to 50 μm thin Si free-standing films. (a) The cell picker picks cells up with vacuum. (b) The magazine used for the the further processing of the removed Si thin-films.*

7.4 Summary and Conclusion

This chapter has introduced a new method to produce free-standing Si thin-films. The method makes use of the fact that porous Si forms in dark only in p-type regions, while n-type regions act as a mask against the electrochemical reaction. This fact is known as selective etching. The method is based on applying a laser-doped n-type masking layer on the front surface of a p^+-type wafer before the porous Si formation. During the electrochemical etching, porous Si forms only in the bulk wafer and not in the masked areas. A heat treatment results in a locally defined buried continuous cavities, which stops only at the n-type regions. Epitaxially grown 50 μm thin Si films on the structure is separated by laser from the host wafer and then removed by a specially designed pick-up system. The removed thin films are placed in a magazine for further processing.

This chapter has also optimized the laser power $P_{\text{opt}} = 170$ mW for the process with minimum under-etching length $d_{\text{ue}} = 1.8$ μm. Increasing the laser power increases the junction depth, and hence enhances the masking properties, but it produces defects at $P \geq 180$ mW. Porous Si forms in the location of these defects, and hence the layer loose its masking properties during the electrochemical etching.

The next chapter introduces a comparative study between free-standing thin solar cells

and conventional transfer solar cells. The free-standing cells have the advantage that the absorption losses in glass and resin are avoided. In addition, the resin in the case of the conventional transfer cells limits the back side processing temperature $T \leq 200$ °C after separation from the host wafer.

Chapter 8

Solar Cells

The Si utility U_{Si} is simply the amount of power generated from one gram of Si under the standard conditions and AM1.5G. A Si utility of unity is achieved by using one of two cells: (i) A 100 μm thick Si solar cell with efficiency η = 23.3 %. (ii) A 50 μm thin Si solar cell with efficiency η = 11.6 %. I increase the Si utility by fabricating a 46.5 μm thin module with Si utility U_{Si} = 0.74 W/g higher than that of a 20 % efficient wafer based module. This chapter presents also a 46.5 μm thin free-standing solar cells with an efficiency η = 17.0 % slightly higher than that of the best transfer solar cell a complicated back side passivation step. A further reduction of the cost and process complexity is achieved by growing an epitaxial emitter directly after the epitaxial growth of the base. The low cost process results in a 47.4 μm thin free-standing cell with an efficiency η = 12.3 %.

Thin solar cells save material, when it is produced with a reasonable technique. For example, wafer thinning is not the right way to produce thin Si solar cells. Decreasing the Si amount used in the solar cell, increases the Si utility. The Si utility U_{Si} is simply the amount of power generated from one gram of Si under the standard conditions and AM1.5G spectrum with a radiation intensity $I_{\mathrm{AM1.5G}} = 100$ mW/cm^2. A Si solar cell with an efficiency η, area A, and thickness d_{c} generates a power

$$P = A\eta I_{\mathrm{AM1.5G}} \tag{8.1}$$

and has a Si mass

$$m_{\mathrm{Si}} = Ad_{\mathrm{c}}\rho_{\mathrm{Si}} \tag{8.2}$$

has a Si utility

$$U_{\mathrm{Si}} = \frac{P}{m_{\mathrm{Si}}} = 4.3\frac{\eta[\%]}{d_{\mathrm{c}}[\mu m]} \tag{8.3}$$

with the Si density $\rho_{Si} = 2.33$ g/cm^3.

Figure 8.1 displays the Si utility plots as a function of the cell thickness at variable efficiency. It is clear that thinner Si solar cells achieve higher Si utility with smaller efficiencies. In other words, to achieve a certain Si utility, for example $U_{Si} = 1$ W/g, one has two possibilities: (i) A 100 μm thick Si solar cell with efficiency $\eta = 23.3$ %. (ii) A 50 μm thin Si solar cell with efficiency $\eta = 11.6$ %. High efficiency thin Si solar cells is physically possible, where wafer thinning to a thickness of around 50 μm still enables solar cells with an efficiency $\eta = 21.5$ % [82]. State-of-the-art transfer process enables the fabrication of about 50 μm thin Si solar cells on a glass substrate with an efficiency $\eta = 16.6$ % [118]. However, still the problems of the transfer process limiting the performance of the transferred cell and hinder the module connection.

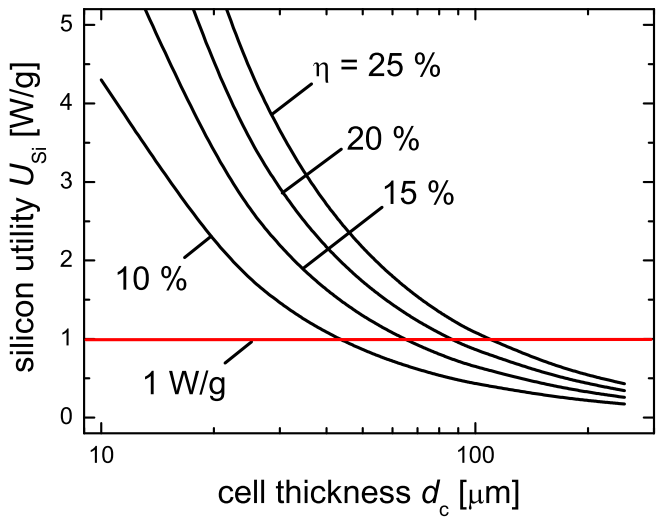

Figure 8.1: *Si utility of solar cells with variable efficiency. Thinner Si solar cells achieve higher Si utility with lower efficiencies.*

Back side laser machining of four cells transferred onto one glass substrate overcome the problem of module connection. A 46.5 μm thin module with efficiency $\eta = 8.1$ % results in a Si utility $U_{Si} \approx 0.74$ W/g higher than a 250 μm thick wafer based module with efficiency $\eta = 20$ %, which shows $U_{Si} \approx 0.34$ W/g. This chapter presents also a 46.5 μm thin free-standing cell with an efficiency $\eta = 17$ %[1]. This free-standing cell shows a Si utility $U_{Si} \approx 1.5$ W/g.

[1]Measured at *ipe* by M. Reuter

8.1 Integrated Mini-Modules

This section introduces a novel method for the integrated module connection of conventional transfer Si solar cells. The method makes use of laser ablation to reach the front side contact from the back side of cells, which are transferred onto one glass substrate. An 8.1 % efficient thin mini-module is fabricated to prove the concept.

8.1.1 Experimental Details

Figure 8.2 illustrates the concept to connect two transfer solar cells, L and R, in series and fabricate a mini-module [120]. After fabricating the solar cells on the epitaxy layer and before transfer, a silver stipe is soldered from one side on the front side grid of cell L and its other side is left outside the cell area. An epoxy resin attaches a glass substrate on the top of the cells. A mechanical force separates the complete area of cells from the wafer. Laser electrically isolates cells from each other and generates an isolated region called no man's land (NML), which is electrically isolated from all cell. In addition, holes are drilled in the NML region using laser exactly on positions of silver stripes to reach them from the back side. The laser parameters are adjusted just to evaporate Si without affecting the silver stripes on the front side. A pulsed excimer laser accomplishes this task by ablation of thin Si layers without affecting the silver strips du to its controllable pulse power P, beam velocity v_{b}, pulse frequency f_{b}, and the turns of beam scanning on Si n_{s}. The optimized laser parameters, which enables the ablation of 50 μm thin transfer layer without affecting the silver beneath it are: $P = 450$ mJ, $v_{\mathrm{b}} = 10$ μm/s, $f_{\mathrm{b}} = 200$ Hz, and $n_{\mathrm{s}} = 10$ turns.

The holes are filled with a conductive glue [149], which brings the front contacts to the back side. Another silver stripe connects the back contact of cell R with the conductive glue in the hole, therefore cells L and R are connected in series. The conductive glue is then annealed at a temperature $T = 120$ °C for 15 min [149]. This method fabricates an 8.1 % efficient integrated mini-module by connecting four 46.5 μm thin cells each has an area $A = 2{\times}2$ cm^2.

8.1.2 Results and discussion

Figure 8.3 pictures a microscopic photo of the no man's land (NML) region between cells L and R. The module is processed by laser with the optimized parameters. The laser isolates cells from each other and successfully drills a 780 μm diameter hole without destroying the silver stripe beneath Si.

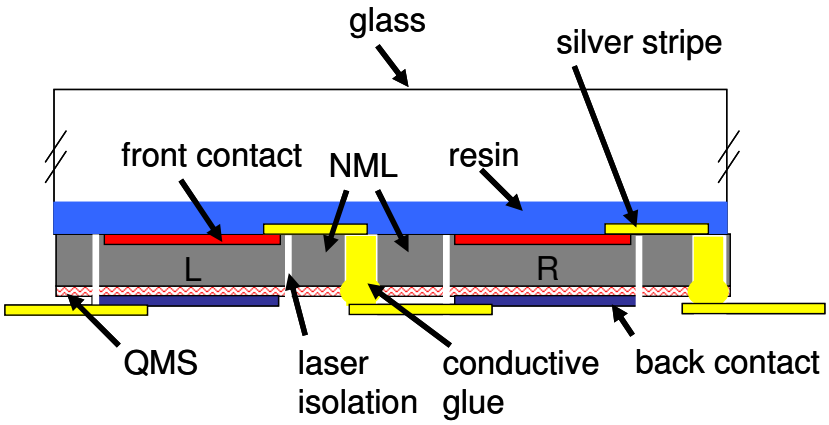

Figure 8.2: *A conceptual schematic of the integrated mini-module connection. The two cells L and R are electrically isolated by laser cuts. The no man's land (NML) is isolated from both cells. The laser drills also a hole in the NML from the back side under the silver stripe, which is connected to the front contact of cell L. The conductive glue brings the front contact of cell L to the back side and connects it to the back contact of cell R.*

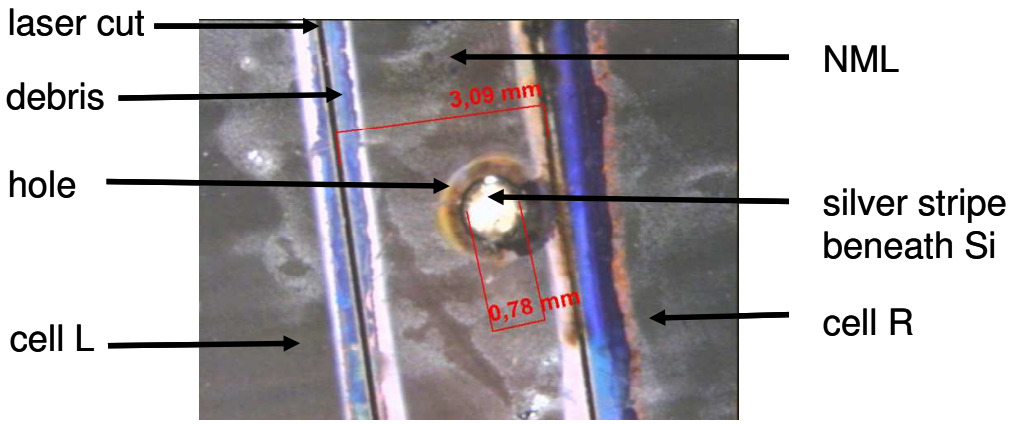

Figure 8.3: *Microscopic photo of the no man's land (NML) region between cells L and R. The module is processed by laser with the optimized parameters: $P = 450$ mJ, $v_b = 10$ μm/s, $f_b = 200$ Hz, and $n_s = 10$ turns. A 780 μm diameter hole is drilled without destroying the silver stripe beneath Si.*

Table 8.1 lists the electrical performance of the fabricated mini-module. The module area is $A_{\mathrm{m}} = 18.5$ cm^2, while the effective cells area is only $A_{\mathrm{eff}} = 16$ cm^2. The module has an open circuit voltage $V_{\mathrm{OC}} = 2.14$ V, which is equivalent to an average cell open circuit voltage $V_{\mathrm{OC}} = 535$ mV, and a short circuit current $I_{\mathrm{SC}} = 129$ mA, which corresponds to a cell short current density $J_{\mathrm{SC}} = 32.3$ mA/cm^2. This method results in a thin module with Si utility $U_{\mathrm{Si}} \approx 0.74$ W/g higher than a 250 μm thick wafer based module with efficiency $\eta = 20$ %, which shows only $U_{\mathrm{Si}} \approx 0.34$ W/g.

Table 8.1: *Results of the thin film Si mini-module determined from the current/coltage characteristics measured under a spectrum similar to AM1.5G. The module consists of four 2×2 cm^2 transfer cells. The four cells are transferred of one glass substrate and connected in series after laser machining from the back side.*

A_{m} [cm^2]	d_{m} [μm]	V_{OC} [V]	I_{SC} [mA]	FF [%]	η [%]
18.5	46.5	2.14	129	55.4	8.1

The method is successful but complicated and the connection of free-standing thin cells would be simpler and industry compatible. Therefore, the present work concentrates mainly on the production of free-standing Si thin-films, see chapter 7. The next section presents the results of free-standing solar cells.

8.2 Free-Standing Solar Cells

This section presents the advantages of the free-standing thin-film Si solar cells over the conventional transfer solar cells [1, 2, 63, 116]. The efficiency η of the free-standing thin-film Si solar cells is boosted up to $\eta = 17$ %[2] just by avoiding the epoxy resin used in the conventional transfer cells. A complex back side contact presented by W. Brendle [1] enables an efficiency $\eta = 16.9$ %[3] slightly lower than the efficiency of the free-standing thin cell with a low cost simple back contact.

8.2.1 Experimental details

The fabrication of the thin monocrystalline Si solar cells starts directly after the restructurization of porous Si in the same chamber, where an epitaxial layer grows on the QMS from $SiHCl_3$ by chemical vapor deposition (CVD). First, a 1.5 μm thin heavily doped p^+-type layer with boron concentration $N_A = 1{\times}10^{19}$ cm^{-3} is grown on the QMS layer. This layer acts as a back surface field (BSF) during the operation of the solar cell to reduce the effect of the high back surface recombination velocity caused by the QMS layer. Second, a 45 μm p-type layer with $N_A = 8{\times}10^{16}$ cm^{-3} is grown to work as an absorber of the cell. The general solar cell fabrication processing sequence precedes as follows:

[2]Presented by M. Reuter [3]

[3]Presented by W. Brendle [1]. The efficiency is independently confirmed by ISE CallLab, Germany

1. Masking the wafer surface by dry thermal oxidation at $T = 1050$ °C with thickness > 200 nm.

2. Lithographic opening of the active cell area.

3. Random pyramids formation to enhance the light trapping by immersing the wafer in a solution of KOH and isopropylethanol (IPA). For the free-standing cells, step 1 and 2 are saved and the fabrication starts by KOH etching, where the edges of the free-standing cell are isolated by laser.

4. RCA cleaning to remove the metallic ions after the KOH etching.

5. Formation of the pn-junction by $POCL_3$ diffusion at $T = 830$ °C. The diffused emitter has a sheet resistance $R_{\mathrm{sh}} \approx 100\ \Omega/\square$.

6. Removal of the phosphorous glass by HF with a concentration of about 5 %.

7. Front surface passivation by 70 nm thin thermal SiO_2. The SiO_2 work also as an antireflection coating only for cells which are not encapsulated. For the capsulated cells, a plasma enhanced chemical vapor deposition deposits a 65 nm thin SiN_x layer with a refractive index $n = 2.05$.

8. Lithographic opening of the front side contact grid.

9. Evaporation of Ti/Pd/Ag and then definition of the front contact grid by a lift-off process. Therefore, the previous lithographic step uses a negative photoresist.

10. At this point, the solar cells are separated from the host wafer and then the back contact is formed.

Figure 8.4 schematically[4] compares the structure of three thin-film Si solar cells [3]. Cells A and B are transferred onto glass substrates using a two component epoxy resin (polytek-301) [2, 114]. Cell C is a free-standing solar cell, which is separated by the pick-up system discussed in chapter 7.3. Al evaporation on the full area of the back side provides the back contact for cells A and C. Cell B has a stacked back side structure, which has been developed by Brendle in his Ph.D. thesis [2]. The optimized back side structure provides low surface recombination velocity, enhancement of light trapping and an acceptable ohmic contact. The back contact is fabricated as follows:

1. Removal of the QMS layer and the heavily doped back surface field by the chemical etching in a diluted HF and HNO_3 mixture [2].

[4]This schematic is taken from [3].

2. Deposition of a thin a-Si:H layer at a temperature $T = 130$ °C. This layer provides a good passivation of the back side, which enables back contact surface recombination $S_b = 15$ cm/s.

3. Deposition of silicon nitride layer, which increases the back side reflection.

4. Evaporation of Al as a back metallization. The silicon nitride/Al system acts as a back side mirror and enhances the red region performance of the cell.

5. Laser fired contacts (LFC) provides point contacts by firing the Al through the nitride layer as well as the a-Si layer to depth of $d_{LFC} = 5.5$ μm in the bulk Si.

6. Annealing of the complete cell at a temperature $T = 220$ °C

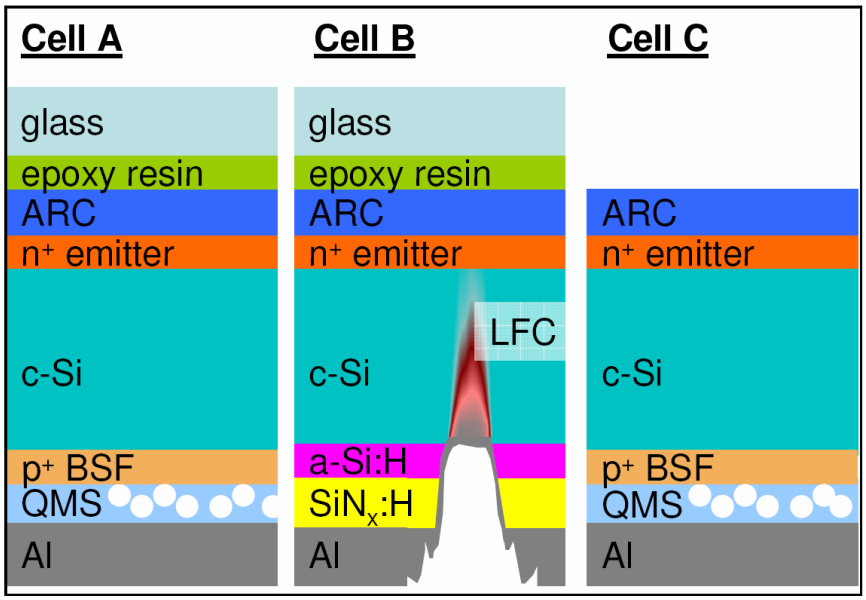

Figure 8.4: ***Cell A:*** *Conventional transfer process with a full area back surface Al metallization. During epitaxy, a heavily doped back surface field is grown on the QMS layer.* ***Cell B:*** *Conventional transfer process with a passivated back side [1]. The back side layer system consists of an a-Si:H layer, SiN_x:H layer and an evaporated Al layer. The dielectric/Al double layer act as a back reflector to enhance the light confinement. A laser fired contact provides the contact of Al to Si through a-Si:H and SiN_x:H layers. The a-Si:H passivats the back side, hence, the QMS layer is etched first. Cells A and B are transferred onto glass by an epoxy resin.* ***Cell C:*** *A free-standing thin-film cell with a full area back surface Al metallization [3].*

The next section compares the performance of the three cells A, B, and C. According to the internal quantum efficiency (IQE) measurements and analysis, cell B with the high performance back side shows an increased diffusion length up to $L_{eff,B} = 120$ μm compared

to cells A and B with $L_{\text{eff}} \approx 70$ μm. The free-standing cell has the advantage that the absorption in the epoxy resin is avoided, which enhances the performance of cell C in the short wavelength range. Characterizing the measured current density/voltage curves of the cells shows an increase of the series resistance of cell B due to its back side contact.

8.2.2 Results and discussion

Table 8.2 lists the electrical performances of the cells A, B, and C described in Fig. 8.4. Cell A has a conversion efficiency $\eta = 16.7$ % with the lowest open circuit voltage $V_{\text{OC}} = 629$ mV and short circuit current density $J_{\text{SC}} = 33.0$ mA/cm^2 [63]. Cell B shows an increase in V_{OC} by $\triangle V_{\text{OC}} = 12$ mV and only a slight 0.5 mA/cm^2 increase in J_{SC}. In spite of the decrease in the FF from $FF_{\text{A}} = 80.5$ % to $FF_{\text{B}} = 78.7$ %, a record cell efficiency $\eta_{\text{B}} = 16.9$ % is achieved [1, 3, 46]. The free standing cell C reaches a slightly higher efficiency $\eta_{\text{C}} = 17.0$ % with a simple and cheap full area Al evaporated contact. The increase of J_{SC} by $\triangle J_{\text{SC}} \approx 6$ mA/cm^2 is due to the avoidance of the resin on the top of the cell, which has a high absorption in the short wave length regime [1, 3].

Table 8.2: *Solar cells output parameters from current density/voltage (J/V) measured under a simulated AM1.5G illumination. The open circuit voltage V_{OC} and the short circuit current density J_{SC} are measured and the fill factor FF and the efficiency η are calculated from the measured J/V curve.*

	A [cm^2]	d [μm]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]
Cell A	2.0	47.6	629	33.0	80.5	16.7†
Cell B	2.0	41.6	641	33.5	78.7	16.9†
Cell C	1.1	46.5	634	36.0	74.6	17.0

† Independently confirmed by ISE CalLab, Germany

The reduced fill factor of the free standing cell $FF_{\text{C}} = 74.6$ % is due to the relatively low parallel resistance probably caused by the laser edge isolation. In addition, the reduced fill factor of cell B compared to cell A is due to the larger series resistance due to the non-optimized point contacts [1]. As described in chapter 2.2.2, Werner plot method [103] determines the equivalent circuit and diode parameters of the three cells A, B, and C. The parameters: the parallel resistance R_{p}, the series resistance R_{s}, the ideality factor, n_{id}, and the reverse saturation current density J_0 are determined as described in chapter 2.2.2.

Figure 8.5 illustrates the Werner plots [103] of the three cells A, B, and C. The linear fitting of the conductance/current density g/J versus the conductance g determines both the series resistance R_s and the ideality factor n_{id} of cells. The smaller x-axis intersection of the plot of cell B indicates the larger series resistance $R_{s,B} = 0.63\ \Omega cm^2$. The slope of the J/V curve at negative bias voltage determines the parallel resistance R_p.

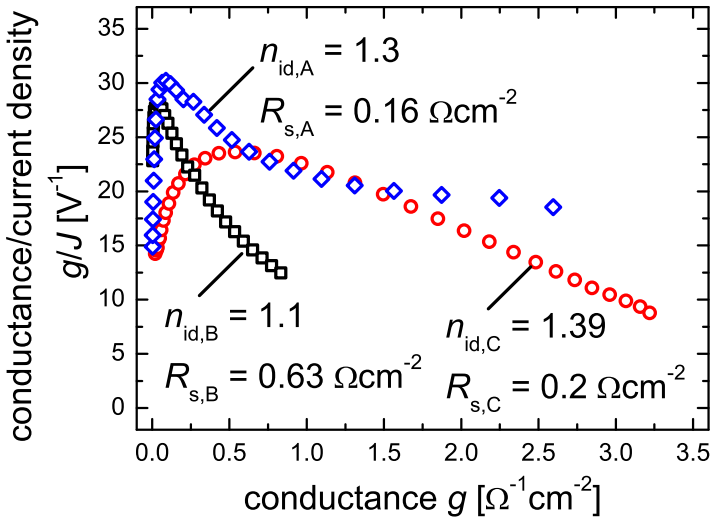

Figure 8.5: *Werner plots of cells A, B, and C determines the ideality factors and series resistances of them. Cells A and C have a relatively large ideality factors larger than that of cell B due to the higher recombination of cells A and C, where their back side is not passivated. The back contact of cell B increases the series resistance of the cell compared to cells A and C.*

Table 8.3 summarizes the determined equivalent circuit components values for the three solar cells A, B, and C. The free-standing cell is fabricated without the planar lithographic definition of the emitter. The cell edge is isolated automatically after the laser cutting and separation. Laser radiation from the front side could probably cause shunts and decreases the parallel resistance. In addition, the best cell with efficiency η = 17.0 % is broken into two pieces during handling, and this could increase the shunt resistance more. The free-standing cell has $R_{p,C} = 39\ k\Omega cm^2$, which is much smaller than those realized by a lithographic planar emitter definition with $R_p \geq 800\ k\Omega cm^2$. However, saving a high temperature process as well as a lithography process is worthy, especially, when the performance of resulted cell is better than those with both expensive processing steps.

The back side structure proposed by Brendle [1] has two effects on the cell: On one

side, the series resistance $R_{\mathrm{s,B}} = 0.63\ \Omega\mathrm{cm}^2$ of cell B is increased due to its non-optimized back side point contacts [1]. On the other hand, cell B has a better back side passivation. Therefore, cell B has reduced ideality factor n_{id} and reverse saturation current density J_0 compared to cell A.

Table 8.3: *Values of the equivalent circuit components of the three solar cells A, B, and C. The parallel resistance of the free-standing cell $R_{p,C}$ is reduced probably due to the laser edge isolation. The series resistance $R_{s,B}$ of cell B is increased due to its back side structure. Cell B has a better back side passivation, therefore its ideality factor n_{id} and reverse saturation current density J_0 are reduced.*

	R_{p} [$\mathrm{k\Omega cm^2}$]	R_{s} [$\mathrm{\Omega cm^2}$]	n_{id} [ ]	J_0 [$\mathrm{mA/cm^2}$]
Cell A	1000	0.16	1.30	2.7×10^{-7}
Cell B	800	0.63	1.10	5.6×10^{-9}
Cell C	39	0.20	1.39	8.0×10^{-7}

Figure 8.6 depicts the internal quantum efficiencies[5] (*IQE*) of cells A, B, and C. The free-standing cell has an enhanced performance in the short wavelength 350 nm $< \lambda <$ 500 nm as it does not contain a resin on its top. Cell B has an enhanced performance in the infrared range (800 nm $< \lambda <$ 1100 nm). The back side reflector reflects the long wavelengths, which are not absorbed during the first path through the cell, again into the cell. The performance of cell C is limited by its low performance back side, where the absorption in the epoxy resin limits the cell B performance. Cell A performance is limited by both effects, low performance back side and high absorption in the resin. The low performance back side means that the reflection in the infrared range is reduced and the recombination at the back side has a high rate. To evaluate the quality of each solar cell quantitatively, the effective diffusion length L_{eff} of the minority charge carriers in the absorber of each cell is extracted from the internal quantum efficiency and the absorbtion length L_α of Si as discussed in chapter 2.2.2.

[5]The internal quantum efficiency is measured by M. Reuter at *ipe*

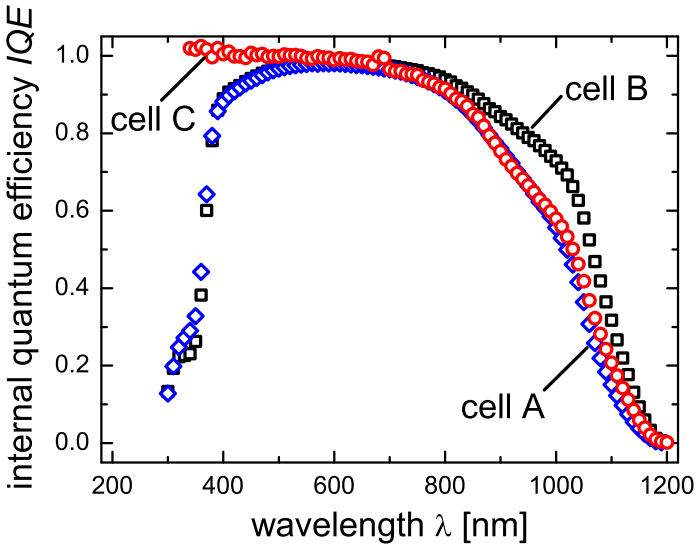

Figure 8.6: *The internal quantum efficiencies of cells A, B, and C. The free-standing cell, C, has an enhanced performance in the short wavelength as it does not contain a resin on its top. Cell B has an enhanced performance in the infrared range. The back side reflector reflects the long wavelengths again, which are not absorbed during the first path through the cell.*

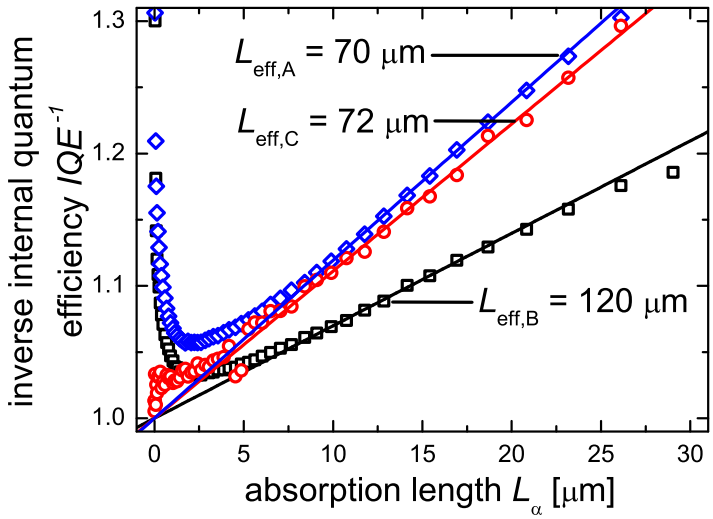

Figure 8.7: *Effective diffusion length L_{eff} calculation for cells A, B and C. Cells A and C have smaller diffusion length $L_{eff} \approx 70\ \mu m$ than that of cell B $L_{eff} = 120\ \mu m$. The enhancement of the diffusion length of Cell B is due to its passivated back side.*

Figure 8.7 extracts the effective diffusion length[6] L_{eff} of electrons in the p-type absorber of the cells A, B, and C. The linear dependence of the inverse quantum efficiency on the

[6]The diffusion length is calculated by M. Reuter (see Ref. [3])

absorption length in the range where $L_\alpha < d_{\text{cell}}$ delivers the effective diffusion length L_{eff} as explained in chapter 2.2.2 [95, 150]. Cells A and C have an effective diffusion length $L_{\text{eff}} \approx 70$ μm smaller than that of cell B $L_{\text{eff,B}} = 120$ μm. The larger diffusion length of cell B is ascribed to the a-Si:H passivated back side after the removal of the QMS and BSF layers.

8.2.3 Further reduction of costs and process complexity

The 10 processing steps listed in section 8.2.2 result in a high performance solar cells, but they consist of two high temperature processes and two lithography steps. The free-standing solar cells in the previous section avoids one high temperature step and one lithography step (steps 1 and 2 in section 8.2.2). Avoidance of these two steps reduces the fabrication complexity, but reduces also the cell performance. However, the deciding factor is not the efficiency, but the cost of one kWh. Therefore, reducing the processing complexity and costs with maintaining a reasonable efficiency decreases the cost of the electricity production. In addition, high temperature processes affect the separation layer properties in the conventional layer transfer process, while many layers are separated during the oxidation and the diffusion processing steps (see chapter 5).

This section achieves aims to a reduction of complexity and cost by saving an additional high temperature step and lithography step, namely the diffusion (step5) and grid opening (step8). The new process grows an epitaxial thin n-type emitter directly after the base epitaxial growth. Therefore, the long time of diffusion and drive-in processes is replaced by a short time epitaxy process. A 0.9 μm thin n-type emitter with phosphorous concentration $N_D = 5\times10^{18}$ cm^{-3} is epitaxially grown directly after the base growth[7]. The total thickness of the resulted thin cell is $d_{\text{cell}} = 47.4$ μm. The target emitter sheet resistance $R_{\text{sh}} = 90$ $\Omega/\square$ is as near as possible to the standard diffused emitter sheet resistance $R_{\text{sh}} = 100$ $\Omega/\square$ used at *ipe* for high efficiency solar cells[8] with the best possible lateral homogeneity.

Free-standing thin-film cells with an epitaxially grown emitter are produced and compared with a reference process. Reference cells are fabricated by growing the same emitter on a 380 thick p-type FZ wafers with resistivity ρ between $\rho = 0.2$ and $\rho = 0.5$. The front side contact grid is not formed by lithography, but by evaporating Ti/Pd/Ag through a shadowing mask. Then a 70 nm thin SiN_x layer is deposited (see step 7 in section 8.2.2).

Table 8.4 lists the mean and standard deviation of the cell parameters of the reference

[7]The epitaxial growth is done by Institute of Microelectronics Stuttgart (IMS) in Germany

[8]IMS group has optimized the epitaxy parameters to get the aimed sheet resistance $R_{\text{sh}} = 90$ $\Omega/\square$

process together with the results of the free-standing thin-film Si solar cell. A 12.3 % efficient thin-film free-standing solar cell is fabricated and compared to a reference process with an average efficiency $\eta_{\text{mean}} = 14.7$ % and standard deviation of the efficiency $\eta_{\text{sd}} = 1.2$ %. The free-standing cell has $V_{\text{OC}} = 602$ mV smaller than that of the record cell with $V_{\text{OC}} = 634$ mV, but in the range of the reference process $V_{\text{OC, mean}} = 607$ mV with a standard deviation $V_{\text{OC, sd}} = 3.1$ mV. The large difference of thickness between the thin cell and the reference cells is probably the reason of the reduced short circuit current density of the thin cell. The thin cell has the same fill factor $FF \approx 69.9$ % as the reference cell. To understand the reduced performance of the thin-film as well as the reference cell, one has to characterize the epitaxially grown emitter.

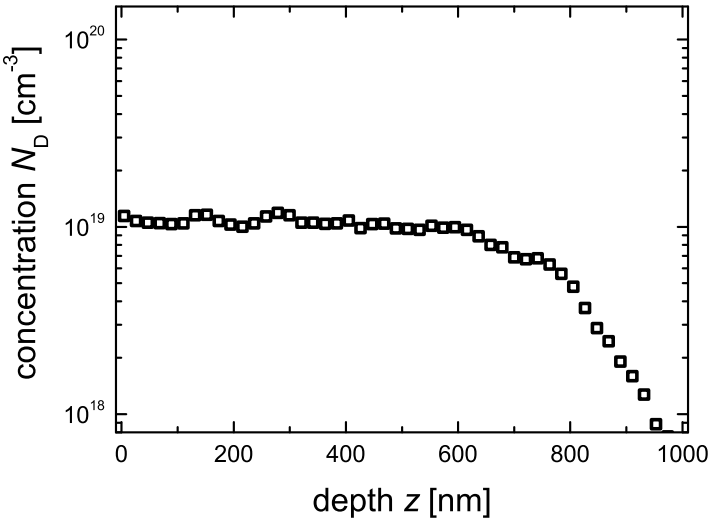

Figure 8.8: *SIMS profile through the epitaxially grown emitter. The emitter profile corresponds to a reduced sheet resistance $R_{sh} = 53\ \Omega/\square$ smaller than that of high efficiency solar cells $R_{sh} = 100\ \Omega/\square$.*

Figure 8.8 shows the measured SIMS[9] profile of the epitaxially grown emitter. The emitter depth is $d_{\text{e}} = 0.9\ \mu$m as designed. However, the phosphorous doping concentration $N_{\text{D}} = 1{\times}10^{19}$ cm^{-3}, which results in a reduced sheet resistance $R_{\text{sh}} = 53\ \Omega/\square$. The reduced sheet resistance is probably the main reason of the low performance of the solar cells with epitaxially grown emitter. In addition, the non-textured surface reduces current density losses. The following analysis separates both effects, the surface quality and the emitter doping, from each other.

[9]SIMS is measured by G. Bilger

Table 8.4: *The output parameters from the current density/voltage (J/V) data measured under a simulated AM1.5G illumination for free standing cells with epitaxially grown emitter compared with a reference cell. The reference cells contains the same epitaxially grown emitter and contacts but on FZ wafers. All cells have area A = 2×2 cm^2. The open circuit voltage V_{OC} and the fill factor FF of the free-standing cell are in the range of the reference values, while the short circuit current density J_{SC} and the efficiency η of the thin free-standing cell are reduced.*

	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]
Mean of the reference process	607	34.6	69.9	14.7
Standard deviation of the reference process	3.1	2.3	1.6	1.2
Free-standing thin cell	602	29.2	69.8	12.3

Losses analysis of the epitaxial emitter:

Table 8.5 compares the the solar cell parameters of cells with and without texture and SiO_2 as a passivation layer of the front surface. The first group[10] of textured cells show a large standard deviation of the open circuit voltage V_{OC}, therefore, a second group is necessary to confirm the obtained values. The second group shows a smaller deviation of the open circuit voltage V_{OC}. The large deviation of the first group stems probably either from the deviation of the wafer resistivity from its specifications, or from the processing tolerances. Table 8.5 shows a strong correlation between the surface texture and the short circuit current density J_{SC}, which is due to the lower reflection of textured surfaces and hence the better light coupling. This analysis leads to that the enhancement of a textured surface is an increase of the short circuit current density by $\triangle J_{\mathrm{SC}} \approx 5$ mA/cm^2. This means that the non-textured surface of reference cells with an epitaxially grown emitter in Table 8.4 does not explain its low performance. The short circuit current density J_{SC} of these cells, in table 8.5, $J_{\mathrm{SC}} = 34.6$ mA/cm^2 is slightly higher than $J_{\mathrm{SC}} = 30$ mA/cm^2 of cells in table 8.5 because the cells with the epitaxial emitter in table 8.4 has a silicon nitride layer as an anti reflection coating, see chapter 2.2.1.

The previous paragraph shows that the surface reflection is not responsible for the low performance of the cells in 8.4 with the epitaxial emitter, because it has a low open circuit voltage $V_{\mathrm{OC}} = 607$ mV and reasonable short circuit current density $J_{\mathrm{SC}} = 30$ mA/cm^2. Therefore, this very low open circuit voltage circuit can not be ascribed to the decrease

[10]Each group consists of 15 cell on the same wafer. Each cell has an area $A = 2\times2$cm^2

of the short circuit current density, but it is due to a decayed physical properties of the cell.

Table 8.5: *Effect of surface texture on the solar cell parameters. Runs 1 and 2 have a textured front surface etched by KOH. Run 2 is taken because the deviation of the V_{OC} of run 1 is high. Surface texture increases the short circuit current density J_{SC} by $\triangle J_{SC} \approx 5\ mA/cm^2$.*

	$V_{\rm OC}$ [mV]	$J_{\rm SC}$ [mA/cm^2]	FF [%]	η [%]
1) with texture	665±35.5	35.5±0.8	80.1±5.3	19±0.45
2) with texture	630±7	36.4±1	75.5±2	17±0.32
3) without texture	650±2.2	30±1.5	79.1±5.4	15.5±1.5

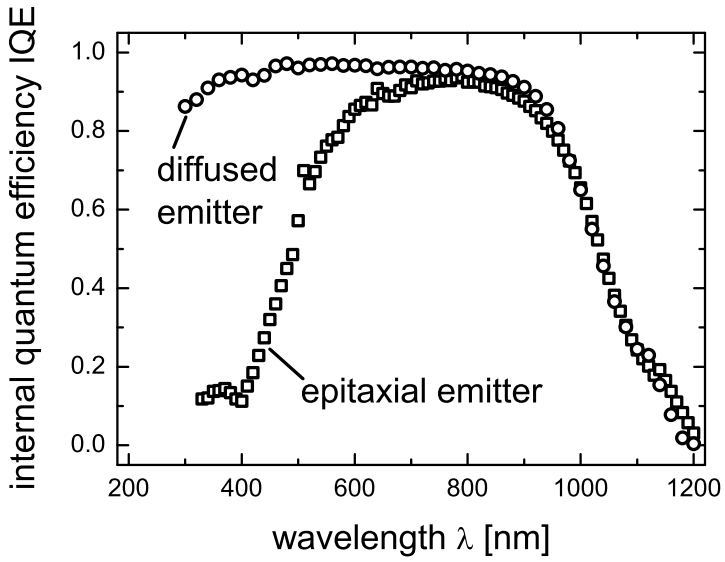

Figure 8.9: *The internal quantum efficiencies of two cells: One cell has an epitaxial emitter and its surface is not textured. The second cell has a diffused emitter and its surface is textured. The large difference in the IQE at short wavelengths regime indicates that the front surface, including the emitter itself, is main source of losses of the cell with the epitaxial emitter.*

Figure 8.9 compares between the measured internal quantum efficiency IQE of a cell with a diffused emitter and a cell with an epitaxial emitter. Both curves coincide at high wavelength regime and deviate at low wavelength regime. The reduced IQE of the cell

with an epitaxial emitter at wavelengths $\lambda \leq 520$ nm is due to low carrier collection[11] probability in the emitter,[12] which is ascribed to the high recombination in the emitter. In addition, the first 4 μm under the emitter, which corresponds to $520 \leq \lambda \leq 700$ nm, have also a low carrier collection. The low carrier collection at positions deeper than the emitter depth indicates that the interface, where the space charge region is located, is probably responsible for this high recombination, because both cells in Fig. 8.9 have bulks with a comparable quality as shown by the IQE at $\leq \lambda > 700$ nm. One possible reason for the high recombination at interface between the epitaxial emitter and the wafer is the roughness of the wafer, as well as the diffusion of boron atoms from the wafer to the emitter near to the interface.

8.3 Summary and Conclusions

This chapter has presented a new method to connect integrated mini-modules based on the conventional transfer process. The method is based on laser machining of cell from the back side after transfer onto one glass substrate. An 8.1 % efficient mini-module provides a silicon utility $U_{\mathrm{Si}} = 0.74$ W/g, which is higher than the double of the Si utility of a 20 % efficient wafer based module.

The present chapter has also introduced a performance comparison between the free-standing Si solar cells and the conventional transfer solar cells. A simple free-standing solar cell with full area Al metallization on the QMS layer has an efficiency $\eta = 17.0$ % slightly higher than that of the best transfer solar cell, which has obtained a complicated back side passivation step. The fabricated cell utilizes the material very efficiently, while the Si utility of the cell is $U_{\mathrm{Si}} \approx 1.5$ W/g.

This chapter has shown that on one hand, the performance of the conventional transfer cell with a passivated back side is limited by the absorption in the epoxy resin on its top. On the other hand, the performance of the free-standing cell is no more limited by the resin, but by the back side performance. Therefore, the efficiency of the free-standing solar cell still has a potential to be boosted. Nevertheless, the deciding factor is not the efficiency, but the cost of 1 kWh, including the material costs as well as the process complexity and costs. For example, further reduction of cost is possible by growing the

[11] The collection of photogenerated charge carriers depends on the effective diffusion length and hence of the recombination rate as shown in chapter 2.2

[12] Radiation with a wavelength $\lambda = 520$ nm has an absorption length $L_\alpha \approx 1$ μm in Si, which is comparable to the emitter depth $d_{\mathrm{e}} = 0.9$ μm and radiation with $\lambda = 520$ nm has $L_\alpha \approx 5$ μm

emitter epitaxially directly after the base epitaxial growth with a Si utility slightly smaller than unity.

Outlook

The present work considers the fabrication of free-standing thin silicon solar cells based on porous silicon as well as its handling concepts. The reduction of the solar cell thickness reduces the material consumption, offers the fabrication of mechanically flexible cells, and enhances the solar cell physics. Therefore, this work also introduces a new concept for integrated module connection of 50 μm thin transfer solar cells on glass. To avoid the glass attachment of transfer cells, the porous silicon formation conditions have to be enhanced. Thus, the main topic of the present thesis is the characterization and modeling of porous silicon. This thesis presents a non-destructive measurement technique for the porosity estimation. The white light interferometric determination of porosity is a quick method and easy to be automated.

Modeling of the silicon/electrolyte interface gives a better understanding of porous silicon formation in a double-chamber etching cell and results in the description of porous silicon selective formation. Based on selective porous silicon formation, local buried cavities form without the need to expensive, high temperature, and complex processes. These cavities enables on one side the separation of thin epitaxially grown silicon layers. On the other hand, buried cavities have also other application fields such as pressure sensors.

This work simulates the double-chamber etching cell based on the conductive medium model. The simulation of the current density homogeneity together with the experimental determination of the porosity homogeneity result in a new wafer chuck. The new chuck enhances the homogeneity of porous silicon by about 10 %. This enhancement increased the process yield and the transferred area. More accurate simulation is achieved by extending the conductive medium simulation with the silicon/electrolyte interface modeling, where the interface causes a non-linear current/voltage relation during the etching process. The composition of both models has a significant importance in the case of etching cells with heavily doped silicon electrodes instead of the common expensive platinum electrodes.

One important issue of an industrial process is its time-consumption. Unfortunately, the electrochemical etching process is more time-consuming than the other solar cell fabrication steps, where etching one wafer takes about three minutes. One possible method

to simplify the transfer-to-industry of the process is the parallel etching. The parallel etching implies etching more than one wafer at the same time with the same current density in the same etching cell. This requires the series connection of the wafers in a large etching cell. Simulating the distributions of the electric field intensity and current density is then necessary.

Free-standing thin silicon solar cell fabrication provides the loop-way to avoid the complex back side processing of the layer transfer solar cells. Instead of the adaptation of all processes to a cell with an epoxy resin and glass on its top, fabrication and handling of free-standing thin solar cells enables the use of the standard processes. However, the standard back contact process used in industry is not suitable to thin solar cells, where back side passivation and light trapping are extremely important. A silicon nitride layer between silicon and aluminium would increases the light reflectivity and decreases the minority carrier recombination rate at the cell back side. The problem is that such a layer electrically isolates the cell from the metal. Therefore, the local removal of the nitride before aluminium application by the commercially available screen-printable etching paste enables point back contact formation.

Appendix A

Light as an Electromagnetic Wave

In the course of this work, I have developed a computer program, which calculates the reflectance R_c from the system transfer matrix $\mathbf{R}$ of a multilayer porous silicon system on a silicon wafer. To consider the interference in the reflected spectrum due to the thin films, light is considered as an electromagnetic wave. The Maxwell equations [151] delivers the wave equations [152]

$$\triangle \mathbf{E} - \text{grad div } \mathbf{E} = \mu\sigma\frac{\partial \mathbf{E}}{\partial t} + \mu\epsilon\frac{\partial^2 \mathbf{E}}{\partial^2 t} \tag{A.1}$$

and

$$\triangle \mathbf{B} = \mu\sigma\frac{\partial \mathbf{B}}{\partial t} + \mu\epsilon\frac{\partial^2 \mathbf{E}}{\partial^2 t} \tag{A.2}$$

for the electric field intensity (E) and the magnetic flux density with the dielectric constant $\epsilon = \epsilon_r\epsilon_0$, the permeability $\mu = \mu_r\mu_0$, and the electrical conductivity σ of the medium. One solution of the wave equations (A.1 and A.2) is the planar electromagnetic wave defined by its spatially and temporally oscillating electric field

$$\mathbf{E} = \mathbf{E}_0 \exp\left(j\frac{2\pi}{\lambda}r - j\omega t\right) \tag{A.3}$$

and magnetic field

$$\mathbf{B} = \mathbf{B}_0 \exp\left(j\frac{2\pi}{\lambda}r - j\omega t\right) \tag{A.4}$$

at a position r and time t and with the amplitudes $\mathbf{E}_0$ and $\mathbf{B}_0$, the frequency ω and the wavelength λ.

The complex refractive index

$$\tilde{n} = \sqrt{\epsilon_r - j\frac{\sigma}{\omega\epsilon_0}} = n + jk \tag{A.5}$$

with the real refractive index n and the extinction coefficient k, which defines the absorption coefficient

$$\alpha = \frac{4\pi k}{\lambda} \tag{A.6}$$

of the material as a function of wavelength λ.

Appendix B

Etching Cell Simulation

Chapter 5 uses the conductive medium model [2] to simulate the electrochemical etching cell with different setups. According to this model, the basic partial differential equation describing the potential inside the electrochemical etching cell is the Poisson's equation

$$\nabla^2 V = -\frac{\rho_c}{\epsilon}, \tag{B.1}$$

where V is the voltage, ρ_c is the charge volumetric density, and ϵ is the dielectric constant of the medium.

The FEMLAB [137] extension module of Matlab [138] provides the two dimensional numerical solution of equation B.1 using the finite element method [137] with the suitable boundary conditions [2]. Two kinds of boundary conditions are possible:

1. Dirichlet condition is used when the potential is known at a certain surface $V = V_0$. For example, the potential at the anode $V = 0$ and at the cathode $V =$ - V_{cathode}.

2. Neumann condition is used when the potential at a surface is not known, but the electric field is known. For example, at the walls of the etching cell, no current flows, the electric field at that surface vanishes.

After solving equation B.1, the program determines the current density J distribution inside the cell, where

$$J = \sigma E. \tag{B.2}$$

with the electric field intensity

$$E = -\nabla V. \tag{B.3}$$

The current densities J_n used in chapter 5 is the component of J, which is normal to the wafer surface.

Appendix C

Abbreviations and Symbols

α	absorption coefficient	1/cm
ϵ	dielectric constant	$cm^2/(Vs)$
ϵ_0	dielectric constant of free space	8.85×10^{-14} $cm^2/(Vs)$
ϵ_r	relative dielectric constant	
ϵ_{Si}	dielectric constant of silicon	11 ϵ_0
ϵ_H	dielectric constant of Helmholtz layer	173 ϵ_0
η	solar cell conversion efficiency	%
λ	wavelength	nm
μ	magnetic permeability	N/A^2
μ_0	magnetic constant	$4\pi \times 10^{-7}$ N/A^2
μ_r	relative magnetic permeability	-
ρ	electrical resistivity	Ωcm
ρ_{Si}	density of silicon	2.3 g/cm^3
$\rho_{a,Si}$	atomic density of silicon	4.82 $\times 10^{22}$ cm^{-3}
σ	electrical conductivity	$1/(\Omega cm)$
τ	lifetime	s
Φ_λ	photon flux density	$1/(m^2nm)$
$\triangle\Phi_\lambda$	change inphoton flux density	$1/(m^2nm)$
ξ	longer path factor for textured cells	0.8
χ_e	electron affinity in silicon	-4.05 eV

A	area	cm^2
AM	Air Mass	-
AM 1.5G	Air Mass 1.5 global	-

AM1.5D	Air Mass 1.5 direct	-
$\mathbf{B}$	magnetic field vector	Tesla
ARC	anti-reflection coating	-
c	velocity of light in vacuum	3×10^8 m/s
CB	conduction band edge	-
c_{HF}	HF mass concentration	%
CVD	chemical vapor deposition	-
CZ	Chochralski grown silicon	-
d	layer thickness	nm
d_{cell}	solar cell thickness	μm
d_{n}	edge of space charge region in n-type	nm
d_{p}	edge of space charge region in p-type	nm
D	minority carriers diffusion constant	cm^2/s
D_{n}	electrons diffusion constant in p-type	cm^2/s
D_{ox}	density of empty states in electrolytes	cm^-3
D_{p}	holes diffusion constant in n-type	cm^2/s
D_{red}	density of occupied states in electrolytes	cm^-3
$\mathbf{E}$	electric field vector	V/m
E	energy	eV
E_g	bandgap energy	eV
E_{ph}	photon energy	eV
E_{C}	conduction band edge	eV
E_{ox}	energy level of oxidized species in electrolytes	eV
E_{red}	energy level of reduced species in electrolytes	eV
E_{redox}	redox energy level in electrolytes	eV
E_{V}	valence band edge	eV
EDX	energy dispersive X-ray analysis	-
EQE	external quantum efficiency	-
f_{c}	electron collection probability density	-
F	penalty function	-
FZ	floating-zone grown silicon	-
FF	fill factor	%

g	generation profile	$1/(\mathrm{cm}^3\mathrm{s})$
GOPS	germanium on porous silicon	-
h	Planck's constant	6.63×10^{-34} Js
H_n	solar cell emitter width	μm
H_n	solar cell base width	μm
I	intensity	$\mathrm{W/m}^2$
$I_\mathrm{AM1.5G}$	intensity of air Mass 1.5 global	1000 $\mathrm{W/m}^2$
ipe	Institut für Physikalische Elektronik	-
IQE	internal quantum efficiency	-
IR	infra-red	-
ISE	Fraunhofer-Institut für Solare Energiesysteme	-
IV	current-voltage	-
J	current density	$\mathrm{mA/cm}^2$
J_0	reverse saturation current density of a solar cell	$\mathrm{mA/cm}^2$
J_M	maximum power point current density	$\mathrm{mA/cm}^2$
J_s	reverse saturation current density of Schottky diode	$\mathrm{mA/cm}^2$
J_{sc}	short circuit current density	$\mathrm{mA/cm}^2$
ΔJ_{sc}	change in short circuit current density	$\mathrm{mA/cm}^2$
k	Boltzmann's constant	1.38×10^{-23} $\mathrm{m^2kgs^{-2}K^{-1}}$
L_α	absorption length	nm
L	minority carriers diffusion length	μm
L_n	electrons diffusion length in p-type bulk	μm
L_p	holes diffusion length in n-type bulk	μm
L_eff	effective diffusion length	μm
$L_\mathrm{n,eff}$	effective electron diffusion length in p-type	μm
$L_\mathrm{p,eff}$	effective hole diffusion length in n-type	μm
L_scr	space charge region width	nm
m	mass	Kg
n	refractive index	-
N_A	acceptor doping concentration	cm^{-3}
N_D	donor doping concentration	cm^{-3}
n_i	intrinsic electron concentration in silicon	1.04×10^{10} cm^{-3}
n_id	ideality factor	-
NML	no man's land	-
p	porosity	%
P	power density	$\mathrm{mW/cm}^2$

P_{M}	solar cell maximum output power density	$\mathrm{mW/cm^2}$
$P_{\mathrm{AM1.5G}}$	incident power density under AM1.5G illumination	$100\ \mathrm{mW/cm^2}$
q	elementary charge	1.6×10^{-19} C
QE	quantum efficiency	-
R	reflectance	%
R_{g}	growth rate	/s
$R_{m,\,c}$	measured/calculated reflectance	%
R_{p}	parallel resistance	$\Omega/\mathrm{cm^2}$
R_{s}	series resistance	$\Omega/\mathrm{cm^2}$
SEM	scanning electron microscope	-
S_{b}	back surface recombination velocity	cm/s
$S_{\mathrm{b,eff}}$	effective back surface recombination velocity	cm/s
SCR	space charge region	-
S_{f}	front surface recombination velocity	cm/s
$S_{\mathrm{f,eff}}$	effective front surface recombination velocity	cm/s
t	time	s
T	temperature	°C
U_{Si}	material utility of silicon	W/g
UV	ultra-violet	-
V	voltage	mV
VB	valence band edge	-
V_{OC}	open circuit voltage	mV
$\triangle V_{\mathrm{OC}}$	change in open circuit voltage	mV
V_{M}	maximum power point voltage	mV
WLI	white light interferometries	-
x, y, z	cartesian coordinates	-

Publication List

1. O. Tobail, M. Soliman and F. A. Abulfotuh, *Optical Analysis of Heterojunction Solar Cell*, presented at the Sharjah Solar Energy Conference, 19-22 February 2001, Sharjah, UAE.

2. O. Tobail, M. Soliman and F. A. Abulfotuh, *Analysis of the Transport Properties and Performance of Heterojunction Solar Cell*, presented at the Sharjah Solar Energy Conference, 19-22 February 2001, Sharjah, UAE.

3. O. Tobail and J. H. Werner, *Voltage Dependent Series Resistance of Thin Film Cu(In,Ga)Se_2 Solar Cells*, presented at the German Physical Society (DPG) - Berlin - Germany, 04-09 March 2005.

4. O. Tobail, P. Khanna, J. P. Rostan, M. Schubert, K. Brenner and J. H. Werner, *Integrated Photovoltaic Mini-Modules of Thin-Film Monocrystalline Si Solar Cells*, presented at the 2nd International Conference on Advances in Engineering Sciences & Technologies - National Research Center (NRC) - Cairo - Egypt, 20. September 2005.

5. M. Zimmermann, J. N. Burghartz, W. Appel, N. Remmers, C. Burwick, R. Würz, O.Tobail, M. B.Schubert, G. Palfinger, and J. H. Werner , *A Seamless Ultra-Thin Chip Fabrication and Assembly Process*, IEDM, 1010 (2006).

6. O. Tobail, Z. Yan, M. Reuter, and J. H. Werner, *Lateral homogeneity of porous silicon for large area transfer solar cells*, Thin Solid Films 516, 6959 (2008).

7. O. Tobail, M. Reuter, J. H. Werner, *Novel Separation Process for Free-Standing Silicon Thin-Films*, presented at the PVSEC-17, Fukuoka, Japan, 03-07 December 2007.

8. O. Tobail, M. Reuter, J. H. Werner, *Novel Separation Process for Free-Standing Silicon Thin-Films*, Sol. Energy Mater. & Sol. Cells, doi:10.1016/j.solmat.2008.09.014 (2008).

9. M. Reuter, W. Brendle, O. Tobail, J. H. Werner, *efficient 50 μm thin solar cells with* 17 *% efficiency*, Sol. Energy Mater. & Sol. Cells, doi:10.1016/j.solmat.2008.09.035 (2008).

Bibliography

[1] W. Brendle, *Niedertemperaturrückseitenprozess für hocheffiziente Siliziumsolarzellen* (Shaker Verlag, Achen, Germany, 2007).

[2] C. Berge, *Separation Layer from Sintering of Porous Silicon, Layer Formation and Applications* (Shaker Verlag, Achen, Germany, 2005).

[3] M. Reuter, W. Brendle, O. Tobail, and J. H. Werner, submitted to Sol. Energy Mater. Sol. Cells (2007).

[4] A. Uhlir, Bell Syst. Tech. J. **35**, 333 (1956).

[5] C. S. Fuller and J. A. Ditzenberger, J. Appl. Phys. **27**, 544 (1957).

[6] D. R. Turner, J. Electrochem. Soc. **105**, 402 (1958).

[7] R. J. Archer, J. Phys. Chem. Solids **14**, 104 (1960).

[8] Y. Watanabe and T. Sakai, Rev. Electron. Commun. Labs. **19**, 899 (1971).

[9] Y. Watanabe, Y. Arita, T. Yokoyama, and Y. Igarashi, J. Electrochem. Soc. **122**, 1351 (1975).

[10] A. G. Cullis, L. T. Canham, and P. D. J. Calcott, Appl. Phys. Rev. **82**, 909 (1997).

[11] X. G. Zhang, *Electrochemistry of Silicon and its Oxides* (Kluwer Academic/Plenum Publisher, New York, 2001).

[12] V. Lehmann, *Electrochemistry of Silicon* (Wiley-VCH-Verlag, Weinheim, 2002).

[13] Y. Arita, K. Kato, and T. Sudo, IEEE Trans. Electron. Devices **24**, 756 (1977).

[14] T. Unagami and K. Kato, Jpn. J. Appl. Phys. **16**, 1635 (1977).

[15] K. Imai and Y. Yoriume, Jpn. J. Appl. Phys. **18-1**, 281 (1979).

[16] L. T. Canham, Appl. Phys. Lett. **57**, 1046 (1990).

[17] V. Lehman and U. Gösele, Appl. Phys. Lett. **58**, 856 (1991).

[18] V. Torres-Costa, R. J. Martin-Palma, and J. M. Martinez-Duart, J. Appl. Phys. **96**, 4197 (2004).

[19] M. Thönissen, S. Billat, M. Krüger, H. Lüth, M. G. Beger, U. Frotscher, and U. Rossow, J. Appl. Phys. **80-5**, 2990 (1996).

[20] M. Thönissen, M. G. Beger, S. Billat, R. Arens-Fisher, M. Krüger, H. Lüth, W. Theiss, P. Hillbrich, G. Grosse, G. Lerondel, and U. Frotscher, Thin Solid Films **297**, 92 (1997).

[21] M. I. J. Beale, N. G. Chew, M. J. Uren, A. G. Cullis, and J. D. Benjamin, Appl. Phys. Lett. **46-1**, 86 (1985).

[22] M. I. J. Beale, J. D. Benjamin, M. J. Uren, N. G. Chew, and A. G. Cullis, J. Cryst. Growth **73**, 622 (1985).

[23] C. S. Solanki, R. R. Bilyalov, J. P. Celis, W., J. Nijs, and R. Mertens, J. Electrochem. Soc. **151**, C397 (2004).

[24] R. L. Smith and S. D. Collins, J. Appl. Phys. **71-8**, R1 (1996).

[25] M. Ligeon, F. Muller, R. Herino, and F. Gaspard, J. Appl. Phys. **66-8**, 3814 (1989).

[26] H. Tanaka, H. Shimada, and A. Kinoshita, J. Electrochem. Soc. **151**, C439 (2004).

[27] K. Imai and H. Unno, IEEE Trans. Electron Devices **ED-31**, 291 (1984).

[28] F. Gaspard, A. Bsiesy, M. Ligeon, and R. Muller, F. Herino, J. Electrochem. Soc. **136-10**, 3043 (2004).

[29] X. G. Zhang, J. Electrochem. Soc. **151-1**, C69 (2004).

[30] S. D. Zhang, X. G. Collins and R. L. Smith, J. Electrochem. Soc. **136-5**, 1561 (1998).

[31] V. Bertagana, C. Plougonven, F. Rouelle, and M. Chemla, J. Electrochem. Soc. **143-11**, 3532 (1996).

[32] A. Valance, Phys. Rev. B **52**, 8323 (1995).

[33] A. Valance, Phys. Rev. B **55**, 9706 (1997).

[34] Y. Kang and J. Jorné, J. Electrochem. Soc. **144-9**, 3104 (1997).

[35] X. G. Zhang, J. Electrochem. Soc. **138-12**, 3750 (1991).

[36] Y. Arita, J. Cryst. Growth **45**, 383 (1978).

[37] J. Rouquerol, D. Avnir, C. W. Fairbridge, D. H. Everett, J. H. Haynes, N. Prenicore, J. D. F. Ramsey, K. S. W. Sing, and K. K. Unger, Pure Appl. Chem. **66**, 1739 (1994).

[38] L. N. Aleksandrov and P. L. Novikov, Thin Solid Films **330**, 102 (1996).

[39] see Ref. [12], p. 57

[40] H. Harada, M. Nakamura, T. Ohwada, S. Okuda, A. Hosono, and M. Mashimo, Jpn. Appl. Phys. **42**, 3379 (2003).

[41] R. Memming and G. Schwandt, Surf. Sci. **4**, 109 (1966).

[42] R. Herino, G. Bomchil, K. Barla, C. Bertrand, and J. L. Ginoux, J. Electrochem. Soc. **134**, 1994 (1987).

[43] L. M. Peter, D. J. Riley, and R. I. Wielgosz, Thin Solid Films **276**, 61 (1996).

[44] Y. Zhao, D. Yang, D. Li, and M. Jiang, Appl. Surf. Sci. **252**, 1065 (2005).

[45] L. Martin, Diplomarbeit, Universität Stuttgart, 2007.

[46] O. Tobail, Z. Yan, M. Reuter, and J. H. Werner, Thin Solid Films **516**, 6959 (2008).

[47] H. Gerischer, Electrochim. Acta **35**, 1677 (1990).

[48] S. R. Morrison, *Electrochemistry of Semiconductor and Oxidized Metal Electrodes* (Plenum Press, New York, 1981).

[49] R. Memming, *Comprehensive Treatise of Electrochemistry* (Plenum Publisher, New York, 1983).

[50] A. J. Bard, A. B. Bocarsly, R. F. Fan, E. G. Walton, and M. S. Wrighton, J. Am. Chem. Soc. **102**, 3683 (1980).

[51] Y. V. Pleskov and Y. Y. Gurevich, *Semiconductor Photoelectrochemistry* (Consultants Bureau, New York, 1986).

[52] S. M. Sze, *Semiconductor Devices: Physics and Technology* (Wiley, New York, 1985).

[53] I. Ronga, A. Bsiesy, F. Gaspard, R. Herino, M. Ligeon, F. Muller, and A. Halimaoui, J. Electrochem. Soc. **138**, 533 (1991).

[54] H. Gerischer, Surf. Sci. **18**, 97 (1969).

[55] G. Müller, Dissertation, Universität Erlangen, 2002.

[56] C. Pickering, M. I. J. Beale, D. J. Robinson, P. J. Pearson, and R. Greef, J. Phys. C: Solid State Phys. **17**, 5535 (1984).

[57] R. L. Smith, S. F. Chuang, and S. D. Collins, J. Electron. Matter. **17**, 533 (1988).

[58] R. L. Smith, S. F. Chuang, and S. D. Collins, Sensor Actuat. A-Phys **23**, 825 (1988).

[59] S. Frohnhoff, M. Marso, M. G. Berger, M. Thoenissen, H. Lueth, and H. Muender, J. Electrochem. Soc. **142**, 615 (1995).

[60] A. G. Cullis and L. T. Canham, Nature **353**, 353 (1991).

[61] J. Li, S. Cai, and S. Zhang, Chin. Sci. Bull. **41-24**, 2060 (1996).

[62] R. Q. Wang, J. J. Li, S. M. Cai, Z. F. Liu, and S. L. Zhang, Appl. Phys. Lett. **72-8**, 924 (1998).

[63] M. H. Al Rifai, M. Christophersen, S. Ottow, J. Carstensen, and H. Föll, J. Electrochem. Soc. **147**, 627 (2000).

[64] J. Carstensen, M. Christophersen, and H. Föll, Mater. Sci. Eng. B **69-70**, 23 (2000).

[65] H. Föll, J. Carstensen, M. Christophersen, and G. Hasse, Phys. Status Solidi A. **182**, 45 (2000).

[66] J. Carstensen, M. Christophersen, and H. Föll, Phys. Status Solidi A. **182**, 63 (2000).

[67] G. Hasse, M. Christophersen, J. Carstensen, and H. Föll, Phys. Status Solidi A. **182**, 23 (2000).

[68] H. Föll, M. Christophersen, J. Carstensen, and G. Hasse, Mater. Sci. Eng. R **39**, 93 (2002).

[69] G. Lérondel and R. Romestain, Thin Solid Films **297**, 114 (1997).

[70] T. C. Choy, *Effective Medium Theory: Princible and Applications* (Oxford University Press, Oxford, 1999).

[71] D. A. G. Bruggeman, Ann. Phys. (Paris) **24**, 636 (1935).

[72] O. S. Heavens, *Optical Properties of Thin Solid Films* (Dover, New York, 1991).

[73] H. A. Macleod, *Thin-Film Optical Filters*, 3 edition (Bristol Institute of Physics Publisher, New York, 1991).

[74] R. J. Martín-Palma, P. Herrero, R. Guerrero-Lemus, J. D. Moreno, and M. Martínz-Duart, J. Mater. Sci. Lett. **17**, 845 (1990).

[75] L. Pavesi, R. Chierchia, P. Bellutti, A. Lui, F. Fuso, M. Labardi, L. Pardi, F. Sbrana, M. Allergrini, S. Trusso, C. Vasi, P. J. Ventura, L. C. Costa, M. C. Carmo, and O. Bisi, J. Appl. Phys. **86**, 6474 (1999).

[76] P. Steiner, F. Kozlowski, and W. Lang, Appl. Phys. Lett. **62-21**, 2700 (1993).

[77] M. A. Green, *Solar Cells: Operating Principles, Technology and System Applications* (University of New South Wales (UNSW), Kensington, New South Wales, Australia, 1999).

[78] A. L. Fahrenbruch and R. H. Bube, *Fundamentals of Solar Cells* (Academic Press Inc., New York, 1983).

[79] M. A. Green, *Third Generation Photovoltaics* (Springer-Verlag, Berlin, Heidelberg, 2006).

[80] M. A. Green, A. W. Blakers, J. Zhao, A. M. Milne, A. Wang, and X. Dai, IEEE Trans. Electron. Dev. **37-2**, 331 (1990).

[81] A. Zhao, J. andWang and M. A. Green, Prog. Photovoltaics: Res. Appl. **7**, 471 (1999).

[82] A. Wang, J. Zhao, and M. A. Wenham, S. R. Green, Prog. Photovoltaics: Res. Appl. **4**, 55 (1996).

[83] J. Y. Lee and S. W. Glunz, Sol. Energy Mater. & Sol. Cells **90**, 82 (2006).

[84] A. G. Aberle, S. Glunz, and W. Warta, J. Appl. Phys. **71-9**, 4422 (1992).

[85] A. W. Stephens, A. G. Aberle, and M. A. Green, J. Appl. Phys. **76**, 363 (1994).

[86] J. Schmidt and A. G. Aberle, J. Appl. Phys. **85**, 3626 (1999).

[87] P. J. Rostan, U. Rau, V. X. Nguyen, T. Kirchartz, M. B. Schubert, and J. H. Werner, Sol. Energy Mater. & Sol. Cells **90**, 1345 (2006).

[88] A. R. Burgers, Prog. Photovolt. Res. Appl. **7**, 457 (1999).

[89] M. Schöfthaler, U. Rau, W. Füssel, and J. H. Werner, in *Proc. 23th IEEE Photovolt. Spec. Conf.* (IEEE, Piscataway, NJ, USA, 1993), p. 315.

[90] R. Brendel, *Thin-Film Crystaline Silicon Solar Cells: Physics and Technology* (Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany, 2003).

[91] C. Donolato, Appl. Phys. Lett. **46**, 270 (1985).

[92] C. Donolato, J. Appl. Phys. **66**, 4524 (1989).

[93] W. V. Roosbroeck, J. Appl. Phys. **26**, 380 (1955).

[94] A.-A. S. Al-Omar and M. Y. Ghannam, J. Appl. Phys. **79**, 2103 (1996).

[95] P. A. Basore, in *Proc. 23th IEEE Photovolt. Spec. Conf.* (IEEE, Piscataway, NJ, USA, 1993), p. 147.

[96] K. Taretto, Dissertation, Universität Stuttgart, 2003.

[97] P. Kittidachachan, T. Markvart, D. M. Bagnall, R. Greef, and G. J. Ensell, Sol. Energy Mater. & Sol. Cells **91**, 160 (2007).

[98] M. A. Green, J. Appl. Phys. **81**, 266 (1997).

[99] see Ref. [90], p. 53

[100] W. Brendle, V. Nguyen, A. Grohe, E. Schneiderlöchner, U. Rau, G. Palfinger, and J. H. Werner, Prog. Photovolt. **14**, 653 (2006).

[101] P. O. Grabits, U. Rau, W. Brendle, G. Bilger, and J. H. Werner, in *Proc. 4th World Conf. Photovolt. Energy Conv.* (IEEE, New York, USA, 2006), p. 424.

[102] O. Tobail, Diplomarbeit, Universität Stuttgart, 2005.

[103] J. H. Werner, Appl. Phys. A **47**, 291 (1988).

[104] LOTUS Systems GmbH, Immendingen, Germany, www.lotus-systems.de.

[105] Hydrofluoric acid safty data sheet, available from HF supplier.

[106] Merkplatt Gefahrstoffe: Fluorwasserstoff, Flusssäure und anorganische Fluoride, M 005, 2/2000, BGI 576,, published by Berufsgenossenschaft der chemischen Industrie, Heidelberg.

[107] S. Nakashima, IEICE Trans. Electron. **E80-C**, 364 (1997).

[108] M. Bruel, Nucl. Instrum. Methods **B108**, 313 (1996).

[109] Q.-Y. Tong, R. Scholz, U. Gösele, T.-H. Lee, and Y.-L. Tan, Appl. Phys. Lett **72**, 49 (1998).

[110] C. H. Yun, A. B. Wengrow, N. W. Cheung, Y. Zheng, R. J. Welty, Z. F. Guan, K. V. Smith, P. M. Asbeck, E. T. Yu, and S. S. Lau, Appl. Phys. Lett **73**, 2772 (1998).

[111] K. Sakaguchi, N. Sato, K. Yamagata, T. Atoji, Y. Fujiyama, J. Nakayama, and T. Yonehara, IEICE Trans. Electron. **E80-C**, 378 (1997).

[112] R. Brendel, H. Artmann, S. Oelting, W. Frey, J. H. Werner, and H. J. Queisser, Appl. Phys. A **67**, 151 (1998).

[113] H. Tayanaka, K. Yamauchi, and T. Matsuhita, in *Proc. 2nd World Conf. on Photovolt. Energy Conv.* (J. Schmid, H. A. Ossenbrink, P. Helm, H. Ehmann and E. D. Dunlop, E. C. Joint Res. Centre, Luxembourg, 1998), p. 1272.

[114] T. J. Rinke, R. B. Bergmann, and J. H. Werner, Appl. Phys. A **68**, 705 (1999).

[115] M. Zimmermann, J. N. Burghartz, W. Appel, N. Remmers, C. Burwick, R. Würz, O. Tobail, M. B. Schubert, P. G., and J. H. Werner, IEDM, 1010 (2006).

[116] T. J. Rinke, Dissertation, Universität Stuttgart, 2004.

[117] R. B. Bergmann, T. J. Rinke, and J. H. Werner, Physikalische Blätter **56 (9)**, 1 (2000).

[118] R. B. Bergmann, C. Berge, T. J. Rinke, J. Schmidt, and J. H. Werner, Sol. Energy Mater. & Sol. Cells **74**, 213 (2002).

[119] J. Rostan, C. Berge, U. Rau, and J. H. Werner, J. Electrochem. Soc. **153**, 133 (2006).

[120] O. Tobail, P. Khanna, P. J. Rostan, M. B. Schubert, K. Brenner, and J. H. Werner, in *2nd International Conference on Advances in Engineering Sciences and Technologies*, *2* (National Research Centre, NRC, Cairo, Egypt, 2005), p. 96.

[121] A. Kiss, Studienarbeit, Universität Stuttgart, 2006.

[122] N. Ximello, *Visible Photoluminescence from Porous Silicon* (Shaker Verlag, Achen, Germany, 2007).

[123] E. Kasper and D. J. Paul, *Silicon Quantum Integrated Circuits, Silicon-Germanium Heterostructure; Devices: Basics and Realization* (Springer Verlag, Heidelberg, Germany, 2005).

[124] J. D. Cressler, *Silicon Heterostructure Handboock: Material, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy* (CRC PRESS, New York, 2006).

[125] C. Claeys and E. Simoen, *Germanium based Technologies: From Material to Devices* (Elsavier, Amesterdam, 2007).

[126] M. Oehme, J. H. Werner, E. Kasper, M. Jutzi, and M. Berroth, Appl. Phys. Lett **89**, 071117 (2006).

[127] E. Kasper and K. Lyutovich, Solid-States Electronics **48**, 1257 (2004).

[128] M. Oehme, private communication.

[129] M. R. Luek, C. L. Andre, A. J. Pitera, M. L. Lee, E. A. Fitzgerald, and S. A. Ringel, IEEE Electr. Dev. Lett. **26**, 142 (2006).

[130] M. Oehme and E. Kasper, *Silicon Heterostructure Handbook* (CRC PRESS, New York, 2006).

[131] M. Oehme, E. Bauer, and E. Kasper, Mat. Sci. & Eng. **B89**, 332 (2002).

[132] M. Oehme, E. Bauer, and E. Kasper, Thin Solid Films **364**, 228 (2000).

[133] M. Oehme, private communication.

[134] see Ref. [2], p. 80

[135] Z. Gaburro, H. You, and D. Babic, J. Appl. Phys. **84**, 6345 (1998).

[136] Z. Yan, Studienarbeit, Universität Stuttgart, 2007.

[137] O. C. Zienkiewicz, R. L. Taylor, and J. Z. Zhu, *Finite Element Method : Its Basis and Fundamentals*, 6th edition (Butterworth-Heinemann, Amsterdam, 2006).

[138] Femlab Version 2.3, Comsol AB, Tegnergatan 23, 11140 Stockholm, Sweden,, www.femlab.com.

[139] H. Kwon, Young W. Bang, *Finite Element Method using MATLAB*, 6th edition (CRC Press, Inc., New York, 1997).

[140] .

[141] Y. K. Xu and S. Adachi, J. Phys. D: Appl. Phys. **39**, 4572 (2006).

[142] see Ref. [49], p. 529

[143] H. Seidel, A. Csepregi, and H. Baumgaertel, J. Electrochem. Soc. **137**, 3612 (1990).

[144] J. H. Werner, *Lecture Script of Solid State Electronics* (Institut für Physikalische Elektronik, *ipe*, Universität Stuttgart, Stuttgart, 2008).

[145] B. H. Brandsden and C. J. Joachain, *Introduction to Quantum Mechanics* (John Wiley and Sons Inc., New Yourk, 1983).

[146] D. K. Ferry, *Quantum Mechanics: An Introduction for Device Physicists and Electrical Engineers* (Institute of Pysic Publishing Ltd, London, 1995).

[147] G. Bilger and G. H. Bauer, Thin Solid Films **119**, 103 (1984).

[148] Final report of the project HiFlex, FKZ 032 9818A, Universität Stuttgart, 2006.

[149] Datenblatt von EPO-TEK H20E-frozen, available from the supplier: Polytec GmbH, www.polytec.de.

[150] see Ref. [52], p. 794

[151] D. Marcuse, *Light Transmission Optics* (Van Nostrand Reinhold Company, New York, 1972).

[152] G. Lehner, *Elektromagnetische Feldtheorie für Inginieure und Physiker*, 3rd edition (Springer, Berlin, Germany, 1996).

Curriculum Vitae

Osama Fouad Tobail

01.09.1974	Born in Alexandria, Egypt
1980–1985	Primary school, Alexandria, Egypt
1985–1988	Preparatory school, Alexandria, Egypt
1988–1992	Secondary school, Alexandria, Egypt
1992–1997	Study at Communications and Electrophysics department, Faculty of Engineering, University of Alexandria, Egypt
08.1997	Bachelors, grade: "very good" graduation project: Automatic Speaker Recognition using Artificial Neural Networks Project grade: "excellent"
1997–2001	Instructor at Alexandria Institute of Technology, Egypt
1998–2001	Graduate study at Faculty of Engineering, Arab Academy for Science and Technology, Alexandria, Egypt
11.2001	Master, final grade: "excellent" Subject: Optical and Performance Analysis of Heterojunction a-Si/c-Si Solar Cell
2001–2003	Teaching assistant at Alexandria Institute of Technology, Egypt
since 08.2003	Researcher at Institute of Physical Electronics (*ipe*), University of Stuttgart, Germany

Acknowledgement

Finally, I would cordially like to thank all the people that enabled the success of this work. It is a pleasure for me to express my gratitude to ...

• Prof. Dr. Jürgen H. Werner for accepting me as a PhD student at his institute, for his sustained interest in my work, for teaching me how to write a proper scientific publication, and for providing excellent working conditions throughout my thesis.

• Prof. Dr. Helmut Föll for kindly taking over the co-report of this thesis.

• Christopher Berge, Johannes Rostan, and Willi Brendle for supporting me with their experience in the layer transfer process.

• Roland Würz, who patiently trained and instructed me on the electrochemical etching process.

• Michael Reuter for critically reading my thesis. It was great fun working with you.

• Christian Ehling, Anke Helbig, Marc Saemann, Nestor Ximello, Carolin Ulbrich, and Gordana Kulusic for their effort during reading and reviewing this thesis.

• Sebastian Eisele, Caroline Carlsson, and Jürgen Köhler from the laser group at *ipe* for the useful discussions and supporting me during performing laser processes.

• Dr. Gerhard Bilger for the SIMS measurements and the useful discussions.

• Uwe Rau and Thomas Wagner for their fruitful guiding motivating discussions.

• Klaus Brenner, Leo Bauer, Birgitt Winter, Brigitte Lutz, Galina Moutchnik, and Christiane Köhler from the technology group at *ipe* for the great support during solar cell processing.

• Wolfgang Appel and Martin Zimmermann from the institute of Microelectronics Stuttgart (IMS) for the useful cooperation and for the epitaxy growth.

• Markus Schubert for the useful discussions and organizing the cooperation with the IMS.

• Michael Oehme from the institut für Halbleitertechnik (IHT) for the molecular beam epitaxy and the characterization of the Ge films.

• all the actual and former members of the *ipe* for an outstanding working atmosphere.

• my parents for enabling me a carefree study and for supporting me.

• my wife Marwa for patiently listening me and spiritually supporting me.

Thank you!
Osama Tobail

Erklärung

Hiermit erkläre ich, dass ich die vorliegende Dissertation "Porous Silicon for Thin Solar Cell Fabrication" selbständig verfasst und nur die angegebenen Hilfsmittel verwendet habe.

Stuttgart, den 05.12.2008

Osama Tobail