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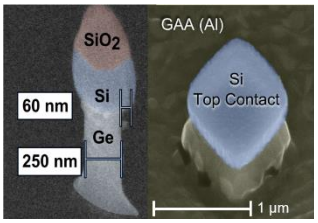

MASTER THESIS

IHT-Research Group „Power Electronics“

Research Thesis at IHT

Bildquelle: „Vertikaler >>Gate-All-Around<<-Transistor in verschiedenen Stadien der Fertigung“, IHT, Universität Stuttgart

Fabrication and Electrical Characterization of Ultra-Thin Substrate IGBT

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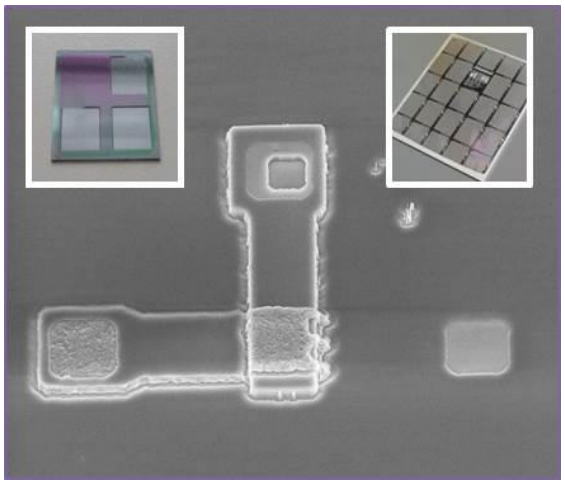
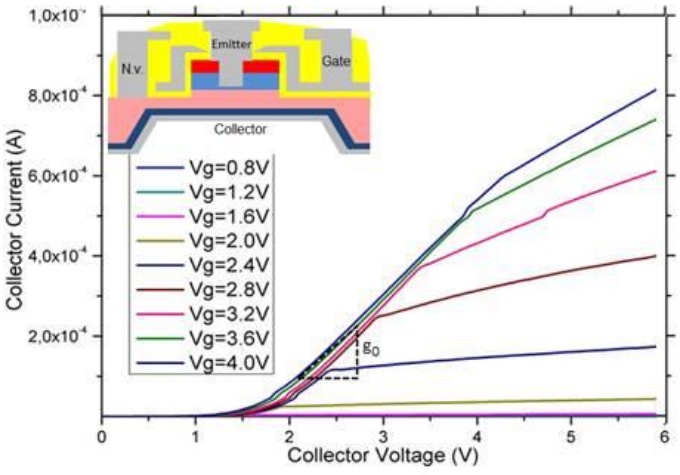
Finally, I wish to thank my parents and friends for their support and encouragement throughout my study.

Abstract

Current topics such as electro-mobility and renewable energy demand the development of power devices with high voltage and current ratings along with minimum switching losses. Amongst the power devices in today's market, IGBTs have gained a lot of significance in this field over its competitors like Power MOSFETS and Thyristors. Today's industry has recently taken a huge step in this direction to implement the use of thin-wafer technology for fabrication of IGBTs to reduce the on-resistance. However, this comes with a complexity of handling these thin wafers which demands the need of high end robotics. For research work, accesses to such resources are not feasible and if we are not able to fabricate device which the industry is fabricating today, we cannot add improvements to it and hence the research in this domain becomes restricted.

The primary objective of this thesis work is to develop a technology for fabrication of Ultra-Thin substrate IGBT which can be achieved at any standard semiconductor research facility and in the course, reducing the on-resistance of the device wherever possible. The most promising solution was the use of Ultra-Thin Si-membranes as a substrate for fabrication. These Si-membranes were fabricated by anisotropic etching of Si wafers by TMAH. IGBT being a four-layered device, the required layers were deposited on the Si-membrane by MBE to achieve very thin and distinct layers which would minimize the on-resistance. Uniquely the Gate terminal of the device was structured on the sidewall of the mesa structure as opposed to conventional trench gate structures. The device with such dimension and structure was initially simulated by the device simulator ATLAS from Silvaco to verify the working of the device and to have a general idea of what kind of a characteristics to expect from the fabricated device. Thereafter the devices were successfully fabricated at our research facility at IHT.





Even though there were numerous technical challenges and difficulties, the technology proved to be robust and we were able to fabricate the first IGBT at IHT even in the first run. The electrical characteristics showed a good forward characteristics of the device with good gate response and high on-current to off-current ratio but the reverse characteristics of the device showed unusual characteristics which is also investigated in this thesis work.

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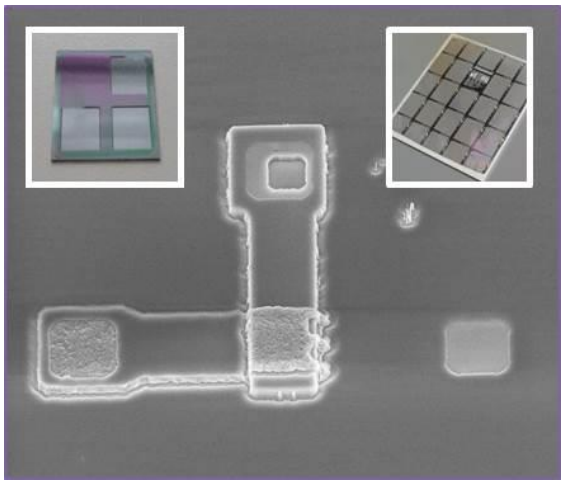
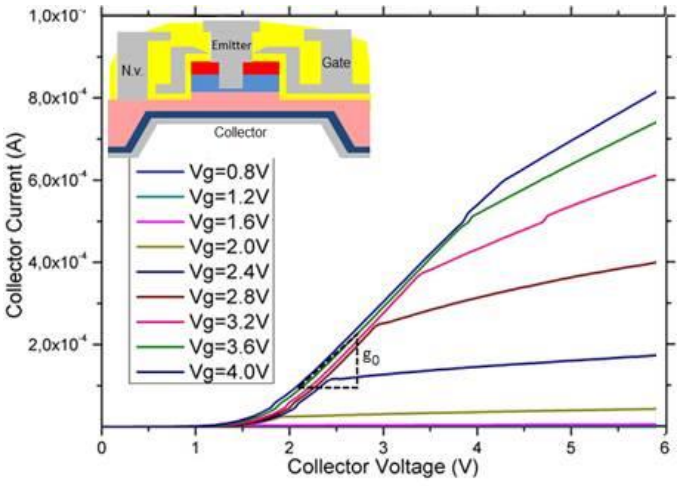
Zusammenfassung der Arbeit

Aktuelle Themen wie Elektromobilität und erneuerbare Energien die Nachfrage die Entwicklung der Stromversorgung mit Hochspannung und Strom mit minimalen Schaltverluste . Unter den Power-Geräte auf dem heutigen Markt, haben IGBTs eine Menge von Bedeutung in diesem Bereich gewonnen gegenüber seinen Wettbewerbern wie Leistungs-MOSFETs und Thyristoren. Die heutige Industrie hat vor kurzem einen großen Schritt in diese Richtung unternommen, um den Einsatz von Thin - Wafer-Technologie für die Herstellung von IGBTs implementieren, um die On-Widerstand zu verringern. Allerdings kommt diese mit einer Komplexität von Umgang mit diesen dünnen Wafern, die die Notwendigkeit von High-End- Robotik verlangt. Für Forschungsarbeiten, greift zu solchen Ressourcen nicht durchführbar sind und wenn wir nicht in der Lage, Geräte herzustellen, welche die Branche Herstellung von heute sind, wir können keine Verbesserungen zu und damit die Forschung in diesem Bereich wird eingeschränkt .

Das primäre Ziel dieser Diplomarbeit ist es, eine Technologie zur Herstellung von Ultra-Thin Substrat IGBT, die in jedem Standard-Halbleiter- und Forschungseinrichtung im Rahmen getan werden kann, um so der On-Widerstand des Gerätes wo immer möglich. Die vielversprechendsten Lösung war die Verwendung von Ultra-Thin Si-Membranen als Substrat für die Herstellung. Eindeutig dem Gate-Anschluß der Vorrichtung wurde an der Seitenwand der Mesa-Struktur aufgebaut, im Gegensatz zu herkömmlichen Trench-Gate-Strukturen. Das Gerät mit einer solchen Dimension und Struktur war zunächst simuliert, indem das Gerät aus -Simulator ATLAS Silvaco um das Funktionieren des Geräts zu überprüfen und um eine allgemeine Vorstellung davon, welche Art von einem Merkmale aus dem Gerät hergestellt erwarten. Danach wurden die Geräte erfolgreich an unserer Forschungsanlage im IHT hergestellt.





Obwohl es zahlreiche technische Herausforderungen und Schwierigkeiten, erwies sich die Technik als robust und wir konnten die ersten IGBT an aus Labor herzustellen sogar im ersten Lauf. Die elektrischen Eigenschaften zeigte eine gute vorwärts Merkmale des Geräts mit guter Reaktion und hohe Gate- on- Strom off- Strom-Verhältnis, aber die umgekehrte Merkmale des Geräts zeigten ungewöhnliche Eigenschaften, die auch in dieser Diplomarbeit untersucht.

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Abbreviations

The following abbreviations are used for simplicity in this entire work:

AFM	Atomic Force Microscope
Al	Aluminium
B	Boron
BHF	Buffered Hydrofluoric Acid
BJT	Bipolar Junction Transistor
CHF_3	Tri-fluoro-methane
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapour Deposition
HF	Hydrofluoric Acid
ICP	Inductive Coupled Plasma
ICP-RIE	Inductive Coupled Plasma Reactive Ion Etching
IGBT	Insulated Gate Bipolar Transistor
MBE	Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
P	Phosphorous
PDB	Planar Doped Barrier
PDBFET	Planar Doped Barrier Field Effect Transistor
PECVD	Plasma-Enhanced Chemical Vapour Deposition
RF	Radio Frequency
RIE	Reactive Ion Etching
Sb	Antimony
SEM	Scanning Electron Microscope
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon dioxide
SMU	Source Measuring Unit
TEOS	Tetra-ethyl-ortho-silicate
TMAH	Tetra-methyl-ammonium-hydroxide

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1. Motivation and Objectives of the Work

1.1. Motivation

Power Semiconductor devices are an essential component in shaping the growth of the Energy Sector in today's world. The constant search for the '*Perfect Switch',* drives and promotes the research for novel device structure, as they have a high impact on the size, cost and efficiency of power electronic systems. With the critical constraint we face in terms of saving power, it becomes the highest priority that we try to reduce losses in whatever form we can. This thesis work is a small step forward in this direction to reduce the ON-State losses in IGBT.

Over the last few decades the world experienced the evolution of many power devices, but amongst them few had an impact as great as the Insulated Gate Bipolar Transistor (IGBT). It finds its application with a versatile range of power rating but is remarkably dominating in the medium voltage (600-2500 V), medium power (10 kW) and medium frequency range up to 20 kHz. It finds widespread application in AC motor drives, traction control, inductive heating systems, radiological systems (X-ray tubes), uninterruptible power supplies, Switch-mode power supplies, harmonic compensator and so on. [1]. Fig. 1.1 gives a graphical overview of the extent of IGBT penetration in power devices market.

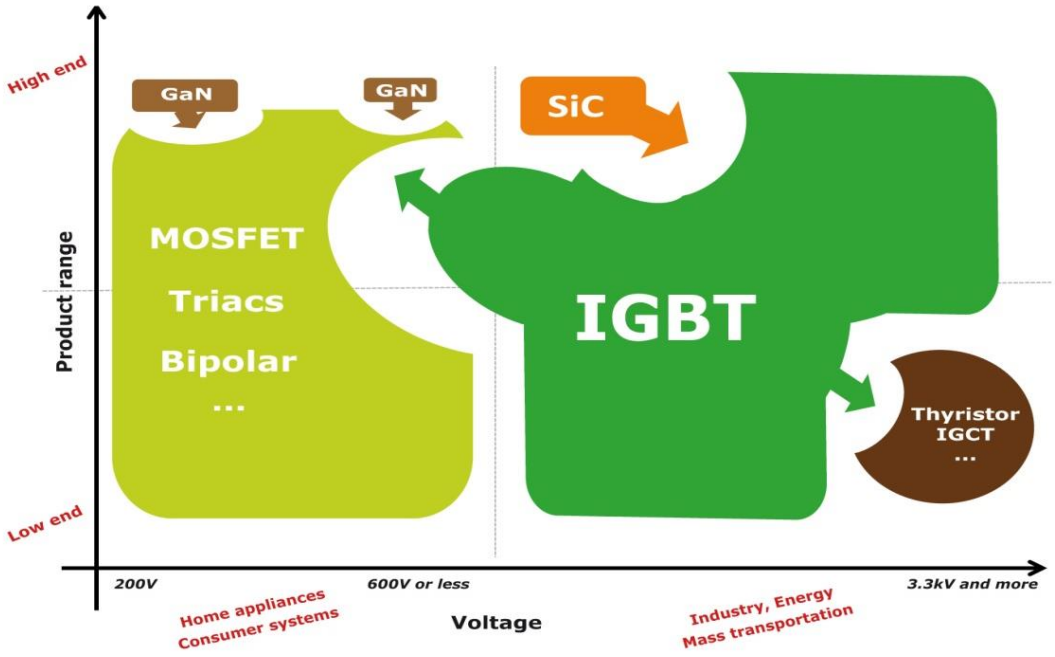

Fig. 1.1 : Power Device Technology Positioning [2]

Although IGBTs have been evolving from several decades now and face competition from new novel devices like SiC, it is nowhere near its downfall. In fact Yole Development's report on 'IGBT Markets & Applications Trends' predicts the steady growth for the IGBT market; specifically, from $3.6B today to $6B by 2018. It can be seen from Fig. 1.2 that the majority of the growth from the IGBT is to come from electro-mobility.

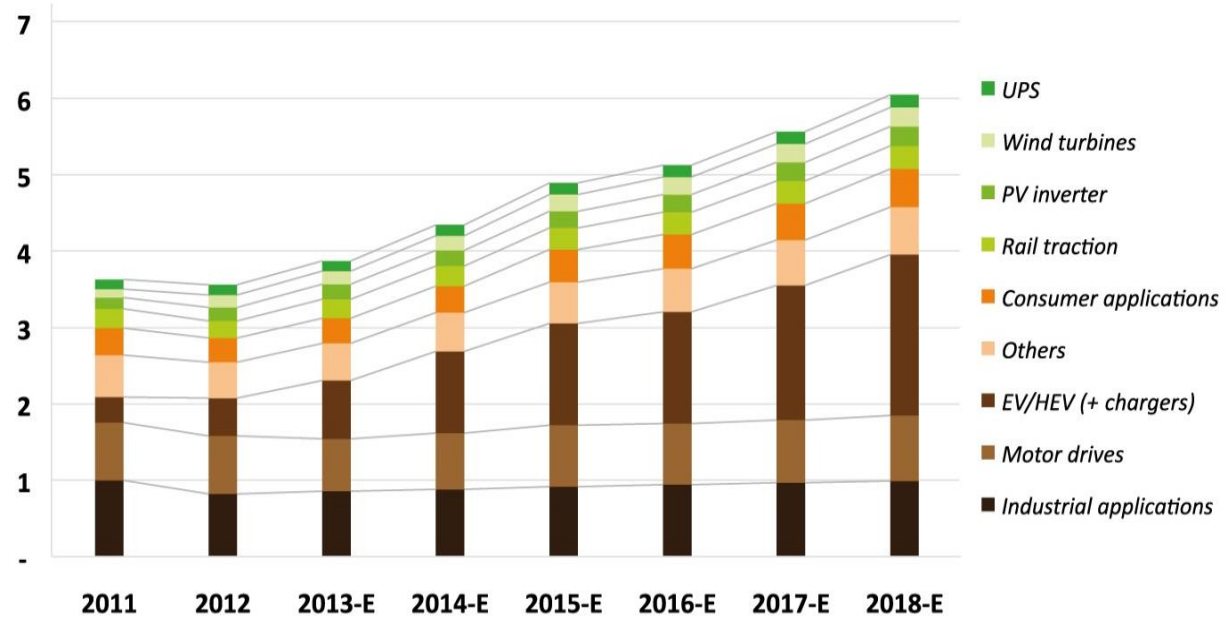

Fig. 1.2 : IGBT Market Forecast 2011-2018 (in $B) [2]

It becomes clear now that, with the major utilization of IGBT in electric drives for vehicles, efficiency and power loss become a critical issue to be handled. We find motivation in this respect to direct our research to overcome the challenges of reducing losses in IGBTs and bring about significant improvement that will help it to remain as the dominant power device in today's Industry.

1.2. Objectives of the Work

With the motivation to reduce the losses in IGBT, the industry today has recently incorporated thin wafer technology to IGBT. The basic principle is to use a thinner substrate for IGBT fabrication. The thinner substrate results in a lower resistance and in turn reduces power losses in IGBT.

But it comes with an added complexity. These thin wafers' thickness are in the order of 100µm, which are very thin and fragile and practically impossible to handle manually. They require dedicated robotic assembly to carry it along the entire process chain. Now, this is quiet acceptable for industry but for academic research, it is not feasible. And, if we cannot produce IGBT equivalent to what industry is producing today, how can we suggest or research improvements in the device.

The primary objective of my work is to answer the above question and come up with a feasible technology development for fabricating thin wafer IGBT without the resources of the industry. So, in a nutshell, we are not developing a new kind of IGBT but rather developing an ultra-thin substrate IGBT with the resources of an academic research laboratory like at IHT, and use it as a test vehicle to incorporate further modification to reduce the on-state losses in the IGBT.

1.3. Work Plan

Fig. 1.3 gives a graphical overview of the intended plan of this research work.

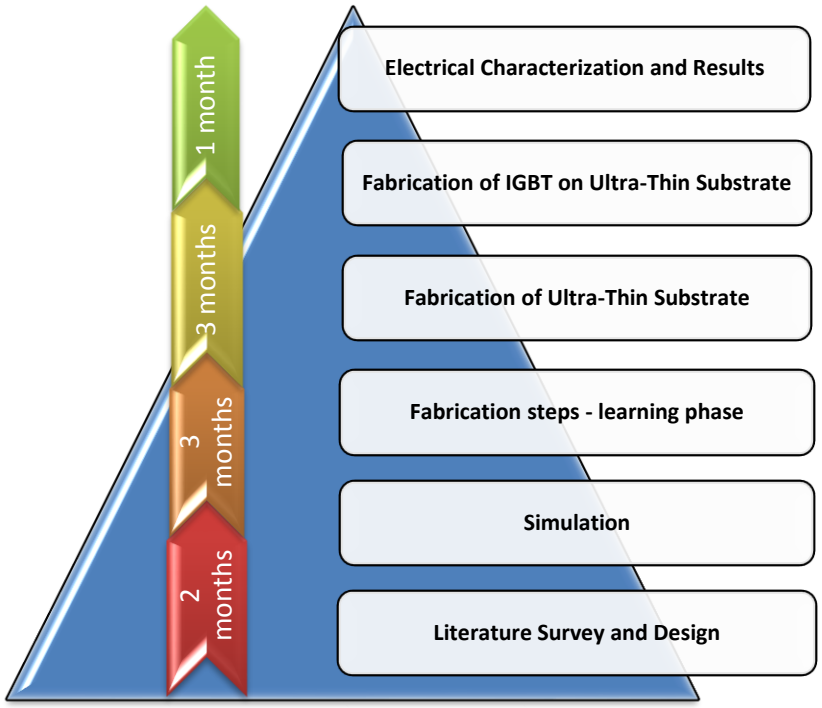

Fig. 1.3 : Graphical Thesis Plan

A step by step approach to this thesis work is described below:

- We begin with the initial literature survey and designing our device.
- We simulate the theoretical design to check feasibility and have a reference characterization of the device.
- Gain practical experience in semiconductor fabrication technologies.
- Technology development to fabricate Ultra-Thin Substrate.
- On these Ultra-Thin Substrates we fabricate IGBTs.
- We then perform the electrical characterization of the devices.
- And finally analyse the device performance of the fabricated devices.

2. Introduction

2.1. Evolution of Power Devices

The evolution of power semiconductor devices was sparked by the invention of power diodes by R.N. Hall in 1952. It was a germanium p-i-n with current rating of 35 A and reverse blocking voltage of 200 V. The improvement of the p-i-n diodes gave impetus to development of various rectifiers which formed the essential component in power conversion. It was followed by the development of the Schottky diode, with a metal-semiconductor junction which can operate with excellent speed and on-state performance but its leakage current is quiet high.

The era of Thyristors dawned in 1957, which quickly became the work horse of power electronics [3]. They have a very high reverse breakdown voltage, high current carrying capability and thus probably have the highest power density. However, these devices come with a major disadvantage that the Thyristor turn-off is passive, i.e. once the Thyristor is "Latched on" to the conducting state it cannot be turned off by external force. To turn off the device, the power applied to the device must be removed or reversed. TRIACs are also a variant in this category which are bidirectional device with a pair of Thyristor in anti-parallel configuration and has found a wide variety of application in alternating current domain [4].

In applications where active turn-on and turn-off of devices are required, power BJT greatly laid its foundation. Modular double or triple Darlington transistors were developed for switching frequencies up to several kHz [1]. Although power BJTs have fast switching capability, it needs very high base current drive in both on-state and during turn-off. A competing device with much higher forward current capability is the Gate turn-off Thyristors [5] which finds ample application in low frequency power systems like uninterruptable power supply (UPS), photovoltaic and fuel cell convertors etc.

The drastic development in MOSFET technology and the need for high speed power devices paved the way for the development of power MOSFETs in 1970s. These devices had excellent switching capabilities along with ease of drive and ability to withstand high rates of on-state voltage (dV/dt). However, power MOSFETs are majority carrier devices whose conduction are unipolar. So, they suffer from high on-resistance and are thus restricted to low power application. The innovation of the Cool-MOS concept [6] [7] [8] [9] is in the direction to reduce the on-resistance of power MOSFETs by addition of p-type strips in n-type drift region. These alternate types region creates a depleted space charge region when in reverse bias. The depleted region can block a higher reverse voltage with the same thickness of drift region or for a constant blocking voltage the doping of the drift region can be significantly increased, consequently decreasing the on-resistance of the device.

Thus, amongst the power devices discussed above, each offers a distinct advantage in certain application while being restricted to other domains due to their shortcomings. It was therefore a natural step to try and blend the properties of MOSFET and BJT into a single device. In the midst of various configuration developed to blend these properties

Insulated Gate Bipolar Transistor (IGBT) emerged to be the milestone breakthrough in the sphere of power semiconductor devices.

Fig. 2.1 gives a general classification overview of all the traditional power semiconductor devices found in today's technology.

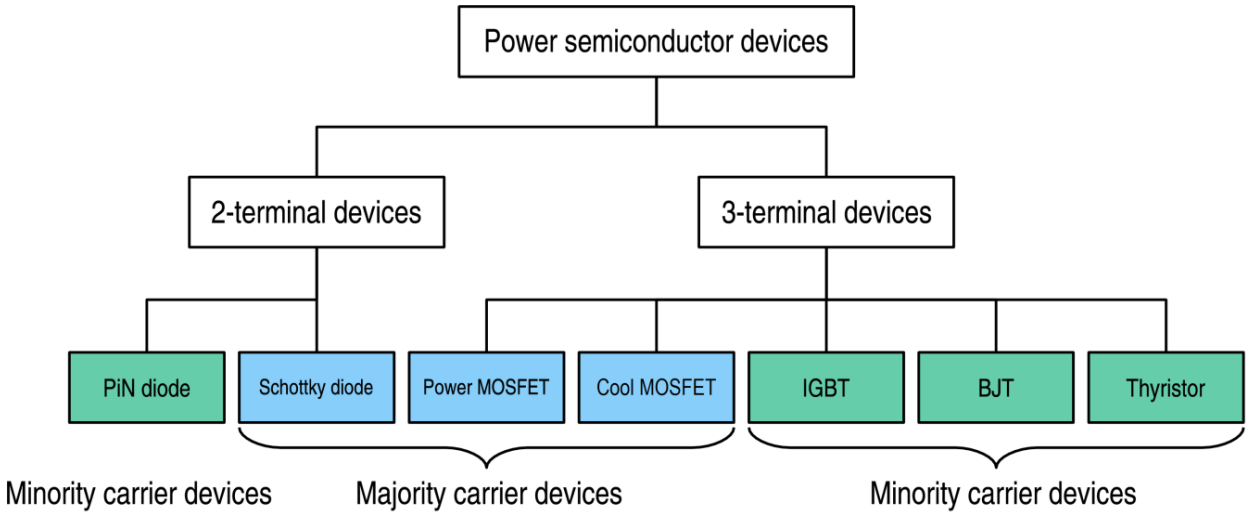

Fig. 2.1 : The power devices family, showing the principal power switches **[10]**.

2.2. Advent of IGBTs

IGBT was demonstrated for the first time by Baliga in 1979 [11]. Over the years it has been referred to by numerous other names which includes Insulated Gate Rectifier (IGR), Conductivity-Modulated FET (COMFET), Gain-Enhanced MOSFET (GEMFET), Bipolar FET (BiFET) and Injector FET. It became commercially available in 1983 [1].

IGBTs are inherently a minority carrier device where the current conduction takes place through both the majority and minority carriers of the semiconductor material it is composed of. It is generally viewed as a device with MOS input characteristics and bipolar output characteristics that is a voltage-controlled bipolar device. Indeed, in principle, it has a very high input impedance and large bipolar current-carrying capability thus allowing the users to combine the advantages of Power MOSFET and BJT into a single monolithic device.

IGBTs have found numerous applications in various power electronic systems, especially in Pulse Width Modulated (PWM) servo and three-phase drives requiring high dynamic range control and low noise. It is also an essential component in Uninterruptible Power Supplies (UPS), Switched-Mode Power Supplies (SMPS), and other power circuits requiring high switch repetition rates. IGBT improves dynamic performance and efficiency and reduces the level of audible noise. It is equally suitable in resonant-mode converter circuits. Optimized IGBT is available for both low conduction loss and low switching loss.

The main advantages [12] of IGBT can be summarized as:

- High Input Impedance.
- It has a very low on-state voltage drop due to conductivity modulation.
- It has superior on-state current density. So smaller chip size is possible and the cost can be reduced.
- Low driving power and a simple drive circuit due to the input MOS gate structure. It can be easily controlled as compared to current controlled devices (thyristor, BJT) in high voltage and high current applications.
- Wide Safe Operating Area. It has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking capabilities.

The main drawbacks that IGBTs suffer from are:

- Switching speed is inferior to that of a Power MOSFET and superior to that of a BJT. The collector current tailing due to the minority carrier causes the turnoff speed to be slow. This can be tackled by electron or proton irradiation at the expenditure of an increase in forward voltage drop.
- There is a possibility of latchup due to the internal PNPN thyristor structure.

2.3. IGBT Structure

Fig. 2.2 depicts the structure of a conventional IGBT unit cell. Amongst the numerous available structures for IGBT found today, this structure exhibits a feature of simplicity and acts as a base for evolution of other IGBT structures. Practically a power IGBT is composed of millions of array of such unit cells in order to meet the high current requirements.

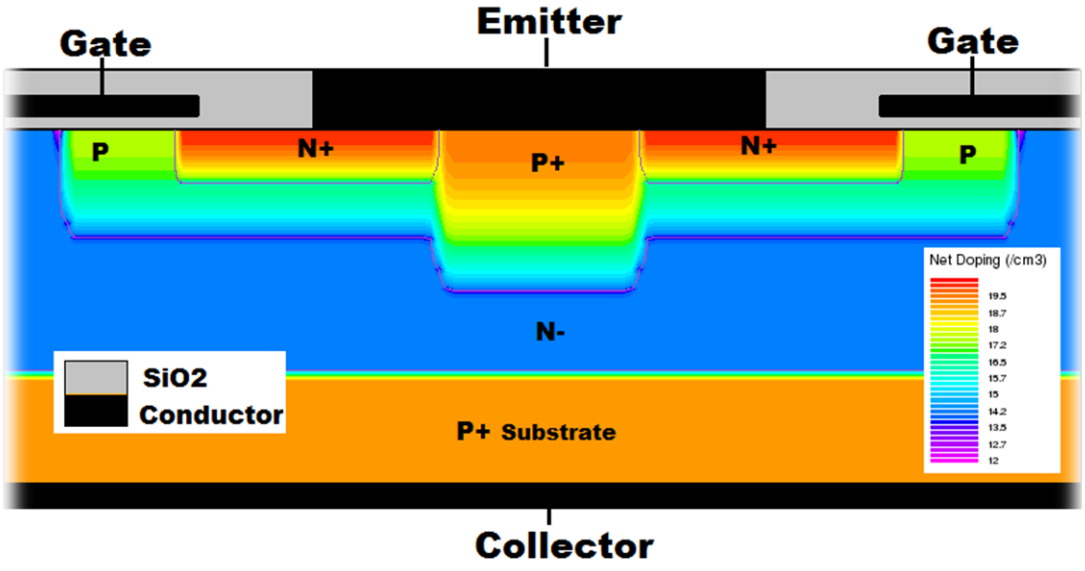

Fig. 2.2 : Conventional IGBT unit cell

IGBT also comprises of a NPNP structure like a thyristor. The top N^+ region of the device, acts as an *Emitter*, while the bottom P^+ region, functions like the *Collector* of the device. The device consist of two base regions, the shallow P region bellow the N^+ emitter is called the *P-Base* region and the central N^- region called the *N-Base* or *Drift region*. There also exists a P^+ region shorted to the N^+ region by the emitter metal contact known as the *Deep P^+ region*.

The MOS component of the IGBT is represented by the N^+ emitter, the P-Base and the N-Base regions. Here, it particularly functions as an N-channel enhancement MOSFET with the SiO_2 and gate structure above the P-Base channel region. The IGBT is controlled by switching this MOSFET on and off. Essentially, it can be said that the structure of an IGBT is similar to that of a vertical power MOSFET including the insulated gate structure and the shorted body (P type) – emitter (N^+ type) structure. But the only difference being the N^+ drain is replaced by a P^+ emitter region.

The thickness and doping concentration of the N^- drift region greatly influence the voltage ratings of the device. A thick or lightly doped drift region increases the voltage handling capacity of the device but also increases the on-state resistance of the device. On the other hand a thin or highly doped drift region gives a very low on-state resistance, thus low power loss, but decreases the voltage rating of the device. This is a crucial trade-off which an engineer has to consider while designing an IGBT. One has to tune the characteristics according to the application needs. A lot of research work is dedicated towards breaking this interdependency of voltage rating and on-state losses of IGBT. One of these methods is to introduce the COOLMOS concept into the IGBT forming a *Super-junction IGBT*, which is the intended future scope of this research thesis.

2.4. Equivalent Circuit of IGBT

To understand the basic functioning of IGBT, it becomes easier if we break the device into small fundamental component and study its equivalent circuit in order to get a clear picture of its operation. Fig. 2.3 depicts the various fundamental components of a conventional IGBT.

It consists of a pair of PNP and NPN transistor, which represents a thyristor. These transistor are represented as Q1 and Q2 respectively in Fig. 2.3 and are connected in a regenerative feedback loop configuration i.e. the collector of the PNP transistor is connected to the base of the NPN transistor, and likewise the collector of the NPN transistor supplies the base current for PNP transistor through the JFET, J1. Since we do not want this regenerative feedback loop to latch up and lose the gate control over the device, we short the base of the NPN transistor to its emitter via the emitter metallization of the IGBT. This ensures that the sum-total gain of the NPN and PNP transistor is less than unity.

$$\alpha_{NPN} + \alpha_{PNP} < 1 \qquad (2.1)$$

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However shorting resistance (R_S -Fig. 2.4 or R1-Fig. 2.3) between the base and emitter of the NPN transistor can trigger a latch up. If a high output current flows through this resistance, the voltage drop generated across it can turn on the NPN transistor automatically initiating an undesirable latch up. Amongst the various ways to reduce such risk, one solution is to increase the doping density of the deep P^+ region.

Since the NPN transistor is always turned off and the drift region is quiet thick to prevent the JFET from turning off, they can be neglected to arrive to a simplified equivalent circuit as indicated by Fig. 2.4. The resulting circuit contains two components only. Therefore, the IGBT is a PNP bipolar transistor driven by a N-channel enhancement MOSFET forming a pseudo-Darlington configuration [1].

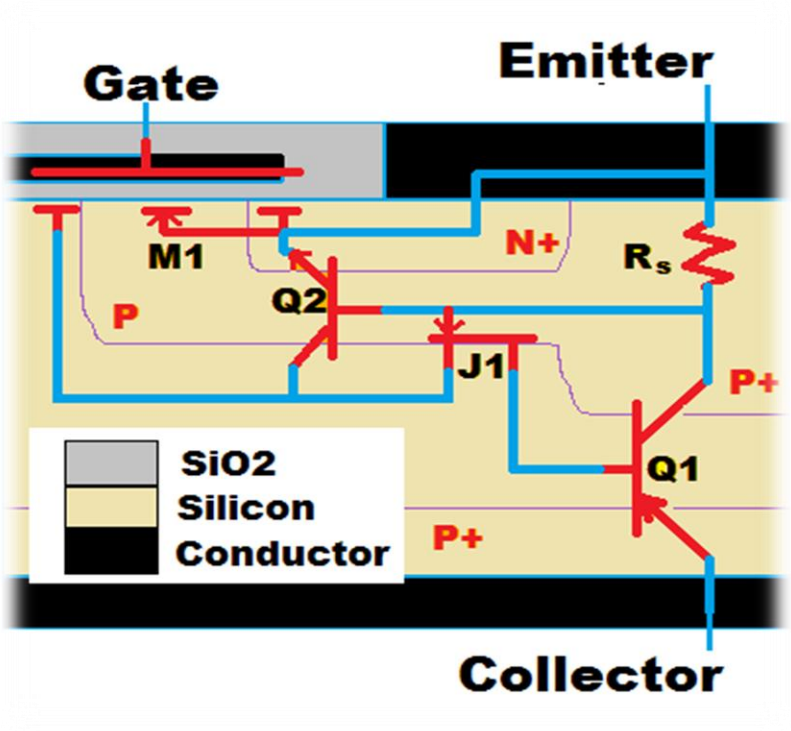

Fig. 2.3 : Fundamental components in IGBT

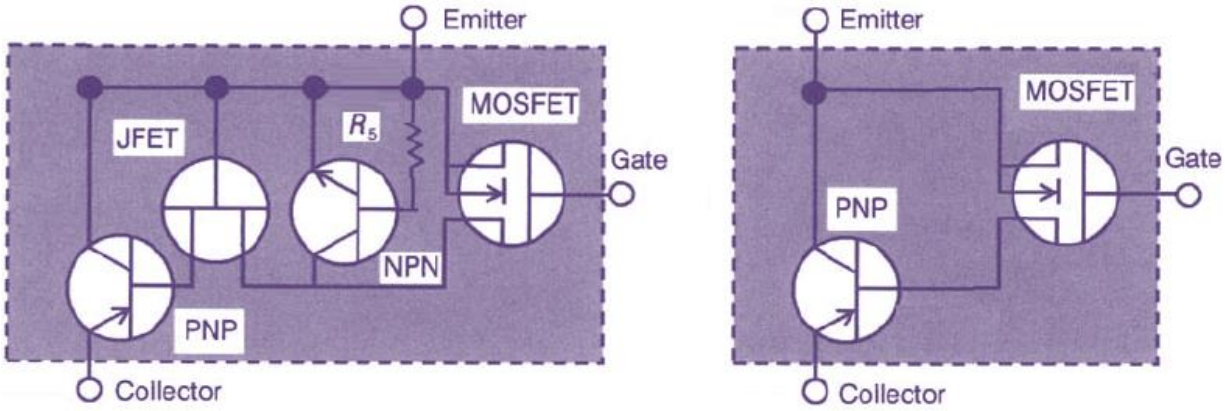

Fig. 2.4 : (Left) Equivalent circuit, (Right) Simplified Equivalent circuit **[1]**

2.5. IGBT Operational Modes

IGBT has three operational modes based on the biasing of the emitter, gate and collector.

2.5.1. *Reverse Blocking Mode*

The IGBT operates in this mode when a positive bias is applied to the Emitter and a negative bias is applied to the collector contact while the gate is shorted to the emitter. In this mode, as shown in Fig. 2.5, junction J1 is forward biased while J1 and J3 are reverse biased. These reserve biased p-n junctions are responsible for blocking any current flow through the device and giving the reverse blocking characteristics.

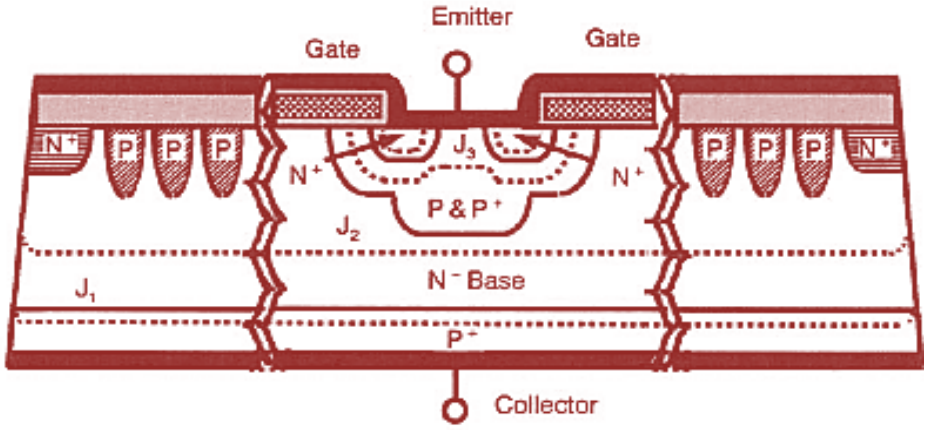

Fig. 2.5 : Reverse Blocking Mode of IGBT **[13]**

The majority of voltage is blocked by the junction J1 whose space charge region penetrates deep into the N-Base region. Thus the doping characteristics and the thickness of this region play a crucial role in determining the blocking voltage of the device. If this region is too thin or very lightly doped then the space charge region may encompass the entire N-Base region till the P-Base region causing punch-through and initiating breakdown of the device. In order to determine optimized trade-off between N-Base thickness (d), doping concentration (N_D) and maximum breakdown voltage (V_{max}) the following relation can be used

$$d = \text{Depletion width at } V_{max} + \text{one minority carrier diffusion length}(L_P) \quad (2.2)$$

$$d = \sqrt{\frac{3\varepsilon_0 \varepsilon_S V_{max}}{qN_D}} + L_P \quad (2.3)$$

where,

ε_0 = permittivity of free space
ε_S = dielectric constant of Si
q = the electronic charge and

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At very high voltage ratings only the first term is dominating so the thickness of the N-Base region is proportional to $\sqrt{V_{max}}$.

A conventional IGBT as shown in Fig. 2.2 was simulated in Silvaco ATLAS to study the variation in electric field in this mode and is represented in Fig. 2.6. It can be seen that the electric field increases with the application of higher reverse voltage and can reach a maximum up to 2 x 10^5 V/cm at junction J1. Also with the increase in reverse voltage the electric field penetrates deeper into the N-Base region along with the depleted region and just before breakdown the electric field approaches junction J2. This condition is depicted by the curve V_{ce} = -750V (N-base region thickness of 70µm) (Fig. 2.6).

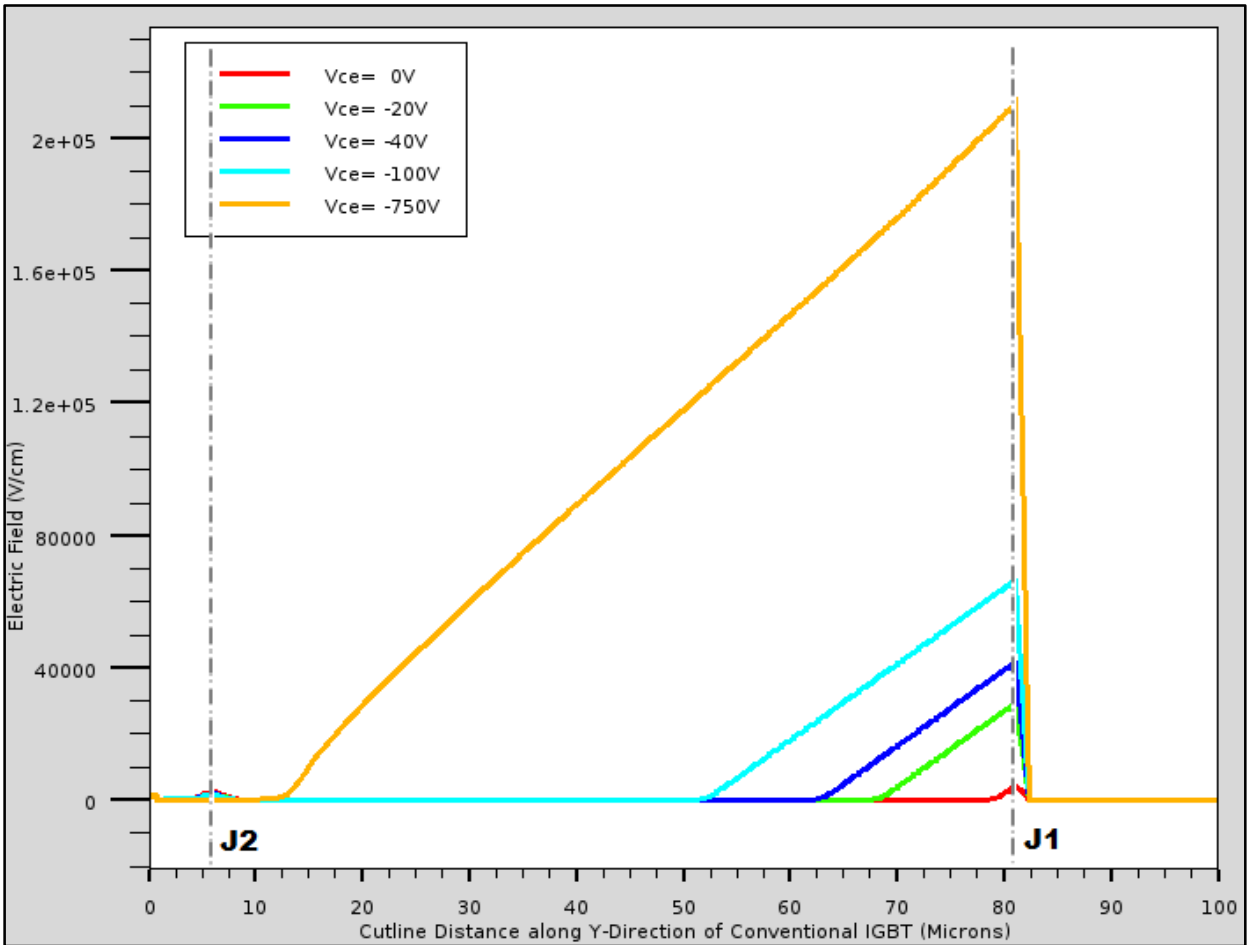

Fig. 2.6 : Electric Field Simulation - Reverse Blocking Mode in Conventional IGBT

2.5.2. Forward Blocking Mode

In this mode, the biasing is reversed as compared to the previous mode while the gate is still shorted to the emitter i.e. the P^+ collector is positive biased while the N^+ emitter is negative biased. This makes the junction J1 and J3 (Fig. 2.7) forward biased but the device is still not in conduction state because junction J2 is reverse biased, withstanding the entire applied voltage across itself. The space charge region stretches partly into the P-Base while penetrating deep into the N-Base region.

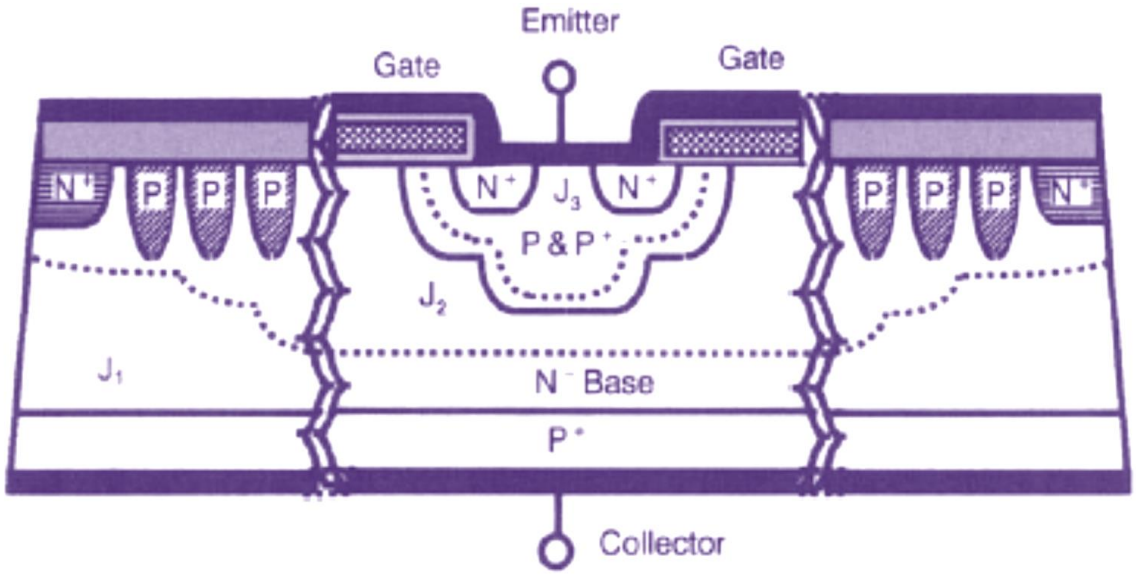

Fig. 2.7 : Forward Blocking Mode of IGBT **[13]**

Again with the help of simulation we tried to study the electric fields in the forward blocking mode and are represented in Fig. 2.8.

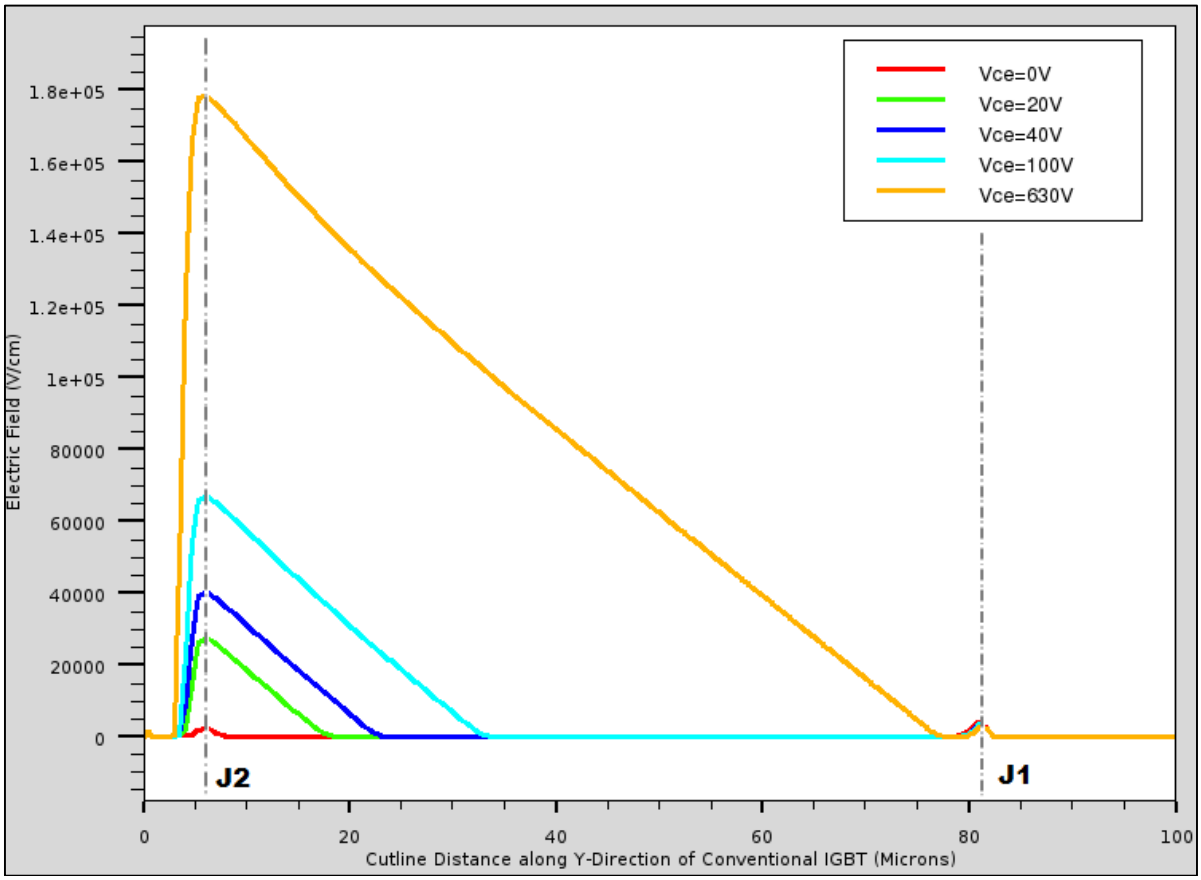

Fig. 2.8 : Electric Field Simulation - Forward Blocking Mode in Conventional IGBT

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It can be observed that the applied voltage is blocked by the electric field at junction J2 reaching to a maximum of about 1.8 x 10^5 V/cm and penetrates more into the N-Base region due to its low doping concentration. As the electric field penetrates deeper with increase in collector voltage a point is reached where it approaches the junction J1. This is the maximum voltage that the device can block because the N-Base region is completely depleted and any further increase in collector voltage causes breakdown.

2.5.3. Forward Conduction mode

IGBT can be brought from forward blocking mode to forward conduction mode by removing the gate emitter short circuit and applying a positive bias to the gate. This voltage should be high enough to invert the P-Base region below it. The N-channel formed in the P-Base region bridges the N^+ emitter and the N-base transporting large amount of electrons into the N-Base region. This makes the junction J1 forward biased and conducting (Fig. 2.9). A large amount of holes (minority carriers) are injected into the N-Base from the P^+ collector region. For this reason the collector is also referred to as the *Injector region* in IGBT.

The injected minority carriers initiate the process of conductivity modulation of the N-Base where the plasma of holes in this region attracts electrons from the emitter side in order to maintain the charge neutrality. The holes from the N-base region can easily pass the space charge region of the reversed biased junction J2 as they are minority carriers and face no hindrance from the electric field present there. The holes that are injected right below the gate region traverse a rectilinear path upward until it is repelled by the positive bias of the gate and then is deflected towards the emitter again (Fig. 2.10). The electrons on the other hand travel from the N^+ emitter through the N-channel to the N-Base and eventually end up at the collector region. Both of these constitute a large current flow and transfer the device into conduction mode with a very low on-resistance.

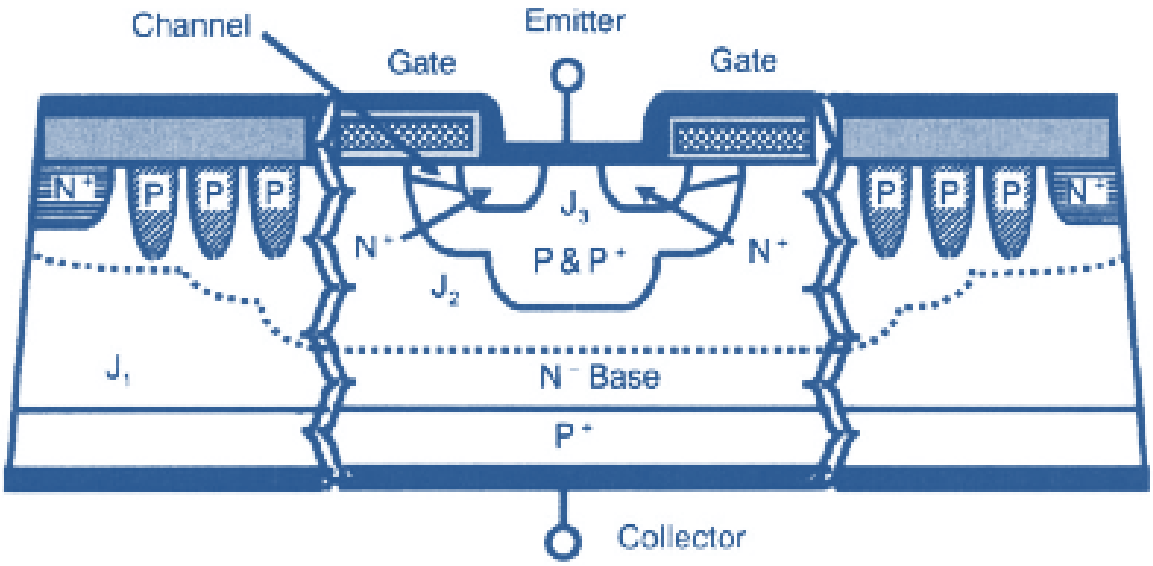

Fig. 2.9 : Forward Conduction Mode of IGBT **[13]**

The saturation of the forward current in IGBT is not solely dominated by the current saturation in the channel region of the MOS component of IGBT but is also controlled by the current gain of the PNP transistor (α_{pnp}).

$$\alpha_{pnp} = \frac{1}{\cosh\left(\frac{W}{L_p}\right)} \qquad (2.4)$$

Where,

W = width of the undepleted N-base region
L_p = minority carrier (hole) diffusion length in N-base region

Therefore as W decreases the gain of the PNP transistor falls and contributes to the saturation of the forward current.

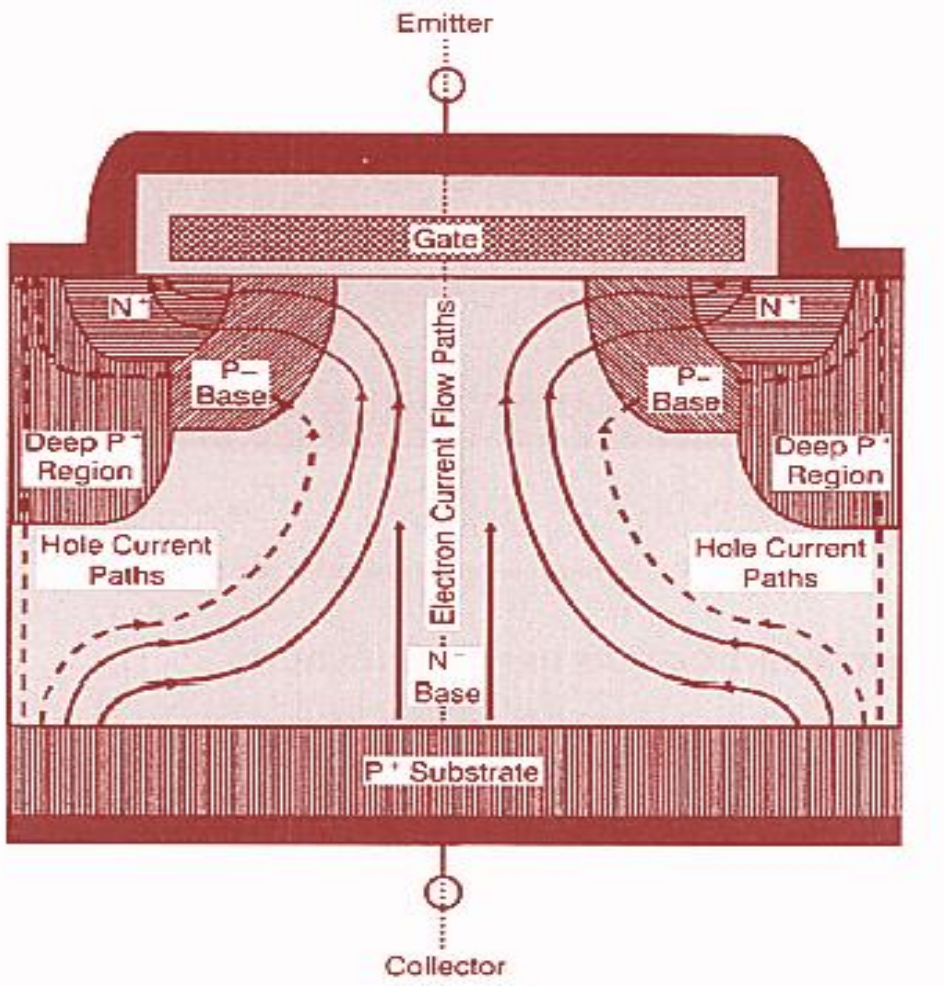

Fig. 2.10 : Electron and hole current flow path **[1]**

The device can be turned off by simply removing the positive bias to the gate. This destroys the N-channel in the P-Base region and cuts off the electron flow path. Once this is stopped, the injection of holes from the collector stops which puts an end to the conductivity

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modulation of the N-Base region. Ultimately the device turns off returning it to forward blocking mode.

2.6. Static Characteristics of IGBT

The static characteristics of IGBT include two families of curves, the output characteristics and transfer characteristics.

2.6.1. Output Characteristic

Fig. 2.11 shows the output characteristics of an conventional IGBT. In this family of curves, each trace is obtained by measuring the collector current (I_{CE}) as a function of collector-emitter voltage (V_{CE}) with constant and distinct the gate-emitter voltage (V_{GE}) constant. In the first quadrant the characteristics have a distinguished feature. Even if a MOSFET channel of the input side is formed, by application of forward bias to gate voltage, the collector current does not flow if the collector-emitter forward voltage drop does not exceed approximately 0.7V. The entire family of curves is translated from the origin by this voltage magnitude. It may be recalled that with a P^+ collector, an extra P-N junction has been incorporated in the IGBT structure. This P-N junction makes its function fundamentally different from the power MOSFET.

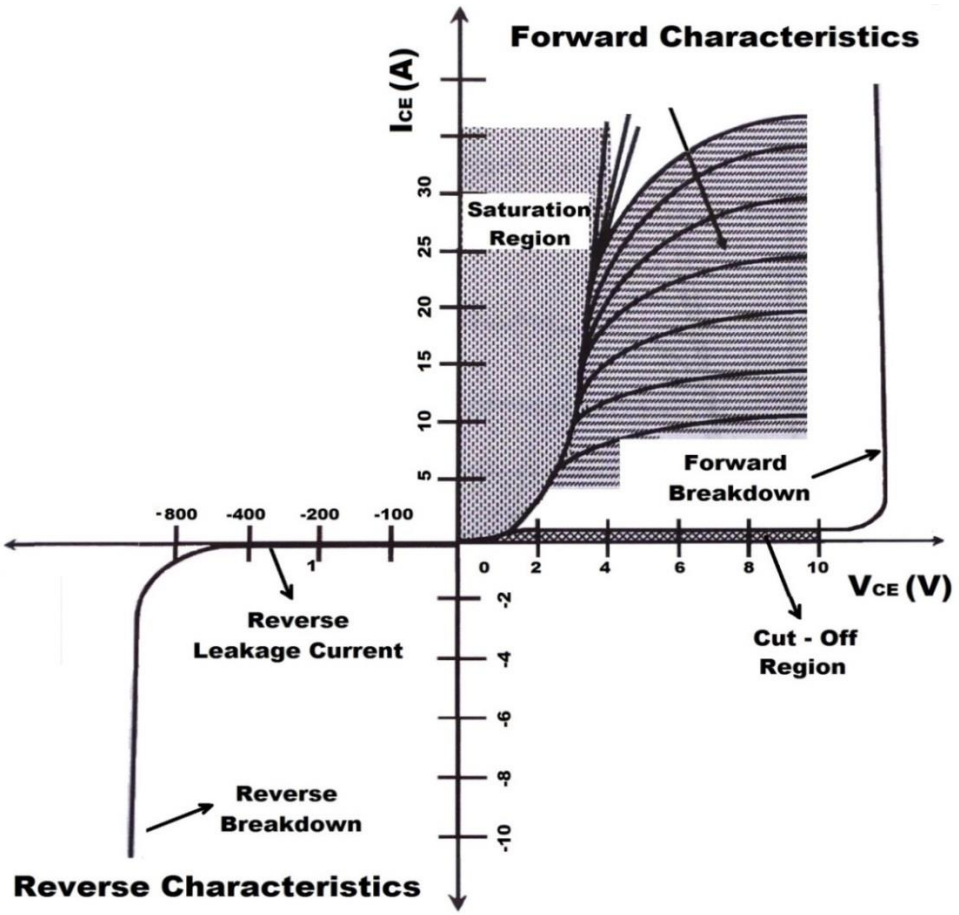

Fig. 2.11 : Output Characteristics of IGBT **[13]**

If no gate voltage is applied and V_{CE} is increased beyond 0.7V the IGBT remains in Cut-Off region and only negligible minority carrier current flows through the device. This corresponds to the *forward blocking mode*. On further increase in V_{CE}, a point is reached when the device enters breakdown and starts conducting even without the gate voltage. On the other hand when a sufficient gate voltage is applied and V_{CE} is increased beyond 0.7V the current, IGBT enters into *forward conduction mode*. In this mode, I_{CE} rises steeply first, then constitutes the linear region and eventually saturates when the channel is pinched off. Once the device saturates ideally it has infinite output resistance but the current I_{CE} increases slightly with increase in V_{CE}. This finite resistance is due to the channel pinch-off phenomenon in MOSFETs. With an increase in gate voltage in this region we see an upward shift of the curves forming a family of curves over a range of gate voltage.

In the reverse region, when a negative bias is applied to the collector the IGBT is forced into *reverse blocking mode* where only a negligible reverse current flows. This current also contributes to the power loss in IGBT modules as is kept as low as possible and is primarily proportional to the operating junction temperature. As the negative bias is increased there comes a point where the space charge region of junction J2 (Fig. 2.5) reaches the collector region and the device breakdown occurs. This is an important rating for the IGBT specification and is dependent on the doping concentration and thickness of the drift region.

2.6.2. Transfer Characteristic

Fig. 2.12 depicts the transfer characteristics of a conventional IGBT for various temperature range. These family of curves are obtained by recording the collecter current while sweeping the gate voltage over a particular range.

The transfer characteristics of an IGBT is similar to that of a power MOSFET only with a higher level of current due to the bipolar current gain in IGBT. The intersection of the tangent to the curve in the linear region with the x-axis gives the *Threshold Voltage* (V_{Th}) of the IGBT. Some literatures also define the threshold voltage as

$$V_{Th} = V_{GE} \mid_{I_{CE} = 1\,mA \,\&\, V_{CE} = 10V} \quad (2.5)$$

Another important parameter obtained from the transfer characteristics is the *Transconductance (g_m)* of the IGBT. It is also a direct measure of the inverse of on-resistance of the IGBT. It is calculated from the slope of the curve in the linear region

$$g_m = \frac{\partial I_{CE}}{\partial V_{GE}} \Bigg|_{V_{CE} = Constant} \quad (2.6)$$

The transconductance of the IGBT increases rapidly with low collector current, then levels as the MOSFET current saturates, limiting the base drive of the bipolar component of IGBT (Fig. 2.13). For further increase in collector current the transconductance again starts decreasing because of the thermal constraints of the device and the saturation of the

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bipolar component. It is also observed that the transconductance also decreases with the increase in operating temperature which is also supported by the fact that the on-resistance of a device increases with temperature due to increased brownian motion of charge carriers.

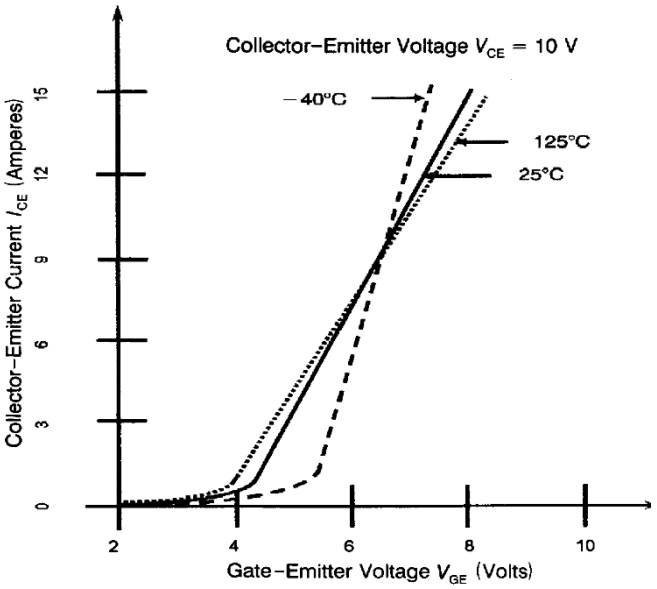

Fig. 2.12 : Transfer Characteristics of IGBT **[13]**

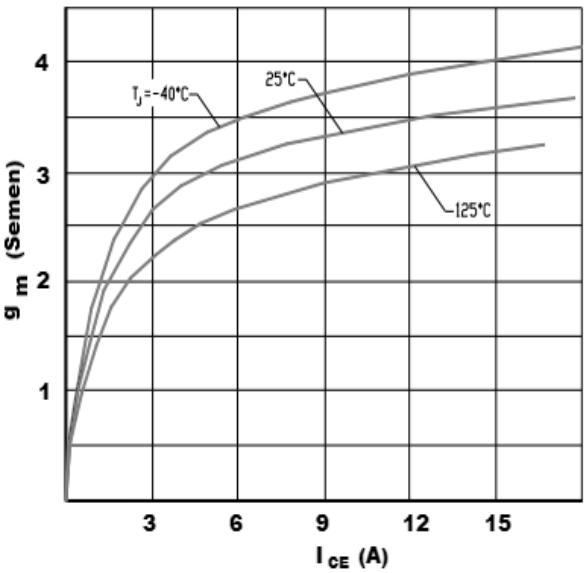

Fig. 2.13 : Transconductance curve of IGBT **[12]**

2.7. Types of IGBTs

In this section we present a short discussion about the basic types of IGBT existing today and from which the concept of the device we fabricate tends to originate.

2.7.1. Punch-Through IGBT

In conventional IGBT also known as *Non Punch-Through (NPT) IGBT* the forward and reverse breakdown voltage is in the same range due to the symmetric device structure. But if this is not required, i.e. the maximum reverse blocking voltage rating is permitted to be lower (like in DC circuits) the symmetry can be compromised for lower on-resistance by adding a N^+ buffer layer between the N-base and collector region. This device is known as *Punch-Through (PT) IGBT* (Fig. 2.14).

The additional N buffer layer provides a constant undepleted region which prevents the current gain of the PNP transistor from saturating and thus giving lower on-resistance. This structure was also simulated and the electric fields and breakdown voltage were extracted and from the results obtained the forward breakdown voltage increases by a factor of approximately 2 and the reverse breakdown voltage decreases by a factor ranging from 6 to 10 with variations in thickness of the buffer layer. It can also be concluded from this that if we desire a fixed forward breakdown voltage, we can achieve it with a thinner N-base drift region and thus reducing the On-resistance of the device. However, the

thickness of the buffer layer should be kept as low as possible as it brings about a significant lowering of the switching speed of the device. The electric fields of a PT IGBT in forward blocking mode are depicted in Fig. 2.15.

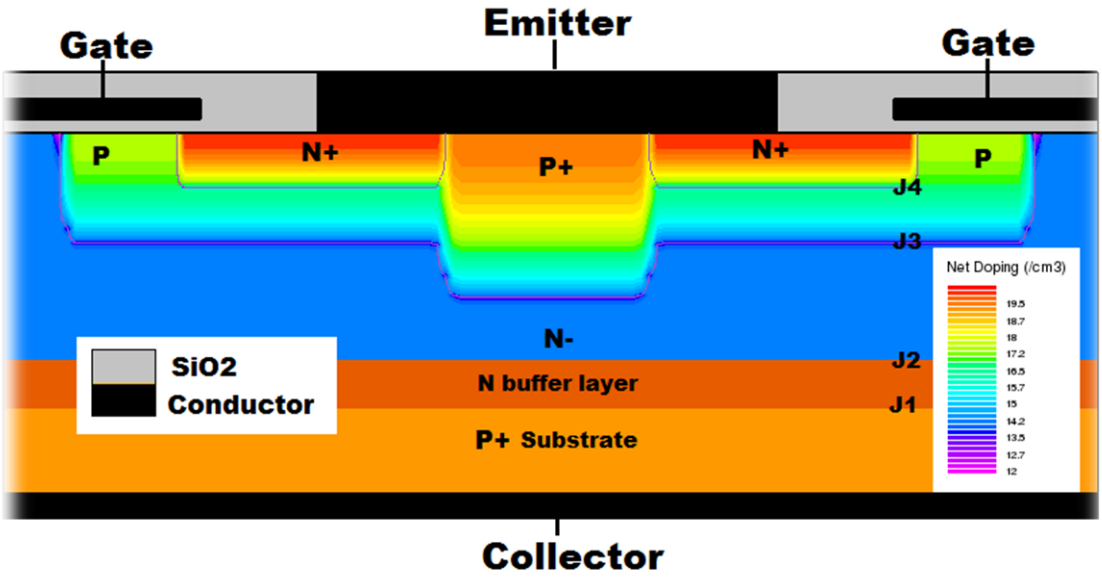

Fig. 2.14 : Punch-Through IGBT

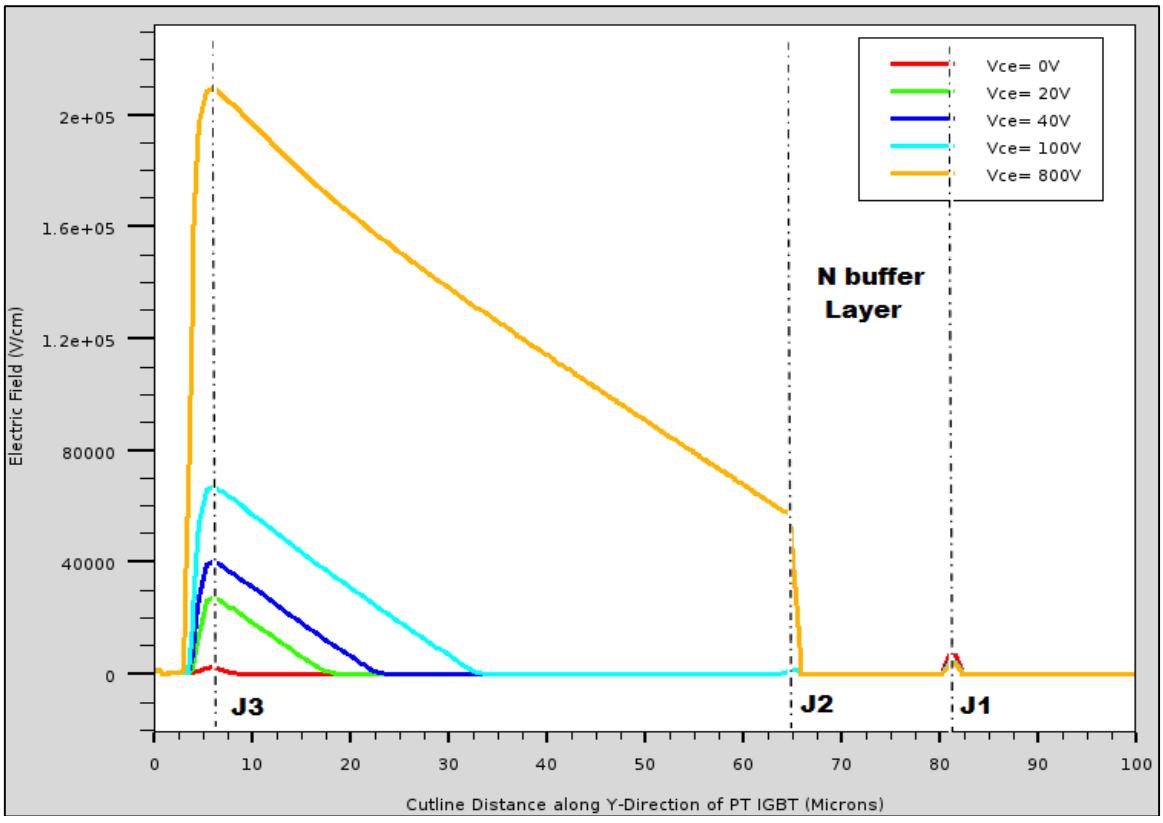

Fig. 2.15 : Electric Field Simulation - PT IGBT

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It can be seen that the electric fields abruptly stop at the N buffer layer and provide for higher forward breakdown voltage at the cost of reverse breakdown voltage. Thus it is a trade-off between switching speed, forward blocking characteristics, reverse blocking characteristics and On-resistance.

2.7.2. Trench Gate IGBT

In forward mode of conventional IGBT there is an immense current and electric field crowding in the N-base region directly below gate. In this region the holes injected by the P+ collector travel up to the gate region and then get repelled by the positive gate voltage towards the emitter. Also, the electrons enter this region through the channel formed. Furthermore, due to the reversed biased junction between emitter and N-base region there exists a very high electric field. Both these condition does not allow sufficient conductivity modulation in this region and contributes to a high on –resistance.

Both the current and electric field crowding can be eliminated by an IGBT with a trench gate structure (Fig. 2.16). In this structure a vertical channel is formed, reducing any lateral component of electron or hole current. Also the paths traversed by the current carriers are reduced resulting in reduction of effective on-resistance of the device. The vertical gate structure also reduces the cell size without compromise on gate length and therefore increases the packing density of the IGBT cells.

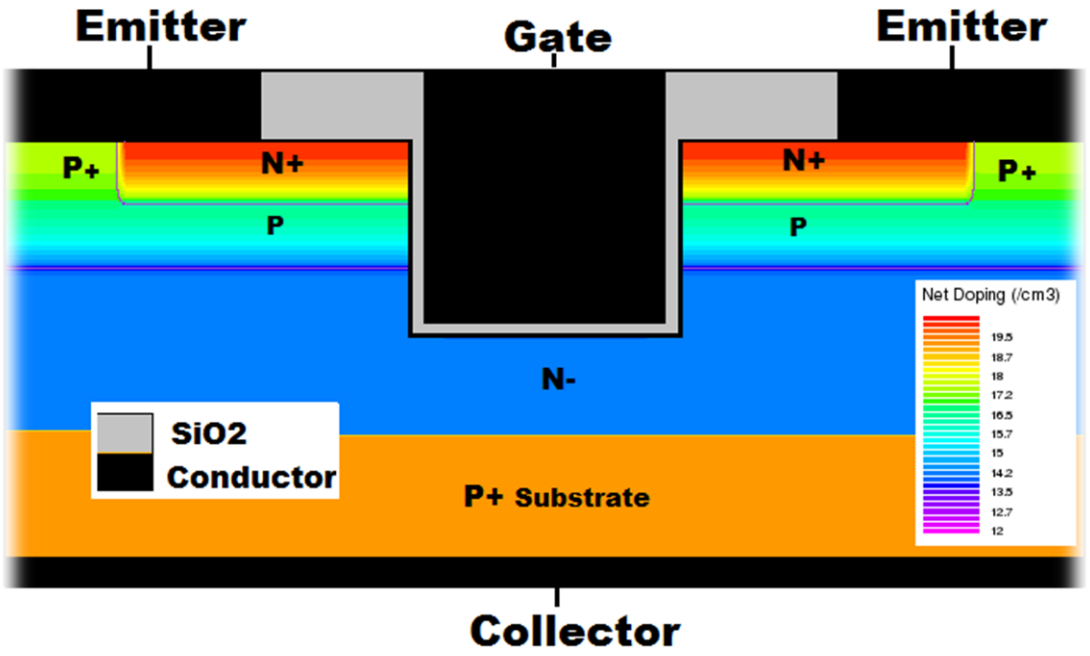


Fig. 2.16 : Trench Gate IGBT

3. Ultra-Thin Substrate IGBT

3.1. Device Structure

The main goal of this research thesis is to fabricate an IGBT on Ultra-Thin Substrate to minimize the power losses of the device. In the previous section we saw the advantages of a Trench-Gate IGBT where the current carriers had to travel a shorter vertical path along the device with minimal lateral component resulting in having a smaller on-resistance. We further try to modify this structure and remove unwanted regions wherever possible.

The Trench-Gate IGBT (Fig. 2.16) is fabricated on a P^+ substrate which generally is around 550µm thick. The thick N-base region is grown over it, consuming a lot of time, followed by double diffusion of the channel region and emitter region. The P^+ collector region is not needed to be thick but since during fabrication we have to start with a base substrate we are forced to use it for the collector region making it unnecessarily thick. This thick substrate, although having a very high doping concentration, adds to a resistance in the current flow path.

A solution to above problem is the use of Ultra-Thin Wafers [14] as the base substrate of the IGBT which are in the order of 100µm thick. With wafers of such dimensions we can use it as the N-base region and then grow very thin layer of P^+ collector region on the bottom side of the substrate in the orders of few hundred nano-meters. Thus a 550 µm collector region is reduced by around a factor of 1000. Also, with this method the processing time to deposit a 100 µm thick N-base region over a P^+ substrate in Trench-Gate IGBT is removed.

If we look closely to the Trench-Gate IGBT structure (Fig. 2.16), the channel region directly below the emitter contact is highly doped in order to reduce the on-resistance and have a good ohmic contact with the emitter while the rest of the channel region is moderately doped. Due to the limitations of the diffusion process to form the channel and emitter region the resultant channel length is in the range of a 1-5 µm. However, with the high end *Molecular Beam Epitaxy* (MBE) machine we are equipped with in our research facility at our institute, epitaxial growth is possible to get thin mono-crystalline layers of any thickness down to some single atom layer of high crystal perfection and purity. This allows for a much thinner channel length and to support the voltage rating of the IGBT the concentration of the channel region is also increased to form a P^+ channel. The thinner and heavily doped channel region accounts for a much lower channel resistance.

An added advantage comes with making the channel region heavily doped is that we do not need a separate P^+ region to make an ohmic contact with the emitter metal. The entire P^+ region having a finite resistance in the Trench-Gate IGBT can be removed and the emitter metal can be made to penetrate down to the channel region.

With all the above modification we designed our Ultra-Thin Substrate IGBT as shown in Fig. 3.1. The thin wafer substrate serves as an N-base region. On it bottom side a thin layer of P^+ collector region is deposited by MBE and on the top side a layer of P^+ channel region and a

N^+ emitter region is grown by MBE. The fabrication of the device is discussed in details in Section 5.

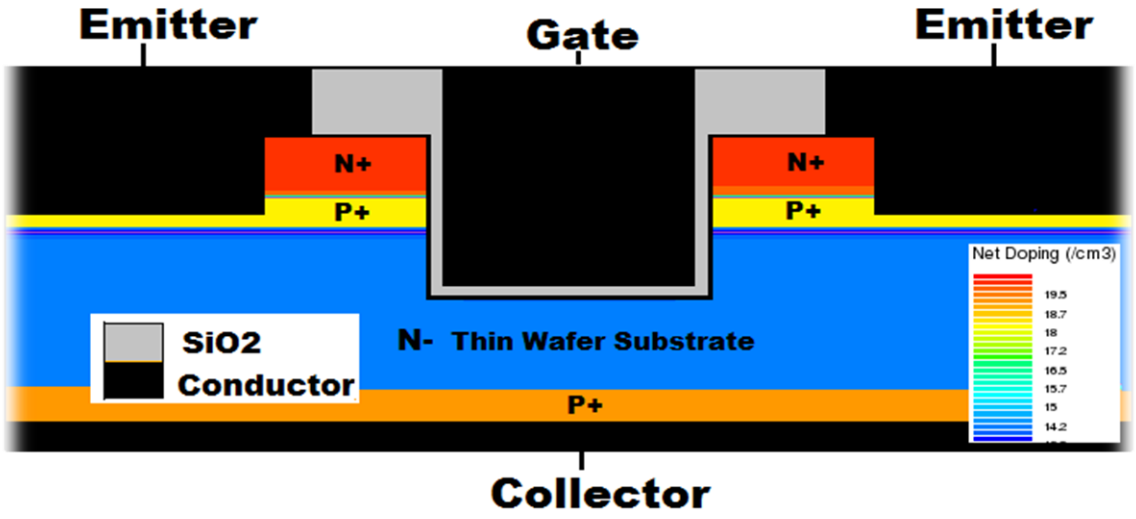
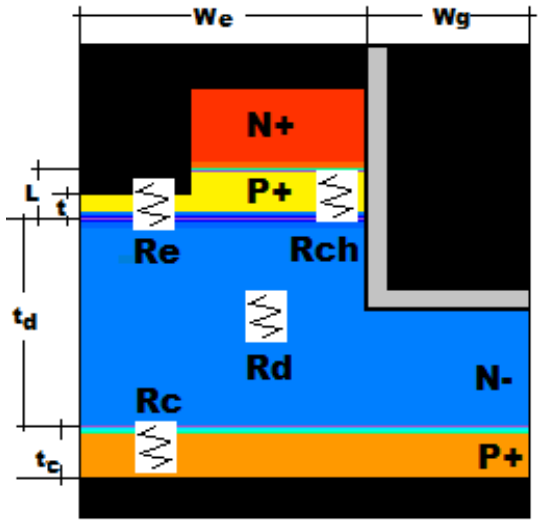


Fig. 3.1 : Ultra-Thin Substrate IGBT

3.2. On-Resistance of MOS component

In the following section the equations for the on-resistance of the Ultra-Thin Substrate IGBT is discussed along with its various components. It is composed of four major parts as shown in Fig. 3.2

- The resistance of the emitter P^+ region (R_e)
- The resistance of the channel region (R_{ch})
- The resistance of the N-base drift region (with current scattering) (R_d)
- The resistance of the collector P^+ region (R_c)



Total on resistance is given by

$$R_{ON} = R_{ch} \,||\, R_e + R_d + R_c \qquad (3.1)$$

Fig. 3.2 : Resistance components of a half Ultra-Thin Substrate IGBT cell

The channel resistance R_{ch} is given by

$$R_{ch} = \frac{L\,(W_e + W_g)}{\mu_n C_{ox}(V_G - V_{th})} \quad (3.2)$$

Where,

μ_n = electron mobility in the channel region
C_{ox} = Gate oxide capacitance per unit area

It can be noted that as compared to the Trench-Gate IGBT, which has a channel length of 5µm, the channel length of Ultra-Thin Substrate IGBT is around 10 times smaller. Hence, the channel resistance is also reduced by a factor of 10.

The drift resistance with consideration of current spreading from the emitter to the collector of the N-base region R_d is given by

$$R_d = \rho_d \left\{ (W_e + W_g)\,.\, ln\left(1 + \frac{W_e}{W_g}\right) + (t_d - W_e) \right\} \quad (3.3)$$

Where,

ρ_d = resistivity of the ultra-thin wafer

The emitter resistance R_e is given by

$$R_e = \rho_{n+}\,.\,t \quad (3.4)$$

Where,

ρ_{p+} = resistivity of the N+ emitter region

As compared to a Trench-Gate IGBT the dimension of '*t*' in Ultra-Thin Substrate IGBT is smaller by a factor of 10. So, proportionately the emitter resistance of the Ultra-Thin Substrate IGBT is reduced by a factor of 10.

And lastly the collector resistance R_c is given by

$$R_c = \rho_{p+}\,.\,t_c \quad (3.5)$$

Where,

ρ_{p+} = resistivity of the P+ collector region

As compared to a Trench-Gate IGBT the dimension of 't_c' in Ultra-Thin Substrate IGBT is smaller by a factor of 1000. So, proportionately the collector resistance of the Ultra-Thin Substrate IGBT is reduced by a factor of 1000.

Note: all the above equations are derived from the resistance component of an UMOSFET [15] which has similar structure to our device.

4. Simulations

4.1. ATLAS a Physically-Based Simulator

All the simulations involved in this thesis are done with ATLAS from SILVACO which is a physically-based two and three dimensional device simulator. It predicts the electrical behaviour of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation [16].

Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions [16]. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid it is possible to simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modelled in DC, AC or transient modes of operation.

The major advantages of Physically-based simulation are: it is predictive, it provides insight, and it captures theoretical knowledge in a simplified version.

Physically-based simulation is different from empirical modelling. The objective of empirical modelling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge. Physically-based simulation is an alternative to experiments as a source of data [16].

Physically-based simulation has become very important for two reasons. Firstly, it is almost always much quicker and cheaper than performing experiments. Secondly, it provides information that is difficult or impossible to measure [16]. The drawbacks of simulation are that all the relevant physics must be incorporated into a simulator, and numerical procedures must be implemented to solve the associated equations. These tasks have been taken care of for users of ATLAS. Users of physically-based device simulation tools must specify the problem to be simulated. Users of ATLAS specify device simulation problems by defining:

1. The physical structure to be simulated
2. The physical models to be used
3. The bias conditions for which electrical characteristics are to be simulated.

ATLAS here is used in conjunction with the VWF INTERACTIVE TOOLS [16]. These include DECKBUILD, TONYPLOT, DEVEDIT, ATHENA and many more. DECKBUILD provides an interactive run-time environment. TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement while ATHENA servers for semiconductor process simulation.

The interaction overview of ATLAS with other tools is shown in Fig. 4.1

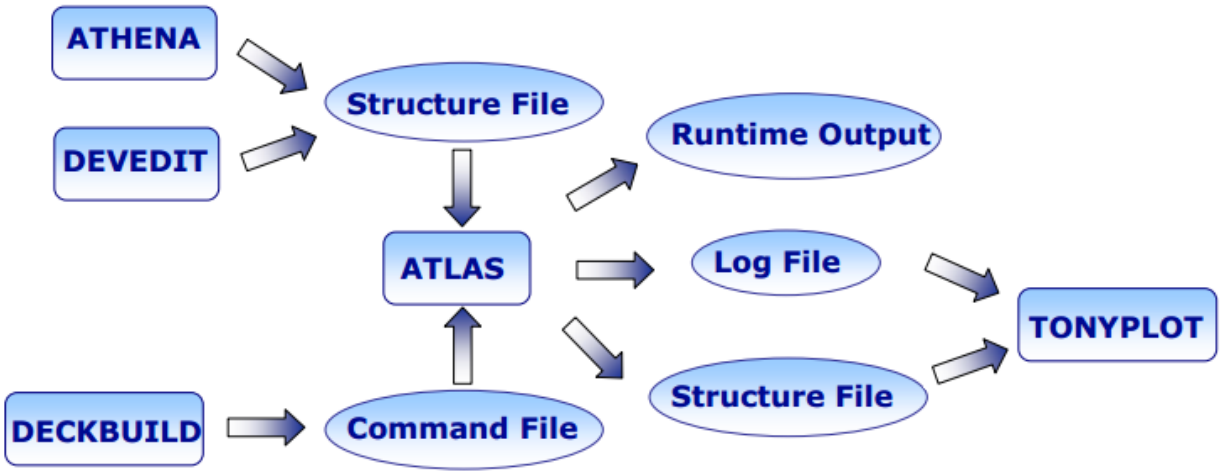


Fig. 4.1 : Interaction with ATLAS software

We use the DECKBUILD command file input for the ATLAS environment to build our Ultra-Thin Substrate IGBT and utilize all the three outputs as well as TONYPLOT to conclude and visualize the simulated results.

The elements in an ATLAS input deck consist of various statements. The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order

Group	*Statements*
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Models Specification	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

Fig. 4.2 : Elements of ATLAS input deck in correct order **[16]**

Each statement consists of a keyword that identifies the statement and a set of parameters. The general format is:

<STATEMENT> *<PARAMETER>=<VALUE> <PARAMETER>=<VALUE>……*

An example of a statement line is:

DOPING *uniform n.type concentration=1.0e16 region=1 outfile=my.dop*

The statement is DOPING. All other items are parameters of the DOPING statement. UNIFORM and N.TYPE are logical parameters. Their presence on the line sets their values to true. Otherwise, they take their default values (usually false). CONCENTRATION is a Real parameter and takes floating point numbers as input values. REGION is an Integer parameter taking only integer numbers as input. OUTFILE is a Character parameter type taking strings as input. The statement keyword must come first but the order of parameters within a statement is unimportant [16].

4.2. Ultra-Thin Substrate IGBT Device Structure

The structure simulated in the following section is in accordance to the fabricated device we discuss in the next chapter. The structure involves a 98.9µm N-base region with a epitaxial layer in the bottom side 400nm thick which serves as the collector and on the top side first the epitaxial P^+ channel layer of thickness 300nm and over that a 400nm N^+ layer forming the emitter region. All the simulation is done with a half cell structure of the IGBT structure shown in Fig. 4.3.

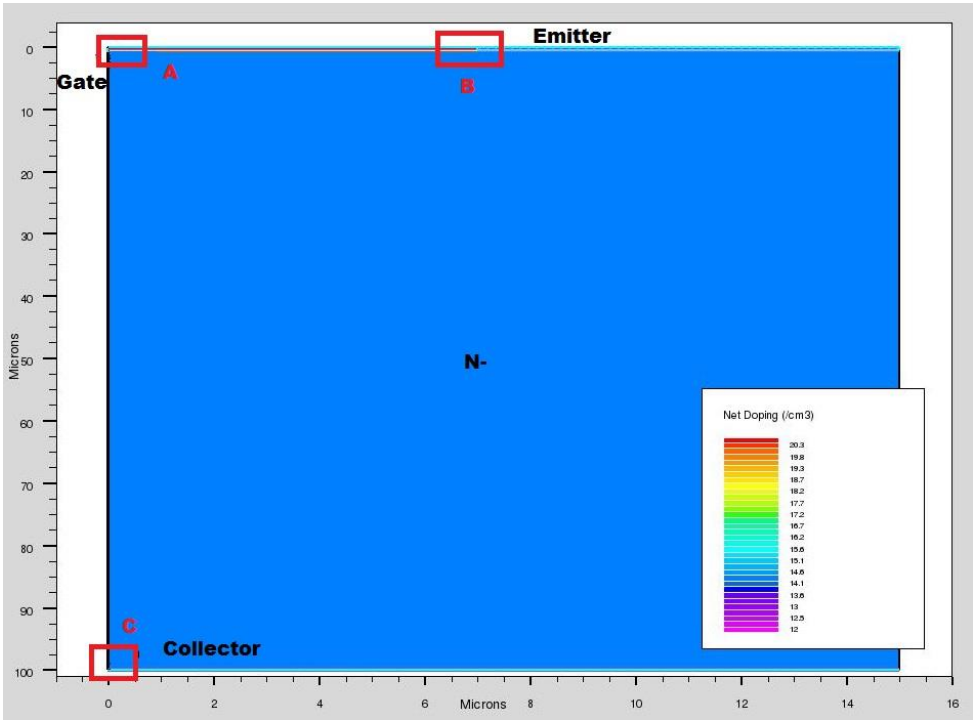


Fig. 4.3 : Ultra-Thin Substrate IGBT structure (to scale)

It is to be noted that in Fig. 4.3 only the N-base region in visible as compared to the other device dimensions it is very large. The zoomed in structures marked with 'A, B & C' in Fig. 4.3 are shown below.

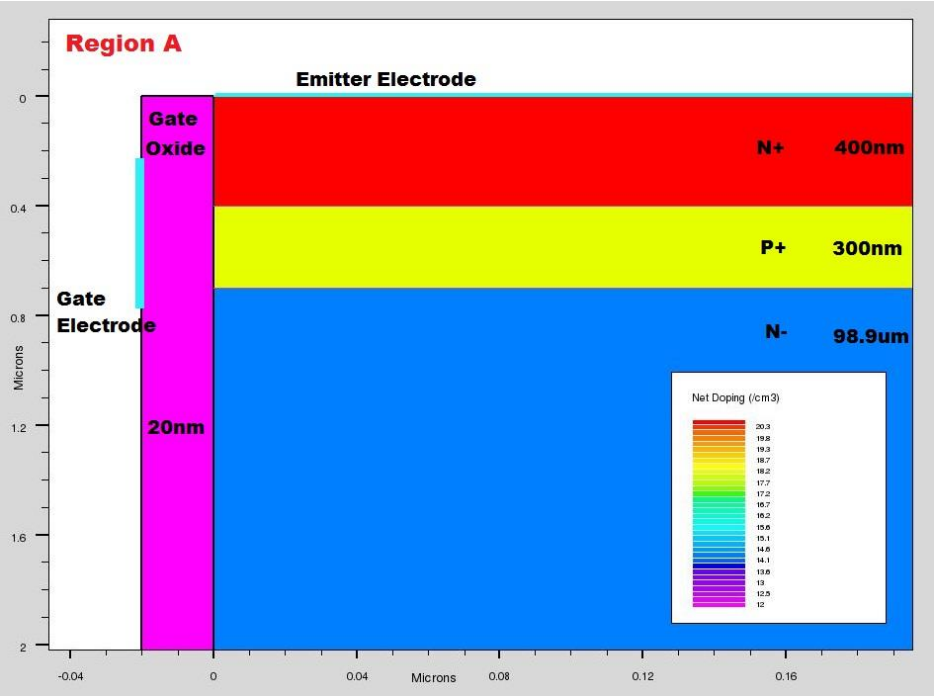


Fig. 4.4 : Region A marked in Fig. 4.3

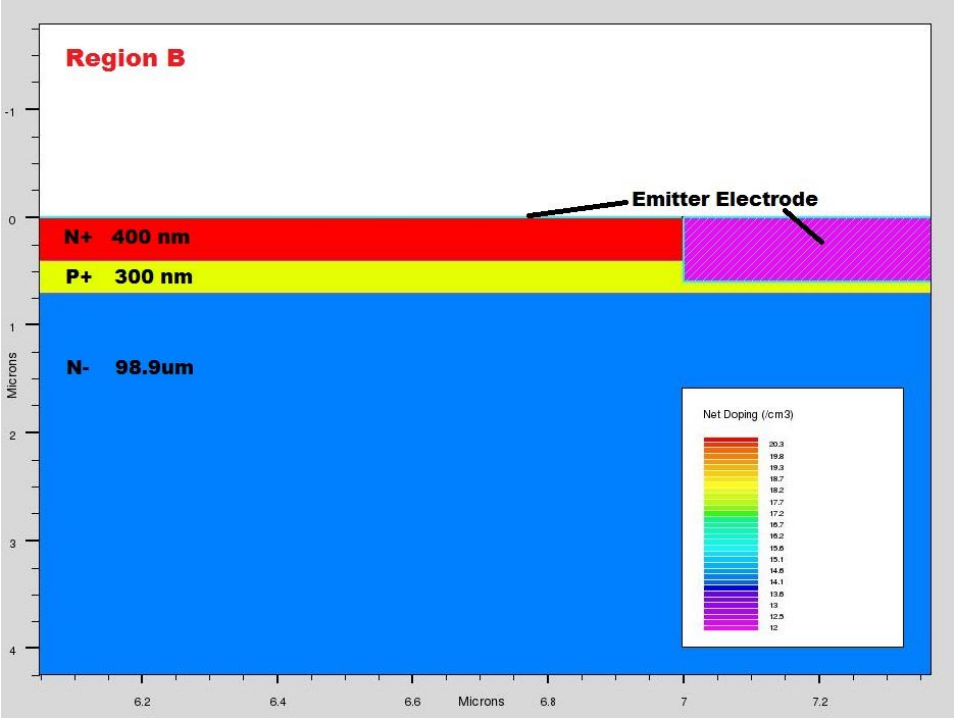


Fig. 4.5 : Region B marked in Fig. 4.3

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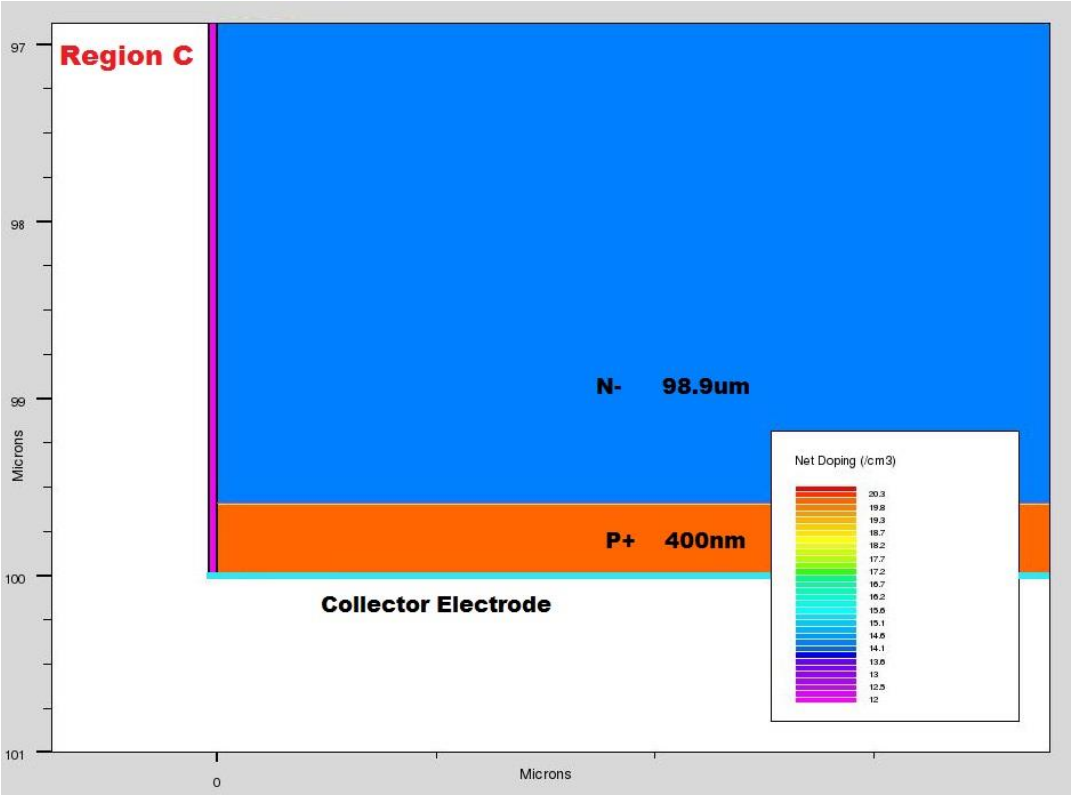

Fig. 4.6 : Region marked C in Fig. 4.3

4.3. Grid Structure for Ultra-Thin Substrate IGBT

The grid structure is probably the most important simulation parameter which determines the outcome of solution. The intersection points in the mesh are where all the transport equations are solved owing to a converging solution.

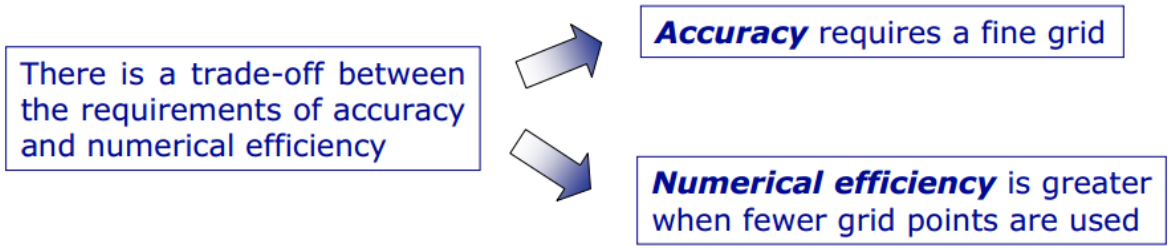

Fig. 4.7 : Trade-off in grid design

The most efficient way to work is to allocate a fine grid only in critical areas and a coarser grid elsewhere. Most critical areas tend to coincide with reverse biased metallurgical junctions. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to construct the device.

The mesh used in our simulation is shown in Fig. 4.8 containing 110,454 simulation points.

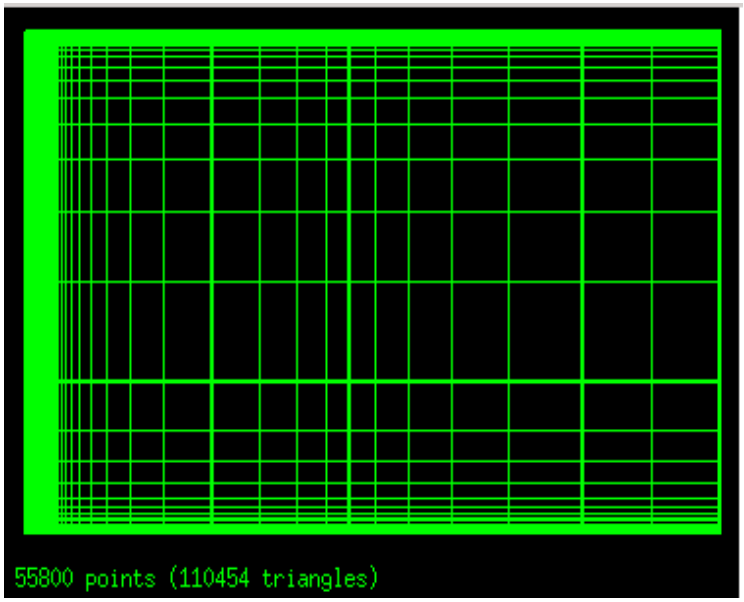

Fig. 4.8 : Grid used for Ultra-Thin Substrate IGBT simulation

4.4. Doping Concentration Profile

The doping concentrations of the MBE layers are an important parameter in fine-tuning the device. It greatly affects the on-resistance and also the breakdown voltage it can withstand. The doping profile of the simulated structure is shown in Fig. 4.9.

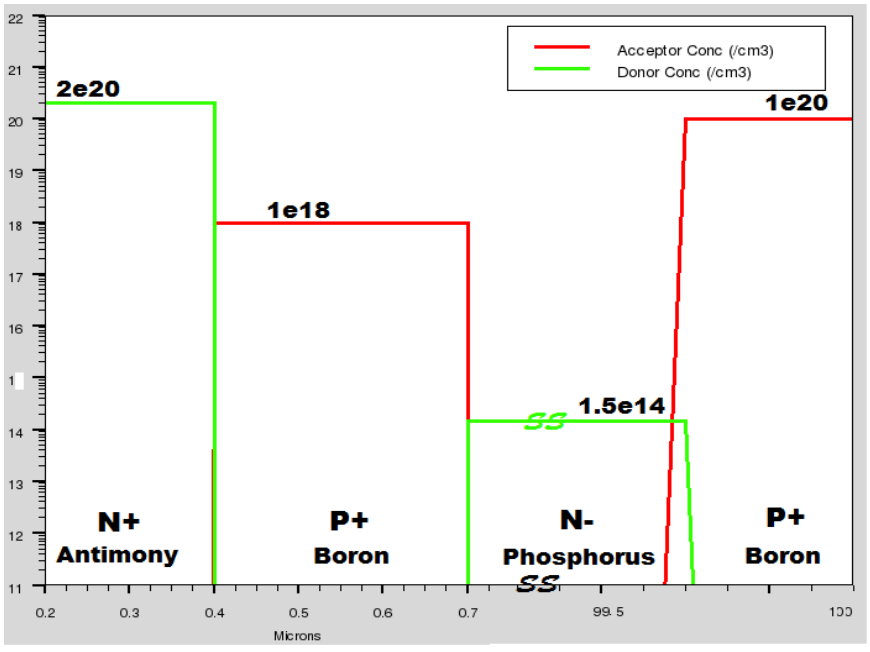

Fig. 4.9 : Doping Profile of Ultra-Thin Substrate IGBT

It is to be noted that due to the epitaxial growth of the layers the doping profile is uniform and abrupt at junctions as opposed to Gaussian profile in diffusion or ion implantation.

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4.5. Band Energy Diagram of Ultra-Thin Substrate IGBT

Atlas allows simulating the conduction and valence band energies of the structure and uses a temperature dependent Universal Energy Bandgap model to calculate the bandgap energies. The model uses the *Varshni's* empirical expression for the bandgap energy E_g,

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad (4.1)$$

Where,

T= Temperature,

$E_g(0), \alpha$ & β = Material Constants (refer to material constants section)

The band energies are shown in Fig. 4.10 on a vertical cutline (x=2microns) of the simulated Ultra-Thin Substrate IGBT.

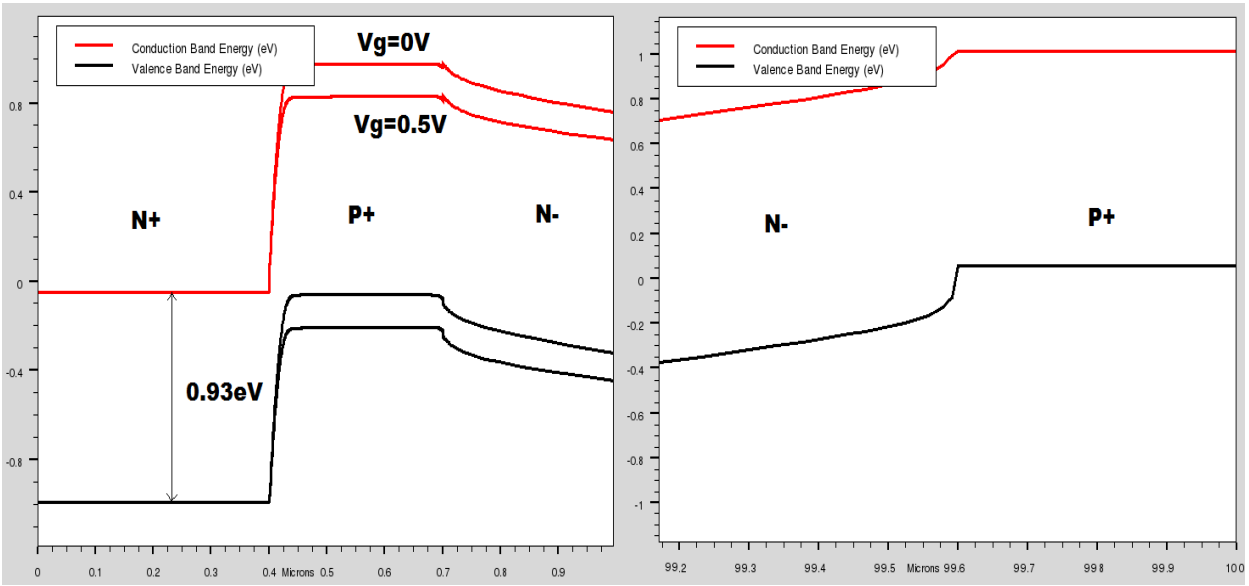

Fig. 4.10 : Band Energy Diagram of Ultra-Thin Substrate IGBT

In Fig. 4.10 (Left) we see the band energy diagram of the MOS-component of the Ultra-Thin Substrate IGBT. The downward shift of the band energy of the channel region with the application of gate voltage is also depicted in the diagram.

4.6. Electron and Hole Mobility in Ultra-Thin Substrate IGBT

The electron and hole mobility values are important parameters which need to be known for various calculations like the effective channel length and resistivity. The model by D. B. M. Klaassen [17] [18] , provides a unified description of majority and minority carrier mobilities. In doing so, it includes the effects of lattice scattering, impurity scattering (with screening from charged carriers), carrier-carrier scattering, and impurity clustering effects at high concentration.

The total mobility can be described by its components using Mathiesen's rule as:

$$\mu_{n0}^{-1} = u_{nL}^{-1} + u_{nDAP}^{-1} \quad (4.2)$$

$$\mu_{p0}^{-1} = u_{pL}^{-1} + u_{pDAP}^{-1} \quad (4.3)$$

Where

μ_{n0} , μ_{p0}	= Total electron or hole mobilities
μ_{nL} , μ_{pL}	=electron and hole mobilities due to lattice scattering
μ_{nDAP} , μ_{pDAP}	= electron and hole mobilities due to donor (D), acceptor (A), screening (P) and carrier-carrier scattering

The Fig. 4.11 shows the simulated electron and hole mobility over a vertical cutline of an Ultra-Thin Substrate IGBT. As expected the mobility of the carriers are higher at low doping concentration while is significantly reduced in highly doped regions.

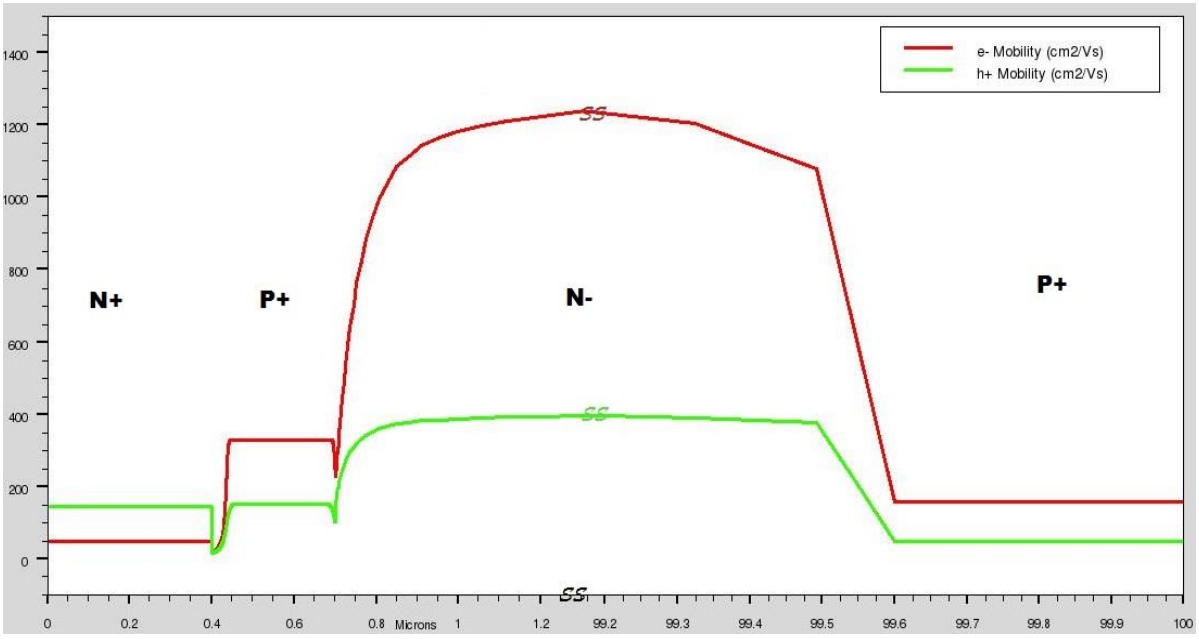

Fig. 4.11 : Electron and Hole Mobility in a Ultra-Thin Substrate IGBT

4.7. Electric Field in an Ultra-Thin Substrate IGBT

The electric field of the Ultra-Thin Substrate IGBT are similar to that of an conventional IGBT where during the forward blocking mode a high electric field is developed at the junction of P^+ channel region and N-base region whereas during reverse blocking mode a high electric field is developed at the junction of N-base region and P^+ collector region.

The graph in Fig. 4.12 depicts the electric field along a vertical cutline of a Ultra-Thin Substrate IGBT in both forward and reverse blocking mode. During forward blocking mode

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i.e. without application of gate voltage, when the collector bias is increased, the applied voltage is blocked by the electric field at the reverse biased junction of P^+ channel region and N-base region. As the collector bias is increased this electric field penetrates deeper in to the N-base region ultimately approaching the collector junction and this marks the onset of forward breakdown. An exactly similar phenomenon occurs in the reverse blocking mode but he electric field develops at the junction between N-base region and P^+ collector region while penetrating towards the P^+ channel region.

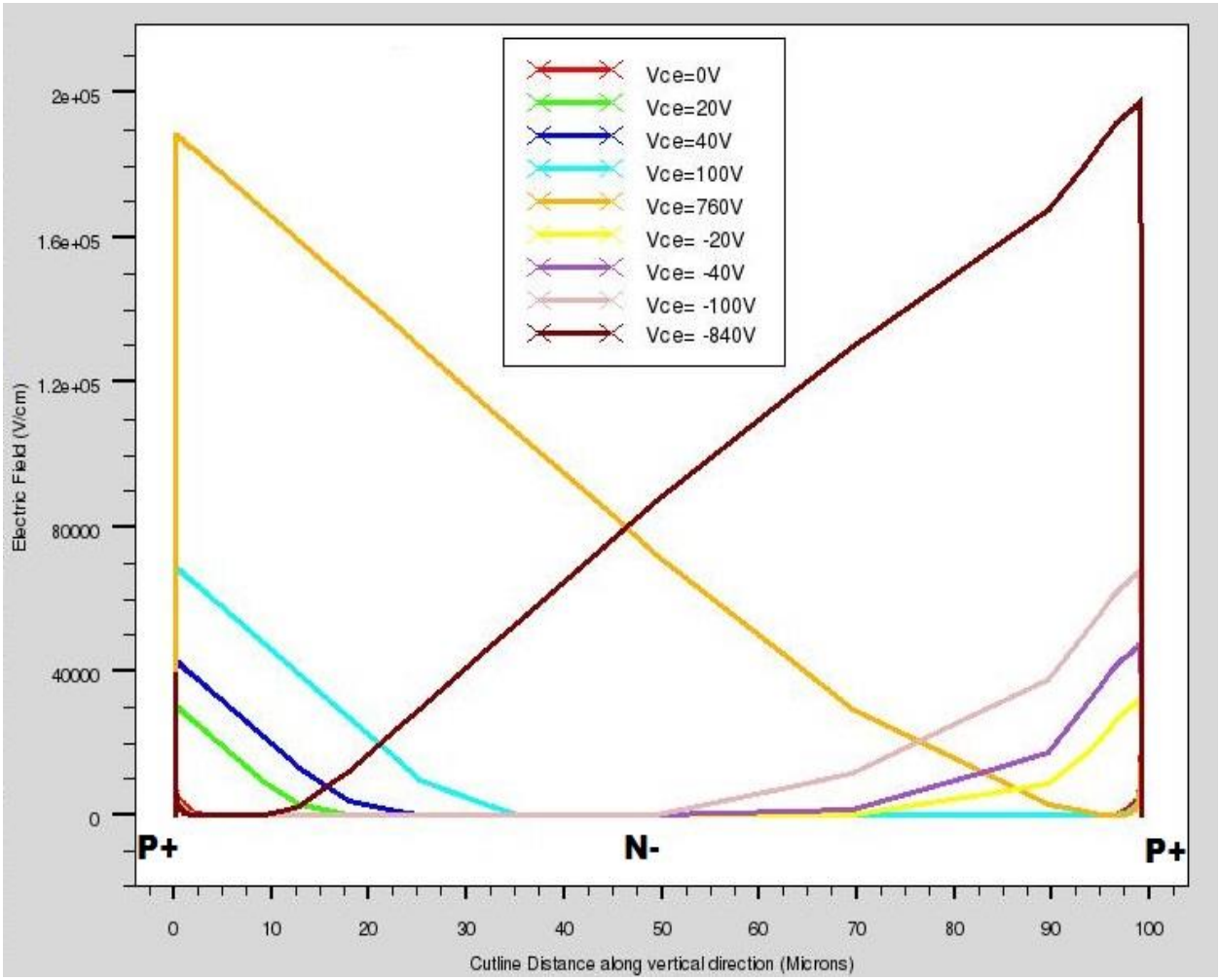

Fig. 4.12 : Electric field of an Ultra-Thin Substrate IGBT along a vertical cutline

4.8. Models for Simulation

In order to simulate the device accurately various models has to be incorporated in the simulation environment. Physical models are specified using the MODELS and IMPACT statements. Parameters for these models appear on many statements including MODELS, IMPACT, MOBILITY and MATERIAL.

The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunnelling [16]. The following tables give a short overview of the models used.

Models	Syntax	Description
Fermi-Dirac	FERMI	Reduced carrier concentrations in heavily doped regions (statistical approach)
Bandgap Narrowing	BGN	Important in heavily doped regions to account for bandgap narrowing. Critical for bipolar gain.

Table 4.1 : Carrier Statistics Models used

Models	Syntax	Description
Concentration Dependent	CONMOB	Lookup table valid at 300K for Si and GaAs only. Uses simple power law temperature dependence.
Concentration and Temperature Dependent	ANALYTIC	Caughey-Thomas formula [16]. Tuned for 77-450K.
Lombardi (CVT) Model	CVT	Complete model including concentration, temperature, parallel and perpendicular electric field and effects. Good for non-planar devices.
Klaassen Model	KLA	Includes concentration, temperature, and electron concentration dependent. Applies separate mobility to majority and minority carriers.
Parallel Electric Field Dependence	FLDMOB	Si models. Required to model any type of velocity saturation effect.
Watt Model	SURFMOB	Transverse field model applied to surface nodes only.

Table 4.2 : Mobility Models used

Models	Syntax	Description
Shockley-Read-Hall	SRH	Uses fixed minority carrier lifetimes.
Concentration Dependent	CONSRH	Uses concentration dependent lifetimes.
Auger	AUGER	Direct transition of three carriers. Important at high current densities.

Table 4.3 : Recombination Models used

Models	Syntax	Description
Silberrherr's Model	SELB	Includes temperature dependent parameters for impact ionization in Si lattice

Table 4.4 : Impact Ionization Models used

Models	Syntax	Description
Band-to-Band (standard)	BBT.STD	For direct transitions. Required with very high fields.
Klaassen Band-to-Band	BBT.KLA	Includes direct and indirect transitions.

Table 4.5 : Tunnelling Models used

4.9. Static Characteristics of Conventional IGBT for Reference

Before the simulation of Ultra-Thin Substrate IGBT we simulate a conventional NPT IGBT to have a characteristic for reference. The conventional IGBT had the doping concentration similar to our simulated IGBT (Section 4.4). However, the doping profile is Gaussian and the channel length is 5µm as shown in Fig. 4.13.

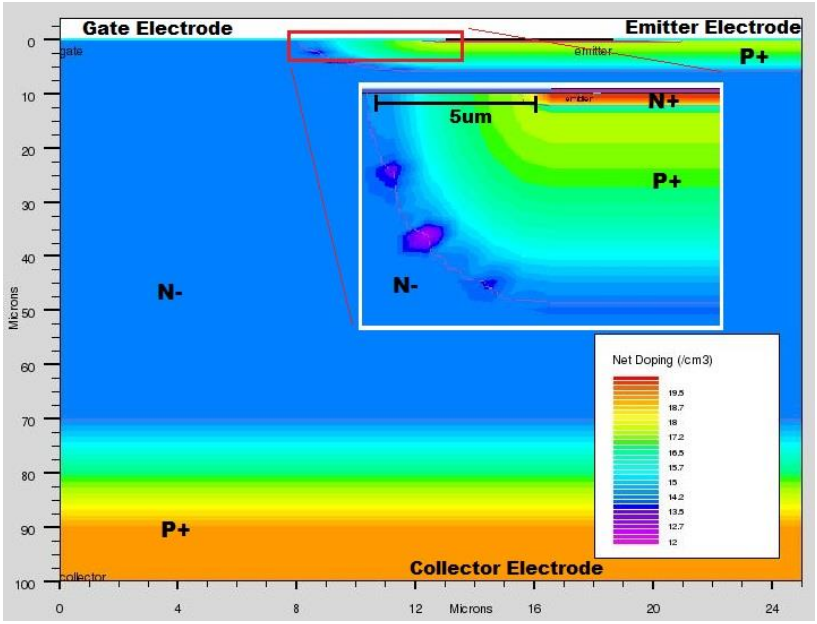

Fig. 4.13 : Simulated Conventional IGBT Structure

The output characteristics and transfer characteristics of the device is shown in Fig. 4.14

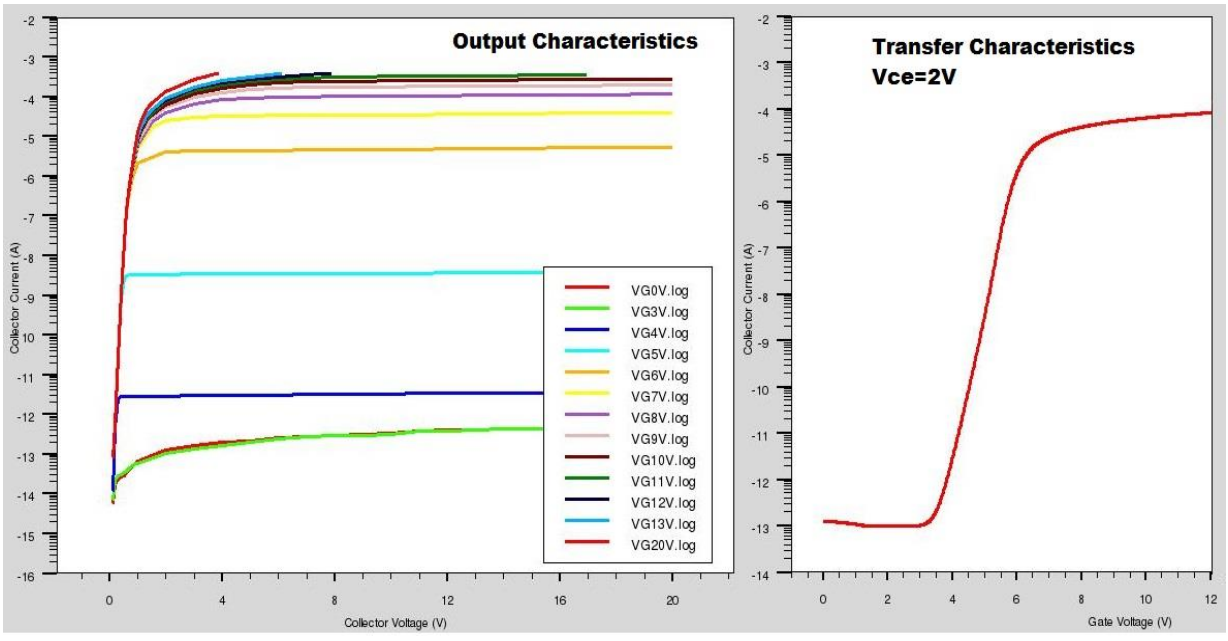

Fig. 4.14 : Static Characteristics of Conventional IGBT

4.10. Static Characteristics of Ultra-Thin Substrate Power MOSFET

To understand the MOS component of the Ultra-Thin Substrate IGBT we have simulated an Ultra-Thin Substrate Power MOSFET. It has exactly the same doping and structural features of the Ultra-Thin Substrate IGBT as shown in Fig. 4.3 to Fig. 4.6 with an exception that the bottom collector layer of the device (P^+ layer in Fig. 4.6) is a N^+ layer instead of a P^+ layer.

The static characteristic of the simulated device is shown in Fig. 4.15.

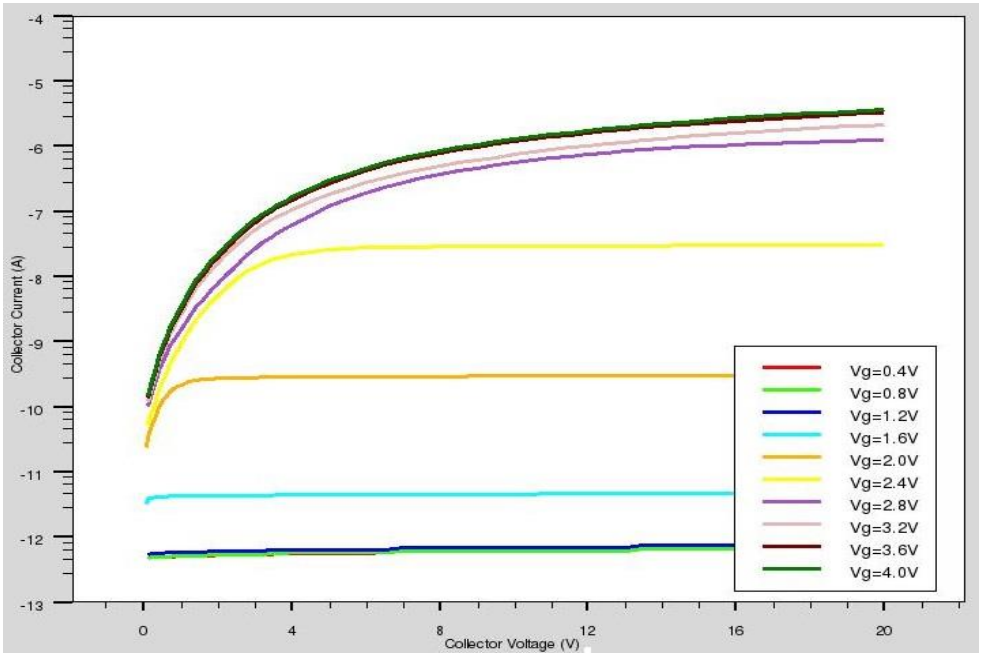

Fig. 4.15 : Output Characteristics of Ultra-Thin Substrate Power MOSFET (Log scale)

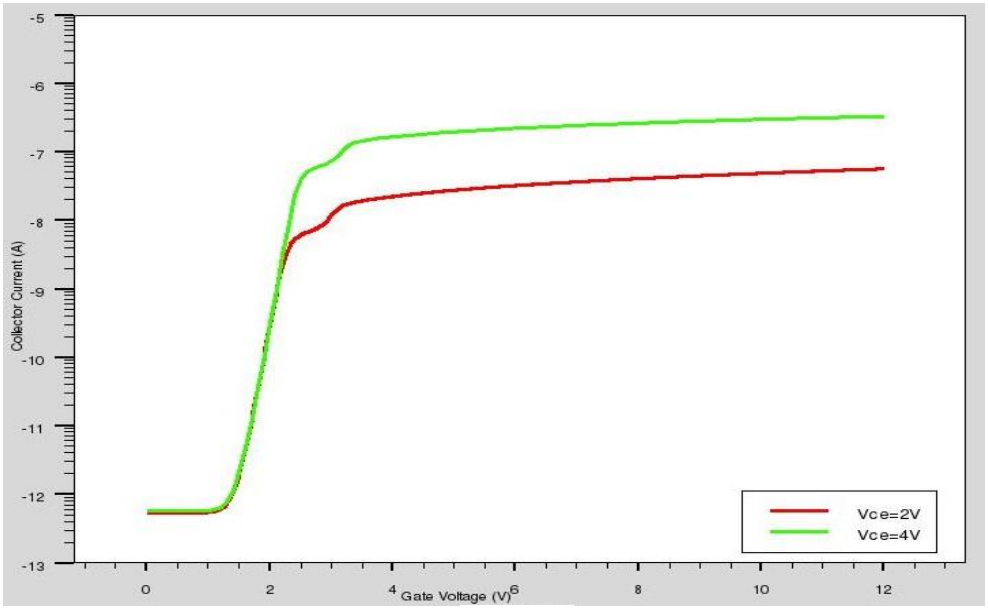

Fig. 4.16 : Transfer Characteristics of Ultra-Thin Substrate Power MOSFET (Log scale)

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It can be observed that maximum current level in Power MOSFETs is lower than that of IGBT as discussed in the theory, earlier. Thus due to the carrier injection of the bottom collector layer the current gain in the IGBT bipolar component is high which is absent in Power MOSFETs. Also the shift in the threshold voltage of the IGBT is also not seen in Power MOSFET due to the absence of the bottom p-n junction.

4.11. Static Characteristics of Ultra-Thin Substrate IGBT

The following section deals with the static characteristics of the designed Ultra-Thin Substrate IGBT and gives us a prediction of how the fabricated device should perform.

The Output Characteristics of the device is shown in Fig. 4.17 and Fig. 4.18 while the Transfer characteristic is depicted in Fig. 4.19.

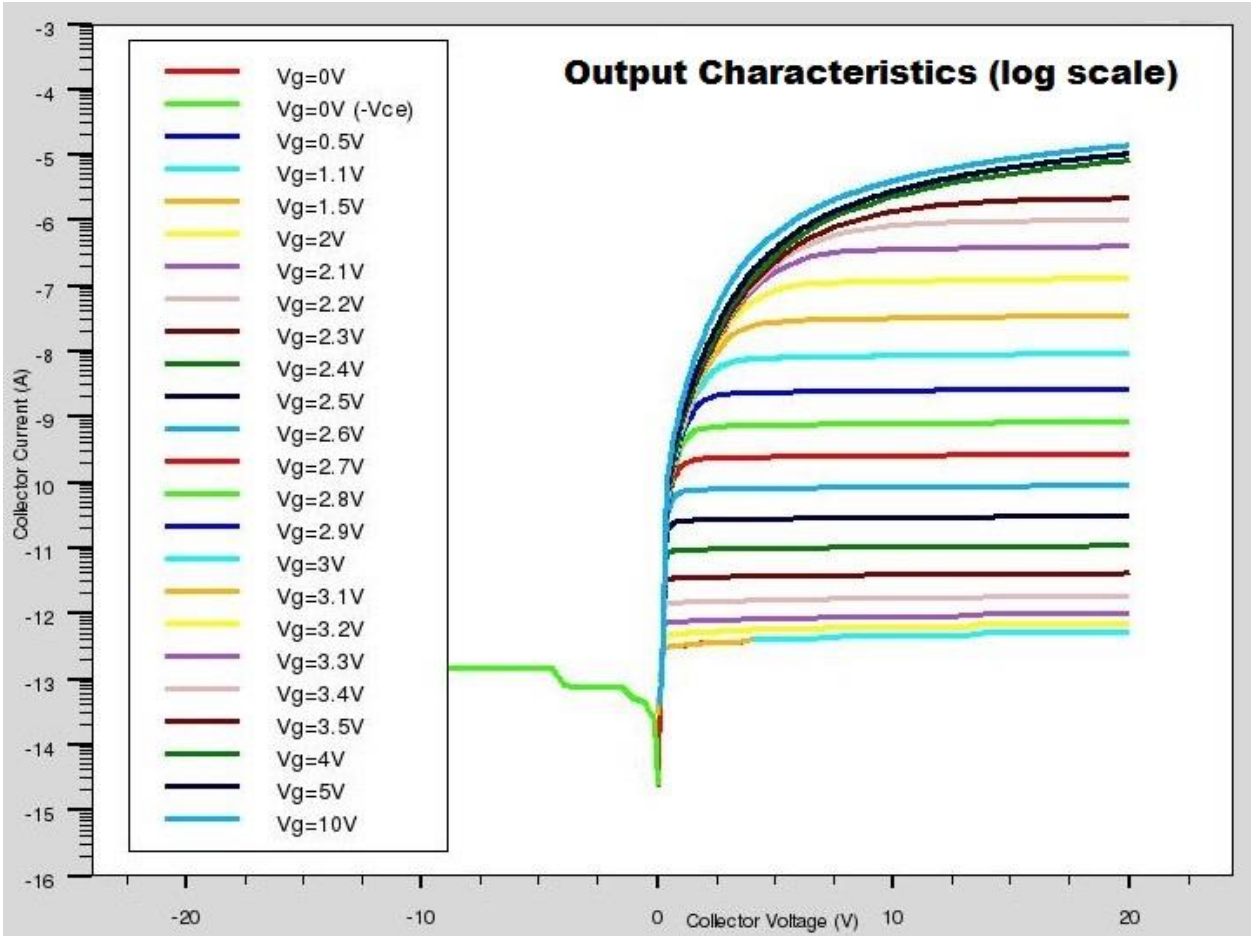

Fig. 4.17 : Output Characteristics of Ultra-Thin Substrate IGBT (log scale)

It can be observed that that the maximum current level is of the order 10^{-5} A. The area of the device is 15µm so the maximum current density is of the order 66.66 A/cm^2. It can also be observed that the gate response is between 2 – 4V. The I_{ON} to I_{OFF} ratio is in the order of 10^7. From Fig. 4.19 the threshold voltage of the IGBT is observed to be around 3V.

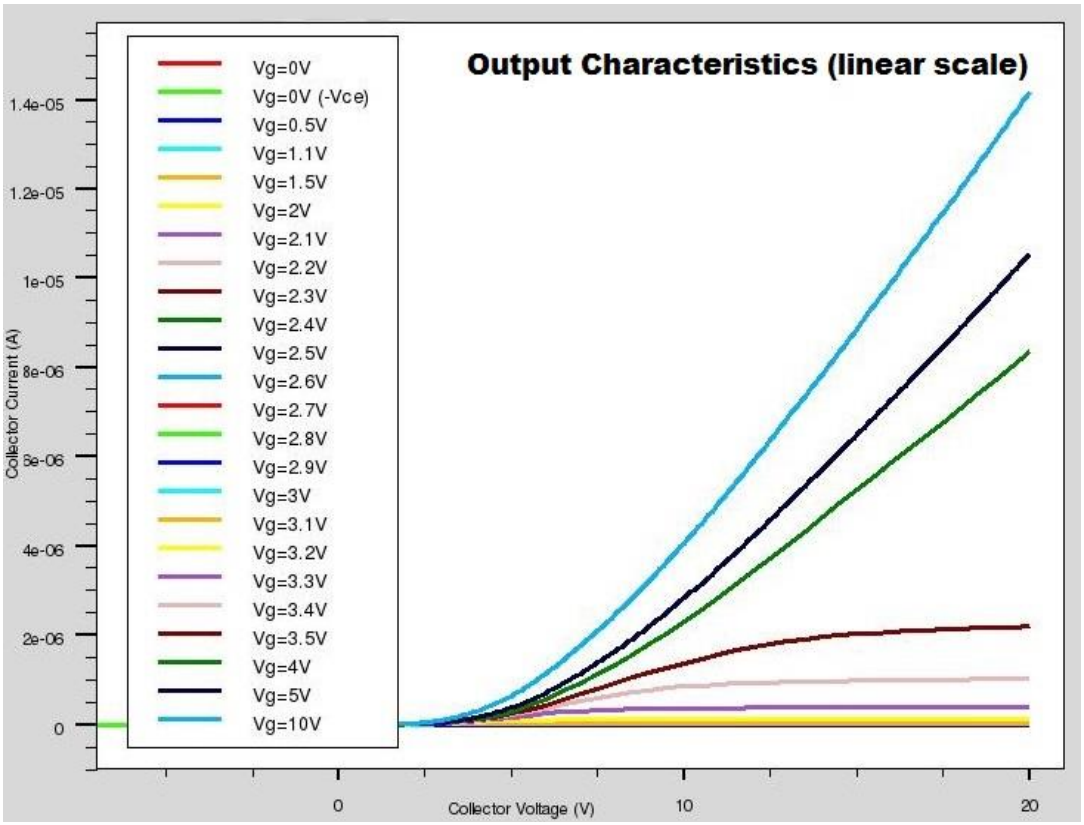

Fig. 4.18 : Output Characteristics of Ultra-Thin Substrate IGBT (linear scale)

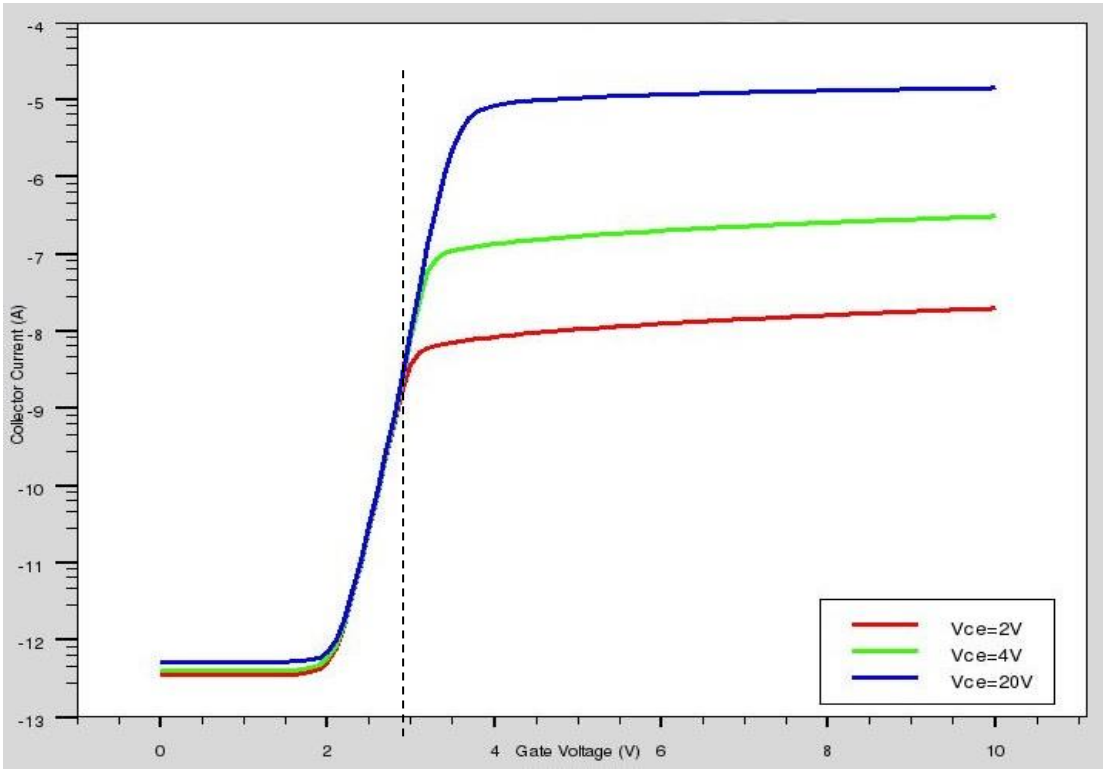

Fig. 4.19 : Transfer Characteristics of Ultra-Thin Substrate IGBT (log scale)

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4.12. Adding Non-Ideal Parameters to the Simulation

The simulation done so far are with ideal device parameters, but during fabrication a lot of non-idealities are added due to constraints of the machines used in fabrication.

Two of those most important parameters are the contact resistance of the electrodes and the fixed charge of the Si-insulator interface. These parameters were added to the simulation to get a more accurate simulation of the fabricated device. With the machine calibration over the years the contact resistance of the electrodes is found to be approximately 1 x 10^{-5} ohm cm^{-2} and the fixed charge present in the gate oxide deposited by PECVD was statistically found to be 8 x $10^{11} cm^{-2}$. The resultant simulation is shown in Fig. 4.20.

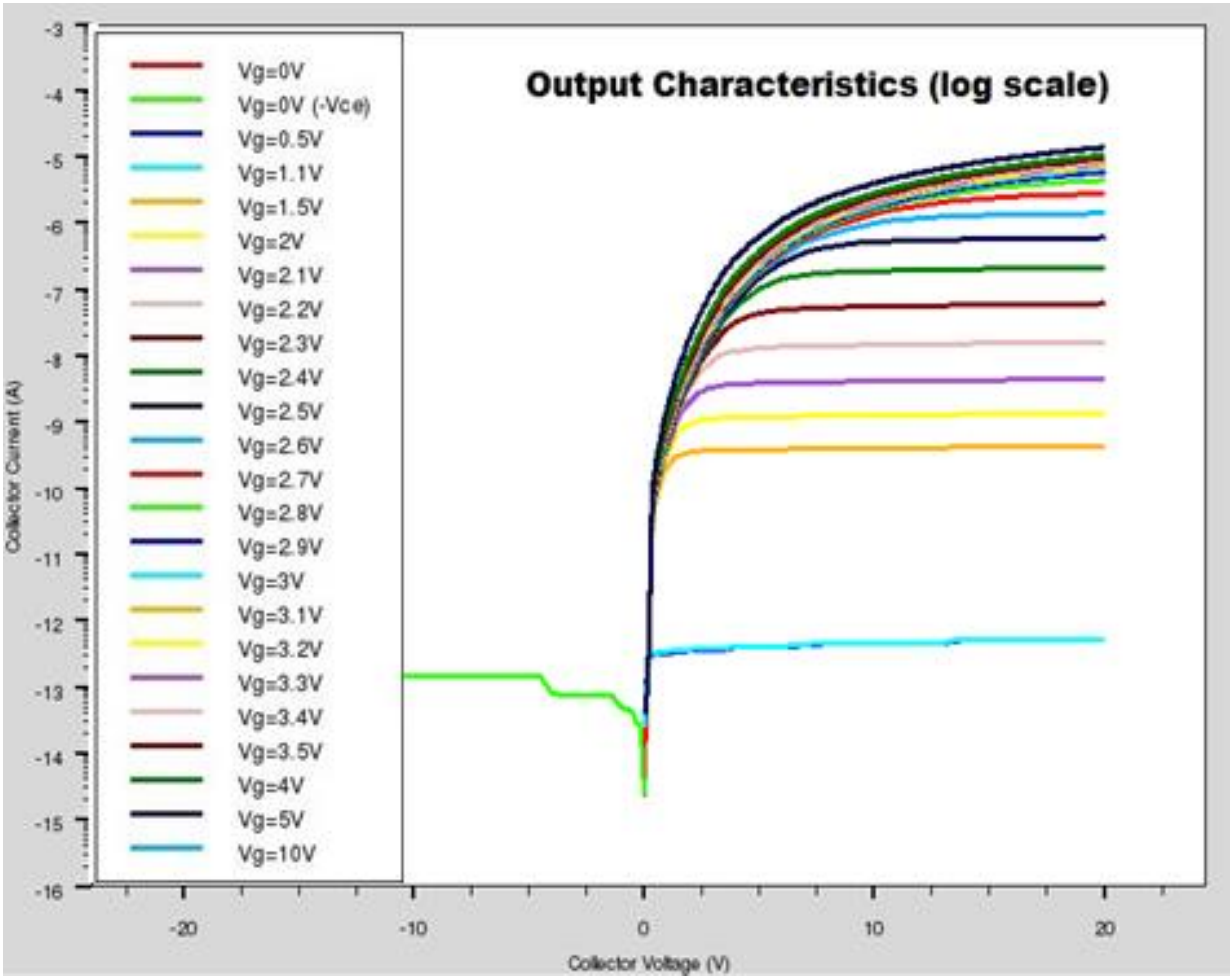

Fig. 4.20 : Output characteristics with fabrication specific parameters

It can be observed that the maximum current limit does not change but the off current of the device increases by a significant amount with the addition of the fixed charge in the Si-Insulator interface and the addition of contact resistance of the electrodes in the device.

4.13. Breakdown Simulation of Ultra-Thin Substrate IGBT

A predictive breakdown simulation of the Ultra-Thin Substrate IGBT is done to get an idea about the expected breakdown of the device in both the forward and reversed biased region.

The simulation result is represented in Fig. 4.21

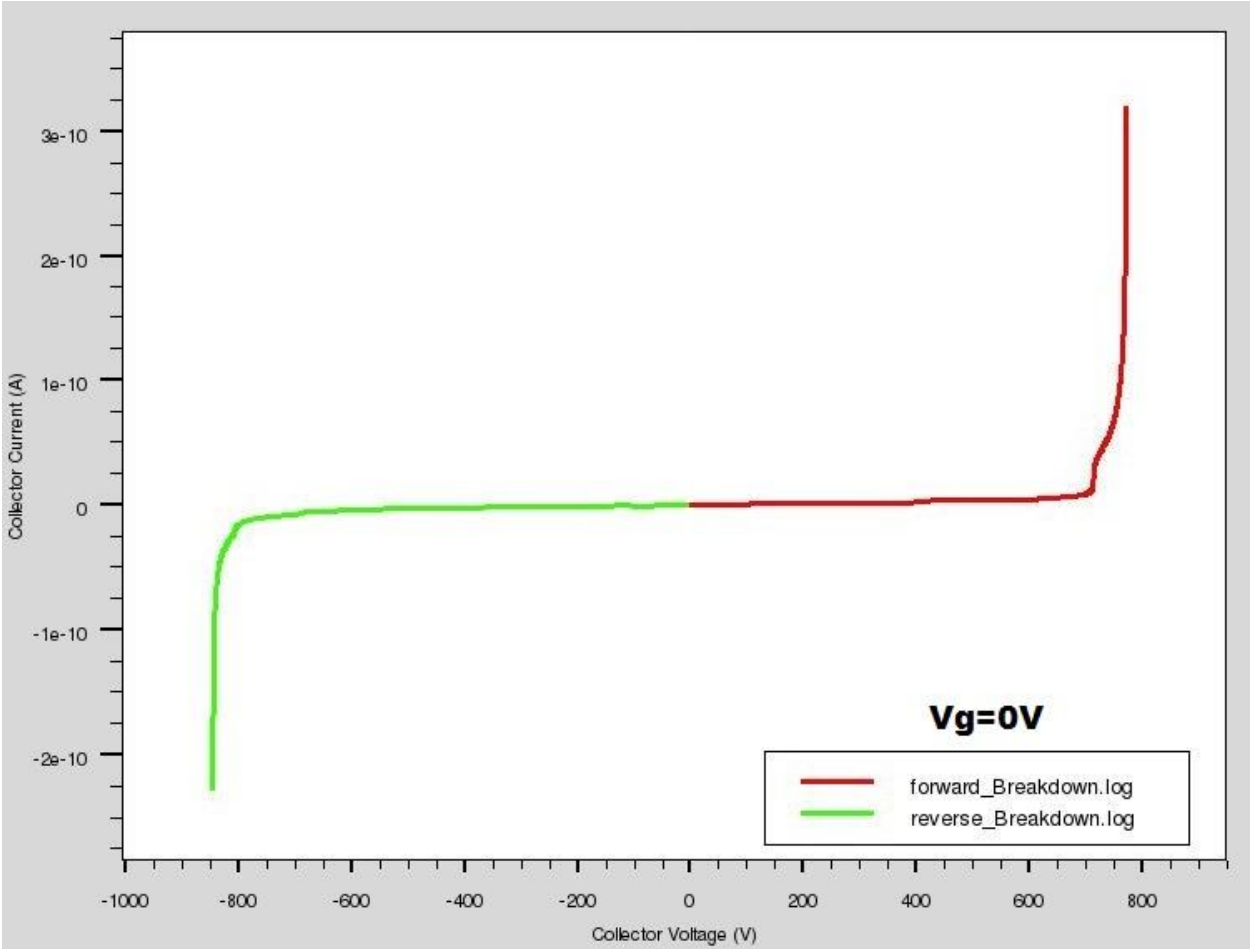

Fig. 4.21 : Breakdown Voltage Simulation

As per the simulations,

- Forward Breakdown Voltage = 771 V
- Reverse Breakdown Voltage = 846 V

5. Device Fabrication

5.1. Substitute for Ultra-Thin Wafer Technology

As discussed in section 1.2 the Ultra-Thin wafer technology that the industry is using today to reduce the power losses in the IGBT comes with a complexity. These Ultra-Thin wafers are of the order of 100µm thick and are impossible to handle manually. They bend even under gravity (Fig. 5.1).

Fig. 5.1 : Ultra-Thin Wafer used by Infineon [19]

These Ultra-Thin wafers require a dedicated robotic assembly chain to handle them throughout the process chain. The huge cost factor involved in having this setup is feasible for industry but for academic research one cannot afford this. And as a consequence, if we cannot manufacture IGBT which are equivalent to the ones, that the industries are producing, how are we going to incorporate improvements into the device. The scope of academic research is highly hampered.

One of the primary objectives of this research was to find an alternative solution for this. After careful consideration and experience in device fabrication we have at IHT we came up with a solution to substitute the Ultra-Thin wafers with **Silicon Membranes** of equivalent thickness.

At IHT we had a few experiences with fabrication of Si membranes giving good results but these were related to its application in sensor design. We aimed at using these membranes as the substrate for building our IGBT on making it the first time to use this technique in fabrication of power semiconductor devices.

5.2. Si Membrane Fabrication

5.2.1. Etching Methods

There are several parameters that are used to classify etching methods. Based on the physical state of the etchants, it is often divided into two classes, wet etching and dry etching. Wet etchants in aqueous solution offer the advantage of low-cost batch fabrication (25 to 50 100-mm-diameter wafers can be etched simultaneously) [20]. Dry etching involves the use of reactant gases, usually in low-pressure plasma, but non-plasma gas-phase etching is also used to a small degree. The equipment for dry etching is specialized and requires the plumbing of ultra-clean pipes to bring high purity reactant gases into the vacuum chamber [21].

Another parameter that is used to classify etching method is the directional selectivity property of the etchant. Isotropic etchants etch uniformly in all directions, resulting in rounded cross-sectional features (Fig. 5.2). By contrast, anisotropic etchants etch in some directions preferentially over others, resulting in trenches or cavities delineated by flat and well defined surfaces, which need not be perpendicular to the surface of the wafer [21].

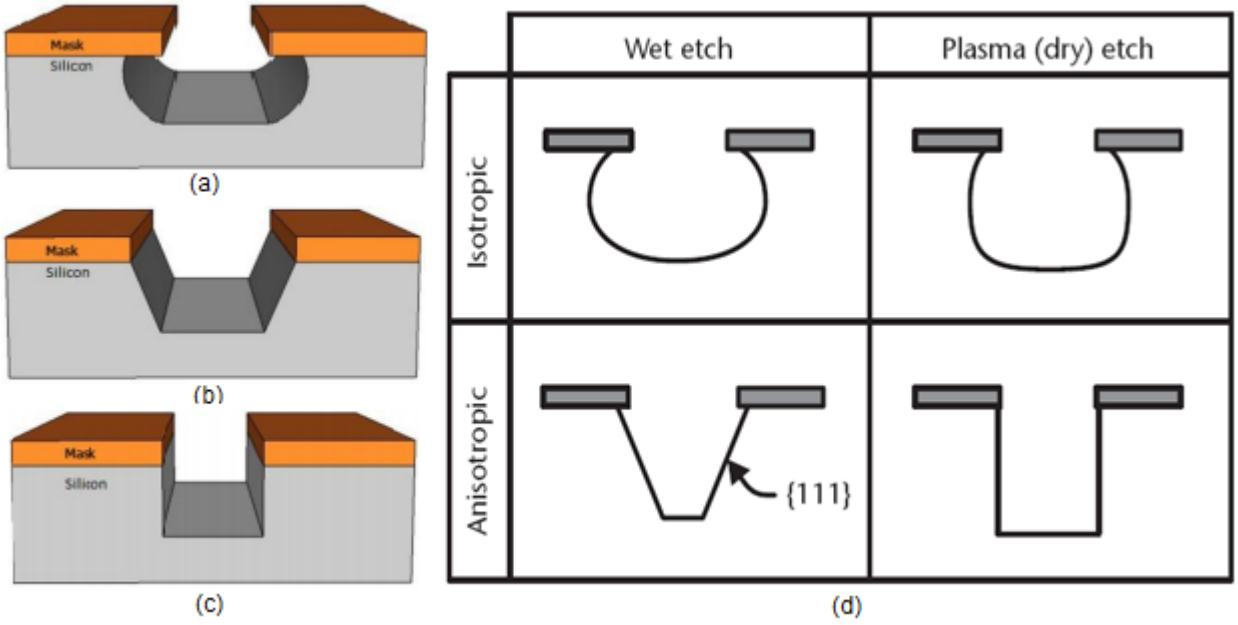

Fig. 5.2 : (a) Anisotropic (b) Partially Isotropic (c) Isotropic Etching **[22]** (d) Etching Classification Table **[20]**

For the purpose of Si membrane etching we choose the method of partially isotropic etching (Fig. 5.2 (b)). This allows the formation of smooth membranes with sharp edges as contrast to rounded edges in isotropic etching. Since the thickness of silicon to be etched to have a Ultra-Thin membrane we select wet etching which is faster and doesn't require complex instruments. The general chemical reaction during the etching is shown below

$$\text{solid} + \text{liquid etchant} \rightarrow \text{soluble products} + \text{gas}$$

$$Si\ (s) + 2OH^- + 2H_2O \rightarrow Si(OH)_2(O^-)_2\ (aq) + 2H_2\ (g)$$

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Hydrogen gas is a by-product of the reaction. The hydroxide ion comes from the anisotropic wet etchants. Potassium hydroxide (KOH), ethylene-di-amine pyro-catechol (EDP) and tetra methyl ammonium hydroxide (TMAH) are the common anisotropic wet etchants for silicon. Alkali metal hydroxide etchants such as potassium hydroxide (KOH) water solution have high silicon etching rates and anisotropic etching capability. Unfortunately, KOH is not CMOS compatible because it contaminates the Si-gate oxides interface with mobile alkali metal ions. EDP on the other hand, with a small amount of Pyrazine, is a commonly used etchant for the anisotropic etching of single crystal silicon and is extensively applied to silicon micromachining. However, EDP is no longer desirable because it is hazardous and contains long-term toxic effects. When it comes into contact with water solution during cleaning, visible amber develops. Such mist creates a serious inhalation hazard in addition to that caused by the evaporation of the ethylene-di-amine from the solution. The quaternary ammonium hydroxide group fulfils the requirements of CMOS-compatibility. In this group, tetra-methyl-ammonium hydroxide ($(CH_3)_4NOH$) is the preferred etchant because it can achieve a fairly high silicon etching rate. However, reproducibility of etching results is still a problem. TMAH satisfies all the requirements: ease of handling, non-toxicity and CMOS-compatibility and hence is chosen for fabrication of our Si membranes [21].

Etching using anisotropic aqueous solution of TMAH results in three-dimensional faceted structures formed by intersecting {111} planes with other crystallographic planes. The easiest structures to visualize are V-shaped cavities etched in {100}-oriented wafers. The etch front begins at the opening in the mask and proceeds in the {100} direction, which is the vertical direction in {100}-oriented substrates, creating a cavity with a flat bottom and slanted sides. The sides are {111} planes making a 54.7º angle with respect to the horizontal {100} surface. If left in the etchant long enough, the etching ultimately self-limits on four equivalent but intersecting {111} planes, forming an inverted pyramid or V-shaped trench. Of course, this occurs only if the wafer is thicker than the projected etch depth. Timed etching from one side of the wafer is frequently used to form cavities or thin membranes [20].

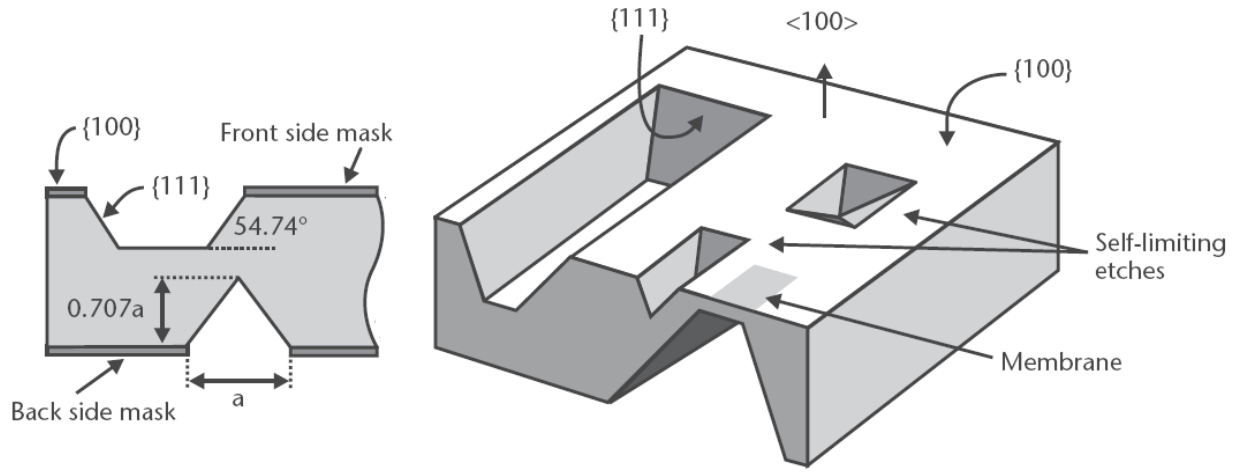

Fig. 5.3 : Structures with TMAH etching **[20]**

5.2.2. Process Steps

The fabrication of Ultra-Thin membranes (Fig. 5.4) starts with an industrial grade Si wafer which is about 550µm thick. First it is cleaned with Piranha cleaning to remove any organic residue on the wafer, followed by RCA1 and RCA2 cleaning. Then a 1 µm thick oxide layer is deposited on both front side and backside of the wafer by PECVD (Fig. 5.4, step 1). The back side oxide is to be structured to make the opening for Si etch in TMAH however the front side oxide serves just as a protective layer to prevent Si etching from the front side

After the oxide deposition a photoresist is used to coat the wafer from both front and back side (Fig. 5.4, step 2). An image reversal photoresist AZ5214 is used, but not for the image reversal property but because it gives a thick layer of photoresist. The spinning of the photoresist is done at 1500 rpm for 30 seconds. This is followed by a flood exposure through an aluminium mask, with four square windows, and then the wafer is developed (Fig. 5.4, step 3). The majority of the oxide from the exposed region is then etched by reactive ion etching and the rest is removed by BHF. Then the remaining photoresist is removed by plasma (Fig. 5.4, step 4).

This structured wafer is put into a TMAH bath just after a quick HF dip to remove any native oxide formed. Just a few nanometres thick native oxide, is sufficient to protect the silicon surface from etching. The TMAH etches the exposed Si surface till the required thickness is reached and is then removed from the bath (Fig. 5.4, step 5).

This wafer is again cleaned by piranha cleaning followed by RCA1 and RCA2 and then the entire oxide is removed by BHF. The resultant wafer consists of Ultra-Thin Si membranes (Fig. 5.4, step 6).

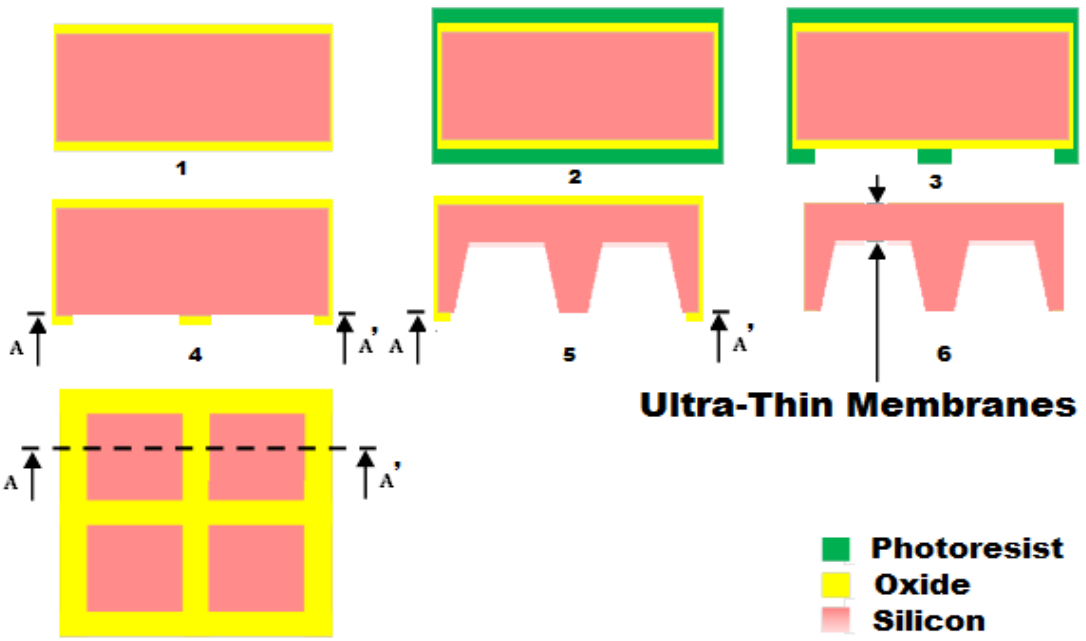

Fig. 5.4 : Process Steps in Ultra-Thin Membrane Fabrication

5.2.3. Etch Setup and Parameters

Although the theory of anisotropic etching with TMAH solution is simple, the actual implementation of the etching technology is quite a challenge. There are numerous parameters that have to be taken into consideration simultaneously to get good results but even after these considerations, reproducibility is a serious concern and it only comes with experience rather than theoretical data.

For our Si membrane a special setup was made to control all the etching parameters as depicted in Fig. 5.5 (a)

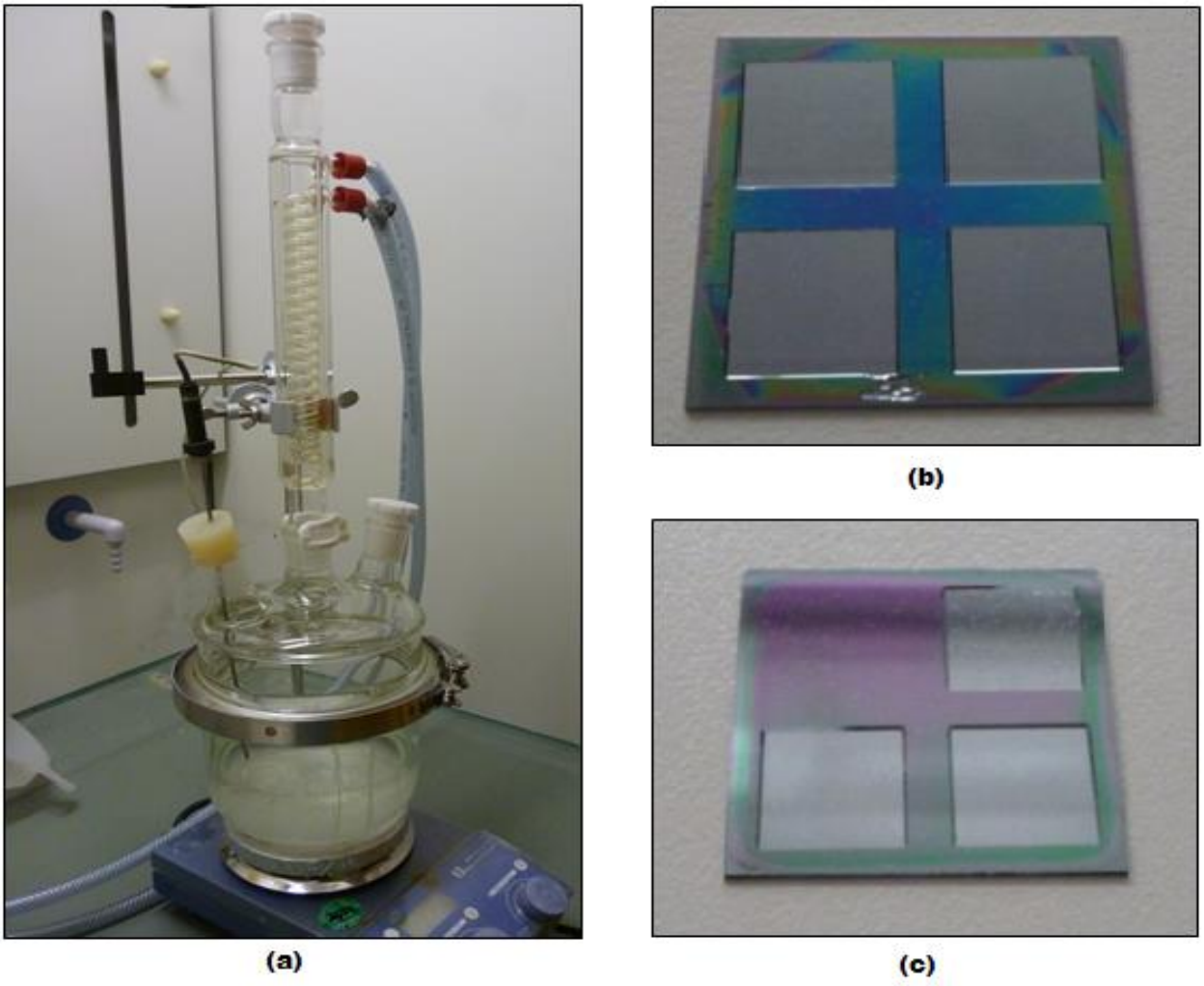

Fig. 5.5 : (a) TMAH Etch Setup at IHT, (b) 4 windows Si-Membrane, (c) 3 windows Si-Membrane

The setup consists of a hard glass container along with a sealed lid having three openings. This is placed over an automated heater with magnetic stirrer with which the temperature and the stirring are controlled during etching. Out of the three openings in the setup one is used for the temperature sensor and one for the release of hydrogen gas. The later opening is fitted with a tap water condenser to prevent the escape of TMAH vapours. This was an

addition in the later stage of our etching process when we faced with the problem that the concentration of the TMAH solution changed drastically during etching due to evaporation resulting in erratic etch rates. The third opening is unused and plugged.

During initial etching, we fabricated 4 windows on a single 4 inch wafer (Fig. 5.5 (b)) but we soon realised that it was difficult to handle it as any contact with the tweezers while holding the wafer breaks the membrane. To avoid this problem we decreased the number of windows to 3 (Fig. 5.5 (c)) so that it allows space for holding the wafer with tweezers without breaking the membranes.

After numerous experiments [21] we came up with the optimum parameters of TMAH etching as described in Table 5.1.

Parameters	Value
TMAH Concentration	25 % by weight
Etch Temperature	75° C
Stirring Speed	500 rpm
Approximate Etch Rate	17 µm / hr.
No. of 35 mm x 35 mm wafer etched / 1.3 litre TMAH	4

Table 5.1 : Optimized TMAH Etch Parameters

5.2.4. Surface Quality of the Ultra-Thin Si Membranes

After the fabrication of Ultra-Thin Si membranes we had to inspect the smoothness of the membrane surface to determine if they were of good quality and comparable to standard industry grade thin wafers. It was also important to determine the surface roughness as the following steps involved depositing layer of Si by MBE on the membranes to fabricate an IGBT. Automatically smooth surface is a critical parameter to determine the quality of the MBE deposited layer and the junctions.

In the first batch of etching we took an industrial wafer and etched the membranes from the top side and found that the surface roughness was comparable to an industrial thin wafer surface. But as required for IGBT fabrication when we etched from the back side we found that the results were not good. The surface was very rough and couldn't be used for MBE further.

We investigated the problem and came to the conclusion that normal industrial wafers are polished only on the top surface, while the bottom surface is rough and unpolished.

We conducted a Chemical Mechanical Polishing (CMP) of the bottom surface of the wafer to make it as smooth as possible. CMP is a process to remove excessive topographic variations and to achieve global and local planarization in microelectronic device fabrication [21]. It uses slurry to polish the wafer surface, which is typically Silica (SiO_2) or alumina (Al_2O_3).

When we etched the membranes from these polished back side we ended up with good results (Fig. 5.6) and the average surface roughness comparable to industrial thin wafers.

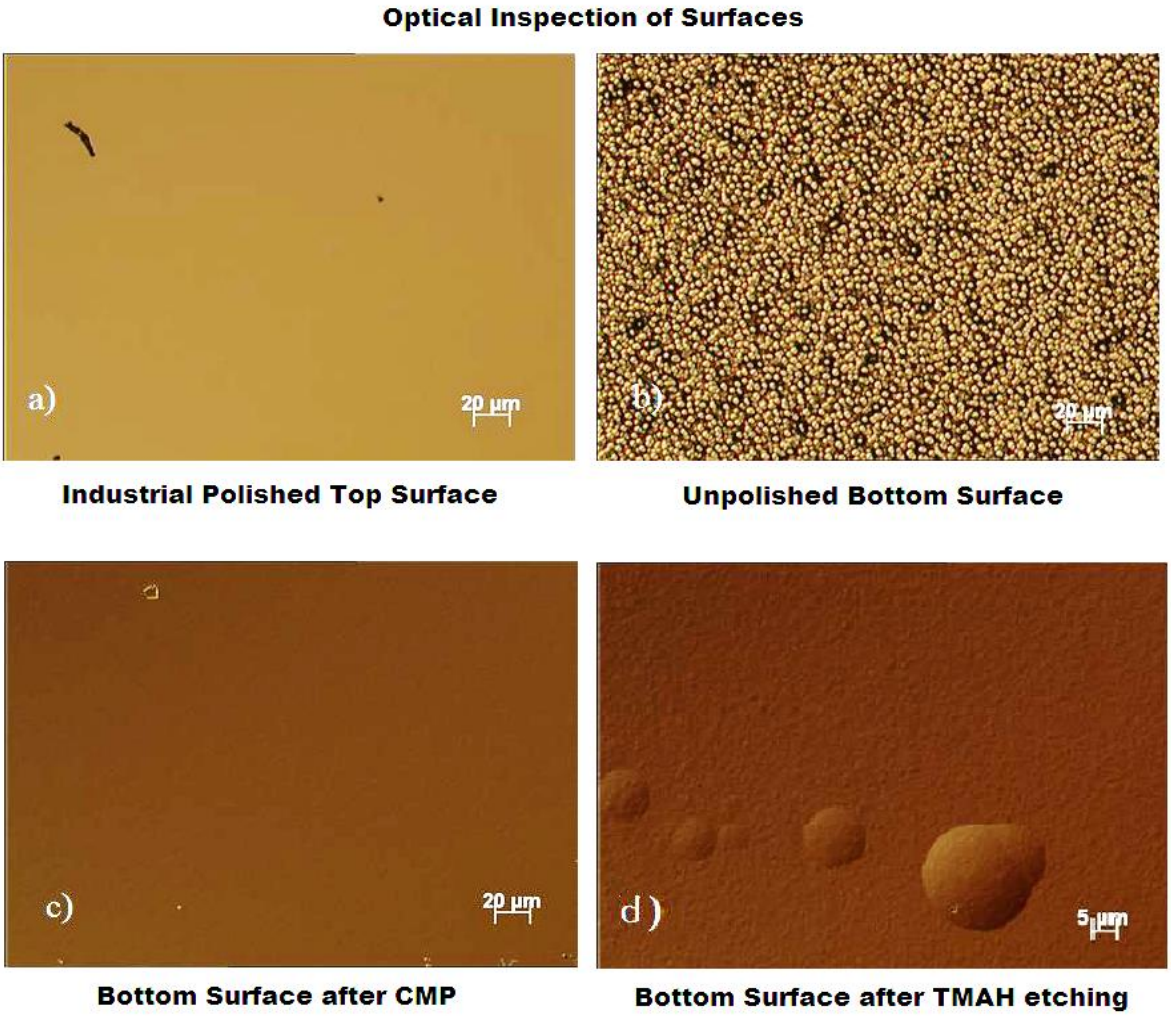

Fig. 5.6 : Optical Inspection of Surface Roughness **[21]**

With close inspection of the etched membranes we saw that there were some round deformities on the membranes as shown in Fig. 5.6 (d). These depressions in the membranes are caused by the TMAH etch. We have two hypotheses for the formation of such deformities; first, these may be caused by the hydrogen bubbles sticking to the surface of Si which accelerates the etching rate causing a local depression. Second, it might be because of defects in the crystal itself. To our experience we think it is the former reason of hydrogen bubbles and a significant part can be reduced by increasing the stirring speed and proper placement of the wafer and also the design of the wafer holder. A more appropriate solution would be to add anti-surfactant to the etching process but they have poisonous properties which prevented us from using them.

The depressions dimensions were of the order of few µm, randomly scattered and covered less than 5% of the total area of the membrane. This led us to accept it as a good quality

surface since we are going to fabricate numerous IGBT on a single membrane its quiet likely majority of the devices would be on the smooth section of the membrane. An AFM was conducted on a 10µm X 10µm smooth patch to confirm the surface roughness (Fig. 5.7) which gave us an average roughness of 1.69 nm which is quiet acceptable to industrial standards.

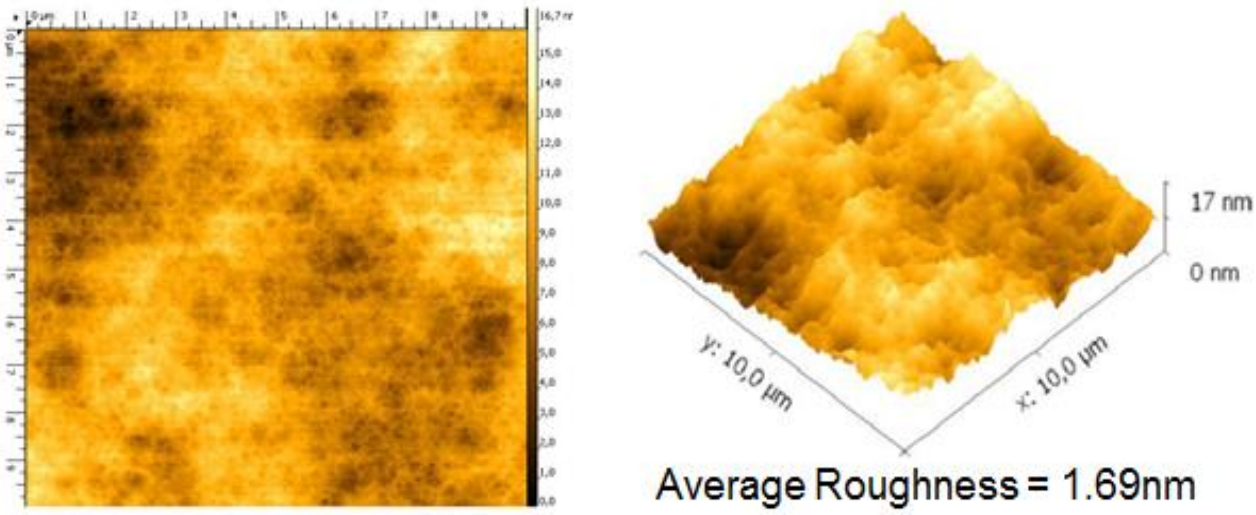

Fig. 5.7 : AFM of a 10µm X 10µm smooth patch on the Ultra-Thin Si Membrane **[21]**

5.3. Mask Set for IGBT Fabrication

The next step in the process of fabricating the device was to choose or design a suitable mask set as it was the first time that an IGBT was to be fabricated in our laboratory at IHT. We chose the 'Uni-BW' mask set.

This mask set is used in IHT for the fabrication of PDBFETs and was developed by Peng Fei-Wang at the Department of Electronics at the Technical University of Munich in collaboration with the University of the Federal Armed Forces Munich. The mask set includes six different layers and is designed for four-inch diameter wafer. The official name of the mask set is *'Vertical Nanomos 2003'*, however at IHT, the name Uni-BW mask set has prevailed.

But this mask set had a shortcoming due to the basic design difference between MOSFETs and IGBT. The Emitter and channel region shorting is absent in MOSFET which is necessary for proper functioning of IGBTs (Fig. 5.8). Without this shorting the IGBT functions as a thyristor and, once turned on, the device enters latch up and gate control is lost. To overcome this we had to design a new mask which ensured the shorting of emitter and channel region of the IGBT. The new mask was designed to create a deep window before the deposition of the contact metal. This design is in accordance to our design in Section 3.1 leading to lower resistance in the region and thus reducing the chances of latch up.

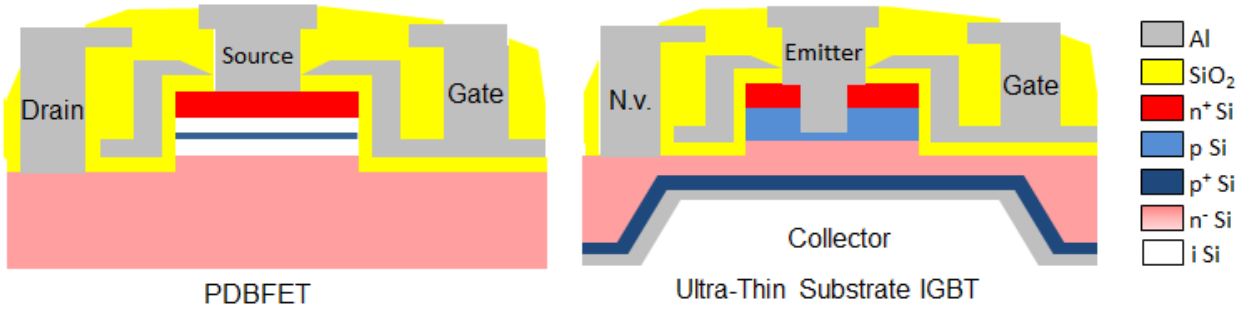

Fig. 5.8 : Difference in Device Structure of MOSFET and IGBT

The design of the new mask was conducted by my fellow colleague Mr. P. Albrodt towards his bachelor thesis at IHT [23]. Table 4.1 shows the entire set of mask used in the fabrication of Ultra-Thin substrate IGBT. It includes mask 3, 4, 5 and 6 from the Uni-BW mask set along with the new mask 5b for deep window etching. The structure of the device formed with these mask set is depicted in Fig. 5.9.

Two IGBTs are placed side by side with different orientation to achieve area efficiency. The top right contact is always of the gate while the emitter contact position varies. An enlarged view of the device also depicted in the aforementioned figure is numbered according to the layers in Table 5.2.

Mask-ID	*Name*	*Mask Type*	*Comments*	*Mask Set*
3	Mesa	Bright Field	1. Lithography	Uni-BW
4	Gate	Bright Field	2. Lithography	Uni-BW
5	Contact Hole	Dark Field	3. Lithography	Uni-BW
5b	Deep Window	Dark Field	4. Lithography	New mask designed
6	Metal Contact	Bright Field	5. Lithography	Uni-BW

Table 5.2 : Mask set used for fabrication of Ultra-Thin Substrate IGBT **[23]**

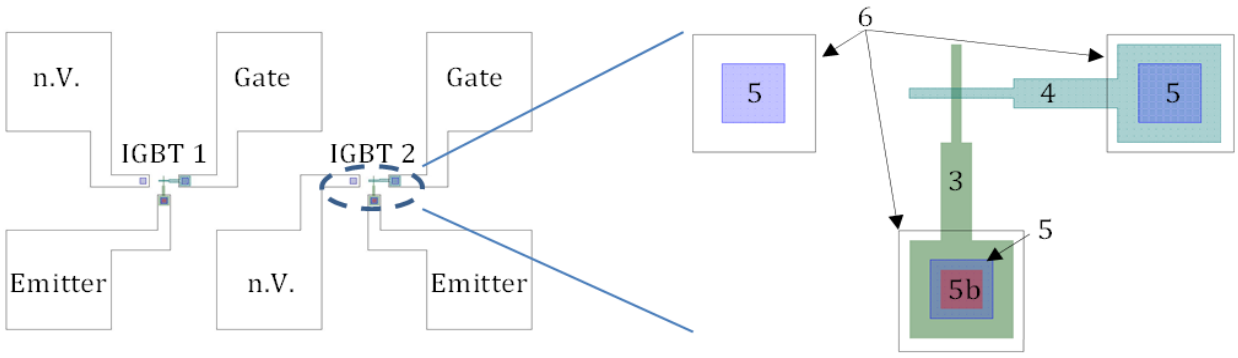

Fig. 5.9 : Device Structure with enlarged view

5.4. Process Flow

The entire overview of the fabrication process flow is illustrated in the Fig. 5.10. It starts with the Ultra-Thin Si membranes as the substrate and concludes with an IGBT structure built on it. The run number for this fabrication was **867-1**

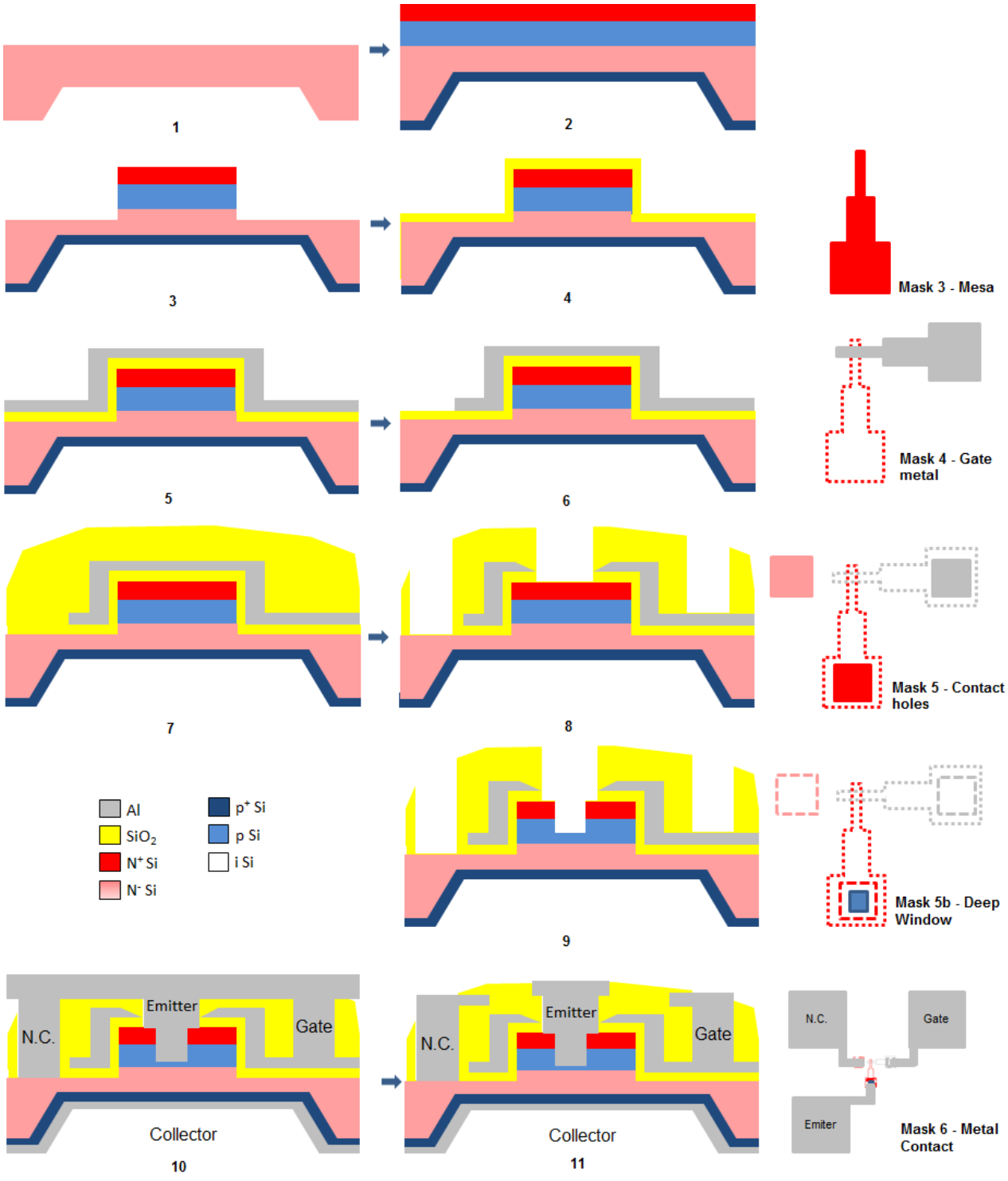

Fig. 5.10 : Fabrication process flow of Ultra-Thin substrate IGBT (run no. 867-1)

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5.4.1. Initial Substrate

With the Si etch technology development discussed in Section 5.2, N^- Si wafers were etched anisotropically using TMAH to get a thin Si membranes a substitute for Ultra-Thin wafers. Among the set of Si membranes etched we chose 4 suitable membranes with varying thickness and good surface quality for the fabrication of Ultra-Thin substrate IGBT. An additional 4 normal N^- wafers were used out of which two were used as test wafers, aiding as a reference for various fabrication process and the rest two for fabrication of conventional IGBT with a drift layer of thickness around 530µm.

The summary of the substrates used in the run 867-1 is given in Table 5.3

Wafer ID	*Membrane*	*Substrate Thickness*	*Comments*
867-1-T1	No Membrane	$t = 530\ \mu m$	Test Wafer
867-1-T2	No Membrane	$t = 530\ \mu m$	Test Wafers
867-1-1	Membrane	$t = 140\ \mu m$	IGBT on Membrane
867-1-2	Membrane	$t = 190\ \mu m$	IGBT on Membrane
867-1-3	Membrane	$t = 270\ \mu m$	IGBT on Membrane
867-1-4	Membrane	$t = 70\ \mu m$	IGBT on Membrane
867-1-5	No Membrane	$t = 530\ \mu m$	Conventional IGBT
867-1-6	No Membrane	$t = 530\ \mu m$	Conventional IGBT

Table 5.3 : Substrates used for run 867-1

Out of the membranes chosen, in a few membranes like 867-1-3, although the surface of the membranes was quiet smooth, the edge of the wafer had a lot of deformations. This is shown in Fig. 5.11. This was probably caused due to bad oxide coverage while etching the membranes. Even though a thick oxide of around 1µm was deposited on both the front and back side of the wafer, the coverage on the side walls of the wafer was not good. With the BHF dip to remove the oxide in the exposed region after lithography and RIE etching the side walls might have been exposed and as a result the TMAH started etching from the side walls. Even with these deformations, we still selected this membrane because the surface quality was very good and there were no pinholes in the active area.

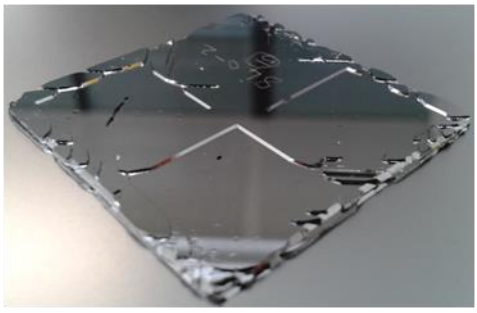

Fig. 5.11 : Deformations at the edge of wafer surface (867-1-3)

5.4.2. MBE Layer Deposition

The next step after choosing the substrates was to deposit necessary layers of doped Si to fabricate an IGBT. Since the wafers need to be perfectly cleaned before loading it into the MBE chambers a standard cleaning process with Piranha, RCA1 and RCA2 cleaning is carried out for all the substrates. The MBE layers were not deposited on the test wafers (867-1-T1 & 867-1-T2) as they were just meant for reference. The layers to be deposited over the substrate are summarized in Table 5.4.

MBE Process No.	*Layer Type*	*Doping Material*	*Layer Concentration*	*Layer Thickness*	*Deposited on Wafer (867-1-x)*
A3709	P++	Boron (B)	1.00 x 10^{20} cm^{-3}	400 nm	5 & 6
A3710	P++	Boron (B)	1.00 x 10^{20} cm^{-3}	400 nm	1,2,3 & 4
A3711	N++/P+	Antimony (Sb)/Boron (B)	2.00 x 10^{20} cm^{-3}/5.00 x 10^{18} cm^{-3}	400nm /300 nm	5 & 6
A3712	N++/P+	Antimony (Sb)/ Boron (B)	2.00 x 10^{20} cm^{-3}/5.00 x 10^{18} cm^{-3}	400 nm /300 nm	1,2,3,4,

Table 5.4 : Deposited MBE layers

The process A3709 is the deposition of the collector region only for the conventional IGBT. As these are just industrial grade N^- wafer without any membranes and had CMP polished bottom surfaces they were processed separately. The layer A3710 also corresponds to the deposition of the collector layer on the bottom side for the membrane devices after which a short HF dip was given. The process A3711 and A3712 correspond to the deposition of the channel layer and emitter layer on the top side of CMP polished 4 inch wafer and membranes, respectively.

A problem was encountered in the MBE machine during the process A3711 and A3712 i.e. deposition of the emitter layer as the receipe was not optimised to depositing 400nm layer. It was developed for 200nm thick deposition only. The flux of Antimony was so high that it led to Antimony segregation, which is a phenomenon where, due to the mismatch in the radius of the atoms of Antimony and Silicon, the Antimony atoms tend to jump up to the uppermost layer forming non-uniform clusters at top [24]. This leads to a very rough top layer. However, after careful examination we found that in most of the wafers there were small area where no Antimony segregation has occurred, thus the surface was not rough and so we continued further with the process.

5.4.3. Mesa Etching

The structuring of the mesa is carried out following the deposition of the MBE layers. The mesa height has to be chosen so that the top N-P-N structure is separated for every device i.e. between every device the layers should be etched till the N^- drift layer at least and preferably deeper.. The exact height to be etched (h_{mesa}) is given by:

$$h_{mesa} = Emitter\ thickness + Channel\ thickness + Safe\ depth \\ = 400\ nm + 300\ nm + 300\ nm = 1\ \mu m \quad (5.1)$$

This step involves the first photolithography in the fabrication with the mask 3 (Table 5.2). It involves spinning of the photoresist AZ6612 followed by hard baking, exposure and development. The etching of the mesa is done by *Inductively Coupled Plasma (ICP) Reactive Ion Etching* (RIE) which uses chemically reactive gases assisted with plasma generated by radio frequency (RF) powered magnetic fields. The usage of RF power enable the generation of plasma at a much lower temperature and thus the MBE layers are not subjected to high temperatures which might lead to diffusions at the layer boundaries. The plasma of HBr gas is used to etch the mesa.

The rough surface due to antimony segregation in the top MBE layer produces a serious issue in the etching process. The regions with initial roughness from the MBE growth turn black after mesa etching as the higher rough surface absorbs more light in contrast to the smooth surface which reflects light. The difference in roughness before and after the mesa etching is inspected using an optical microscope as shown in Fig. 5.12 and Fig. 5.13 respectively. There is a clear distinction between the reflectivity of the surface indicating the degree of roughness.

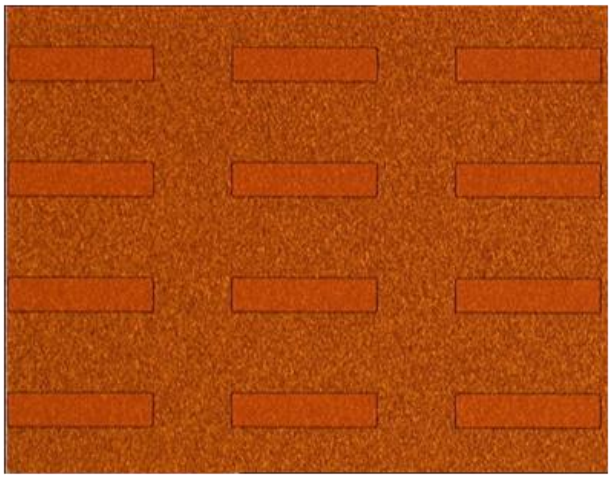

Fig. 5.12 : Test Structure just before mesa etching

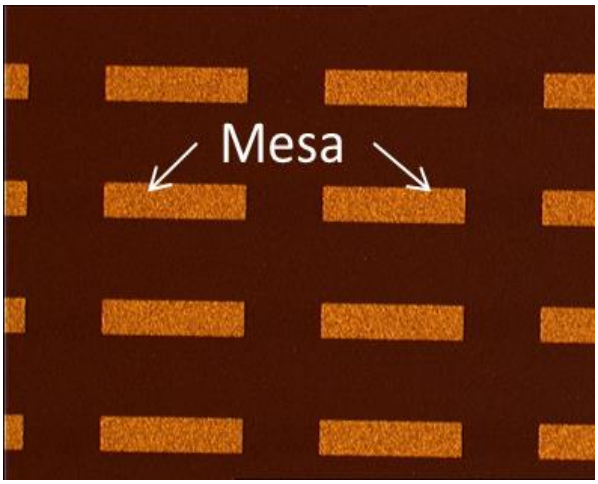

Fig. 5.13 : Test structure after mesa etching

Another problem that arises with the roughness is that the exact mesa height cannot be measured after etching. The ICP-RIE machine etch rate is specific to the run, thus, the machine is conditioned every time before every set of etch, then a couple of test runs are done with test wafers to calculate the etch rate. Thereafter the device wafers are etched for a calculated time and the height of the mesa is measured using a profilometer. However, in our run measurement with profilometer was unsuccessful as the tip of the profilometer jumped from one peak to other without recording the depth of the troughs due to high roughness. The etch rate (r) in this case was predicted from the test wafers.

$$r_{T1} = \frac{h_{mesa}}{t_{etch}} = \frac{940\ nm}{200\ s} \approx 282\ \frac{nm}{min} \quad (5.2)$$

$$r_{T2} = \frac{h_{mesa}}{t_{etch}} = \frac{915\ nm}{210\ s} \approx 261\ \frac{nm}{min} \quad (5.3)$$

$$t_{etch\_m} = \frac{h_{mesa}}{r_{T2}} = \frac{1\ \mu m}{261\frac{nm}{min}} \approx 230\ s \quad (5.4)$$

The etching of the device wafers were thus done for a total of 250s and the remaining photoresist is removed. Again, the actual mesa height couldn't be measured at the end of the process owing to the high roughness of the surface. A 3-D schematic of the mesa structure is shown in Fig. 5.14

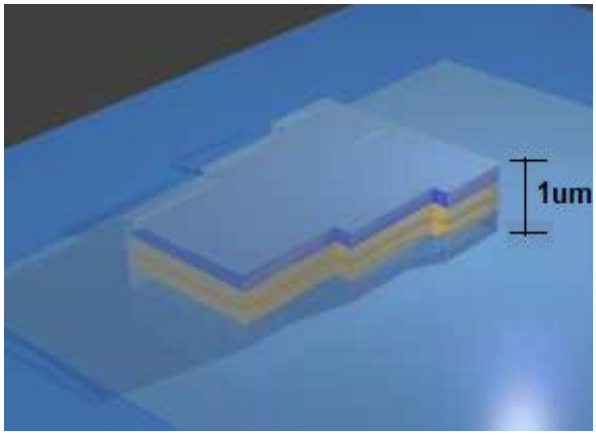

Fig. 5.14 : 3-D schematic of the mesa after ICP-RIE **[25]**

5.4.4. Gate Oxide Deposition

Following the mesa etching a short HF dip is given to the wafers prior to the deposition of gate oxide by Plasma Enhanced Chemical Vapour Deposition (PECVD) using Tetraethyl Orthosilicate (TEOS) as the precursor. The agitation of the TEOS with RF or DC power to form plasma allows thermal decomposition of TEOS at around 100° C. This low temperature deposition prevents the thermal diffusion of doping atoms. Again the machine is highly sensitive and needs to be calibrated and conditioned before every run, then a test run is conducted to measure and calculate the deposition rate (r_{dep_gox}) and thus the exact time (t_{dep_gox}) to achieve the required thickness is determined. In our fabrication we use a 20 nm thick gate oxide layer (d_{gox}).

$$r_{dep\_gox} = 49\ \frac{nm}{min} \quad (5.5)$$

$$t_{dep\_gox} = \frac{d_{gox}}{r_{dep\_gox}} = \frac{20\ nm}{49\frac{nm}{min}} \approx 25\ s \quad (5.6)$$

Thus, on the device wafer the deposition is done for 24 seconds to achieve a 20 nm thick gate oxide lay

5.4.5. Gate Metal Deposition

To prevent the contamination of the gate oxide the wafer has to be immediately deposited with the gate metal. This is done by the sputtering system from Oxford Instruments in our laboratory at IHT. The sputtering is done by removing atoms from the metal source target using RF agitated plasma and allowing it to deposit on wafer. The desired thickness of gate electrode was 600 nm (d_{Al}). The deposition rate (r_{dep_1}) and time (t_{dep_Al}) is given by:

$$r_{dep\_Al} = 400\ \frac{nm}{min} \tag{5.7}$$

$$t_{dep\_Al} = \frac{d_{Al}}{r_{dep\_Al}} = \frac{600\ nm}{400\frac{nm}{min}} \approx 90\ s \tag{5.8}$$

The deposition of Al was done for 95 seconds but later inspection with profilometer showed the actual thickness to be 800nm. However, the thickness of the gate electrode is not a critical parameter and only influences the thickness of passivation oxide to be deposited on the device for proper coverage.

5.4.6. Structuring of Gate Metal

The next step involves the structuring of the gate metal to form gate fingers over every device. It includes a photolithography step similar to the one discussed in Section 5.4.3 but with mask 4. The Uni-BW mask set has various different kinds of gate fingers [25] ranging from thick to thin and double and triple fin gate fingers. The structure of the mask and the position of the gate finger with respect to the mesa structure are shown in Fig. 5.4 Step 6.

After the entire photolithography steps involving the photoresist spinning, hard bake, mask alignment, exposure and development, the exposed aluminium needs to be completely etched. This is again done with the ICP RIE machine with HBr as the etch gas. An approximate etch rate is deduced from the test wafer and the approximate time to etch 800 nm Aluminium is calculated.

$$r_{etch\_Al} = 480\ \frac{nm}{min} \tag{5.9}$$

$$t_{etch\_Al} = \frac{d_{Al}}{r_{etch\_Al}} = \frac{680\ nm}{480\frac{nm}{min}} \approx 85\ s \tag{5.10}$$

The RIE etching was done for 85 seconds followed by 30 seconds of over etch and thereafter wet etched in H_3PO_4 to remove any leftover metals from the sidewalls. After this, the remaining photoresist from the wafer was removed and it was inspected using an optical microscope which confirmed good quality of the gate structures.

5.4.7. Passivation Oxide Deposition

Following the structuring of gate electrode, a low temperature passivation oxide is deposited with PECVD using TEOS precursor at 250 ˚C. The rule of thumb adopted in our laboratory is that the thickness of the passivation oxide must be a minimum of 100 nm more than the thickness of gate metal deposited. This rule ensures the complete coverage of the gate fingers with passivation oxide. The thickness of gate electrode being 800 nm, the thickness of passivation oxide to be deposited is 900 nm (d_{pox}). Again the deposition rate (r_{dep_pox}) is calculated from the runs on the test wafer and the exact deposition time (t_{dep_pox}) is determined by:

$$r_{dep\_pox} = 54\ \frac{nm}{min} \tag{5.11}$$

$$t_{dep\_pox} = \frac{d_{pox}}{r_{dep\_pox}} = \frac{900\ nm}{54\ \frac{nm}{min}} \approx 1000\ s \tag{5.12}$$

The oxide deposition is done for the stipulated period of time and then the wafer is measured to determine the actual thickness of the passivation oxide. This measurement is done using a Reflectometer which uses the reflectivity of various incident radiations to determine the thickness of the oxide layer. Under the inspection of the Reflectometer the oxide thickness showed to be 930 nm which is quiet acceptable. The next step involves the etching of the passivation oxide to form contact windows over the contact region.

5.4.8. Etching of the Contact Window

This step involves the third lithography step of the fabrication and is similar to the previous lithography step only with the mask number 5 as shown in Fig. 5.10 Step 8. However due to poor contrast difference between the top passivation oxide layer and the mask itself alignment was a serious problem. The best fit alignment was performed; however some deviations were still observed but were within the limits to make contact with gate electrode and mesa region.

The etching of the oxide is done in parts. The initial majority thickness of the oxide is etched by the Sentech RIE equipment which uses CF_4 as the etchant

$$r_{etch_{RIE}} = 49\ \frac{nm}{min} \tag{5.13}$$

$$t_{etch\_RIE} = \frac{d_{pox\_RIE}}{r_{etch\_RIE}} = \frac{880\ nm}{49\ \frac{nm}{min}} \approx 1080s \tag{5.14}$$

The remaining oxide is removed by a BHF dip. The etch rate and required etching time is calculated below:

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$$r_{etch\_HBF} = 100\ \frac{nm}{min} \quad (5.15)$$

$$t_{etch\_HBF} = \frac{d_{pox\_HBF}}{r_{etch\_HBF}} = \frac{50\ nm}{100\ \frac{nm}{min}} \approx 30s \quad (5.16)$$

During the RIE it was however experienced that the selectivity of oxide to photoresist etching was lower than the expected value. In the regions with tiny dimensions, the photoresist was completely etched along with the passivation oxide below it. When this was followed by a BHF dip, the exposed aluminium gate fingers with smaller dimensions also got etched away. This problem was detected later during the lithography of the next step i.e. the deep window etching (both optical images below are taken after the photolithography of the next step). This problem was seen in both the test wafers (Fig. 5.15) and device wafers (Fig. 5.16) so we could conclude that it was not due to the rough MBE layers but due to problems in the etching process.

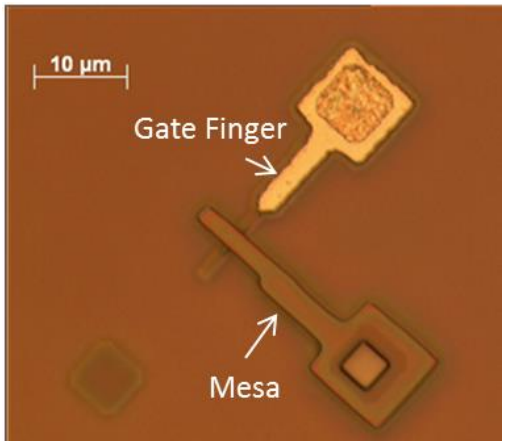

Fig. 5.15 : Gate fingers completely etched in 867-1-T1

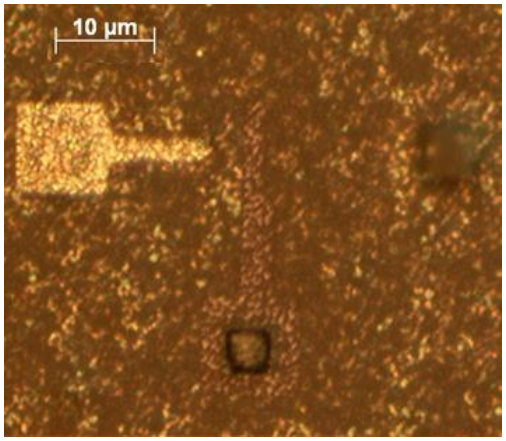

Fig. 5.16 : Gate fingers completely etched in 867-1-5

It was also observed that even though some of the gate electrodes were not removed, they were completely exposed. This would lead to improper electrical isolation of the electrodes. This was confirmed by inspection of the wafer using a Scanning Electron Microscope (SEM). As shown in Fig. 5.17 the left part of the mesa has oxide while the aluminium over the mesa is exposed.

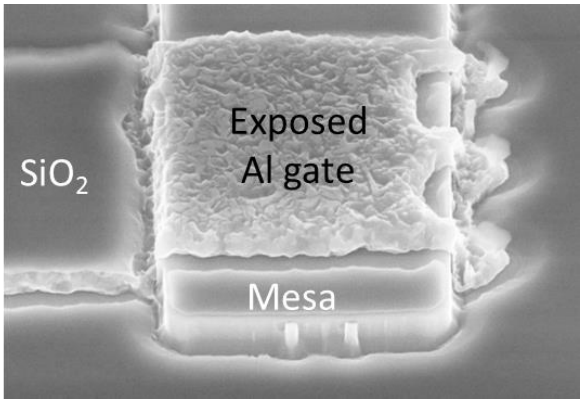

Fig. 5.17 : SEM image of exposed gate metal

5.4.9. Deep Window Etching

The step following the etching of contact window is the etching of the deep window which provides the necessary shorting of the emitter and channel region. This step involves the fourth lithography step of the fabrication with the newly designed mask 5b. This step is a critical step as it has huge impact on the functioning of the device.

Etching of the deep window should strictly terminate within the P^+ channel region to have a working IGBT. If the etch is too shallow i.e. it doesn't reaches the P^+ channel region and is restricted to the N^+ emitter region then the necessary shorting of the emitter and channel region is not met. On the other hand if the window is etched too deep and touches the N^- drift region then the entire device crumbles down to a p-n junction which is not desirable. The exact height to be etched is therefore given by:

$$h_{Deep\_Window} = Emitter\ thickness + \frac{2}{3}\ Channel\ thickness \qquad (5.17)$$
$$= 400 + \frac{2}{3}300\ nm = 600\ nm$$

The etching is again performed with the ICP-RIE machine and the etch rate is determined by test runs and then the actual etch time is calculated to get the required depth.

$$r_{etch\_DeepWin} = 255\ \frac{nm}{min} \qquad (5.18)$$

$$t_{etch\_DeepWin} = \frac{d}{r_{etch\_DeepWin}} = \frac{600\ nm}{255\ \frac{nm}{min}} \approx 145s \qquad (5.19)$$

After etching for the calculated amount of time the depth of the deep window was measured to be approximately 550 nm which is acceptable as it surely makes contact with the P^+ channel region. To study the actual profile of the deep window a SEM and a 3 dimensional profiling was done as depicted in Fig. 5.18 and Fig. 5.19 respectively. It can be seen that the alignment of the deep window is not exactly at the centre of the contact window as the mask alignment proved to be a serious challenge with the non-uniform surface of the wafer. A detailed encounter of this step is discussed in [23].

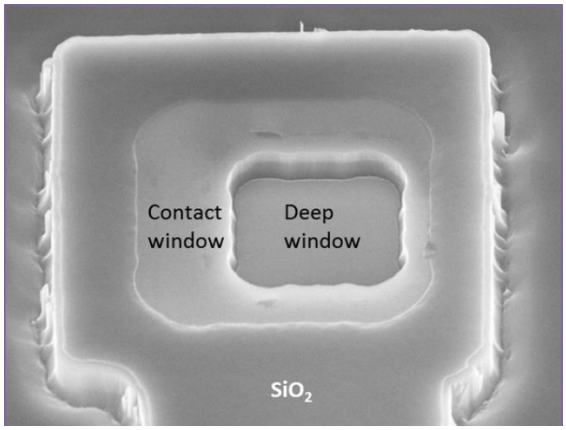

Fig. 5.18 : SEM image of the Deep window in 867-1-T1

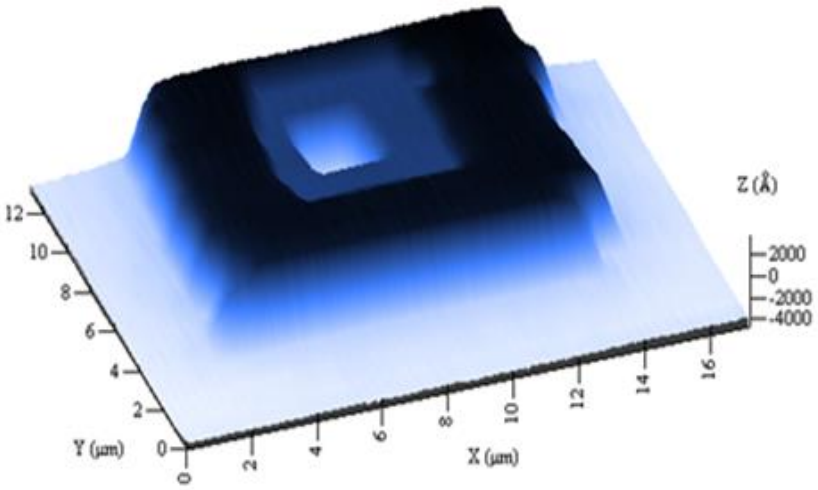

Fig. 5.19 : Three-dimensional profiling of the deep window

5.4.10. Electrode Metal Deposition and Structuring

After the etching of the deep window the next step involves the deposition of the electrode metal which is similar to the step discussed in Section 5.4.5. The deposition needed to be done on both the top and bottom side of the wafer. The desired thickness of the Al sputter was 1400 nm. As calculated from equations (5.7) and (5.8) the deposition time was calculated to be 210 seconds. The actual deposition height was confirmed to be of 1400 nm with measurements from profilometer. The structuring of the electrodes on the top surface were done with the last photolithography step with mask 6 followed by ICP-RIE with HBr and then wet chemical etching using H_3PO_4, similar to the process in Section 5.4.6. After the etching process the remaining photoresist were removed and the wafers were visually inspected.

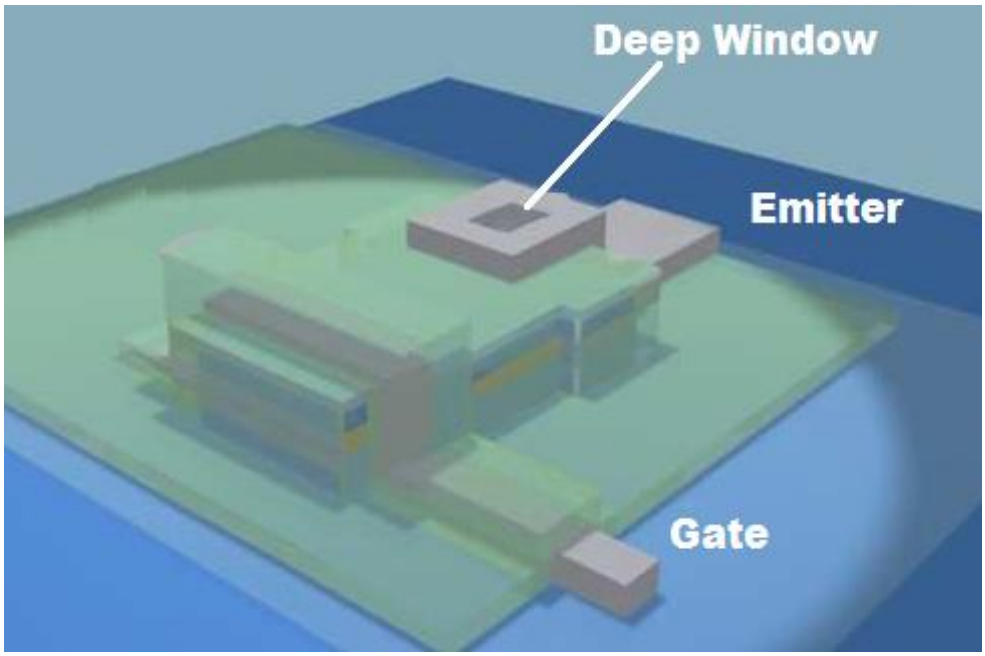

Fig. 5.20 : 3-D Structure of the Ultra-Thin substrate IGBT **[25]**

5.5. Process Summary

The fabrication process of the run 867-1 was successfully completed even with the numerous problems faced during the process.

Another major problem that we encountered and have not been discussed so far was the difficulties in all the photolithography steps. Due to the membranes on the back side of the wafer and uneven surfaces the photoresist spinning was a challenging task. Careful and marked placement of the wafer had to be done so that the vacuum was able to hold the wafer in order to prevent it from flying away during the photoresist spinning.

This problem of rough bottom surface leading to poor vacuum holding also posed a challenge during mask alignment. After every alignment check, the wafer moved, so only predictive corrections of alignment could be done. In the end, after exposure the wafer would stick to the mask even when the chuck has been lowered. We practically had to knock the top surface of the mask to force the wafer to fall back to the chuck. Again this had a high risk of breaking the membrane while falling and had to be executed with utmost care.

Overall, even with so many problems, the fabrication turned out to be quiet robust as we could complete the fabrication for 3 of the initial 6 substrate wafer we started with.
The summary of the run is shown in

Wafer ID	*Fabrication Summary*	*Comments on quality*
867-1-1	Successfully Completed	Has areas with low roughness
867-1-2	Successfully Completed	Has areas with low roughness but one membrane window is broken post fabrication
867-1-3	Successfully Completed	Has areas with low roughness
867-1-4	Broken	Not completed
867-1-5	Successfully Completed	Completely rough and black hence not useable
867-1-6	Successfully Completed	Completely rough and black hence not useable

Table 5.5 : Summary of the run 876-1

The optical images of the fabricated wafers are shown below:

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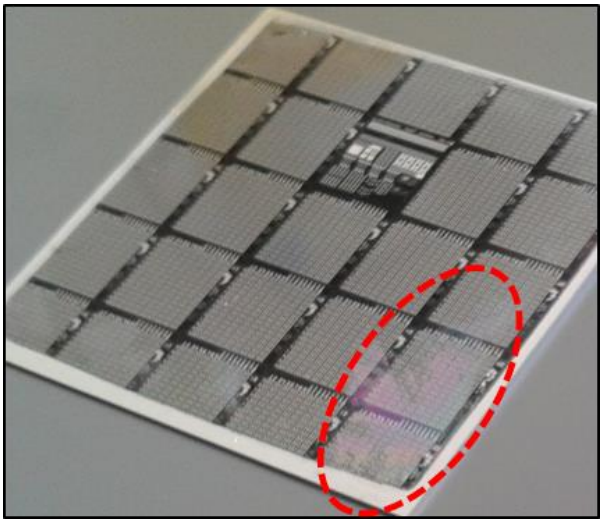

Fig. 5.21 : 867-1-1 with less rough area marked in red

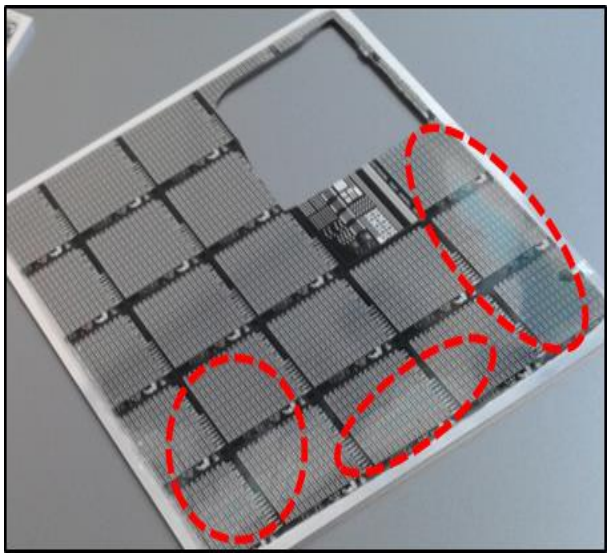

Fig. 5.22 : 867-1-2 with less rough area marked in red

6. Electrical Characterization

6.1. Instruments and Test Setup

For the Electrical characterization of the fabricated Ultra-Thin substrate IGBT we use the KEITHLEY 4200 Semiconductor Characterization System (SCS) attached with Karl Suss Probe Station in our laboratory at IHT.

The 4200-SCS (Fig. 6.1) is a modular, fully integrated parameter analyser that performs electrical characterization of materials and semiconductor devices. The system has 3 Medium Power Source Measuring Unit (SMU) and 1 High Power SMU which acts as a constant voltage or current source and also as a high precision sensing unit with a preamplifier. Every SMU has 2 ports one for forcing the voltage or current to the Device Under Test (DUT) and one to sense the voltage or current.

The Probe Station has 4 micromanipulators which can move precisely in three dimensions and a wafer chuck connected to the vacuum line to hold the wafer. . Each micromanipulator has a probe needle with the tip diameter of 30 micron to probe the contact pads of DUT. The entire setup is shown in Fig. 6.2.

Fig. 6.1 : Keithley 4200 SCS tool at IHT

The collector electrode in our Ultra-Thin substrate IGBT is on the bottom side of the wafer so we used the chuck contact for the collector region. However, the disadvantage of using the chuck is the series resistance and the parasitic shunt capacitance of the chuck affects the device characteristics. A single input to double output triaxial convertor is used to separate the force and the sense wire, thereby removing the series resistance of the measuring wires. These are connected to the force and sense port of SMU 1 respectively. The gate electrode which we intend to use only as a force probe, as we do not need measurements of the gate current, is only connected to the force probe of SMU 2. Finally the emitter contact uses the two probes to nullify the series resistance of the measuring cable and is connected to SMU 3.

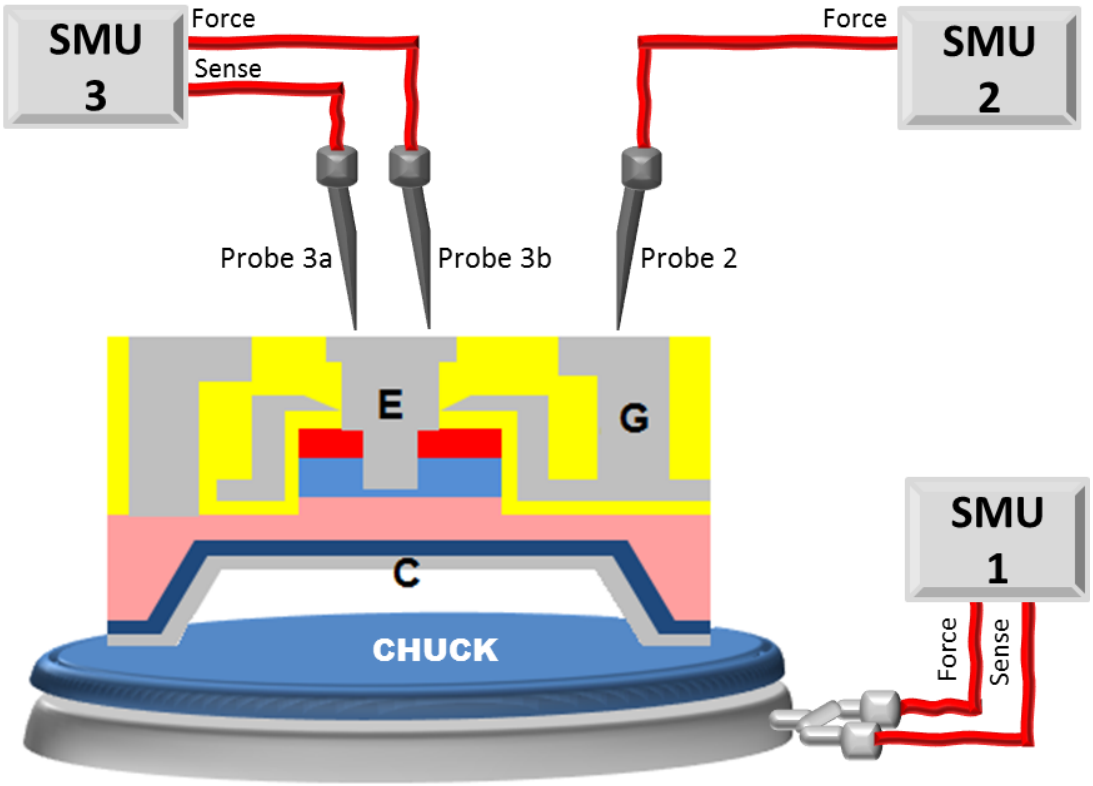

Fig. 6.2 : Electrical characterization test setup

6.2. Static Characteristics

As discussed in Section 2.6 Static characteristics of the IGBT consist of output characteristics and transfer characteristics in forward biased mode. In this section, Forward bias, reverse bias and Junction characteristics of the fabricated IGBT is presented and analysed.

6.2.1. Output Characteristics

The output characteristics comprise of the set of traces in which each trace is obtained by measuring the collector current (I_{CE}) as a function of collector-emitter voltage (V_{CE}) with constant and distinct gate-emitter voltage (V_{GE}). The forward output characteristic of a device from 867-1-3 on the non-membrane region is shown in Fig. 6.3.

Since the device is on a non-membrane region the effective drift region is 530 µm thick. It can be observed from the output characteristics that the maximum current is in the range of 8 X 10^{-4} A. The maximum current density (J_{Cmax}) is given by:

$$J_{Cmax} = \frac{I_{Cmax}}{Area\ of\ Mesa} = \frac{8\ X\ 10^{-4}}{140\ X\ 10^{-8}} = 571.43\ A/cm^2 \qquad (6.1)$$

Where, the *Area of the Mesa* is taken from the designed mask parameters (Appendix C)

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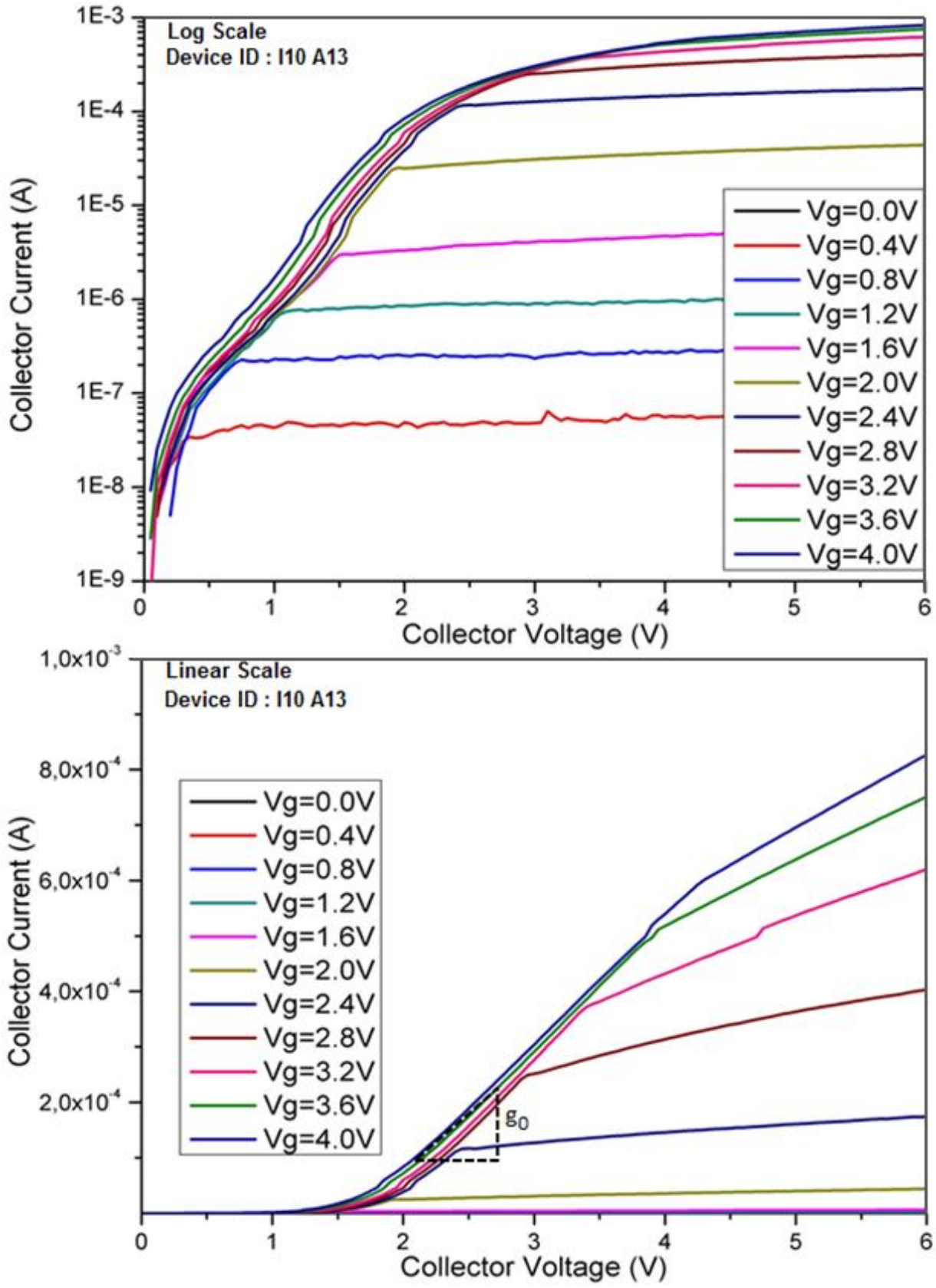

Fig. 6.3 : Output characteristics of a non-membrane device on 867-1-3

These collector current traces were measured by sweeping the collector voltage from 0 to 6V while stepping the gate voltage from 0 to 4V in steps of 0.4 V. The gate response of the device is observed to be between 0 and 3 V which is quiet acceptable. The current gain ratio (I_{ON}/I_{OFF}) of the device is given by:

$$I_{ON}/I_{OFF} = \frac{I_{Csat}\ at\ ON\ state}{I_{Csat}\ at\ \ OFF\ state} = \frac{8\ X\ 10^{-4}}{2\ X\ 10^{-8}} = 4\ X\ 10^{-4} \qquad (6.2)$$

The current gain ratio thus has a high value which is desirable. However, the offset or knee voltage as seen for the linear output characteristics is around 1.5 V as compared to the normal range of around 0.7 V [13]. A hypothesis is due to the huge collector junction on the bottom side which is common to all the devices. Due to the large area of the junction, a small defect in any part of the junction affects every device on the same wafer. The possible solution is to dice the chips and then measure them for proper readings.

The output conductance (g_0) of the IGBT is given by the slope of the linear output characteristics in the linear region by:

$$g_0 = \left.\frac{\partial I_{CE}}{\partial V_{CE}}\right|_{V_{GE}=Constant} \qquad (6.3)$$

Gate Voltage (V) V_{GE}	Collector Voltage (V) V_{CE}	Collector Current (µA) I_{CE}	$\frac{\partial I_{CE}}{\partial V_{CE}}$ (mho)
4	2.40	166.0860	233.7334E-6
4	2.45	177.0199	218.6777E-6
4	2.50	188.7465	234.5323E-6
4	2.55	200.2502	230.0745E-6
4	2.60	211.5710	226.4165E-6
		Average =	**228.6869E-6 mho**

Table 6.1 : Calculations for output conductance g_0 of device I10A13

The output characteristics of a device on a membrane are shown in Fig. 6.4. The maximum current level and the gate response are similar to that of the previous non-membrane device.

However, we see a dip in saturated collector current with the increase in collector voltage. The exact reason for this phenomenon could not be confirmed but is expected to be due to charge storage in the drift region [26]. Also, the collector of the devices on membrane is not directly connected to the chuck but is connected via the collector electrode in the non-membrane region (Fig. 6.2). This may add a huge series resistance in the path of the current and prevents it from having the characteristics of an Ultra-Thin substrate IGBT. The possible solution is to dice the membrane devices out of the wafer and then measure to devices to be sure that the effects of series resistance are not present.

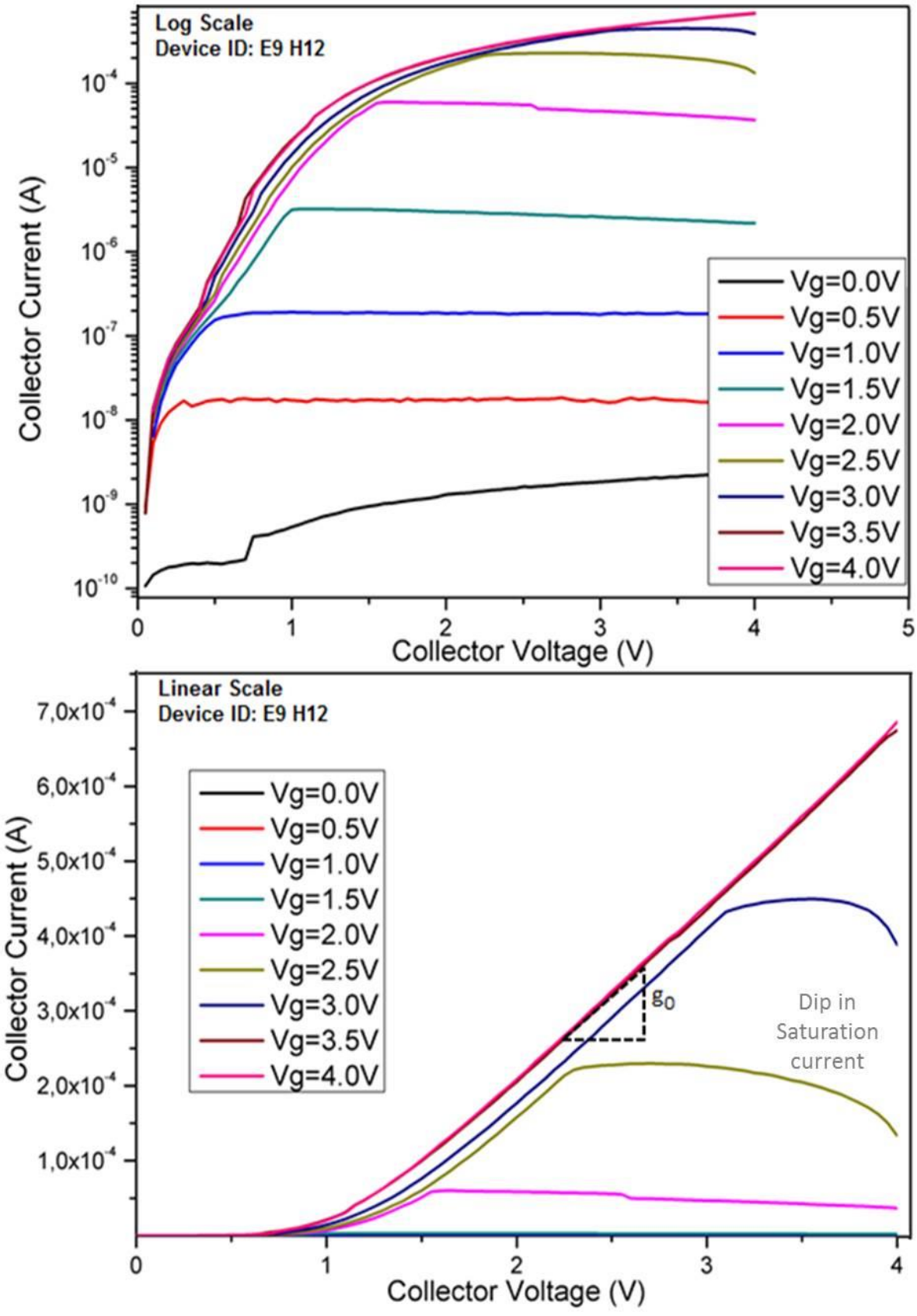

Fig. 6.4 : Output characteristics of a membrane device on 867-1-2

Gate Voltage (V) V_{GE}	Collector Voltage (V) V_{CE}	Collector Current (µA) I_{CE}	$\frac{\partial I_{CE}}{\partial V_{CE}}$ (mho)
4	2.60	349.4172	240.1264E-6
4	2.55	337.4172	239.9995E-6
4	2.50	326.0964	226.4173E-6
4	2.45	313.7074	247.7795E-6
4	2.40	302.5632	222.8847E-6
		Average =	**235.4415E-6**

Table 6.2 : Calculations for output conductance g_0 of device E9 H12

When the output conductance of the device on membrane is compared to the one of the non-membrane devices, it is found that the output conductance of the device on the membrane is higher than its counterpart as expected even with the high series resistance.

6.2.2. Transfer Characteristics

As discussed in Section 2.6.2 the transfer characteristic of a device is obtained by tracing the collector current (I_{CE}) while sweeping the gate voltage (V_{GE}) at a constant collector to emitter voltage (V_{CE}). The transfer characteristics of two devices are shown in Fig. 6.5. Both the graphs are in logarithmic scale, so the threshold voltage is depicted by the point where the graph starts to saturate, i.e. in the linear domain when the collector current enters the linear region. For both the devices the threshold voltage is around 3 V. In industrial grade IGBT the threshold voltage are in the range of 5 V [27] to reduce short-circuit current while switching and increasing the noise margin of the device. However, a threshold voltage of 3 V also falls in the acceptable range for various applications. The dynamic trans-conductance (g_m) of the device is given by the slope in the linear region:

$$g_m = \left.\frac{\partial I_{CE}}{\partial V_{GE}}\right|_{V_{CE}=Constant} \quad (6.4)$$

Collector Voltage (V) V_{CE}	Gate Voltage (V) V_{GE}	Collector Current (µA) I_{CE}	$\frac{\partial I_{CE}}{\partial V_{CE}}$ (mho)
3	2.5	137.444	4.2639E-4
3	2.55	159.589	4.6745E-4
3	2.6	184.190	5.0010E-4
3	2.65	209.599	5.2218E-4
3	2.7	236.408	5.5280E-4
		Average =	**4.9379E-04**

Table 6.3 : Calculations for g_m for device E9 I14

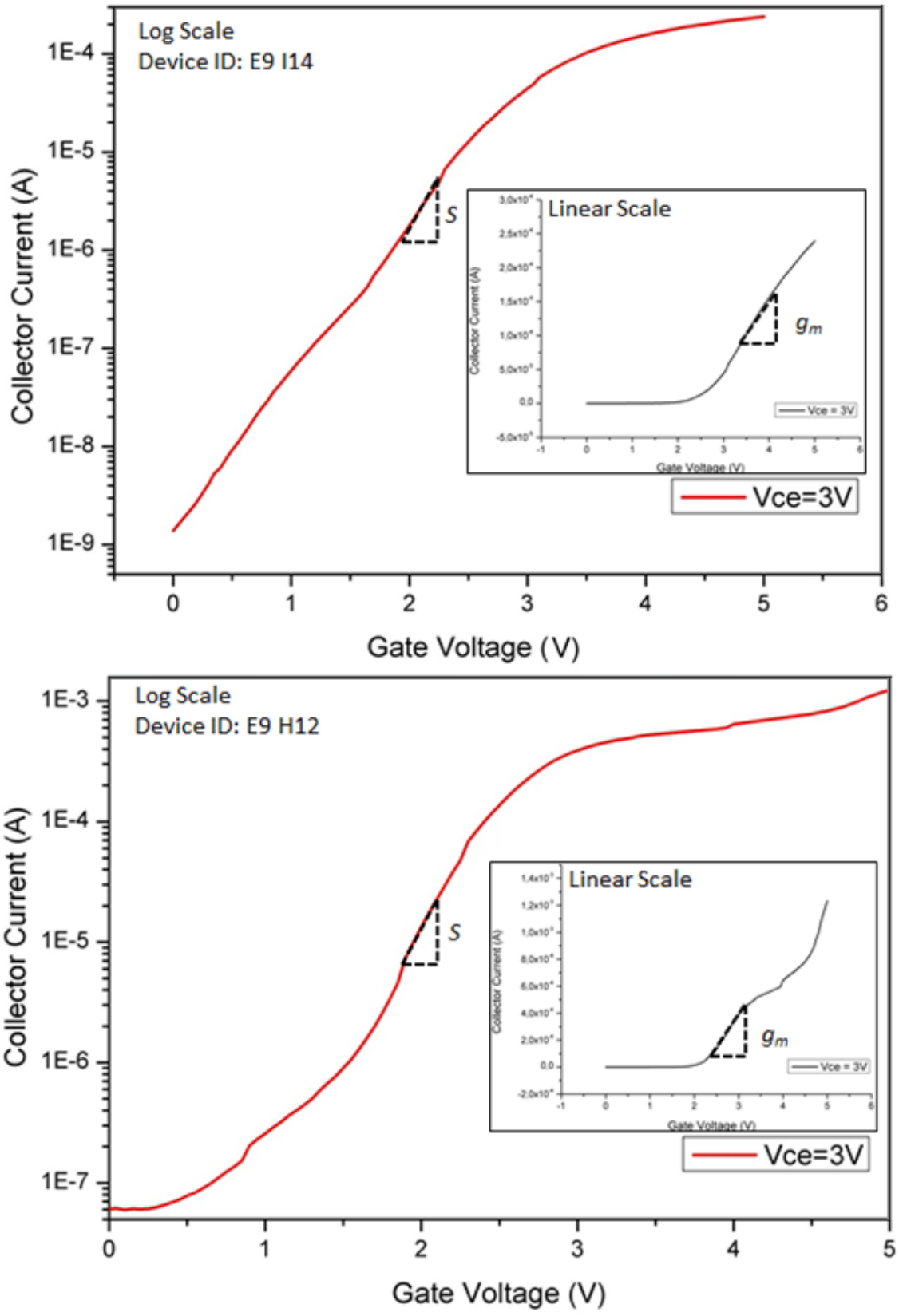

Fig. 6.5 : Transfer characteristics of devices on 867-1-2

Collector Voltage (V) V_{CE}	Gate Voltage (V) V_{GE}	Collector Current (µA) I_{CE}	$\frac{\partial I_{CE}}{\partial V_{CE}}$ (mho)
3	3.5	102.092	5.7319E-6
3	3.55	107.534	5.7380E-6
3	3.6	113.556	5.5018E-6
3	3.65	119.01	5.4757E-6
3	3.7	124.56	5.4544E-6
		Average =	**5.5804E-06**

Table 6.4 : Calculations for g_m for device E9 H12

The sub-threshold swing (S) of the device is given by:

$$S = \left(\frac{\partial \log(I_{CE})}{\partial V_{GE}}\right)^{-1}\Bigg|_{V_{CE}=Constant} = \left(\frac{1}{I_{CE}} X \frac{1}{\ln 10} X \frac{\partial I_{CE}}{\partial V_{GE}}\right)^{-1}\Bigg|_{V_{CE}=Constant} \quad (6.5)$$

Device	Gate Voltage (V) V_{GE}	Collector Current (µA) I_{CE}	$\frac{\partial I_{CE}}{\partial V_{CE}}$ (mho)	S (mV/Dec)
E9 I14	2.2	4.06964E-6	1.29376E-6	**7243**
E9 H12	2.2	3.77154E-5	1.8175E-4	**477.82**

Table 6.5 : Calculation of sub-threshold swing S

6.2.3. *Reverse Bias Characteristics*

Up to now we discussed about the forward output characteristics of the device, i.e. the device operating in forward blocking mode and forward conducting mode. However, when the device was biased to reverse blocking mode, it was observed that the blocking capability of the device was not present. The entire output characteristic in the forward and reverse biased mode is shown in Fig. 6.6.

It was observed that even with a small reverse biased collector voltage the device turned on and reached compliance soon, without the application of any gate voltage. The blocking seen for a small voltage initially is the current blocked by the p-n junction between the channel and drift region until its knee voltage.

One of the possible explanations for this behaviour can be that, while handling of the wafer with tweezers during the fabrication process the collector region might have been scratched thus exposing the drift layer. Consequently when the bottom collector electrode was deposited it had a direct connection with the drift layer which prevented the reverse blocking capabilities. Another reason could be that the top p-n junction between the emitter and the channel region has a lot of deformities due to Antimony segregation and

prevents the device from blocking the reverse bias. In order to check the quality of junctions, a set of electrical measurements have been carried out and presented in the following section.

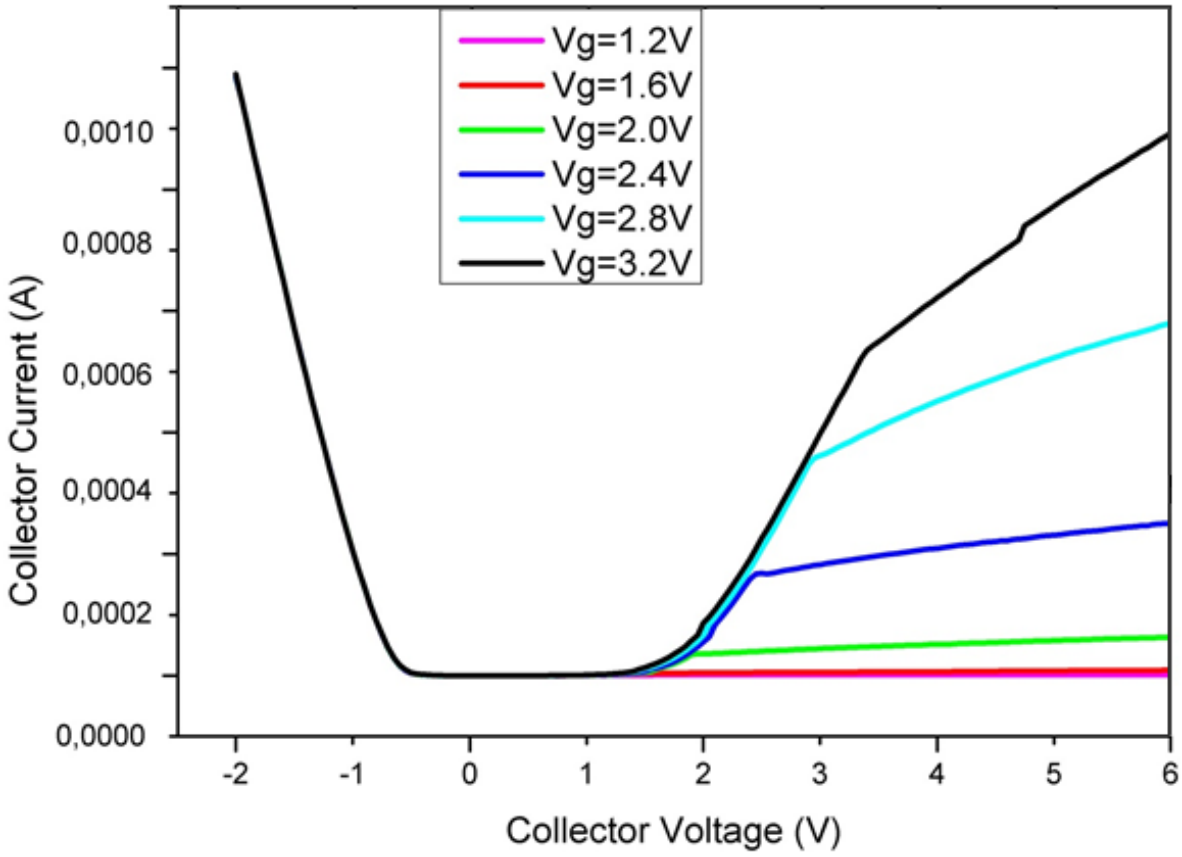

Fig. 6.6 : Reverse output Characteristics of 867-1-3

6.2.4. *Junction Characteristics*

To understand where the problem lies with the reverse characteristics we studied the junction characteristics of the 2 out of 3 junctions in our device. This was possible due to the redundant body contact present due to the usage of the Uni-BW mask set, which is originally used to fabricate PDBFETs.

The p-n junctions that could be measured were the bottom junction between the N^- Drift layer and the P^+ collector region. This characteristic is shown in Fig. 6.7. It can be clearly seen that reverse characteristics of the bottom junction suffers from breakdown at a really early stage. As discussed in previous section the possible explanation for this is that there might have been scratches on the bottom P^+ collector MBE layer, which is quiet thin and the collector electrode may be directly connected to the N^- drift layer at some area. Also, the side walls are exposed to the atmosphere as passivation of the side walls is not possible completely and therefore the surface charge might be causing the early breakdown of the device. However, the middle junction between the channel layer and drift layer shows a good characteristic as shown in Fig. 6.8. The top junction could not be analysed due to the shorting of the emitter and channel region.

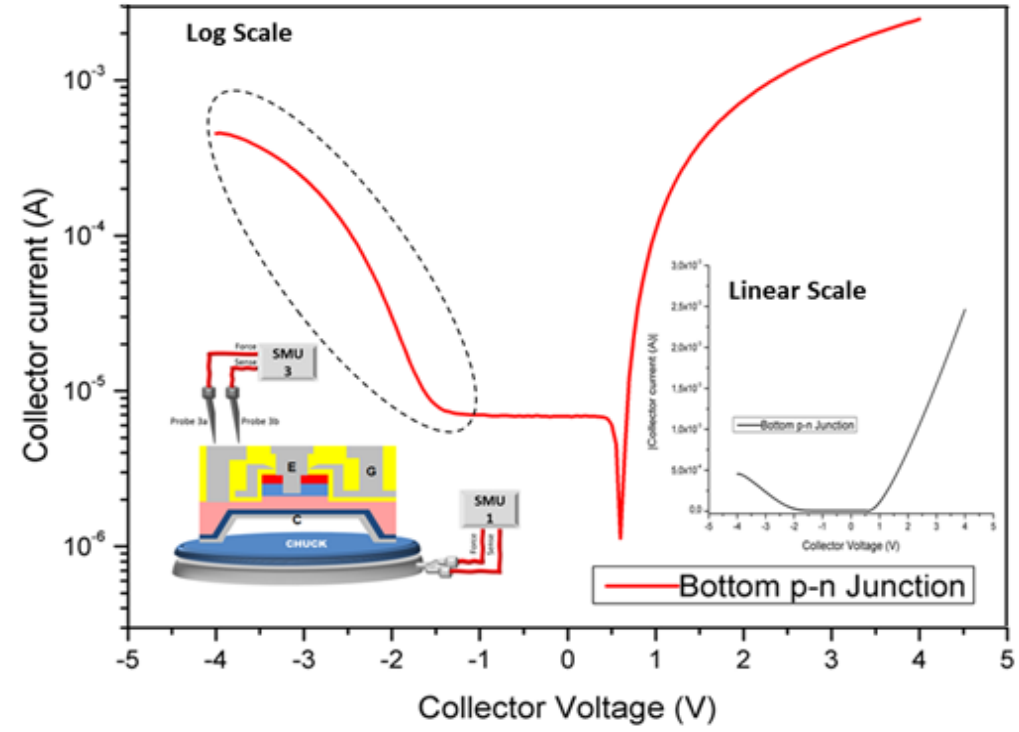

Fig. 6.7 : Bottom junction characteristics Device ID E9 H12

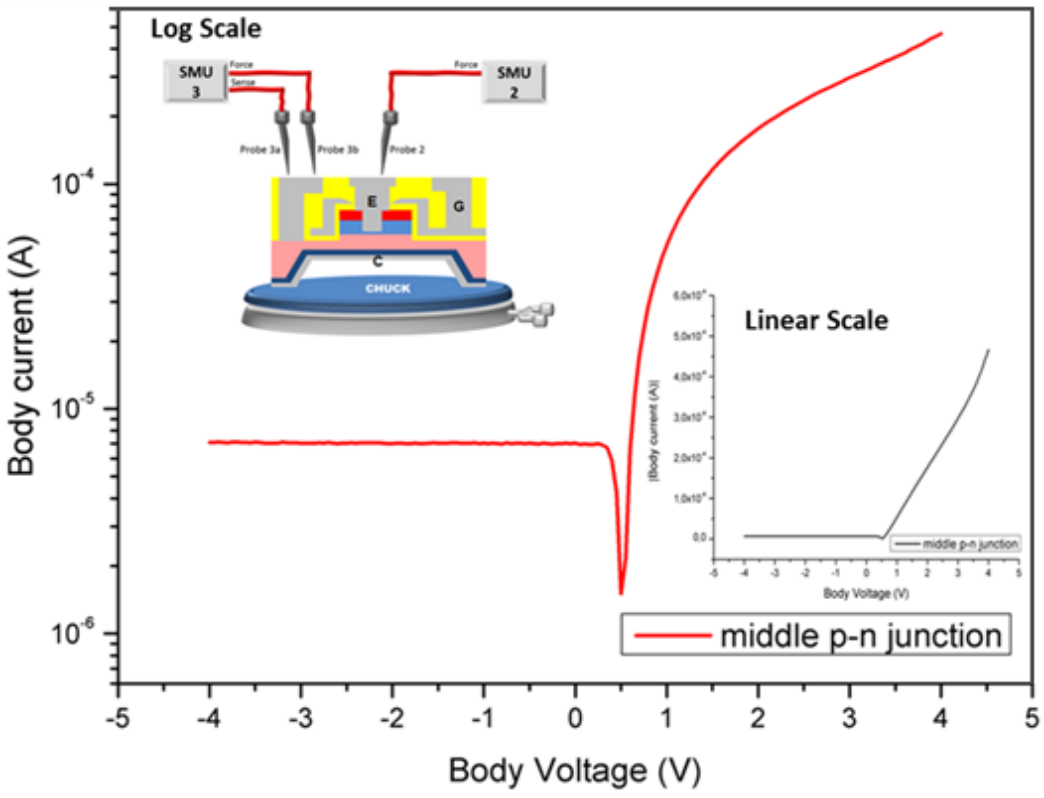

Fig. 6.8 : Middle junction characteristics Device ID E9 H12

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6.3. Comparison with Simulation Results

The electrical characteristics of the fabricated IGBT with the simulation results obtained in Chapter 4 are compared and presented here. The comparison is depicted in Fig. 6.9.

It is observed that the current levels in the fabricated device are almost two orders more in the fabricated device as compared to the simulated device. This can be attributed to fact that the simulation is done with ideal junction characteristics. The defects and other non idealities present in the device bulk and junctions change the characteristics drastically. A possible way to verify this was to include non idealities like, interface trap models into the simulation but due to lack of time this was not possible. Another factor that might lead to this higher magnitude of current is the surface current on the exposed side walls. The possible solution is passivation of the side walls by some means to prevent the surface currents.

However, it is also observed that the gate response is similar in both the fabricated and simulated device and also the ratio of on current to off current is also similar.

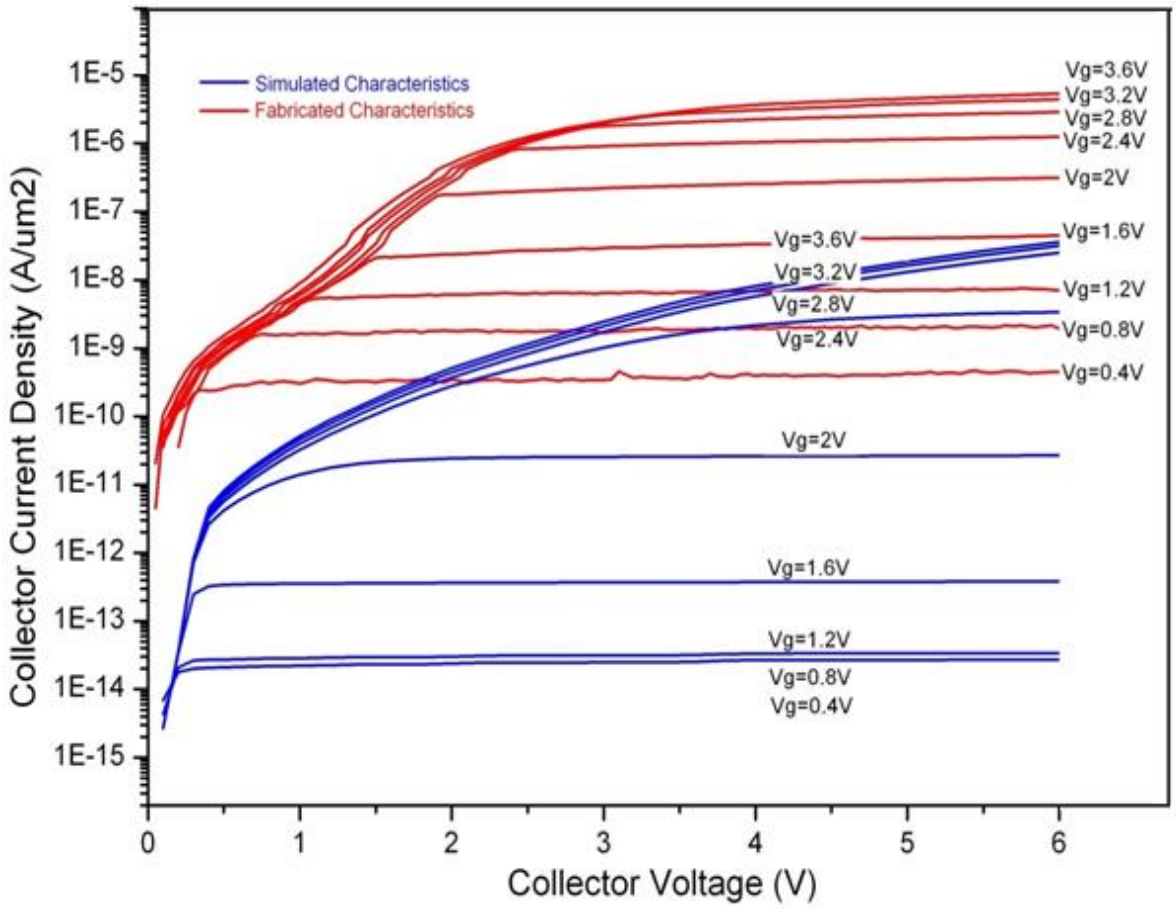

Fig. 6.9 : Comparison of output characteristics of fabricated and simulated device

7. Summary and Future Works

7.1. Summary

The primary aim of this thesis work was to fabricate an Ultra-Thin substrate IGBT with the resources available in an academic research facility like the one at IHT, which, in the long run, would serve as a test vehicle for investigating further techniques to reduce the power loss in an IGBT.

The initial phase of this work involved the theoretical design of our Ultra-Thin substrate IGBT from a trench gate IGBT with minor modifications like, the emitter electrode penetrating into the channel region for better on-resistance and significant reduction of chances of latch-up of the device. This theoretical design was simulated using the device simulator ATLAS from Silvaco to verify that the theoretical design works and to have a general idea of what kind of a characteristics to expect from the fabricated device. The models, so chosen, were to mimic the condition of the actual fabricated device as closely as possible including the effects of having fixed charge and contact resistance specific for the machines at IHT laboratory.

The first challenge in fabrication was to find a suitable alternative for the industrial Ultra-Thin wafer, which could be processed manually. The most promising solution was found in the usage of Si-membranes as a substitute. The Si-membranes were fabricated by anisotropic etching of a normal industrial grade wafer with TMAH. The technology for this etching was developed and important parameters were optimized to achieve good surface quality of the etched membranes. A large number of Si-membranes were etched and from them a set of membranes with varying thickness and good surface quality were chosen to be used as a substrate for the fabrication of Ultra-Thin substrate IGBT.

The required semiconductor layers were deposited precisely by MBE which allowed us to minimize the thickness of all the layers, wherever possible. The Uni-BW mask set along with the addition of the new mask for deep window was used to structure the IGBT. Even with numerous difficulties and technological challenges we experienced during the fabrication process, we were able to complete the entire fabrication process.

The electrical characterization showed the characteristics of an IGBT with a good forward characteristics, sufficient gate response and high on-current to off-current ratio. However, the reverse characteristics suffered from early breakdown. The cause of this problem was also investigated within the time constraint of the thesis and the junction characteristics were studied to explain the problem. It was found that the p-n junction between the collector region and the N^- drift region suffered from premature breakdown. Overall, it could be said that the fabrication process is quiet robust that even with all the difficulties, we were able to fabricate working devices.

Thus an Ultra-Thin Substrate IGBT has been successfully fabricated in our research laboratory using Si-membranes as the substitute for Ultra-Thin wafers.

7.2. Future Works

With the successful fabrication of the Ultra-Thin substrate IGBT the immediate step involves solving the reverse characteristics problem of the device. A step in this direction would be to fabricate the bottom collector region by diffusion so that there is no junction defects due to MBE layers grown on rough surfaces. It is necessary to develop a process for the prevention of Antimony segregation during the deposition of the top emitter region by MBE.

Another important aspect to be considered is to design a mask set specific for IGBT where the design of the structures are optimised. The gate width should be maximized and unnecessary gate electrode dimensions should be removed as they add to the input capacitance of the device and hampers the fast switching characteristics of the device. Also the area of the emitter contact should be maximized for better current handling capabilities. The exposed device layers on the side walls of the wafer must also be passivized somehow to restrict the flow of surface current of the device.

In the domain of reduction of power losses in IGBT, which stands to be our long term goal, we intend to incorporate a δ-doped channel in our device which has proved to reduce the channel resistance in MOSFET. The challenge however remains to achieve the channel region and emitter region shorting due to the restriction of controlling etch depth to a precise range of few nanometres. Another promising modification is the incorporation of 'CoolMOS' principle into the IGBT. This would involve fabricating alternate n-type and p-type pillars in the drift region leading to reduction in the on-state losses of the IGBT.

With this vision, although this thesis work is concluded, an immense amount of work is to be done to achieve our aim of reducing losses in the most dominant power semiconductor device, the IGBT.

Appendix

A. Bibliography

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B. Simulation Structure Code

ATLAS code for Ultra-Thin Substrate IGBT:

```
##################################################################
go atlas
#Mesh Parameters
mesh  space.mult=1.0
x.mesh loc=-0.02 spac=0.01
x.mesh loc=0.00 spac=0.001
x.mesh loc=0.6 spac=0.2
x.mesh loc=4 spac=1
x.mesh loc=7 spac=0.5
x.mesh loc=12 spac=1.5
x.mesh loc=15 spac=1.5
y.mesh loc=0.00 spac=0.1
y.mesh loc=0.4 spac=0.001
y.mesh loc=0.7 spac=0.001
y.mesh loc=70.00 spac=20
y.mesh loc=97.00 spac=1
y.mesh loc=99.60 spac=0.1
y.mesh loc=100.00 spac=0.2
#Region Declaration
region     num=1 x.min=-0.08 x.max=0  oxide
region     num=2 x.min=0.0  silicon
#Electrode Declaration
electrode   name=gate         x.min=-0.02 x.max=-0.02 y.min=0.2 y.max=0.8
electrode   name=emitter     x.min=0 x.max=15 y.min=0 y.max=0
electrode   name=emitter      x.min=7 x.max=15 y.min=0 y.max=0.6
electrode   name=collector     bottom
#Contact Declaration
contact name=gate aluminum con.resistance=1e-3
contact name=emitter con.resistance=1e-3
contact name=collector con.resistance=1e-3
#Doping Declaration
doping     region=2 uniform conc=1.5e14 PHOSPHORUS Y.min=0.7 y.max=99.6
doping     region=2 uniform conc=1.0e20 BORON    y.t=99.6 y.b=100
doping     region=2 uniform conc=1e18 BORON y.min=0.4 y.max=0.7
doping     region=2 uniform conc=2e20 ANTIMONY y.min=0 y.max=0.4 x.max=7
#Model Declaration
mater    region=2 taup0=1e-6 taun0=1e-6
models   analytic  surfmob MOS BIPOLAR  BBT.STD BBT.KL KLA
impact   selb
interface qf=8e11 x.min=-0.02 x.max=0.02 y.min=0.3 y.max=0.8
#Initial Solution
solve    init  outf=init.str
output     e.field val.band con.band impact
save outf=IGBT01.str
tonyplot IGBT01.str
#Numerical Solutions used
method  newton trap maxtraps=8 climit=1e-5
##################################################################################
#Code for various measurements
##################################################################################
```

C. Mask Description

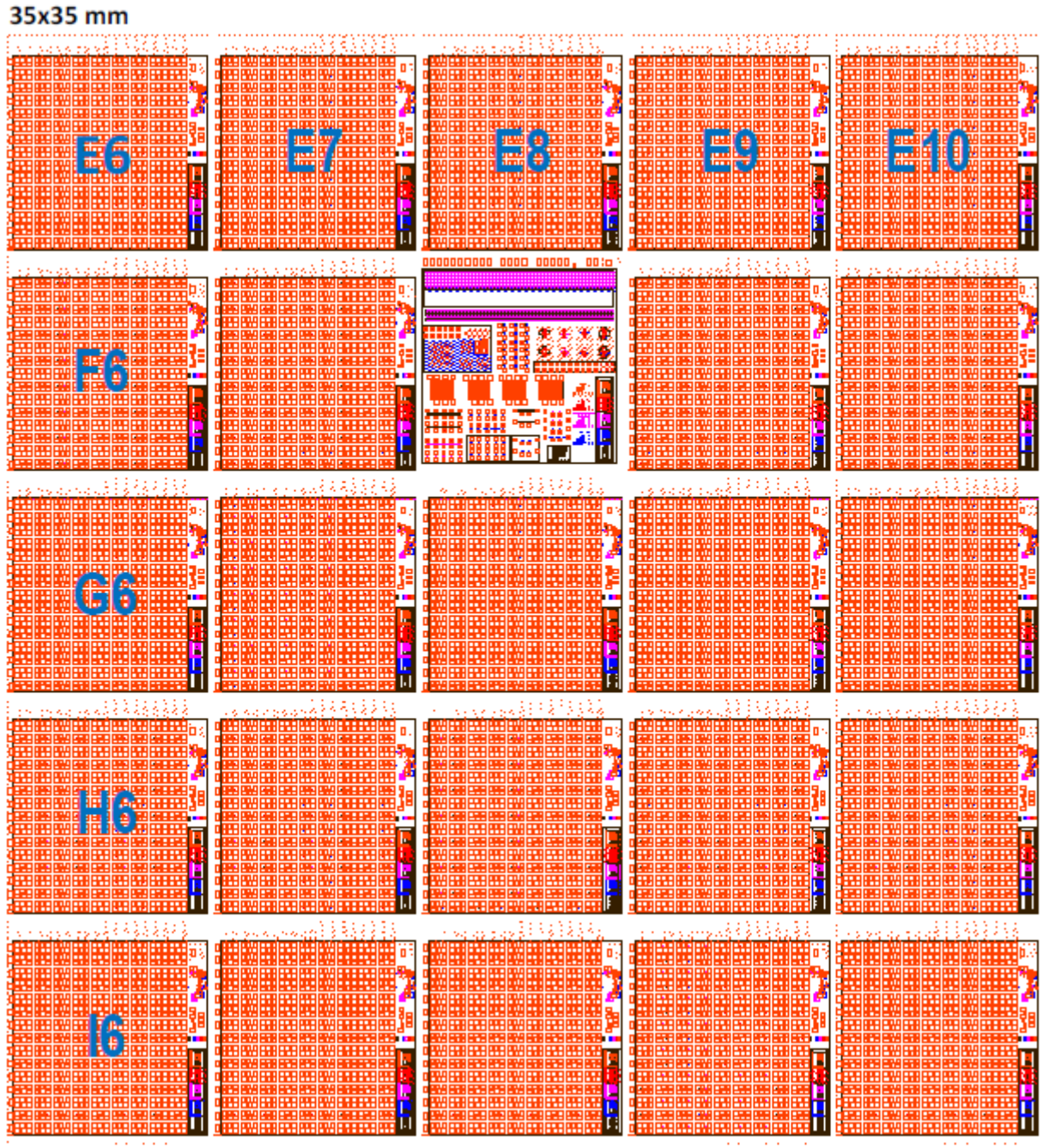

Fig. : Uni BW mask with chip identifiers

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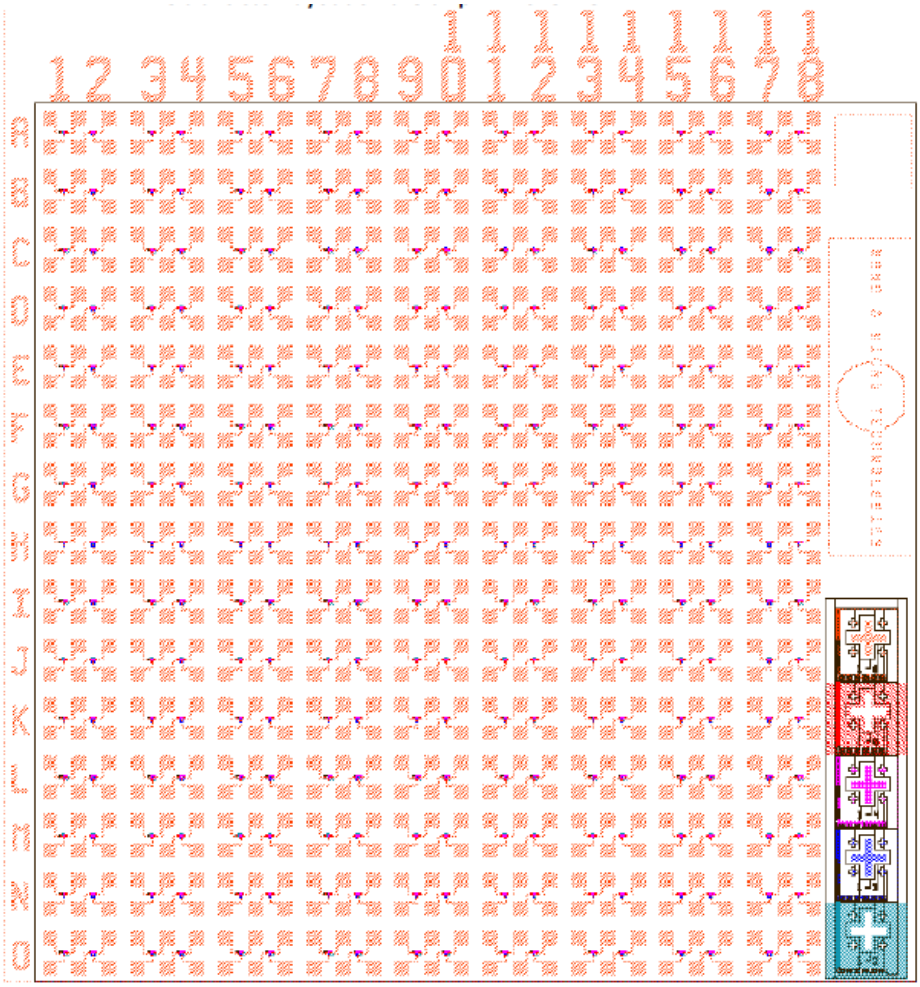

Fig. : 6 X 6 mm² chip with identifier mark, alignment crosses and transistor

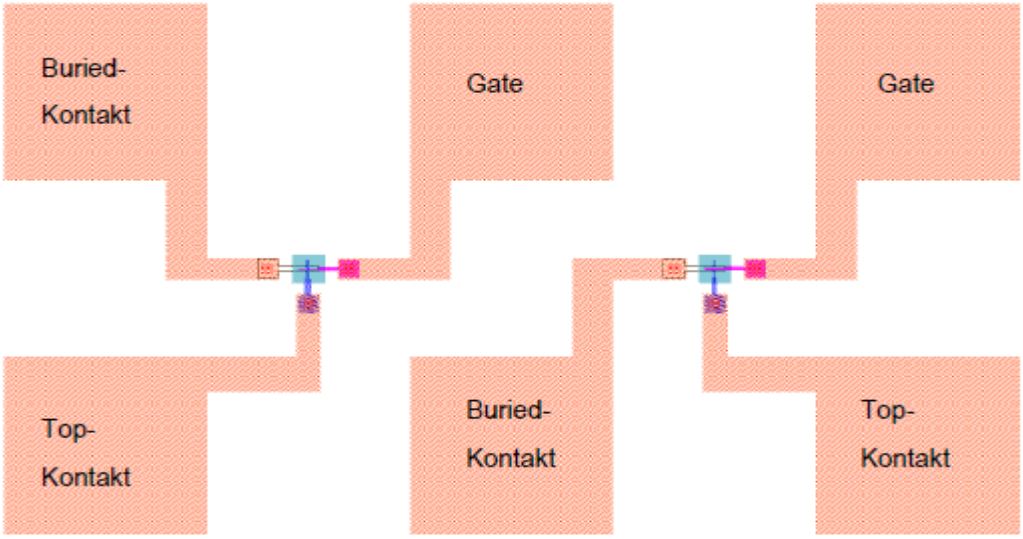

Fig. : Two adjacent transistor

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140
B	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140
C	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140	140
D	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150
E	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150
F	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150
G	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200
H	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200
I	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200
J	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240
K	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240
L	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240	240
M	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300
N	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300
O	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300

Table : Mesa Area (µm²)

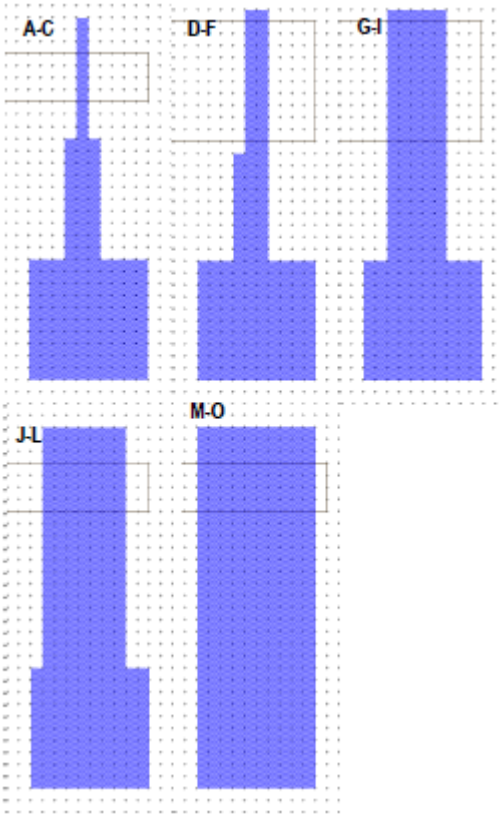

Fig. : Mesa structure of Uni-BW mask

Fig. : Gate structure of Uni-BW mask

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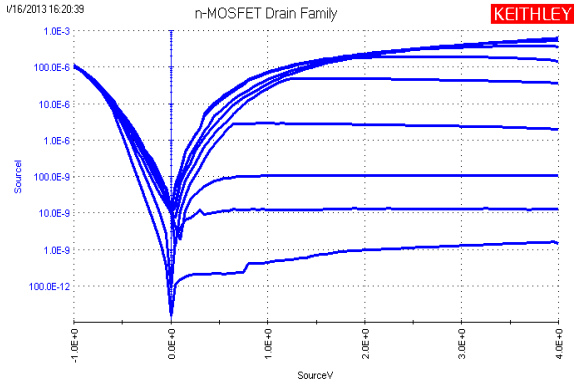
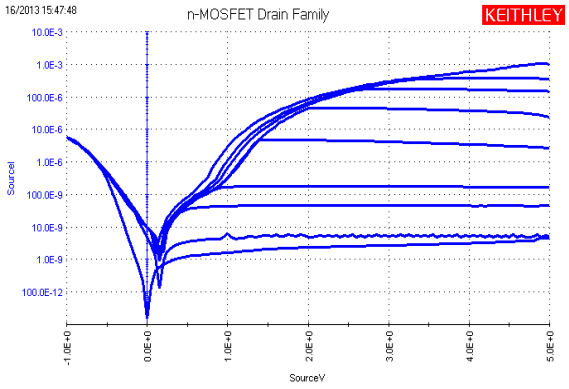
D. Further Electrical Characterization



Device ID: E9 H18



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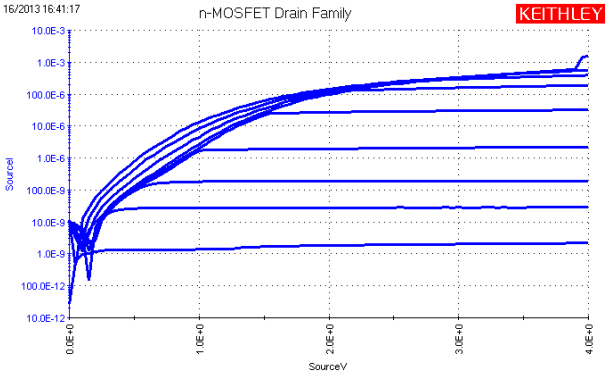

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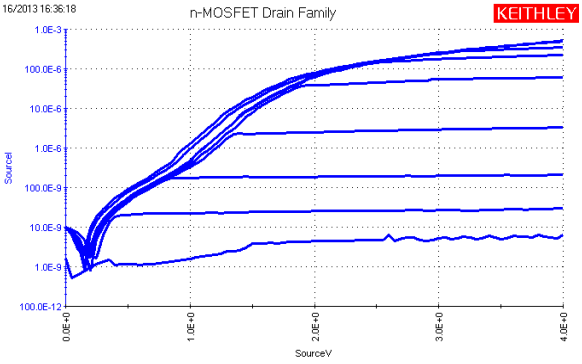
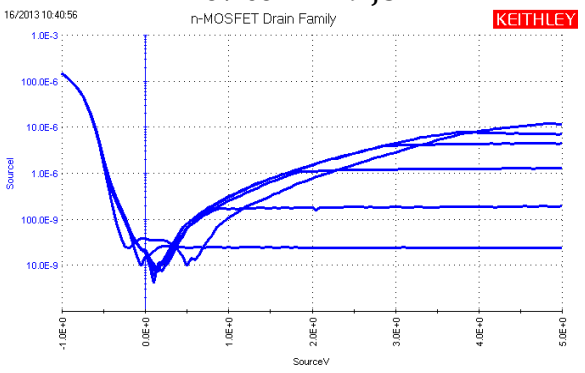
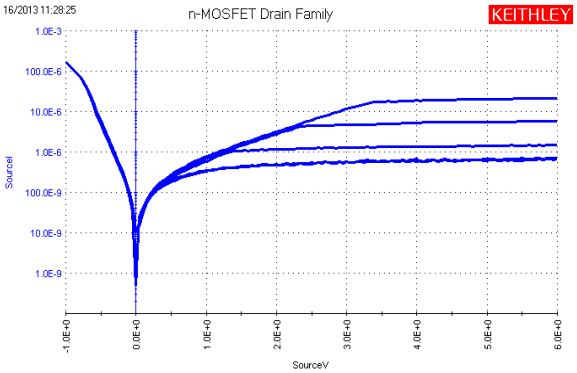


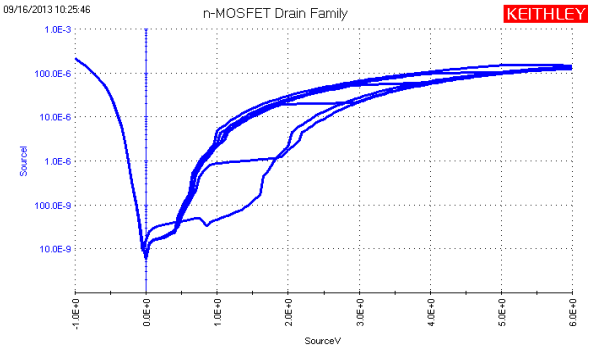
Device ID: E10 M16



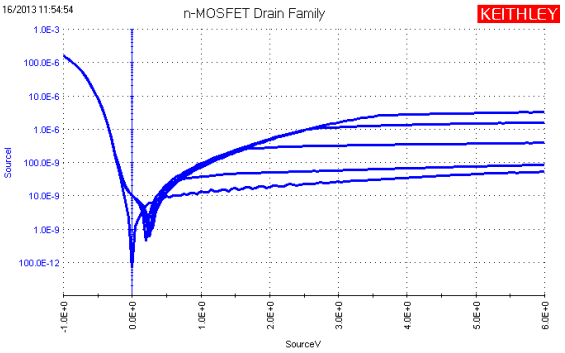
Device ID: I10 E3



Device ID: I10 F3



Device ID: I10 C6



Device ID: I10 G3

E. Declaration

I hereby declare that I have made this work independently and only using the specified literature and resources. Exact sentences or parts of sentences are referenced as a quote and inclination towards any specific concepts taken from other works are adequately referenced. The work has not been submitted to any inspection authority in the same or similar form and is not published.

Stuttgart, 11.November.2013 Signature

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