16 × 16 BIT PARALLEL MULTIPLIER BASED ON 6K GATE ARRAY WITH 0·3 μm AlGaAs/GaAs QUANTUM WELL TRANSISTORS

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The design and performance of a 16 × 16 bit parallel multiplier based on a 6 K gate array will be presented. This LSI semicustom IC demonstrates the high potential of our AlGaAs/GaAs quantum well FETs with a gate length of 0·3 μm. The best multiplication time measured was 7·2 ns.

Introduction: AlGaAs/GaAs heterojunction FETs have proven most successful for application in both digital and analogue integrated circuits operating in the gigahertz range. A promising technology for AlGaAs/GaAs quantum well transistors with double delta doped supply layers [1] and gate lengths down to 0·2 μm [2] was developed for high speed logic [3, 4], analogue circuits [5] and optoelectronic ICs with monolithic integrated MSM photodiodes [6]. To demonstrate the integration complexity, a 16 × 16 bit parallel multiplier based on a 6 K gate array was designed and fabricated successfully.

Fabrication technology: Fig. 1 shows the cross-section of our recessed gate AlGaAs/GaAs double heterojunction depletion

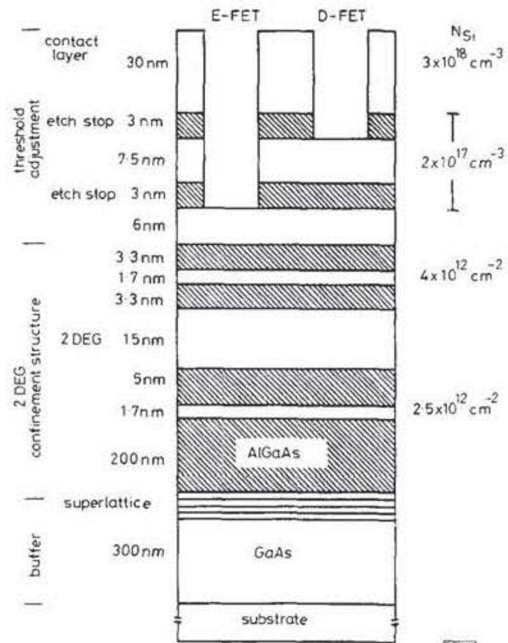

Fig. 1 *Cross-section of heterojunction structure*

and enhancement transistors with double delta doped supply layers. The gate length of 0·3 μm is realised by direct writing electron beam lithography. The metallic connections consisting of gold are fabricated in two layers. The first layer is deposited according to design rules of 2 μm wide lines each separated by 3 μm. The second layer is used to form capacitances and airbridges or to reduce the parasitic sheet resistance of the first metallic interconnections. The contact holes are $3 \times 3\,\mu m^2$. Thin film Ni/Cr resistors can also be integrated.

Gate array architecture: The gate array, which measures $6 \times 6\,mm^2$, consists of 6336 basic cells each with one depletion and two enhancement FETs which can be configured as inverters, 2-, 3- or 4-inputs NORs, and 2- or 3-input NANDs, all constructed in direct coupled FET logic. The gate width is 10 μm for the E-FETs and 5 μm for the D-FETs. The cell size is $48 \times 18\,\mu m^2$. The basic cell layout is shown in Fig. 2. Fig. 3 depicts a micrograph of the gate array. Each of the 66

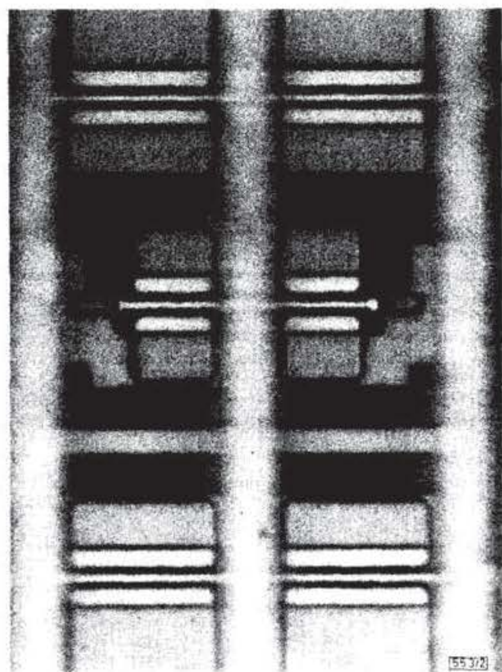

Fig. 2 *Micrograph of two gate array basic cells*

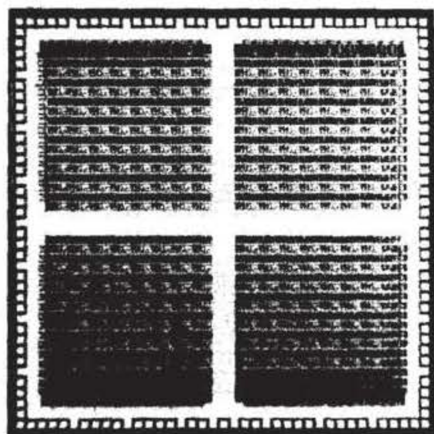

Fig. 3 *Micrograph of gate array*

columns contains 96 cells. The 16 interconnection tracks of the first metallisation are placed between the columns. The second metallisation is used for the power supply and connections to ground within the basic cells, to configure the D- and E-FETs into logic gates as mentioned and for horizontal tracks. The layout of the main power supply and ground connection lines has been optimised to guarantee a maximum deviation of 100 and 50 mV, respectively, over the whole chip. In addition it acts as an on-chip capacitance for the power supply. The left and right sides of the array contain 60 buffers which can be programmed for inputs or outputs. 30 input only and 30 output only buffers are placed on the top and bottom, respectively. The output buffers exhibit a typical measured rise time of 90 ps for 50 Ω loads. The chip has 152 bond pads, 96 for the signals, 30 for the ground and 26 for the power supply.

The 16×16 bit multiplier, which uses 46% of cell array transistors, acts as a test vehicle for the LSI gate array. The well known parallel carry-save-architecture [7] was chosen for circuit simplicity. An additional integrated selftest permits ease of measurement of the maximum multiplication time.

Simulation results: An advanced SPICE model describing the QWT large signal and microwave performance very precisely has been developed previously [8] and implemented. A maximum input frequency of 2·6 GHz was predicted for a 1 : 2 frequency divider based on an edge triggered D-flipflop.

Furthermore, SPICE-calculated values for the delay times of the different logic gates were used as inputs for the timing simulator HILO. Analysing the time critical path in this multiplier, a maximum operation time of ~7 ns was predicted.

Measurements: Measurements gave a typical maximum frequency of 2·7 GHz and a best value of 3·0 GHz for the frequency divider based on our gate array.

Fig. 4 shows the pulse diagram of the most significant bit of the best 16×16 bit multiplier in selftest mode. From the oscillation a maximum multiplication time of 7·2 ns can be derived. The drain bias V_{DD} was 1·5 V, and the power consumption 1·6 W. For V_{DD} values of 0·5 and 2·0 V multiplication times of 7·4 and 7·1 ns, and power consumptions of 248 mW and 2·5 W, respectively, were measured.

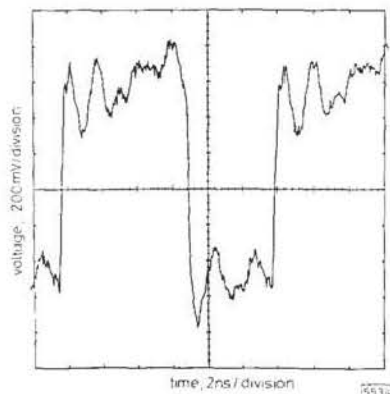

Fig. 4 *Most significant bit (inverted) in selftest mode*

Summary: A 16×16 bit parallel multiplier based on a 6 K gate array with 0·3 μm gate length quantum well transistors was designed and fabricated. A maximum multiplication time of 7·2 ns, and a power consumption of 1·6 W were measured for the best device. These results demonstrate the LSI capability of E/D DCFL ICs manufactured by means of our technology.

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