

10 - 20 Gbit/s GaAs/AlGaAs HEMT ICs for High Speed Data Links

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Abstract

A set of ICs has been developed for the high speed data link at data rates above 10 Gbit/s. A recessed gate process for double pulse doped quantum well transistors has been used with e-beam written 0.3 μm gates. A 4 bit multiplexer and a laser diode driver for the transmitter as well as transimpedance amplifier, bit synchronizer and 4 bit demultiplexer for the receiver have been successfully operated with data rates up to 20 Gbit/s.

Introduction

Fibre optical links with extremely high data rates are required in long haul telecommunication networks, but also within super computers. For applications over short distances, fully integrated GaAs circuits are possible for transmitter and receiver with a wavelength of 0.85 μm . Fig. 1 shows the system block diagram with the components, which have been fabricated at the IAF. A parallel data stream has to be serialized by a 4:1 multiplexer. The serial data-stream is amplified by the laser driver, which also delivers the DC current for the AlGaAs/GaAs laser diode. The optical signal, which is transmitted across the fibre, is received by a MSM-photodiode. The MSM-photodiode is integrated with the transimpedance amplifier. The received optical signal induces a photocurrent, which is the input signal for the bit synchronisation after amplification. The synchronized serial data signal is splitted into four channels by the 1:4 demultiplexer. In this paper, we describe all chips and the measured results except the bit synchronizer, which has already been published [1].

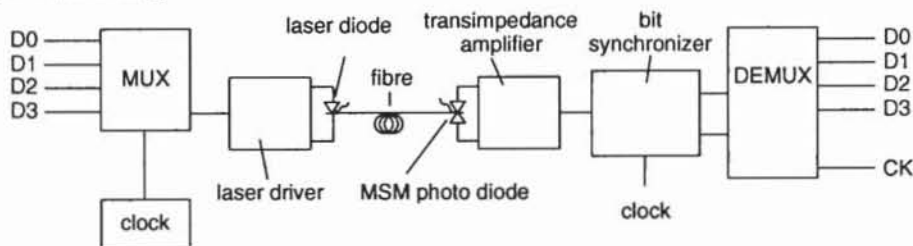


Fig. 1: Block diagram of the high speed optical data link.

Technology

All chips are fabricated using the same recessed-gate process for double pulse-doped quantum well HEMTs [2]. Both, enhancement and depletion type of transistors are realized on the same MBE wafer with AlGaAs etch stop layers and a selective reactive ion etch

process. The gates of the transistors lengths of 0.3 μm and the fingers of the MSM-photodiode are defined by electron beam lithography. The fabrication process includes NiCr resistors, MIM capacitors and two metal layers for device interconnect. The DC- and RF-performance of the FETs is listed in table 1.

	DFET	EFET
f_T	40 GHz	45 GHz
g_m	350 mS/mm	450 mS/mm
I_{dsmax}	350 mA/mm	200 mA/mm

Table 1: Typical transistor parameters.

Circuit Design and Measurements

To reduce power consumption, E/D direct coupled FET logic (DCFL) is used in logic circuits and source coupled FET logic (SCFL) is applied in those functions with highest speed requirements. All circuits have been simulated and optimized using IAFSPICE [3], which enhances SPICE2G6 with an HEMT model.

4:1 MUX

Fig. 2 shows the MUX block diagram. It consists of two stages of 2-bit MUX and timing circuitry. To ensure speed the circuit was designed in source coupled FET logic with differential signal flow. The functional test of the MUX at 6 Gbit/s is shown in Fig. 3. The maximum data rate for a single 2:1 MUX is 20 Gbit/s [4].

Laser Driver

The circuit diagram of the laser driver is shown in Fig. 4. The differential design can easily be linked to the MUX. The DC bias of the laser diode is driven by the transistors EF72, EF82. The high speed signal is sharpened by EF71 and EF81 after preamplification of the input stages EF1...6. Fig. 5 shows the input and output eye diagram of the laser driver at a data rate of 10 Gbit/s, which is

limited by the speed of the pulse pattern generator [5]. To demonstrate the maximum data rate, a 2:1 multiplexer was integrated with a laser driver. The input signals to the multiplexer have been generated by different delay lines from the pulse pattern-generator to the inputs of the MUX. Open eyes have been obtained at the laser driver output at a data rate of 18 Gbit/s, as shown in Fig. 6.

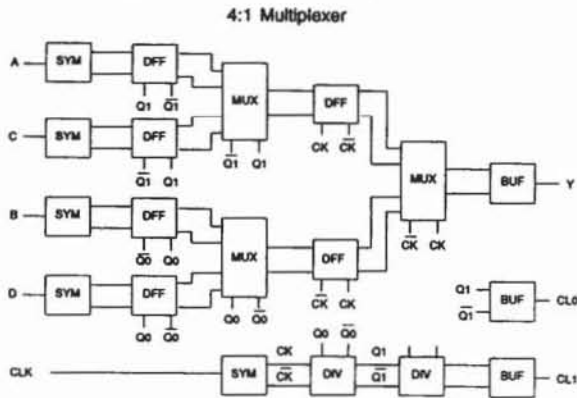


Fig. 2: Block diagram of the 4:1 multiplexer using differential SCFL.

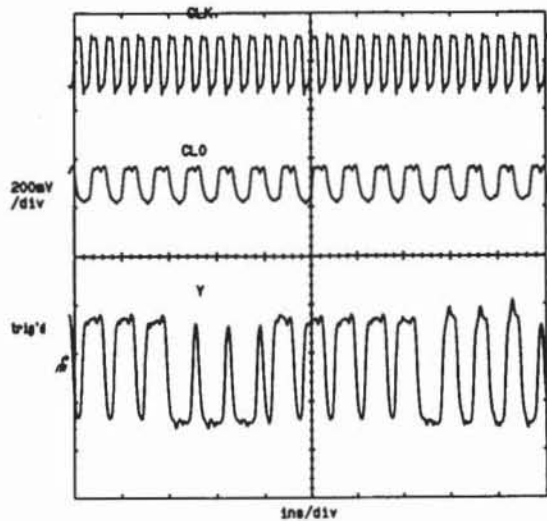


Fig. 3: Timing diagram of the 4:1 multiplexer. Clock, one of four input signals and the multiplexed output signal at 6 Gbit/s showing the functionality.

Transimpedance Amplifier

The circuit diagram of the transimpedance amplifier is shown in Fig. 7. The receiver consists of an MSM photo diode, a transimpedance amplifier, a second-stage amplifier and an output buffer [6]. A 500 Ω feed back resistor is used in the first transimpedance stage. After the next amplifying stage a source follower is used as 50 Ω line driver. The small signal bandwidth exceeds 14 GHz, as shown in Fig. 8. This is to the best of our knowledge, the highest

bandwidth yet reported for a transimpedance amplifier. The sensitivity of the circuit is -15.3 dBm as calculated from the noise spectrum, shown in Fig. 9, and transimpedance data using the theory of R.G. Smith and S.D. Personick [7].

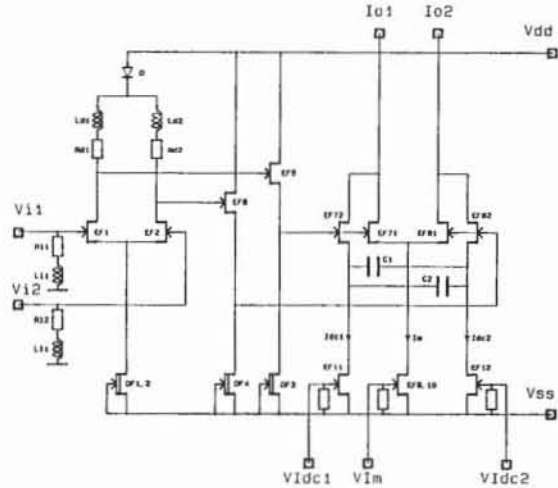


Fig. 4: Circuit diagram of the laser driver.

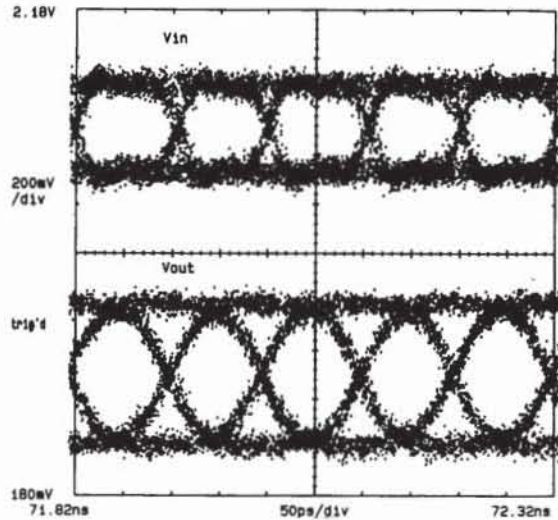


Fig. 5: Eye diagrams of the input signal (top) and output signal (bottom) of the laser driver at 10 Gbit/s.

1:4 Demultiplexer

The block diagram of the 1:4 demultiplexer is shown in Fig. 10. The serial input data is first shifted into 4 pre-register and together with the first bit of the next word transferred to the output registers, while the incoming bit is saved in another preregister. This principle allows maximum data acquisition time at the output and resolves all timing problems in the first register stage [8]. Fig. 11 shows an high speed test at 11 Gbit/s proving full high speed functionality of the chip.

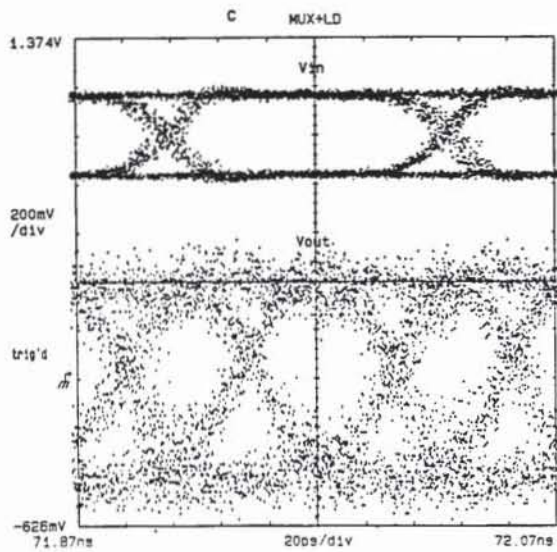


Fig. 6: Input (top) and output (bottom) eye diagrams of an integrated laser driver with 2:1 multiplexer at 18 Gbit/s.

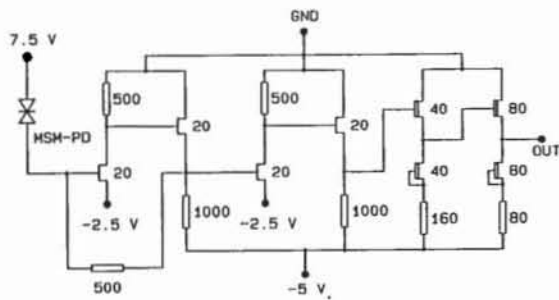


Fig. 7: Circuit diagram of the photo receiver.

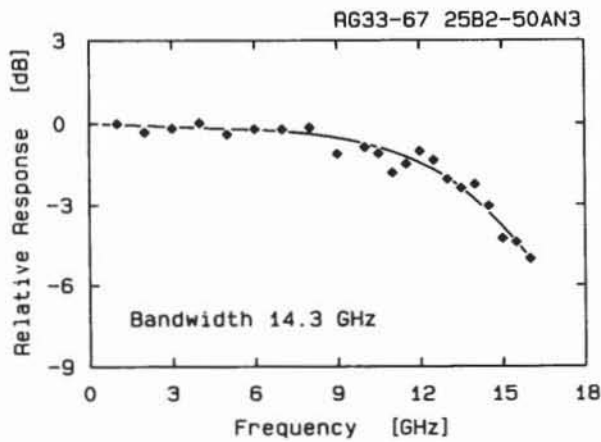


Fig. 8: Measured small-signal bandwidth of the transimpedance amplifier with integrated MSM photo diode.

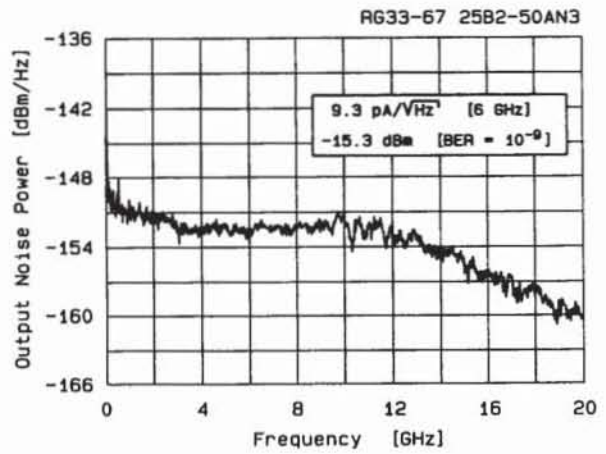


Fig. 9: Measured output noise power spectrum of the photo-receiver.

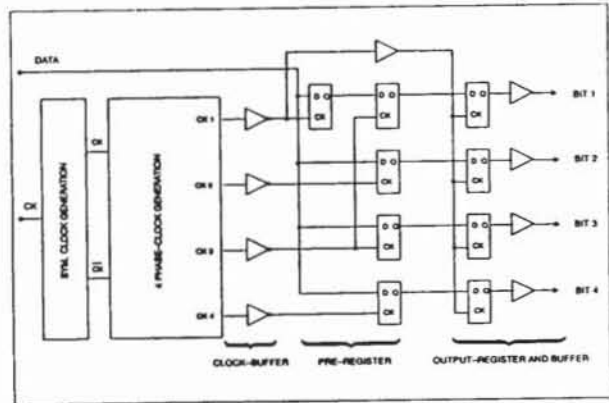


Fig. 10: Block diagram of the 1:4 demultiplexer. The register are using DCFL, while the timing circuitry is applying SCFL.

Conclusion

For the first time, all key components of an optical high speed data link have been fabricated and tested using the same $0.3 \mu\text{m}$ HEMT technology with data rates in excess of 10 and up to 20 Gbit/s. Due to the low power logic and the common technology of the circuits, monolithic integrated transmitter and receiver for optical communication links will be available in the near future.

Acknowledgement

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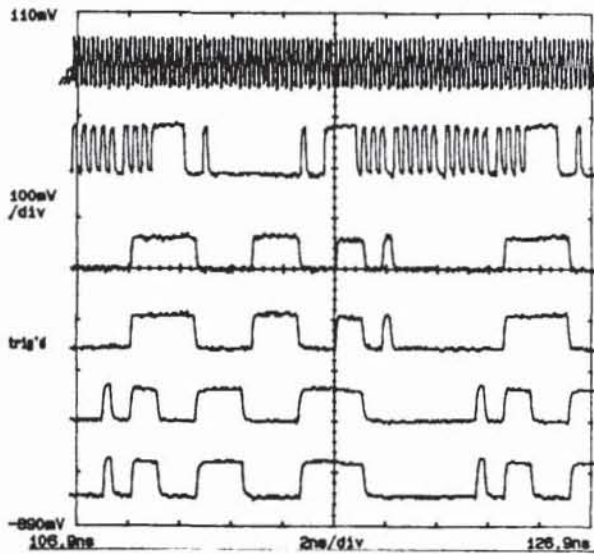


Fig. 11: Timing diagram of 1:4 demultiplexer at 11.6 Gbit/s. The clock signal (top), the serial data input and the four output data signals (bottom) show high speed functionality.

References

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