

20 Gb/s Monolithic Integrated Clock Recovery and Data Decision

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Abstract: An IC for 20 Gb/s clock recovery and data decision was realised using 0.3 μm gate-length QW-HEMTs. A narrow-band regenerative frequency divider with on-chip resonator filters is used for the clock recovery. The parallel processing concept is accepted for the data decision. The complex IC was tested on wafer using 5 and 10-Gb/s input data. The desired 10-GHz clock signal and regenerated data signals have been obtained. The 2x2 mm² IC has a power consumption of about 0.5 W at -3 volt supply voltage.

Introduction: An excellent feature of the digital data communication is that the data signal can be regenerated many times with a very small bit error rate in the repeaters of the transmission channel and in the receiver. The data regeneration includes two operations: the clock recovery (CR) and the data decision (DEC). The relation between the CR and the DEC is so close that they are realised at best monolithically. In this paper we report such a GaAs IC for 20-Gb/s CR and DEC including the functions of frequency dividing and 2:1 demultiplexing.

Block Diagram and Principle: As depicted in Fig. 1, our IC can be partitioned in six blocks. The blocks labelled by Preproc. and NRFD (narrow-band regenerative frequency divider) forms a CR sub-circuit after Wang et al [1,2]. The blocks DEC I and DEC II are for the parallel data decision after Clawin et al [3]. The blocks of Input-Buffer&Branching and the Output-Buffer&Branching are used to make the connections between the CR and the DECs.

The input data at the bitrate of 20 Gb/s will be at first buffered and then flow into three branches: two go to the parallel DEC and one goes to the CR. In the pre-processor the data signal will be processed so that in the output signal a strong spectral line arises from the continuous spectrum at the bit frequency of 20 GHz.

The NRFD is in fact a loop with a positive feedback [1,2]. Under the excitation of the 20-GHz spectral component from the pre-processor and with the narrow-band characteristic of the loop, a sine-form signal having a fundamental frequency of 10 GHz will be generated. That is the recovered clock signal. To make the data decision at a beneficial phase, the CR-subcircuit includes a phase-shifting function. In the block of the Output-Buffer&Branching the recovered clock signal flows also into three branches: one to the clock signal output and two (with anti-phases) to DEC's. Under the timing function of the clock signals, two demultiplexed data signals will be regenerated by the DEC's.

Circuit Techniques: As described above, a signal with a strong spectral line at the bit frequency of 20 GHz should be created by the pre-processor. The pre-processor should have a balanced structure so that it can be directly connected to the NRFD's mixer, which is generally made of a double-balanced multiplying circuit. In addition, it should be easily integrated. Therefore, the modified XOR-circuit, developed by us for the CR with a PLL [4,5], is also very suitable here.

The CR with a passive filter can have a lower jitter, a higher stability and no out-of-lock problem as the CR with a PLL. In the past, however, the CR with a passive filter was exclusively implemented with an IC and an off-chip filter. The main reason lies on two contrary factors: The CR's filter should have a very high Q-factor, e.g. >300 , but the Q-factors of on-chip inductive and capacitive elements for the filter construction are relative low, e.g. <30 . In our IC this problem is solved by using an NRFD including cascaded single-tuned resonators (three stages in the realised IC).

The data decisions were carried out by using three DFF's (delay flip-flops) in each channel: Two build up a traditional DEC-circuit and one for synchronising two output data streams.

Fabrication: The microphotograph of the $2 \times 2 \text{ mm}^2$ IC which includes 356 HEMTs, 64 diodes, 24 resistors, and 10 inductors, is shown in Fig. 2. For the fabrication of the IC the same process as for both ICs in [4,5] was used. The $0.3 \text{ }\mu\text{m}$ gate length QW-HEMTs show a transit frequency f_T of $\sim 50 \text{ GHz}$. The second metal of air-bridge form was used to realise the inductors.

Measurement Results: All 21 chips on a 2-inch wafer were measured on wafer using $50\text{-}\Omega$ coplanar probes, under them 15 chips have a power consumption of less than 0.5 W at -3 V supply voltage and about 1 W at -5 V . The untuned CR sub-circuits have a central frequency of $f_C = 10.22 \text{ GHz}$ with a standard deviation of 66 MHz at -5 V supply voltage. Reducing the voltage from -5 to -3 volt, f_C changes only less than 15 MHz . The tuning range of the central frequency is about 300

MHz. That means that f_c can easily be adjusted to the desired value of about 10 GHz for the 4xSTM-16 data stream of the SDH standards.

Further, 10 chips have both the functioned CR and DEC. Fig. 3 shows the wave forms of the input data, the recovered clock, and the complementary output data streams of DEC I. Fig. 4 shows the eye-diagrams of the input and one output data signal at 10 Gb/s. In these two cases the single-tuned circuit of the pre-processor in the CR sub-circuit was tuned at the fourth and the second harmonic of the bit frequency of the input data stream, respectively. Due to lack of the pattern generator at higher bitrates, further measurements will be carried out later. But simulations and first measurements show, that our circuit can function at bitrates around 20 Gb/s.

Conclusions: An IC for 20 Gb/s clock recovery and data decision were successfully realised and measured. Both the CR and the DEC functions were demonstrated. It is shown that ICs having an ultra-high speed and a lower power consumption can be realised using GaAs HEMT-technologies.

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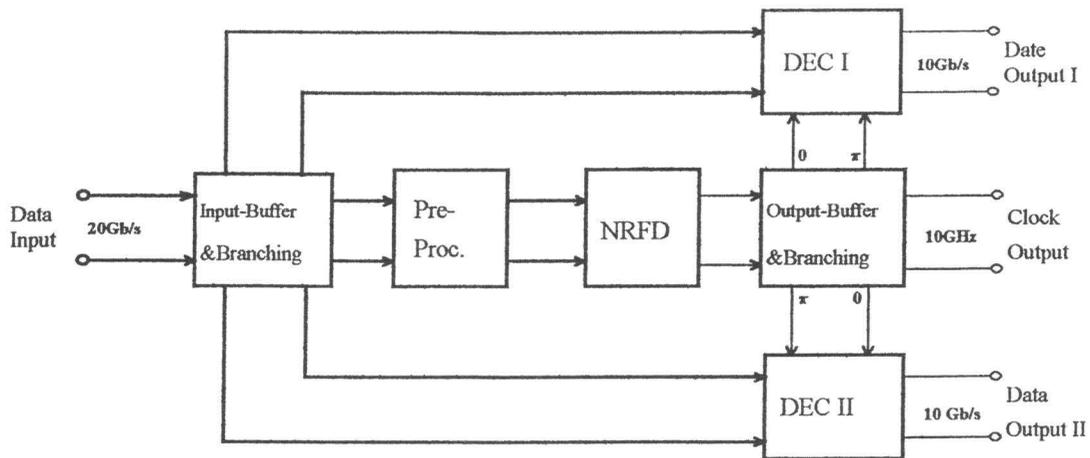


Fig. 1 Blockdiagram of the IC for 20Gb/s clock recovery and data decision.

Fig. 2 Microphotograph of the MIC for 20 Gb/s clock recovery and data decision. (chip area: 2x2 mm²)

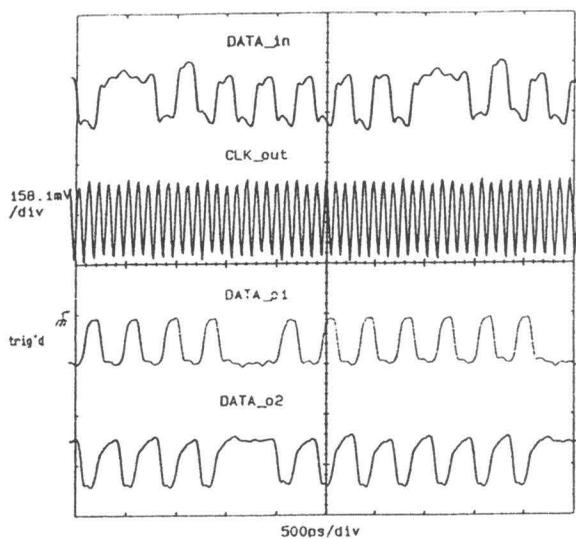
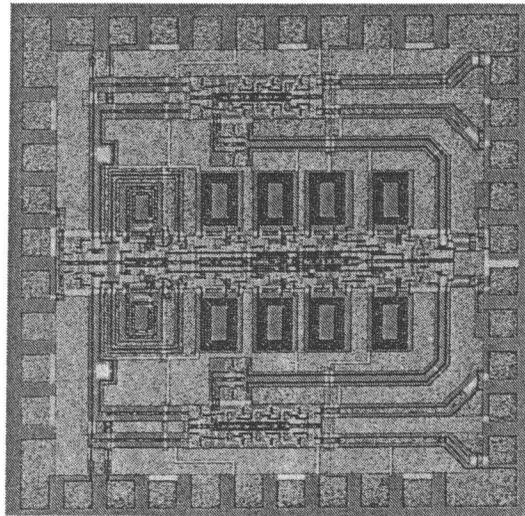


Fig. 3 Wave forms of the 5 Gb/s input Data, the recovered 10 GHz clock, and the complementary output data of DEC I.

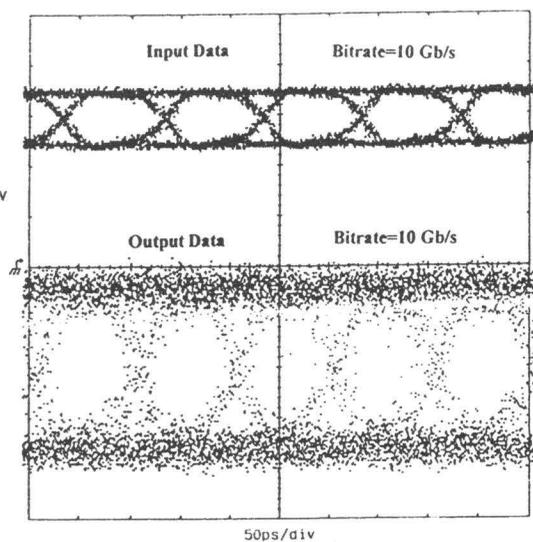


Fig. 4 Eye-diagrams of the input and one output data at 10 Gb/s.