7.5 GB/S Monolithically Integrated Clock Recovery Circuit Using PLL and 0.3-μm Gate Length Quantum Well HEMT's

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***Abstract*— A monolithically integrated clock recovery (CR) circuit making use of the phase-locked loop (PLL) circuit technique and enhancement/depletion AlGaAs/GaAs quantum well-high electron mobility transistors (QW-HEMT's) with gate lengths of $0.3\,\mu$m has been realized. A novel preprocessing circuit was used. In the PLL a fully-balanced varactorless VCO was applied. The VCO has a center oscillating frequency of about 7.7 GHz and a tuning range greater than 500 MHz. A satisfactory clock signal has been obtained at a bit rate of about 7.5 Gb/s. The power consumption is less than 200 mW at a supply voltage of -5 V.**

I. Introduction

At our institute a set of IC's has been developed for high-speed optical transmission systems at bit rates between 10 and 20 Gb/s [1]. An IC for CR at these high-bit rates was lacking yet. In fact, the IC realization of CR is generally accepted as the weak link of high-speed system integration [2]. Though several fundamental subcircuits at rates greater than 6 Gb/s have emerged [2], [3], the rates of the realized IC's for a full CR function are limited to 4 Gb/s, both for the CR category with a surface-acoustic-wave (SAW) filter [4], and with a PLL [5]. This paper describes a monolithic IC for the CR with a PLL at a rate of 7.5 Gb/s.

II. Circuit Principle

The block diagram of the CR circuit with a PLL is shown in Fig. 1. In the preprocessor block, the input data signal, assumed to have an NRZ (non-return-to-zero) format, is processed such that the signal v_i', which has a strong spectral line among its continuous spectrum, is generated. The phase of v_i' is then compared in the phase detector (PD) with that of the oscillating signal v_0' from the VCO. By this way the phase difference signal v_p is obtained. After filtering, the voltage controlling signal v_{co} of the VCO is formed. Using this signal, the phase of v_0 will then follow that of v_i.

For the preprocessor two typical circuits are generally used: (a) a differentiating circuit followed by a full-wave rectifier and, (b) one (for the single-ended input) or two (for the differential input) delay lines with a length of $T_b/2$, i.e., a half-bit period, combined with an XOR logic circuit. The former can easily be integrated. The disadvantage is that its output is single-ended, which is not favorable for the interconnection with a commonly used double-balanced PD. Using two delay lines, the latter can have a fully balanced structure. However, the integration of these $T_b/2$ long delay lines is usually impractical. In addition, both circuits can only generate a signal of an RZ (return-to-zero)-like waveform. Such a signal has a steadily falling spectral curve around the bit frequency f_b [6], [7]. This means that both circuits themselves do not function as an ideal preprocessor [7]. For this reason an improved circuit, as shown in Fig. 2 in [8], has been developed. That circuit can be considered as a combination of two typical preprocessing circuits because the normal differential current amplifier of the lower level of the XOR is replaced by the differentiating circuit of the first type of preprocessor. In this combination, a peaked, unipolar current pulse will be generated at each level transition of the input data signal. The other important improvement of our preprocessor is that, instead of two resistors, a single-tuned LC resonator including on-chip inductors is used as the loading circuit of the XOR. The improvement results in three advantages for the preprocessor as well for the whole CR circuit:

1) The gain of the preprocessor is greatly increased.
2) The LC resonator shows a filtering function. A sine wave output signal form can be obtained. The spectrum of such a signal is much purer and is favorable for further processing. Thus the performance of the CR system can be improved.
3) An output signal whose spectrum is symmetrical to the bit frequency f_b can be obtained. Thus, an optimal CR system can be constructed.

Since our preprocessor is fully-balanced and includes no delay lines, it is suitable for monolithic integration in the system.

As the main processing part of a CR circuit, a PLL is a suitable substitution for the passive filter followed by a limiting amplifier. In our PLL, the double-balanced multiplier circuit with a capacitively-coupled current amplifier shown by Fig. 11 in [4] was adopted for the PD by replacing the bipolar transistors with HEMT's. With this circuit the influence of the dc components of both input signals can be completely eliminated.

For the LF, the typical lead-lag active low-pass was utilized. To adjust the LF performance and to maintain the balanced performance on the input side of the OPAM (operation amplifier), four off-chip devices, i.e., C_1, C_2, R_{21}, and R_{22} are

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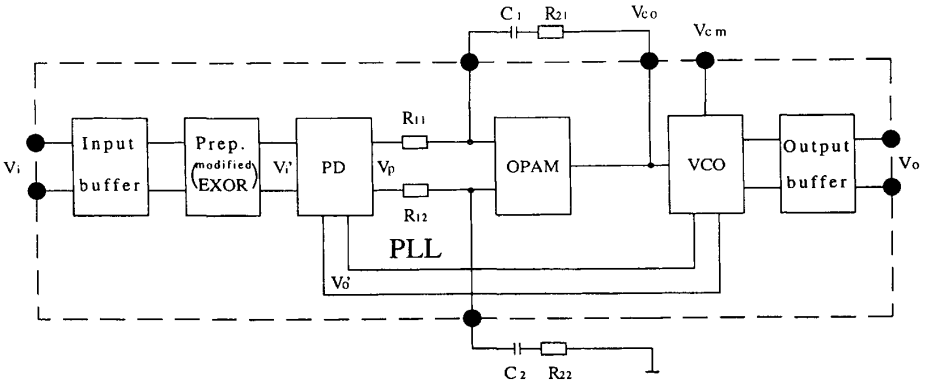

Fig. 1. Block diagram of the monolithically integrated 7.5 Gb/s clock recovery IC.

scheduled. The OPAM consists of three stage differential amplifiers. To increase the gain, depletion HEMT's are used as active loads in the first two stages.

Among the sub-circuits of a PLL, the VCO is the crucial one. The performances of a PLL are essentially determined by that of the VCO. In our PLL, a fully-balanced varactorless VCO has been developed on the basis of the circuit in [9]. As described there, two capacitively-coupled Darlington pairs were used for the active unit, and the gate-drain junctions of the input transistors of the Darlington pairs were used as varactors. Two decisive improvements are: 1) two on-chip inductors instead of one off-chip 1/4 λ transmission line stub are used for oscillation; and 2) a fully-balanced structure is used. Since in this VCO there are less uncertain parameters than other VCO's that need one or more off-chip frequency stabilizing elements, very high center frequencies can be obtained with small deviations. Because of the fully-balanced structure, all common-mode interferences caused by temperature, supply voltage, and all other interferring signal sources can be suppressed effectively, and therefore, a much lower noise level can be obtained. Moreover, the VCO can be directly connected back to the PD and is very favorable for the integrated realization of the whole system.

III. Fabrication

The microphotograph of the IC which includes about 150 HEMT's, 20 resistors, 4 inductors, and 6 capacitors, is shown in Fig. 2. The chip area is $1.5 \times 1.0\,\mathrm{mm}^2$.

The same standard process as for all IC's in [1] was used for the fabrication of our CR chip. A double-pulse-doped quantum well HEMT structure was fabricated by molecular beam epitaxy. Both enhancement and depletion mode HEMT's were incorporated on the same chip. 0.3-μm gates were patterned by electron beam direct writing. The gate recesses were obtained by reactive ion etching. The transit frequency f_T of typical enhancement HEMT's is 50 GHz. Precision resistors were made using nickel-chromium thin films. The capacitors were formed by the metal-isolator-mtal structure, and the inductors were constructed using the second metal of the airbridge form. A detailed description of the process can be found, for example, in [10].

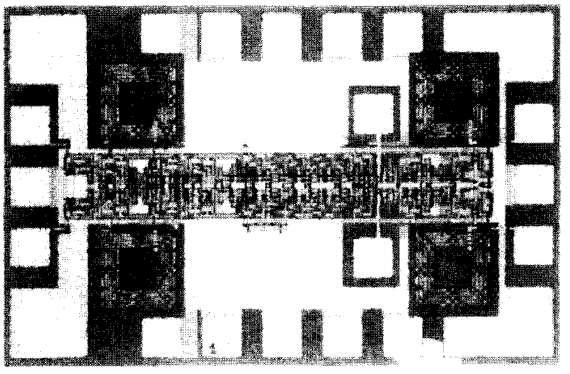

Fig. 2. Microphotograph of the CR chip.

IV. Measured Results

About 16 chips distributed over one 2-in wafer were measured on wafer using 50-Ω coplanar test probes. The power consumption of the chip is less than 200 mW at a supply voltage of -5 V. The VCO's have a center frequency of 7.7 GHz with a standard deviation of 60 MHz. The spectral line width of a free-running VCO is less than 500 kHz. The ratio of the center frequency to the spectral linewidth is about 16,000. The phase noise estimated from the spectrum is about -88 dBc/Hz at 1 MHz offset. Taking into account the fact that the $1/f$ noise of the GaAs FET's is 20–30 dB greater than that of the bipolar transistors [11], the obtained values from the free-running VCO can be considered as in good order. The total control range is more than 500 MHz. This is wide enough to compensate the deviation of the center frequency caused by variations of process, temperature, supply voltage, etc. In the phase-locked case the -3 dB spectral linewidth was immediately reduced to the level of the input signal, namely, about 15 kHz.

Fig. 3 shows on-wafer measured waveforms of the input PRBS (pseudo-random bit sequence) with a length of $2^{10} - 1$

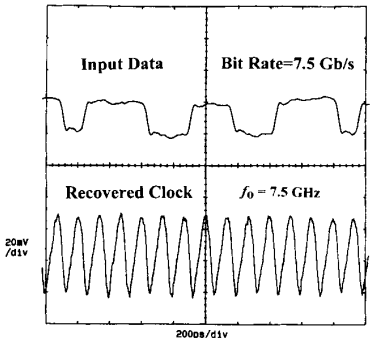

Fig. 3. Input (upper) and output (lower) signal wave forms of the 7.5 Gb/s CR.

at a bit rate of about 7.5 Gb/s (upper) and the recovered clock signal (lower) from one of the CR chips. The rms time jitter is about 2 ps.

It should be pointed out that the desired bit rate of this IC is 10 Gb/s. The measured value of 7.5 Gb/s is determined mainly by the on-chip inductors of the VCO.

V. Conclusion

We have designed, fabricated, and tested a clock recovery IC using the PLL technique and AlGaAs/GaAs QW-HEMT's. An operating bit rate as high as 7.5 Gb/s was demonstrated. The power consumption is less than 200 mW. With slight parameter modifications our CR circuit can be implemented in the future SDH/SONET system at the bit rate of about 10 Gb/s, i.e., 4 × STM-16 or STS-192, and using the same circuit concept, a clock recovery at around 20 Gb/s is realizable.

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