15 Gbit/s INTEGRATED LASER DIODE DRIVER USING 0·3 μm GATE LENGTH QUANTUM WELL TRANSISTORS

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An integrated laser diode driver was realised using enhancement/depletion 0.3 μm recessed-gate AlGaAs/GaAs quantum well transistors. Fully-open eye diagrams were observed at bit rates up to 10 Gbit/s with 50 Ω loads. The maximum DC and modulation current were 25 and 45 mA, respectively. The power consumption is less than 450 mW.

Introduction: A 20 Gbit/s 2 : 1 multiplexer (MUX) using GaAs/AlGaAs quantum well transistors [1] and a 15 GHz GaAs/AlGaAs multiquantum well laser diode (LD) [2] have been developed. The laser diode driver (LDD) presented here was scheduled for linking the MUX and the LD so that a very high-speed transmitter for optical digital communication systems could be realised. Furthermore, it ranks with the few LDDs that can operate at bit rates above 10 Gbit/s [3–5].

Circuit design: The design of a high-speed LDD is challenging because the requirements, such as large output current and high speed, are contradictory. For large currents, normally in the range of some tens of milliamps up to 100 mA, large dimensioned output transistors and large driving signals are necessary. Both are unfavourable for high speed. In addition, the large-signal transients of an LD, particularly the fall time at turn off, impose limitations on the maximum achievable modulation bit rate [6]. In our design an RF current compensation technique aimed at reducing the fall time of the LDD itself and of the driven LD was introduced.

The circuit diagram of our LDD is shown in Fig. 1. It consists of three stages: the preamplifier, the source follower, and the output. Both enhancement and depletion mode double delta-doped quantum well AlGaAs/GaAs/AlGaAs high electron mobility transistors (QW-HEMTs) [7] were used as active devices. At the input terminals lossy matching was used. In the preamplifier an RF voltage compensation was introduced by the inductors Ld1 and Ld2. The diode D here was used for level shifting. The enhancement HEMTs (E-HEMTs) EF71, EF81, EF9 and EF10 in the output stage form a normal current amplifier. The current amplifier offers the basic modulation current for the driven LD. The E-HEMTs EF72, EF82, EF11, and EF12 and the capacitors C1 and C2 form a capacitively coupled current amplifier (C^3A). This was used mainly to produce a drive signal with sharp undershoots, as proposed in Reference 8, so that the turn-off delay and the fall time of the LD could be reduced; this is realised through dynamic reduction of the biasing current I_{dc2} of EF82 (for I_{o2} as the output to the LD). I_{dc2} acts also as the DC of the LD. I_{dc1} can, accordingly, be selected to be much smaller than I_{dc1}, so that the power consumption, the rise time and, further, the chirping effect of the LD are not greatly affected.

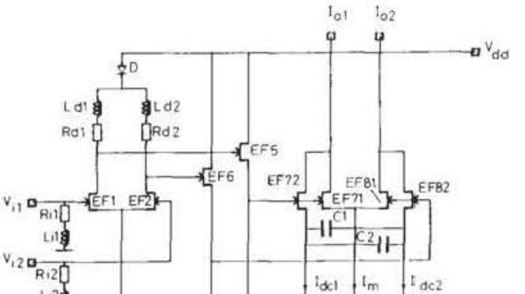

Fig. 1 *Circuit diagram of laser diode driver with C^3A*

Simulation results: The waveforms of the LDDs with and without the C^3A are shown in Fig. 2, obtained through a SPICE simulation using an in-house adopted HEMT model. The sharp undershoot caused by the C^3A can be clearly seen.

The dynamic characteristic of the LDD was simulated for two loading cases. In the first case the output I_{o2} is linked to V_{dd} across a modelled LD, and I_{o1} is directly linked to V_{dd}. This case corresponds to loading with an on-chip LD. In this case both the simulated rise and fall time of the output current pulse are equal to 21 ps, and the maximum attainable bit rate is over 20 Gbit/s. In the second case the output I_{o2}, and I_{o1}, are linked to V_{dd} across a 50 Ω resistor, which corresponds to the situation in a 50 Ω measuring setup. In this case the rise and fall time increase to about 30 and 40 ps, respectively. This predicts that a maximum bit rate of about 12 Gbit/s should be obtained from a 50 Ω test setup.

Fabrication: The photomicrograph of the $1 \times 1\,mm^2$ chip is shown in Fig. 3. As active devices, the QW-HEMTs were fabricated by molecular beam epitaxy (MBE). Both enhancement and depletion mode HEMTs were processed on the same wafer using reactive ion etching (RIE) for the gate recess. Gates 0·3 μm long were obtained by electron beam direct write [7, 9]. The E-HEMTs typically exhibit a maximum transconductance of 500 mS/mm, a maximum drain current of more than 180 mA/mm and a transit frequency of about 45 GHz.

Measurement results: The chip was measured on-wafer using 50 Ω coplanar test probes. The maximum DC and modulation output current were equal to 25 and 45 mA, respectively. In this case, the total DC and power consumption are less than 90 mA and 450 mW, respectively. A fully-open eye diagram (Fig. 4) was obtained at 10 Gbit/s using a Tektronix 11801A digitalscope. The NRZ test signal was supplied by an Anritsu 10 Gbit/s pulse pattern generator. Furthermore, the chip was measured using a sinewave generator. The large-signal bandwidth is about 5·6 GHz. That indicates that the LDD should show an open eye diagram at bit rates above 11 Gbit/s. The value is very close to the simulated value of about 12 Gbit/s. Thus, we deduce that the LDD can be operated at bit rates above 15 Gbit/s for an on-chip LD.

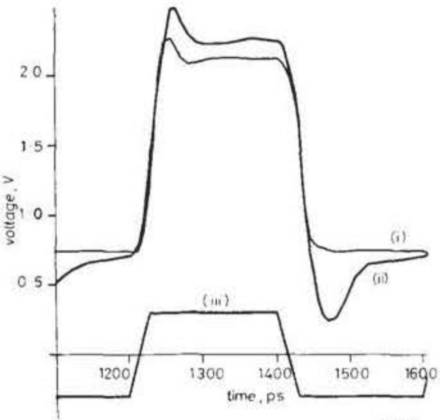

Fig. 2 *Simulated wave forms of LDDs with and without C^3A*

(i) output signal, without C^3A
(ii) output signal, with C^3A
(iii) input signal

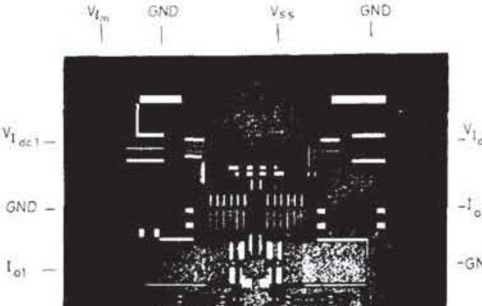

Fig. 3 *Photomicrograph of LDD chip*

Conclusion: We have designed, fabricated and tested a laser driver IC using AlGaAs/GaAs quantum well transistors. It uses a capacitively-coupled current amplifier to reduce the turn-off delay and the fall time of the driven laser diode. Fully-open eye diagrams were observed at bit rates up to 10 Gbit/s. The maximum DC and modulation current was 25 and 45 mA, respectively. The IC can be used in an optical digital transmitter to drive a laser diode at a bit rate above 10 Gbit/s.

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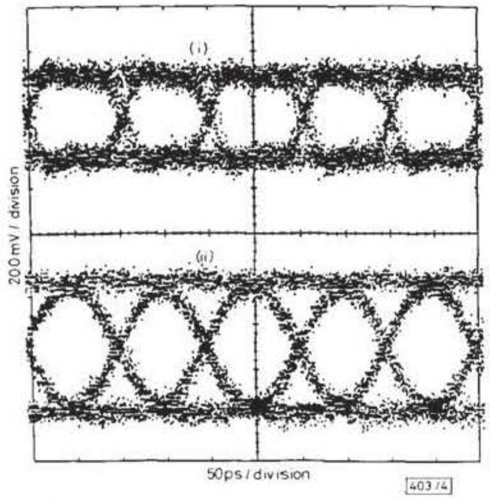

Fig. 4 *Eye diagram of input and output signals at 10 Gbit/s from 50 Ω measuring setup*

(i) V_{in}
(ii) V_{out}

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