Special Brief Paper

An 18–34-GHz Dynamic Frequency Divider Based on 0.2-μm AlGaAs/GaAs/AlGaAs Quantum-Well Transistors

Andreas Thiede, Manfred Berroth, *Member, IEEE*, Ulrich Nowotny, Jörg Seibel, Roland Bosch, Klaus Köhler, Brian Raynor, and Joachim Schneider

I. Introduction

DIGITAL frequency dividers are of increasing importance in a wide field of device applications for high-speed communication systems and high-end measuring equipment. Ever-increasing frequency limits have led to the demand for GaAs approaches.

Dynamic frequency dividers based on 0.2-μm GaAs MESFET's have achieved a 26.5-GHz operational frequency [1]. Operation also at 26.5 GHz was reported based on 0.25-μm inverted AlGaAs HEMT technology [2], [3]. High-speed ECL static frequency dividers using Si bipolar transistors, AlGaAs/GaAs hetero bipolar transistors, and AlInAs/InGaAs HBT's have achieved operation at 25 GHz, 34.8 GHz, and 39.5 GHz, respectively [4]–[6].

A promising technology for AlGaAs/GaAs/AlGaAs quantum-well transistors with double-delta doped supply layers [7] and gate lengths down to 0.2 μm [8] was developed at our institute, for high-speed logic [9], [10], analog circuits [11], and optoelectronic IC's [12]. An integration complexity of 20 000 transistors was demonstrated [13]. The design and performance of a dynamic frequency divider operating in the 18–34 GHz range will be presented here.

II. E/D-AlGaAs/GaAs/AlGaAs Quantum-Well Transistor Process

Fig. 1 shows a cross section of our recessed gate AlGaAs/GaAs/AlGaAs double-heterojunction depletion and enhancement type transistors with double delta doped supply layers. The narrow bandgap GaAs channel forms a quantum well between the wide-gap AlGaAs layers. The AlGaAs spacers are optimized for high electron transfer from the supply layers into the channel, and on the other hand for reduced Coulomb scattering by spatial separation of the electrons in the channel and donors in the supply layers.

AlGaAs etch stops are used for both the enhancement and depletion type transistors. The GaAs is removed by a dry etch process; the AlGaAs etch stops, however, are removed by conventional wet etching.

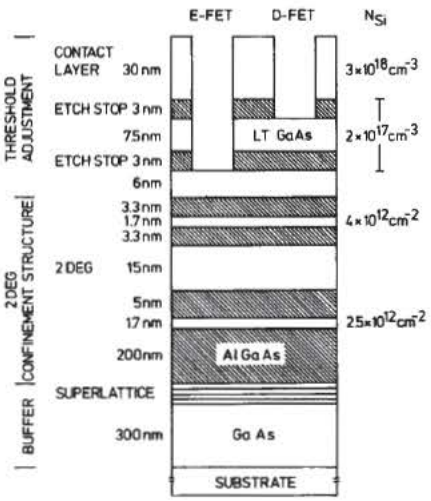

Fig. 1. Cross section of the AlGaAs/GaAs/AlGaAs heterojunction structure.

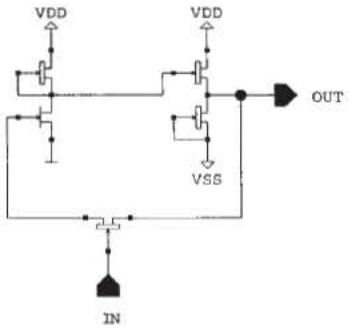

Fig. 2. Dynamic frequency divider circuit schematic.

This structure offers three advantages over standard MESFET's:

- large carrier density in the channel, typically 1.8×10^{12} cm^{-2}, and a high electron mobility of about 7000 cm^2/Vs;
- high differential drain resistance of about 50 kΩ μm, and transconductance of about 400 mS/mm due to electron confinement in the channel; and

Manuscript received May 18, 1993; revised August 10, 1993. This work was supported by the German Federal Ministry of Research and Technology under DFE Project TK357/8.

The authors are with the Fraunhofer Institute for Applied Solid-State Physics, D-79108 Freiburg, Germany.

IEEE Log Number 9212553.

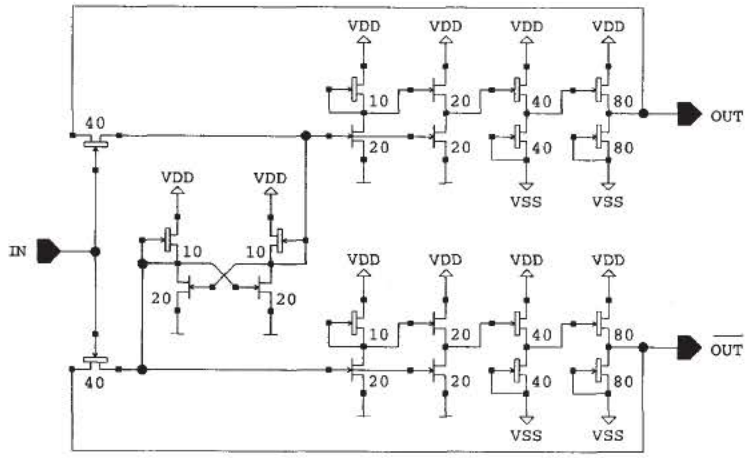

Fig. 3. Circuit schematic of the dynamic frequency divider with a memory type flip-flop.

TABLE I
QUANTUM-WELL TRANSISTOR PARAMETERS FOR 0.2-μM GATE LENGTH

Type	g_m	f_T	f_{max}
E	> 500 mS/mm	> 70 GHz	> 100 GHz
D	> 350 mS/mm	> 55 GHz	> 100 GHz

- precise control of threshold voltage (10 mV standard deviation across a 2-in wafer).

We have developed a mix-and-match technology combining an e-beam with optical lithography whereby the e-beam is used for writing the gates only.

Table I gives an overview of the transconductance g_m, the transient frequency f_T, and the maximum frequency f_{max} of our enhancement and depletion type transistors for a gate length of 0.2 μm. Our standard process sequence includes Schottky diodes, NiCr thin-film resistors, and MIM capacitors. For optoelectronic circuits, MSM photodiodes can be monolithically integrated [12]. Two gold layers are used for interconnections, the top layer using an airbridge technique, thus reducing parasitic capacitances.

III. Circuit Design

The maximum input frequency to a static divider is restricted to about

$$f_{togg} = 1/2t_{pd}$$

where t_{pd} is the delay time of the logic inverter. Dynamic frequency dividers generally can operate up to twice the input frequency of static dividers:

$$f_{togg} = 1/t_{pd}.$$

The simplest realization of a dynamic frequency divider is shown in Fig. 2. A single inverter and a buffer stage are connected in series, and the output of the buffer is fed back to the inverter input by a transfer gate. The inverter is switched with half the frequency of the transfer gate. The time at which the transfer gate is switched on due to the high level applied to the input is no longer than the delay of the inverter buffer chain, and that delay in turn will be shorter than one input pulse period. These equations give the upper and lower limits of stable operation of the divider circuit

$$(2t_{INV} + 2t_{SF})^{-1} < f < (t_{INV} + t_{SF})^{-1}$$

where t_{INV} and t_{SF} are the propagation delays of the inverter and the source follower, respectively.

During the time when the transfer gate is switched off, the logic state is stored only in the capacitance of the high-ohmic inverter input node. For higher frequencies, however, especially for very short rise and fall times, the gate capacitance of the transfer gate can cause a loss of data. Data storage in a memory type flip-flop as presented in [2] and [3] is more reliable. Fig. 3 depicts the circuit schematic. The memory type flip-flop comprises two ED–DCFL inverters. These DCFL inverters never will reach 30 GHz operation, but in this case the outputs are directly driven. Thus the gate widths of the flip-flop transistors should be small in comparison to the driving buffers. To switch the flip-flop symmetrically two ring oscillators were used, each consisting of one SBFL inverter and two source followers. The push–pull stages of the SBFL inverters guarantee low output inpedance and a high voltage swing.

Because of finite rise and fall times, an appropriate delay in the inverter output signals is very important for stable operation of the divider. Therefore a second source follower was used in the ring oscillator chain.

The gate widths of the transfer transistors are a trade-off between a high on-conductance and a low capacitive load for the driving source follower.

The circuit design was optimized by SPICE simulation on the basis of an in-house developed HEMT network model presented earlier [14]. All transistors have gate lengths of 0.2 μm; the optimized values for the gate width are shown in the figure.

For higher frequencies 1/3 and 1/4 division can be expected, but the appropriate bandwidth for stable operation declines.

IV. Results

Fig. 4 is a micrograph of the divider circuit. The chip size excluding buffers is approximately 150 μm × 200 μm. The

Fig. 4. Micrograph of the divider circuit.

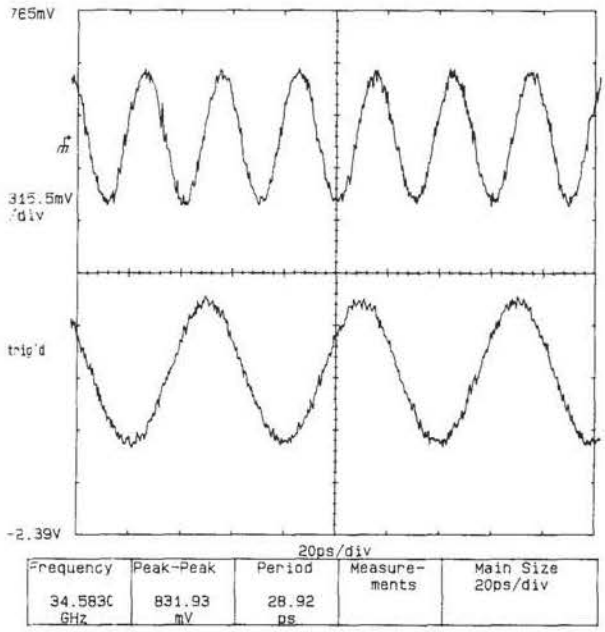

Fig. 5. Measured pulse diagram of a 34-GHz input and the 17-GHz output of the dynamic frequency divider.

input is applied to the bond pads using a coplanar line and on chip terminated to match 50 Ω.

Measurements carried out on the digital dynamic frequency divider show a lower limit for stable operation of 18 GHz. A value of 34 GHz for the maximum input frequency was obtained. Fig. 5 shows the pulse diagram of the 34-GHz input and the 17-GHz output. As far as we know this is the best result ever reported for HEMT circuits, and similar to the frequency limit shown by use of AlGaAs/GaAs HBT's.

Between 36 GHz and the 40-GHz limit of the test equipment, an operation modulus of 1/3 division could be shown. The divider can operate with single-phase input. The input voltage swing is about 1 V at 18 GHz and decreases as the frequency increases.

Both single-phase and differential outputs are possible. The circuit runs at a power supply of $V_{DD} = 2$ V and $V_{SS} = -2$ V. A power consumption as low as about 250 mW was obtained for the divider without buffers.

A fully functional yield greater than 50% was obtained.

V. Summary

The design and performance of a dynamic frequency divider was presented. This digital IC demonstrates the ability of our AlGaAs/GaAs/AlGaAs quantum-well FET's with gate lengths of 0.2 μm. Stable operation was achieved in the frequency range from 18 GHz up to 34 GHz with a power consumption of 250 mW. As far as we know, this is the best result ever reported for HEMT circuits, and it is similar to the frequency limit achieved by use of AlGaAs/GaAs HBT's.

Acknowledgment

The authors are grateful to the entire staff of the laboratory. They especially want to thank H. S. Rupprecht for his directing and continuous encouragement and T. Jakobus for his expert technology management.

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