Ultra-low-noise readout circuits for magnetoresistive sensors

Von der Fakultät für Informatik, Elektrotechnik und Informationstechnik der Universität Stuttgart zur Erlangung der Würde eines Doktor-Ingenieurs (Dr.-Ing.) genehmigte Abhandlung

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سنكون يومَا مَا نريد، لَا الرحلَةُ ابتدَأَت و لَا الدرب انتهي.

One day we will be what we want to be. The journey has not started and the road has not ended.

Mahmoud Darwish – Palestinian poet

To my family

La familia es todo

Erklärung

Hiermit erkläre ich,

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- dass ich keine anderen als die angegebenen Quellen und alle wörtlich oder sinngemäß aus anderen Werken übernommenen Aussagen als solche gekennzeichnet habe,
- dass die eingereichte Arbeit weder vollständig noch in wesentlichen Teilen Gegenstand eines anderen Prüfungsverfahrens ist,
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Abstract

The continuous search for highly sensitive, agile and cost-effective sensors for magnetic biosensing applications has been met with high performance magnetoresistive (MR) sensors. While the MR effect has been discovered 150 years ago, there is a growing trend of improving the sensitivity of MR sensors while keeping their noise performance as low as possible. However, such improvements have to be complemented with high performance frontends that can effectively amplify the minute MR sensor's signals while keeping the system's noise floor unaltered. More importantly, the designed frontends have to be equipped with offset compensation peripheral circuits that can efficiently handle the large spread of the base resistance in MR sensors with high MR ratios such as in tunnel magnetoresistive (TMR) sensors.
In this thesis, we developed multiple frontend electronics that successfully interfaced MR sensors while, simultaneously, achieving competitive noise performance compared to state-of-the-art (SoA) designs tailored for MR sensor readout. The first variant of chips are specifically designed for high performance and high linearity designs thanks to a novel implementation of an ultra-low-noise current bias achieving SoA current noise floor of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and chopped voltage-mode amplification stages resulting in a total voltage noise floor of $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, including a TMR sensor and a reference resistor with base resistance of $1\,\mathrm{k}\Omega$.
In order to integrate an analog-to-digital converter (ADC) without substantial additional power and/or area, we show in this work a continuous-time current-mode Sigma-Delta modulator (CT C-SDM) that can directly interface MR sensors without additional amplifiers. Our proposed design does not only show a competitive noise floor of $8.1\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$, but also features a novel DC servo loop (DSL) around the modulator that maximizes the useful dynamic range (DR) of the modulator while successfully rejecting the undesired DC offsets of MR sensors.
Both design variants shown in this thesis, pave the way to designing high performance point-of-care (PoC) systems for in-vitro diagnostics while keeping their costs low compared to alternative bulky and expensive systems.

Zusammenfassung

Die ständige Suche nach hochempfindlichen, beweglichen und kostengünstigen Sensoren für magnetische Biosensorik-Anwendungen wurde mit hochleistungsfähigen magnetoresistiven (MR) Sensoren beantwortet. Obwohl der MR Effekt bereits vor 150 Jahren entdeckt wurde, gibt es einen stetigen Trend, die Empfindlichkeit von MR Sensoren zu verbessern und gleichzeitig ihr Rauschverhalten so gering wie möglich zu halten. Solche Verbesserungen müssen jedoch durch leistungsstarke Frontends ergänzt werden, die die winzigen Signale des MR Sensors effektiv verstärken können, ohne das Rauschverhalten des Systems zu beeinträchtigen. Noch wichtiger ist, dass die entwickelten Frontends mit Peripherieschaltungen zur Offsetkompensation ausgestattet sind, die die große Streuung des Basiswiderstands in MR Sensoren mit hohen MR Verhältnissen, wie z.B. in tunnelmagnetoresistiven (TMR) Sensoren, effizient handhaben können.
Die erste Generation der Chips wurde speziell für Hochleistungs- und Hochlinearitätsdesigns entwickelt, die dank einer neuartigen Implementierung einer extrem rauscharmen Stromquelle, mit einem Stromrauschen von $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$, und einer gechoppten Spannungsverstärkerstufe, einem TMR Sensor sowie einem Referenzwiderstand von $1\,\mathrm{k\Omega}$, zu einem Gesamtspannungsrauschen von $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ führt.
Versuchend, einen Analog-Digital-Umsetzer (ADU) ohne wesentliche zusätzliche Leistung und/oder Fläche zu integrieren, zeigen wir in dieser Arbeit einen zeitkontinuierlichen Sigma-Delta-Modulator im Strommodus (CT C-SDM), der MR Sensoren ohne zusätzliche Verstärker direkt anschließen kann. Das von uns vorgeschlagene Design weist nicht nur ein konkurrenzfähiges Grundrauschen von $8.1\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ auf, sondern verfügt auch über eine neuartige DC-Servoschleife (DSL) um den Modulator, die den nutzbaren Dynamikbereich des Modulators maximiert und gleichzeitig die unerwünschten DC-Offsets der MR Sensoren erfolgreich unterdrückt.
Beide in dieser Arbeit gezeigten Design-Varianten ebnen den Weg für die Entwicklung hochleistungsfähiger Point-of-Care (PoC)-Systeme für die In-vitro-Diagnostik und und sind gleichzeitig platzsparend und kostengünstig im Vergleich zu (kommerziellen) Systemen.

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Nomenclature

Abbreviations

AAF Antialiasing filter

ADC Analog-to-digital converter

AMR Anistropic magnetoresistance

ASIC Application specific integrated circuit

BW Bandwidth

C-SDM Current-mode Sigma-Delta modulator

C-TIA Capacitive transimpedance amplifier

CCIA Capacitively-coupled instrumentation amplifier

CFIA Current-feedback instrumentation amplifier

CMFB Common-mode feedback

CMRR Common-mode rejection ratio

CT Continuous-time

DAC Digital-to-analog converter

DR Dynamic range

DSL DC servo loop

DUT Device under test

ELD Excess loop delay

FDDA Fully differential difference amplifier

FDM Frequency division multiplexing

FIR Finite impulse response

GBW Gain-bandwidth product

GMR Giant magnetoresistance

HRZ Half-return-to-zero

I-SDM Incremental Sigma-Delta modulator

IA Instrumentation amplifier

IC Inversion coefficient

IIT Impulse invariant transform

MLD Mixed-logical dynamical

MNT Magnetic nanotag

MR Magnetoresistance

MSA Maximum stable amplitude

NRZ Non-return-to-zero

NTF Noise transfer function

opamp Operational amplifier

OTA Operational transconductance amplifier

PCB Printed circuit board

PGA Programmable gain amplifier

PoC Point-of-care

PSD Power spectral density

QN Quantization noise

R-TIA Resistive transimpedance amplifier

SCR Switched capactior resistor

SDM Sigma-Delta modulator

SNDR Signal to noise and distortion ratio

SNR Signal to noise ratio

SoA State-of-the-art

SPI Serial Peripheral Interface

SQNR Signal to quantization noise ratio

SQUID Superconducting quantum interference device

STF Signal transfer function

SV Spin-valve

TIA Transimpedance amplifier

TMR Tunnel magnetoresistance

UGF Unity-gain frequency

Symbols

α_{H} Modified Hooge parameter

γ Thermal noise excess factor

C_{ox} Oxide capacitance per unit area

f Frequency

f_{fl} 1/f-corner frequency

g_{m} Transconductance

k Boltzmann constant

n Slope factor

T Absolute temperature

U_{T} Thermal voltage

V_{th} Threshold voltage

KF Flicker noise factor

1 Introduction

1.1 Motivation and research objectives

Magnetoresistive (MR) sensor systems are gaining momentum in the biosensing research sector due to their simplicity, low-cost and excellent sensitivities [2]. The growing interest in MR sensor systems has also extended their application horizon to include magnetic neural recorders [3] that aim to record single-events at the neuronal scale. To achieve unprecedented sensitivities, research is extensively done on both the sensor's front as well as the frontend electronics side. With advancing technologies and the ability to precisely manufacture new MR sensors, tunnel magnetoresistors (TMR) are becoming more attractive to the aforementioned applications due to their unparalleled sensitivities [4, 1]. Unfortunately, without high performance readout electronics tailored to the specific needs of the MR sensors, such sensitivities cannot be fully exploited. The challenges posed upon the readout electronics include the following:

- The frontend has to be able to compensate for large offsets generated by the MR sensor, especially in TMR sensors where the MR ratio is high.
- The noise performance of the MR sensor frontend has to be kept lower than the MR sensor to preserve the intrinsic signal-to-noise ratio (SNR) of the MR sensor system.
- The large parasitic capacitance of the MR sensor should be handled by the frontend electronics without sacrificing the performance or the bandwidth of operation.

As a starting point, we carefully examined state-of-the-art (SoA) designs and observed that most frontend designs are tailored for giant magnetoresistive (GMR) sensors where the offsets are usually lower compared to TMR sensors due to their lower MR ratios and sensitivities. Moreover, while SoA designs show excellent noise performance, they still show higher noise floor compared to the MR sensor. As a result, we find the design of highly versatile frontend electronics for TMR with ultra-low-noise floors a design space that has not been explored before. In this work, we investigate two design architectures that can be embedded in MR sensor systems. With high performance MR sensor systems, electronics with small form factor, cost and competitive noise floors, we envision that the next generation of point-of-care (PoC) systems can be used everywhere in the world with very high sensitivities needed for in-vitro diagnostic systems.

1.2 Thesis organization

This thesis is divided into 7 chapters including this motivational chapter. The rest of this thesis is organized as follows:

- **Chapter 2** presents a short theoretical background about different MR sensors including their advantages and disadvantages as well as their readout challenges. Afterwards, a brief comparison of available readout topologies for MR sensor readouts is introduced.
- **Chapter 3** introduces the first generation of MR sensor readout chips using voltage-mode amplifiers and current-mode biasing electronics for the MR sensors. The results of this chapter are used to pinpoint the challenges behind reaching very low-noise frontend electronics for MR sensor systems.
- **Chapter 4** is devoted to the second generation of MR sensor systems using a novel low-noise current bias achieving SoA current noise floors. Moreover, the newly designed chips feature a chopped voltage-mode readout for excellent noise performance lower than the noise floor of the MR sensors used in this work.
- In **Chapter 5**, we turn our attention to current-mode designs aiming to lower the power and area requirements of an MR sensor system. We start this part of the thesis by proposing an accurate analytical noise model of transimpedance amplifiers (TIAs) that is applicable for resistive TIAs (R-TIAs), capacitive TIAs (C-TIAs), and current-mode analog-to-digital converters (ADCs). In the end, we provide circuit designers with a noise-aware design methodology of TIAs, which is particularly important for low-noise TIA variants.
- In **Chapter 6**, we introduce a continuous-time current-mode Sigma-Delta modulator (CT C-SDM) that can directly interface MR sensors without additional circuitry upfront. Moreover, we propose a DC servo loop (DSL) around the modulator to increase the effective dynamic range (DR) of the modulator for applications with large input DC offsets, such as TMR sensor systems.
- **Chapter 7** concludes this thesis with a brief discussion comparing the different circuit architectures introduced in this work. Finally, suggestions for future research considerations regarding low-noise MR and quantum sensor systems are presented.

1.3 Research contributions

This work has lead to 2 journal papers and 8 conference proceedings. Most of the research outcome of this work can be classified into the following areas:

- **Low-noise voltage-mode readout electronics for MR sensors:** In this research, two different electronic chips dedicated to MR sensor systems are developed. It has been shown in this work that both chips could successfully interface TMR sensors. Specifically, the second generation of chips achieves a SoA current noise floor for MR sensor bias which is 5x lower compared to the SoA, and the overall voltage noise of the frontend achieves 2x lower noise compared to prior arts [5, 6, 7].
- **Low-noise CT C-SDM for MR sensors:** In order to reduce the footprint of the embedded electronics by directly interfacing an MR sensor with an ADC, potentially reducing its costs, we introduce a CT C-SDM with a novel DSL and finite impulse response (FIR) digital-to-analog converter (DAC) [8]. Together with our detailed analytical noise model for TIAs, our design offers a competitive solution for MR sensor systems [9].

One of the future steps following this research is to extend our CT C-SDM to an incremental SDM (I-SDM) allowing for multiplexing an array of MR sensors used in bioassay systems, for example. Towards this goal, in this thesis, we have already presented for I-SDMs a mixed-logical dynamical (MLD) system that can precisely determine the stability of I-SDMs for different modulator orders and internal quantizer levels [10].

2 MR sensor systems: A brief introduction and review of the SoA

MR sensors are becoming increasingly attractive for multiple applications ranging from automotive systems, over consumer electronics and to biomedical sensor systems. In this chapter, different types of MR sensors are discussed including their physical structures, as well as their advantages and disadvantages. Moreover, the basic principles of the readout systems are explained including readout architectures for MR sensors. Afterwards, we compare different MR sensors in terms of noise, complexity, and multiplexing capabilities. To this end, the architecture of the amplifiers used in such systems are also explained alongside with their advantages and disadvantages.

2.1 Types of MR sensors

A magnetic sensor is a sensor that converts the magnitude and/or phase of a magnetic field to an electrical signal that can be processed by subsequent electronics. Since magnetic sensors play an important role in numerous applications, there is a continuous driving force to improve their performance. This can be done not only by improving the current MR sensors, but also researching different physical phenomena contributing to the research of new types of magnetic sensors. A magnetic sensor can be as simple as an induction coil detecting changes in the magnetic flux density. While coils can be very simple to build, they cannot operate at DC and can be bulky to achieve high resolutions [11]. Alternatively, Hall sensors can be used to measure both DC and AC fields due to the Lorentz force [12]. At the higher end of magnetic sensors, the superconducting quantum interference device (SQUID), relying on the Josephson effect, offers unmatched limit of detection (LOD) of single-digit $\mathrm{fT}/\sqrt{\mathrm{Hz}}$ [13]. Despite their excellent sensitivity, they always need to operate at cryogenic temperatures and are typically large in size [14]. As a result, SQUIDs are only suitable for high-end research and niche projects requiring measuring minute magnetic fields irrespective of the affordability or complexity of the system. On the other hand, MR sensors provide very good sensitivities while being available in smaller sizes and can operate in room temperature [15]. As a result, MR sensors are available on the market since 1994 [16].

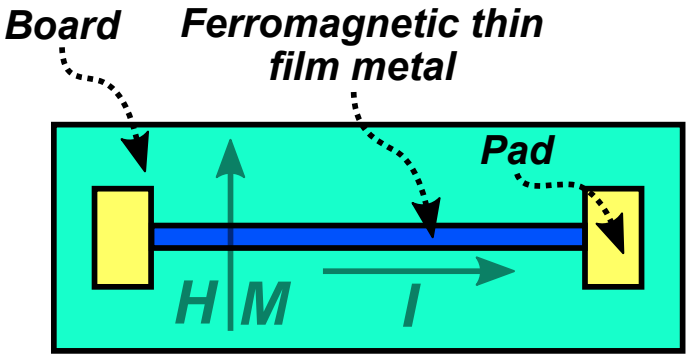

Figure 2.1: Sketch of an AMR sensor in the low resistance state where the current is applied across a ferromagnetic thin film metal. After applying a magnetic field H, a change in the magnetization M of the ferromagnetic material is observed.

2.1.1 AMR sensors

MR sensors are not only gaining momentum in the life sciences fields as will be described in details in this work [2, 17], but they are widely spread in multiple domains such as automotive [18], consumer electronics [19] or even for industrial environments [20]. Although being incorporated in many application these days, the origin of MR effect is not new and has been discovered more than 150 years ago by the famous mathematical physicist and engineer Lord Kelvin (William Thomson) in 1851 [21]. His experiments show that a resistance change, measured by supplying current in iron, is observed when the piece of iron is subjected to a magnetic field. He also observed the same phenomena with nickel but the change in resistance was higher compared to iron while applying similar magnetic fields. What is also interesting is that an increase in resistance is observed when the applied magnetic field is *along* the direction of the supplied current. On the other hand, a reduction of resistance has been detected when the applied magnetic fields are *across or perpendicular to* the direction of the applied current. It took the world 100 more years, until 1975, to transform this idea into a practical realization using the infamous anisotropic magnetoresistive (AMR) sensor as foreseen by Thompson, Romankiw and Mayadas in [22]. A comprehensive review of the physics behind AMR is given in an accompanying paper by McGuire and Potter in [23] where they show that the change in the observed resistance is due to the change of resistivity of the ferromagnetic material. This phenomena is caused by a change in the direction of magnetization in response to the applied fields. Without applying any fields, the direction of the magnetization is parallel to the anistropy axis (easy axis). The concept of an AMR sensor is illustrated in Fig. 2.1. In this figure, a ferromagnetic thin film metal is placed on a printed circuit board (PCB) acting as physical support. A current is applied through two pads on the PCB and a change in voltage across the two pads can be measured when an external magnetic field H is applied. The applied field in return changes the magnetization M of the free layer and, ultimately, changes the resistance of the ferromagnetic material. The resistivity ρ of the ferromagnetic

material becomes a function of the angle ϕ between the applied current I and the magnetization M as follows [24]:

$$\rho(\phi) = \rho_{\perp} + \left(\rho_{\parallel} - \rho_{\perp}\right)\left(1 - \sin^2(\phi)\right), \tag{2.1}$$

where $\rho_{\perp,\parallel}$ are the resistivities for $\phi = 0°$ and $90°$, respectively. While the transversal magnetic field intensity H_x is not shown in eq. 2.1, it is already included in the angle ϕ as follows [25]:

$$\sin(\phi) = \frac{H_x}{H_S}, \tag{2.2}$$

where H_S is the saturation field. A typical transfer characteristic is shown in Fig. 2.2 highlighting the change in resistance observed in an AMR sensor while changing the magnetic field. An apparent drawback of this structure is that the sensor is extremely non-linear at zero fields where the sensor is supposed to operate. Moreover, the AMR characteristics shows a symmetrical resistance behavior for both positive and negative fields rendering this structure useless for detecting the direction of the magnetic fields. One could however observe that the transfer characteristic is highly linear at $H_x/H_0 = \pm 0.7$ or $\phi = 45°$. Consequently, an external magnetic field can be applied to alter ϕ to $45°$. A simpler solution presented in [24] proposes to rotate the current vector by $\phi = 45°$ while keeping the magnetization vector unaltered. This can be achieved by covering the ferromagnetic material by stripes of a conductor forcing the current to flow in a direction perpendicular to the stripes as shown in Fig. 2.3. By mechanically placing these stripes with an angle $\phi = 45°$ to the easy axis, the resistance curve is shifted as highlighted in Fig. 2.4 and the advantages of such design are twofold. First, the sensor is more linear at $H_x = 0$ which is desirable for many applications operating around such fields. Moreover, the direction of the magnetic field can be extracted due to the asymmetrical resistance characteristic around zero fields.
In order to characterize AMR sensors, and generally all MR sensors described in this work, two main properties of MR sensors are highlighted in Fig. 2.5. First, the

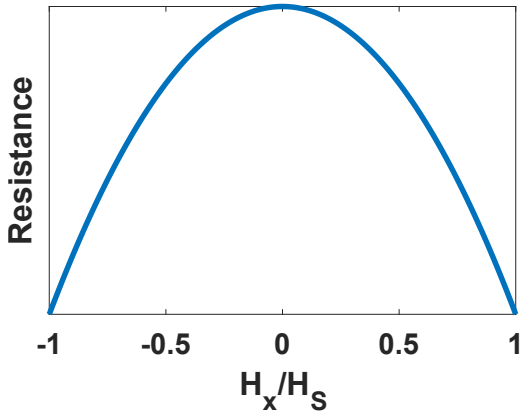

Figure 2.2: A typical transfer characteristic of an AMR sensor.

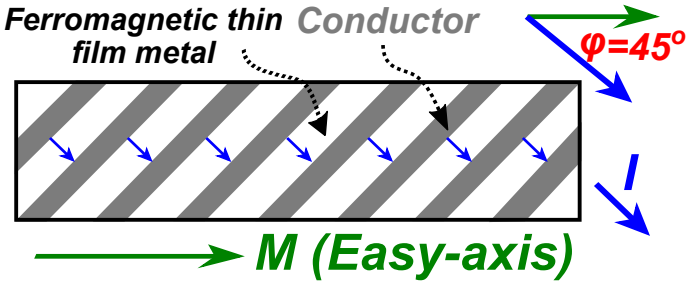

Figure 2.3: A sketch of an AMR sensor exhibiting stripes of a conductor in order to force the current to flow at an angle $\phi = 45°$ to the easy axis.

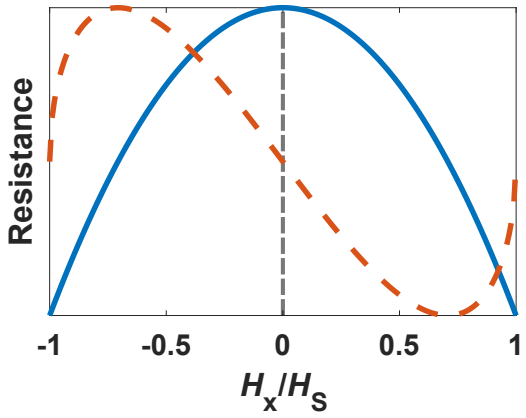

Figure 2.4: Resistance as a function of the applied field for the case when $\phi = 45°$ (in dashed orange) compared to the resistance against the applied field for $\phi = 0°$. In the first case, the AMR sensor has a linear output around $H_x = 0$. Moreover, the direction of the field can be extracted from the resistance curve due to the asymmetrical characteristic.

MR ratio which is defined as follows:

$$\mathrm{MR} = \frac{R_{\max} - R_{\min}}{R_{\min}}. \tag{2.3}$$

Moreover, the sensitivity of the MR sensor is extracted at the operating point of the sensor. In many cases, the operating point is located at $H = 0$. In this case, the sensitivity S at H_0 is expressed as:

$$S = \frac{\partial R}{\partial H}\Big|_{H=H_0}. \tag{2.4}$$

While AMR sensors can be used in multiple applications to detect magnetic fields, they typically show limited MR ratios of only 2% [26]. Hence, new technologies have been developed to overcome this drawback and increase the output signal of an MR sensor, and in return, relax the noise requirements of the frontend connected to the MR sensor.

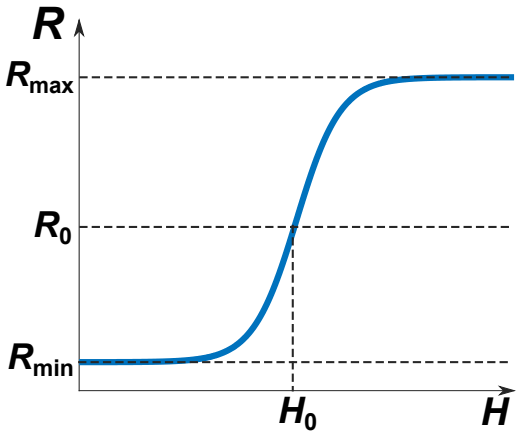

Figure 2.5: A typical MR curve to illustrate the difference between MR ratio and the sensitivity of a MR sensor.

2.1.2 GMR sensors

The next generation of MR sensors has been discovered by experimenting structures composed of magnetic and nonmagnetic metal layers formed in a multi-layer structure. A major breakthrough has been achieved by Albert Fert [27] and Peter Grünberg [28] when they observed the first GMR effect using a multi-layer structure made of magnetic layers of Iron (Fe) separated by a thin non-magnetic conductive layer of Chromium (Cr). Eventually, both scientists won the Nobel prize in Physics in 2007 for their important discovery that changed the course of MR sensors in our time.

The physical phenomena behind the GMR effect can be illustrated as follows. In principle, antiferromagnetic coupling can occur between two adjacent Fe layers when the Cr thickness is below 3 nm [27]. This translates to a change in the magnetization of the Fe layers into an antiparallel state. By applying an external magnetic field, the magnetization of the top layer is changed to be parallel w.r.t. the bottom layer (parallel state). The resistance of the parallel and antiparallel states can be explained with the aid of Fig. 2.6 showing a GMR arrangement and a simple circuit diagram corresponding to such a structure. In Fig. 2.6a, the antiparallel state is shown where the magnetization of the Fe layers are opposite to each other. An electron with a spin-up state (highlighted in yellow) passes the first boundary with limited scattering since the spins of the electron and the ferromagneitc layer are aligned. The limited scattering leads to smaller resistance as shown in the resistance diagram Fig. 2.6a (middle). After passing the second boundary, the spins are now antiparallel to each other and scattering increases eventually increasing the resistance. Similarly, the electron with a spin-down state (highlighted in green) experiences the same scattering mechanism but in opposite direction. The overall resistance for the entire structure is then called the antiparallel resistance. Similarly, Fig. 2.6b shows the flow of electrons when the GMR sensor is configured in the parallel state. In this case, an electron with a spin-up state experiences little scattering in the resistance

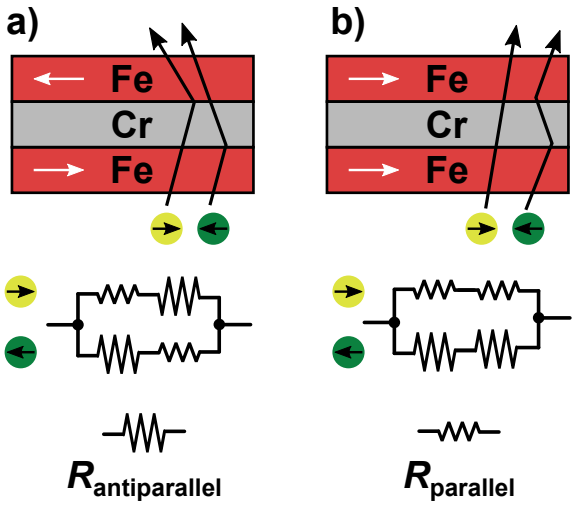

Figure 2.6: A sketch showing a GMR element and the flow of electrons in a) parallel and b) antiparallel states.

through both boundaries since it is aligned with the Fe layers resulting in a small resistance. In contrast, an electron with a spin-down state experiences larger scattering through both boundaries. Evidently, this structure forms a parallel resistance which is smaller compared to the antiparallel resistance shown in Fig. 2.6a.
The sensitivity of the multilayer GMR structure has been improved later in 1991 by introducing a different GMR structure called the spin-valve (SV) sensor [29]. Analog to the multilayer structure, SV sensors use an antiferromagnetic layer acting as pinning layer on the top or the bottom of the ferromagnetic material. This pinning layer pins the ferromagnetic layer, which means that it fixes the magnetization of the ferromagnetic layers without relying on the antiferromagnetic coupling between the different layers. In other words, the magnetization of one ferromagnetic layer is pinned by an added antiferromagnetic layer and not by the coupling between ferromagnetic layers through a spacer [30]. The overall structure of a GMR SV sensor as well as its resistance characteristics are shown in Fig. 2.7.

2.1.3 TMR sensors

Since nanotechnology is a key enabler to designing robust and thin magnetic and non-magnetic layers, tunnel magnetoresistive (TMR), also known as magnetic tunneling junction (MTJ), are gaining momentum for highly sensitive MR sensors. This is achieved by replacing the non-magnetic conductor in a SV sensor with a very thin insulator forming a tunnel barrier [31]. The insulating barrier is mostly made of Al_2O_3, or more recently, MgO with a thickness down to 1 nm [30]. While MR ratios of only 10% at room temperature have been achieved in 1995 [32], innovative structures lead to a huge increase in MR values to 70% [33] and 600% [4] using Al_2O_3 and MgO spacers, respectively. While TMR sensors display superior sensitivity com-

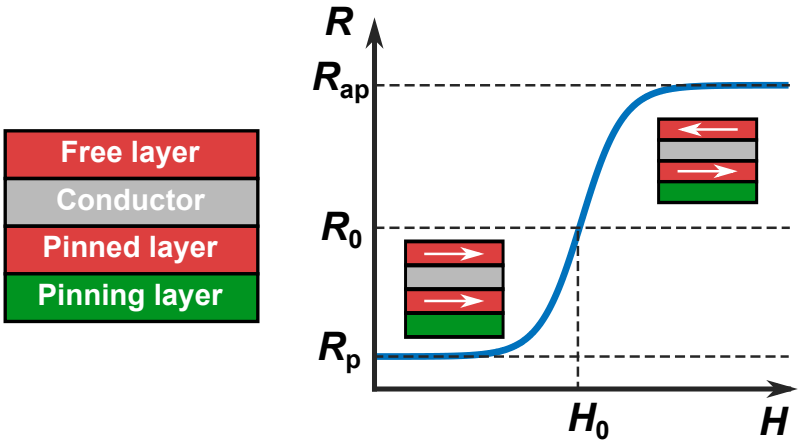

Figure 2.7: A typical resistance profile of an MR sensor while sweeping the magnetic field H.

pared to GMR sensors, their 1/f-noise is relatively higher and bias dependent [34], limiting their performance for low-noise applications. Overall, the voltage noise PSD of the TMR sensor $S_{\Delta V^2_{\mathrm{TMR}}}$ is given by:

$$S_{\Delta V^2_{\mathrm{TMR}}} = 4kTR_{\mathrm{TMR}} + \frac{\alpha_{\mathrm{H}} \cdot I_{\mathrm{b}}^2 \cdot R_{\mathrm{TMR}}^2}{A \cdot f}, \tag{2.5}$$

where k is the Boltzmann constant, T is absolute temperature, R_{TMR} is the TMR resistance, I_{b} is the bias current, α_{H} is a modified Hooge parameter, A is the area of the TMR element, and f is the frequency of operation. While the noise power is proportional to the bias current squared, I_{b}^2, the SNR is a better measure of the overall performance of the sensor. The SNR of a TMR element is given by:

$$\mathrm{SNR}_{\mathrm{TMR}} = \mathrm{MR}\,\frac{I_{\mathrm{b}}^2 \cdot R_{\mathrm{TMR}}^2}{S_{\Delta V^2_{\mathrm{TMR}}}} = \mathrm{MR}\left[\frac{I_{\mathrm{b}}^2 \cdot R_{\mathrm{TMR}}}{4kT} + \frac{A \cdot f}{\alpha_{\mathrm{H}}}\right]. \tag{2.6}$$

Eq. (2.6) shows that the SNR can be improved by increasing the bias current, I_{b}, only in the thermal noise-limited region. On the other hand, increasing area as well as the MR ratio are the only possible routes to improve the SNR for 1/f-limited region. To improve the low-frequency noise performance of TMR sensors, [1] suggests placing multiple TMR elements in series and in parallel to lower their 1/f-noise contribution. An example of such a configuration is shown in Fig. 2.8 where the micrograph of a TMR sensor consisting of 1102 TMR elements connected in such a matrix form is used to lower the 1/f-noise [35]. While the large MR ratio of a TMR sensor leads a higher SNR, cf. eq. (2.6), it also leads to a large voltage offset that could saturate the frontend amplifier. This large voltage offset is caused by the large process variation in a TMR base resistance and is then amplified by the large MR ratio of the TMR sensor. As a result, in the next section, we will discuss different MR sensor readout frontends specifically tailored to deal with these large offsets, while amplifying the

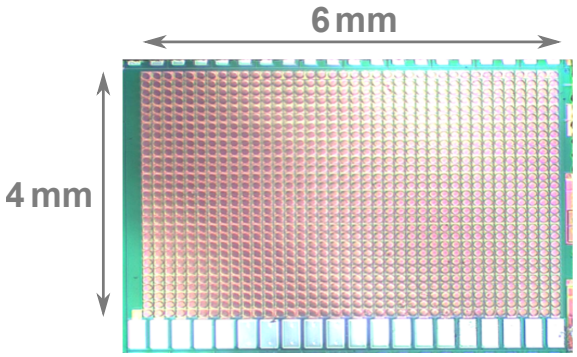

Figure 2.8: A micrograph of a TMR sensor consisting of 1102 TMR elements connected in series and parallel to reduce the 1/f-noise [1].

minute MR sensor signals and simultaneously preserving the intrinsic SNR of the MR sensor.

2.2 Readout of MR sensors

While many emerging applications such as biosensing PoC systems [36, 2] and human machine interfaces for augmented reality applications [37] rely on MR sensors due to their excellent sensitivities, robustness and low cost, they still impose strict requirements on the signal conditioning circuitry. This is mainly due to the large magnetic fields associated with the earth magnetic field or external fields generated by different instruments used around the setup. This challenge is more pronounced in TMR sensors due to their high MR ratio leading to an increased voltage offset at the input of the frontend amplifiers. Ultimately, a reduction in the amplifier's dynamic range is expected or, in worse cases, the outputs of the amplifiers are saturated by the large undesired offsets. To counteract such offsets, different frontend architectures can be employed. One of the early promising designs for GMR sensors incorporated a transimpedance amplifier (TIA) as the GMR sensor frontend [2]. The TIA frontend offers a virtual ground at the input, cf. Fig. 2.9, and hence, simplifies current summation of an array of MR sensors thanks to the virtual ground. This in turn allows for frequency division multiplexing (FDM) and, consequently, reduces the total time required to readout the MR array. Another advantage of the TIA-based architecture is that the voltage bias $V_{\mathrm{B},i}$ noise can be minimized by appropriate low-pass passive filters using large off-chip capacitors, for example. On the other hand, filtering current noise of a current bias can be achieved using complex electronics to filter the bias noise as shown in details in the next chapter. This design also minimizes the offset of the MR sensor by adding a current source/sink using V_{DAC} applied to R_{DAC}. All these characteristics render the TIA frontend a simple solution for MR array readout. However, the primary drawback of the TIA-based architecture is that the output of the TIA does not change linearly with a change in the input resistance. To mathematically identify this non-linearity, a Taylor series

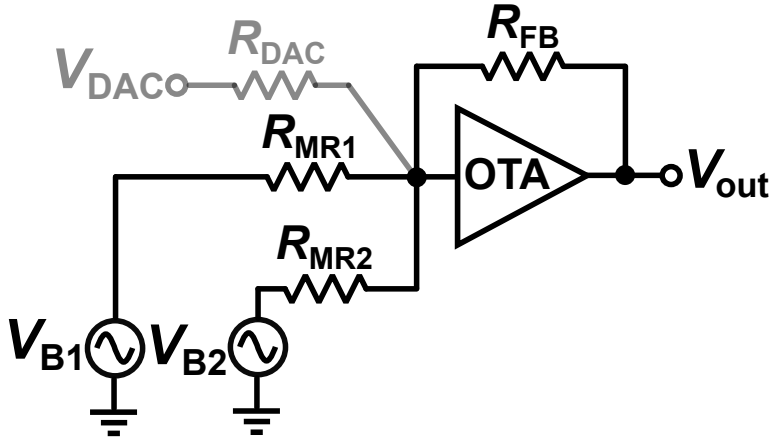

Figure 2.9: TIA frontend for MR sensors.

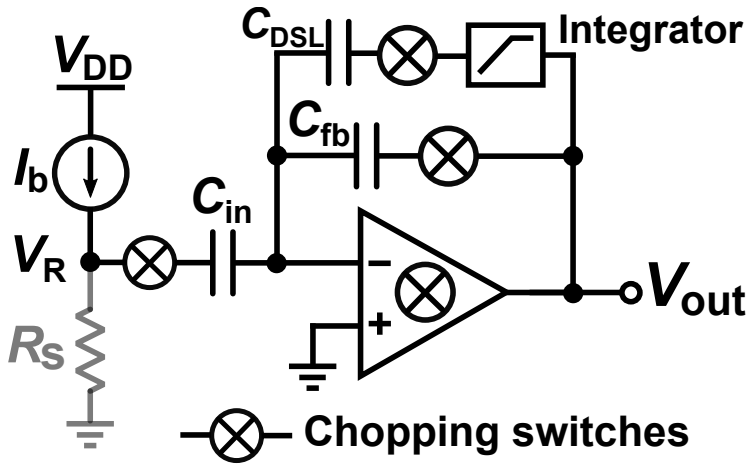

Figure 2.10: Block diagram of a CCIA with a DSL to compensate for the DC offsets.

can be used to express the output of the TIA, $V_{\text{out}}(t)$ as follows:

$$V_{\text{out}}(t) = \frac{V_{\text{B}} \cdot R_{\text{FB}}}{R_{\text{MR}} + \frac{\Delta R}{2}\sin(\omega_f t)} \approx \frac{V_{\text{B}} \cdot R_{\text{FB}}}{R_{\text{MR}}} \left(1 + \left(-\frac{\Delta R}{2R_{\text{MR}}}\sin(\omega_f t)\right)\right) + \left(-\frac{\Delta R}{2R_{\text{MR}}}\sin(\omega_f t)\right)^2 + \dots \tag{2.7}$$

For large $\Delta R/R_{\text{MR}}$, this non-linearity manifests itself as harmonic distortion [2]. In order to mitigate the intrinsic non-linearity of the TIA readout of MR sensors, a current bias followed by a voltage readout can be adopted, creating an intrinsically linear readout. An example of such architecture is shown in Fig. 2.10 where a capacitively-coupled instrumentation amplifier (CCIA) [38] is used to readout the voltage signal V_{R}. By incorporating chopping switches at the input of the CCIA, the amplifier's 1/f-noise and offset can be eliminated. However, when using chopping, the CCIA cannot block the MR sensor's DC signal due to the switched capacitor

structure forming a resistor, with an undesired input rms current, allowing the undesired DC component of the signal to pass without attenuation to the input of the FDDA. To solve this problem, a DC servo loop (DSL) is incorporated in the design to block the DC offset generated by the MR sensor. Ignoring the finite DC gain of the amplifier, the closed-loop gain (A_{CL}) of the CCIA at the frequency band outside the DSL operating frequency band can be calculated as follows:

$$A_{\mathrm{CL}} = -\frac{C_{\mathrm{in}}}{C_{\mathrm{fb}}}, \tag{2.8}$$

where C_{in} and C_{fb} are the input and the feedback capacitors, respectively. To compensate the offset, the DSL capacitance C_{DSL} has to be chosen large enough with respect to the maximum output voltage tolerable by the DSL integrator $V_{\mathrm{DSL,out}}$ and the maximum expected input offset $V_{\mathrm{offset,in}}$. The output voltage of the DSL $V_{\mathrm{DSL,out}}$ is given by:

$$V_{\mathrm{DSL,out}} = \frac{C_{\mathrm{in}}}{C_{\mathrm{DSL}}} V_{\mathrm{offset,in}}. \tag{2.9}$$

It is important to point out that $V_{\mathrm{DSL,out}}$ is limited by the amplifier supply voltages and cannot be arbitrarily chosen. While C_{in} is usually fixed to define A_{CL}, increasing C_{DSL} is the most practical solution to compensate for large offsets. However, this introduces a tradeoff between tolerable offset voltage and input-referred noise of the CCIA. The input-referred noise PSD of the CCIA, $S_{\Delta V^2_{\mathrm{CCIA}}}$, can be described in terms of the amplifier voltage noise PSD, $S_{\Delta V^2_{\mathrm{opamp}}}$, as follows [39]:

$$S_{\Delta V^2_{\mathrm{CCIA}}} = \left(\frac{C_{\mathrm{in}} + C_{\mathrm{fb}} + C_{\mathrm{DSL}} + C_{\mathrm{opamp}}}{C_{\mathrm{in}}} \right)^2 S_{\Delta V^2_{\mathrm{opamp}}}, \tag{2.10}$$

where C_{opamp} is the input capacitance of the opamp. As a result, increasing C_{DSL} can improve the maximum tolerable offset while, unfavorably, deteriorating the noise floor. This offset-noise tradeoff is more pronounced in TMR sensor systems due to the large voltage offsets at the amplifier inputs demanding a large C_{DSL} increasing the noise floor.

In order to break the offset-noise tradeoff, Fig. 2.11 shows a simple non-inverting amplifier can be used in combination with a current-mode DAC to compensate for the offset. While this design is intrinsically linear and simple to realize, it shows large (and unfavorable) baseline-to-signal ratio [40]. This effect is more pronounced in biosensing platforms where large magnetic fields are applied in the non-sensitive direction of the MR sensors to excite the magnetic nanotags (MNTs) used to detect a specific biomarker. Ultimately, the MR sensor is not totally blind to the applied fields and an undesired field components would be sensed by the MR sensor, due to the imperfect alignment for example, and could appear as a huge baseline signal at the input of the MR sensor [40, 36]. To compensate for such problems, a fully-differential CCIA with a reference sensor has been shown in [40, 36] where the baseline signal appears at both the MR and the reference sensor equally. As a result, the baseline signal appears as common-mode input signal and is attenuated

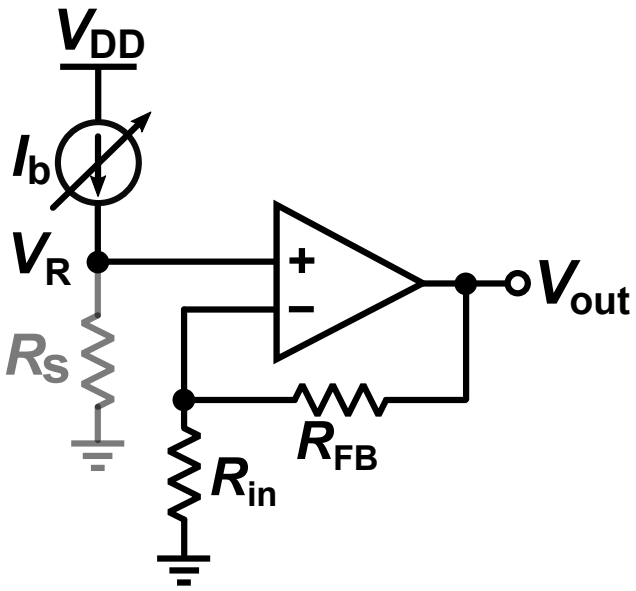

Figure 2.11: Non-inverting amplifier used for MR sensor readout.

by the common-mode rejection ratio (CMRR) of the CCIA. Another possibility to mitigate the offset-noise tradeoff of CCIAs is to implement a fully-differential difference amplifier (FDDA) as shown in Fig. 2.12a. The FDDA has been introduced back in 1987 [41] and it can be also found in prior arts under the name of current-feedback instrumentation amplifier (CFIA) [42]. In [43], an FDDA is used to readout a GMR sensor array and Fig. 2.12 shows an extension of the implemented design whilst including a reference sensor for an improved baseline-to-signal ratio. Herein, it is important to differentiate between the resistance of the MR sensor R_{S} and the reference sensors R_{REF}. Their resistances can be expressed in terms of their base resistances R_{MR}, undesired baseline resistance due to the field excitation R_{B} and the desired resistance change due to the detected MNTs $R_{\Delta\mathrm{R}}$ as follow:

$$\begin{aligned} R_{\mathrm{S}} &= R_{\mathrm{MR}} + R_{\mathrm{B}} + R_{\Delta\mathrm{R}}, \\ R_{\mathrm{REF}} &= R_{\mathrm{MR}} + R_{\mathrm{B}}. \end{aligned} \tag{2.11}$$

It is important to mention that the reference sensor does not show any signal component since it is usually covered with epoxy to avoid detecting any signal from MNTs [40]. Now assuming an infinite CMRR, the FDDA output can be expressed as follows:

$$V_{\mathrm{out}} = R_{\Delta\mathrm{R}} \cdot \frac{R_{\mathrm{FB}}}{R_{\mathrm{in}}}. \tag{2.12}$$

Despite the open-loop nature of the FDDA at nodes V_{R} and V_{REF}, the non-linearities are heavily attenuated in this structure due to the separate feedback. Fig. 2.12b highlights the non-linearity cancellation of the structure. Assuming perfect matching of the differential pairs, the non-linearity at the output current of M_{n1} and M_{n2}, as well as M_{n3} and M_{n4}, are equal to each other, and hence are perfectly canceled. A

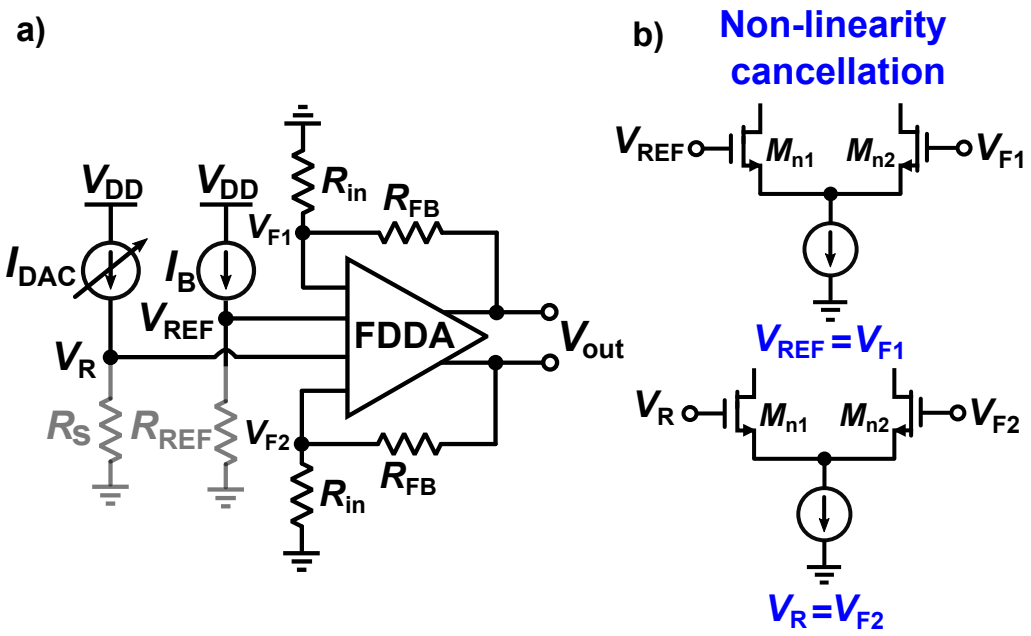

Figure 2.12: An FDDA used for MR sensor readout while rejecting baseline signals.

Table 2.1: Comparison between different MR frontend topologies.

	TIA	CCIA	Non-inv. amp.	FDDA
Complexity	Very simple	Complex	Simple	Average
Linearity	Non-linear	Very linear	Linear	Linear
Noise (low offset)	Excellent	Good	Very good	Average
Noise (large offset)	Excellent	Average	Very good	Good
Baseline rejection	Good	Good	Bad	Good

drawback of an FDDA compared to a CCIA is its higher noise floor for the same power. Neglecting the DSL in a CCIA, an FDDA has four input transistors, or two differential pairs, compared to only a single differential pair in a CCIA. This means that the noise power is two times higher in an FDDA. However, the large DC offsets necessitating a large C_{DSL} in a CCIA, cf. Fig. 2.10, increases its noise floor and can be comparable to an FDDA in the end. On the other hand, an FDDA does not have any offset-noise tradeoff and can be power efficient, if large offsets are expected, compared to a CCIA. Table 2.1 compares the different MR sensor readout frontends with respect to their performance.

3 First generation of voltage-mode readout chips

One of the main goals of this thesis is to present robust frontends for MR sensors. These frontends should preserve the intrinsic SNR of the entire sensor chain while being versatile against any environmental fluctuations. To this end, integrated circuits are chosen for the design of the frontend due to their flexibility and smaller footprints allowing the chips to be connected near to the MR sensors, and as a result, would reduce any parasitic coupling. In this work, magnetic neural recording and biosensing systems are considered as the main applications. In the first case, offsets are mainly generated due to external magnetic fields depending on the lab setup or the orientation of the magnetrode, in vivo, as well as large earth's magnetic field. Similarly, biosensing applications suffer from offsets due to external fields as well as baseline magnetic fields due to the field excitation of the magnetic nanotags [40]. While a differential measurement would help in reducing the baseline signal similar to [40], it cannot be extended to neural recording applications due to the absence of a reference sensor [3]. As a result, the frontend design has to compensate for these offsets, or be immune against them or completely eliminate them. In this chapter, we present the first generation of voltage-mode chips used for high performance MR sensor readout. After showing our measurement results, we finalize this chapter with findings to improve the performance of the voltage-mode readout electronics.

3.1 Design and implementation

In this work, we aim to design and develop a frontend chip that can be utilized for neural recording and magnetic biosensing applications. As shown in Table 2.1, there are multiple topologies that can be used for MR frontends. In this work, we chose a current bias with an FDDA frontend for the first two generations of the MR readouts. This is particularly important for designs with large offsets requiring high baseline rejection. Moreover, the chosen architecture provides a more linear output with respect to the change of the MR signal compared to a simple TIA as explained in the previous chapter. The chip architecture of the first generation of voltage-mode frontends is shown in Fig. 3.1. Any offset generated due to e.g. undesired external magnetic fields or temperature drifts is continuously monitored by the proposed DC-coupled readout scheme and calibrated using an on-chip 11-bit binary-weighted current-mode DAC compensating a major part of the offset generated by the mismatch of the MR and the reference sensors as well as the

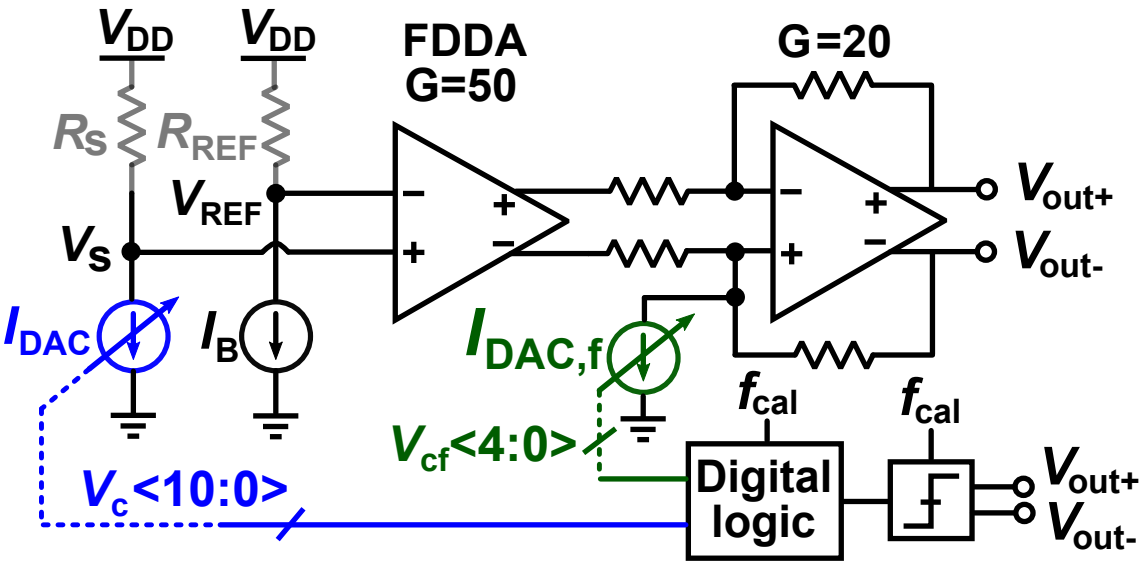

Figure 3.1: Overall block diagram of the readout chip.

offset generated by the amplifiers in the frontend. The residual offset is afterwards compensated by another 5-bit DAC that is connected to the second-stage amplifier. It is worth mentioning that the noise requirements of the second-stage DAC is relaxed compared to the frontend 11-bit DAC since it is connected after the output of the first amplifier, and hence, its input-referred noise is attenuated by the large gain of the FDDA. The timing diagrams of the DACs are shown in Fig. 3.2 highlighting the compensation operation. The first voltage gain stage is realized as an FDDA with a gain of 50. The FDDA is chosen over a classic three-opamp instrumentation amplifier (IA) due to its improved power efficiency, still providing the required high input impedance [44]. The FDDA is followed by a second fixed gain stage with a gain of 20 providing more gain to the frontend while having enough driving capabilities to drive the chip pads and the backend ADC on the PCB. In total, we designed the frontend to have a fixed gain of 60 dB to amplify the minute signals of the MR sensor.

3.1.1 Amplifier implementation

FDDA design

To achieve a high gain accuracy with a relatively large closed-loop gain of 50, a two-stage Miller compensated opamp is implemented. The detailed schematic of the FDDA is shown in Fig. 3.3 featuring an input stage that uses a current reuse scheme to increase the transconductance for a given bias current, and thereby, the power efficiency for a given speed and noise requirement [45]. Moreover, the input differential pairs are designed with a large area to reduce their 1/f-noise contribution. Their aspect ratio is chosen for an operation in weak inversion to maximize the $g_\mathrm{m}/I_\mathrm{d}$

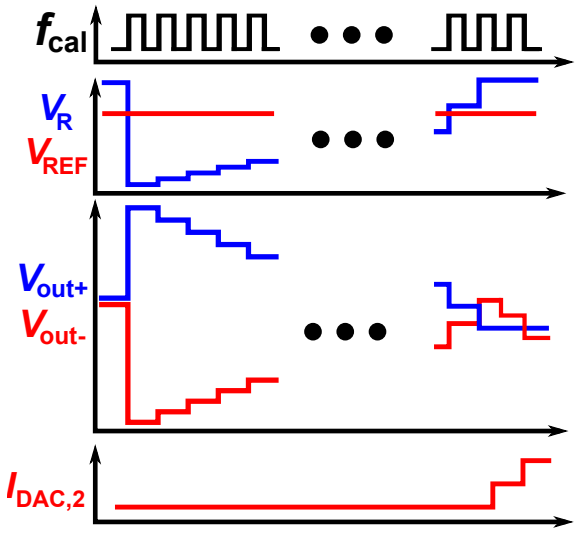

Figure 3.2: Timing diagram of the auto-calibration phase.

ratios of the individual transistors. Simulations showed that the PMOS transistor is superior compared to its NMOS counterpart in terms of 1/f-noise for a given transistor area in the utilized 180 nm technology. Accordingly, the sizing of M_{n1-2} and M_{n4-5} have been chosen larger compared to M_{p1-2} and M_{p4-5} with device sizes of 750 µm/1.5 µm and 480 µm/5 µm, respectively. Despite the relatively large device size, the input-referred noise of the FDDA exhibits a high 1/f-corner frequency of around 50 kHz as shown in Fig. 3.4. The closed-loop gain of the FDDA is not only set by the ratio of the feedback resistors, but also by the transconductances of the input and feedback differential pairs as follows:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{\text{mn1}} + g_{\text{mp1}}}{g_{\text{mn3}} + g_{\text{mp3}}} \cdot \frac{R_2}{R_1}. \tag{3.1}$$

As a result, for $g_{\text{mn1}} = g_{\text{mn3}}$ and $g_{\text{mp1}} = g_{\text{mp3}}$, the closed-loop gain becomes R_2/R_1. The stability of the high-gain FDDA is assessed using the STB analysis performed in Cadence Virtuoso. The loop gain of the FDDA is shown in Fig. 3.7 where a phase margin of 83° and a unity-gain frequency (UGF) of 3 MHz are simulated. To set the output common-mode of the FDDA, the common-mode feedback (CMFB) circuit used for the FDDA is shown in Fig. 3.5. The input pair of the CMFB circuit, $M_{n1,2}$ extract the output common-mode voltage of the amplifier, cf. Fig. 3.3, and compares it to the desired common-mode voltag $V_{\text{CM}} = V_{\text{DD}}/2$ [46]. To improve the stability of the CMFB circuit, the output voltage of the CMFB circuit controls only a part of the current of the input stage of the DDA, cf. M_{p5-p8} in Fig. 3.3. This in turn reduces the loop gain and significantly improves the stability of the CMFB loop. The simulated loop gain of the CMFB loop is shown in Fig. 3.6 and highlights the improved phase margin by lowering the current controlled by the CMFB. All in all, the phase margin improves from 34° to 67° due to the reduced loop gain.

Second-stage OTA

An additional two-stage Miller-compensated OTA follows the FDDA to provide an additional gain of 20. The transistor-level diagram of the second stage amplifier as well as its CMFB circuit are shown in Fig. 3.8. Since the output of second stage OTA has to accommodate data with higher swings compared to the FDDA's output, the input stage of the CMFB circuit had to be changed compared to that of the FDDA to keep the input transistors of the CMFB circuit in the saturation region, cf. Fig. 3.5. To solve this problem, averaging resistors $R_1 = R_2 = 1\,\mathrm{M\Omega}$ are used to extract the common-mode signal of the OTA's outputs. We have chosen higher resistance values to preserve the high output impedance of the OTA, and hence, keep the open-loop gain unaltered.

3.1.2 Sensor biasing

To implement a voltage-mode readout for optimum linearity, the MR sensors are biased with a current source. An 11-bit current-mode binary-weighted DAC is used to compensate any DC offset, e.g. due to mismatch between sensor and reference element, while introducing minimum noise into the system. The noise of the current-mode DAC is critical in this design since it is directly added to the input of the sensor system. The current noise power spectral density (PSD) of a MOS transistor in saturation can be modeled as:

$$S_{\Delta I^2_{\mathrm{nD}}} = 4kT\gamma g_{\mathrm{m}} + \frac{\mathrm{KF}\cdot g_{\mathrm{m}}^2}{C^{\mathrm{n}}_{\mathrm{ox}}\cdot W\cdot L\cdot f}, \tag{3.2}$$

where k is Boltzmann's constant, T is the absolute temperature, γ is the thermal noise excess factor, KF is the flicker noise factor, C_{ox} is the oxide capacitance per unit area, n is the slope factor and W and L are the transistor width and length, respectively. To choose an optimum transistor type for the current source, the current noise PSD of all available transistor flavors were simulated for $I_{\mathrm{d}} = 1\,\mathrm{mA}$ and compared while fixing their aspect ratios and their $g_{\mathrm{m}}/I_{\mathrm{d}}$ for a fair comparison. In this technology, there are high-threshold and low-threshold 1.8-V NMOS and PMOS devices that can be used as current sources. The simulated noise performance of each transistor as a current source is shown in Fig. 3.9. Clearly, the low-threshold PMOS device shows the best flicker noise performance, however, the low-threshold NMOS device shows a very low thermal noise performance compared to other transistors. As a result, the low-threshold NMOS transistor was chosen for the current source design. It is worth mentioning that for low-frequency applications, the low-threshold PMOS transistor would outperform the other options. Thermal and flicker noise are minimized by choosing an operating bias point deeply in strong inversion, where the transistor's $g_{\mathrm{m}}/I_{\mathrm{d}}$ can be minimized. Additionally, the second term in eq. (3.2), the contribution due to the devices flicker noise, is minimized by proper device sizing using sufficiently large devices. Overall, to satisfy both the thermal and the flicker noise requirements, DAC unit elements with aspect ratios of $850\,\mathrm{nm}/80\,\mu\mathrm{m}$

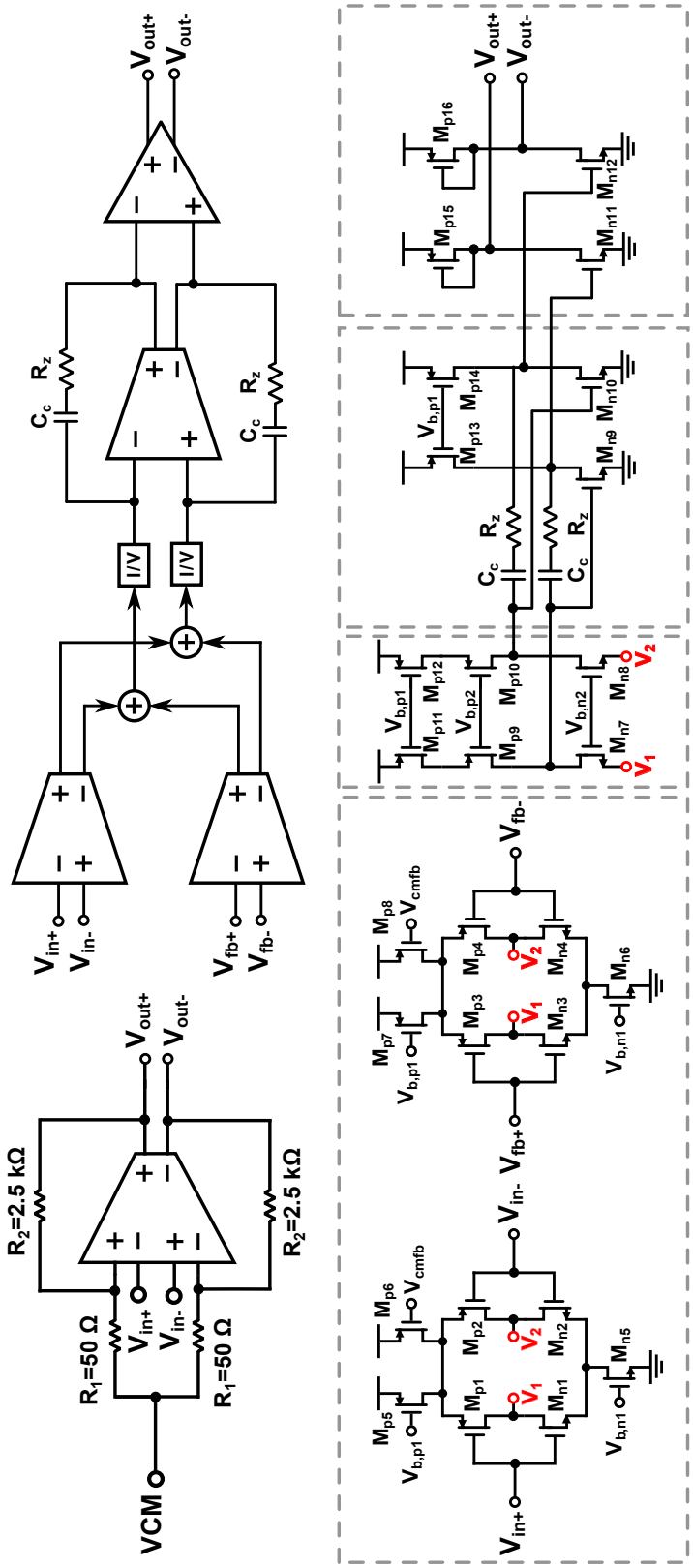

Figure 3.3: Block diagram of the implemented FDDA and transistor-level schematics of the building blocks.

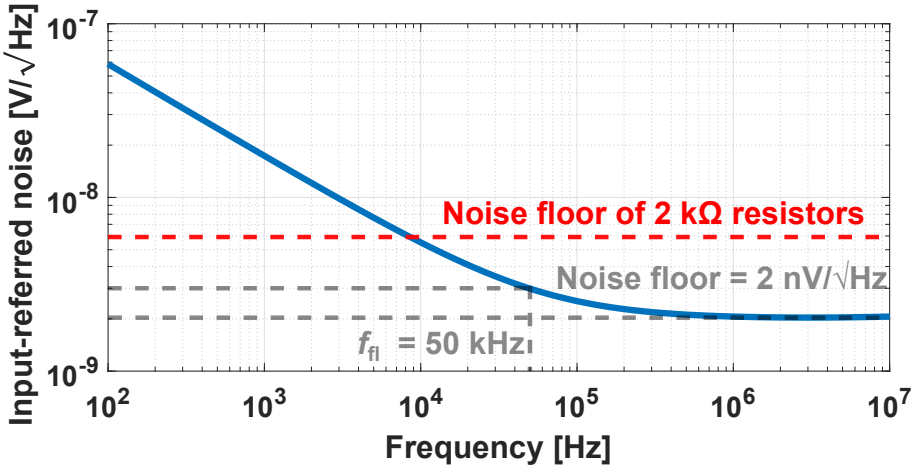

Figure 3.4: Input-referred voltage noise spectral density of the FDDA.

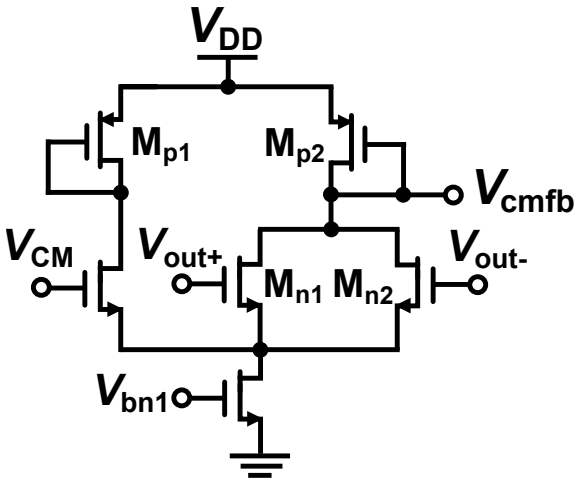

Figure 3.5: Transistor-level schematics of the CMFB circuit of the FDDA.

with a relatively large $|V_{\mathrm{ds,sat}}| = 600\,\mathrm{mV}$ are used for this design. Fig. 3.10 shows a transistor-level schematic of the 11-bit current DAC where the current is switched on and off using the cascoded devices via a switch. The switch is controlled by the on-chip digital logic, cf. Fig 3.1. This DAC's switching scheme via the cascoded devices is much faster compared to switching on and off the current source device due to the smaller capacitance accompanied with the cascoded MOS device compared to the relatively large, noise-critical current source MOS. For better matching, $M_{\mathrm{cs},i}$, cf. Fig. 3.10, are implemented using unit devices, and hence, 2048 unit elements for the 11-bit DAC are designed and layouted on-chip. To further improve matching of the DAC, the unit elements are organized in a common-centroid layout. The Module Generation tool (Modgen) was used to perform the placement of the elements efficiently.

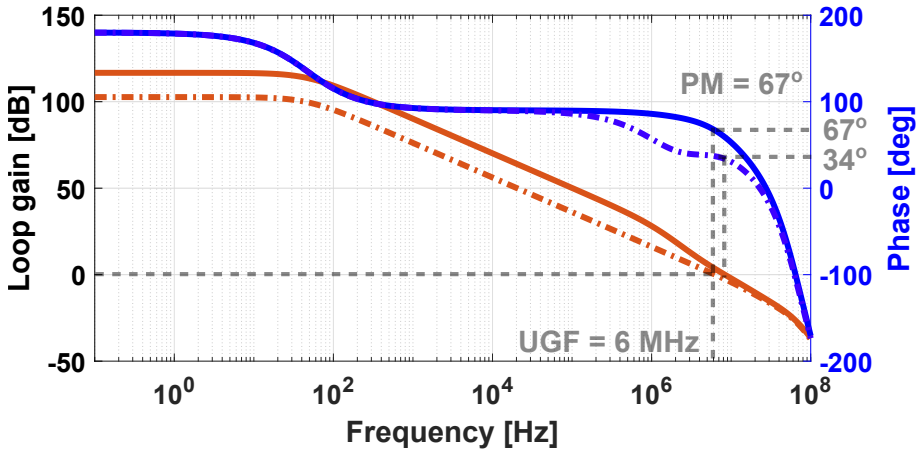

Figure 3.6: Simulations of the CMFB loop gain with and without current splitting in the CMFB loop.

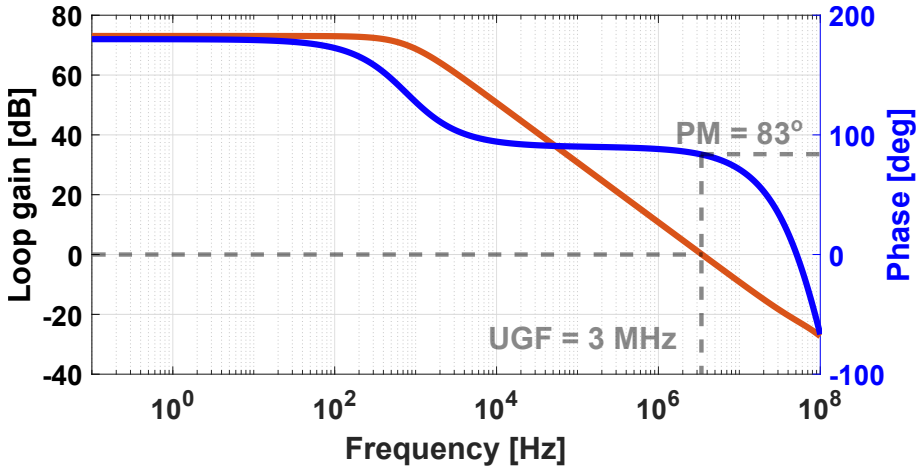

Figure 3.7: The stability of the FDDA in its closed-loop configuration.

3.2 Measurement results

The chip micrograph is shown in Fig. 3.11. It has been manufactured in 180-nm SOI CMOS technology with a total area of 1.85 mm x 1.2 mm. Using a single 1.8-V supply, the chip draws a total current of 7.7 mA, resulting in a total power dissipation of 14 mW. The presented chip has been electrically tested and characterized using a custom-designed evaluation platform, which includes the TMR sensor presented in [47] and shown in Fig. 2.8 with a nominal resistance of 830 Ω and a sensitivity of 93 Ω/mT for a bias current of 1.1 mA. The sensor is mounted on the PCB using an interposer board before connected to our custom-designed readout PCB. For this measurement, the reference resistor is implemented using an ohmic resistor of nominally equal value. Magnetic fields in the sensitive direction of the TMR sensor are generated using custom-designed Helmholtz coils wound around a 3D-printed

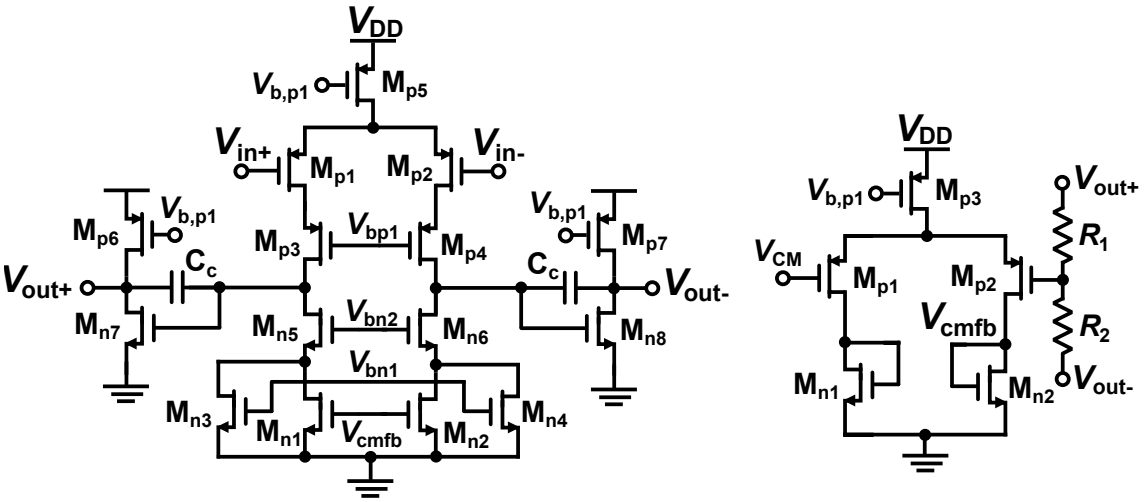

Figure 3.8: Transistor-level schematics of the second stage amplifier as well as its CMFB circuit.

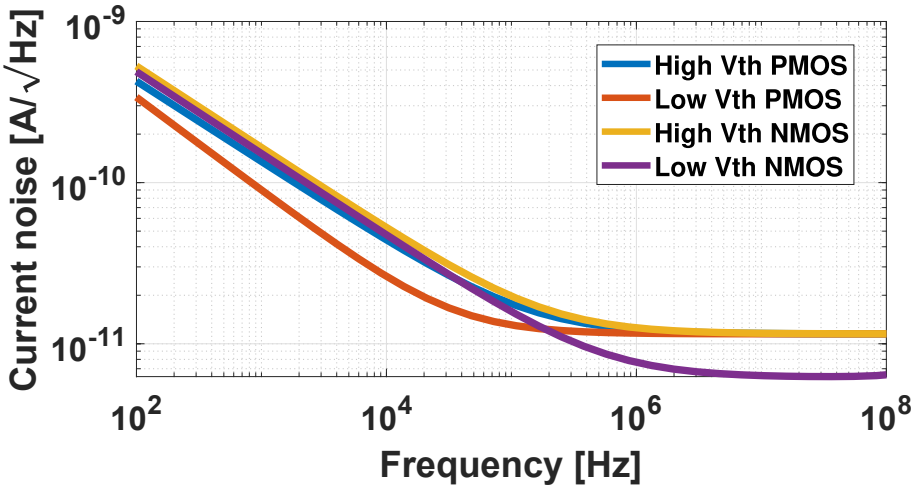

Figure 3.9: Current noise PSDs of low and high threshold voltage NMOS and PMOS transistors.

holder to characterize the TMR element and measure its sensitivity.
To characterize the fabricated chip, we have measured the input-referred noise and the frequency response of the overall system. The corresponding results are shown in Fig. 3.12. The measured 1/f-corner frequency is 7 kHz. The input-referred thermal noise floor of the entire system consisting of the TMR sensor, biased by the ASIC, and the readout electronics is 9.5 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ which corresponds to a limit of detection (LoD) of 300 $\mathrm{pT}/\sqrt{\mathrm{Hz}}$. From the total system noise, we extrapolated an input-referred noise of the chip (biasing and readout) of 7 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. We also characterized the AC response of the chip. The measured AC gain in the passband is 60 dB, including DC. The measured 3 dB bandwidth is 500 kHz with a small peaking around

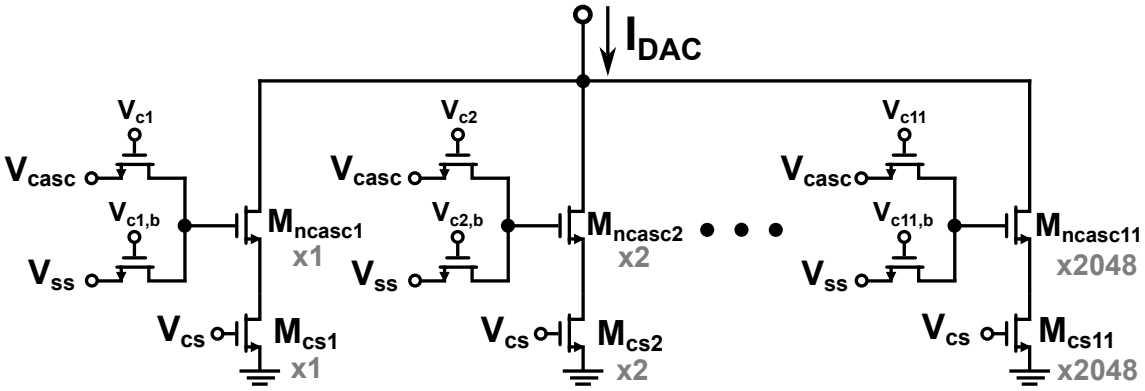

Figure 3.10: Transistor-level schematic of the 11-bit current DAC.

200 kHz of 1 dB. This peaking can easily be compensated in the digital domain. The bandwidth is sufficient to bring the TMR signal outside the 1/f-noise region by field modulation [2]. Moreover, we have evaluated the spurious-free dynamic range (SFDR) of the presented chip by applying test signals of different amplitudes to the input. Fig. 3.14 shows the output spectrum for a maximum input voltage signal with amplitude of 1.35 $\mathrm{mV_{pp}}$ and a frequency of 5 kHz. The measured SFDR is 64 dB and originates from the mismatch of the input differential pairs of the FDDA. Beyond this amplitude, the distortion of the FDDA increases significantly due to the open-loop nature of the input differential pairs. One important feature of the implemented design is its capability to bias largely different sensor resistances. In order to demonstrate this capability, we replaced the TMR by a potentiometer and used a fixed reference resistor with base resistance of 1 kΩ at the second chip input. Fig. 3.13 depicts the output voltage offset of the chip for different input resistances after applying the automatic, on-chip offset calibration routine, cf. Fig. 3.1. According to the figure, the chip can successfully calibrate resistances between 535 Ω and 4.8 kΩ, making the chip compatible with the large process variations of TMR sensors. Finally, we also investigated the stability of the chip over time. This is important to ensure that the system is sufficiently stable to avoid calibrations during biosensing measurements, which can take up to several minutes. According to Fig. 3.13, the chip operates in a stable fashion for at least 30 minutes, which is sufficient for all practical measurement conditions. Here, it is worth mentioning that all experiments have been carried out without any magnetic field shielding.

3.3 Findings of the first generation of chips

The first generation of chips, presented in [5], provides a solid starting point for MR sensor readouts for frequencies in the kHz range. Unfortunately, the higher noise at lower frequencies originating from both the FDDA and the current bias limits the SNR at low frequencies. This is particularly important for neural recording applications where the frequency of interest is from 0.1 Hz up to 15 kHz [48]. On the

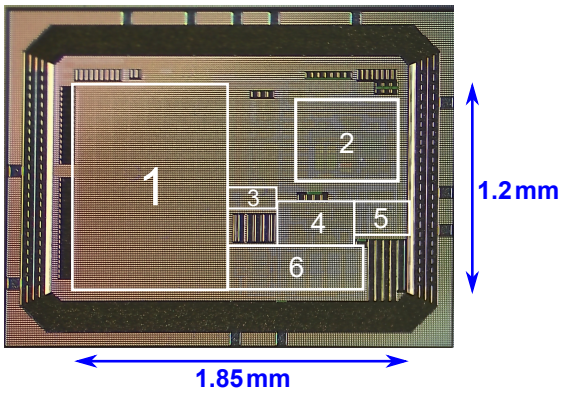

Figure 3.11: Chip micrograph where (1) is the 11-bit DAC, (2) is the FDDA, (3) is the digital control circuity, (4) is the 5-bit DAC, (5) is the second gain stage, and (6) is the biasing of the reference resistor.

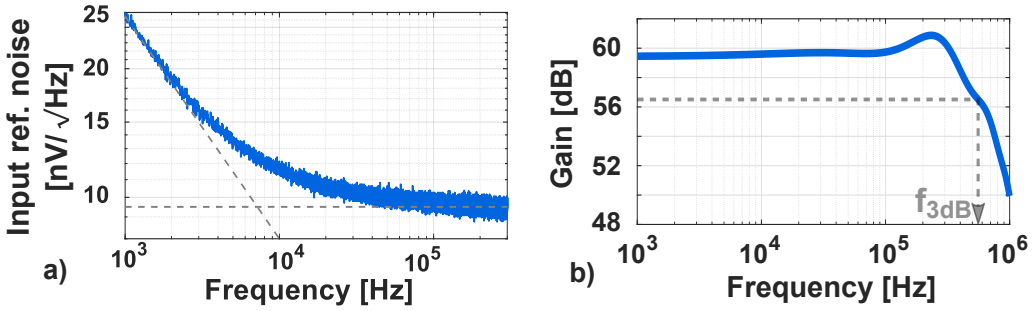

Figure 3.12: a) The measured input-referred voltage noise of the biosensing platform. b) The measured AC response of the IC.

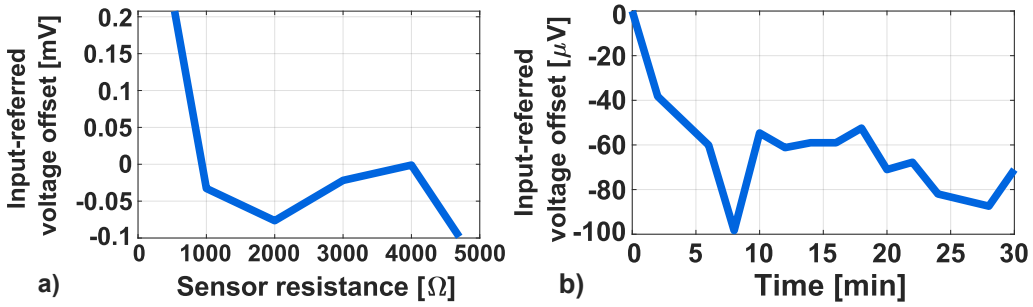

Figure 3.13: a) Input-referred voltage offset of the chip for different offsets between sensing and reference resistors. b) Time stability of the input-referred voltage offset.

other hand, exciting MNTs at high frequencies could shift the signal at frequencies higher than the chip's 1/f-noise for biosensing applications. This comes at the expense of higher power consumption due to the increased coil impedance at higher frequencies. Consequently, reducing the chip's 1/f-corner frequency would result in improved SNR for neural recording applications and lower power consumption for biosensing PoC systems. Reducing the amplifier's 1/f-corner frequency could

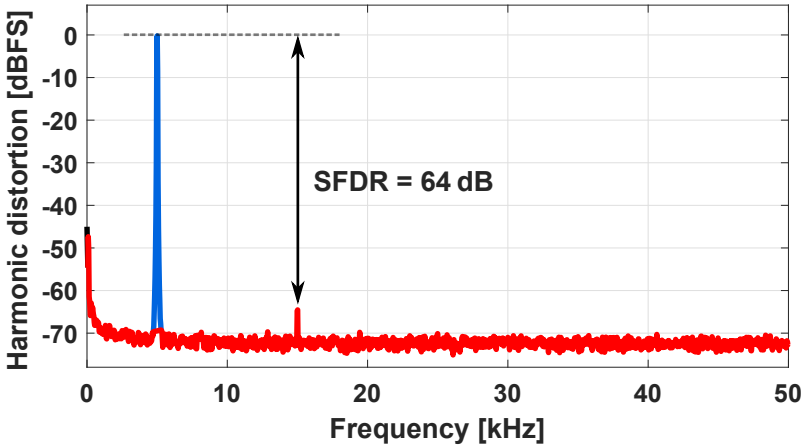

Figure 3.14: The measured chip output distortion for a test signal with an amplitude of 1.35 $\mathrm{mV_{pp}}$ and a frequency of 5 kHz.

be achieved by well-known techniques such as chopping or correlated double sampling [49]. However, reducing the noise, and ultimately 1/f-noise, of current sources is not trivial and the solutions available in SoA designs suffer from some drawbacks that will be discussed in the next sections. On a different note, most biosensing applications require a frontend being able to multiplex an array of MR sensors to perform multiple assays using a single frontend to save area and power. Such requirement mandates a versatile frontend that can either tolerate offsets from each sensor in the array, or alternatively, compensate for the offset of each sensor at a time. The aforementioned chip can only compensate for the offset of one sensor and cannot extend the compensation for an array of sensors since the offset compensation process takes a substantial amount of time, limiting the readout time of an array of sensors. A solution to such problem is to compensate the offsets of each sensor in the array upfront, store the data on-chip and then amplify the sensor's signal while multiplexing the array and load the stored calibration data at the same time, assuming a negligible offset drift. Finally, the first generation of chips features a fixed signal gain of 60 dB which can be a limiting factor for systems with larger signal amplitudes such as in biosensing platforms demanding lower frontend gains, or at least, programmable gain in the frontends.

4 Second generation of readout chips

In order to overcome some of the drawbacks of the first generation of chips and improve their overall noise performance, namely the noise floor and the low frequency noise of the electronics, multiple solutions are investigated in this chapter and a novel technique to reduce the noise of the current bias of MR sensors is introduced. Moreover, different concepts to improve the flexibility of the readout chip to increase its dynamic range and multiplexing capabilities are introduced in the second generation of the voltage-mode chips. More specifically, amendments in the sensor bias and the frontend electronics are introduced in the second generation of chips rendering them more suitable for both neural recording and biosensing applications. We begin this chapter with a brief summary of the implementation of very low noise current sources shown in the literature. Afterwards, we present the architecture of the second generation of chips featuring a novel current bias with very low noise performance and a frontend with an improved 1/f-corner frequency and a programmable gain allowing this chip to be incorporated in both neural recorders and biosensing platforms.

4.1 Towards the design of ultra-low-noise current sources

A simple realization of a current source biasing an MR sensor is shown in Fig 4.1a, where a PMOS transistor biased in saturation is used as a current source. Following the analysis shown in chapter 3, the voltage noise PSD at node V_{R}, $S_{\Delta V_{\mathrm{R}}^2}$, due to the thermal noise of the MR sensor resistance and the current noise PSD of the MOS transistor, $S_{\Delta I_{\mathrm{nD,OL}}^2}$, can be written as follows:

$$S_{\Delta V_{\mathrm{R}}^2} = 4kTR_{\mathrm{s}} + S_{\Delta I_{\mathrm{nD,OL}}^2} \cdot R_{\mathrm{s}}^2, \tag{4.1a}$$

$$S_{\Delta I_{\mathrm{nD,OL}}^2} = 4kT\gamma g_{\mathrm{m}} + \frac{\mathrm{KF} \cdot g_{\mathrm{m}}^2}{C_{\mathrm{ox}} \cdot W \cdot L \cdot f}, \tag{4.1b}$$

where $S_{\Delta I_{\mathrm{nD,OL}}^2}$ is the current noise PSD of M_{CS}, k is the Boltzmann constant, T is absolute temperature, γ is the excess noise factor, g_{m} is the transconductance of transistor M_{CS}, KF is the flicker noise factor, C_{ox} is the oxide capacitance per unit area and W and L are the transistor width and length, respectively. To lower $S_{\Delta I_{\mathrm{nD,OL}}^2}$, one can bias the transistor deeply in strong inversion to lower $g_{\mathrm{m}}/I_{\mathrm{d}}$ where:

$$\frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} = \frac{2}{|V_{\mathrm{ds,sat}}|}. \tag{4.2}$$

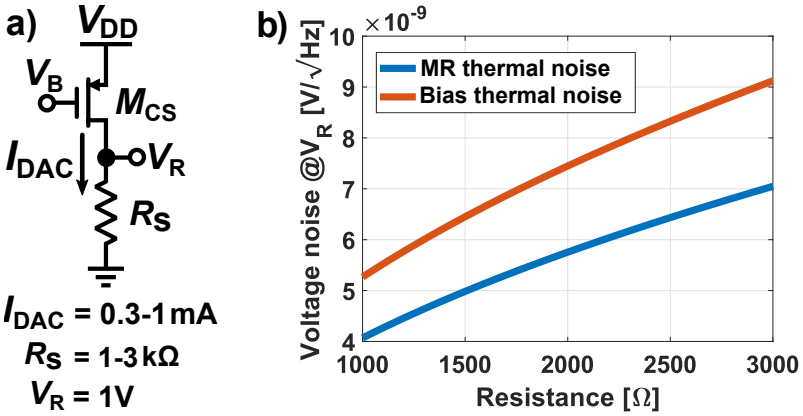

Figure 4.1: a) A simple implementation of a PMOS current source biasing an MR sensor. b) Voltage noise at V_R due to the thermal noise of the MR sensor and the current bias.

However, this approach limits the useful dynamic range of the sensor's output since the required low $g_\mathrm{m}/I_\mathrm{d}$ corresponds to a large $|V_\mathrm{ds,sat}|$, and a lower voltage overhead is available across the sensor terminals. The best-case achievable thermal and flicker noise floor depends largely on $|V_\mathrm{ds,sat}|$ which is strongly correlated with the supply voltage V_DD of the current source. In this work, we have $V_\mathrm{DD} = 1.8\,\mathrm{V}$, I_DAC has to be adjusted between 0.3 mA and 1 mA to be able to bias an MR sensor resistance of $3\,\mathrm{k\Omega}$ down to $1\,\mathrm{k\Omega}$ setting V_R to 1 V. This leaves a maximum $|V_\mathrm{ds,sat}|$ of 0.8 V for the current source. Ignoring flicker noise of the PMOS transistor, the theoretical voltage noise floor due to the MR sensor resistance and the current bias using $|V_\mathrm{ds,sat}| = 0.8\,\mathrm{V}$, according to eq. (4.1a) is shown in Fig. 4.1. Unfortunately, the best-case noise floor of the current bias is still higher than the noise floor of the MR sensor, and hence, the intrinsic SNR of the MR sensor is degraded due the current bias despite using a very large $V_\mathrm{ds,sat}$. A simple way to reduce the current noise of a current source is using source degeneration to reduce the effective transconductance G_m [50] in the following manner:

$$G_\mathrm{m} = \frac{g_\mathrm{m}}{1 + g_\mathrm{m} \cdot R_\mathrm{deg}}, \tag{4.3}$$

where R_deg is the degeneration resistance added at the source of the current source transistor. Despite the simplicity of a source degenerated transistor, it cannot be simply scaled in a high resolution DAC with very small current steps due to the large DAC footprint associated with large resistors for small currents. As an alternative, multiple designs, cf. [43, 40, 36] configure the source degenerated current source transistor in a voltage feedback loop allowing to adjust the current by V_B and R_deg. Ultimately, the current noise PSD of the MOS device is attenuated by the large voltage loop gain of the design. Fig. 4.2 shows the basic architecture used in the aforementioned designs for a current source embedded in a voltage feedback loop. The total PSD of the aforementioned closed-loop design can be written as follows:

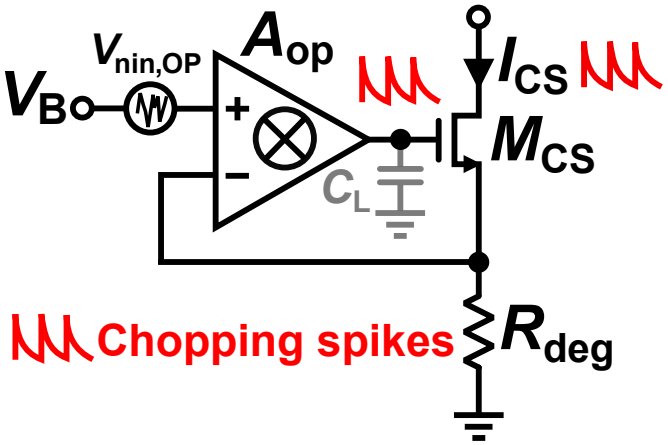

Figure 4.2: A current source embedded in a voltage feedback loop to lower its noise.

$$S_{\Delta I^2_{\mathrm{nD,CL}}} = \frac{S_{\Delta I^2_{\mathrm{nD,OL}}}}{A^2_{\mathrm{op}}} + \frac{S_{\Delta V^2_{\mathrm{nin,OP}}}}{R^2_{\mathrm{deg}}} + \frac{4kT}{R_{\mathrm{deg}}}, \tag{4.4}$$

where $S_{\Delta V^2_{\mathrm{nin,OP}}}$ is the input-referred voltage noise PSD of the amplifier. Clearly, the noise of the current source can be significantly attenuated by the open-loop gain of the amplifier. However, $S_{\Delta V^2_{\mathrm{nin,OP}}}$ is translated to the output current noise PSD by R_{deg} without further attenuation. By only considering the noise of the input differential pair of the opamp and ignoring the rest of the noise contributors, $S_{\Delta V^2_{\mathrm{nin,OP}}}$ can be expressed as follows:

$$S_{\Delta V^2_{\mathrm{nin,OP}}} = 2\left[\frac{4kT\gamma}{g_{\mathrm{m,in}}} + \frac{\mathrm{KF}}{C_{\mathrm{ox}} \cdot W_{\mathrm{in}} \cdot L_{\mathrm{in}} \cdot f}\right]. \tag{4.5}$$

The first summand of eq. (4.5) represents the thermal noise contribution of the input differential pair while the second summand models its flicker noise. To reduce the thermal noise floor of the opamp, $g_{\mathrm{m,in}}$ can be increased by biasing the input pair in weak inversion or by increasing the current in the input stage. On the other hand, flicker noise can be reduced by chopping the amplifier, cf. Fig. 4.2. This increases the complexity of the design by adding chopping switches and increasing the voltage spikes at the output of the amplifier, and consequently, disturbing the current bias as illustrated in Fig. 4.2. These drawbacks of increased power consumption and the extra chopping in the current bias present a bottleneck for such designs targeting very low noise floors. In [40, 36, 43], the thermal noise floor of the current bias is limited to $10\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. This high noise floor would degrade the intrinsic SNR of the MR sensors. For example, a $1\,\mathrm{k\Omega}$ MR sensor resistor would have a thermal noise floor of $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while $10\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ would contribute to a significantly higher voltage noise floor of $10\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ which is much higher compared to the noise floor of the MR sensor. As a result, we introduced a novel solution to improve the noise suppression of the current bias and preserve the intrinsic SNR of the MR sensor.

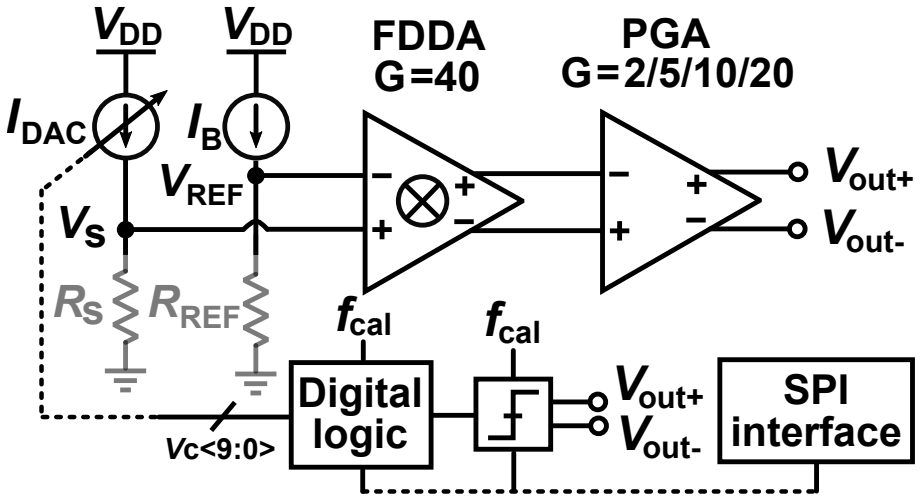

Figure 4.3: System level block diagram of the readout chip.

4.2 Second generation of chips: design and implementation

In chapter 3, the first generation of voltage readout chips were presented, and their drawbacks have been highlighted, namely, the high noise floor of the current bias as well as the high low-frequency noise originating from the readout chain. Moreover, we have established that a programmable gain in the frontend would improve the flexibility of the readout electronics to handle different sensors with wider dynamic ranges. This can be controlled by a standard interface, such as an SPI interface, facilitating the choice of different voltage gains as well as initiating the auto-calibration routine needed to compensate for the MR sensor resistance offsets. We tackle the aforementioned drawbacks in the second generation of chips by adopting multiple design changes.

Fig. 4.3 shows the block diagram of the presented readout ASIC, consisting of the current bias of the sensor and the subsequent voltage amplifiers. An on-chip fixed current source and an adjustable current DAC bias the reference resistor and the MR sensor, respectively. This differential readout scheme improves the baseline-to-signal-ratio [40]. Similar to the first generation of chips, the compensation of the offset between the sensor and the reference resistor is achieved by continuously monitoring the difference between the MR and the reference resistor output voltages using a DC-coupled readout circuit formed by an FDDA and a programmable gain amplifier (PGA), which feeds a dynamic comparator followed by a digital logic that finds the DAC digital codeword necessary to compensate the offset. The automatic compensation routine is triggered via an on-chip SPI interface.

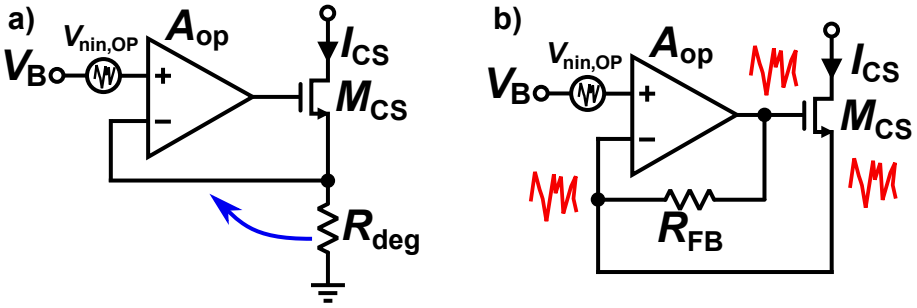

Figure 4.4: a) Block diagram of the opamp based current source. b) Simplified version of the proposed low-noise TIA-based current source as well as the intrinsic noise suppression of the embedded opamp.

4.2.1 An ulta-low-noise current bias

The design depicted in Fig. 4.2 shows a promising solution to lower the noise of a current bias. However, as explained in the previous section, the best reported noise of the shown design is limited to $10\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The bottleneck of this design stems from the noise of the internal amplifier. We propose a simple adjustment of the aforementioned design as shown in Fig. 4.4 where we moved the degeneration resistance R_{deg} to the feedback of the amplifier. This way, the voltage-mode feedback, cf. Fig. 4.4a, is turned into a transimpedance amplifier (TIA) structure, cf. Fig. 4.4b. Although the introduced modification might seem simple and does not change the core idea of the current bias, the performance of the current bias is altered heavily. First of all, the voltage gain across the TIA is unity (ignoring the input capacitance of the TIA). This means that the input-referred voltage noise of the TIA is copied to its output, and the effective small signal gate-source voltage $|v_{\mathrm{gs}}|$ of transistor M_{CS} is zero due to the noise of the TIA. As a result, the noise of the amplifier embedded in the loop is nulled by the TIA feedback topology. On the other hand, the noise of the current source M_{CS} is only attenuated by the loop gain being $g_{\mathrm{m}} \cdot R_{\mathrm{FB}}$ compared to A_{DC} for the case in Fig. 4.4a. In this proposed structure, chopping around the amplifier is not needed, and hence, all the drawbacks observed from chopping the amplifier are mitigated. This small adjustment presents an effective and simple solution to lower the noise of the current source.

Current DAC design

While Fig. 4.4b shows the general idea of the proposed architecture, it does not show the complete picture of its actual implementation. Fig. 4.5 shows the actual implementation of the proposed current DAC with the TIA-based feedback loop. The DC current of the current source M_{CS} is set by its gate-source voltage and its W and L. According to Fig. 4.4b, the source voltage of the current bias is defined by the virtual short of the opamp, and the source voltage of the transistor M_{CS} is set to $V_{\mathrm{b,s}}$. However, the gate voltage cannot be controlled by the TIA feedback

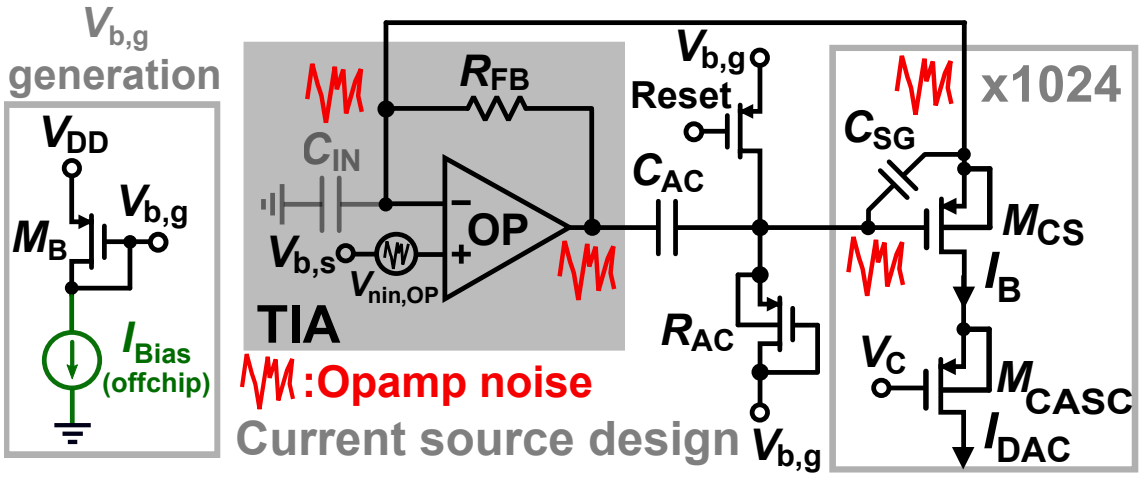

Figure 4.5: Block diagram of the proposed TIA-based low-noise current-mode DAC.

loop since the gate-voltage would be completely dependent on the current flowing through the feedback resistor and set to $V_{b,s} - (I_{CS} \cdot R_{FB})$. To set the gate voltage to a well-defined potential, an AC coupling network is integrated in the feedback loop as shown in Fig. 4.5 acting as a high-pass filter or an AC-coupling network blocking the DC component from the TIA. Afterwards, the gate bias voltage $V_{b,g}$ is generated by a diode connected PMOS transistor, which is embedded into the current DAC to provide a PVT stable current mirror type biasing for M_{CS}. By setting the corner frequency of the AC coupling network f_{hpf} low enough, the loop gain remains unaltered at frequencies higher than the corner frequency and the gate voltage of transistor M_{CS} can be defined by the voltage $V_{b,g}$ through the pseudoresistor R_{AC}. The choice of C_{AC} is important for multiple reasons. First, a large C_{AC} would reduce the high-pass corner frequency f_{hpf} as needed, and consequently, increase the loop gain at low frequencies. Secondly, C_{AC} forms a voltage divider between the output of the opamp and the gate voltage of transistor M_{CS}. This voltage divider effectively lowers the loop gain due to the attenuation of the voltage signal at the output of the opamp. Moreover, the output voltage of the opamp would not be copied to the gate voltage of transistor M_{CS} which effectively would not allow for canceling of the noise of the opamp, because the small-signal v_{sg} due to the noise of the opamp will not be zero anymore. On a different note, a reset switch is added to the gate of the transistor M_{CS} to reset this high impedance node if necessary.
In order to implement the desired 10-bit DAC, a unit DAC element with a dimension of $W/L = 1\,\mu m/1\,\mu m$ is chosen with $|V_{ds,sat}| = 150\,mV$ to output a unit current of $1\,\mu A$. By connecting 1024 DAC unit elements in parallel, a total output current of $1\,mA$ can be obtained. The open-loop current noise PSD of this transistor is simulated in Fig. 4.6 (blue) showing a high noise floor of $11\,pA/\sqrt{Hz}$ for a total current of $1\,mA$. Interestingly, the open-loop noise current PSD is on par with the measured noise floor of the designs shown in [43, 40, 36]. A simulated $g_m = 10\,mS$ is obtained for the low threshold PMOS transistor with a gate-source capacitance of

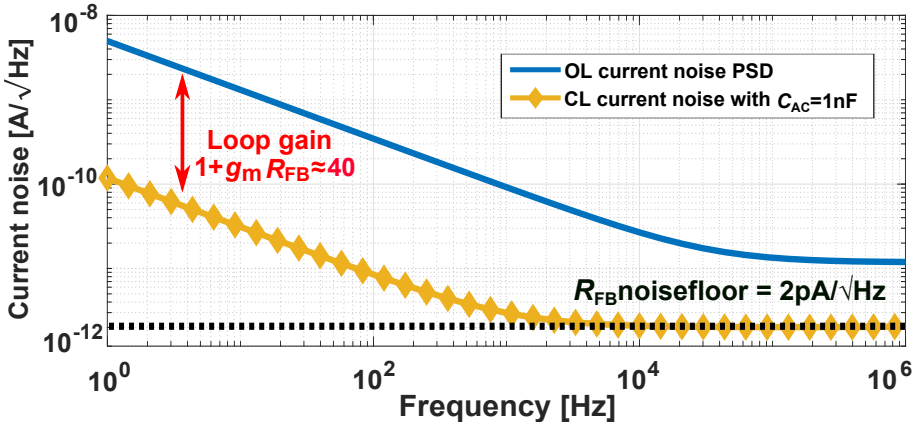

Figure 4.6: Simulated current noise PSD of the proposed closed-loop (CL) bias compared to the open-loop (OL) system.

$C_{SG} = 6.4\,\text{pF}$ and $g_{ds} = 100\,\mu\text{S}$. The aforementioned transistor flavor is chosen due to its superior flicker noise performance, cf. Fig. 3.9. Although the chosen transistor shows a higher noise floor compared to the low threshold NMOS transistor, the noise floor is set by the feedback resistance R_{FB} irrespective of the noise floor of the different current sources. To maximize the noise suppression of the current source, a larger feedback resistance is desired. However, the choice of R_{FB} is limited by the headroom requirements in the TIA since the output voltage of the TIA would be set by the current bias and R_{FB}. In this design, two flavors of transistors with 1.8 V core devices and 5 V I/O devices are available in the technology portfolio and hence a large $R_{FB} = 4\,\text{k}\Omega$ is chosen providing a maximum voltage swing at the output of the TIA of $\approx 4\,\text{V}$ for a maximum $I_{DAC} = 1\,\text{mA}$. Although the 5 V I/O devices are not optimized for low noise operation, their noise is nulled at the output of the current bias due to the inherent noise cancellation of the opamp noise as illustrated in Fig. 4.5. By using an $R_{FB} = 4\,\text{k}\Omega$, $R_{AC} = 10\,\text{G}\Omega$ and a very large $C_{AC} = 1\,\text{nF}$ to examine the best-case noise performance of the proposed system, the simulated closed-loop current noise is shown in Fig. 4.6 (yellow). As highlighted in the figure, the CL performance is improved by the loop gain $1 + g_m R_{FB}$, or 40x for this design, compared to the open-loop response. The noise floor is set by R_{FB} and is equal to $2\,\text{pA}/\sqrt{\text{Hz}}$. Fig. 4.6, however, gives a simplified view of the noise of the current bias. The complete noise analysis of the current noise should also include the effect of the capacitive divider, namely between C_{AC} and C_{SG}, as well as the finite channel conductance of transistor M_{CS}. As illustrated in Fig. 4.5, the small-signal v_{sg} is close to zero, however, the small signal v_{sd} is non-zero. As a result, the finite output conductance g_{ds} would lead to non-zero noise at the output of the current bias due to the opamp's noise. A simple model shown in Fig. 4.7 is implemented in the Cadence design environment to simulate the aforementioned second-order effects. The ideal model simplifies the current source M_{CS} as a voltage controlled current source (VCCS) and its g_m sets the small-signal current gain. On the other hand, the large

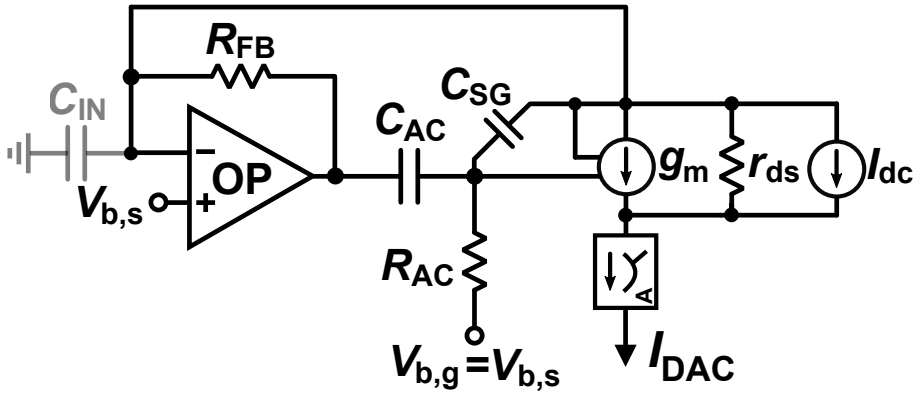

Figure 4.7: Block diagram of the proposed current bias using ideal components from the analogLib.

signal current I_{DC} is set with an ideal current source. The small-signal conductance, modeling the CLM effect, is taken into consideration by adding a resistor in parallel with a current source with a value of r_{ds}. Accounting for these effects, the resulting output current noise PSD of the proposed current bias is given by:

$$\begin{aligned} S_{\Delta I^2_{\mathrm{nD,CL}}} \approx & \frac{S_{\Delta I^2_{\mathrm{nD,OL}}}}{(1+g_{\mathrm{m}}R_{\mathrm{FB}}x_{\mathrm{div}})^2} + \frac{4kT}{R_{\mathrm{FB}}} \\ & + \left[S_{\Delta V^2_{\mathrm{nin,OP}}} + S_{\Delta V^2_{\mathrm{b,s}}}\right] \left[\frac{g_{\mathrm{ds}} - j\omega g_{\mathrm{m}} R_{\mathrm{FB}} C_{\mathrm{in}} x_{\mathrm{div}}}{1+g_{\mathrm{m}}R_{\mathrm{FB}}x_{\mathrm{div}}}\right]^2 \\ & + S_{\Delta V^2_{\mathrm{b,g}}} \left[\frac{g_{\mathrm{m}}}{1+j\omega R_{\mathrm{AC}}C_{\mathrm{AC}}\left(1+g_{\mathrm{m}}R_{\mathrm{FB}}\right)}\right]^2, \end{aligned} \tag{4.6}$$

where $x_{\mathrm{div}} = C_{\mathrm{AC}}/\left(C_{\mathrm{AC}} + C_{\mathrm{SG}}\right)$ and C_{IN} is the opamp input capacitance. Here, it is important to point out that, in contrast to the open-loop case, increasing g_{m} improves the overall noise performance by increasing the loop gain, cf. eq. (4.1). Hence, the scheme of Fig. 4.4b favors an operation of transistor M_{CS} in weak inversion, drastically reducing the headroom requirements for the current source. According to eq. (4.6), finite channel conductance g_{ds}, non-zero C_{IN} as well as finite C_{AC} lowers the attenuation of the noise of the current bias. Although using a very large C_{AC} combined with a long transistor to keep g_{ds} as low as possible, provided that $C_{\mathrm{AC}} \gg C_{\mathrm{SG}}$, would be optimum for noise performance, the chip area would be significantly large. As a result, C_{AC} is chosen as 20 pF. It is worth mentioning that the source and gate bias noise voltages can be made negligible by adding simple low-pass filters using area-efficient pseudoresistors and MOS capacitors, for example. It is also important to investigate the effect of the finite C_{AC} on the noise suppression of the current bias. Fig. 4.9 shows the simulated transfer function of the OL current noise to the total output of the current bias. For a large $C_{\mathrm{AC}} = 1\,\mathrm{nF}$, the noise is scaled by 24.5 mA/A matching the inverse of the loop gain of $(1+g_{\mathrm{m}}R_{\mathrm{FB}})^{-1} \approx 1/40 \approx 25\,\mathrm{mA/A}$. On the other hand, the noise suppres-

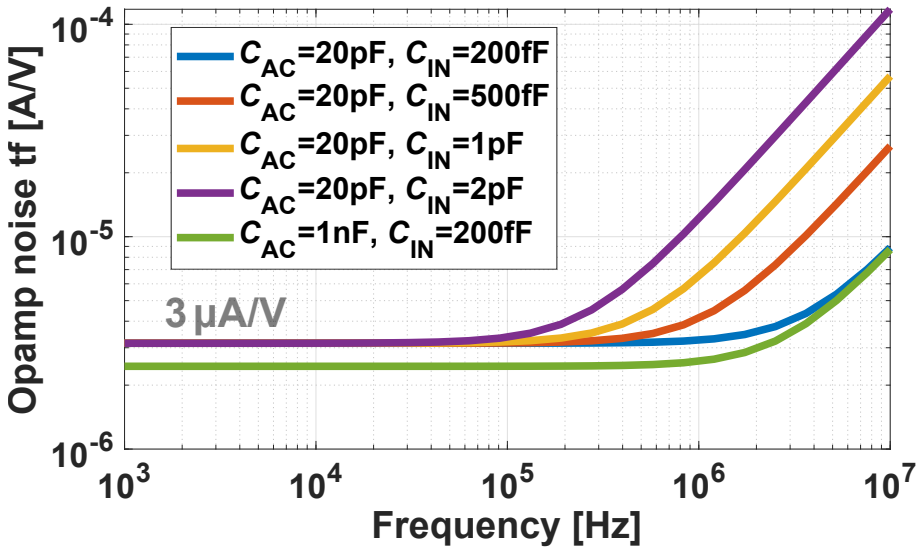

Figure 4.8: Simulated transfer function from the input-referred voltage noise of the embedded opamp to the output current.

sion of the current bias is worsened from 24.5 mA/A to 28 mA/A due to a lower $C_{\mathrm{AC}} = 20\,\mathrm{pF}$, cf. the factor x_{div} in eq (4.6).

Embedded opamp noise

It is also important to investigate the embedded opamp noise performance on the total output noise. The transfer function of the input-referred noise of the opamp to the output current is simulated in Fig. 4.8 for different C_{IN} values. The simulated output noise due to the opamp noise is high-pass shaped due to C_{IN}. Moreover, a larger C_{IN} shifts the high-pass corner frequency to the left, or smaller frequencies, as shown in eq. (4.6). Furthermore, increasing C_{AC} to a very large, yet impractical, value of $C_{\mathrm{AC}} = 1\,\mathrm{nF}$, and hence increasing x_{div} to unity, cf. eq. (4.6), lowers the noise floor further. It is important to quantify the noise requirements of the embedded opamp to achieve a current noise floor lower than the noise floor of the feedback resistance $R_{\mathrm{FB}} = 4\,\mathrm{k\Omega}$. An output noise contribution from the opamp around $0.5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ compared to a noise floor of $2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ originating from R_{FB} would render the opamp noise negligible. Since the opamp contributes $\approx 3\,\mu\mathrm{A/V}$, cf. Fig. 4.8, a minimum input-referred voltage noise of $170\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is needed to obtain a maximum output noise of $0.5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. To specify the power requirements of the opamp, the relationship between the input-referred voltage noise of the opamp and the transconductance of the input differential pair is used, cf. the first summand of eq. (4.5). For an input-referred voltage noise of $170\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, a minimum input transconductance of $g_{\mathrm{m,in}} = 770\,\mathrm{nS}$ is needed. The required bias current would then depend on the chosen bias point. Even in worse cases where $g_{\mathrm{m}}/I_{\mathrm{d}}$ is as low as one, where the power efficiency of the opamp is not optimized, an opamp bias current of around $I_{\mathrm{b,OP}} = 2 \cdot 770\,\mathrm{nA} \approx 1.6\,\mu\mathrm{A}$ would be required. Clearly, the opamp bias cur-

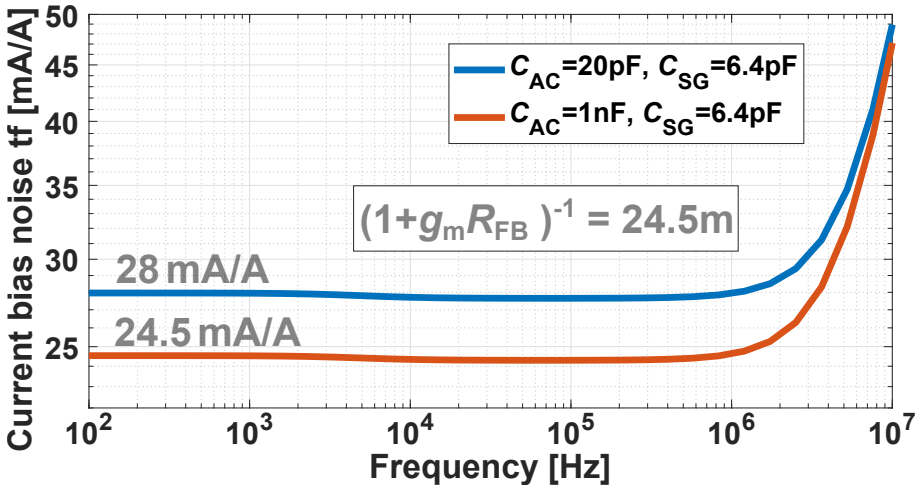

Figure 4.9: Simulated transfer function from the OL current bias noise to the output current noise.

rent, and hence power, is much lower compared to the sensor bias current of 1 mA. The implemented current source can provide currents up to 1 mA to maximize the MR output signal. Since the utilized MR sensors provide base resistances between 1 kΩ and 3 kΩ, a larger feedback resistor in the TIA of the bias control loop of 4 kΩ is needed to provide a noise floor below that of the MR sensor. To accommodate the maximum voltage drop of ≈ 4 V across R_{FB}, we used shifted power supplies between $V_{\mathrm{SS}} = 1.8\,\mathrm{V}$ and $V_{\mathrm{VDD,L}} = 3.6\,\mathrm{V}$ inside the biasing circuitry, as also shown in Fig. 4.10. This allowed implementing the input stage of the TIA opamp using core 1.8 V devices and lower the overall power consumption by lowering the supply voltage of the input stage. To this end, only the opamp's output stage has to use 5 V I/O devices supplied from a supply between $V_{\mathrm{SS}} = 1.8\,\mathrm{V}$ and $V_{\mathrm{DD,H}} = 6.8\,\mathrm{V}$. Consequently, no additional biasing network is needed for the readout chain. It is worth mentioning that the proposed biasing scheme can also be accommodated with a single supply when using smaller values of R_{FB} at the expense of increased noise floors. Moreover, the entire TIA can be implemented using the 5 V I/O devices at the expense of higher power consumption. The transistor-level model of the embedded opamp is shown in Fig. 4.11 where the low-voltage stage of the amplifier is a standard two-stage folded cascode amplifier with a PMOS input differential pair for lower 1/f-noise and Miller capacitance to compensate for the two-pole system. The high-voltage amplifier stage is a simple NMOS common-source amplifier with an active current source load. Overall, the three-stage nested Miller amplifier provides a large gain to precisely control the source bias of the MR sensor current source via the virtual ground. The noise of the opamp shown in Fig. 4.11 is simulated with and without activating the reset switch, cf. Fig. 4.5. The reset switch is implemented for multiple reasons. First, the reset is turned on if the potential of the high impedance node, at the gate of the transistor M_{CS}, is charged to a different potential due to parasitic coupling for example. Moreover, during the auto-calibration phase of the

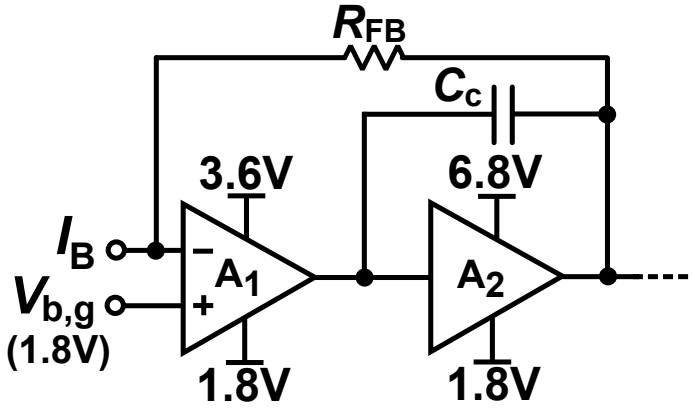

Figure 4.10: Block diagram of the embedded TIA.

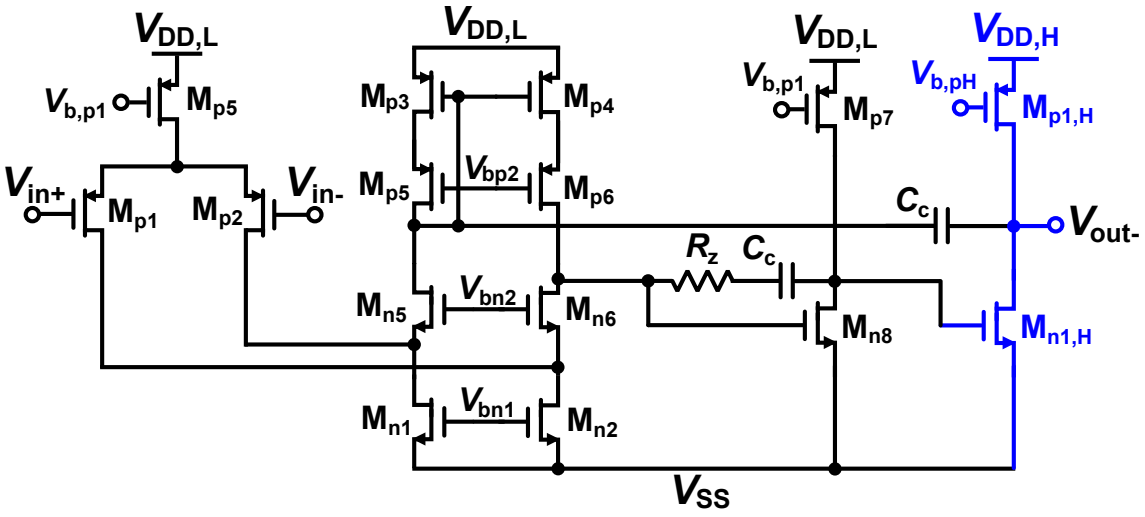

Figure 4.11: Block diagram of the embedded TIA. The high-voltage transistors are shown in blue.

MR sensor, the reset switch is turned on until the calibration is complete. The reason is because while turning on and off the unit DAC elements of the current source, the high impedance node at the gate of transistor M_{CS} is disrupted by the switching effect and have to be either constantly reset during calibration or kept at a low impedance as we propose in this design. More importantly, noise simulations in Fig. 4.12 show that the opamp noise is kept well below the intrinsic noise generated by R_{FB}. The largest noise contribution from the opamp originates from the flicker noise of transistors M_{n1} and M_{n2}. Moreover, the noise of the opamp is increased by around four orders of magnitude when the reset switch is on. This is because the intrinsic cancellation of the opamp noise is not valid anymore since the cut-off frequency of the AC coupling network formed by R_{AC} and C_{AC} is shifted to much higher frequencies when the reset switch is activated. The overall simulated noise of the transistor-level current DAC design is shown in Fig. 4.13. It is worth men-

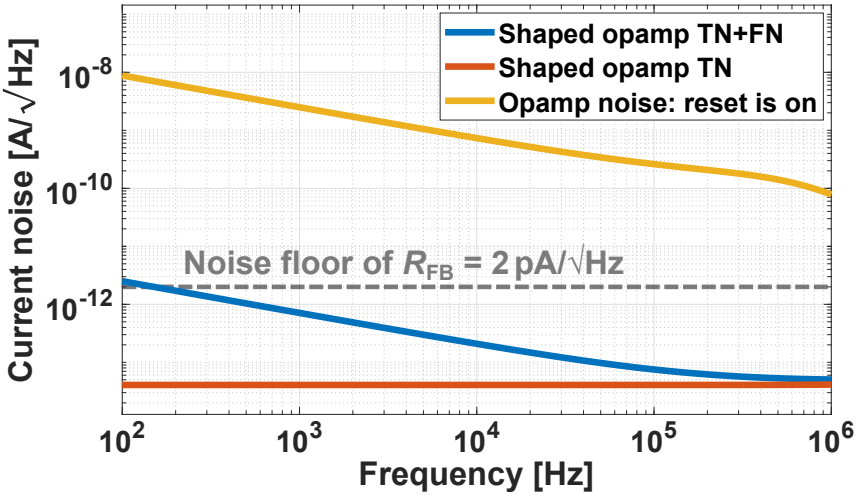

Figure 4.12: Simulated noise of the embedded opamp with and without activating the loop.

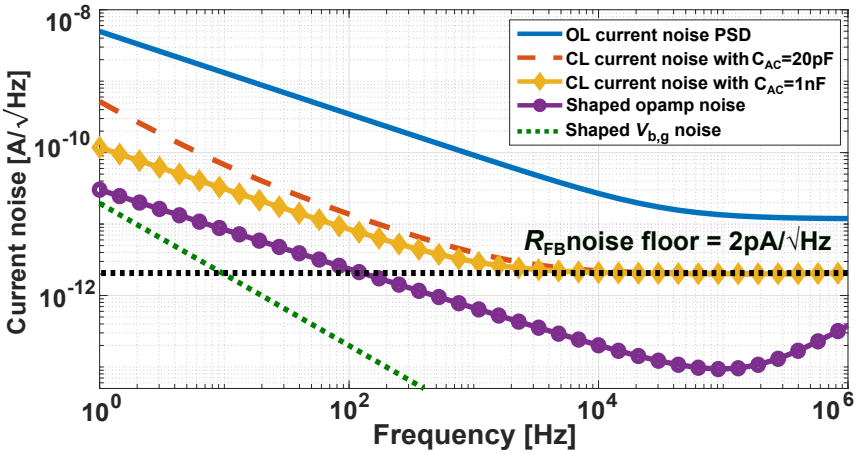

Figure 4.13: Simulated noise of the current bias.

tioning that the simulated opamp noise is higher compared to the simulation shown in Fig. 4.12 due to the smaller $C_{\mathrm{AC}} = 20\,\mathrm{pF}$, yet still lower by around one order of magnitude compared to the CL current bias noise. Finally, assuming a fairly large bias voltage noise of $S_{\Delta V_{\mathrm{b,g}}} = 100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, for frequencies above 1 Hz, the resulting current noise is still negligible.

4.2.2 Frontend design

According to Fig. 4.3, the low-noise bias current I_{DAC} flows through the MR sensor and produces a voltage signal which is subsequently amplified by an FDDA followed by a PGA. The advantages of the FDDA compared to a CCIA and a classic non-inverting amplifier are explained in details in chapter 3. In the presented design, the FDDA has a fixed gain of 40 and the PGA features four different gain settings

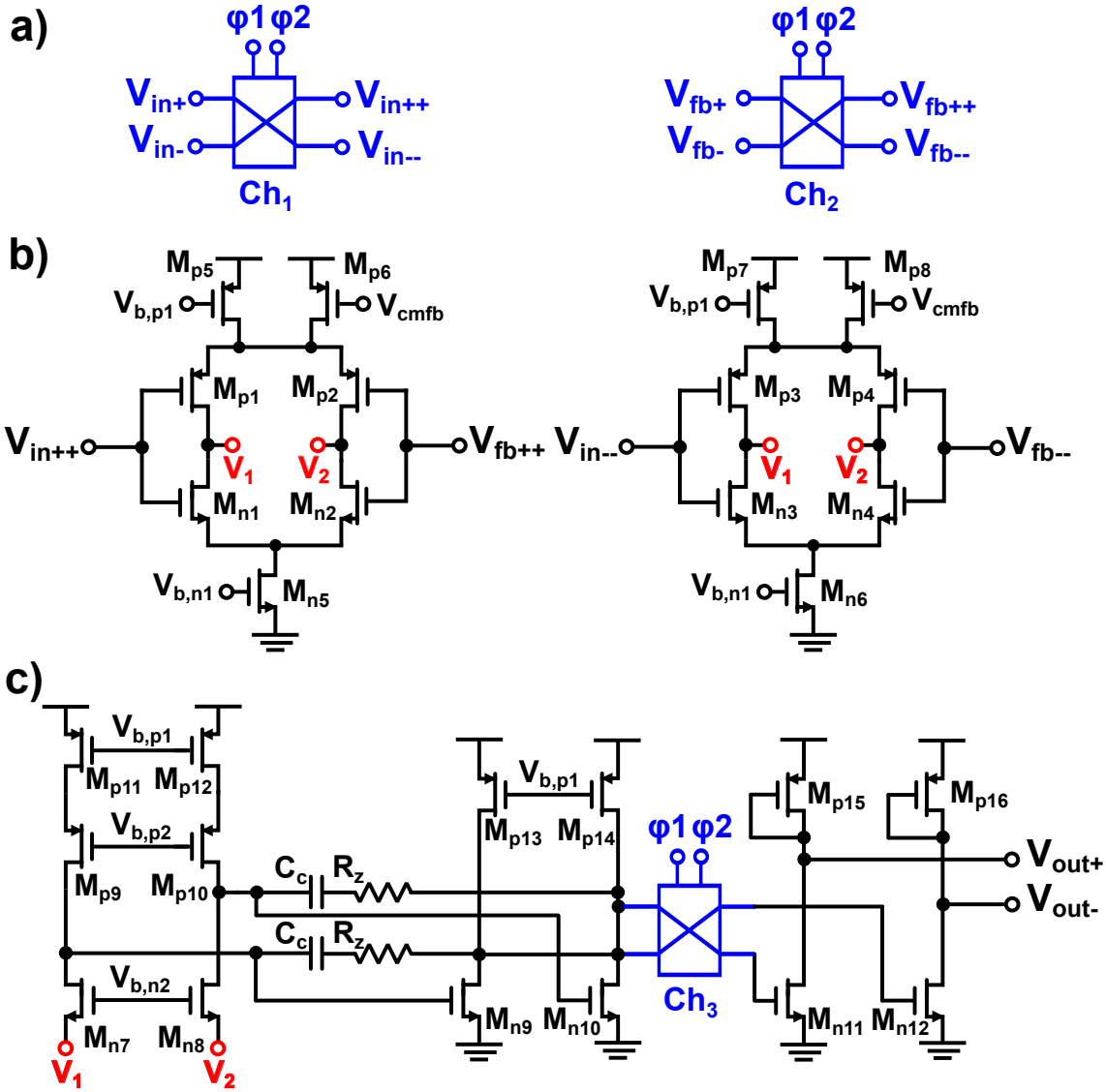

Figure 4.14: Transistor-level block diagram of the FDDA where a) shows a block diagram of the input choppers, b) is the transistor-level model of the input stage of the FDDA, and c) shows the rest of the FDDA design.

to accommodate different dynamic range requirements. Since the FDDA is directly interfacing the MR sensor, special care for its noise performance is taken into consideration. Fig. 4.14 shows the transistor-level model of the designed FDDA alongside with the chopping switches. Although the FDDA design is similar to that of the first generation of chips, cf. chapter 3, it is further optimized for an improved flicker noise behavior. In order to lower the power consumption of the FDDA while maintaining a good noise performance, the input differential pairs are implemented using stacked PMOS and NMOS pairs [51]. As a result, the overall transconductance is increased without changing the bias current. To achieve a better flicker noise per-

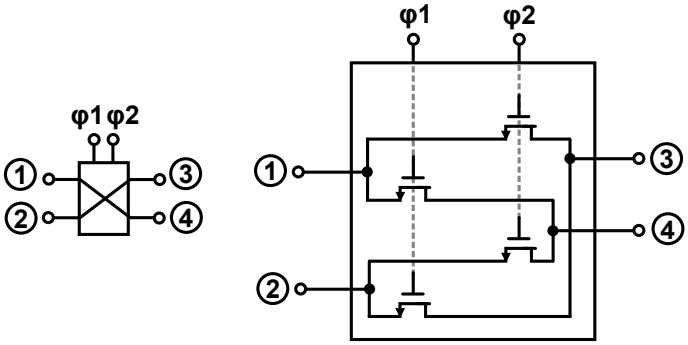

Figure 4.15: Transistor-level model of the chopper.

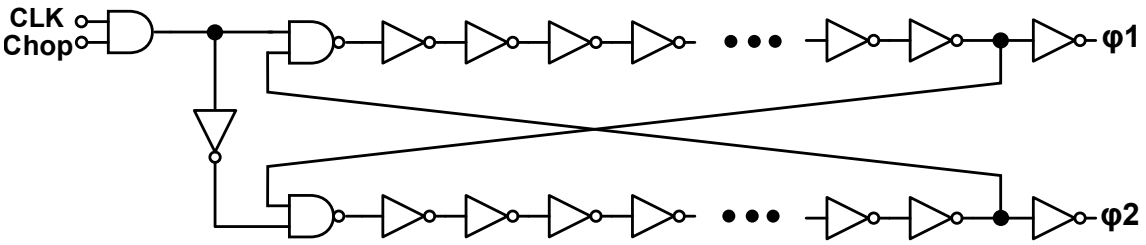

Figure 4.16: Non-overlapping clocks generator.

formance, chopping switches are incorporated to modulate the signal away from the noise-critical low-frequency region [49]. The most noise-critical transistors in the FDDA are the input differential pairs, namely $M_{\mathrm{n,p1-4}}$ as well as the current sources $M_{\mathrm{p11,12}}$, cf. Fig. 4.14. The input choppers, CH_1 and CH_2, are placed normally at the gate terminal of the input differential pairs. Traditionally, the output choppers can be placed at the source of transistors $M_{\mathrm{n7,8}}$ as well as $M_{\mathrm{p11,12}}$ [52], however, these choppers would have to have low on-resistance, R_{on}, to lower the voltage drop across them. In this design, the output choppers are placed at the input of the output stage. In this way, the choppers only have to to drive small gate capacitances of transistors M_{n11} and M_{n12}. The choppers are built using four NMOS switches as shown in Fig. 4.15. The NMOS transistors are favored to PMOS transistors due to their larger mobility, and hence, lower R_{on} for the same aspect ratio. The generation of the clocks needed for the choppers is achieved using a simple non-overlapping clock generator shown in Fig. 4.16. In this way, both clocks ϕ_1 and ϕ_2 are generated using a single off-chip clock source. Moreover, an extra AND gate is added at the input of the non-overlapping clock generator to switch off the network if chopping is not needed. The control signal is set through the on-chip SPI interface, cf. Fig. 4.3, and used to measure and compare the performance of the chopped against the unchopped design. The simulated input-referred voltage noise of the FDDA is shown in Fig. 4.17 (blue). The simulated noise floor of the unchopped FDDA is $2.7\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while the 1/f-corner frequency is located at around $f_{\mathrm{fl}} = 60\,\mathrm{kHz}$. Choosing an appropriate chopping frequency depends mainly on the 1/f-corner frequency and the 3-dB corner frequency of the amplifier $f_{3-\mathrm{dB}}$ [49]. On the one hand, choosing a

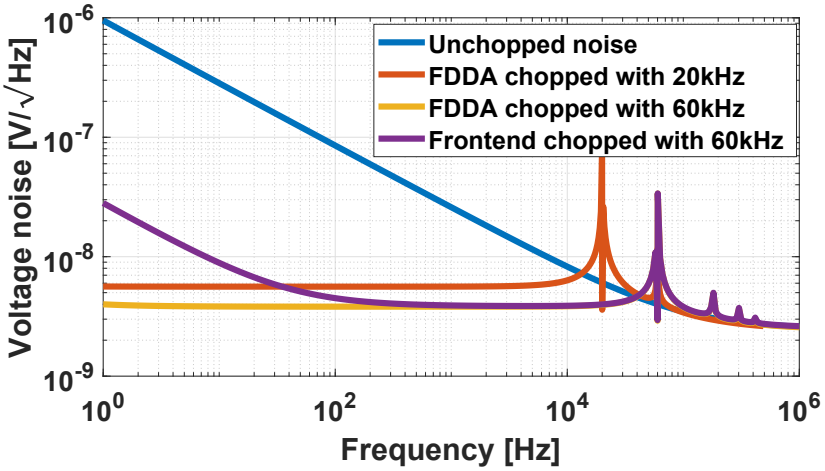

Figure 4.17: Simulated input-referred noise of the standalone chopped and unchopped FDDA as well as the input-referred noise of the chopped frontend.

chopping frequency $f_{\mathrm{ch}} \ll f_{3-\mathrm{dB}}$ leads to a suboptimal reduction in the 1/f-noise while, favorably, keeping the white noise floor unaltered. On the other hand, choosing $f_{\mathrm{ch}} \gg f_{\mathrm{fl}}$ leads to better cancellation of the 1/f-noise while increasing the white noise floor due to noise folding caused by the finite GBW of the opamp. Simulations show that a chopping frequency of $f_{\mathrm{ch}} = 60\,\mathrm{kHz}$ achieves good rejection of the the 1/f-noise. The simulated input-referred voltage noise of the chopped FDDA with a chopping frequency of $f_{\mathrm{ch}} = 60\,\mathrm{kHz}$ is shown in Fig. 4.17 (yellow) where the 1/f-corner frequency is very small and the noise floor is only marginally increased to $3.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. To relax the constraints on the speed of the chopping switches, a lower chopping frequency f_{ch} can be an alternative design choice. To illustrate the effect of lowering f_{ch}, the input-referred voltage noise is simulated with $f_{\mathrm{ch}} = 20\,\mathrm{kHz}$ showing an increase of the noise floor to $5.6\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Since the minimum intrinsic noise floor of the MR sensor is set by the lower base resistance of $1\,\mathrm{k\Omega}$ and a noise floor of $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, a chopping frequency of $f_{\mathrm{ch}} = 60\,\mathrm{kHz}$ is chosen for this work. The simulated input-referred noise of the frontend including the chopped FDDA and the PGA is shown in Fig. 4.17 (purple). A slight increase due to the 1/f-noise is observed and is located at approximately 50 Hz. While the PGA can be chopped as well to reduce its 1/f-corner frequency, the residual flicker noise of the current bias will dominate the flicker noise as will be shown in the following section.

4.3 Measurement results

4.3.1 Electrical characterization

First, the chip is electrically characterized before testing its performance with MR sensors. The chip micrograph is shown in Fig. 4.18. The chip is manufactured in 180 nm SOI CMOS, occupying an active area of $1.7\,\mathrm{mm}^2$. The largest two blocks

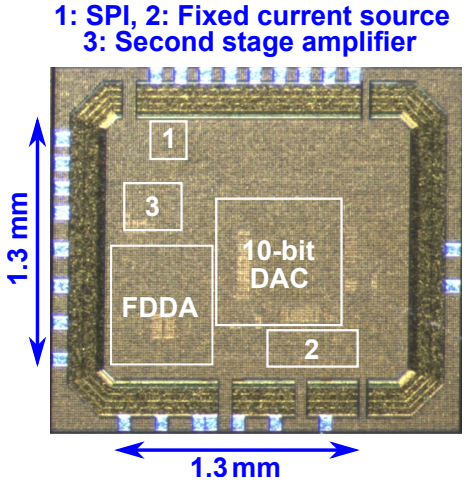

Figure 4.18: Chip micrograph.

in the design are the 10-bit DAC (including the low-noise TIA feedback design) as well as the FDDA. The fixed current of 1 mA used to bias the reference sensor features a much smaller footprint compared to the DAC. The reason is that the DAC unit cells are arranged in a common centroid design, and hence, the routing of the DAC elements results in an increase in the total area compared to the fixed current bias. The presented readout chain consumes 10.4 mW from a 1.8 V supply while the entire chip, including the MR and reference resistor bias, consumes 38 mW from 1.8 V, 3.6 V and 6.8 V supplies [6].

Current bias characterization

To demonstrate the effectiveness of the presented biasing scheme, a separate setup was designed to measure the current bias noise. An external TIA is used as an amplification stage for the current bias. The TIA is built with the amplifier ADA4625 from Analog Devices [53] which features a very low noise input current noise of $4.5\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$. It also can operate with supply voltages up to 36 V which allows using a large feedback resistance in the TIA reducing the overall input-referred current noise of the setup. Fig. 4.19 shows the measured closed-loop output noise of transistor M_{CS} for bias currents of 350 µA, 700 µA and 1 mA. The measured noise floor is $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ with activated control loop and is defined by the feedback resistor R_{FB} for all current settings. A slight increase in the flicker noise is observed for higher currents due to the larger C_{SG} associated with a larger effective device area used for larger currents. Hence, the factor x_{div} is reduced for higher currents, and, as a result, the low-frequency noise is slightly increased, cf. eq. (4.6) and Fig. 4.5. The measured current noise floor presents a 5x improvement compared to previous designs [36, 43] using a voltage-mode feedback system to lower the noise of the current bias compared to the proposed TIA-based feedback loop. The measured output characteristics of the current source for $I_{\mathrm{DAC}} = 500\,\mu\mathrm{A}$ and $I_{\mathrm{DAC}} = 1\,\mathrm{mA}$ are shown

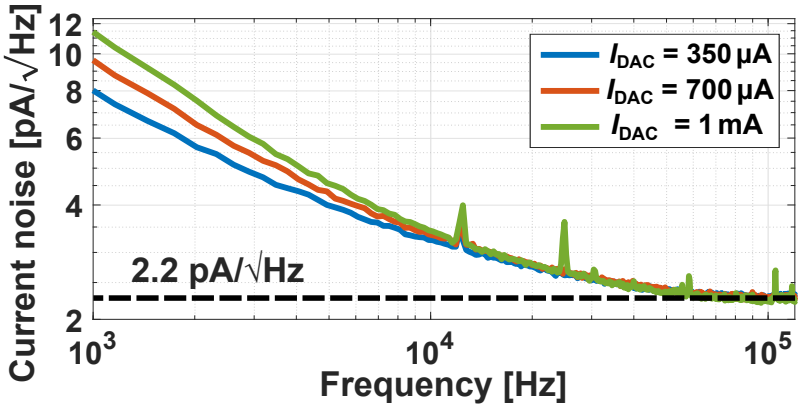

Figure 4.19: Measured current noise PSD of I_{DAC} for different current settings.

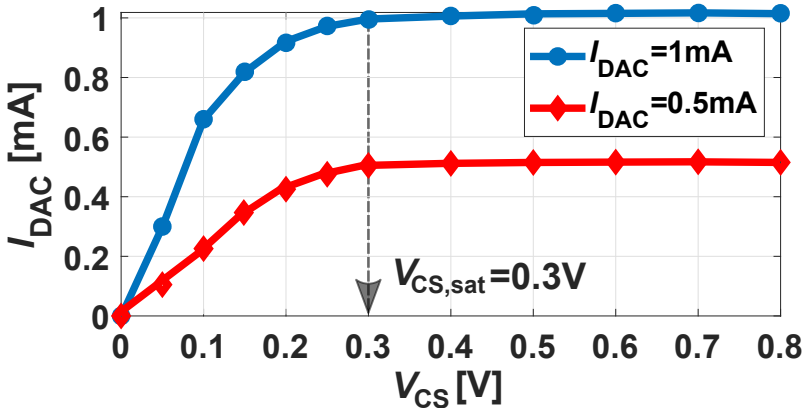

Figure 4.20: Measured output characteristics of I_{DAC} for different current settings.

in Fig. 4.20. Despite the very-low noise operation of the designed current source, it can operate with V_{CS}, where V_{CS} is the voltage drop across the cascoded current source (M_{CS} and M_{CASC} in Fig. 4.5), as low as 0.3 V. The low voltage around the current bias is possible due to the relaxed $g_{\mathrm{m}}/I_{\mathrm{d}}$ requirement to improve the noise floor. For the design, a higher g_{m} would increase the noise suppression of the current bias, and therefore, lowers the saturation voltage of the current bias.

Frontend characterization

The measured input-referred noise of the frontend with and without chopping ($f_{\mathrm{ch}} = 60\,\mathrm{kHz}$) is shown in Fig. 4.21. This measurement is conducted by first compensating for the amplifier offset and then measuring the output spectrum. This is achieved by first calibrating for the sensor offset, and then agressively filtering the input voltage nodes by 22 µF capacitors at the input nodes V_{S} and V_{REF}, cf. Fig. 4.3. This effectively filters the noise originating from the resistors and current bias while setting the correct DC operating points needed for the frontend. The measured noise floor with chopping is $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ compared to a simulated $3.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. With

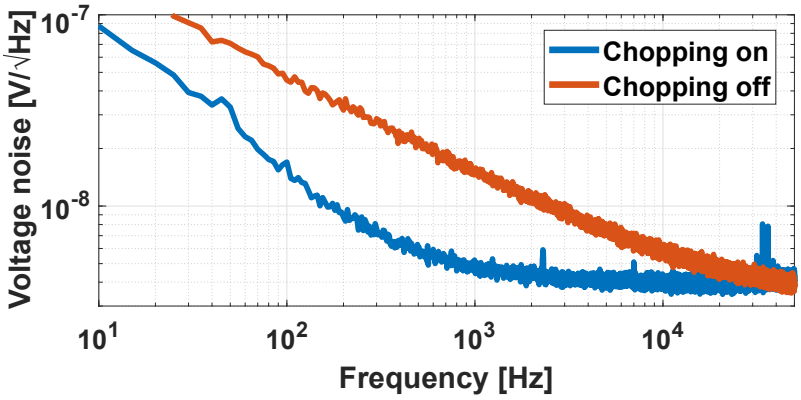

Figure 4.21: Measured input-referred voltage noise PSD of the amplifier chain without and with chopping at 60 kHz.

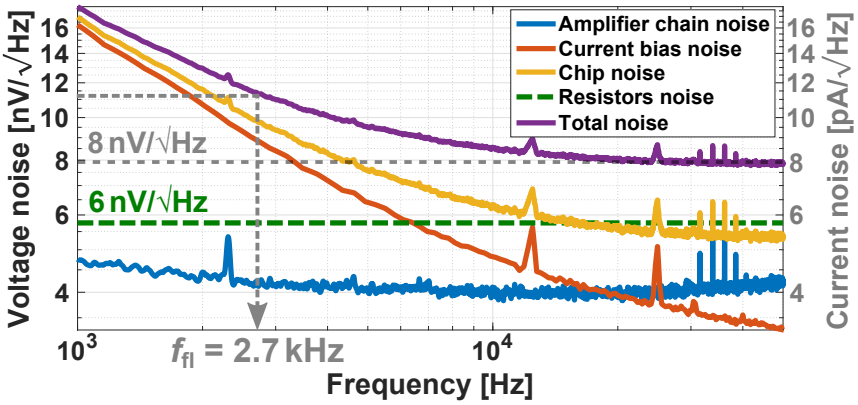

Figure 4.22: Measured input-referred voltage noise PSD of each circuit block and the total measured noise using a 1 kΩ sensor.

enabled chopping, the measured 1/f-noise corner frequency is 400 Hz which is an order of magnitude higher compared to the simulated 1/f-corner frequency. The residual flicker noise after chopping originates from the unchopped PGA, cf. Fig. 4.3.

Overall noise performance

One important aspect of this work is to quantify the noise contribution of each block on the overall performance. Ideally, the noise of the sensor's biasing and the frontend amplifiers should be lower compared to the intrinsic noise floor of the MR sensor and the reference resistor. A drawback of such an approach is the lower power efficiency which is crucial for PoC systems relying on batteries as a power source. Fig. 4.22 shows the measured input-referred voltage and current noise PSDs of each circuit block, the total noise PSD of the chip as well as the total noise PSD of the complete system including the MR sensor and reference resistor. The total noise contribution should be evaluated for extreme values of the desired resistances of 1 kΩ up to

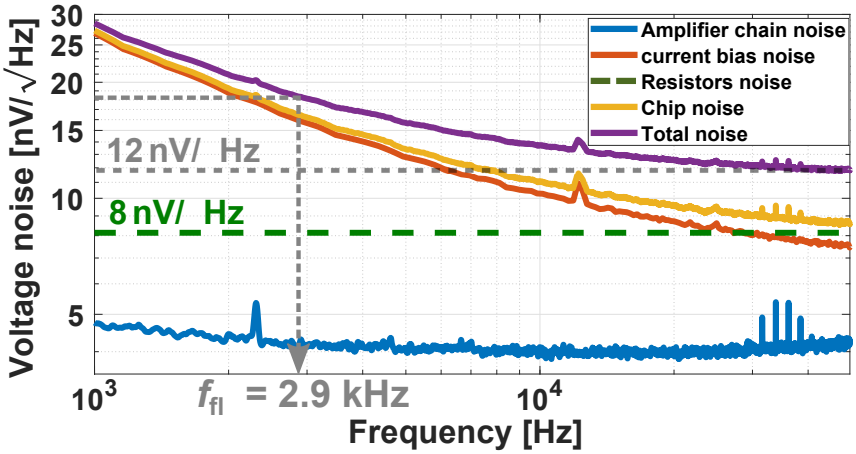

Figure 4.23: Measured input-referred voltage noise PSD of each circuit block and the total measured noise for a 3 kΩ sensor scenario.

3 kΩ. The lower end of the base resistance results in the best-case intrinsic SNR assuming that the sensitivity of the sensor does not change with the base resistance. On the other hand, the higher end of resistance values would directly increase the noise contribution of the current bias since the noise of the current bias would be amplified by the resistance values. First, the noise of the lower limit of MR resistance is investigated in Fig. 4.22 for base resistance of 1 kΩ. In total, the sensor and the reference resistors contribute for a thermal noise floor of $6\,\mathrm{nV}\sqrt{\mathrm{Hz}}$. The noise floor of the electronics, including the amplifier chain, the fixed current bias and the current DAC, is kept lower than the noise floor of the sensor and reference resistors. Looking at the overall noise performance of the system, including both resistors, the measured noise floor is at $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ with a 1/f-corner frequency of $f_{\mathrm{fl}} = 2.7\,\mathrm{kHz}$. As a result, the degradation in the SNR due to the electronics is 2.5 dB.
On the other hand, the noise using a 3 kΩ sensor resistance is evaluated using a 3 kΩ and a 1 kΩ ohmic resistors, representing the MR sensor and reference resistor, respectively, and the breakdown of this noise measurement is shown in Fig. 4.23. The reference sensor is not changed to highlight the mismatch compensation of the chip due to the 10-bit current DAC. As expected, the ohmic resistors' noise floor is increased to $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and the overall noise floor of the system is increased. The total noise floor including the integrated electronics and the resistors is $12\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Overall, the SNR degradation is slightly worse compared to the pair of the 1 kΩ resistors and corresponds to a degradation of 3.5 dB. The 1/f-corner frequency is slightly increased to 2.9 kHz whilst having limited effect on the overall noise performance of the system. For biosensing systems demanding very high SNR, the modulation frequency of MNTs are chosen above the 1/f-corner frequency of the complete system.

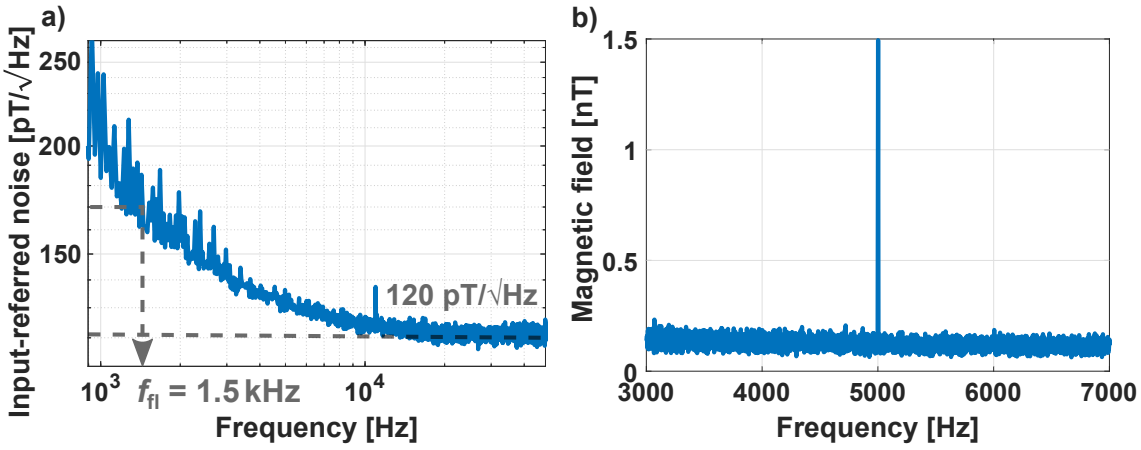

Figure 4.24: a) Input-referred magnetic noise PSD of the TMR system. b) Measured spectrum with an input magnetic field of $1.5\,\mathrm{nT_{rms}}$.

4.3.2 Measurements including a TMR sensor

After the electrical characterization of the system, the TMR sensor system was evaluated using the proposed chip. As a first step, we built a measurement setup in order to characterize the TMR element in terms of its sensitivity and the offset field required to shift its operation to its linear region where its sensitivity is maximized. In order to do so, we used two Helmholtz coils in order to generate the magnetic fields used to properly characterize the TMR element. To reduce the complexity of the setup, a large AC voltage is applied to the coils at a frequency higher than the 1/f-corner frequency of the MR system of 5 kHz. The excited field by the coil were in the range of 100 µT and is measured using a Hall sensor. A large field might saturate an MR sensor, however, it is necessary for the field calibration since a hall sensor has a lower sensitivity compared to an MR sensor. Afterwards, the TMR sensor already presented in [35] is evaluated by replacing one of the ohmic resistors with the TMR sensor. The characterization of the sensitivity of the sensor is then evaluated by applying a much smaller field but at the same frequency of 5 kHz since the 100 µT field would saturate the TMR element. While keeping the frequency fixed, the excited magnetic field scales linearly with the applied voltage, and hence, the applied fields can be precisely monitored using the reference measurement using the hall device. To start the test, the autocalibration routine is started to compensate for the mismatch between the TMR sensor and the reference resistor. The measured base resistance of the TMR sensor is 1.4 kΩ and a sensitivity of 110 V/A/mT for a bias current of 700 µA. The measured input-referred voltage noise floor is $8.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ which is in good agreement with the measurements using ohmic resistors, cf. Fig. 4.22 and Fig. 4.23. For the same bias current, the measured input-referred magnetic field noise PSD shown in Fig. 4.24a. The measured magnetic noise floor is $120\,\mathrm{pT}/\sqrt{\mathrm{Hz}}$ with a 1/f-noise corner frequency of $f_{\mathrm{fl}} = 1.5\,\mathrm{kHz}$. Fig. 4.24b shows the spectrum at the output of the sensor system when applying a

magnetic field at a frequency of 5 kHz with an amplitude of 1.5 nT_{rms}. The measured SNR is 22 dB, from which a limit of detection (LOD) of 120 $pT/\sqrt{Hz}$ has been calculated, which is compatible with the measured magnetic field noise in the absence of a signal, verifying the absence of nonlinear noise folding effects.

4.4 Benchmarking and conclusions

4.4.1 Comparison against state-of-the-art

Table 4.1 compares this work to the state-of-the-art in MR frontends with current biasing as well as a commercial adjustable very low-noise current source LM134 from Texas Instruments [54]. The proposed current bias features 45x improvement in the noise floor as well as a lower $V_{CS} = 0.3\,V$ compared to $V_{CS} = 0.85\,V$ for the LM134 chip for the 1 mA configuration. Although the LM134 chip can output currents up to 10 mA, simple adjustments can be made to increase the output current of the DAC while keeping its noise lower compared to the LM134 chip.
Compared to SoA MR sensor designs incorporating current biasing, this design achieves the lowest current bias noise floor, the lowest voltage noise floor as well as the lowest input-referred magnetic noise floor. The main reason behind the excellent noise performance is the current bias design. In [36] and [43], the noise of the current bias is suppressed using the voltage-mode feedback structure limiting the noise floor to 10 $pA/\sqrt{Hz}$. However, the design by Costa [43] intended to modulate the MNTs at a frequency of $f_{mod} = 211\,Hz$ which is lower than the 1/f-corner frequency of the GMR sensor of $f_{mod} = 10\,kHz$. This translates to lower noise requirements from the current bias. Finally, the very large improvement in the magnetic noise floor can be traced to the improvement in the current bias design, as well as the higher sensitivity of the TMR sensor compared to a GMR sensor used in the other designs.

4.4.2 Conclusions

In this chapter, we have presented the second generation of improved MR readout chips, also published in [6, 7]. The design improvements mainly focused on the noise performance as well as improvements in the design programmability. The noise improvements are achieved by a novel current bias scheme embedded in a TIA-based feedback loop to lower the noise of the current bias by the loop gain. Moreover, in our presented scheme, the noise of the embedded amplifier is highly attenuated by the proposed structure rendering the design suitable for ultra-low-noise applications. Consequently, the DAC unit element dimensions in the second generation of chips are greatly reduced from 0.85 µm/80 µm to only 1 µm/1 µm. This directly translates to 70x reduction in the DAC footprint without any increase in the noise floor. Another important feature of this design is the relaxed requirement of $V_{ds,sat}$. The proposed current bias operates with $V_{ds,sat} = 150\,mV$ compared to $V_{ds,sat} = 600\,mV$ for the first generation of chips. The proposed current bias

achieves a SoA noise floor of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for currents up to 1 mA which shows as 5x improvement compared to prior arts. Its large bias current range accommodates the high process variations of TMR sensors. Another measure to lower the noise of the frontend is to include chopping switches for the FDDA. Consequently, the 1/f-corner frequency of the frontend is improved from 10 kHz to 400 Hz with a noise floor of $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The overall frontend with the current bias and nominally equal resistors of $1\,\mathrm{k}\Omega$ and negligible 1/f-noise shows a noise floor of $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a 1/f-corner frequency of $f_{\mathrm{fl}} = 2.7\,\mathrm{kHz}$.
We improved the chip programmability by changing the second-stage amplifier in the first generation of chips to a programmable variant. The PGA provides different gain settings, and the overall gain of the frontend can be adjusted between 80 and 800 based on the dynamic range requirements of the MR sensor. To control the chip's different modes of operation, we implemented an on-chip SPI interface to control the autocalibration routine, the gain of the PGA, as well as switching on and off different circuit blocks if needed.
The low-noise operation of the chips, as well as their large dynamic range, provide a very good starting point to build high performance PoC systems relying on highly sensitive MR sensors. Moreover, the low-noise offset compensation scheme allowed us to handle large changes in the base resistance of the MR sensor facilitating the use of such PoC systems in different environments.

Table 4.1: Comparison against the state-of-the-art.

	LM134 TI [54]	Costa TBCAS'17 [43]	Zhou JSSC'21 [36]	**This work ESSCIRC'21 [6] SSC-L'22 [7]**
Current bias	up to 10 mA	0.5 mA	–	**up to 1 mA**
Bias noise floor [pA/$\sqrt{\text{Hz}}$]	100^{α}	10	$\approx 10^{\gamma}$	**2.2**
Minimum V_{CS} [V]	0.85^{α}	–	–	**0.3**
Sensor	–	GMR	GMR	**TMR**
Resistance [Ω]	–	850	1300	**1400**
Reference sensor	–	No	No	**Yes**
Voltage noise floor [nV/$\sqrt{\text{Hz}}$]	–	16	$\approx 15^{\gamma}$	**8**
1/f-corner frequency	–	$< 100\,\text{Hz}^{\gamma,\beta}$	$< 50\,\text{Hz}^{\gamma,\psi}$	**1.5 kHz**
Input-referred noise [nT/$\sqrt{\text{Hz}}$]	–	11.5	8.2^{γ}	**0.12**
Supply voltages [V]	–	3.3	1.8	**1.8, 3.6, 6.8**
Bias power [mW]	–	1.6	–	**27.6**
Readout power [mW]	–	4.9	2.5	**10.4**
Area [mm^2]	–	3.17	1.92^{ψ}	**1.7**
Process [µm]	–	0.35	0.18	**0.18**
Number of sensors	–	192	1	**1**

$^{\gamma}$Estimated from figures and text. $^{\alpha}$For 1 mA current. $^{\psi}$Includes ADC.
$^{\beta}$Sensor's 1/f-corner frequency $\approx$ 10 kHz.

5 Noise-aware design methodology for low-noise TIAs

In the previous chapters, high performance MR readouts are discussed by presenting very low noise chips with superior linearity thanks to their current bias. Clearly, such high performance readouts are possible at the expense of an increased die area as well as higher power consumption needed for a low-noise current bias. Alternatively, a voltage-mode excitation of MR sensors and a TIA-based readout can be adopted for lower power applications and/or applications with a strict area constraint. A TIA-based readout is widely used for high performance current readout as well as for MR sensing systems. Consequently, this chapter extends the discussion of TIA design for both MR sensor systems as well as high performance current readouts. This being said, this chapter is divided into two sections. The first section presents an overview of different TIA architectures in terms of design complexity, noise performance and power requirements. The second section focuses on the design of high performance TIAs and offers a design guideline for an optimized TIA design in terms of its noise performance. The proposed noise-aware design methodology is valid for all TIA architectures and is, to a great extent, independent of the internal amplifier topology.

5.1 Motivation and design topologies

5.1.1 The need of high performance current readouts

In many sensor readout applications, a decision has to be made whether to choose a voltage-mode or a current-mode frontend based on multiple parameters such as power consumption, required chip area, multiplexing capabilities, sensor's excitation and many more. One example of such applications are MR sensor systems. As thoroughly discussed in the last two chapters, a voltage-mode readout for MR sensors with current excitation is adopted for higher linearity. However, this comes at the expense of higher power consumption needed to generate a low-noise current bias. Moreover, a low-noise current bias is not commonly available on the market and, even high performance current sources, are not optimized for very low-noise operation. On the other hand, a low-noise voltage bias can be, in principle, easily generated using a battery or an external low-noise voltage reference, and hence, a current readout using a TIA can be more power efficient. Not only MR sensor, or resistive sensors as a whole, can be readout using a TIA, but also many optical systems

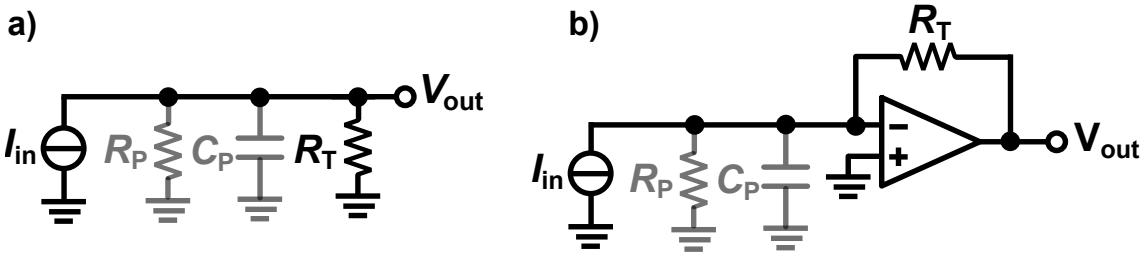

Figure 5.1: a) Current readout using a simple resistor. b) Current readout using an R-TIA.

are readout by high performance and low-noise TIAs. Moreover, many emerging materials and life science applications create an increasing need for ultra-low-noise current readouts. Examples of such applications include nanoscale cell imaging [55], nanopore sensing [56], as well as probing chemical reactions on the nanoscale [57]. In all these applications, an ultra-low-noise current readout is required to preserve the intrinsic signal-to-noise ratio (SNR) of the experiment as close as possible. As a result, this chapter does not exclusively focus on TIA design for MR sensors, which is the main focus of this work, but also expands the analysis to high performance TIAs with very-low-noise requirements.

5.1.2 TIA topologies

Many TIA topologies are thoroughly explained in the literature offering a suitable interface for sensors with a current output. All these topologies feature (very) low input impedance creating a close-to-ideal output load for a current bias.
A very simple current readout is shown in Fig. 5.1a where a resistor R_T is connected directly to the output of current source I_in representing the output current of the sensor. Ideally, the output voltage can be described as $|I_\mathrm{in} \cdot R_\mathrm{T}|$ where R_T is the transimpedance resistance. This simple design has multiple drawbacks. First, any voltage swing around the output node is also coupled to the sensor. Surely, an ideal current source is not affected by the voltage fluctuations around it, however, a real current source posses a finite impedance and a non-linear behavior. An example of such systems would be photodiodes, where the voltage bias across the diode determines dominantly its operating region, and the voltage swings across the diode would affect its linearity. Moreover, the load impedance of the sensor is proportional to R_T and cannot be picked arbitrarily low without lowering the overall gain, and consequently, increasing the input-referred noise. Another drawback of this simple design is the parasitic capacitance and its effect on the system's bandwidth. In this configuration, capacitance C_P in parallel to R_T creates a pole frequency at $\omega_\mathrm{P} = 1/(R_\mathrm{T}C_\mathrm{P})$ limiting the bandwidth of the readout. Finally, the voltage bias across the sensor cannot be set without additional circuitry defining the voltage bias across the sensor.
To solve these drawbacks, resistor R_T can be placed as the feedback element of an

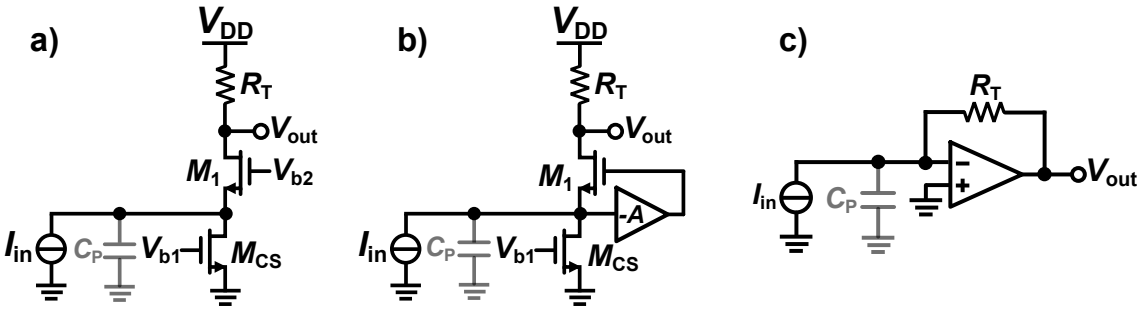

Figure 5.2: a) Common-gate TIA. b) Regulated common-gate TIA. c) Closed-loop R-TIA.

amplifier, and all together, forming a resistive TIA (R-TIA) as shown in Fig. 5.1b. To understand the reason behind the superior performance of the R-TIA compared to the simple design shown in Fig. 5.1b, the output and input voltages of the R-TIA in terms of the open-loop gain of the amplifier $A_{\rm op}$ can be computed as follow:

$$V_{\rm out} = -\frac{A_{\rm op}}{A_{\rm op}+1}\left(I_{\rm in}\cdot R_{\rm T}\right) \approx -I_{\rm in}\cdot R_{\rm T}, \tag{5.1a}$$

$$V_{\rm in} = -\frac{1}{A_{\rm op}+1}\left(I_{\rm in}\cdot R_{\rm T}\right) \approx 0. \tag{5.1b}$$

One can conclude from the above equations that the input and output voltage swings are completely decoupled (for large $A_{\rm op}$) and the input voltage node can be very quiet irrespective of the output swing. Since $V_{\rm in}$ is very small, the input impedance of the R-TIA is also very small (ideally zero for an infinite $A_{\rm op}$) and independent of the feedback resistance $R_{\rm T}$.

Open-loop versus closed-loop TIAs

TIAs do not necessarily need to be implemented in closed-loop configurations, open-loop architectures with low input impedance would be an alternative design choice. Fig. 5.2 shows three different TIA topologies based on open-loop configurations (Fig. 5.2 a,b) and the closed-loop R-TIA, cf. Fig. 5.2c. The open-loop configurations use a common-gate input stage which is known for its low input impedance. In all these configurations, the transimpedance at low frequencies is defined by the transimpedance resistance $R_{\rm T}$. One of the first designs for open-loop based TIA is based on a common-gate input stage (or a common-base input stage for designs incorporating BJTs) [58]. The common-gate TIA has an input impedance of $1/g_{\rm m,M1}$, assuming small to medium values of $R_{\rm T}$, which can be low for large bias currents. The bandwidth of this design is evaluated as $\omega_{3-\rm dB} = g_{\rm m,M1}/C_{\rm P}$. As a result, for high speed applications, it is desirable to increase $g_{\rm m,M1}$ which can be achieved by increasing the bias current. However, increasing the bias current would eventually lead to a reduction in the chosen transimpedance resistance $R_{\rm T}$ for a targeted output

voltage swing limited by the supply voltage [59]. Alternatively, a regulated common-gate topology elevates this tradeoff by introducing an amplifier to boost the effective transconductance of transistor M_1, $g_{\mathrm{meff,M1}}$, to become $g_{\mathrm{meff,M1}} = (A+1) \cdot g_{\mathrm{m,M1}}$ [60]. This also translates to a lower effective input resistance providing a close-to-ideal load to the current sensor. Consequently, the g_{m} needed to achieve the target bandwidth is lowered by the gain of the auxiliary amplifier, and effectively, lowers the current requirement of the TIA while relaxing its output dynamic range requirements. However, both common-gate designs suffer from another tradeoff between the noise of the current source and dynamic range. For both designs, the input-referred noise of the TIA can be expressed as:

$$S_{\Delta I_{\mathrm{in}}^2} = 4kT \left(\gamma \, g_{\mathrm{m,CS}} + \frac{1}{R_{\mathrm{T}}} \right). \tag{5.2}$$

Again, this clearly indicates the tradeoff between, this time, the transconductance of the current source $g_{\mathrm{m,CS}}$ and the transimpedance resistance R_{T}. A closed-loop TIA such as the R-TIA shown in Fig. 5.2 mitigates such tradeoff. The noise of the opamp, primarily controlled by its bias current, can be chosen freely without being forced to scale the feedback element, (R_{T} in this case). As a result, low-noise current readout systems favor closed-loop TIA designs due the the additional degree of freedom of lowering the TIA noise while maintaining the desired transimpedance. However, similar to any closed-loop system, such configuration is typically limited to low to medium speed designs due to its closed-loop nature. Generally, the open-loop designs shown in Fig. 5.2a,b are used for high speed, low-medium resolution designs while the closed-loop designs are typically used for low-noise current readout systems.

Closed-loop TIAs

Figure 5.3 shows three different structures of closed-loop TIAs that are typically employed, namely R-TIAs [61, 62], capacitive TIAs (C-TIAs) [63, 64] and current-mode Sigma Delta modulators (SDMs) [65, 66, 8]. Although R-TIAs, shown in Fig. 5.3a, are widely used in many low-noise applications, C-TIAs are gaining attention for applications with very low input currents, such as measurements on nanodevices [67]. C-TIAs employ capacitors as the transimpedance element in the feedback of the amplifier, cf. Fig. 5.3b. This is particularly important when a large transimpedance is needed to amplify minute current signals without using very large resistors. Such large resistors, in the MΩ or even GΩ range, can only be implemented using active devices such as pseudoresistors [68] limiting the overall linearity of the system. Needless to say, a capacitor is a noise-free component whilst a resistor is noisy. A drawback of C-TIAs is that they are not suitable for processing DC signals since the feedback capacitor alone does not provide a DC path. As a result, DSLs are usually employed to source/sink the DC current. Moreover, the DC feedback of the TIA has to be set by additional circuitry. This can be done by constantly resetting

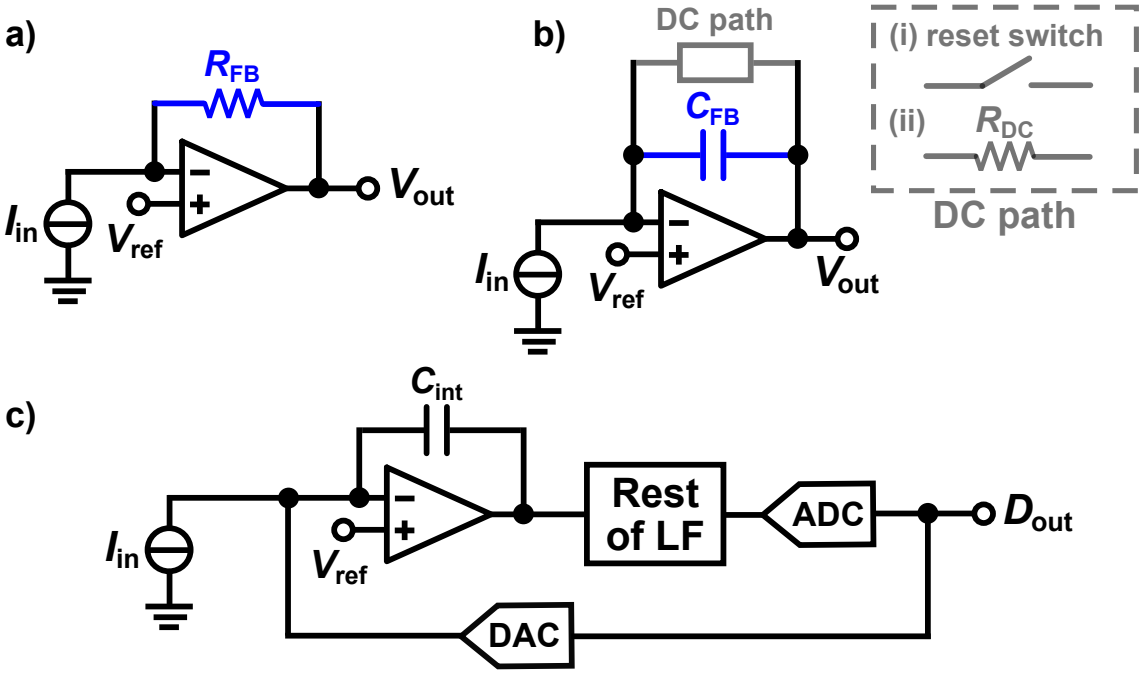

Figure 5.3: Block diagram of a) an R-TIA, b) a C-TIA with a feedback DC path, and c) a current-mode SDM.

the feedback capacitance using a switch connected in parallel to the feedback capacitor to avoid saturating the TIA. Alternatively, a very large feedback resistor can be connected in parallel to the feedback capacitor providing a DC path from the output to the input of the TIA. It is worth mentioning that the feedback resistance, even if implemented using a pseudoresistor, does not affect the linearity of the TIA since the desired signal component flows through the feedback capacitance and not through the very large resistance. On the other hand, applications with lower transimpedance benefit from small ohmic resistors, with smaller footprints, compared to large feedback capacitors. Another alternative for TIAs is to directly interface the sensor with a current-mode SDM as shown in Fig. 5.3c. Strictly speaking, a current-mode SDM does not fall under the umbrella of TIAs since the output of the current-mode SDM is a digital representation of the input current and not an output voltage. However, there is a strong similarity between R-TIAs, C-TIAs and current-mode SDMs in terms of their input stages since they are all comprised of an opamp with resistive and/or capacitive feedback. Moreover, the opamp in all architectures exhibits close-to-identical noise performance as will be thoroughly discussed in section 5.2. As a result, it is justified to compare the current-mode SDM within other TIA structures similar to [69]. The main motivation behind directly interfacing the sensor with a current-mode SDM is to reduce the power consumption and the area needed for the frontend compared to interfacing the sensor with an R- or a C-TIA followed by a classical voltage-mode ADC. A detailed analysis of current-mode SDMs and their advantages are explained in details in Chapter 6.

5.2 Noise in closed-loop TIAs

In this work, we solely focus on closed-loop TIAs due to their very low-noise operation. The current goal is to closely analyze the noise of these TIAs and come up with a noise-aware design methodology to design the optimum amplifier embedded in the TIA. At first glance, it might seem that R-TIAs, C-TIAs and current-mode SDMs would show a different noise behavior due to their different structures. However, all three types of TIAs share the same input-referred noise transfer functions with respect to the opamp's noise, total input capacitance and resistance as well as the feedback capacitance and/or resistor. As a result, a single design methodology of all three different TIAs can be adopted in this work. This being said, changing one topology to another does not necessarily mean that the input-referred noise would be unaltered since the value of the passive elements would change from an R-TIA to a C-TIA or a current-mode SDM. However, the noise equations remain the same, and as a result, a single noise-aware design approach can be used for all TIA configurations as will be shown in this chapter. Fig. 5.4a shows the input stage of the three TIAs. The advantages and disadvantages of each architecture are discussed in detail in [69].

5.2.1 Noise in TIAs with large transimpedance values

What is interesting is that all TIA topologies display very similar design tradeoffs when striving for an optimum noise performance. More specifically, the input-referred voltage noise PSD of the opamp is shaped by the square of the magnitude of the input admittance as illustrated in Fig. 5.4b. At low frequencies, the input admittance is mainly given by the feedback resistance up to the corner frequency $f_{\mathrm{fc}} = 1/2\pi R_{\mathrm{FB}} C_{\mathrm{in}}$, where C_{in} is the input capacitance of the TIA. At frequencies higher than f_{fc}, the input admittance is defined by the input capacitance C_{in} and is equal to $2\pi f C_{\mathrm{in}}$. As a result, the input admittance, defining the shaping of the input-referred noise of the opamp, scales with frequency. The total admittance Y_{in} at the TIA input can be expressed as follows:

$$Y_{\mathrm{in}} = \frac{1}{R_{\mathrm{FB}}} + 2\pi f C_{\mathrm{in}}. \tag{5.3}$$

Overall, the input-referred noise PSD $S_{\Delta \mathrm{I}^2_{\mathrm{in,TIA}}}$ shown in Fig. 5.4b (left) is shaped by the square of the input admittance expressed in eq. (5.3) producing the characteristic noise power spectral density (PSD) at the TIA input shown in Fig. 5.4b (right) and expressed as:

$$S_{\Delta \mathrm{I}^2_{\mathrm{in,TIA}}} = S_{\Delta \mathrm{V}^2_{\mathrm{in,opamp}}} \cdot |Y_{\mathrm{in}}|^2 + \frac{4kT}{R_{\mathrm{FB}}}. \tag{5.4}$$

Up to the 1/f-corner frequency of the opamp, f_{fl}, the input-referred voltage noise PSD of the opamp is dominated by flicker noise before it reaches its white noise floor. The flicker noise corner frequency f_{fl} is mainly determined by the utilized

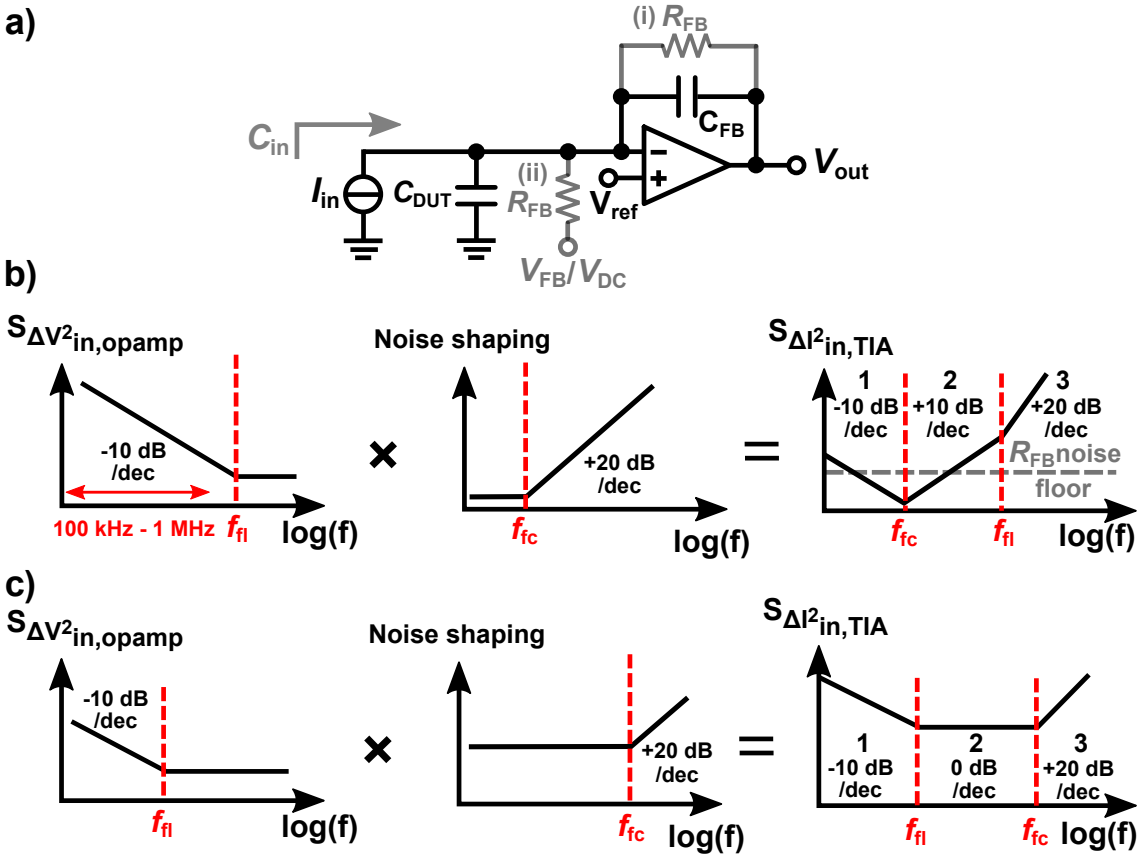

Figure 5.4: a) Input stage of a generic current readout circuit. b) Illustration of the origin of the different regions of the opamp noise PSD referred to the TIA input for large transimpedance. c) Illustration of the origin of the different regions of the opamp noise PSD referred to the TIA input for small transimpedance.

technology and the device geometry. Here, for modern CMOS technologies, values for f_{f} between a few tens of kHz and several MHz are common [70]. To reduce f_{f}, the device geometry can be increased, however, this comes at the expense of reducing f_{fc} due to increasing C_{in} as long as C_{in} is dominated by the input capacitance of the TIA and not by C_{DUT}. Therefore, as illustrated in Fig. 5.4b (middle), the opamp noise transfer function is initially flat, with a value of $1/R_{\mathrm{FB}}$, and then rises with +20 dB/dec beyond the corner frequency f_{fc}, resulting in the typical TIA input-referred noise PSD shown in Fig. 5.4b (right), which, for low frequencies, rolls of with −10 dB/dec (region 1), before it rises with +10 dB/dec (region 2) and +20 dB/dec (region 3) beyond the frequencies f_{fc} and f_{fl}, respectively. Due to the relatively large values of f_{fl} for deep submicron CMOS realizations of the OTA, the shaped flicker noise in region 2 typically limits the achievable performance of low-noise CMOS TIAs. This introduces a strong tradeoff in the design since lowering the flicker noise requires large device geometries, which, in turn, increases the effective input capacitance C_{in}, and, thereby eventually deteriorates the overall noise performance

of the TIA by lowering f_{fc}.

5.2.2 Noise in TIAs with low transimpedance values

Here it is important to observe the input-referred noise for applications with small and large current signals as well as their respective frequency of operation. The sketch shown in Fig. 5.4b is valid for applications with very small currents that require large transimpedance values. As a result, f_{fc} can be relatively small and the 1/f-corner frequency f_{fl} can be larger than f_{fc}. However, for applications requiring lower transimpedance values, such as for MR sensor readouts, the situation is different . The different noise shaping is shown in Fig. 5.4c with lower transimpedance values, in the kΩ regime for example. In this situation, there is a flicker noise limited region followed by a flat noise region, limited by thermal noise. Finally, f_{fc} is usually located at frequencies higher than the signal bandwidth. In this scenario, it is simpler to lower f_{fl} without significantly limiting the bandwidth by shifting f_{fc}, as long as f_{fc} is kept higher than the signal bandwidth. This being said, a clear distinction between applications with low current amplitudes and high current amplitudes cannot be made since the input-referred current noise depends on several factors such as input capacitance, the transimpedance and the bandwidth of operation. However, a single set of design equations can still relate all these designs together as will be shown in the next sections.

5.2.3 A noise model of the embedded opamp

As previously shown in eqs. (5.3) and (5.4), the input-referred noise of the TIA depends on the shaped opamp noise as well as the noise of the feedback resistor R_{FB}. However, there is a clear tradeoff regarding lowering the input-referred noise of the TIA by lowering the input-referred voltage noise of the embedded opamp. In many cases, lowering the input-referred voltage noise of an opamp is achieved by increasing the size of the input pair, for lower flicker noise, or increasing the bias current of the opamp which eventually can be reached by increasing the size of the input pair. As a result, an increase in the input capacitance C_{in} is unavoidable, and hence, an increase in Y_{in} is also expected. In order to further analyze the noise of the opamp and its effect on the overall noise performance of the TIA, the noise contribution of each noise-critical transistor in the opamp is derived and referred to the input noise of the TIA.
Fig. 5.5 shows a possible transistor-level realization of an R-TIA using a simple differential pair with current mirror loads as opamp. While practical opamp realizations utilize more complex architectures, the circuit of Fig. 5.5 contains all noise critical devices. The capacitance introduced by the sensing element is modeled by the capacitance C_{DUT}. As a rule of thumb, large values of C_{DUT} can greatly deteriorate the overall TIA noise performance by lowering f_{c} if no extra measures, such as bootstrapping, are considered. To obtain the input-referred noise of the TIA, the

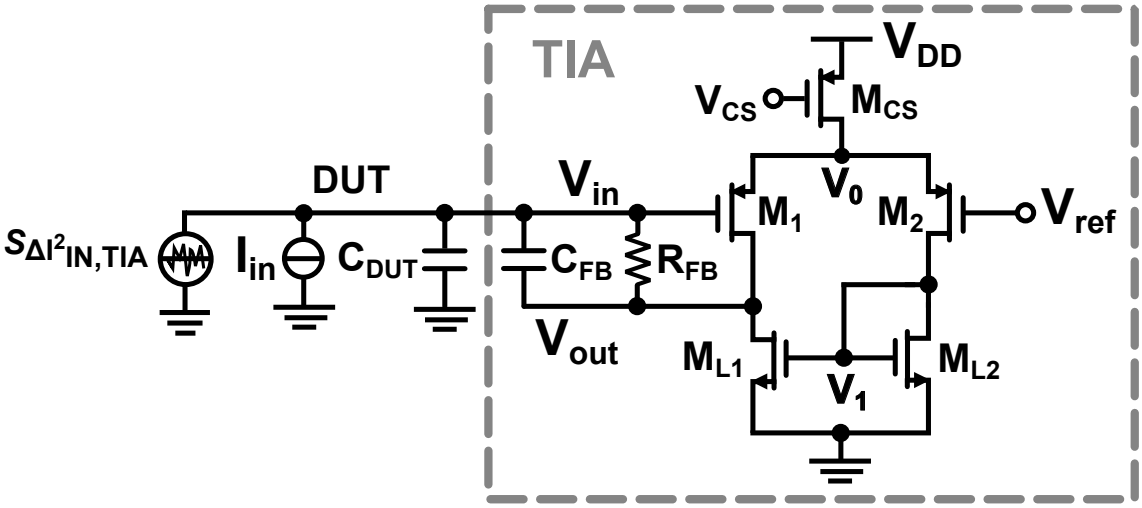

Figure 5.5: Transistor-level realization of an R-TIA using a simple differential-pair amplifier with current mirror load.

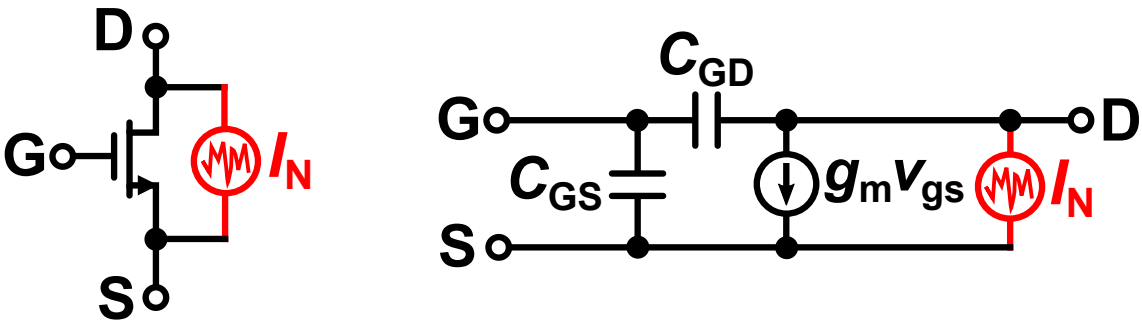

Figure 5.6: Small-signal model of an NMOS used to derive the total input-referred noise of the TIA.

superposition principle can be applied. That is, for linear systems, and assuming small signals, uncorrelated noise sources can be analyzed separately and added in the power domain to obtain the total input-referred current noise PSD according to:

$$S_{\Delta I^2_{\mathrm{nOTA,eq}}} = \sum S_{\Delta I^2_{\mathrm{IN},Mi}}, \tag{5.5}$$

where $S_{\Delta I^2_{\mathrm{IN},Mi}}$ is the input-referred noise PSD of each single transistor M_i. To analyze each noise source, the small-signal model of the TIA is used and the noise of each transistor is referred to the input. The simplified small-signal model of a single noisy NMOS transistor is shown in Fig. 5.6. Overall, the embedded opamp inside the TIA is modeled as an integrator, without its small-signal conductance g_{ds}, simplifying the analysis of the TIA and allowing to arrive at a compact closed-form expressions suitable for design purposes. The effect of the finite transconductance g_{ds} will be shown in the next sections when the noise of a transistor-level opamp model is simulated and compared to the analytical model.

Noise due to the input differential pair

To start with, the noise of the input differential pair is analyzed since it is the most critical noise block of the amplifier. It is commonly mentioned in the literature that each input transistor would generate equal input-referred noise. This is true for fully-differential circuits with no mismatch introduced in the circuit. However, due to the single-ended nature of most current sensors, the single-ended structure shown in Fig. 5.5 is employed in most designs. As a matter of fact, in the standard single-ended output TIA configuration of Fig. 5.5, the noise of the two transistors in the differential pair is weighted differently. More specifically, the input-referred noise of transistor M_1 is given by:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,M1}}} = S_{\Delta \mathrm{V}^2_{\mathrm{IN,M1}}} \left[\omega \left(C_{\mathrm{GG,M1}} + C_{\mathrm{DUT}} + C_{\mathrm{FB}} \right) + \frac{1}{R_{\mathrm{FB}}} \right]^2, \tag{5.6}$$

where $C_{\mathrm{GG,M1}}$ is the total gate capacitance of transistor M_1 as follows:

$$S_{\Delta \mathrm{V}^2_{\mathrm{IN,M1}}} = S_{\Delta \mathrm{I}^2_{\mathrm{n,M1}}} / g^2_{\mathrm{m,M1}} \tag{5.7}$$

By contrast, the input-referred noise of M_2 is given by:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,M2}}} = S_{\Delta \mathrm{V}^2_{\mathrm{IN,M2}}} \left[\omega \left(C_{\mathrm{GD,M2}} + C_{\mathrm{DUT}} + C_{\mathrm{FB}} \right) + \frac{1}{R_{\mathrm{FB}}} \right]^2. \tag{5.8}$$

Eq. (5.8) indicates that the noise PSD of transistor M_2 is not shaped by the total gate capacitance of M_2 but only its gate-drain capacitance C_{GD}. The different noise transfer functions are due to the uneven loading of M_1 and M_2. It is worth mentioning that, in fully-differential structures, the transistors M_1 and M_2 equally contribute to the total input-referred noise. For very low-noise designs with correspondingly large values of R_{FB} in the range of several GΩ, R_{FB} dominates the noise behavior only at very low frequencies [61, 67]. Consequently, the largest fraction of the integrated input-referred noise originates from shaped noise produced by the term $\left[\omega \left(C_{\mathrm{GG/GD}} + C_{\mathrm{DUT}} + C_{\mathrm{FB}} \right)\right]^2$. In designs with low transimpedances however, this asymmetry in the shaped noise between the two transistors in the differential pair can be neglected to a large extent. This is because the noise would be primarily shaped by the feedback resistance R_{FB} and not by the capacitance (at least until fairly very high frequencies for low transimpedances).

Noise due to the current mirror load

While in many textbooks, the effect of the current mirror is claimed to be negligible, care has to be taken that the conditions to achieve this situation are met in practice. More specifically, the input-referred noise originating from transistors $M_{\mathrm{L1,2}}$ is given by:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,ML1/2}}} = \frac{S_{\Delta \mathrm{I}^2_{\mathrm{n,ML}}}}{g^2_{\mathrm{m,M1}}} \left[\omega \left(C_{\mathrm{GG,M1/2}} + C_{\mathrm{DUT}} + C_{\mathrm{FB}} \right) + \frac{1}{R_{\mathrm{FB}}} \right]^2. \tag{5.9}$$

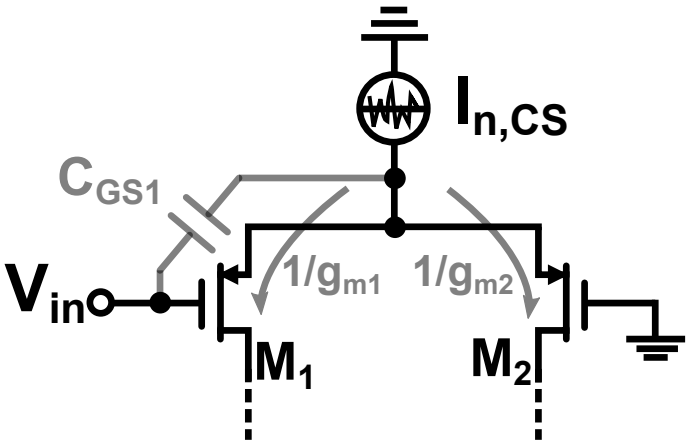

Figure 5.7: Small-signal model of an NMOS used to derive the total input-referred noise of the TIA.

According to eq. (5.9), the noise contribution of $M_{\mathrm{L1,2}}$ can be minimized by biasing the input differential pair in weak inversion and biasing the transistors $M_{\mathrm{L1,2}}$ in strong inversion. However, such approach has to be considered with a pinch of salt since larger capacitance is always accompanied by biasing transistors in weak inversion. Fortunately, reducing flicker noise of the current mirror loads can be straight forward by simply increasing their area without worrying about their additional capacitance, cf. eq. (5.9).

Noise due to the tail current source

Due to the asymmetrical loading of the OTA, even when assuming perfect matching, the noise from the tail current source is visible in the OTA output and, therefore, also contributes to the total input-referred TIA noise. The input-referred noise of the tail current source can be visualized using Fig. 5.7 and is the current division between the two branches. Overall the input-referred noise of the tail current source can be computed as:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,MCS}}} = S_{\Delta \mathrm{I}^2_{\mathrm{n,CS}}} \left[\frac{\omega\, C_{\mathrm{GS1}}}{2\, g_{\mathrm{m,M1}} + \omega\, C_{\mathrm{GS1}}} \right]^2 . \tag{5.10}$$

At low frequencies, eq. (5.10) simplifies to:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,MCS}}} \approx \frac{S_{\Delta \mathrm{I}^2_{\mathrm{n,CS}}}}{4\, g^2_{\mathrm{m,M1}}} \left(\omega\, C_{\mathrm{GS,M1}}\right)^2 . \tag{5.11}$$

Consequently, at lower frequencies, the contribution of the tail current source to the overall TIA noise can be made negligible by proper biasing of the tail current source in strong inversion, device sizing to minimize its flicker noise contribution and designing the input pair with a sufficiently large transconductance. However,

at higher frequencies, eq. (5.10) becomes:

$$S_{\Delta \mathrm{I}^2_{\mathrm{IN,MCS}}} \approx S_{\Delta \mathrm{I}^2_{\mathrm{n,CS}}}, \tag{5.12}$$

due to the current branch through C_{GS1} indicating the need for designing the tail current source with sufficiently low high-frequency current noise, i.e. sufficiently high inversion coefficients. Alternatively, noise reduction techniques such as source degeneration can be adopted to attenuate the noise of the tail current source.

5.2.4 Modeling thermal and flicker noise of MOSFETs

The current noise PSD of a MOSFET, $S_{\Delta \mathrm{I}^2_{\mathrm{n,M}i}}$, that occurs in the expressions for the input-referred TIA noise in the previous discussion includes a number of different physical noise sources inside the device. The two most important noise sources are the noise due to the resistance of the inversion channel and flicker noise originating from mobility fluctuations and fluctuations of the number of carriers in the channel due to interface defects. In this work, we look closely in the design space and how to pick the bias points of the noise-critical transistors for an optimized noise behavior. First, we examine the gate-referred thermal noise of a MOS transistor which can be expressed as:

$$S_{\Delta \mathrm{V}^2_{\mathrm{IN,thermal}}} = \frac{4kT\gamma}{g_{\mathrm{m}}}, \tag{5.13}$$

where γ is the thermal noise excess factor. As a result, lowering the thermal noise floor can be accomplished by increasing the transconductance g_{m}. This is usually achieved by either increasing the bias current without changing the transistor's dimensions, or by increasing the aspect ratio W/L to increase g_{m} without additional power penalty. The latter solution introduces extra gate capacitance increasing the total input admittance, and eventually, results in a higher noise floor at higher frequencies. Overall, thermal-noise limited designs, such as [67], adopts a design methodology of increasing the bias current as much as possible without changing the transistor's dimensions. For such cases, the upper limit of this approach is the allowed voltage headroom around the transistor. In designs limited by thermal noise, the design tradeoff is simple: Increase the current as much as possible, as long as the voltage headroom allows.

Unfortunately, all designs presented in the literature striving for low flicker noise performance have adopted a single design strategy which is choosing a PMOS transistor for the input stage for its superior flicker noise performance. For older technologies (down to 0.18 µm), the channel of the PMOS transistor was usually buried in the substrate, and hence, the traps between the oxide and the channel were minimized [71]. In such technologies, flicker noise can be neglected during the noise optimization process. However, in advanced technologies, flicker noise can be problematic and might dominate the total noise. A simplified expression of the gate-referred flicker

voltage noise PSD of a MOSFET $S_{\Delta V^2{}_{IN,flicker}}$ can be extracted as:

$$S_{\Delta V^2{}_{IN,flicker}} = \frac{KF}{C_{ox} \cdot W_{eff} \cdot L_{eff} \cdot f^{EF}}, \tag{5.14}$$

where KF is the flicker noise coefficient, C_{ox} is the oxide capacitance per unit area, and W_{eff} and L_{eff} are the effective gate width and length, respectively. Even this simplified model clearly reveals the tradeoff between lowering the input-referred current noise PSD due to the flicker noise of the input pair presents itself. By simply increasing the effective width and length of the input pair, $S_{\Delta V^2{}_{IN,flicker}}$ can be reduced while increasing the input admittance due to the increased gate capacitance. The optimum gate capacitance is already derived in [67] and is given by:

$$C_{GG} = C_{DUT} + C_{FB}. \tag{5.15}$$

Combining the results of eqs. (5.13), (5.14) and (5.15), the tradeoffs in reducing the flicker noise are still simple since the flicker noise is bias independent. As a result, the bias point is chosen based on the thermal noise floor requirements (in strong inversion), while the flicker noise is set by choosing $W \cdot L$ satisfying the condition defined by eq. (5.15). Unfortunately, the assumption that flicker noise is bias independent, is far from true for many technologies. The simple flicker noise model shown in eq. (5.14) disregards important information about the relationship between flicker noise and the bias point. In this thesis, we adopt a more precise flicker noise model provided in the BSIM4 MOSFET model, in which the gate-referred flicker noise is given by [72]:

$$S_{\Delta V^2{}_{IN,flicker}} = \frac{KF \cdot I_{ds}^{AF}}{C_{ox} \cdot L_{eff}^2 \cdot f^{EF} \cdot g_m^2}, \tag{5.16}$$

where EF (≈ 1) is the flicker noise frequency exponent modeling the slope of the flicker noise and AF (≈ 1) is the flicker noise exponent. For a given technology, all coefficients of eq. (5.16) can be extracted from simulations. It is worth noting that while the width W does not appear directly in eq. (5.16) it is implicitly included in I_{ds}^{AF}/g_m^2. Eq. (5.16) shows that flicker noise can be reduced by choosing the bias point of the MOSFET in weak inversion where g_m/I_{ds} is maximized. This introduces a strong design tradeoff since, for lower flicker noise, weak inversion operation is beneficial. On the other hand, the shaped thermal noise can be reduced by biasing the input pair in strong inversion.
In summary, the following statements are applicable for the design of the differential pair:

- To reduce flicker noise, maximizing g_m/I_{ds} is desired without significantly increasing $C_{GG} + C_P + C_{FB}$. This can be achieved by biasing the transistors in weak inversion.

– To reduce thermal noise, maximizing g_m is desired without significantly increasing $C_\mathrm{GG}+C_\mathrm{P}+C_\mathrm{FB}$. This can be achieved by biasing the input differential pair deeply in strong inversion. This constraint is particularly important for applications with f_fc comparable or lower than the actual signal's bandwidth.

Since most designs suffer from both types of noise, we will discuss in the following parts how to pick an optimum design point depending on the sensor's and technological parameters.

Designing for minimum opamp noise

In the following, we will derive design equations for the total opamp noise. Typically, there is a finite set of design variables namely the input transistors' width W and length L, as well as their drain current I_ds. Consequently, the proposed design equations would only include these variables. As a first step, the transconductance g_m in eq. (5.16) is substituted by a single equation valid in all bias operation regions, i.e. weak, moderate and strong inversion operation. According to the EKV model [73], g_m can be expressed as:

$$g_\mathrm{m} = \frac{2 \cdot I_\mathrm{ds}}{n \cdot U_\mathrm{T}. \cdot \left(1 + \sqrt{4 \cdot \mathrm{IC} + 1}\right)}, \tag{5.17}$$

where n is the slope factor, U_T is the thermal voltage, and IC is the inversion coefficient. The value of IC reflects the operating region of the transistor and can be related to physical transistor parameters according to:

$$\mathrm{IC} = \frac{I_\mathrm{ds}}{2 \cdot n \cdot \mu \cdot C_\mathrm{ox} \cdot U_\mathrm{T}^2 \cdot \frac{W}{L}}, \tag{5.18}$$

where μ is the carrier mobility and C_ox is the oxide capacitance per unit area. On the other hand, the capacitances in eq. (5.3) can be approximated as:

$$\begin{aligned} C_\mathrm{GG} &\approx \frac{2}{3}\left(W \cdot L \cdot C_\mathrm{ox}\right) + C_\mathrm{GSo} + C_\mathrm{GDo}, \\ C_\mathrm{GD} &\approx C_\mathrm{GDo}, \qquad C_\mathrm{GS} \approx \frac{2}{3}\left(W \cdot L \cdot C_\mathrm{ox}\right) + C_\mathrm{GSo}, \end{aligned} \tag{5.19}$$

where C_GSo and C_GDo are the gate-source and gate-drain overlap capacitances, respectively. It is worth mentioning that these equations are only valid for strong inversion and saturation operations, however, they provide a very good approximation to the total capacitance. Now, the transconducatnce g_m is expressed as a function of the aforementioned design parameters W, L and I_ds.

5.2.5 Design example

Next, the design equations introduced in the previous sections are used within our noise-aware TIA design methodology. First, a design example of a current sensor

with its parasitic capacitance of $C_{\mathrm{DUT}} = 2\,\mathrm{pF}$ is assumed. Also, assuming $R_{\mathrm{FB}} = 10\,\mathrm{G\Omega}$, dictated by the maximum input current and the required dynamic range, and $C_{\mathrm{FB}} = 50\,\mathrm{fF}$ to ensure stability/acceptable peaking in the frequency response, the design is optimized to achieve optimal noise performance. Since the design of the opamp would depend primarily on the frequency of operation, the design will be optimized for two different operating frequencies of 50 kHz (medium-speed design) and 5 MHz (relatively high-speed design).

Finding the optimized design parameters

The first step of the proposed design procedure is to extract all required technology parameters namely KF, EF, C_{ox}, C_{GSo}, C_{GDo} and the slope factor n. All these parameters can be extracted from the process's datasheet, and/or SPICE simulations. For this design example, we use a 180 nm CMOS partially depleted (PD) SOI technology. The transistor length of the input transistors, L, is then typically chosen to achieve a good tradeoff between gain and speed. Here, we chose $L = 250\,\mathrm{nm}$. Now, the optimum transistor width W and bias current I_{ds} are to be evaluated to achieve the best noise performance for both the 50 kHz and 5 MHz design cases. The analytical model presented in the previous section can be used to create a 3D plot of the input-referred current noise as a function of W and I_{ds}. From the 3D plots, the optimum W and I_{ds} can be extracted for all NMOS and PMOS transistor flavors in the design kit. In this technology, low-threshold PMOS transistors show the best noise performance for both designs. It is worth mentioning that changing the design requirements or sensor's parasitics might result in a different optimum transistor flavor. Figures. 5.8 and 5.9 show the input-referred TIA noise for PMOS input transistors at a frequency of 50 kHz and 5 MHz, respectively. The optimum design choices for W and I_{ds} can directly be extracted from the global minimum of the 3D plot over the tolerable power range.
To clarify the effect of choosing different I_{ds} and W on the noise performance, marginal plots of the input-referred noise as a function of transistor width W for discrete values of I_{ds} are shown to the right of the plots. The marginal plots illustrate two important conclusions. First, increasing current does not necessarily lower the noise floor as observed in the optimized design at 50 kHz, cf. Fig. 5.8 (right). This is due to the increase of the flicker noise when the bias current increases, i.e. shifting the operation of the input pair to stronger inversion levels. On the other hand, increasing the bias current can lower the thermal noise floor for the optimized design at 5 MHz. In this case, increasing the current would increase the flicker noise corner frequency f_{fl}, however, the corner frequency is still lower than the frequency of operation. The second important observation from the two marginal plots is that the optimum transistor's width depends on the bias current inside the opamp. This dependence is not shown in [67] where the optimum width, or gate capacitance C_{GG}, depends solely on the input capacitance of the system, cf. eq. (5.15). Moreover, the effect of C_{DUT} on the overall noise performance is investigated. To this end, C_{DUT} is swept from 200 fF to 10 pF and optimum design parameters for the width W and

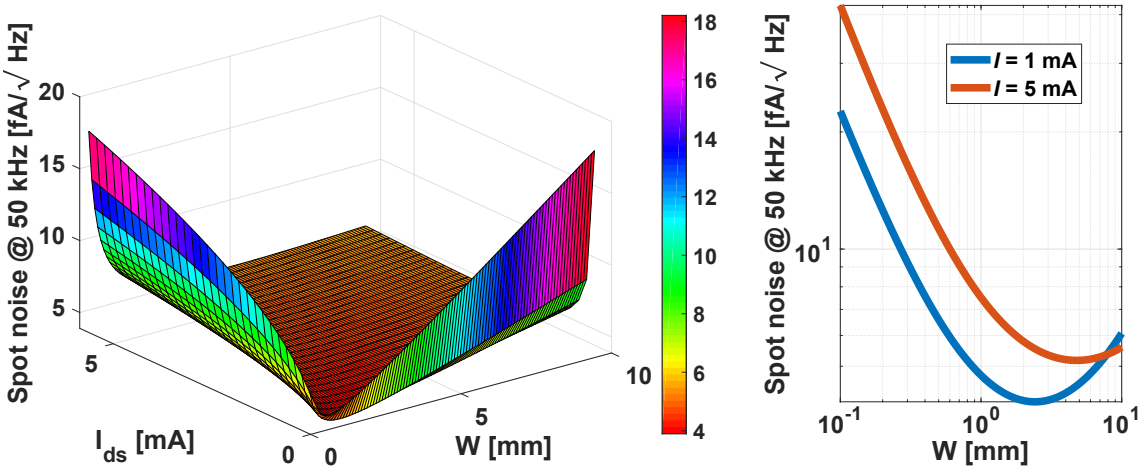

Figure 5.8: 3D plot of the TIA input-referred spot noise of the input transistors at 50 kHz as a function of W and I_{ds}.

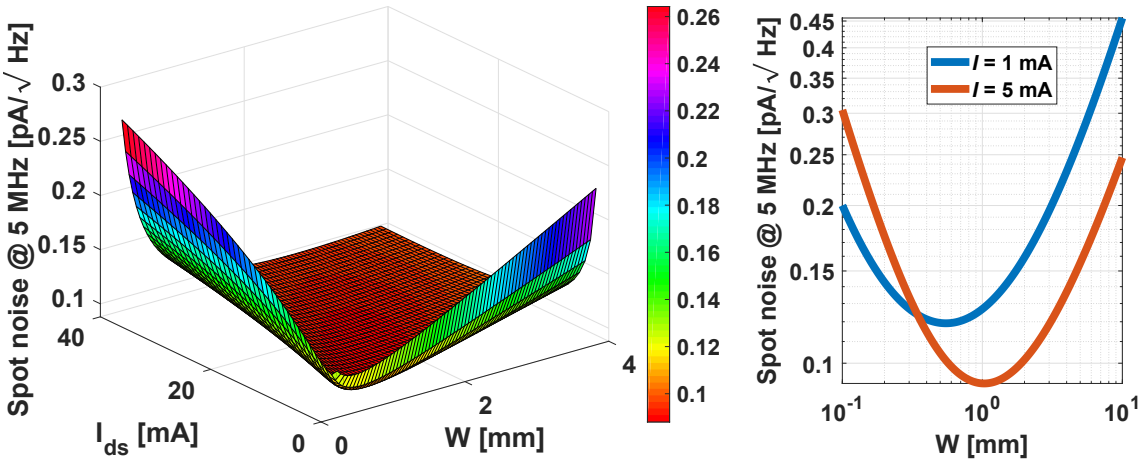

Figure 5.9: 3D plot of the TIA input-referred spot noise of the input transistors at 5 MHz as a function of W and I_{ds}.

bias current I_{ds} of the input transistors are found using the proposed approach. Fig. 5.10 shows the optimum device width and bias current for $L = 250\,\mathrm{nm}$ for designs optimized at 50 kHz, 500 kHz and 5 MHz. While the increase in the optimum W is mostly linear with an increase in C_{DUT}, cf. Fig. 5.10a, the optimum current varies by two orders of magnitude, cf. Fig. 5.10b. It is also shown that the optimum transistor's width W is mostly independent on the frequency of operation. Overall the results of Figs. 5.10a and 5.10b show that by biasing the input differential pair at a lower IC for the 50 kHz design leads to a lower input-referred noise. For faster designs, increasing the bias currents and using a higher IC results in an optimum noise performance, as suggested in [74]. For each of the three designs, the optimum spot noise is shown in Fig. 5.11 while sweeping C_{DUT}. As expected, the optimum noise performance degrades with increasing C_{DUT} and operating frequency.

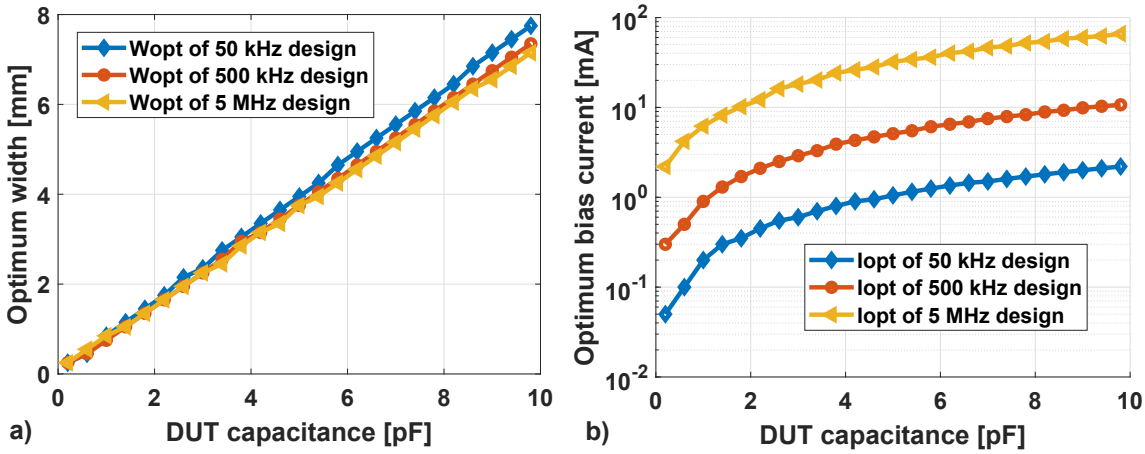

Figure 5.10: a) Optimum width and b) optimum bias current of the input differential pair as a function of C_{DUT} for designs optimized at 50 kHz, 500 kHz and 5 MHz.

Comparison between the analytical and the simulated model

To verify the usefulness and benefits of the proposed design approach, we have compared it against a design optimization that only takes thermal noise into account. The design optimized for thermal noise has been found using the approach of [67], which suggests to maximize I_{ds}, while fulfilling the relationship $C_{\mathrm{GG}} = C_{\mathrm{DUT}} + C_{\mathrm{FB}}$. Choosing an inversion coefficient deeply in strong inversion (IC = 75), this design approach results in an optimum width of $W = 1\,\mathrm{mm}$ and a current of $I_{\mathrm{ds}} = 28\,\mathrm{mA}$. This design is compared against the two designs optimized for minimum spot noise at frequencies of 50 kHz and 5 MHz with the proposed method that evaluates the analytical model equations presented in this work, taking into account thermal and flicker noise. The corresponding simulation results are shown in Fig. 5.12. According to the figure, the designs optimized for flicker and thermal noise consume significantly less current while achieving a significantly better noise performance in the case of the 50 kHz design and an identical noise performance in the case of the 5 MHz design. This clearly shows that, especially for low to medium-frequency designs, excessive currents lead to increased flicker noise that degrades the overall TIA performance, cf. Fig. 5.8 (right). Even for relatively high-speed designs, taking flicker noise into account greatly saves power and results in a significantly reduced TIA noise. Finally, we have verified the accuracy of the proposed analytical model by comparing it against Spectre simulations of the circuit of Fig. 5.5, extended by cascode devices to produce sufficient open-loop gain in the OTA. The corresponding simulation results for the 50 kHz optimized design are shown in Fig. 5.13. The blue curve depicts the noise predicted from the proposed analytical model and the red and yellow curves correspond to Spectre simulations including the noise of the differential pair only and all transistors, respectively. According to the figure, the proposed analytical model shows very good agreement with the red curve, the small difference around the corner frequency originating from the inaccuracy of the simplified flicker

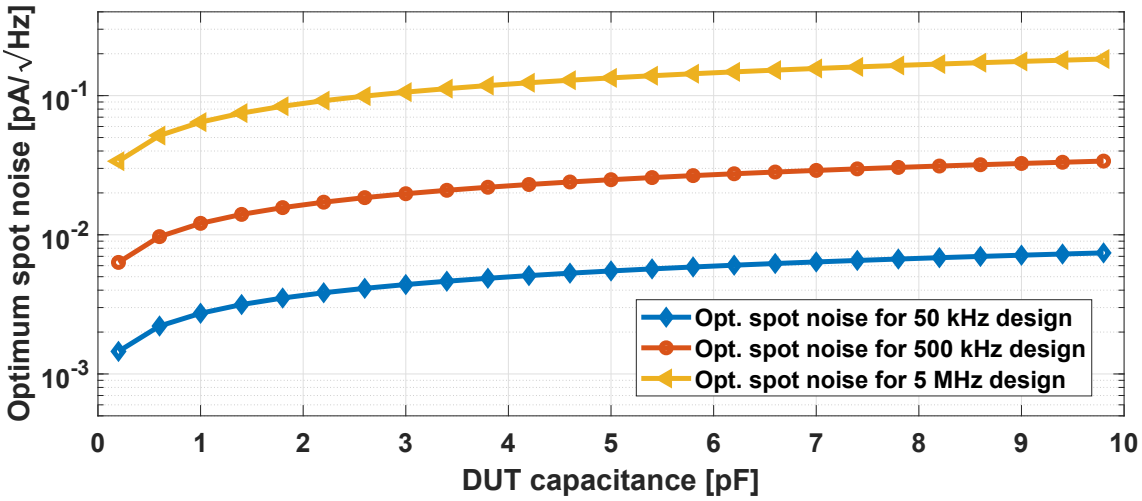

Figure 5.11: Optimized spot noise of the TIA at 50 kHz, 500 kHz and 5 MHz as a function of C_{DUT}.

noise model of eq. (5.16). The additional discrepancy between the analytical model and the simulation including all noise sources for very large frequencies beyond the OTA's gain bandwidth originates from additional noise due to the tail current source.

5.3 Conclusions

In this chapter, first, a brief review of different TIA topologies was given. More specifically, the difference between OL and CL TIAs in terms of their noise-speed tradeoff was highlighted. Since this work is dedicated to low-noise designs, the noise of CL TIAs is examined in detail. More specifically, we introduced, in detail, a list of analytical equations modeling the noise of noise-critical transistors in TIAs and their embedded opamps. As shown, the noise of the input differential pair can dominate the entire noise performance, followed by the noise of the current mirror loads and, surprisingly, the noise of the tail current source. The latter source of noise is visible due to the single-ended nature of most TIAs. Several important conclusions are drawn from our analysis, which are also published in [9]. First, a design methodology based on lowering the thermal noise, by increasing the bias current, does not necessarily lower the input-referred current noise of a TIA. On the contrary, for flicker noise limited designs, an increase in the bias current shifts the operation of the differential input pair into strong inversion, and ultimately, the flicker noise corner frequency f_{fl} is shifted to higher frequencies. Surprisingly, our analytical model shows that, in low-speed designs, a lower current bias can lead to a lower noise floor. On the other hand, high-speed designs can benefit from increasing the bias current where f_{fl} is kept way lower than the frequency of operation. Secondly, while our design equations are relatively simple and comprise only very few design

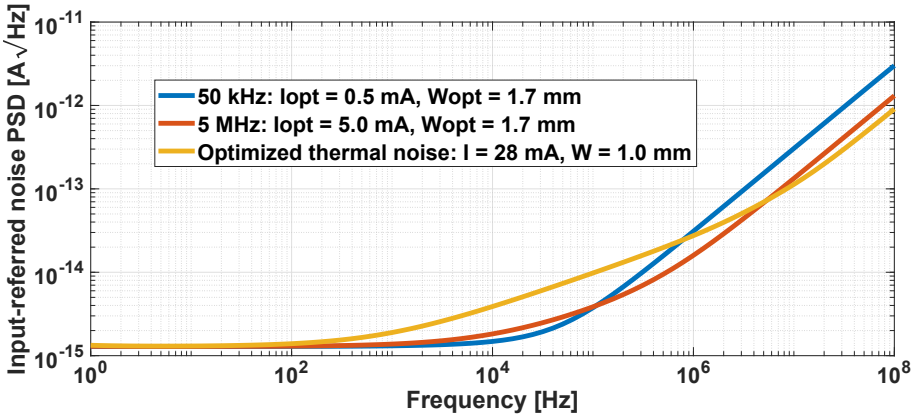

Figure 5.12: Comparison of two design optimized for spot noise at 50 kHz and 5 MHz using the method proposed in this paper against a conventional design optimized for thermal noise only and independent of the operating frequency.

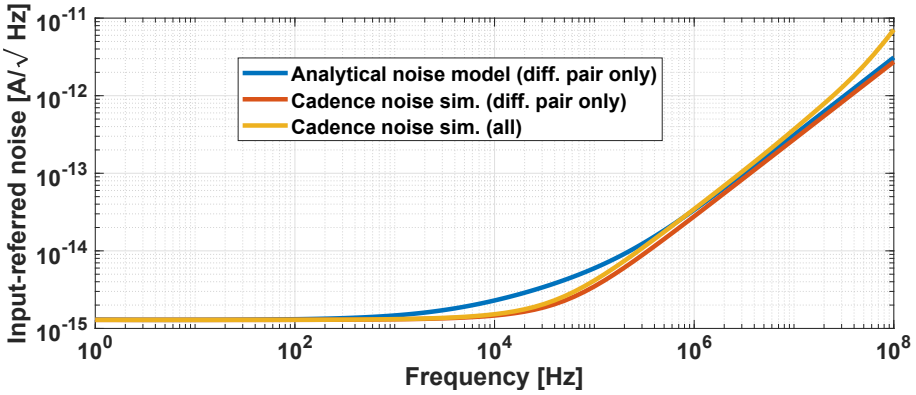

Figure 5.13: Comparison of the proposed analytical model against Spectre simulations.

and technological variables, they match, to a very large extent, with the Spectre simulations performed on a design example on 180 nm SOI technology. Another conclusion drawn from our work is that the optimum gate-capacitance of the input differential pair C_{GG} depends on the bias current and not only the sensor's capacitance C_{DUT} and feedback capacitance C_{FB} as shown in [67]. Interestingly, for given bias currents, the optimum gate-capacitance C_{GG} is independent, to a large extend, of the frequency of operation. This being said, our simple design model, based on analytical equations and technological parameters, can be used as a guideline to circuit designers offering a noise-aware design methodology for TIAs.

6 A frontend for MR sensors using a current-mode $\Sigma\Delta$ modulator

In chapter 5, we introduced a detailed noise model of ultra-low noise TIAs and a noise-aware design methodology of low-noise closed-loop TIAs. We also showed that these equations are valid for R-TIAs, C-TIAs and current-mode $\Sigma\Delta$ modulators. In this chapter, we discuss the design of a continuous-time current-mode $\Sigma\Delta$ modulator (CT C-SDM) for both biosensing as well as life science sensing applications. The reasons behind choosing CT C-SDMs over R-TIAs and C-TIAs are discussed in this chapter by introducing the advantages and tradeoffs of CT C-SDMs compared to R-TIAs and C-TIAs in terms of power consumption, area and achievable noise performance. Following this discussion, the design procedure of a CT C-SDM is introduced and validated by a chip design of a CT C-SDM with finite impulse response (FIR) feedback for jitter immunity. Moreover, this design features a DSL, similar to that of C-TIAs, to increase the dynamic range of a CT C-SDM in the presence of large DC current offsets.

6.1 Towards the design of compact TIAs

Recent quantum and life science applications create an expanding need for current frontends with excellent noise performance and large dynamic ranges. An example of such applications includes quantum magnetometers based on nitrogen vacancy (NV) centers in diamond [75, 76]. The excitation of such systems is done by green laser and their readout comprise of photodiodes detecting the red fluorescence signal of the NV centers. Afterwards, their output current is typically amplified by a low-noise TIA to maintain the intrinsic SNR of the input diode. Unfortunately, the desired red fluorescence signals are typically very small and are superimposed on large undesired signals originating from the excitation signal by green light. As a result, very low-noise TIAs are needed to resolve the small red fluorescence signal. On the other hand, a large dynamic range is essential to ensure proper TIA operation without being disturbed by the undesired green laser. This is very similar to the readout of MR sensors, where the signal component is encoded in the small-signal resistance, while the base resistance is contained in the DC part of the resistance. By applying a voltage bias to the MR sensor, a current output with a large unwanted DC component and a smaller desired AC component is processed by the TIA. For such applications, TIAs are realized either with a resistive feedback (R-TIA) [77] or with a capacitive feedback (C-TIA) as shown in Fig. 6.1. The TIA is then followed by

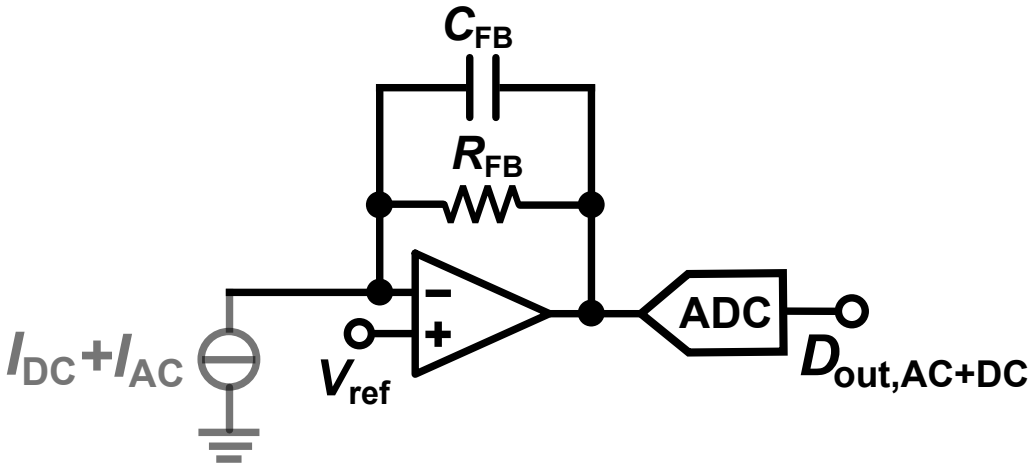

Figure 6.1: Generic R- and C-TIAs with subsequent ADC.

an ADC to digitize the analog signal. The tradeoffs of large undesired DC currents and noise can be understood for both R-TIAs and C-TIAs as follows: Larger DC currents forces the usage of smaller feedback resistors R_{FB} for R-TIAs which directly translates to an increase in the thermal noise floor. The ADC that follows the R- or C-TIAs also suffers from a low transimpedance in the prior TIA stage. For a large transimpedance, the noise of the ADC, composed of quantization and electronic noise, is attenuated by the transimpedance gain when referred to the input of the system. Now, because of the lower transimpedance value, the noise of the ADC has to be heavily reduced to keep the input-referred noise of the system unaltered. As a result, the overall power consumption of the ADC is expected to increase because of the small transimpedance dictated by the undesired DC currents. To mitigate these drawback in R-TIAs and C-TIAs, a DC servo loop (DSL) is frequently added around the TIA to separate the AC and DC signals [63, 62]. The AC signal processed by the TIA, is then digitized by an ADC as illustrated in Fig. 6.2. In this scheme, the AC and DC signals are separated from each other. Although the analog DC output $V_{\mathrm{out,DC}}$ requires an ADC with a large dynamic range, it still can be digitized with a lower resolution ADC compared to the ADC processing the smaller AC signals. As a result, the noise-power tradeoff tradeoff is relaxed by using a large transimpedance value in the TIA and an ADC with higher tolerable noise floor. However, using a TIA followed by an ADC consumes more power and area than directly digitizing the current with a current-input ADC [78]. A promising candidate for a low-noise current-mode ADC, cf. Fig. 6.3a that can directly digitize the sensor current output signal is a current-mode ΣΔ modulator (C-SDM) [79, 80]. This approach removes the need for an additional frontend TIA and, hence, can be more compact and power efficient. However, in this approach, large DC currents accompanying the AC signals can be problematic since they can degrade the modulator's effective dynamic range for the AC signal. Moreover, a direct consequence of the large DC currents is an increase in the quantization noise as well as the thermal noise of the C-SDM.

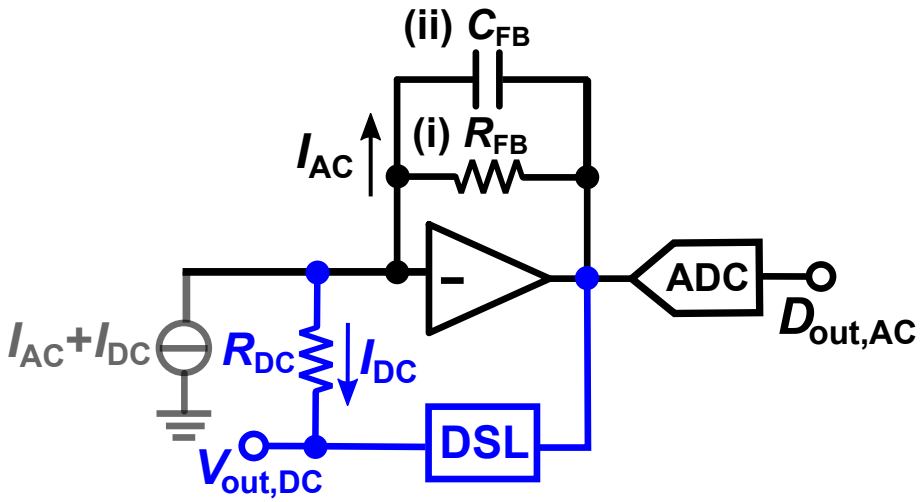

Figure 6.2: Generic R- and C-TIAs with subsequent ADC and a DSL to increase the readout's dynamic range.

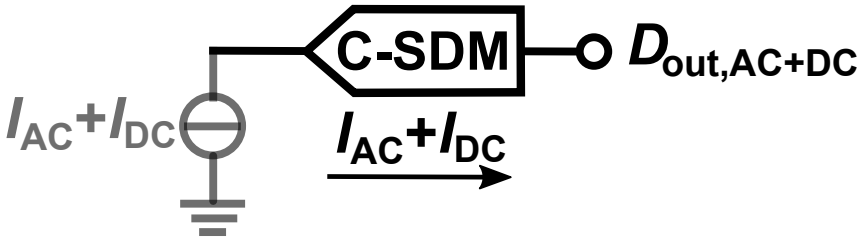

Figure 6.3: Generic current-mode ADC.

This is explained in details together with the operation of a CT C-SDM in the next sections.

6.2 CT C-SDM: Concepts and design tradeoffs

In this section, the design process of a CT C-SDM is presented alongside with the design strategy of the critical blocks of the modulator. This includes the proper choice of a feedback DAC to ensure clock jitter robustness, sufficient anti-aliasing filtering (AAF), as well as relaxing the linearity requirements of the first integrator. Furthermore, the tradeoffs between speed, quantization noise, electronic noise, dynamic range and power consumption are introduced. Finally, two SoA designs incorporating a CT C-SDM frontend are discussed and their advantages and disadvantages are evaluated before introducing our CT C-SDM design.

6.2.1 CT C-SDM design fundamentals

Fig. 6.4 shows the block diagram of a generic CT C-SDM. Interestingly, the structure of a current-mode CT SDM is very similar to a voltage-mode CT SDM except for

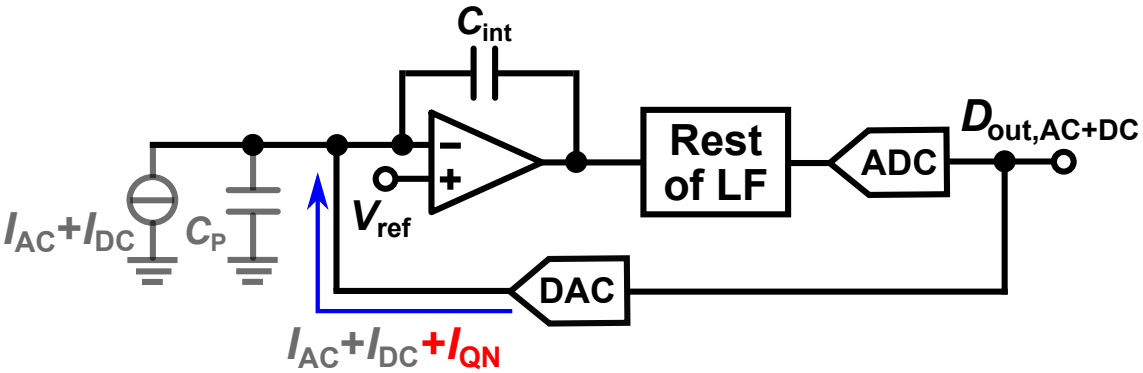

Figure 6.4: Generic block diagram of a CT C-SDM.

the input stage. In a current-mode SDM, the input resistor of the classical RC integrator in a voltage-mode SDM is omitted. As a result, the input-impedance is significantly lowered by the open-loop gain of the embedded amplifier of the first integrator stage providing a close-to-ideal load to the current-mode sensor. Another fundamental difference between the voltage- and the current-mode modulators is the parasitic capacitance introduced at the input. In a voltage-mode SDM, the input resistor of the first RC integrator is implemented on-chip, as a result, any parasitic capacitance at the input of the chip due to traces, ESD capacitance at the chip pads or the sensor, are driven by the input voltage source. In C-SDMs, however, the parasitic capacitance C_P is located at the virtual ground of the first integrator. As a result, such undesired capacitances load the integrator, and could lead to severe SNR degradation or possible instability as will be discussed in detail in section 6.2. The advantages of a CT C-SDM are similar to a voltage-mode SDM. Most importantly, the inherent anti-aliasing filtering property of the CT loop filter allows interfacing sensors directly with a CT modulator without the need for an extra AAF filter [80]. The operation of the C-SDM is explained as follows: The large loop gain inside the modulator, formed by a single or a cascade of integrators, ensures that the average feedback current signal, i.e. the DAC's output in Fig. 6.4, is equal to the input signal. As a result the modulator's output, which is also the outermost DAC's input, is nothing but the digital representation of the input signal together with the modulator's quantization noise. Similar to voltage-mode SDMs, the quantization noise depends on multiple factors, such as the modulator's order, the number of bits in the internal ADC, the chosen NTF and the oversampling ratio.

DAC tradeoffs

The internal ADC in the SDM has N-bits of resolution. As a result, the feedback DAC has the same resolution. The full-scale of the feedback DAC plays an important role in the modulator's operation while influencing its quantization noise floor. This can be understood by the simple sketch shown in Fig. 6.5 showing the transfer characteristics of an N-bit DAC. The two most important parameters of the DAC

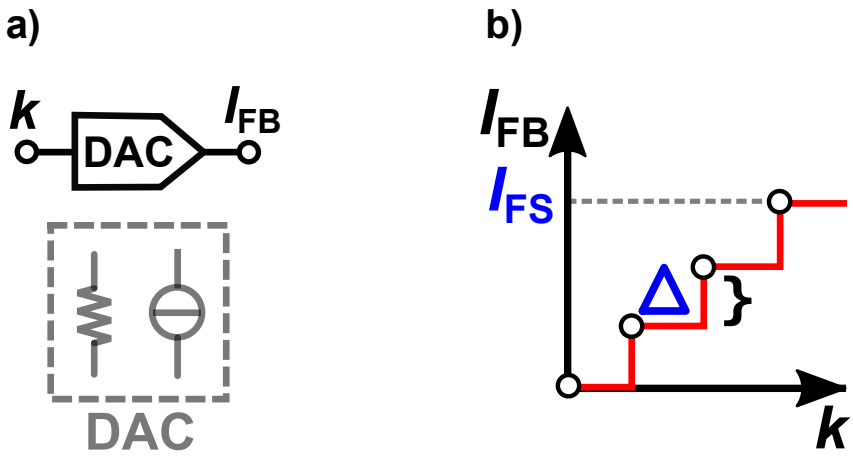

Figure 6.5: a) Block diagram of a generic DAC. b) Transfer characteristics of an N-bit DAC.

are the full-scale output current of the DAC, I_{FS}, and the quantization step Δ. It is worth mentioning that the quantization step is not generated by the DAC per se but is the outcome of the finite quantization levels in the ADC. For an N-bit DAC, the quantization step is computed as follows:

$$\Delta = \frac{I_{\mathrm{FS}}}{2^N - 1}. \tag{6.1}$$

Clearly, choosing a smaller quantization step, or quantization error, is helpful to reduce the quantization noise floor. However, for a fixed DAC design with a fixed number of bits N, a smaller quantization error leads to a reduced full-scale current I_{FS}, cf. eq. (6.1). Choosing a proper I_{FS} is important for the stability of the modulator and the largest input signal you want to quantize, as well as the noise performance of the modulator. The stability of a C-SDM is similar to that of a voltage-mode SDM. In the latter, a modulator is stable as long as the input voltage is smaller than or equal the maximum stable amplitude (MSA) of the modulator. Similarly, I_{FS} has to be larger than the input current I_{in} to ensure proper operation. The minimum I_{FS} ensuring stability depends on the order of the loop filter, the number of quantization bits in the internal ADC, and the aggressiveness of the NTF. Although increasing I_{FS} greatly beyond I_{in} can provide a safety margin for stability, two major tradeoffs can be expected. First, larger I_{FS} yields a higher quantization error as explained shortly above. Secondly, an indirect consequence of increasing I_{FS} is the higher electronic noise. For example, a current steering DAC can be implemented for the feedback DAC with an $I_{\mathrm{FS}} = 1\,\mathrm{mA}$. Increasing the full-scale current to $I_{\mathrm{FS}} = 10\,\mathrm{mA}$, by placing more transistors in parallel, would increase the current noise floor PSD by a factor of ten. This tradeoff is very similar to R-TIAs, where a larger input current necessitates smaller feedback resistors, and hence, an increase in the input-referred noise is inevitable. Now, it is important to draw the following conclusion: A large DC current component at the input of the C-

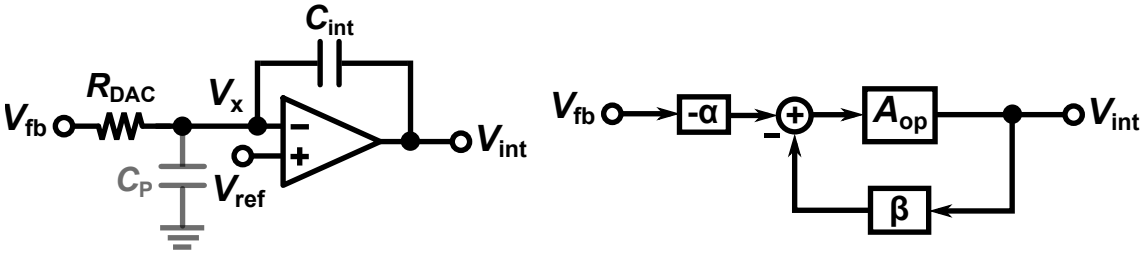

Figure 6.6: a) Schematic diagram of the first integrator. b) Equivalent block diagram of the first integrator.

SDM requires a DAC with a sufficiently large I_{FS} to ensure stability. Consequently, this limits the achievable signal to quantization noise ratio (SQNR) as well as the overall SNR of the modulator.

First opamp design considerations

Another critical block in the C-SDM is the first integrator, and specifically, the design of its embedded opamp for multiple reasons. First, errors generated by the opamp, including noise and non-linearities, are not shaped by the loop filter. Moreover, the opamp's speed, or unity-gain frequency (ω_{UGF}), has to be chosen large enough to drive the large parasitic capacitance C_{P} at the input without adding large delay to the loop. As a rule of thumb, the ω_{UGF} of the integrator can be chosen around 1-2 f_{s} for stable operation of a CT modulator [81]. Fig. 6.6 shows a block diagram of an active RC integrator with a parasitic capacitance C_{P} for a resistive feedback DAC. Now, the effect of the finite ω_{UGF} of the amplifier on the closed-loop transfer function of the integrator with large parasitic capacitances C_{P} is analyzed. To model the finite speed of the opamp, a simple model for the opamp A_{op} with infinite DC gain and a finite bandwidth is used. Overall, the open-loop response of the amplifier is modeled as $A_{\mathrm{op}} = s/\omega_{\mathrm{UGF}}$. Next, the feedforward and the feedback gains α and β, respectively, cf. Fig. 6.6, are derived to obtain the closed-loop gain of the integrator. The equivalent circuit models used to derive α and β are shown in Figs. 6.7b and c. Overall, α and β are given by:

$$\alpha = \frac{1}{1 + s \cdot R_{\mathrm{DAC}} \cdot (C_{\mathrm{P}} + C_{\mathrm{int}})}, \tag{6.2a}$$

$$\beta = \frac{s \cdot R_{\mathrm{DAC}} \cdot C_{\mathrm{int}}}{1 + s \cdot R_{\mathrm{DAC}} \cdot (C_{\mathrm{P}} + C_{\mathrm{int}})}. \tag{6.2b}$$

Combining the results of the above equations, the closed-loop transfer function of the integrator becomes:

$$\frac{V_{\mathrm{int}}}{V_{\mathrm{fb}}} = \frac{-\alpha \cdot A_{\mathrm{op}}}{1 + \beta \cdot A_{\mathrm{op}}} = \frac{-1}{(s \cdot R_{\mathrm{DAC}} \cdot C_{\mathrm{int}})(1 + s/\omega_{\mathrm{nd}})}, \tag{6.3}$$

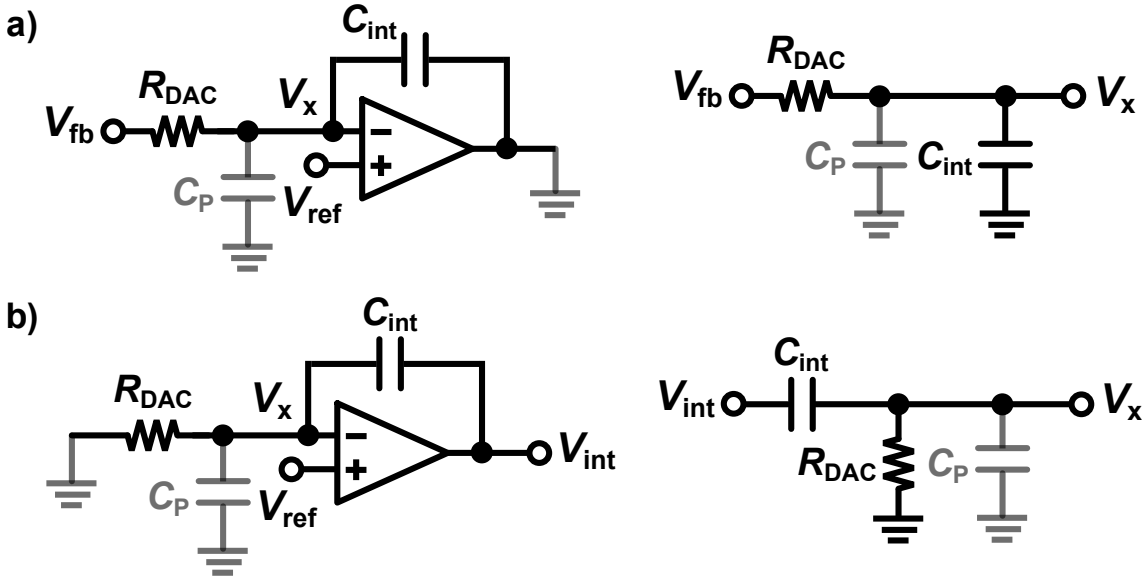

Figure 6.7: a) Schematic diagram used to obtain α. b) Schematic diagram used to obtain β.

where ω_{nd} is a non-dominant pole and can be expressed as follows:

$$|\omega_{\mathrm{nd}}| = \frac{1 + (\omega_{\mathrm{UGF}} \cdot R_{\mathrm{DAC}} \cdot C_{\mathrm{int}})}{R_{\mathrm{DAC}} \cdot (C_{\mathrm{P}} + C_{\mathrm{int}})}. \tag{6.4}$$

Assuming $\omega_{\mathrm{UGF}} \gg 1/R_{\mathrm{DAC}} \cdot C_{\mathrm{FB}}$, the non-dominant pole frequency ω_{nd} of the integrator can be written according to:

$$|\omega_{\mathrm{nd}}| = \omega_{\mathrm{UGF}} \frac{C_{\mathrm{int}}}{C_{\mathrm{P}} + C_{\mathrm{int}}}. \tag{6.5}$$

Consequently, the parasitic capacitance at the input of the integrator shifts the non-dominant pole frequency ω_{nd} to a lower frequency, and as a result, increases the loop delay. To counteract this adverse effect, the speed of the embedded opamp ω_{UGF} is typically increased worsening the power-efficiency of the modulator. Alternatively, the value of the integration capacitance C_{int} can be also increased at the expense of larger chip area and higher slew-rate requirements.
The speed of the opamp is one important design criterion setting the lower limit on its power consumption. However, the noise of the opamp is an equally important design parameter that can determine the power consumption of the opamp. In chapter 5, a detailed analysis of the noise of the TIA is presented for R-TIAs, C-TIAs and C-SDMs, as well as the noise-shaping of the embedded opamp when referred to the input node. Considering both noise and speed requirements of the opamp, a proper decision regarding the power consumption of the opamp can be made.

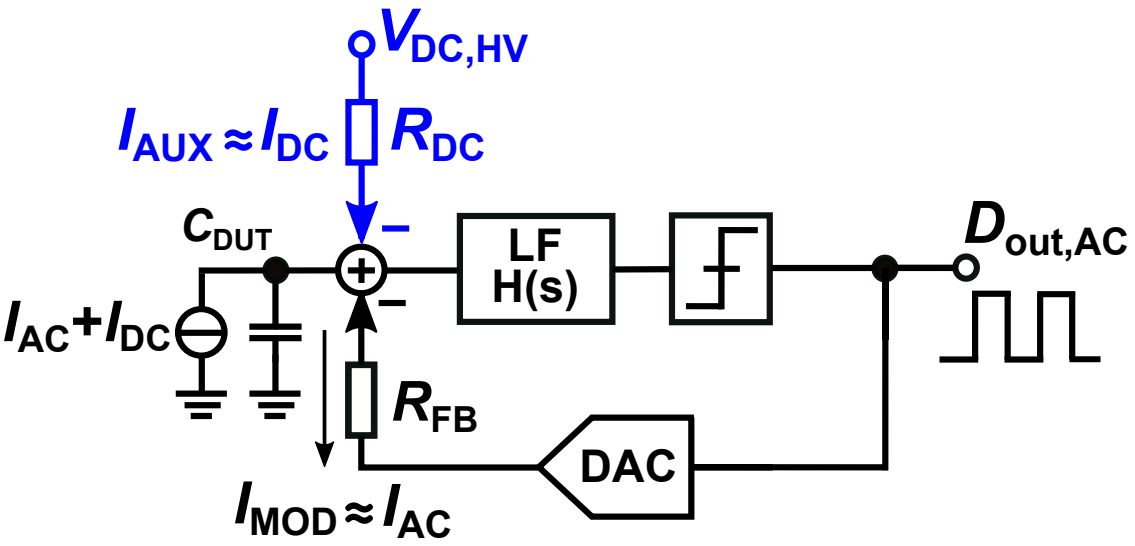

Figure 6.8: Block diagram of a generic C-SDM with a DC path to source/sink the undesired DC current.

6.3 Improving the dynamic range of C-SDMs using DSLs

As discussed in the previous section, there is an implicit tradeoff between the dynamic range and the noise floor of an SDM. This tradeoff is aggravated in the case of input DC currents. Here, we try to break this tradeoff to increase the useful dynamic range of the SDM, while simultaneously improving the system's noise floor.

6.3.1 Steering the DC current away from the DSM

The simplest idea to break the aforementioned tradeoff is to source or sink the DC current away from the SDM. Fig. 6.8 shows a block diagram of a generic C-SDM (in black) with a feedback resistor R_{FB} forming the current feedback DAC. Since the input node of a CT C-SDM is a virtual ground, cf. Fig. 6.4, a current-summation node can be easily formed by connecting an auxiliary resistor R_{DC} biased at suitable a DC-voltage $V_{\mathrm{DC,HV}}$ (in blue). By precisely controlling $V_{\mathrm{DC,HV}}$, the entire DC current can be steered away from the C-SDM. In this case, the feedback resistance R_{FB} can be significantly increased, since the modulator does not need to handle the large DC currents, improving the quantization noise as well as electronic noise floor. It is important to point-out that in order to improve the electronic noise floor of the system, the auxiliary DC path has to be operated from a high-voltage supply to allow choosing $R_{\mathrm{DC}} > R_{\mathrm{FB}}$ to avoid any noise degradation due to the DSL resistance. Steering the current away from the SDM is a simple and effective solution to improve the SDM's useful dynamic range and its noise performance. However, it does not provide a practical solution since the voltage $V_{\mathrm{DC,HV}}$ has to be constantly adjusted if

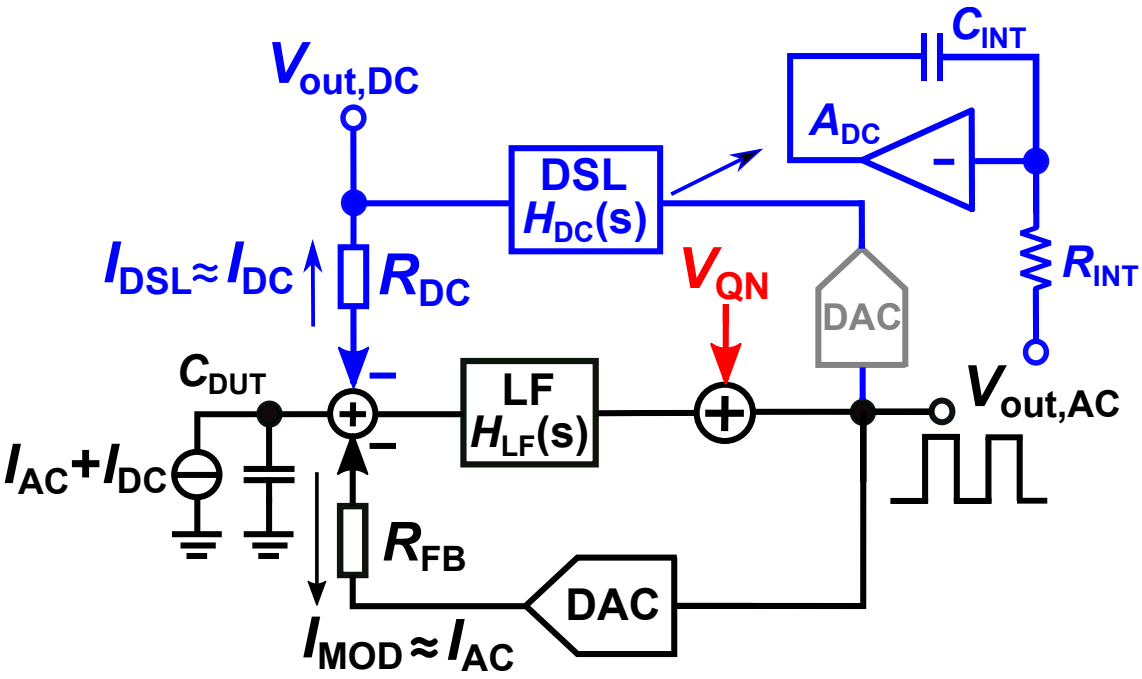

Figure 6.9: Block diagram of a generic C-SDM with the proposed DSL in blue.

the DC operating point of the sensor is constantly changing. For example, the base resistance of an MR sensor, especially a TMR sensor, would change significantly depending on the orientation of the sensor or the earth magnetic field in the lab. As a result, a novel technique to "automatically" steer away the DC current from C-SDMs is adapted in this work.

6.3.2 Embedding a DSL around a C-SDM

A DSL is a feedback loop that automates the process of steering DC currents away from the C-TIAs [63, 64], and more recently, in R-TIAs [62]. It simply comprises of an active integrator with large DC gain in the feedback loop, to process the DC currents, and very low gain at the signal bandwidth, allowing the signal to be processed by the TIA. Here, we propose using DSLs inside a C-SDM to improve the SDM's dynamic range for AC signals. Fig. 6.9 shows the block diagram of the proposed C-SDM incorporating a DSL. In the proposed scheme, the output bitstream of the modulator is (optionally) converted to the analog domain via a DAC and then low pass filtered using an active integrator with a DC gain of A_{DC} and a corner frequency of $\omega_{\mathrm{c}} = 1/\left(R_{\mathrm{int}} \cdot C_{\mathrm{int}}\right)$, where R_{int} and C_{int} are the integration resistance and capacitance, respectively. The DAC is only needed for SDMs with embedded multi-bit quantizers and can be left out for modulators with single-bit quantizers. Afterwards, the output voltage of the DSL $V_{\mathrm{out,DC}}$ together with the DC resistor R_{DC} either sources or sinks the input DC current while, ideally, allowing only the AC current to flow in the modulator.

6.3.3 Modified STF and NTF

While the input stage of a C-SDM is identical to that of a C-TIA, stabilizing the DSL around the C-SDM is significantly simpler. This is because in the C-TIA case, the DSL has to contain a zero in addition to the low-frequency pole defining the cut-off frequency to ensure sufficient phase margin due to the pole at DC owing to the integrator in the signal path that is part of the DSL [63]. In contrast, in the proposed scheme, the DSL is connected to the overall modulator output. Consequently, the signal transfer function (STF) of the modulator, without the DSL, displays a low-pass behavior with a cut-off frequency that is chosen according to the highest signal frequency component. This in return relaxes the stability requirements of the DSL when connected to the modulator since the pole of the feedback integrator is the only low-frequency stability-relevant pole inside the DSL. In the proposed architecture, however, it is important to evaluate the DSL's effect on the overall SDM performance. This is of particular importance since both loops, the SDM and the DSL loops, are nested in this structure. To assess the performance of the system, the modified STF and NTF are evaluated for this structure. First, the modulator's NTF is examined, which is given by:

$$\mathrm{NTF} = \frac{V_{\mathrm{out,AC}}}{V_{\mathrm{QN}}} = \frac{1}{1 + \dfrac{H_{\mathrm{LF}}(\mathrm{s})}{R_{\mathrm{FB}}} + \dfrac{H_{\mathrm{LF}}(\mathrm{s}) \cdot H_{\mathrm{DC}}(\mathrm{s})}{R_{\mathrm{DC}}}}. \tag{6.6}$$

For sufficiently large ω, the NTF can be approximated as follows:

$$\mathrm{NTF}|_{\omega \gg \omega_{\mathrm{c}}} \approx \frac{R_{\mathrm{FB}}}{H_{\mathrm{LF}}(\mathrm{s})}. \tag{6.7}$$

One can conclude from eq. (6.7) that the DSL does not interfere with the modulator's NTF which can be set independently by the modulator's loop filter. On the other hand, the STF can be written as:

$$\mathrm{STF} = \frac{V_{\mathrm{out,AC}}}{I_{\mathrm{AC}} + I_{\mathrm{DC}}} = \frac{H_{\mathrm{LF}}(\mathrm{s})}{1 + \dfrac{H_{\mathrm{LF}}(\mathrm{s})}{R_{\mathrm{FB}}} + \dfrac{H_{\mathrm{LF}}(\mathrm{s}) \cdot H_{\mathrm{DC}}(\mathrm{s})}{R_{\mathrm{DC}}}}. \tag{6.8}$$

For a finite DC gain A_{DC} in the DSL, $H_{\mathrm{DC}}(\mathrm{s})$ can be expressed as:

$$H_{\mathrm{DC}}(\mathrm{s}) = \frac{A_{\mathrm{DC}}}{1 + \mathrm{s} \cdot \dfrac{A_{\mathrm{DC}}}{\omega_{\mathrm{c}}}}. \tag{6.9}$$

Eq. (6.8) can be approximated for very low frequencies ($\omega \ll \omega_{\mathrm{c}}$) and within the signal band of the SDM according to:

$$\mathrm{STF_{DC}}|_{\omega \ll \omega_{\mathrm{c}}} \approx \frac{R_{\mathrm{DC}} \cdot R_{\mathrm{FB}}}{R_{\mathrm{DC}} + A_{\mathrm{DC}} \cdot R_{\mathrm{FB}}} \approx \frac{R_{\mathrm{DC}}}{A_{\mathrm{DC}}} \approx 0, \tag{6.10a}$$

$$\mathrm{STF_{AC}}|_{\omega \gg \omega_{\mathrm{c}}} \approx R_{\mathrm{FB}}. \tag{6.10b}$$

Similarly, by setting ω_c to a sufficiently small value and for sufficiently small frequencies ω, the output voltage of the DSL $V_{out,DC}$ can be written as:

$$V_{out,DC}|_{\omega \ll \omega_c} = I_{DC} \cdot \frac{R_{DC}}{1 + \frac{R_{DC}}{R_{FB} \cdot A(s)}} \approx I_{DC} \cdot R_{DC}, \tag{6.11}$$

where R_{DC} and R_{AC} are shown in Fig. 6.9. That is, by designing the gain of the amplifier inside the DSL large enough, the DSL processes the entire input DC current. This, in turn, renders the two feedback loops mostly independent, the DSL processing only DC (and very low-frequency components), the SDM feedback loop processing all AC signals outside the bandwidth of the DSL. Thus, for frequencies above ω_c, the SDM output $D_{out,AC}$ represents the desired pulse density encoded representation of the AC input signal according to:

$$D_{out,AC}|_{\omega \gg \omega_c} \approx I_{AC} \cdot R_{FB}. \tag{6.12}$$

At much lower frequencies ($\omega \ll \omega_c$), the SDM does not process any signals rendering the modulator as a bandpass filter. The low-pass filter cut-off frequency is set by the inherent AAF property of the CT loop filter. Ignoring the finite DC-gain of the integrator, the 3-dB high pass corner frequency of the bandpass filter ω_{BP} can be evaluated by setting the STF in eq. (6.8) to STF $= R_{FB}/\sqrt{2}$ as follows:

$$\omega_{BP} = (1 + \sqrt{2}) \cdot \omega_p \cdot \frac{R_{FB}}{R_{DC}}. \tag{6.13}$$

Similarly, the corner frequency of the DSL ω_{LP} can be determined by setting $V_{out,DC}$ in eq. (6.11) to $V_{out,DC} = (I_{DC} \cdot R_{DC})/\sqrt{2}$ as follows:

$$\omega_{LP} = (\sqrt{2} - 1) \cdot \omega_p \cdot \frac{R_{FB}}{R_{DC}}. \tag{6.14}$$

Overall, the C-SDM displays a bandpass behavior rejecting DC offsets, while translating the input AC current to an output voltage by a transimpedance of R_{FB} before being digitized by the modulator. On the other hand, the DC currents are processed by the DSL with a transimpedance of R_{DC}. The overall illustration of the C-SDM with the employed DSL is shown in Fig. 6.10.

6.4 A CT C-SDM employing a DC servo loop

The goals of this thesis do not only include the design of high performance frontends for MR sensors as shown in chapter 4, but also area-efficient designs with very good noise performance. Therefore, the design of a C-SDM is discussed in this part of the thesis. The designed modulator is also intended for quantum applications, and hence, the modulator's performance in terms of noise and dynamic range is to be considered thoroughly. The design specifications are set as follows. A worst-case

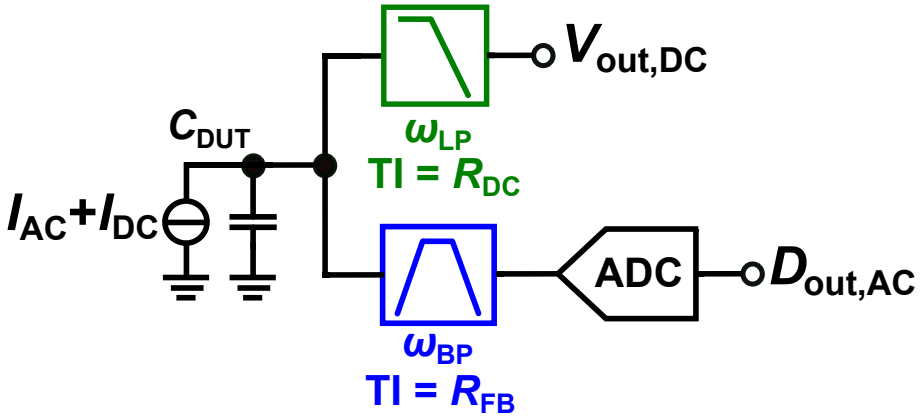

Figure 6.10: Equivalent model of the C-SDM employing a DSL.

Table 6.1: A summary of the design requirements of the C-SDM.

Signal bandwidth	200 kHz
Dynamic range	$\geq$ 70 dB
Signal amplitudes	$\geq$ 100 μA_{pp}
Noise floor	$\leq$ 20 pA/$\sqrt{Hz}$
Input parasitic capacitance	$\leq$ 500 pF
Input DC current	Yes

thermal noise floor of 20 pA/$\sqrt{Hz}$ is required. Although the target noise performance is 2.5x higher compared to our presented MR sensor frontend in chapter 4, it is still competitive to the SoA designs shown in table 4.1. Moreover, the modulator is designed to digitize maximum signal amplitudes in the range of 100 μA_{pp} expected from MR sensors. On the other hand, the readout of the photodiodes for NV-based magnetometers set the bandwidth of the modulator. In many cases, the bandwidth of such readouts are typically around 100 kHz [82, 83]. As a result, a bandwidth of 200 kHz is chosen for the modulator, allowing for higher bandwidth if needed.
The design specifications of the modulator are based on the required noise performance and speed while fitting the dynamic range requirements of the input signal. For example, a C-SDM designed to readout an array of MR sensors would interface a large parasitic capacitance C_P at the input. Moreover, both for a photodiode readout and an MR sensor readout, a DC current would significantly reduce the usable dynamic range of the modulator if no measures are taken. In this work, the modulator is intended to drive large parasitic capacitances of up to 500 pF while being able to handle large undesired DC currents. A summary of the required specifications is shown in Table 6.1.

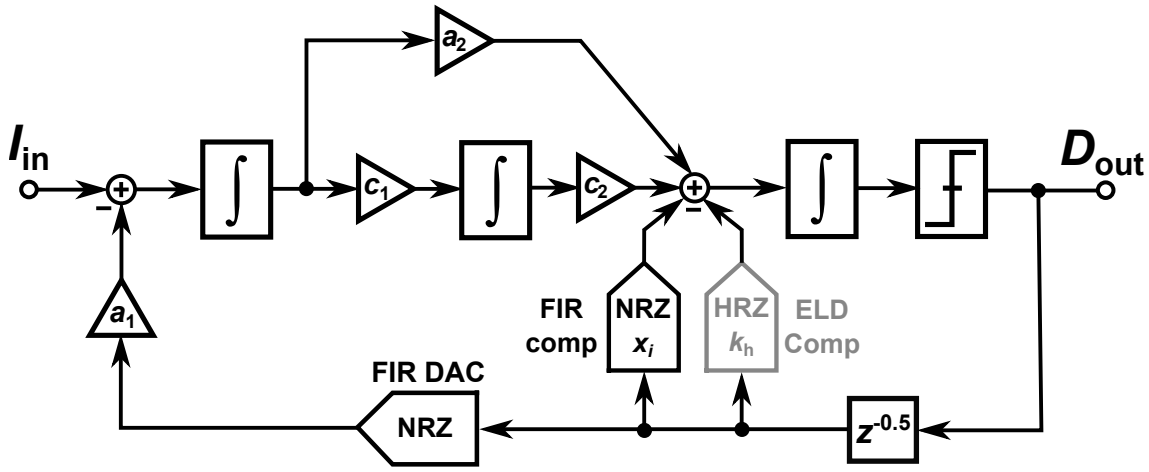

Figure 6.11: Block diagram of a third-order CIFFB C-SDM with FIR feedback.

6.4.1 System-level design of the C-SDM

First, a suitable architecture of the C-SDM is chosen. Multiple architectures are available in the literature such as the cascade of integrators in feedforward (CIFF) structure, cascade of integrators in feedback (CIFB) structure, and the the hybrid cascade of integrators in feedforward and feedback (CIFFB) structure [84]. In this work, a third-order CIFFB structure is chosen for multiple reasons. First, a CIFFB architecture removes the necessity of building a power-hungry adder before the quantizer similar to CIFB architectures. Secondly, it only features two DACs in the loop filter compared to three DACs in the CIFB topologies. The innermost DAC of the CIFFB structure is important for the operation of the SDM and is also reused for the ELD compensation of the structure. A block diagram of the C-SDM with a CIFFB loop filter is shown in Fig. 6.11. In order to increase the linearity of the frontend, a single-bit quantizer and DAC are implemented in the SDM. This comes with the expense of a lower clock jitter robustness due the single-bit DAC. To mitigate this problem, a finite-impulse-response (FIR) DAC is adopted in this work similar to [85], cf. Fig. 6.11. For R-DACs, however, a large number of taps would directly lead to an increase in the tap resistance which in turn increases the DAC's parasitic capacitance and area. In this work, a 4-tap FIR DAC is sufficient for good jitter robustness without significant increase in the chip area. Since the FIR DAC changes the modulator's NTF due to the low-pass filtering property of the FIR DAC, a compensation FIR DAC is added at the input of the last integrator. The coefficients of the compensation FIR DAC x_i are chosen to restore the modulator's NTF. A schematic of an N-tap FIR DAC is shown in Fig. 6.12 and embedded in the C-SDM shown in Fig. 6.11. The FIR and compensation FIR DACs has the

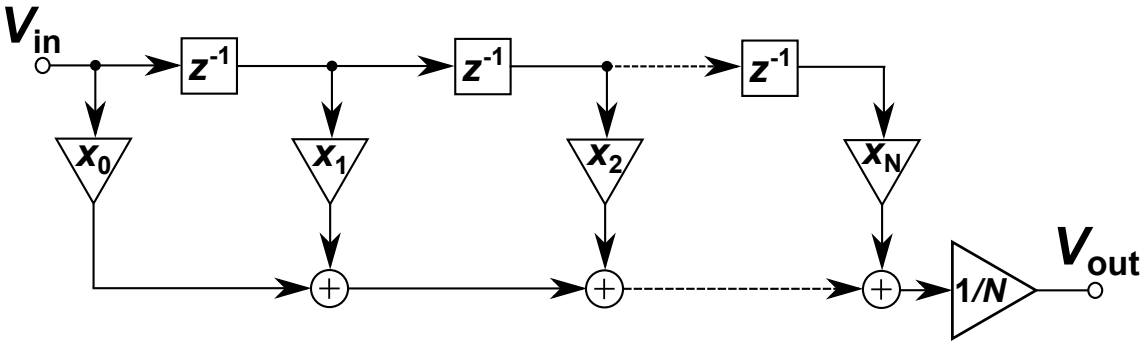

Figure 6.12: Block diagram of an N-tap FIR DAC.

following transfer functions:

$$\mathrm{FIR}[z] = \frac{1}{4}\left(1 + z^{-1} + z^{-2} + z^{-3} + z^{-4}\right), \tag{6.15a}$$

$$\mathrm{FIR_c}[z] = x_0 + x_1 z^{-1} + x_2 z^{-2} + x_3 z^{-3}. \tag{6.15b}$$

6.4.2 Modulator's coefficient scaling

In order to derive proper coefficients for the CT C-SDM, two popular approaches can be applied. First, the CT coefficients can be directly extracted and the modulator's stability can be simulated using the automated design environment available on *www.sigma-delta.de* [86]. Alternatively, the discrete-time (DT) coefficients can be computed using the Schreier Delta-Sigma toolbox [87]. Afterwards, the CT coefficients can be derived using the impulse-invariant transform (IIT). In this work, the latter method is used to derive the CT coefficients since the FIR DAC is not yet supported on the automated design online tool (until the time of writing this thesis). The IIT of an SDM loop filter with an order less than or equal to three and for non-return-to-zero (NRZ) DACs [88] is shown in table 6.2. The shown transformations are also valid for the proposed CIFFB modulator with FIR feedback since the FIR DAC is composed of multiple NRZ DACs shifted in time. The DT loop-filter (LF) can be written in terms of the discrete-time coefficients $a_{\mathrm{DT},i}$ as follows:

$$\mathrm{LF}|_{\mathrm{DT}} = \frac{a_{\mathrm{DT},3} z^{-1}}{(1 - z^{-1})} + \frac{a_{\mathrm{DT},2} z^{-2}}{(1 - z^{-1})^2} + \frac{a_{\mathrm{DT},1} z^{-3}}{(1 - z^{-1})^3}. \tag{6.16}$$

Before obtaining the CT coefficients of the modulator, a delay of half a sampling period is inserted in the loop to accommodate for the excess loop delay (ELD) in the loop filter. Such delay is usually compensated using a half return-to-zero (HRZ) DAC and has a coefficient of k_{h}, cf. 6.11.
Using the transformations shown in Table 6.2, the CT coefficients setting the NTF

Table 6.2: DT equivalent of CT loop-filters with rectangular feedback DAC pulses.

S-domain	Z-domain
$\frac{1}{s}$	$\frac{\omega_0}{z-1}$, $\omega_0 = \beta - \alpha$
$\frac{1}{s^2}$	$\frac{\omega_1 \cdot z + \omega_0}{(z-1)^2}$, $\omega_0 = \frac{\beta^2 - \alpha^2}{2}$, $\omega_1 = \frac{\beta(2-\beta) - \alpha(2-\alpha)}{2}$
$\frac{1}{s^3}$	$\frac{\omega_2 \cdot z^2 + \omega_1 \cdot z + \omega_0}{(z-1)^3}$, $\omega_0 = \frac{\beta^3 - \alpha^3}{6}$, $\omega_1 = -\frac{\beta^3 - \alpha^3}{3} + \frac{\beta^2 - \alpha^2}{2} + \frac{\beta - \alpha}{2}$
	$\omega_2 = \frac{\beta^3 - \alpha^3}{6} - \frac{\beta^2 - \alpha^2}{2} + \frac{\beta - \alpha}{2}$

$a_{1,2}$, $x_{0,1,2}$ and k_h are derived as follows:

$$\begin{aligned} a_1 &= a_{\mathrm{DT},1}, \quad a_2 = 1 + a_{\mathrm{DT},2}, \\ x_0 &= \frac{1}{96}\left(-7a_{\mathrm{DT},1} - 6a_{\mathrm{DT},1}a_{\mathrm{DT},2} + 192a_{\mathrm{DT},3}\right), \\ x_1 &= \frac{a_{\mathrm{DT},1}}{96}\left(-19 + 54a_{\mathrm{DT},2}\right), \\ x_2 &= \frac{a_{\mathrm{DT},1}}{96}\left(5 + 6a_{\mathrm{DT},2}\right), \\ k_\mathrm{h} &= \frac{1}{2}\left(a_{\mathrm{DT},1} - 2a_{\mathrm{DT},1}a_{\mathrm{DT},2} + 4a_{\mathrm{DT},23}\right). \end{aligned} \tag{6.17}$$

Now, the NTF is synthesized using the Schreier Delta-Sigma toolbox using an adequate out-of-band gain (OBG). For single-bit quantizers, Lee criterion is used indicating that an SDM modulator with a single-bit quantizer is likely to be stable for OBG ≤ 2 [89]. In this work, and frequently in prior art, an OBG $= 1.5$ is used for single-bit quantizers. The synthesized DT NTF for the third order modulator can be written as:

$$\mathrm{NTF}|_{\mathrm{DT}} = \frac{(z-1)^3}{(z-0.67)(z^2 - 1.53z + 0.66)}. \tag{6.18}$$

It is worth mentioning that the coefficients $c_{1,2}$ in Fig. 6.11 are used to scale the output swing of the integrators. After running a single transient simulation of the Simulink model using the coefficients shown in eq. 6.17, dynamic scaling of the integrators is done by adjusting all the coefficients with respect to c_i, cf. Fig. 6.11, while keeping the NTF unaltered. The scaled CT coefficients are summarized in Table 6.3.

Table 6.3: A summary of the CT coefficients used in the C-SDM.

$a_{\mathrm{DT},1}$	$a_{\mathrm{DT},2}$	$a_{\mathrm{DT},3}$	a_1	a_2	c_1	c_2	x_0	x_1	x_2	x_3	k_h
0.8	0.288	0.044	0.07	0.56	0.1	0.62	0.20	0.019	0.016	0.0025	0.17

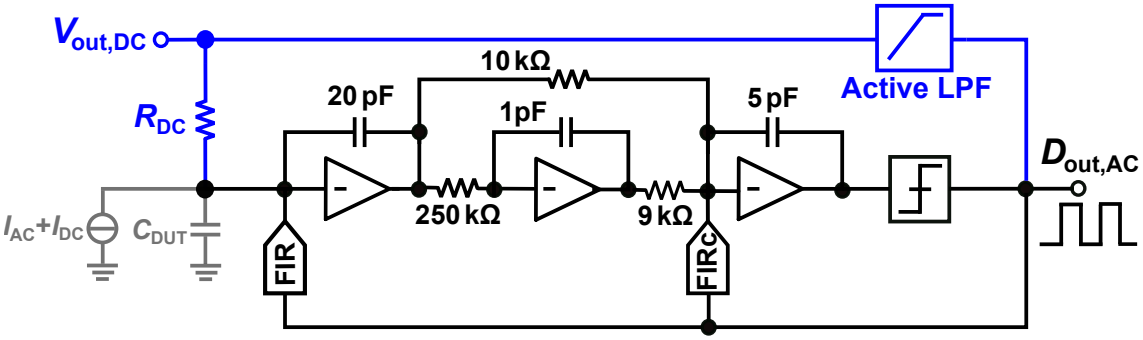

Figure 6.13: Architecture of the on-chip C-SDM and the off-chip DSL (in blue).

Fig. 6.13 shows the architecture of the presented C-SDM with an off-chip DSL (in blue) implementation to verify the usefulness of our proposed design. The off-chip DSL is tested with an output stage with a maximum voltage swing of ±10 V. Here, the higher output voltage enables the use of a larger feedback resistance R_DC to prevent increasing the thermal noise floor ideally defined by the feedback resistance of the SDM. In the presented implementation, we have used a value of $R_\mathrm{DC} = 50\,\mathrm{k\Omega}$, which provides minimum added noise compared to the effective feedback resistance of $R_\mathrm{FB} = R_\mathrm{TAP}/N_\mathrm{TAPS} = 20\,\mathrm{k\Omega}$ of the SDM. The modulator is designed for a signal bandwidth of $\mathrm{BW} = 200\,\mathrm{kHz}$ and a sampling frequency of $f_\mathrm{s} = 36\,\mathrm{MHz}$, corresponding to an oversampling ratio of $\mathrm{OSR} = 90$.

6.4.3 FIR DAC design

To improve the robustness of the modulator against clock jitter several methods have been proposed in the literature including FIR feedback DACs [85] and switched capacitor resistor (SCR) DACs [79]. While the SCR DACs show excellent robustness against clock jitter [90], they degrade the anti-aliasing filtering property of the modulator [91]. This is of particular importance in this design since the modulator is the frontend of the sensor system, and implementing an AAF upfront before the ADC would deteriorate the power efficiency of the system. Therefore, in the presented design, we use a 4-tap FIR feedback DAC to improve jitter immunity. Fig. 6.14a shows a typical implementation of a single FIR tap using a pair of switches and a resistor connected to the first OTA. While a resistive feedback DAC provides an improved noise performance compared to a current-steering DAC [85], it usually exhibits lower speed and higher voltage fluctuations on the supply lines. The origin

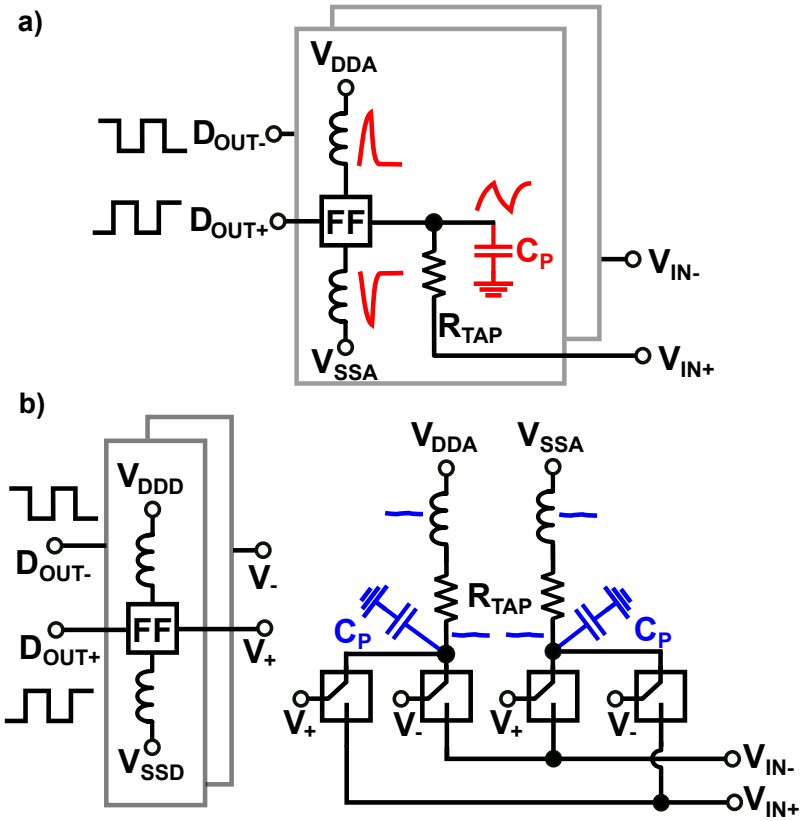

Figure 6.14: a) Conventional FIR tap showing the switching problem at the analog supplies and the finite settling time due to the parasitic capacitance across the tap resistor. b) An FIR tap with highly attenuated switching fluctuations at the supply lines and the parasitic capacitance due to switching the FIR tap resistance at the virtual ground nodes.

of the fluctuations is illustrated in Fig. 6.14a, which shows the effect of toggling of the comparator output on V_{DDA} and V_{SSA}. Moreover, for larger resistors as they are required for low noise operation, the parasitic capacitance C_{P} increases, which degrades the DAC settling time. Ultimately, this lowers the achievable OSR and, thereby, the achievable SNR, and, if uncompensated, in the worst case, can even lead to modulator instability. Moreover, parasitic bond wire inductances exacerbate the fluctuations on the V_{DDA} and V_{SSA} lines [92]. To solve these problems, we adopt the solution proposed in [93] by using a DAC similar to the classic current-steering DAC but replacing the current source by a resistor as shown in Fig. 6.14b. In this case, the parasitic capacitance associated with the resistor C_{P} is always kept at a fixed potential (V_{DDA} or V_{SSA}, respectively) and, therefore, the settling time is significantly reduced. Moreover, the analog supply lines, V_{DDA} and V_{SSA}, respectively, become much quieter since the comparator toggling drives the differential switches of the resistive-steering DAC instead of charging and discharging C_{P}, cf. Fig 6.14b. The simulated virtual ground voltages for both DACs are shown in Fig. 6.15. It is

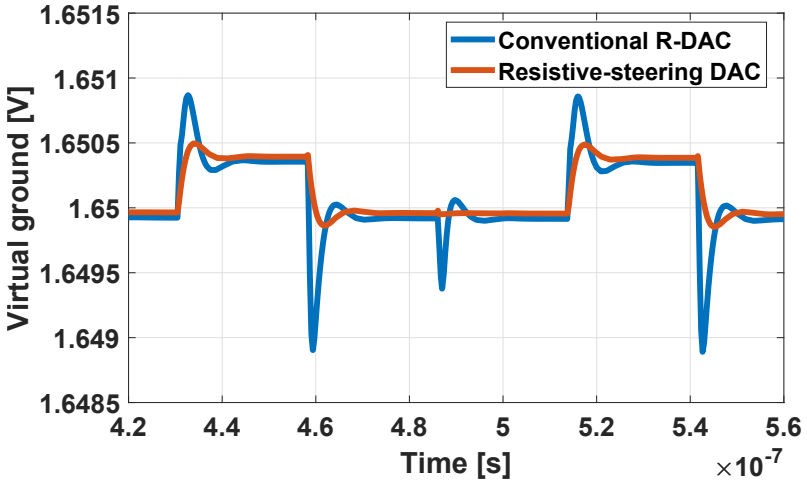

Figure 6.15: Simulated virtual ground node for the typical FIR DAC implementation against the resistive-steering DAC.

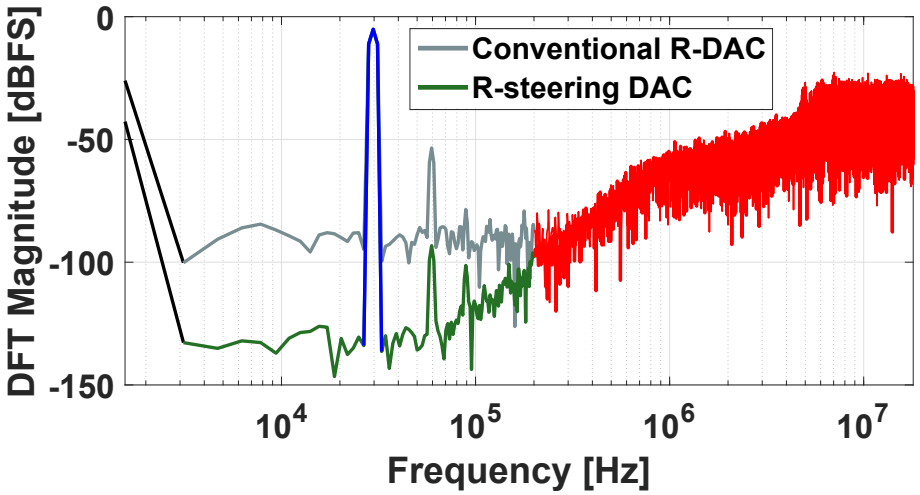

Figure 6.16: Simulated spectra of the C-SDM with the typical FIR and the resistive-steering DACs with 2^8 FFT points.

clear that the virtual ground node experiences less voltage fluctuations with switching the resistor a the virtual ground. This is also reflected on the modulator's SNR and SNDR. Fig. 6.16 shows the different spectra of the two DACs for a sampling frequency of $f_s = 36\,\text{MHz}$. As shown in Fig. 6.16, the simulated noise floor of the SDM with the conventional DAC is much worse compared to switching the DAC at the virtual ground. Moreover, the second-order harmonic is attenuated as shown by this simulation by 40 dB. It is worth mentioning that switching the resistive DAC at the virtual ground has been readdressed and improved by adding a dummy structure as shown in [94, 95], however, in this design, the achieved SNDR with switching the resistive DAC at the virtual ground is enough for our application.

6.4.4 Design of the first integrator

The design of the first integrator has to fulfill multiple criteria. First, the open-loop DC gain of the amplifier has to be chosen large enough to avoid significant quantization noise penalty [96]. Secondly, the UGF of the opamp, or more specifically its g_{m}, has to be chosen large enough to stay within the thermal noise budget of the amplifier relative to the entire SDM. Moreover, the speed of the opamp has to be considered while taking into account the input parasitic capacitance C_{P} as previously shown in eq. (6.5). In this work, a two-stage miller-compensated amplifier design is adopted for sufficiently large DC gain. The transistor-level model of the amplifier embedded in the first integrator is shown in Fig. 6.17 featuring a wide swing telescopic amplifier with a PMOS input stage to lower the flicker noise of the opamp. The output stage of the opamp consumes a significant current of 14 mA to be able to drive the large parasitic capacitances at the SDM's input. To decide on the proper ω_{UGF} of the opamp, system-level simulations are done for an amplifier built with ideal Spectre components. Surprisingly, the minimum ω_{UGF} required to avoid instability in the modulator is only $0.14\,f_{\mathrm{s}}$. This could be due to the very small coefficient in the first integrator $a_1 = 0.07$ relaxing the ω_{UGF} requirements of the embedded opamp. Fig. 6.18 shows the simulated ω_{UGF} of the integrator for different input capacitances. According to this simulation, the ω_{UGF} of the amplifier can preserve the SNR of the modulator as long as $C_{\mathrm{P}} \leq 1.3\,\mathrm{nF}$. This view, however, is optimistic and does not truly reflect the non-ideal DAC transfer characteristic or its finite output impedance. As a result, the effect of the parasitic input capacitance will be revisited in the measurement results section.

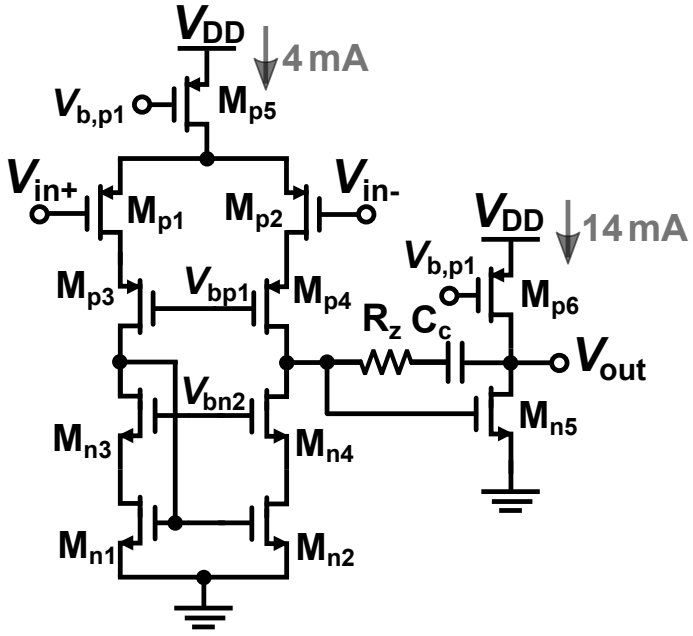

Figure 6.17: The transistor-level model of the first amplifier.

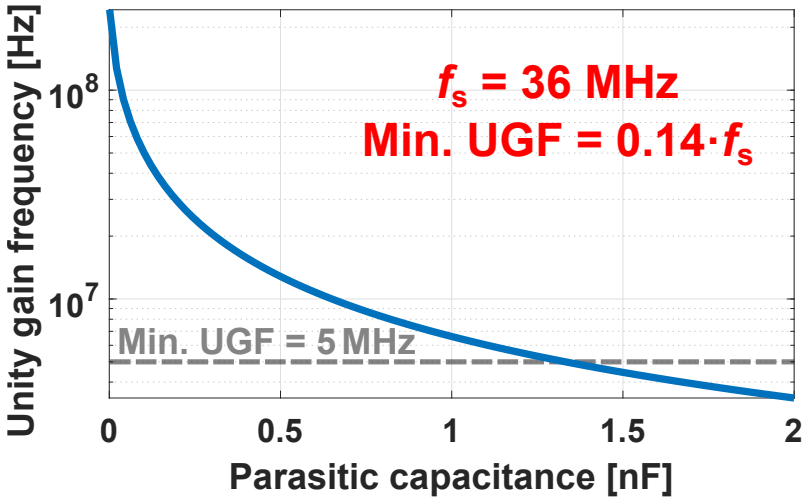

Figure 6.18: Effect of the parasitic input capacitance on the ω_{UGF} of the first integrator. The minimum $\omega_{\mathrm{UGF}} = 5\,\mathrm{MHz}$.

6.4.5 Measurement results

The proposed modulator is manufactured in 180 nm bulk CMOS, and its micrograph is shown in Fig. 6.19. Despite its capability to drive large input capacitances, it only occupies an active area of $0.64\,\mathrm{mm}^2$ and consumes 64 mW from a 3.3 V supply. It is worth mentioning that the first integrator consumes 94% of the total power, i.e. 60 mW, to be able to drive the large input parasitic capacitance C_{P}. This shows that adding insignificant amount of power can convert a TIA into a C-SDM functioning as a TIA followed by an ADC without the additional burden of building a separate ADC to the backend of the sensor chain.
To evaluate the performance of the CT C-SDM, we bonded the chip directly on a test PCB to lower the effect of parasitic capacitances and inductance due to chip carriers. The PCB contains all necessary auxiliary circuits containing LDOs, clock buffers, as well as a microcontroller to setup the capacitive bank of the CT C-SDM. Afterwards, the digital bitstream of the SDM is saved on a computer and the data is analyzed using Matlab.

Performance of the modulator

Fig. 6.20 displays the output spectrum of the modulator for a peak-to-peak input AC current of $I_{\mathrm{AC,MSA}} = 137\,\mu\mathrm{A_{pp}}$ at a frequency of $f_{\mathrm{sig}} = 12\,\mathrm{kHz}$. The measured peak SNR and SNDR are 77 dB and 76.8 dB, respectively. Moreover, the measured SFDR is 81 dB and is limited by the fourth harmonic. In this measurement setup, no additional input capacitance is added. The measured noise floor and integrated noise over the 200 kHz BW are $15\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and $6.9\,\mathrm{nA_{rms}}$, respectively. The measured dynamic range (DR) is 80 dB. Next, we investigated the effect of the input parasitic capacitance C_{P} on the overall modulator's performance. Fig. 6.21a shows

the measured SNR and SNDR for different values of C_P up to 1.5 nF. Surprisingly, the SNR and SNDR are improved by adding parasitic capacitance up to 180 pF before dropping again as expected. By adding $C_P = 180$ pF, the SNR and SNDR are improved by around 5 dB reaching 82.3 dB and 81.6 dB, respectively. The reason behind this improvement in the SNR and SNDR with additional C_P can be explained as follows. The digital supply lines V_{DDD} and V_{SSD} supplying the flip flops of the FIR DAC, cf. 6.14b, also used as the supply lines for the chip pads and their internal circuits such as the digital buffers for the clock regeneration as well as a digital buffer for the output of the SDM. These buffers consume a relatively large amount of power, and consequently, disturb the power lines, and eventually, disturb the FIR performance. Adding additional C_P at the input effectively filtering such disturbances in the output of the FIR DAC. The improved performance lead to an increase in the DR by 5 dB reaching 85 dB with $C_P = 180$ pF. Similarly, the input-referred noise floor of the C-SDM improved from 15 pA/$\sqrt{\text{Hz}}$ to 8.1 pA/$\sqrt{\text{Hz}}$.
Next, the modulator's capability to reject strong interfering signal was evaluated. This was done by measuring the AAF property of the modulator under the influence of out-of-band signals between $f_s = 36$ MHz and $f_s + f_{BW} = 36.2$ MHz. The AAF rejection for the aforementioned input frequency band is shown in Fig. 6.21b. The measured AAF rejection is almost constant with minimal fluctuations between −63.1 dB and −63.6 dB. It is worth mentioning that the AAF rejection property of the modulator is independent of the input parasitic capacitance C_P and the DSL.

Performance of the modulator with the DSL

Next, we have compared the dynamic range with and without the DSL to demonstrate that the DSL has no effect on the modulator's noise performance and MSA. These measurements are conducted by connecting an off-chip DSL connected to an $R_{DC} = 50\,\text{k}\Omega$. The active LPF the DSL, cf. Fig. 6.13, is implemented using

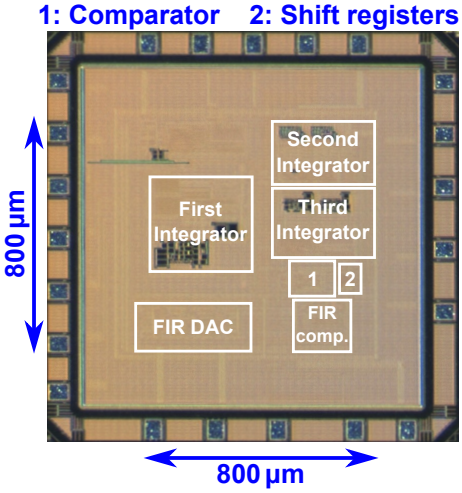

Figure 6.19: Annotated chip micrograph.

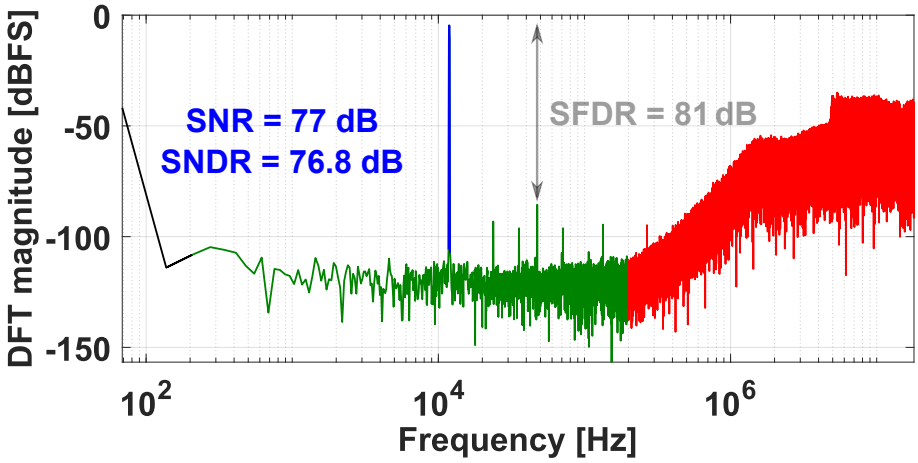

Figure 6.20: Measured output spectrum of the SDM with 2^{19} FFT points for an input signal of $I_{\mathrm{AC,MSA}} = 137\,\mu\mathrm{A_{pp}}$ at $f_{\mathrm{sig}} = 12\,\mathrm{kHz}$.

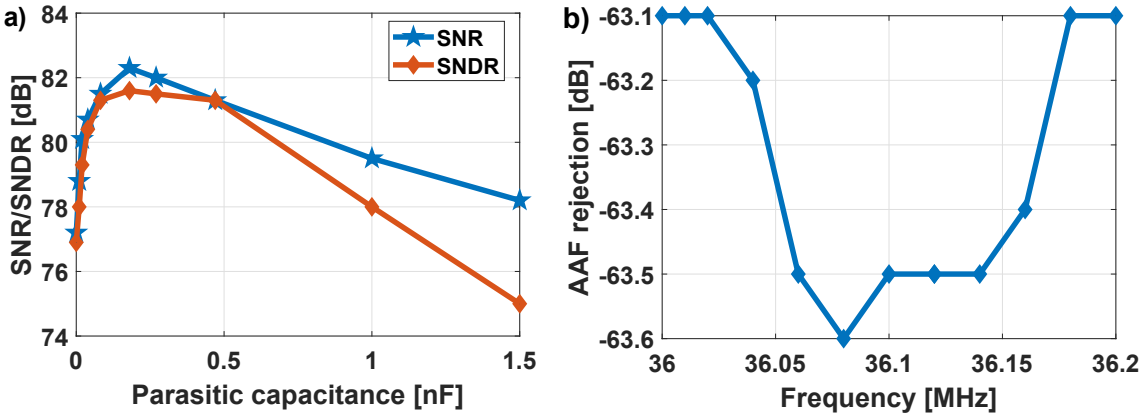

Figure 6.21: Measured SNR and SNDR of the SDM with different values of C_{P}.

the SR560 from Standford Research Systems (SRS) which is a bench-top voltage preamplifier [97]. The low-pass corner frequency of the SR560 can be adjusted to frequencies as low as 0.1 Hz to shift the low-pass corner frequency of the DSL as low as desired. Fig. 6.22 shows the dynamic range plots for the SDM without DSL and without offset and in the presence of a 50 µA offset as well as the DR plot for the SDM including the DSL and in the presence of the 50 µA offset. The signal frequency for all DR plots was $f_{\mathrm{sig}} = 12\,\mathrm{kHz}$. The dynamic range plots with and without the DSL are virtually identical, confirming the negligible effect of the DSL on the modulator's noise and stability performance. Moreover, Fig. 6.22 clearly demonstrates the reduced dynamic range of the SDM without DSL, which is restored to the original value by introducing the proposed DSL. For the utilized DC current of $I_{\mathrm{DC}} = 50\,\mu\mathrm{A}$, the DSL provides an improvement in the dynamic range of 13 dB. Naturally, the improvement in the DR depends on several factors, namely, the DC gain of the integrator, its corner frequency and the ratio $R_{\mathrm{DC}}/R_{\mathrm{FB}}$, cf. sub-

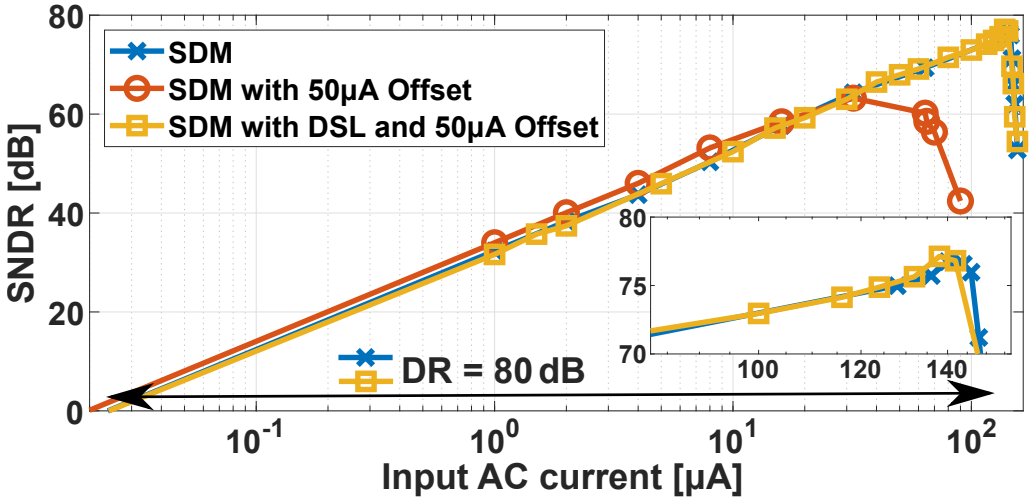

Figure 6.22: DR plots of the SDM without DSL, with an input offset of 50 µA and with the same offset but with DSL connected to the modulator.

section. 6.3.3. Finally, the stability of the DSL is tested by applying a large DC step of 100 µA on top of a small AC signal (4 μA_{pp}) to the input of the modulator and measuring the output voltage of the DSL, $V_{out,DC}$. The results of this test are shown for three different values of the BW of the DSL in Fig. 6.23. In all three cases, the DSL output shows a benign settling behavior without any overshoots.

6.5 Benchmarking and conclusions

6.5.1 Comparison against state-of-the-art

Table 6.4 compares this work to the state-of-the-art designs employing a current-mode SDM as a frontend for current-based sensors. It is worth mentioning that the different input dynamic range requirements of our design compared to the design by Amayreh [66] and Rajabzadeh [65] make it harder to draw a fair comparison between the three designs. The table is meant to show the different CT C-SDMs available for different sensor applications. However, we want to point out the clear advantages and novelties in our design. First, our design incorporate an FIR DAC that ensures suitable jitter immunity as well as decent AAF property for out-of-band signals. In the design by Amayreh, a current-division-based DAC with a NRZ pulse shape is incorporated. Their design achieved an excellent AAF rejection while showing inferior jitter robustness. On the other hand, an SCR feedback employed in the design by Rajabzadeh showed excellent jitter robustness at an expense of insufficient AAF due to the large peak currents associated by the SCR feedback [98]. One important novelty of our design is embedding a DSL in a C-SDM. A DSL can increase the useful DR of the C-SDM modulator with little overhead. Moreover, a DSL can be simply embedded in any C-SDM irrespective of the modulator order,

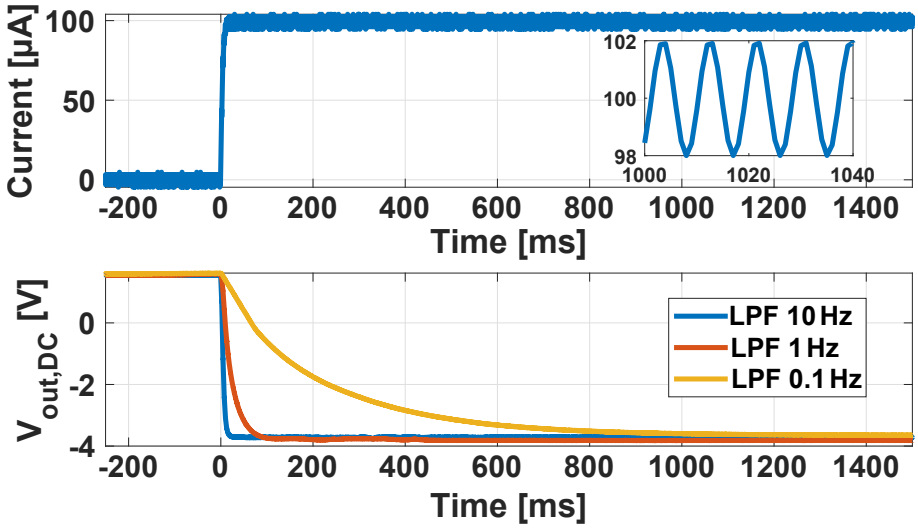

Figure 6.23: Output step response of the DSL (bottom) when the an input step DC current of 100 µA is applied on top of an input AC current of 4 μA_{pp} (top).

architecture or the feedback type. Regarding the modulator's performance, our design features the highest SNR/SNDR and DR reported between the three designs. Although our reported noise floor is the worst among the three designs, it can be improved by using larger R_{FB}. Finally, our design consumes the largest power, however, it can handle very large input capacitances C_P up to 1 nF at the input of the C-SDM.

6.5.2 Conclusions

In this chapter, the design of a C-SDM as a frontend for MR sensors as well as life science applications was compared to classic frontend current readout topologies such as C-TIAs and R-TIAs. A major bottleneck for a C-SDM employed as a sensor frontend is the reduction of the useful dynamic range of the modulator due to the large DC offsets expected from current-mode sensors. While R-TIAs and C-TIAs can employ smaller transimpedances to accommodate such offsets, they suffer from higher noise floors. Alternatively, a DSL can be built around the TIA to steer away the DC current from the frontend TIA. In C-SDMs, the DC offsets do not only lead to an increased thermal noise floor similar to R- and C-TIAs, but also higher quantization noise limiting their applicability as a high performing frontend. As a result, in this work, we propose adding a DSL around the entire modulator, similar to R- and C-TIAs, to get rid of the undesired offsets. Although the SDM has two nested loops, namely the SDM feedback loop and the DSL, they do not interfere with each other due to their different frequency response.
To verify the usefulness of the DSL embedded in a C-SDM, we designed and implemented a C-SDM in 180 nm bulk CMOS with an off-chip DSL as a proof of concept. The C-SDM consumes 64 mW from a 3.3 V supply where 60 mW are consumed by

Table 6.4: Comparison against the state-of-the-art.

	Amayreh TBCAS'19 [66]	Rajabzadeh ESSCIRC'19 [65]	**This work ISCAS'22** [8]
Feedback DAC	NRZ	SCR	**FIR**
Technology [nm]	350	180	**180**
Supply voltage [V]	±1.5	3	**3.3**
Power [mW]	6.73	2	**64**
Area [mm^2]	0.63	0.024	**0.64**
Bandwidth [kHz]	10	100	**200**
OSR	80	100	**90**
Peak SNR [dB]	68	–	**77/82.3$^{\alpha}$**
Peak SNDR [dB]	60	66/72	**76.8/81.6$^{\alpha}$**
Dynamic range [dB]	–	69/74	**80/85$^{\alpha}$**
ENOB [bits]	9.7	10.7/11.7	**12.5/13.3$^{\alpha}$**
Noise floor [$pA/\sqrt{Hz}$]	$2 \cdot 10^{-3}$	0.498	**15/8.1$^{\alpha}$**
AAF at $f_s + f_{BW}$ [dB]	-96	–	**-63.1**
Separate AC and DC	No	No	**Yes$^{\beta}$**
Input cap. (C_P) [pF]	2	–	**1000**
Max. input current [µA]	±0.288	±9.1	**±68.5**

$^{\alpha}$with $C_P = 180\,pF$. $^{\beta}$The DSL is implemented off-chip.

the first integrator to drive large parasitic capacitances up to 1 nF. Moreover, we have switched the resistive DAC at the virtual ground [93] to improve the speed performance compared to a conventional resistive DAC while maintaining a lower noise floor compared to a current-steering DAC. This is particularly important for low-noise C-SDMs where large a feedback impedance, with a large parasitic capacitance, is needed. The resistive steering DAC combines the high speed of a current steering DAC with the low noise of a resistive DAC. The modulator has a signal bandwidth of 200 kHz and can digitize signals up to 137 μA_{pp} with a peak SNR and SNDR of 85 dB and 81.6 dB, respectively. With a large dynamic range of 85 dB, low input-referred noise floor of 8.1 $pA/\sqrt{Hz}$, the ability to drive large capacitance as well as possibility of adding a DSL around the modulator, the proposed design is ideally suited for MR sensor arrays as well as many upcoming quantum sensing applications such as NV center based magnetometers.

7 Conclusion and outlook

In this chapter, we will summarize and discuss the key results of this thesis followed by an outlook including ideas to improve the results of this work.

7.1 Results and discussion

The main aim of this thesis was to design ultra-low-noise frontends for MR sensors. Our approach to find a close-to-optimum design was to investigate two complementary design approaches. The first design variant was based on a voltage-mode readout with a low-noise current bias for the MR sensors. By contrast, the second design variant utilized a CT C-SDM to directly interface an MR sensor. Both design variants were optimized for ultra-low-noise performances.

7.1.1 A voltage-mode readout frontend for MR sensors

First generation of voltage-mode readout chips

In chapters 3 and 4, we discussed the first design variant which is based on a current bias for the sensor, and a voltage readout scheme for the MR signal using an FDDA. This design was optimized in terms of linearity, low offset and noise by the following measurs:

- Good linearity is ensured by choosing a current bias for the MR sensor over a voltage bias followed by a TIA [2].
- A low offset is achieved by incorporating an 11-bit DAC to calibrate any offset between the MR sensor and the reference resistor.
- Having identified the sensor bias current source the bottleneck for achieving low noise, we biased the current source using a very large $g_\mathrm{m}/I_\mathrm{ds}$, resulting in a relatively large $V_\mathrm{ds,sat} = 600\,\mathrm{mV}$ for low thermal noise floor. Moreover, the dimensions of the current source transistors were chosen relatively large to lower the flicker noise yielding in an aspect ratio for each unit element of $850\,\mathrm{nm}/80\,\mu\mathrm{m}$.

The first generation of chips was manufactured in 180 nm SOI technology and consumes 10.4 mW. Despite of the good noise performance of the chip of $9.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a flicker noise corner frequency of $f_\mathrm{fl} = 7\,\mathrm{kHz}$, the following drawbacks were observed:

- The DAC's large $V_{\mathrm{ds,sat}}$ limits the voltage swing around the MR sensor.
- The chip's footprint of $4.7\,\mathrm{mm}^2$ is relatively large, increasing the total cost of the MR sensor system especially for arrays of MR sensors, owing to the unavoidable large DAC unit element size for lower 1/f-noise.

Next, a novel solution was adapted in the second generation of chips to reduce its noise contribution as well as the chip area.

Second generation of voltage-mode readout chips

The second generation of voltage-mode chips included a novel ultra-low-noise current bias scheme that achieves a state-of-the-art noise floor of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for a bias current up to 1 mA. This is achieved by embedding the current bias in a TIA-based loop, offering a large suppression of the current bias noise by the loop gain $g_{\mathrm{m}} \cdot R_{\mathrm{FB}}$ while simultaneously relaxing the noise requirements of the TIA compared to the designs in [36, 43]. Moreover, the DAC's unit element aspect ratio has been decreased from $W/L = 850\,\mathrm{nm}/80\,\mu\mathrm{m}$ in the first generation of chips to only $W/L = 1\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ in the second generation of chips which translates to an area reduction of 68x for the DAC's unit element and thereby also the overall DAC. Moreover, the large $V_{\mathrm{ds,sat}} = 600\,\mathrm{mV}$ could be reduced to only $V_{\mathrm{ds,sat}} = 150\,\mathrm{mV}$. To further improve the low-frequency noise performance, chopping was added to the FDDA to shift its 1/f-corner frequency from 10 kHz to 400 Hz.
The chip has been manufactured in 180 nm SOI technology and consumes 38 mW from 1.8 V, 3.6 V and 6.8 V supplies. Overall the second generation of chips advances the state-of-the-art (SoA) designs incorporating a current bias for MR sensors in the following aspects:

- Lowest current bias noise reported of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for a bias current of 1 mA which is 5x lower compared to SoA designs.
- Lowest voltage noise reported for MR sensors of $8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ thanks to the ultra-low-noise current bias and the voltage readout. The measured noise floor of the second generation of chips is 2x lower compared to the previous SoA.

The low-noise sensor bias and readout electronics together with the chip's capability to compensate for large offsets and the gain programmability of the frontend allows interfacing the chip with TMR sensors with large base resistance spread. In this work, we demonstrated a magnetic noise floor of $120\,\mathrm{pT}/\sqrt{\mathrm{Hz}}$.
Although the second generation of chips show exceptional noise performance, a few tradeoffs could be observed. First, the power consumption due to the low-noise current bias was higher compared to the voltage amplifier chain. Secondly, the chips had to be operated with three different supply voltages which can be restrictive for the practicality of the MR sensor system since three different stable voltage supplies have to be generated on the PCB level. As a result, a different readout strategy based on a C-SDM was also investigated and compared to the voltage-mode readout chips.

7.1.2 A CT C-SDM for MR sensors

The second design architecture we discussed in this thesis is an MR sensor frontend using a CT C-SDM. Owing to the single-ended nature of most current-mode circuits, including R-, C-TIAs and C-SDMs, we started the design process by analyzing the noise performance of TIAs as well as introducing a design guideline for low-noise TIAs in chapter 5. Here, we were able to draw he following conclusions:

- Since the 1/f-noise performance is bias-dependent, the design strategy for the embedded amplifier of low-noise TIAs depends primarily on the frequency of operation. For low-frequency TIAs, sizing the differential input pair in weak or the onset of moderate inversion and low bias current could improve the low-frequency noise performance. On the other hand, high-frequency TIAs benefit from a large bias current and strong inversion mode of operation for the differential pairs.

- Especially for TIAs with large transimpedance values, the noise of the amplifier's tail current source becomes important since it is not canceled by the differential operation due to the asymmetrical load of a single-ended TIA.

Using our detailed analytical model of the noise of TIAs, we could accurately replicate the noise performance of TIAs using transistor-level simulations. This allowed us to create a noise-aware analytical design framework of TIAs that greatly speeds up the design process.
Based on our noise analysis, we were able to design a CT C-SDM in 180 nm CMOS simultaneously proving the current to voltage conversion and the digitization of the input current, cf. chapter 6. Operating from a single 3.3 V supply and consuming total power of 64 mW, the CT C-SDM achieved a peak SNR and SNDR of 82.3 dB and 81.6 dB, respectively, and a dynamic range of DR = 85 dB over a bandwidth of BW = 200 kHz. With a transimpedance of 20 kΩ and a maximum MSA of 137 μA_{pp}, a current noise floor of 8.1 $pA/\sqrt{Hz}$ was achieved. Additionally, our design features the following architectural novelty compared to SoA C-SDMs:

- A DSL is embedded around the entire modulator to improve the useful dynamic range of the modulator in the presence of large DC currents by steering away the DC current away from the C-SDM.

While the functionality of the DSL was demonstrated by an off-chip implementation of an active LPF, integrating the DSL on-chip would not consume much power or area, since the noise of the amplifier is shaped by the LPF with its very-low cut-off frequency.

7.1.3 Important design findings

In this thesis, two design variants for the readout of MR sensors have been developed, namely a voltage-mode readout and a CT C-SDM. While the first design

variant focuses on high performance in terms of linearity and noise, the C-SDM can be more compact and simpler to realize due to the absence of a current bias and its associated bias noise. Another important factor to consider is the parasitic input capacitance C_{P}. In the voltage-mode readout chips, C_{P} has little influence on the frontend's performance. On the other hand, C_{P} reduces the effective ω_{UGF} of CT C-SDMs, and hence, increases the power consumption of the first integrator.
This being said, both design variants have their own merits; the voltage-mode readout offers the highest linearity and lowest noise, while the CT C-SDM with the DSL serves as a TIA, DSL, and an ADC that can be fitted easily in smaller areas. Depending on the C_{P}, the CT C-SDM can be more power efficient compared to the voltage-mode readout.

7.2 Areas for future work

7.2.1 Low-noise current bias for NV-based magnetometers

The low-noise current source shown in chapter 4 is not only suitable for biasing MR sensors, but also for laser diode drivers used in NV-based magnetometers. Most laser diode drivers are implemented similar to the designs shown in [36, 43]. By integrating our novel current bias into laser diode drivers, the noise of the current bias can be rendered negligible while avoiding complex noise reduction techniques such as chopping. Another adjustment that can be integrated in our current bias is to include MOS capacitors instead of metal-insulator-metal (MIM) capacitor for C_{AC}. In this way, the large AC coupling capacitor can have a smaller footprint or, alternatively, a larger capacitor can be added to reduce the influence of the voltage divider caused by C_{AC} and C_{SG}, cf. eq. (4.6).

7.2.2 Extending the C-SDM to a C-ISDM

The CT C-SDM shown in chapter 6 provides a promising starting point for MR sensor readouts, however, the total silicon area directly scale with sensor arrays. A simple solution would be to turn the C-SDM to an incremental current-mode SDM (C-ISDM) allowing multiplexing between uncorrelated channels [99]. While I-SDMs are widely used in sensor readouts, their stability are mostly assessed using linear methods without considering the quantizer non-linearities. To solve this problem, we proposed in [10] an exact mixed-logic dynamical (MLD) system providing an iron-clad prediction of the stability of ISDMs for different loop filters and quantizer resolution. In the future, the designed C-SDM can be adjusted to work in an incremental mode of operation and interfaced with an array of MR sensors. This would allow us to build a compact PoC system for MR sensor systems.

Bibliography

[1] R. Guerrero, M. Pannetier-Lecoeur, C. Fermon, S. Cardoso, R. Ferreira, and P. P. Freitas, "Low frequency noise in arrays of magnetic tunnel junctions connected in series and parallel," *Journal of Applied Physics*, vol. 105, no. 11, p. 113922, 2009. [Online]. Available: https://doi.org/10.1063/1.3139284

[2] D. A. Hall, R. S. Gaster, K. A. A. Makinwa, S. X. Wang, and B. Murmann, "A 256 Pixel Magnetoresistive Biosensor Microarray in 0.18 µm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1290–1301, 2013.

[3] L. Caruso, T. Wunderle, C. M. Lewis, J. Valadeiro, V. Trauchessec, J. Trejo Rosillo, J. P. Amaral, J. Ni, P. Jendritza, C. Fermon, S. Cardoso, P. P. Freitas, P. Fries, and M. Pannetier-Lecoeur, "In Vivo Magnetic Recording of Neuronal Activity," *Neuron*, vol. 95, no. 6, pp. 1283–1291.e4, 2017.

[4] S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. M. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, "Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeBMgOCoFeB pseudo-spin-valves annealed at high temperature," *Applied Physics Letters*, vol. 93, no. 8, pp. 1–4, 2008.

[5] A. Mohamed, M. Schmid, A. Tanwear, H. Heidari, and J. Anders, "A low noise cmos sensor frontend for a tmr-based biosensing platform," in *2020 IEEE SENSORS Conference*, 10 2020, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/9278826

[6] A. Mohamed, H. Heidari, and J. Anders, "A readout circuit for tunnel magnetoresistive sensors employing an ultra-low-noise current source," in *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 331–334.

[7] A. Mohamed, M. Wagner, H. Heidari, and J. Anders, "A frontend for magnetoresistive sensors with a 2.2 pA/$\sqrt{\text{Hz}}$ low-noise current source," *IEEE Solid-State Circuits Letters*, pp. 1–1, 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9701597

[8] A. Mohamed, L. Baumgärtner, J. Zhao, D. Djekic, and J. Anders, "A current-mode $\Sigma\Delta$ modulator with FIR feedback and DC servo loop for an improved dynamic range," *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022.

[9] A. Mohamed, D. Djekic, L. Baumgärtner, and J. Anders, "Noise-aware design methodology of ultra-low-noise transimpedance amplifiers," in *ICECS 2021 - 28th IEEE International Conference on Electronics Circuits and Systems (ICECS)*, 11 2021, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/9665532

[10] A. Mohamed and J. Anders, "Stability Analysis of Incremental ΣΔ Modulators using Mixed-Logic Dynamical Systems and Optimal Control Theory," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[11] S. Tumanski, "Induction coil sensors—a review," *Measurement Science and Technology*, vol. 18, no. 3, pp. R31–R46, jan 2007. [Online]. Available: https://doi.org/10.1088/0957-0233/18/3/r01

[12] E. H. Hall, "On a new action of the magnet on electric currents," *American Journal of Mathematics*, vol. 2, no. 3, pp. 287–292, 1879. [Online]. Available: http://www.jstor.org/stable/2369245

[13] R. C. Jaklevic, J. Lambe, A. H. Silver, and J. E. Mercereau, "Quantum interference effects in josephson tunneling," *Phys. Rev. Lett.*, vol. 12, pp. 159–160, Feb 1964. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.12.159

[14] J. F. Barry, M. J. Turner, J. M. Schloss, D. R. Glenn, Y. Song, M. D. Lukin, H. Park, and R. L. Walsworth, "Optical magnetic detection of single-neuron action potentials using quantum defects in diamond," *Proceedings of the National Academy of Sciences*, vol. 113, no. 49, pp. 14 133–14 138, 2016. [Online]. Available: https://www.pnas.org/content/113/49/14133

[15] M. Pannetier, C. Fermon, G. L. Goff, J. Simola, and E. Kerr, "Femtotesla magnetic field measurement with magnetoresistive sensors," *Science*, vol. 304, no. 5677, pp. 1648–1650, 2004.

[16] I. Campbell and A. Fert, "Chapter 9 transport properties of ferromagnets," ser. Handbook of Ferromagnetic Materials. Elsevier, 1982, vol. 3, pp. 747–804. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1574930405800951

[17] L. Caruso, T. Wunderle, C. M. Lewis, J. Valadeiro, V. Trauchessec, J. Trejo Rosillo, J. P. Amaral, J. Ni, P. Jendritza, C. Fermon, S. Cardoso, P. P. Freitas, P. Fries, and M. Pannetier-Lecoeur, "In vivo magnetic recording of neuronal activity," *Neuron*, vol. 95, no. 6, pp. 1283–1291.e4, 2017. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0896627317307031

[18] C. Treutler, "Magnetic sensors for automotive applications," *Sensors and Actuators A: Physical*, vol. 91, no. 1, pp. 2–6, 2001, third European Conference on Magnetic Sensors and Actuators. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0924424701006215

[19] J. R. Childress and R. E. Fontana, "Magnetic recording read head sensor technology," *Comptes Rendus Physique*, vol. 6, no. 9, pp. 997–1012, 2005.

[20] H. Schewe and W. Schelter, "Industrial applications of magnetoresistive sensors," *Sensors and Actuators, A: Physical*, vol. 59, no. 1-3, pp. 165–167, 1997.

[21] W. Thomson, "On the Electric Conductivity of Commercial Copper of Various Kinds, Proceedings of the Royal Society of London," vol. 8, pp. 550–555, 2013.

[22] D. A. Thompson, L. T. Romankiw, and A. F. Mayadas, "Thin Film Magnetoresistors in Memory, Storage, and Related Applications," *IEEE Transactions on Magnetics*, vol. 11, no. 4, pp. 1039–1050, 1975.

[23] T. R. Mcguire and R. I. Potter, "Anisotropic Magnetoresistance in Ferromagnetic 3D Alloys," *IEEE Transactions on Magnetics*, vol. 11, no. 4, pp. 1018–1038, 1975.

[24] K. E. Kuijk, W. J. Van Gestel, and F. W. Gorter, "The barber pole, a linear magnetoresistive head," *IEEE Transactions on Magnetics*, vol. 11, no. 5, pp. 1215–1217, 1975.

[25] R. Hunt, "A magnetoresistive readout transducer," *IEEE Transactions on Magnetics*, vol. 7, no. 1, pp. 150–154, 1971.

[26] T. G. S. M. Rijks, S. K. J. Lenczowski, R. Coehoorn, and W. J. M. de Jonge, "In-plane and out-of-plane anisotropic magnetoresistance in $ni_{80}fe_{20}$ thin films," *Phys. Rev. B*, vol. 56, pp. 362–366, Jul 1997. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.56.362

[27] M. N. Baibich, J. M. Broto, A. Fert, F. N. Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant Magnetoresistance of (001)/(001)Cr Magnetic Superlattices," *Phys. Rev. Lett.*, vol. 61, pp. 2472–2475, Nov 1988. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.61.2472

[28] P. Grünberg, R. Schreiber, Y. Pang, M. B. Brodsky, and H. Sowers, "Layered magnetic structures: Evidence for antiferromagnetic coupling of Fe layers across Cr Interlayers," *Phys. Rev. Lett.*, vol. 57, pp. 2442–2445, Nov 1986. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.57.2442

[29] B. Dieny, V. S. Speriosu, S. Metin, S. S. Parkin, B. A. Gurney, P. Baumgart, and D. R. Wilhoit, "Magnetotransport properties of magnetically soft spin-valve

structures (invited)," *Journal of Applied Physics*, vol. 69, no. 8, pp. 4774–4779, 1991.

[30] P. P. Freitas, R. Ferreira, and S. Cardoso, "Spintronic Sensors," *Proceedings of the IEEE*, vol. 104, no. 10, pp. 1894–1918, 2016.

[31] J. G. Simmons, "Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film," *Journal of Applied Physics*, vol. 34, no. 6, pp. 1793–1803, 1963.

[32] J. S. Moodera, L. R. Kinder, T. M. Wong, and R. Meservey, "Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions," *Phys. Rev. Lett.*, vol. 74, pp. 3273–3276, Apr 1995. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.74.3273

[33] D. Wang, C. Nordman, J. M. Daughton, Z. Qian, and J. Fink, "70% TMR at room temperature for SDT sandwich junctions with CoFeB as free and reference layers," *IEEE Transactions on Magnetics*, vol. 40, no. 4 II, pp. 2269–2271, 2004.

[34] P. Freitas, R. Ferreira, S. Cardoso, and F. Cardoso, "Magnetoresistive sensors," *Journal of Physics: Condensed Matter*, vol. 19, no. 16, p. 165221, 2007.

[35] S. Zuo, H. Heidari, D. Farina, and K. Nazarpour, "Miniaturized Magnetic Sensors for Implantable Magnetomyography," *Advanced Materials Technologies*, vol. 5, no. 6, p. 2000185, 2020. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/admt.202000185

[36] X. Zhou, E. Mai, M. Sveiven, C. Pochet, H. Jiang, C. C. Huang, and D. A. Hall, "A 9.7-nTrms, 704-ms Magnetic Biosensor Front-End for Detecting Magneto-Relaxation," *IEEE Journal of Solid-State Circuits*, pp. 1–1, 2021.

[37] J. Ge, X. Wang, M. Drack, O. Volkov, M. Liang, G. S. Cañón Bermúdez, R. Illing, C. Wang, S. Zhou, J. Fassbender, M. Kaltenbrunner, and D. Makarov, "A bimodal soft electronic skin for tactile and touchless interaction in real time," *Nature Communications*, vol. 10, no. 1, pp. 1–10, 2019.

[38] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μ W 60 $nV/\sqrt{\text{Hz}}$ Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, 2011.

[39] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, 2007.

[40] X. Zhou, M. Sveiven, and D. A. Hall, "A CMOS Magnetoresistive Sensor Front-End With Mismatch-Tolerance and Sub-ppm Sensitivity for Magnetic Immunoassays," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1254–1263, 2019.

[41] E. Sackinger and W. Guggenbuhl, "A versatile building block: the cmos differential difference amplifier," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, pp. 287–294, 1987.

[42] B. van den Dool and J. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative roll," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 7, pp. 743–749, 1993.

[43] T. Costa, F. A. Cardoso, J. Germano, P. P. Freitas, and M. S. Piedade, "A Cmos Front-End With Integrated Magnetoresistive Sensors for Biomolecular Recognition Detection Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 5, pp. 988–1000, 2017.

[44] S. Huang, M. Ismail, and S. R. Zarabadi, "A wide range differential difference amplifier: a basic block for analog signal processing in MOS technology," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 5, pp. 289–301, 1993.

[45] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb 1991.

[46] J. Duque-Carrillo, "Continuous-time common-mode feedback networks for fully-differential amplifiers: a comparative study," in *1993 IEEE International Symposium on Circuits and Systems*, 1993, pp. 1267–1270 vol.2.

[47] S. Zuo, H. Heidari, D. Farina, and K. Nazarpour, "Miniaturized Magnetic Sensors for Implantable Magnetomyography," *Advanced Materials Technologies*, vol. 5, no. 6, p. 2000185, 2020. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/admt.202000185

[48] R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[49] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[50] A. Sheikholeslami, "Source degeneration [circuit intuitions]," *IEEE Solid-State Circuits Magazine*, vol. 6, no. 3, pp. 5–6, 2014.

[51] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, 1991.

[52] J. Wu, M.-K. Law, P.-I. Mak, and R. P. Martins, "A 2μW 45-nv/$\sqrt{\text{hz}}$ readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudofeedback dc servo loop," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 4, pp. 351–355, 2016.

[53] *ADA4625, 36 V, 18 MHz, Low Noise, Fast Settling Single Supply, RRO, JFET Op Amp*, Analog Devices.

[54] *LM134/LM234/LM334 3-Terminal Adjustable Current Sources*, Texas Instruments, 5 2013.

[55] P. Novak, C. Li, A. I. Shevchuk, R. Stepanyan, M. Caldwell, S. Hughes, T. G. Smart, J. Gorelik, V. P. Ostanin, M. J. Lab *et al.*, "Nanoscale live-cell imaging using hopping probe ion conductance microscopy," *Nature methods*, vol. 6, no. 4, pp. 279–281, 2009.

[56] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nature methods*, vol. 9, no. 5, p. 487, 2012.

[57] M. Brunet Cabré, D. Djekic, T. Romano, N. Hanna, J. Anders, and K. McKelvey, "Microscale electrochemical cell on a custom CMOS transimpedance amplifier for high temporal resolution single entity electrochemistry," *ChemElectroChem*, 2020.

[58] E. Säckinger, *Broadband circuits for optical fiber communication*. John Wiley & Sons, 2005.

[59] A. Sharif-Bakhtiar, M. G. Lee, and A. C. Carusone, "Low-power cmos receivers for short reach optical communication," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1–8.

[60] S. M. Park and H.-J. Yoo, "1.25-gb/s regulated cascode cmos transimpedance amplifier for gigabit ethernet applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, 2004.

[61] D. Djekic, G. Fantner, K. Lips, M. Ortmanns, and J. Anders, "A 0.1% THD, 1-MΩ to 1-GΩ Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1913–1923, 2018.

[62] D. Djekic, M. Häberle, A. Mohamed, L. Baumgärtner, and J. Anders, "A 440-kOhm to 150-GOhm Tunable Transimpedance Amplifier based on Multi-Element Pseudo-Resistors," in *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 403–406.

[63] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, 2009.

[64] M. Häberle, D. Djekic, G. E. Fantner, K. Lips, M. Ortmanns, and J. Anders, "An Integrator-Differentiator TIA Using a Multi-Element Pseudo-Resistor in its DC Servo Loop for Enhanced Noise Performance," in *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, 2018, pp. 294–297.

[65] M. Rajabzadeh, M. Häberle, A. Jain, and M. Ortmanns, "An Integrated Readout for Current Sensing based on a $\Sigma\Delta$ Modulator with Switched Capacitor Feedback," in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, 2019, pp. 321–324.

[66] M. Amayreh, G. Baaken, J. C. Behrends, and Y. Manoli, "A Fully Integrated Current-Mode Continuous-Time Delta-Sigma Modulator for Biological Nanopore Read Out," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 1, pp. 225–236, 2019.

[67] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, 2009.

[68] E. Guglielmi, F. Toso, F. Zanetto, G. Sciortino, A. Mesri, M. Sampietro, and G. Ferrari, "High-value tunable pseudo-resistors design," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2094–2105, 2020.

[69] M. Rajabzadeh, D. Djekic, M. Haeberle, J. Becker, J. Anders, and M. Ortmanns, "Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT $\Sigma\Delta$ Modulator," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.

[70] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel, and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 994–1001, 2000.

[71] T. Watanabe, "Low-noise operation in buried-channel MOSFET's," *IEEE Electron Device Letters*, vol. 6, no. 7, pp. 317–319, 1985.

[72] T. H. Morshed, D. D. Lu, W. M. Yang, M. V. Dunga, X. Xi, J. He, W. Liu, M. C. Kanyu, X. Jin, J. J. Ou *et al.*, "Bsim4v4.7 mosfet model," *Dept. Elect.*

Eng. Comput. Sci., Univ. California, Berkeley, Berkeley, CA, USA, Tech. Rep, 2011.

[73] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical mos transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog integrated circuits and signal processing*, vol. 8, no. 1, pp. 83–114, 1995.

[74] G. Ferrari, F. Gozzini, and M. Sampietro, "A Current-Sensitive Front-End Amplifier for Nano-Biosensors with a 2MHz BW," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 164–165.

[75] M. I. Ibrahim, C. Foy, D. R. Englund, and R. Han, "High-Scalability CMOS Quantum Magnetometer With Spin-State Excitation and Detection of Diamond Color Centers," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 3, pp. 1001–1014, 2021.

[76] J. L. Webb, J. D. Clement, L. Troise, S. Ahmadi, G. J. Johansen, A. Huck, and U. L. Andersen, "Nanotesla sensitivity magnetic field sensing using a compact diamond nitrogen-vacancy magnetometer," *Applied Physics Letters*, vol. 114, no. 23, p. 231103, 2019. [Online]. Available: https://doi.org/10.1063/1.5095241

[77] D. Djekic, G. Fantner, J. Behrends, K. Lips, M. Ortmanns, and J. Anders, "A transimpedance amplifier using a widely tunable PVT-independent pseudo-resistor for high-performance current sensing applications," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, 2017, pp. 79–82.

[78] M. Rajabzadeh, D. Djekic, M. Haeberle, J. Becker, J. Anders, and M. Ortmanns, "Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT $\Sigma\Delta$ Modulator," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.

[79] M. Rajabzadeh, M. Häberle, A. Jain, and M. Ortmanns, "An integrated Read-out for Current Sensing based on a $\Sigma\Delta$ Modulator with Switched Capacitor Feedback," in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, 2019, pp. 321–324.

[80] M. Amayreh, G. Baaken, J. C. Behrends, and Y. Manoli, "A Fully Integrated Current-Mode Continuous-Time Delta-Sigma Modulator for Biological Nanopore Read Out," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 1, pp. 225–236, 2019.

[81] M. Ortmanns, F. Gerfers, and Y. Manoli, "Influence of finite integrator gain bandwidth on continuous-time sigma delta modulators," in *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03.*, vol. 1, 2003, pp. I–I.

[82] H. A. El-Ella, S. Ahmadi, A. M. Wojciechowski, A. Huck, and U. L. Andersen, "Optimised frequency modulation for continuous-wave optical magnetic resonance sensing using nitrogen-vacancy ensembles," *Optics express*, vol. 25, no. 13, pp. 14 809–14 821, 2017.

[83] J. F. Barry, J. M. Schloss, E. Bauch, M. J. Turner, C. A. Hart, L. M. Pham, and R. L. Walsworth, "Sensitivity optimization for NV-diamond magnetometry," *Rev. Mod. Phys.*, vol. 92, p. 015004, Mar 2020. [Online]. Available: https://link.aps.org/doi/10.1103/RevModPhys.92.015004

[84] R. Schreier, G. C. Temes *et al.*, *Understanding delta-sigma data converters*. IEEE press Piscataway, NJ, 2005, vol. 74.

[85] A. Sukumaran and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, 2014.

[86] T. Brückner, C. Zorn, J. Anders, J. Becker, W. Mathis, and M. Ortmanns, "A GPU-Accelerated web-based synthesis tool for CT Sigma-Delta modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 5, pp. 1429–1441, May 2014.

[87] R. Schreier, "The delta-sigma toolbox for Matlab," 01 2000.

[88] J. Cherry and W. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 376–389, 1999.

[89] K. C. . Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 3, pp. 309–318, March 1990.

[90] M. Ortmanns, F. Gerfers, and Y. Manoli, "A continuous-time /spl sigma//spl delta/ modulator with reduced sensitivity to clock jitter through scr feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 875–884, 2005.

[91] S. Pavan, "Alias Rejection of Continuous-Time $\Delta\Sigma$ Modulators With Switched-Capacitor Feedback DACs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, pp. 233–243, 2011.

[92] B. Razavi, "The Current-Steering DAC [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 10, no. 1, pp. 11–15, 2018.

[93] P. Shettigar and S. Pavan, "Design Techniques for Wideband Single-Bit Continuous-Time $\Delta\Sigma$ Modulators With FIR Feedback DACs," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2865–2879, 2012.

[94] R. Theertham, P. Koottala, S. Billa, and S. Pavan, "Design Techniques for High-Resolution Continuous-Time Delta–Sigma Converters With Low In-Band Noise Spectral Density," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2429–2442, 2020.

[95] A. Baluni and S. Pavan, "Analysis and Design of a 20-MHz Bandwidth Continuous-Time Delta-Sigma Modulator With Time-Interleaved Virtual-Ground-Switched FIR Feedback," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 3, pp. 729–738, 2021.

[96] V. R. Gonzalez-Diaz and F. Pareschi, "A 65nm continuous-time sigma-delta modulator with limited ota dc gain compensation," *IEEE Access*, vol. 8, pp. 36 464–36 475, 2020.

[97] *SR560 - Low-noise voltage preamplifier*, Stanford Research Systems, rev. c.

[98] S. Pavan, "Alias Rejection of Continuous-Time $\Delta\Sigma$ Modulators With Switched-Capacitor Feedback DACs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 2, pp. 233–243, 2011.

[99] J. Markus, J. Silva, and G. Temes, "Theory and applications of incremental $\Delta\Sigma$ converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 4, pp. 678–690, 2004.

List of author publications

Some of the research leading to this thesis have appeared previously in the following publications:

Journal articles

1. **A. Mohamed**, M. Wagner, H. Heidari and J. Anders, "A Frontend for Magnetoresistive Sensors With a 2.2-pA/$\sqrt{\text{Hz}}$ Low-Noise Current Source," in IEEE Solid-State Circuits Letters, vol. 5, pp. 17-20, 2022.

2. M. Elsobky, **A. Mohamed**, T. Deuble, J. Anders and J. N. Burghartz, "A 12-to-15 b, 100-to-25 kS/s Resolution Reconfigurable, Power Scalable Incremental ADC Using Ultrathin Chips," in IEEE Sensors Letters, vol. 5, no. 2, pp. 1-4, Feb. 2021.

Conference proceedings

1. **A. Mohamed**, L. Baumgärtner, J. Zhao, D. Djekic and J. Anders, "A current-mode $\Sigma\Delta$ modulator with FIR feedback and DC servo loop for an improved dynamic range," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), 2022, pp. 1-5.

2. **A. Mohamed**, D. Djekic, L. Baumgärtner and J. Anders, "Noise-aware design methodology of ultra-low-noise transimpedance amplifiers," 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2021, pp. 1-5.

3. **A. Mohamed**, H. Heidari and J. Anders, "A readout circuit for tunnel magnetoresistive sensors employing an ultra-low-noise current source," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), 2021, pp. 331-334.

4. D. Djekic, M. Häberle, **A. Mohamed**, L. Baumgärtner and J. Anders, "A 440-kOhm to 150-GOhm Tunable Transimpedance Amplifier based on Multi-Element Pseudo-Resistors," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), 2021, pp. 403-406.

5. **A. Mohamed**, M. Schmid, A. Tanwear, H. Heidari and J. Anders, "A Low Noise CMOS Sensor Frontend for a TMR-based Biosensing Platform," 2020 IEEE SENSORS, 2020, pp. 1-4.

6. **A. Mohamed** and J. Anders, "Stability Analysis of Incremental ΣΔ Modulators using Mixed-Logic Dynamical Systems and Optimal Control Theory," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5.

7. J. Zhao, **A. Mohamed** and J. Anders, "An Active CMOS NMR Field Probe with Custom Transceiver and ΣΔ Modulator ASICs and an Optical Link," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5.

8. **A. Mohamed**, A. Sakr and J. Anders, "FIR Feedback in Continuous-Time Incremental Sigma-Delta ADCs," 2019 17th IEEE International New Circuits and Systems Conference (NEWCAS), 2019, pp. 1-4.