LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTORS ON ULTRA-THIN SINGLE-CRYSTALLINE SILICON

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In the name of Allah, The most beneficent, The most merciful

Read: In the name of thy Lord Who createth, (1) Createth man from a clot. (2) Read: And thy Lord is the Most Bounteous, (3) Who teacheth by the pen, (4) Teacheth man that which he knew not. (5)

(Al-Quran,96)

Contents

Zusammenfassung

In dieser Arbeit werden die Integration und Optimierung von Lateral Diffundierten Metall-Oxid-Halbleiter (LDMOS)-Transistor-Strukturen auf ultra-dünnen (20 µm) Chipfilm™ Substraten vorgestellt.

Die Eigenschaften dieser extrem flach ausgeführten LDMOS-Transistoren werden mithilfe der Simulationswerkzeuge Atlas und Athena von Silvaco eingestellt, optimiert und im Hinblick auf die Einflüsse von Prozessparameterschwankungen untersucht. Der Herstellungsprozess der Chipfilm™-Substrate beginnt mit einem herkömmlichen Bulk-Silizium-Wafer der an der Oberfläche eine 1-2 µm tiefe p^+-Schicht erhält. Darauf wird eine epitaktischen Schicht gewachsen, mit der die Chipdicke eingestellt wird. Die sich mit der hohen Epitaxietemperatur ergebende Ausdiffusion aus der vergrabenen p^+-Schicht kann die Funktion des LDMOS-Transistors, der in die Epitaxieschicht integriert wird, nachteilig beeinflussen und wird deshalb über den Prozesssimulator Atlas nachgebildet. Die *n*-Wanne und die *n*-Implantation des Driftgebietes werden im Herstellungsprozess kombiniert. Hierfür wird ein einziger Diffusionsschrittt bei 1150 ^{O}C für 900 Minuten eingesetzt. Das thermische Budget ist so gewählt, dass die vertikale Ausdiffusion von Bor aus der vergrabenen p^+-Schicht tolerierbar bleibt. Shallow Trench Isolation (STI) wird verwendet, um gewünschte Dicke des Feldoxids bei einem minimalen thermischen Budget zu erreichen Eine Implantation zur Einstellung der Schwellenspannung wird nur für den NLDMOS ausgeführt. Das 15 nm dicke Gate-Oxid ist kombiniert mit dem Gateoxid der Niederspannungs Transistoren der 0,5-µm-CMOS-Technologie bei IMS CHIPS. Die Materialabscheidungen für Poly-Gate und Spacer , sowie die Drain- und Source-Implantationen werden mit mithilfe von Standard-Prozessschritten durchgeführt. Der Prozessablauf ist ansonsten vollständig kompatibel mit dem der Hochspannungs-LDMOS-Technologie von IMS CHIPS.

Die Optimierung der Bauelementparameter umfasst die Tiefe des Shallow Trench, die Implantationsdosen und die Implantationsenergien. Für eine Durchbruchspannung von 100 V beträgt die optimierte Tiefe des Shallow Trench ca. 300 nm, die Tiefe des *p*-Drift-Diffusionsgebietes ~ 1 µm und die Tiefe des Übergangs von *n*-Wanne auf *p*-Drift-Diffusionsgebiet ~ 5 µm. Aufgrund des relativ tiefen Übergangs der *n*-Drift-Region ist der NLDMOS weniger anfällig für Streuungen der Prozess-Parameter, während der flachere Übergang des *p*-Drift-Diffusionsgebietes den PLDMOS sehr empfindlich auf solche Schwankungen reagieren lässt. Die Simulationsergebnisse zeigen, dass, um eine

Durchbruchspannung von über 100 V zu erhalten, die Tiefe des Shallow Trench für den PLDMOS genau im Bereich von 200 bis 350 nm liegen sollte. Daher ist eine sehr genaue Einstellung der Grabentiefe im Falle der ultra-dünnen PLDMOS erforderlich.

Die Simulationen der elektrischen Eigenschaften sowohl für die NLDMOS und die PLDMOS sind mit den folgenden Einstellungen durchgeführt worden: Kanallänge = 10 µm; Länge der Gate-Feldplatte = 10 µm; Länge des Driftgebietes = 20 µm; Implantationsdosis für *n*-Wanne und Driftgebiet = $4 \cdot 10^{12}$ cm^{-2}; Implantationsdosis des *p*-Driftgebiets-Implantatdose = $6 \cdot 10^{12}$ cm^{-2}; Substratkonzentration = $1 \cdot 10^{15}$ cm^{-3}. Die Simulationsergebnisse ergeben eine Schwellenspannung von 0,6 V für den NLDMOS und 1,2 V für den PLDMOS. Der maximale Drainstrom des NLDMOS beträgt 180 µA/µm während dieser sich im Falle des PLDMOS auf 30 µA/µm beläuft.

Das Maskenlayout wird mit dem Entwurfswerkzeug COMPASS generiert. Vor der eigentlichen Integration der LDMOS werden Chipfilm™ Wafer gefertigt, auf denen die endgültige Chipdicke frühzeitig durch die Lage der vergrabenen Hohlräume vorgegeben ist. Zum Vergleich werden die verschiedenen Test-Baulemente sowohl auf Chipfilm™- als auch auf Bulk-Wafern hergestellt.

Die Eingangs- und Ausgangskennlinien der NLDMOS und PLDMOS werden mithilfe von Messungen auf dem ungesägten Wafer bestimmt Die Kanalbreiten von NLDMOS und PLDMOS betragen 50 µm bzw. 100 µm. Die Kanallänge ist in beiden Fällen 9 µm. Die Messergebnisse zeigen, dass NLDMOS sowohl auf Chipfilm™ Wafern als auch auf Bulk-Referenz-Wafer erwartungsgemäß funktionieren. Der NLDMOS weist eine Durchbruchspannung von > 100 V mit einem Drainstrom von ca. 4,5 mA auf, der etwa halb so groß wie der aus der Simulation erwartete Strom ist. Als ein Grund hierfür sei die Selbsterwärmung des Bauelements im Test genannt, die aus dem Abfallen des Drainstroms mit ansteigender Drain-Source-Spannung offensichtlich ist. Auf Bulk-Referenz-Wafern ist die Durchbruchspannung der PLDMOS Transistoren etwa 50 V bei einem Drainstrom von ~ 0,3 mA, was 10-mal geringer ist als der simulierte Wert. Auf Chipfilm™ Wafern weisen die PLDMOS Transistoren keine Funktionalität auf. Untersuchungen zeigen, dass Prozess-Schwankungen der Grund für dieses Ergebnis sind. Diese Abweichungen vom optimierten Entwurf umfassen eine größere Tiefe des Shallow Trench, eine geringe Tiefe der Drift-Implantation und ein irrtümlich dickeres

Gateoxid von 100-nm im Vergleich zum gewünschten Wert von 15 nm; hierdurch endet ein Großteil der Dosis der *p*-Drift-Implantation im Gateoxid, sodass das Driftgebiet unzureichend stark und tief dotiert wird.

Nach den Messungen auf dem Wafer werden Gräben an den Chip-Kanten geätzt und die ultra-dünnen Chips mithilfe des Pick, Crack & Place^{TM} - Verfahrens vom Trägerwafer abgelöst.

Die Chips werden auf drei verschiedenen Substraten aufgebaut, auf einem freien Silizium-Wafer, in einem 24-poligen Keramik-Gehäuse und auf einer Polyimid-Folie. Die elektrischen Eigenschaften werden in jedem Fall zunächst im flachen Zustand gemessen. Der Abfall des Drain-Stroms wird als Indikator des Grades der Eigenerwärmung verwendet Der Abfall des Drain-Stroms infolge Eigenerwärmung ist minimal (10%) beim Bulk Referenz-Wafer. Beim Chipfilm^{TM} -Wafer ist der Wert erhöht auf 24%, d.h. der thermische Widerstand ist in diesem Fall beinahe 3-mal höher als der des Bulk Referenz-Wafers. Der Grund für diesen Unterschied ist der effektiv höhere thermische Widerstand im Bereich der vergrabenen Hohlräume auf den Chipfilm^{TM} Wafern, die den Wärmefluss von der aktiven Schicht zum gekühlten Substrat hin erhöhen. Auf Polyimid-Folie beträgt der Abfall des Drain-Stroms sogar 35%. Der interne Temperaturanstieg berechnet sich zu mindestens 13 ^{O}C für den Bulk-Referenz-Wafer und bis zu 40 ^{O}C im Falle der Polyimid-Folie.

Die Chips auf Folien sind auch unter Biegebeanspruchung gemessen worden. Der Biegeradius wird von 100 mm bis 7,5 mm variiert, was einer Zugspannung von bis zu 200 MPa entspricht. Die Messungen werden sowohl für Längs-und Querrichtung durchgeführt, um so longitudinalen sowie transversalen Stress relativ zu Stromfluss in Kanal einzuprägen. Der NLDMOS zeigt die erwartete Zunahme des Drain-Strom in beiden Fällen, wobei der größere Anstieg für die longitudinale Ausrichtung gemessen wird

Abschließend kann festgestellt werden, dass die vorliegende Arbeit trotz der unvollständigen experimentellen Ergebnisse einen Hinweis darauf gibt, dass sowohl der NLDMOS als auch der PLDMOS auf sehr dünnen Silizium-Substraten bis zu einer Dicke von 10 µm machbar sind, und, dass diese Bauelemente mit Verwendung herkömmlicher TCAD-Werkzeuge entworfen und optimiert werden können.

Abstract

In this thesis, single-crystal silicon based ultra-thin (~ 20 μm) high-voltage (100 V) lateral diffused metal-oxide semiconductor (LDMOS) transistor structures and their fabrication results on Chipfilm™ substrates are presented.

The characteristics of ultra-thin LDMOS transistors are first simulated using the tools Atlas and Athena of Silvaco. Processing starts with a conventional bulk silicon wafer which, in Chipfilm™ technology, receives a 1–2 μm p^+ layer at the wafer surface. Epitaxial layers are grown over this p^+ layer. The buried p^+ doping profile of the Chipfilm™ wafers is replicated in Atlas by simulating the epitaxial layer growth over a p^+ layer. The *n*-well and *n*-drift implants are combined in order to reduce the processing steps. A drive-in step for 900 minutes at 1150 ^{O}C is employed after *n*-well/drift implant. The thermal budget for the drive-in is set after simulating the effect of boron-out diffusion from the p^+ layer at the bottom of epitaxial layer. Shallow trench isolation (STI) is used to achieve desired thickness of the field oxide while keeping the thermal budget at a minimum. A threshold implant is used only in the NLDMOS. A 15 nm thick gate-oxide is used, which is identical to the thickness used in the low-voltage CMOS structures of the corresponding 0.5-μm CMOS technology at IMS CHIPS. The poly-gate and spacer deposition, as well as the drain and source implants, are performed by using standard process steps. The process flow is otherwise fully compatible with that of a high-voltage LDMOS technology of IMS CHIPS.

Optimisation of various device parameters is then performed. These parameters include depth of shallow trench and junctions, implant doses and implant energies. For a breakdown voltage of 100 V the optimised trench depth is found to be 300 nm, the *p*-drift junction depth is ~ 1 μm and the *n*-well/drift junction depth is ~ 5 μm. Due to relatively deep junctions of the *n*-drift region, the NLDMOS is less vulnerable to slight variations in those optimised process parameters, whereas the shallower *p*-drift junction depth makes the PLDMOS quite sensitive to such variations. Simulation results show that in order to keep the breakdown voltage above 100 V the shallow trench depth of the PLDMOS should be precisely in the range of 200 – 350 nm. Therefore, very accurate control of the trench depth is required in case of the ultra-thin PLDMOS.

Simulations of electrical characteristics for both the NLDMOS and the PLDMOS are performed with these settings: channel length = 10 μm; gate field-plate length = 10 μm ;

drift region length = 20 µm ; gate field-plate length = 10 µm ; *n*-well/drift implant dose = $4 \cdot 10^{12}$ cm^{-2}; *p*-drift implant dose = $6 \cdot 10^{12}$ cm^{-2}; substrate concentration = $1 \cdot 10^{15}$ cm^{-3}. The simulation results reveal a threshold voltage of 0.6 V for the NLDMOS and of 1.2 V for the PLDMOS. The maximum drain current in case of NLDMOS 180 µA/µm whereas in case of the PLDMOS it is 30 µA/µm.

The device layout for mask fabrication is generated by using the COMPASS design automation tool. Prior to LDMOS fabrication, Chipfilm™ wafers are prepared to achieve buried cavities on the wafers, which separate and define the thin chips early on. Control devices are fabricated on bulk reference wafers, which received the same processing as Chipfilm™ wafers with the exception of the buried cavities.

On-wafer measurements are performed for receiving DC input and output characteristics of both NLDMOS and PLDMOS. The channel widths of NLDMOS and PLDMOS are 50 µm and 100 µm, respectively. The channel length is 9 µm in both cases. The measured results show that NLDMOS works properly on both Chipfilm™ wafers and bulk reference wafers. The NLDMOS exhibits a break down voltage of > 100 V with a drain current of about 4.5 mA, which is nearly half of the value expected from the simulation of an optimized device structure. The drain current decays in the saturation region due to self-heating, which arises due to the excessive power dissipation in the device. On bulk reference wafers, the breakdown voltage of PLDMOS transistors is about 50 V with a drain current of ~ 0.3 mA, which is 10-times less than the simulated value. On Chipfilm™ wafers the PLDMOS transistors do not exhibit any functionality. Investigations reveal that process variations are the reason for this result. These variations include a higher shallow trench isolation (STI) depth, a low drift-implant depth and a growth of a 100 nm thick oxide instead of 15 nm by mistake, through which the *p*-drift implant is performed. All these variations add up to vanishing of the drift region and, hence, device failure.

After on-wafer measurements, trenches are etched at the chip edges and the ultra-thin chips are detached from the original wafer by using a Pick, Crack&Place™ technique.

The chips are then placed on three types of substrates, including a blank silicon wafer, a 24-pin ceramic package and a polyimide foil. Electrical characteristics are measured for each case in flat state. Reduction in drain current with increasing drain-source bias is examined to verify device self heating in each case. The reduction in drain current due to self heating is minimum (10%) in case of bulk reference wafer. For the case of Chip-

film^{TM} wafer it is 24% since the thermal resistance in this case is almost 3-times higher than for the bulk reference wafers. The reason for this difference is the presence of the buried cavities in Chipfilm^{TM} wafers, which hinder the flow of heat from the active layer to the bulk which is in thermal contact to the ambient. On polyimide foil the reduction in drain current amounts to even 35%. The junction temperature rise above ambient is minimum 13 ^{O}C in case of the bulk reference wafer and maximum 40 ^{O}C in case of the polyimide foil.

The chips on foil are also measured under bending stress. The bending radius is varied from 100 mm to 7.5 mm, representing a tensile stress up to 200 MPa. Measurements are performed for both longitudinal stress and transversal stress relative to the current flow in transistor channel. The NLDMOS exhibits the expected increase in drain current for both cases, with the larger increase in case of longitudinal stress.

The results summarized in this thesis, in spite of the incomplete experimental evidence, provide an indication that both NLDMOS and PLDMOS on thin silicon substrates down to 10 µm thickness are feasible and that those devices can be designed and optimized by using conventional TCAD tools.

1 Introduction

The roadmap for miniaturization of electronic devices posed by the well-known Moore's law [1] has led the electronic industry to the realm of flexible electronics. This paradigm shift from thick and rigid electronic chips to mechanically flexible ultra-thin chips has revealed an entire new domain of electronics applications. Radio frequency identification (RFID), smart dust, electronic textile, electronic lens, three-dimensional integrated circuits (3D ICs) and flexible displays are only a few examples from this new domain [2]-[4]. System-in-foil, an emerging area of flexible electronics, offers integration of a complete micro system on a single flexible substrate. The system-in-foil technology, thus, helps in increasing mechanical flexibility and reliability of a flexible system and also in reducing cost [5].

Flexible electronic systems require mechanically rugged flexible substrates, high performance ultra-thin chips and a low-cost fabrication process. The materials adopted for flexible substrates include flexible glass sheets, thin metal and plastics foils [6]-[8]. Glass films bear good mechanical and thermal stability and have a high melting temperature. Glass substrates also fulfill the requirements of low permeability, surface smoothness and low co-efficient of thermal expansion (CTE). However, glass films are brittle and expensive. Production of large and thin sheets of glass is not an easy task. Thin metal foils show good barrier properties against oxygen and moisture. They can withstand high processing temperatures. However, they are expensive and not able to last through multiple bending events. Because of their opaque properties they can only be used in non-transmissive displays or products. Plastic substrates like Polyether terephthalate (PET), Polyether Naphthalate (PEN) and Polyimide (PI) are inexpensive and suitable candidates for roll-to-roll (R2R) production. Although the plastic foils are inexpensive, they have relatively low glass transition (T_g) and melting (T_m) temperatures as compared to metal foils and thin glass sheets [9],[10]. Direct fabrication on plastic substrates therefore requires low temperature processed transistors.

Organic thin-film transistors (OTFT) require a low fabrication process (< 200 ^{O}C), which makes them suitable for direct fabrication on plastic substrates. However, they suffer from very low carrier mobilities ranging from 10^{-2} to 3 cm^2/Vs, which is the major shortcoming in organic TFT technology [11]-[13]. The fabrication temperatures required for hydrogenated amorphous silicon (a-Si:H) TFT are in the range of 150 ^{O}C to 300 ^{O}C. The a-Si:H TFT is a well established technology supporting active-matrix

(AM) LCD and organic light emitting diode displays (OLED). However, the mobility values of TFTs in this technology lies in the range of 1–5 cm^2/Vs [14],[15]. These very low mobility values prevent from exploiting a-Si:H technology for high-performance circuit integration. Fabrication of TFTs on nano-crystalline and micro-crystalline films increases the electron mobility to about 40–50 cm^2/Vs [16],[17]. Polysilicon TFTs bear mobility values of about 300 cm^2/Vs for NMOS and 100 for PMOS transistors but the processing temperatures (~650 ^{O}C) is not well suitable for plastic substrates [18]. Low temperature (< 350 ^{O}C) processed polysilicon TFTs can be directly fabricated on plastic substrates, like polyimide, but at the cost of low carrier mobility values which reduce to about 50 cm^2/Vs [19].

The state of the art single-crystal silicon technology offers carrier mobility values of about 1050 cm^2/Vs and 450 cm^2/Vs for *n*-type and *p*-type silicon, respectively. However the fabrication process includes very high temperature steps which are not suitable for direct fabrication on plastic substrates. Transfer of pre-fabricated transistors onto flexible plastic substrates has paved the way for having high-speed devices on flexible substrates [20].

Applications of flexible electronics, like flexible displays, require high-voltages, usually several tens of volts, in order to drive the pixels through matrix back-planes. Technologies like quick-response liquid powder displays require voltages up to 70 V for proper functionality [21]. In addition to the high voltage, high carrier mobility values are also required to meet the requirements of displays with fast refreshing rate. This scenario makes the ultra-thin chips with high-voltage single-crystal transistors very attractive for such applications.

Handling of ultra-thin chips is a major issue in flexible electronics. Conventional methods of back-side grinding do not work efficiently for thickness far below 50 µm. However, non-conventional techniques like “Dicing and thinning” [22], “Dicing before grinding” [23] and chip fabrication on buried cavities known as “Chipfilm^{TM} technology” [24] have been developed to deal with ultra-thin chip handling and placements issues.

The conventional structure of a high-voltage MOS transistor structure on bulk silicon contains deep well regions (up to a few tens of micrometers) in order to sustain high-voltage across their well-substrate junctions. These deep-well regions put a constraint

on reduction of device thickness. Silicon-on-insulator (SOI) technology offers structures of high-voltage MOS devices with a silicon layer thickness of < 10 µm [25], but the SOI technology is still entangled in challenges like removal and transfer of ultra-thin chips from Insulator substrates, complexity of the process and most prominently the high cost [26].

Bulk technology offers low cost solution for device fabrication. Unfortunately, only a few attempts have been made to make use of this low cost bulk technology for flexible electronics. An ultra-thin high-voltage (~ 100 V) LDMOS transistor structure using bulk silicon technology was reported in 2008 [27] where a back-side grinding technique was employed to reduce the chips thickness to 35 µm. To our knowledge, no reports have been published so far for ultra-thin high-voltage LDMOS with thickness below 35 µm using low cost bulk silicon technology. Reduction in chip thickness to less than 20 µm is required in order to increase the mechanical flexibility and stability of the thin micro system. By using Chipfilm™ technology, ultra-thin chips with thicknesses < 20 µm can easily be fabricated.

In this work, we present a process for ultra-thin high-voltage LDMOS transistor integration on Chipfilm™ wafers. The process is fully compatible with conventional high-voltage LDMOS transistor technology using shallow trench isolation (STI). Before device fabrication the conventional bulk silicon wafers are processed through Chipfilm™ technology to form buried cavities underneath a 1–2 µm p^+ layer. An epitaxial layer with a well defined thickness is grown over this p^+ layer which is then used for device fabrication. Ultra-thin high-voltage LDMOS chips with thickness ~ 20 µm are realized. The measured results of the performance of these LDMOS on ultra-thin chips are presented for flat and bent state.

In chapter 2, structures and phenomena relevant to high-voltage devices are explained. Chapter 3 deals with the issues related to ultra-thin chips. Pros and cons of difference flexible substrates and handling of ultra-thin with special reference to Chipfilm™ technology are presented. A method for characterization of ultra-thin chips under bend state is shown. Physical phenomena like piezoresistivity and thermal issues are also discussed.

Chapter 4 describes an application example to show under which requirements such ultra-thin devices have to operate. The example of a flexible display is considered and the requirements of the system are discussed for this scenario. Attempts for making

driver circuits using different technologies have been discussed along with their limitations. Particular attention is given to the issue of device self-heating.

Chapter 5 is divided into two parts. The first part deals with the process simulation of ultra-thin LDMOS devices. The simulated electrical characteristics are presented along with the effect of parameter variation on the device performance. The second part shows the details of device fabrication and related issues.

In chapter 6, the measured results are presented for the fabricated devices. The measurements are performed for both flat state and bend state.

In chapter 7, the performance of the fabricated ultra-thin high-voltage NLDMOS transistor as a high-voltage switch in a flexible-display driver circuit is presented. The device parameters are extracted through HSPICE and ICCAP. The load is calculated for a 15-inch display and the high-voltage switch is simulated in HSPICE. At the end, the device junction temperature, which is considerably above ambient temperature, is calculated.

In chapter 8, we summarize the results and discuss the potential for improving the device characteristics.

2 High-voltage metal-oxide-semiconductor (HVMOS) transistors

From nano-devices to power circuits, the operating voltage ranges from a few volts to hundreds of volts. The term “high-voltage” is, therefore, a relative term. Generally, voltages up to 5 V are regarded as low voltages and levels beyond that are considered high-voltages [28]**.** The trend of device integration technology is to increase device density, reduce supply voltage levels and at the same time achieve optimized performance, speed and cost. This trend has caused a compatibility gap between the integrated circuit (IC) output power capabilities and the requirements of high biases for systems like display drivers, automotive applications and motor controls. The compatibility gap is filled by introducing an interface block between low-voltage processing circuits and high-voltage applications. The interface block employs high-voltage transistors to shift the bias levels according to the system requirements. In most cases metal-oxide semiconductor (MOS) devices are used in level-shifter or driver circuits as compared to bipolar-junction transistors, because of their high input impedance and the required simple gate drive circuits. The basic structure and operation of a conventional high-voltage MOS transistor is similar to that of a conventional low-voltage MOS transistor. In order to sustain high-voltages, additional features, like a drift-region, are incorporated in these structures.

2.1 Low-voltage MOS transistor

A typical low-voltage MOSFET is a four terminal device (substrate, gate, source and drain). Figure 2.1 illustrates the schematic sketch of a MOSFET structure. The region under the gate, bordered by source and drain is called the channel region. An appropriate voltage at the gate terminal produces an inversion layer in channel region. The inversion layer connects the drain and source terminals by providing a conductive path (channel) between them. Once connection is established, current starts flowing between the source and drain terminals through the channel.

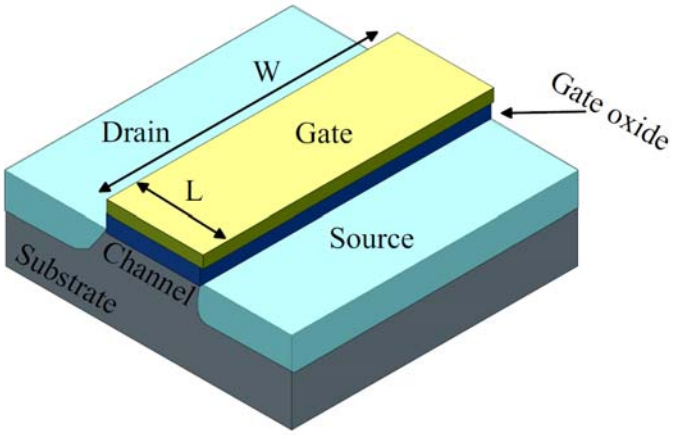
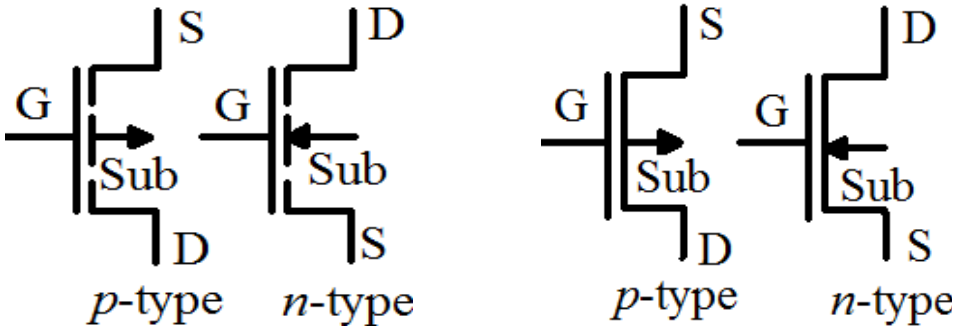


Figure 2.1: Conventional low-voltage MOS transistor structure.

The type of charge carriers in the inversion layer determines the type of a MOS transistor as either an *n*-type transistor (in case of electrons) or a *p*-type (in case of holes). If the inversion layer and, thus, the channel are formed due to the application of voltage at the gate terminal, the device is termed as an *enhancement mode*. If, however, the channel exists without applying any gate voltage and gate voltage is used to either suppress or further open the channel, the device is called a *depletion mode* transistor. Symbols of enhancement mode and depletion mode MOSFETS are shown in figure 2.2.



a) b)

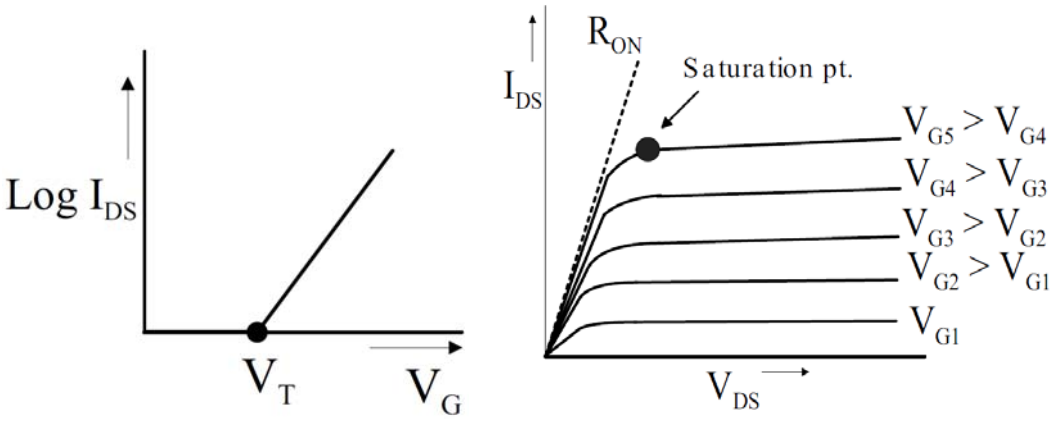
Figure 2.2 : Circuit symbols of MOSFETs a) Enhancement mode b) Depletion mode

Since the structures of the two types of MOS transistors are identical, they are considered complementary with respect to the types of doping and the bias polarities. Therefore, from now on, for both low-voltage and high-voltage MOS transistors only

the case of *n*-type MOS (NMOS) enhancement mode will be discussed unless mentioned otherwise.

2.1.1 MOSFET operation:

The NMOS transistor requires a positive voltage at the drain terminal with respect to the source terminal for proper operation. The gate-voltage (V_{gs}) is used to switch the transistor from ON to OFF state, and vice versa. At low gate-voltage (V_{gs} < threshold voltage (V_t)) the transistor is in the OFF-state. If V_{gs} becomes higher than V_t i.e. $V_{gs} > V_t$, an inversion layer of electrons builds the channel region, provides a conductive path between source and drain region and brings the transistor in the ON-state. With further increase in V_{gs}, more minority charge from the bulk enters the inversion layer and increases the conductivity of the channel path. The more conductive the channel is, the higher is the current flowing between source and drain. Typical input and output characteristic curves of an NMOS transistor are shown in figure 2.3:



a) b)

Figure 2.3: a) Input characteristics b) Output characteristics

The output characteristics indicate, that in the vicinity of drain voltage V_{DS} = 0 V the drain current I_{DS} increases linearly. With the increase in V_{DS}, this variation in the drain current I_{DS} becomes proportional to V_{DS}^2 until a saturation point is reached. Beyond the saturation point, the current remains almost constant with further increase in V_{DS}. For linear and saturation region the drain current (I_{DS}) is given as:

$$I_{DS} = \frac{W}{L}\frac{C_{OX}}{2}\mu_n\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \qquad \text{(Linear)} \qquad (2.1)$$

$$I_{DS} = \frac{W}{L}\frac{C_{OX}}{2}\mu_n\left(V_{GS} - V_T\right)^2 \qquad \text{(Saturation)} \qquad (2.2)$$

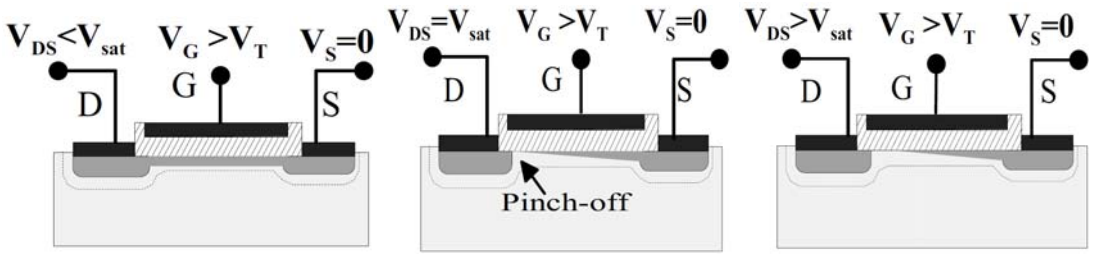
At the saturation point near the drain, the difference of gate and drain voltages becomes equal to threshold voltage (V_T) i.e.

$$V_{GS} - V_{DS}(sat) = V_T \qquad (2.3)$$

This reduces the thickness of the inversion layer to zero near the drain contact, as shown in figure 2.4b. The state of an entirely suppressed inversion layer is called “pinch-off”, the location at which this occurs is called “pinch-off point” and the drain voltage at which pinch-off is initiated is called V_{DS}(sat). The pinch-off point first appears near the drain contact because there the reduction of the local gate-bulk bias compared to the applied gate-source bias is maximum. If V_{DS} is further increased beyond V_{DS}(sat), the pinch-off point starts moving towards the source terminal, while the gap to the drain contact is covered by a space-charge region (figure 2.4c). The charge carriers have to travel now through both the channel inversion layer and the space charge region. In the space-charge region the high electric-field sweeps them towards the drain terminal at maximum carrier velocity, while within the channel the carriers move considerably slower (except for very short channels). Due to variation in length of the inversion layer, the channel length cannot be considered constant. A change in channel length (ΔL) has to be taken into consideration. This variation in effective channel length (L - ΔL) with varying V_{DS} leads to a non-constant drain current (I_{ds}) in the saturation region; this is called “channel length modulation” [29].

The ability of a transistor to control analog signal characteristics, e.g. amplification, is described by its trans conductance. In the case of MOS transistors this is the ratio of change in drain current to change in gate voltage. i.e.

$$g_m = \frac{\Delta I_D}{\Delta V_G} \qquad (2.4)$$



a) b) c)

Figure 2.4: a) Linear mode b) Saturation point c) Pinch-off point moves towards the source terminal.

In non-saturation region, the trans-conductance does not depend upon gate voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{WC_{OX}\mu}{L} V_{DS} \tag{2.5}$$

However, in saturation region, the trans-conductance becomes a linear function of the gate voltage V_G

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{WC_{OX}\mu}{L}\left(V_{GS} - V_T\right) \tag{2.6}$$

2.1.2 MOS parasitics

The performance of a semiconductor device depends largely on its parasitic capacitances and resistances. These parasitics are formed due to the overlapping of different types of material layers during fabrication. In case of a MOSFET, there are various parasitic capacitances and resistances. A simplified schematic of these parasitics is shown in figure 2.5.

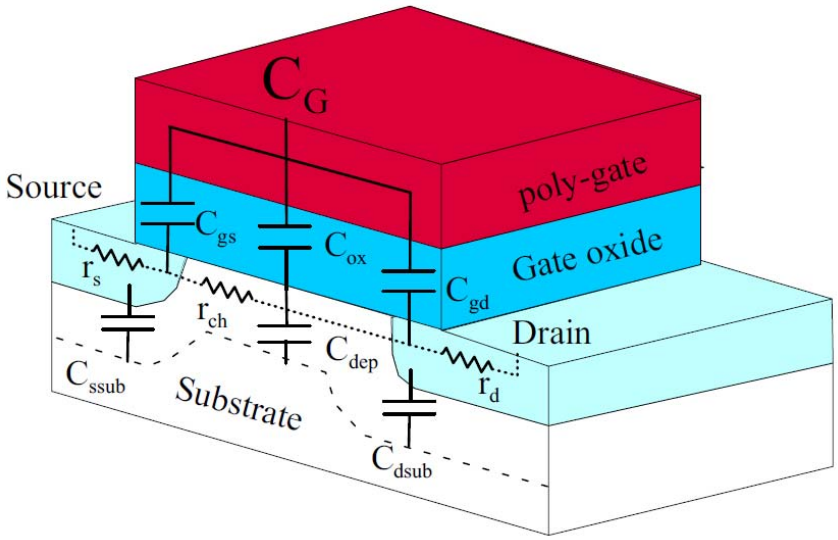


Figure 2.5: Parasitic capacitances and resistances in a MOS transistor.

Here

C_G = Overall gate capacitance

C_{gs} = gate-source overlap capacitance

C_{gd} = gate-drain overlap capacitance

C_{ox} = Gate-oxide capacitance

C_{dep} = Capacitance due to depletion region under gate-oxide

C_{dsub} = drain-substrate capacitance

C_{ssub} = source-substrate capacitance

r_d = drain series resistance

r_s = source series resistance

r_{ch} = resistance from slope of output I-V curve

The presence of insulator layer between gate contact and substrate gives rise to gate capacitance C_G. Mainly, it comprises of gate-oxide capacitance which is given in terms of capacitance per unit area as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.7}$$

where ε_{ox} and t_{ox} are the permittivity and thickness of the gate-oxide respectively. The capacitance due to the depletion region C_{dep} in a semiconductor underneath the gate-oxide also affects the gate-capacitance, depending if a channel is formed or not. It is in series with the gate-oxide capacitance and its value changes with variation in the applied gate voltage. The source and drain regions do not end exactly at the edges of the gate. A small portion of source/drain dopant diffuses into the area underneath the gate-oxide. The overlapping of the gate and the source/drain results into formation of considerable overlap capacitances. The overlap capacitances due to source and drain regions are represented as C_{gs} and C_{gd} respectively (figure 2.5). These capacitances add up in the oxide capacitance and increase the total gate capacitance. C_{dsub} and C_{ssub} are the capacitances of the depletion region between the substrate and the drain or source regions. In case of common source mode, where the source is connected with the substrate, C_{ssub} does not have any influence on the device behavior as the voltage across it is always zero [29].

2.2 High-voltage MOS (HVMOS) transistors

Reports on the high-voltage blocking capabilities of MOS devices started appearing in literature during the early 70's [30]. By the mid 70's, due to the rapid improvement in MOS device performance, the research focus was shifting slowly from bipolar to MOS transistors for high-voltage applications. In 1979, the Reduced Surface Field (RESURF) technique was proposed, which enabled thin epitaxial layers to sustain high voltages [31].

2.2.1 RESURF technique

Using the RESURF technique, a comparably higher breakdown voltage is achieved by having complete depletion of a drift region before occurrence of lateral breakdown. Figure 2.6 shows the structure of a RESURF diode, taken from [30]**,** which consists of a lateral p^+/n^- diode and a vertical p^-/n^- diode.

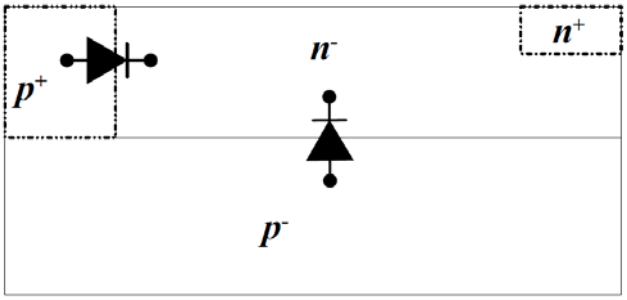


Figure 2.6: RESURF diode [30].

Under normal circumstances (non-RESURF condition), the breakdown occurs at the p^+/n^- junction, as shown in figure 2.7. In the p^+ region, the depletion region cannot penetrate, which results into a high electric field for relatively low voltages, thus, causing junction breakdown.

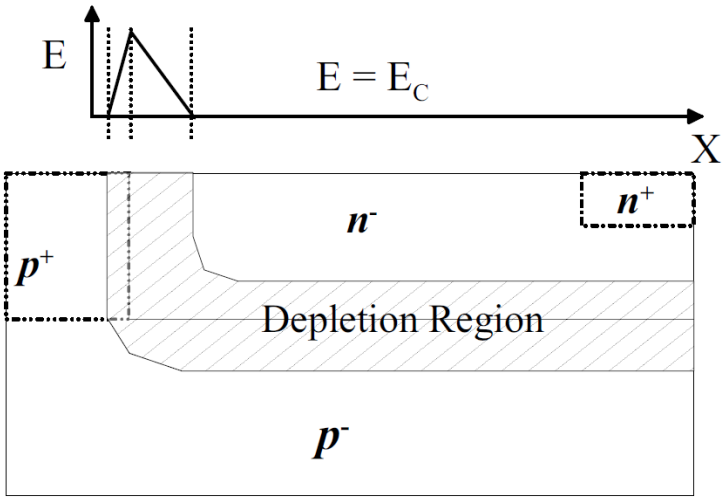


Figure 2.7: RESURF diode – breakdown at the p^+/n^- junction.

Using the RESURF technique, the doping density of the *n*- region and its thickness is adjusted so that the depletion region of vertical diode reaches the surface before the breakdown limit of the lateral diode appears. This helps in redistribution of the field lines over a relatively large area and, thus, reduces the maximum electric field below the critical level even for higher voltages as shown in figure 2.8.

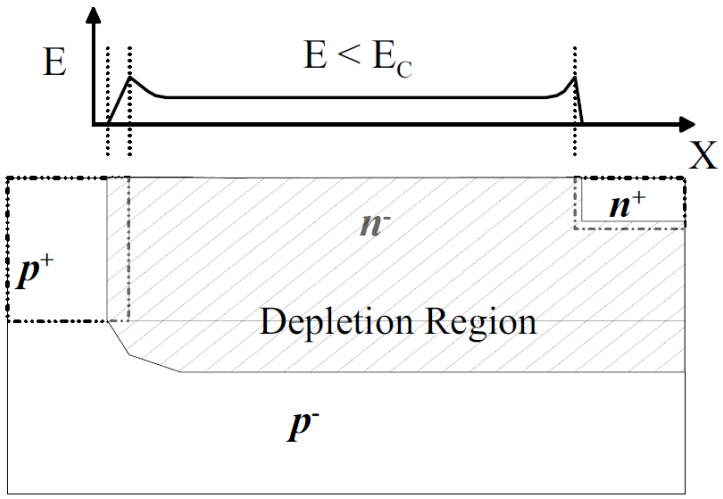


Figure 2.8: Electric field peaks for the RESURF condition

Under RESURF condition, the peak electric field appears at two positions, i.e. at the junction of p^+/n^- diode and at the edge of n^+ region. RESURF condition depends upon the charge density and the thickness of *n*-layer [31]. For a substrate doping of $2–3 \cdot 10^{14}$ cm^{-3} the optimum charge density was calculated to be $1 \cdot 10^{12}$ cm^{-2} [31]**.** i.e.

$$N_{epi} \cdot d_{epi} = 10^{12} \text{ at/cm}^2 \qquad (2.8)$$

where

N_{epi} = doping concentration of epi layer

d_{epi} = thickness of epi layer.

Besides N_{epi} and d_{epi}, the substrate doping (N_{sub}) and the distance between n^+ and p^+ regions (drift length) also influence the breakdown voltage limit [31],[32].

In LDMOS, the RESURF technique was first applied by S. Colak [33]. A breakdown voltage of an LDMOS of 425 V was reported with a specific On-resistance of 9.4 ohm-mm^2. Later on, a number of attempts have been made to optimize the RESURF technique for improving both the breakdown voltage (BV) limits and R_{on} of MOSFET

devices [34]-[36]. During early 90's, a successful application of the RESURF technique on Silicon-on-Insulator device was reported [37]. This led to a breakdown voltage of more than 600 V. Today, the RESURF technique is used in almost any high-voltage MOS transistor.

In order to raise the breakdown voltage limit and reduce R_{on}, various methods in addition to RESURF can be applied. Among these are the use of internal field rings [38],[39], employment of a buried layer [40] and modifications like triple well architecture and super-junction LDMOS [41],[42]. Super junction design exploits alternate *n* and *p*-type layers to form a multi-RESURF structure. Use of field plates also enhances the breakdown voltage by modifying the distribution of field lines at the surface [43]-[45].

2.2.2 High-voltage MOS transistor structure

The structure of a typical high-voltage MOSFET is similar to that of a conventional low-voltage MOSFET. Both contain drain, source, gate and substrate terminals and a channel region between drain and source. The presence of a low-doped drift region in addition helps to sustain high-voltages, as shown in figure 2.9. The operation of a high-voltage MOSFETs is similar to that of a low voltage MOSFETs. A gate voltage above threshold creates a channel between source and drift region. The charge carriers flow from source to drain through the channel and the drift region.

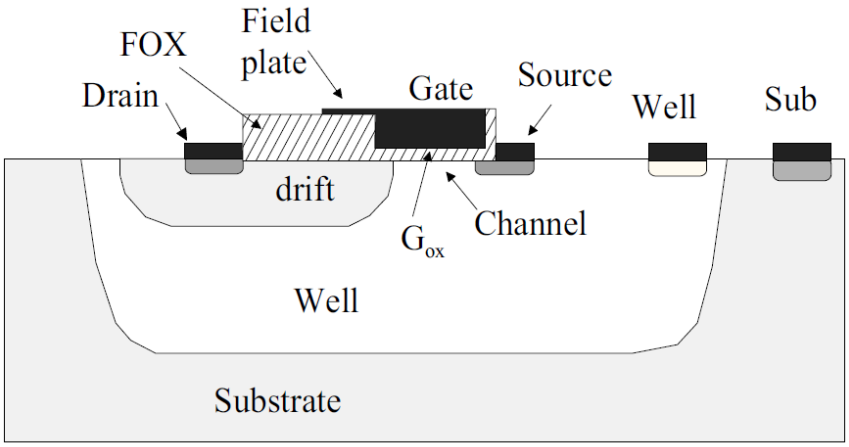


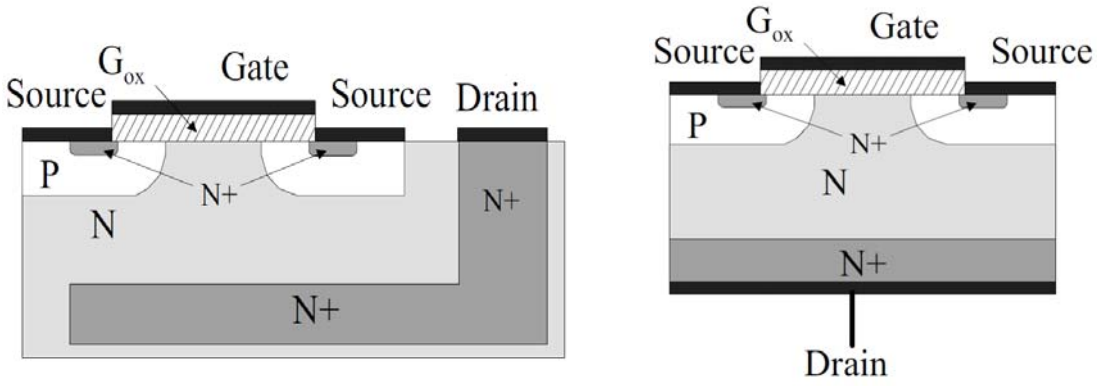
Figure 2.9: High-voltage lateral DMOS transistor structure.

Besides the classification of high-voltage MOSFET as *n*-type and *p*-type or as enhancement and depletion mode, the high-voltage MOSFETs are also categorized on the basis of direction of flow of current in drift region. The current in the drift region can be made either to flow either in horizontal (lateral MOS) or in vertical direction (VMOS).

In a lateral high-voltage MOS transistor, as shown in figure 2.9, the lightly doped drift region is extended laterally and current flows along the horizontal direction between source and drain. The channel formation mechanism could be similar to that of a vertical MOSFETs i.e. as double-diffused structure (DMOS) or with a channel formed by drain-extension (DEMOS). Through drain-extension, a uniform lightly-doped drift region is implanted to extend the drain region to the gate terminal. This helps in reducing the electric field underneath the gate oxide [46]. The channel region is defined by the separation of drift region and source region.

Lateral DMOS devices do not require complex processing like their vertical counterparts. The peak electric field resides at the surface, which can be altered by varying the drift implant dose and by using a gate field plate. The gate field-plate is usually formed by extending the poly-gate over the thick field-oxide within the drift region. Field plates move the peak field point from the surface to the bulk substrate at the edge of the field plate [47].

Vertical MOS transistors offer higher breakdown voltages, high-transconductance and low on-resistance values. The vertical flow of current is achieved by either introducing a buried layer in the substrate or by forming the drain terminal at the back (or bottom) side of the device as shown in figure 2.10.



a) b)

Figure 2.10: a) Buried layer -drain on top b) Drain on bottom

In a vertical MOS transistor, the channel region is formed by a double-diffusion method in which the same lithographic mask window is used for implantation of the channel and the source regions. The channel region is formed by having a deep drive-in of channel implant as compared to the source implant. The difference in diffusion depths determines the channel length. Because of the double-diffusion, the channel has a non-uniform doping profile.

In another type of vertical MOS transistor called V-groove MOS (VVMOS) [48], the channel is formed by first diffusing an unpatterned base-region (p-base in this case) followed by diffusion of the source contact. The substrate acts as a drift region. The base-region left between source contact and drift region after the diffusion step serves as the channel. A V-shape groove is then etched, which crosses the channel region and ends up in the drift region. This technology relies on an anisotropic etching technique to form a V-shape groove. The gate electrode is deposited within the groove region to cover both base and source. In this manner a channel is formed along the walls of the groove as shown in figure 2.11.

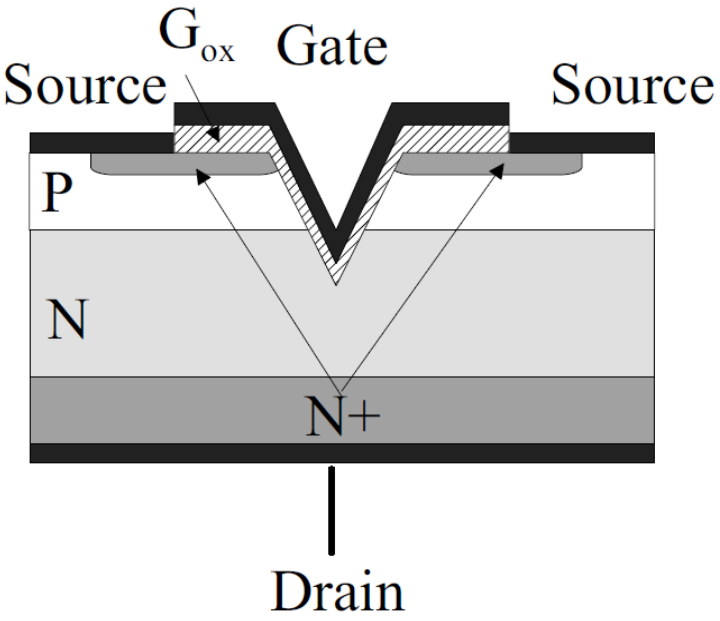


Figure 2.11: V-groove MOS transistor (VMOS) structure

In planar vertical MOS transistors, the channel current flows horizontally whereas the drift current flows vertically. The device design requires an optimization trade-off in speed and on-resistance. The vertical V-groove structure suffers from field crowding at the *p*-diffusion and the *n*-drift junction due to a cylindrical junction edge. Also, controllability of the threshold voltage is less than in a lateral DMOS device. However, this technique offers lower on-resistance than a simple vertical DMOS while maintaining the switching speed [49].

The output characteristic curve of an *n*-channel high-voltage MOS transistor is similar to that of a low-voltage NMOS transistor as shown in figure 2.3. At $V_g = V_s = 0$ V, the high-voltage drops across the drift-well junction. The maximum voltage that can be applied depends upon the breakdown limit of the drift-well reverse biased junction. At positive gate voltages, with respect to source, the current starts flowing through channel and drift regions.

For low drain voltage, channel and drift regions both contribute to the on-resistance. For large gate biases, the channel resistance and, hence, the total on-resistance reduces until a point where the on-resistance becomes independent of further change in gate bias. At this stage, the on-resistance becomes almost equal to the drift resistance. A small value of on-resistance is always desirable to achieve low power dissipation ($P_{dissipation}$), given

as

$$P_{dissipation} = I_d V_d = I_d^2 R_{on} \tag{2.9}$$

Also, power dissipation per unit area is given as

$$\frac{P_{dissipation}}{A} = J_d^2 R_{on,sp} \tag{2.10}$$

where

A = chip area

J_d = current density (on-state)

$R_{on,sp}$ = on-resistance per unit area = Specific on-resistance

In a lateral high-voltage MOS transistor the specific on-resistance is given as

$$R_{on,sp} = R_{source} + R_{ch} + R_{accum} + R_{drift} + R_{drain} \tag{2.11}$$

Where

R_{ch} = Resistance of the channel region.

R_{accum} = Resistance of the overlap area between the drift region and the gate

R_{drift} = Resistance of the drift region.

2.3 Breakdown mechanism

In MOS transistors, breakdown occurs due to different phenomena which include avalanche breakdown, surface breakdown, snapback breakdown and gate oxide breakdown.

2.3.1 Avalanche breakdown

In high-voltage MOS devices, the reverse-biased depletion regions sustain high-voltages. The electric field in the depletion region becomes high enough to sweep away any electron entering that region. The velocity of charge carriers and, hence, their energy increases with increasing electric field. For an electric field higher than $1 \cdot 10^5$ V/cm, the charge carriers attain their saturation velocity limit, i.e. $1 \cdot 10^7$ cm/sec. Further increase in the electric field provides the charges carriers with sufficient energy to create

electron-hole pairs by interacting with lattice atoms in their path. This phenomenon is called impact ionization. The electron-hole pairs generated as a result of impact ionization also starts moving towards the depletion boundaries. If the electric field is very high, these electron-hole pairs can receive sufficient energy to generate additional electron-hole pairs themselves. In this way a large number of charge carriers are generated.

The number of electron-hole pairs generated by a single charge carrier while moving through a distance of 1cm in depletion region is described by the impact ionization coefficient. For an electric field ranging from $1.75 \cdot 10^5$ to $6 \cdot 10^5$ V/cm, an approximate value of ionization coefficient is given as

$$\alpha = 1.8 \cdot 10^{-35} E^7 \tag{2.12}$$

Where

α = impact ionization coefficient

E = Electric field strength

Avalanche breakdown occurs when the impact ionization rate become infinite. The avalanche breakdown limit also depends upon the type of junction i.e. if an abrupt, linearly graded junction or diffused junction applies. The junction termination also plays an important role in the determination of the breakdown voltage limit. After implantation, the dopants diffuse vertically as well as laterally. The result is that the edges of the junctions take on the form of a cylindrical or spherical contour. The associated depletion region follows that shape. The electric field lines are forced into crowding at the edges in order to maintain charge balance. This crowding of field lines at the edges leads to high impact ionization as compared to a planar diffused region. This leads to junction breakdown at edges to occur sooner than for a planar region. The crowding of field lines is worst in case of a spherical junction compared to a cylindrical or planar junction. Therefore, such junctions are subject to earlier breakdowns than cylindrical and planar junctions.

2.3.2 Surface breakdown

The breakdown voltage strongly depends upon the depletion region shape which itself follows the junction termination shape. At the surface, the junction terminates with a corner. This shape is the form of a quarter of spheroid [50]. Its radius of curvature is equal to the junction depth. The worst field line crowding occurs in this region compared to the planar junction. In case of charges present at the surface, the shape of the depletion region and, hence, the breakdown voltage limit vary significantly. For example, in case of *n*-type doping on a *p*-substrate, a positive surface charge will extend the depletion region away from the *p*-*n* junction. This spreads the electric field lines, resulting in an increase of breakdown voltage. On the other hand, a negative surface charge in this case will produce the opposite effect by increasing the electric field at the corner [51].

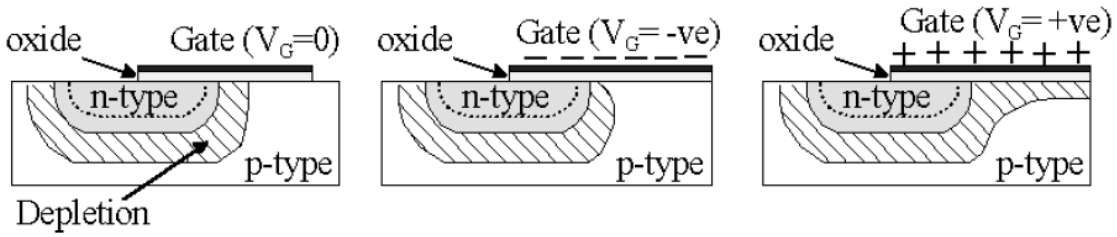


Figure 2.12: Surface field effects: For negative surface charges, depletion region contract. For positive surface charges, depletion region expand under the gate.

2.3.3 Snapback breakdown

Snapback breakdown occurs when a high-voltage across the drain-substrate junction causes a high number of electron-hole pairs within the depletion region due to impact ionization. The holes start moving towards the substrate terminal. Due to the intrinsic substrate resistance, the substrate potential increases near the source contact. When the substrate potential becomes sufficiently high to forward bias the source-substrate junction, the source starts providing electrons to the drain terminal though the substrate. This forms a parasitic bipolar transistor in which the source acts as the emitter, the

substrate as the base and the drain as the collector. When electrons from the source reach the drain-substrate junction, they generate electron-hole pairs within the depletion region. This further increases the forward biasing of the substrate-source junction and in this way a positive feedback loop then leads to the junction breakdown [52].

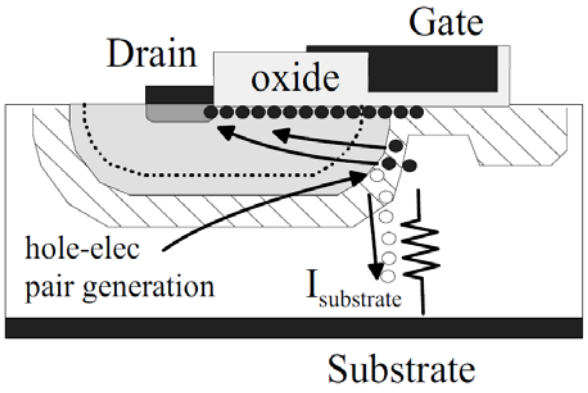


Figure 2.13: Snap back effect

2.3.4 Gate oxide breakdown

Gate oxide breakdown occurs when a conductive path is developed locally through the gate oxide which provides a low-resistance path or even a short between the gate metal/poly and source/drain/substrate regions. Due to the scaling down of devices, the thickness of gate oxide has decreased to only a few nanometers. At these small values the gate oxides are more vulnerable to failure. Failures can occur due to a number of reasons like electrostatic discharge (ESD), rough surface condition, defects in substrates, thermal damage, and traps formation due to channel hot carriers. Whatever the cause of defect may be, the gate oxides are divided into three categories based upon their quality and failure time. The first category relates to defect free gate-oxides. They feature a maximum electric field of 12 MV/cm. Generally, these gate-oxides show the same breakdown voltage as their thickness in nano-meter, i.e. 10 V for 10 nm. The second category relates to gate oxides containing certain defects or a combination of defects as mentioned above. These gate oxides show earlier breakdown and can sustain electric field only up to 7 MV/cm. The third category is the class of gate oxides that possess a considerable amount of defects and show failure even for very small electric fields [28].

2.4 Anomalous effects

In high-voltage devices, deviation from typical MOS characteristic curves may occur due to anomalous effects, which can be due to a number of reasons such as high-resistive paths and high impact ionization. These effects include the Kirk effect, the quasi-saturation effect, the kink-expansion effect and self-heating. A brief introduction to these effects is given below:

2.4.1 Kirk effect

The theory of the Kirk effect was first presented to account for the decrease of cut-off frequency (f_t) in bipolar power transistors at high current densities [53]. In a *p-n-p* or *n-p-n* bipolar transistor the base-collector junction is reversed biased for proper operation of the transistor. The minority carriers from the base enter the collector after passing through a depletion region. The depletion region exists on both sides of base-collector junction. In the depletion region, the drift velocity of minority carriers is limited by scattering [52]**,** which hinders the instantaneous sweeping of charge carriers towards the collector contact. Therefore, a small minority charge carrier density always exists in depletion region. The depletion region readjusts its boundaries on both sides according to the variation in minority charge density to maintain charge neutrality

The value of this charge carrier density depends upon the collector current level. Under normal circumstances this amount is negligible and does not affect the performance of device. For higher current densities, the influx of minority charge carriers in depletion region becomes greater than the out-flux towards collector region. In this situation, the minority charge carrier density in the depletion region becomes no longer negligible. The depletion region on the base side becomes narrow as the charges of the same polarity are passing through it. The depletion region on the collector side becomes increased due to an accumulation of charge carriers of opposite polarity at the depletion boundary. This increases the effective base width and the depletion region moves towards the collector contact. This effect is called Kirk effect. The Kirk effect occurs when the following relation between charge density and density of ionized impurity holds

$$j \geq nqv_s \tag{2.13}$$

where

j = current density

n = minority charge carrier density in depletion region

v_s = Scattering limited velocity.

In high-voltage lateral DMOS transistors, with the increase in current, the electric field lines shift towards drain terminal due to the Kirk effect. Other factors, like the avalanche effect, add up to raise the field strength at the drain terminal. This leads to an early breakdown of the device. However, in case of VDMOS, the Kirk effect poses no drastic changes because of the absence of a RESURF condition and having space for current spreading [54].

2.4.2 Quasi saturation effect

Low doping concentration in the drift region of high-voltage LDMOS or in the collector region of power bipolar transistors produces a quasi saturation region. Common saturation effects arise due to either pinch-off or velocity saturation of charge carriers in the channel region. However, if the velocity saturation occurs first in the drift region instead of the channel region the quasi-saturation effect appears in the device characteristics.

The quasi-saturation state appears at the point when the incoming carrier density exceeds the doping level of the drift. The difference between Kirk effect and quasi saturation is that the Kirk effect occurs only for high drain or collector voltages in the saturation region while quasi-saturation occurs at low voltages already [55]. Quasi-saturation effects can be minimized or even eliminated by increasing the doping level in the drift region, which not only reduce this anomalous effect but will also improve the on-resistance.

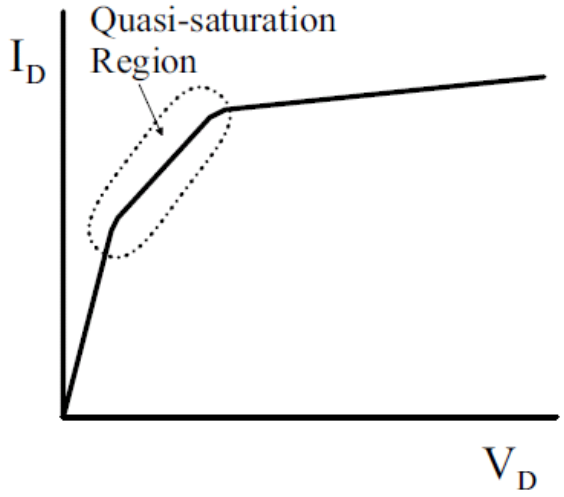


Figure 2.14: Quasi saturation effect

2.4.3 Kink or expansion effect

The kink effect [56] or expansion effect [57] is a step-like rise of drain saturation current in the device characteristics. It occurs because of high impact ionization rate which serves as an extra source of mobile charge carriers. These extra mobile electron/hole pairs create a quasi-neutral region underneath the channel in the body. This accumulation of charges raises the potential of the source-body junction and brings it to forward biased mode. As a result the drain current increases until the voltage across the body-source junction increases to 0.6–0.7 V. At this stage the drain current saturates again. Contrary to a high-doped drift region, in a low-doped drift region the impact ionization rate is not sufficient to generate a significant amount of charge carriers which can cause the kink-effect [58]. The kink effect does not appear if the parasitic bipolar transistor turns ON before achieving a high impact ionization rate. In order to keep the parasitic bipolar transistor OFF before kink-effect is apparent, methods like reducing the value of the shunt resistance of the parasitic *n-p-n* transistor [59] can be employed.

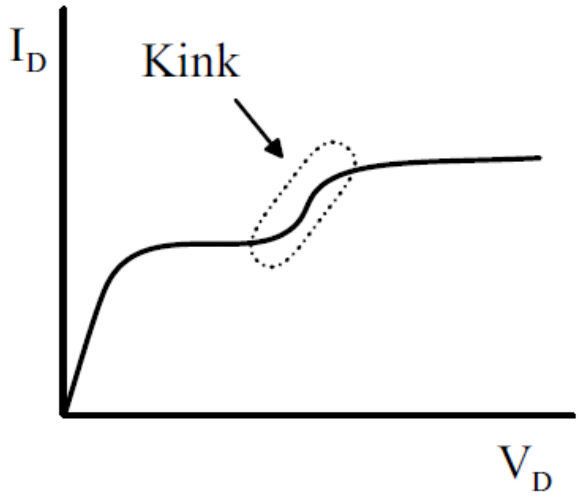


Figure 2.15: Kink Effect

2.4.4 Self -heating effect

Self heating occurs due to an internal power dissipation of a device. Each MOS device has some finite internal resistance (on-resistance). When the current flows through it, power dissipates in the device in the form of heat. The dissipated heat, if incompletely removed from the device, starts raising the active device temperature. This rise in temperature not only degrades the device performance but can even lead to the device failure. For low-voltage MOS devices on thick substrates the self-heating factor is negligible. But in high-voltage devices the self-heating effect no longer remains insignificant. Also with the device scaling and increasing integration density self-heating becomes one of the major issues in device design. With the increase of the internal device temperature due to self-heating the charge carrier mobility decreases because of increased lattice scattering. This causes a negative resistance effect in the characteristic output curves where the current starts falling with increasing drain voltage, as shown in figure 2.16.

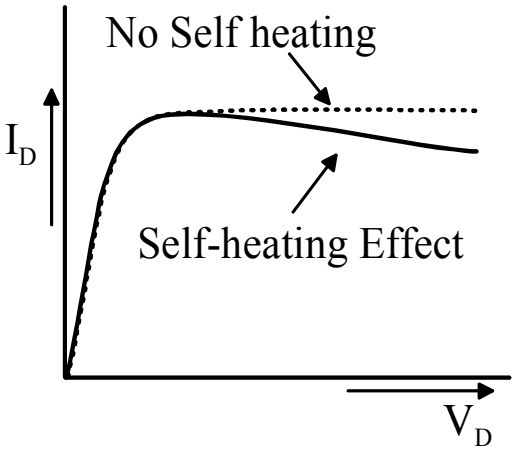


Figure 2.16: Self-heating effect

Three phenomena have an impact on heat generation in the LDMOS device. These are

a. Joule heat

b. Recombination heat

c. Thomson heat

Joule heat depends upon the current density and the electric field. The generation and recombination mechanism of charge carriers gives rise to recombination heat. Furthermore, Thomson heat arises due to current flow through a region having spatially varying temperature. Together, these heating mechanisms give rise to hot spots in a MOS device and leads to device degradation and failure. Among these, Joule heat plays the major role but other mechanisms also have an impact, particularly in case of thermal breakdown and high current density [60].

Self heating effects can be minimized by reducing the internal resistance of the device and connecting a proper heat sink to the internal device in order to remove the heat out from the integrated device. Reduction in the internal resistance, however, requires modification of the device structure. In most cases a trade-off in on-resistance and other device parameters, like breakdown voltage, has to be made. Inclusion of additional features with the device structure, such as *p*-top layers [60] or low doped drain (LDD) implant [61] can help improve the device performance by suppressing the cause of heating phenomena.

2.5 Process flow of conventional high-voltage MOS transistor

The process flow for a typical high voltage MOS transistor is similar to that of a low voltage MOS transistor. Fabrication is performed on a silicon-wafer with [100] surface orientation to benefit from maximum surface mobility and minimum ON-resistance. A lightly doped substrate is required to achieve high breakdown voltages. A conventional process flow of high-voltage MOSFET is shown in figure 2.17.

A high resistivity substrate acts as a starting material. This high-resistivity is achieved by growing an epitaxial layer onto the substrate wafer. A thin screen oxide needs to be grown prior to the implantation steps in order to protect the silicon surface from energetically activated surface contaminants entering the bulk substrate during high-energy implantation. After epitaxy and thin-oxide growth, a well implantation is performed by accelerating high-energy ions into the epitaxial layer followed by a drive-in step. The drive-in step is performed at high temperatures, usually 1100 ^{O}C to 1200 ^{O}C for several hours in order to allow the impurity ions to diffuse sufficiently deep into the substrate material. The implant for the drift region is done after the well implantation followed by a separate drive-in step. A thick field oxide is then grown over the drift region and the field region. The thick field oxide is usually patterned by a local oxidation (LOCOS) technique. After the LOCOS step, a threshold ion implantation is performed to adjust the device's threshold voltage. The threshold implant is followed by a gate-oxide growth and a polysilicon deposition. Implantation for source and drain contact regions is then made to minimize the surface contact resistance and allow for forming low-resistive metal-silicon contacts. The processing ends with the passivation and metallization steps.

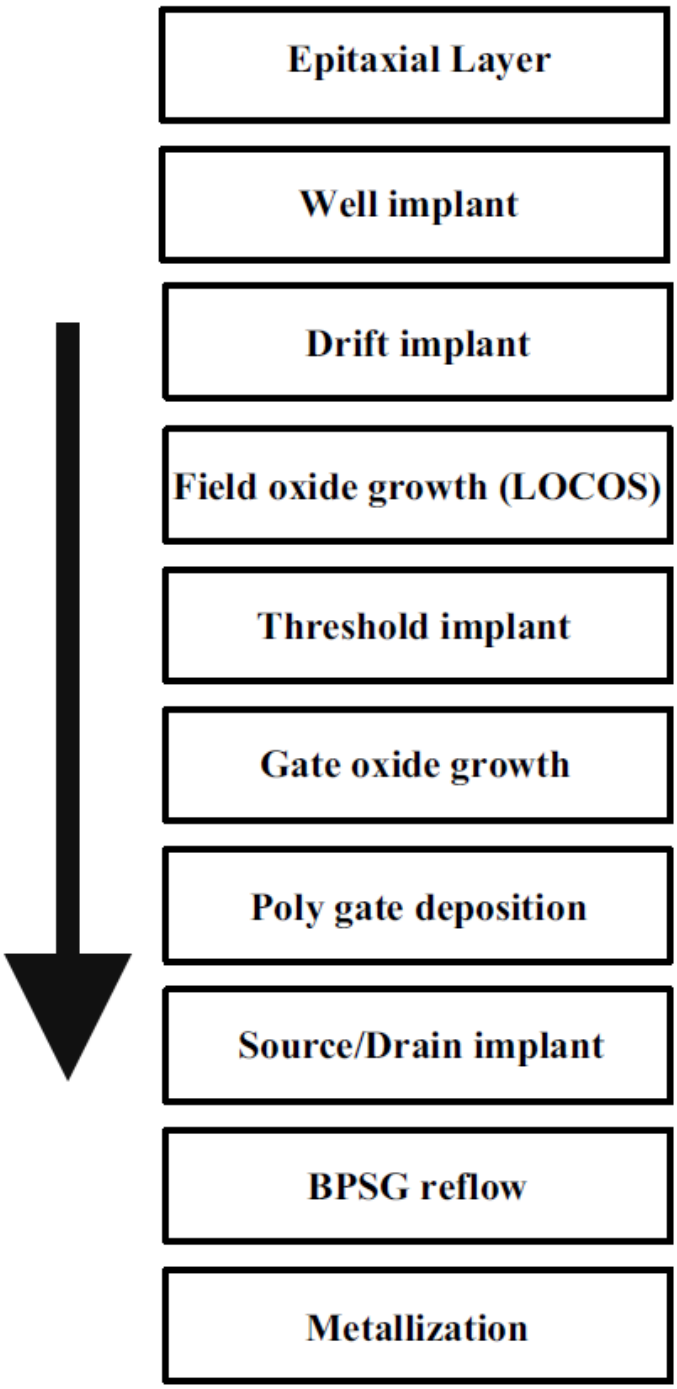


Figure 2.17: **Process flow for a conventional high-voltage lateral DMOS transistor.**

3 Ultra-thin chips

The performance of integrated circuits in ultra-thin chips does not only rely on the performance of the active devices but also on the properties and the state of substrates underneath. Handling of ultra-thin silicon chips during fabrication and after removal during assembly are quite challenging. In this chapter we provide a brief overview of these issues. We also discuss the properties of ultra-thin chips under stress, the characterization of stress effects on the active device and heating effects in a high-voltage transistor on an ultra-thin chip on a flexible substrate.

3.1 Flexible substrates

Flexibility, stability and reliability of flexible electronic products depend largely on the properties of the flexible substrates which serve as a substrate material for the active devices. Besides acting as a substrate material these flexible substrates are used for encapsulation purposes. As the cost of a flexible electronic product significantly depends on the cost of the flexible substrate itself, the focus therefore is on inexpensive flexible substrates in view of mass production of flexible electronic systems.

A good flexible substrate is supposed to have some or all of the following aspects, high glass transition (T_g) and melting (T_m) temperatures, high mechanical stability, low permeability, a smooth surface, optical transparency and a low coefficient of thermal expansion (CTE).

Thin flexible glass films, as well as metal and plastics sheets, can be used as a starting substrate. Glass films bear good mechanical and thermal stability and have a high melting temperature. Glass substrates also fulfill the requirements of low permeability, surface smoothness and low CTE. However, glass films are brittle and comparably expensive. Production of large and thin sheets of glass is not an easy task.

Thin metal foils possess good barrier properties against oxygen and moisture. They can also withstand high processing temperatures. However, they are also expensive and not able to survive multiple bending events. Because of their opaque properties they can only be used in non-transmissive displays or products.

Plastic substrates are inexpensive and suitable candidates for roll-to-roll (R2R) production. There exist a number of candidate plastic substrates. They are divided into crystalline and amorphous materials. A list of polymer substrate belonging to these categories is shown in table 1.

Table 1: Categorisation of polymer materials

Semi-crystalline	**Amorphous**
Polyether terephthalate (PET) Polyether Naphthalate (PEN) Polyetheretherketone (PEEK)	Polycarbonate (PC) Polyethersulphone (PES) Polyarylate (PAR) Polycyclic Olefin (PCO) Polyimide (PI)

In order to replace glass substrates, plastic substrates must possess characteristics comparable to that of glass. They, however, offer various properties expected from a good substrate material, some of which are mentioned below.

The CTE and the T_g are two important factors which must be taken into consideration when selecting a suitable flexible substrate material in order to avoid cracks and strains at later processing stages. It has been shown in [8] that the polymers like polyimide (PI) (T_g ~ 350 ^{O}C) and polyethersulphone (PES) (T_g ~ 220 ^{O}C) have high glass transition temperatures (T_g) and low CTEs. On the other hand, T_g values for Polyether terephthalate (PET) and Polyether Naphthalate (PEN) lie in the range of 80 ^{O}C and 120 ^{O}C, respectively. Values of CTE for PET and PEN materials fall in between the CTEs of PES and PI materials, with PI having the minimum value (8-20 ppm/^{O}C). The quality of PEN substrates can, however, be increased by applying heat stabilization techniques [8].

Flexible display can be bottom emissive or top emissive. For the bottom emissive case the optical clarity of the substrate is essential. However, this is not in the case for the top

emissive display. Therefore, such products can easily utilize opaque substrates like thin metal sheets.

Polycarbonate (PC) and cyclic olefin co-polymer (COC) could be the potential candidate on the basis of good optical clarity but they suffer from poor CTEs and thermal resistance [62].

Polyimide (PI) is yellow in colour with poor optical properties. Therefore, only colourless PI substrates [63] can be used for such applications. PET and PEN have relatively good optical clarity and moisture absorption but are poor in terms of the maximum operating temperatures (T_g (PEN): 120 ^{O}C ; T_g (PET) : 80 ^{O}C) and surface smoothness. Low operating temperature excludes the use of these polymers in high temperature processing.

Flexible plastic substrates are relatively poor in gas diffusion barrier properties as compared to glass substrates. Products like flexible displays, especially organic light-emitting diodes (OLEDs), are very sensitive to moisture. The permitted water vapour transmission rate (WVTR) for OLED (lifetime > 10000 hours) is $1 \cdot 10^{-6}$ g/m^2/day [10] and the Oxygen transmission rate (OTR) is required to be less than 10^{-5} mL/m^2/day (for OLED) [9]. No polymer has such high barrier properties. Solution to this problem is coating with barrier layer on flexible substrates. A few nanometer thick oxide layer, alternating layers of organic and inorganic materials or coating of thin films can be employed to serve as barrier layer [9],[64].

Processing of an electronic system requires a number of solvents and chemicals. Flexible substrates are, thus, required to have good resistance to solvents. Generally, the semi-crystalline polymers bear better resistance against various solvents than the amorphous ones. A hard coat is required to enhance the solvent resistance of amorphous polymers.

3.2 Chipfilm^{TM} technology

Handling of ultra-thin chips during fabrication and after removal from the original substrate is not an easy task. Conventional back-side grinding techniques are not well suitable for wafer thickness < 50 μm due to the crack formation, limited thickness control and poor surface quality. Methods like dicing by thinning [22] have shown good

results in dealing with these issues. However, in the subtractive methods, the final chip thickness is determined at the end of chip fabrication. The final thickness depends upon the trench depth which can vary for each processing lot. In contrast, Chipfilm^{TM} technology [24] is an additive method which allows to precisely determine the chip thickness before device fabrication.

For the Chipfilm™ process, conventional *p*-type bulk wafers are required. In the beginning of fabrication, alignment marks on the bulk silicon wafers are made, which identify the areas where the chips will be positioned later on. In the next step, a dual porous silicon layer is formed at the wafer surface through anodic etching at different etching currents. The dual porous silicon is composed of an upper fine-porous layer and a lower coarse-porous layer. The thickness of this dual porous silicon layer is about 1.5 µm. Annealing at a high temperature is then performed, during which the fine porous layer transforms to single-crystalline silicon containing micro cavities, whereas a formation of a continuous buried cavity takes place in the coarse porous region. The porosity in the silicon layer is directly influenced by the boron concentration at the wafer surface [65]. A Boron concentration of $5 \cdot 10^{18}$ cm^{-3} is used to achieve the desired porosities.

In Chipfilm^{TM} technology, the buried cavities are present only underneath the chip areas. The area between the chips is kept protected from anodic etching through implantations of Phosphorous in that region. This helps the chip area to have firm contacts with the bulk silicon substrate during device fabrication. An epitaxial layer of a defined thickness is grown, which determines the final thickness of the chip prior to device integration during the CMOS process. After completion of the fabrication process, the firm attachments along the chip edges are reduced to only a few anchors by deep reactive ion etching. The chips can then be detached from the substrate and be assembled by using a Pick, Crack&Place™ process. The processing sequence for a Chipfilm^{TM} wafer is shown in figure 3.1.

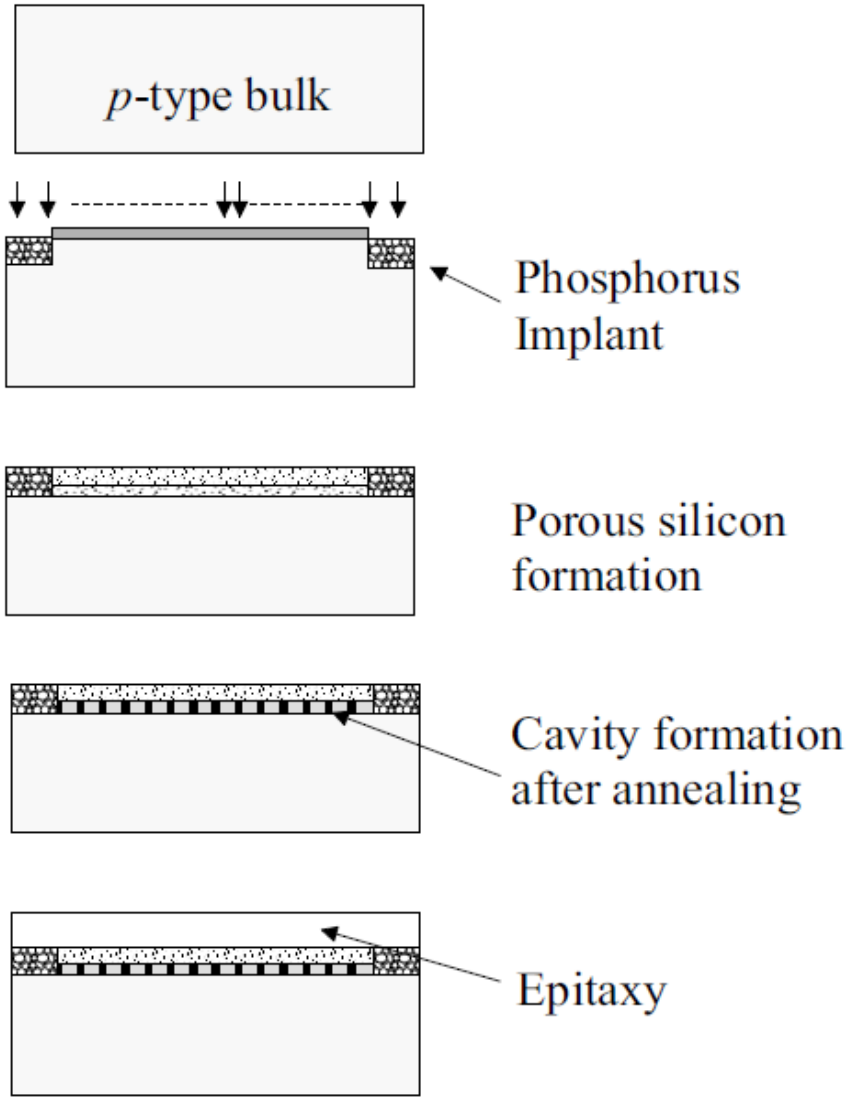
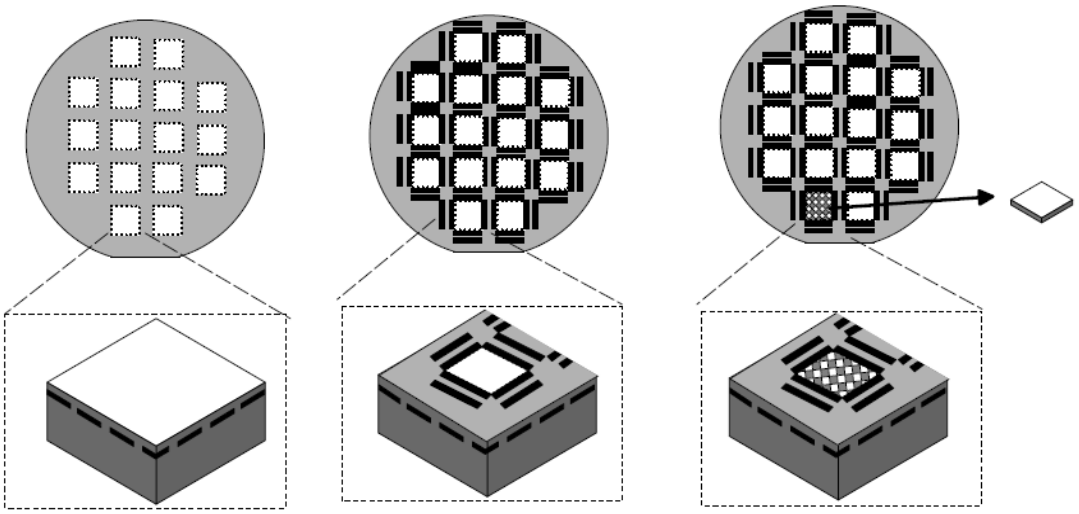


Figure 3.1 : Chipfilm™ process

The Pick, Crack&Place™ sequence is shown in figure 3.2. In figure 3.2a the white squares show the chips fabricated on the Chipfilm^{TM} wafer with cavities underneath the chips. The trenches etched along the sides of the chips are shown in figure 3.2b. In the last stage the chips needs to detached by using the Pick, Crack&Place™ process.



a b c

Figure 3.2: The Pick, Crack&Place™ process. a) buried cavities (shown in black) after the Chipfilm™ process, b) trench etching along the chip edges c) Chip detachment.

3.3 Piezoresistive effects

Ultra-thin transistors have to operate under bending stress in mechanically flexible systems. Physical bending introduces various stress inside the transistor structure, which alters their characteristics. The relation between externally applied stress and resulting strain is given by Hooke's law

$$\sigma = E \cdot \varepsilon \tag{3.1}$$

where

σ = externally applied uniaxial stress

E = Young's modulus (constant of proportionality)

ε = Strain induced

or for the case of uniaxial stress along x-direction

$$\sigma_x = E \cdot \varepsilon_x \tag{3.2}$$

A typical stress-strain curve is shown in figure 3.3

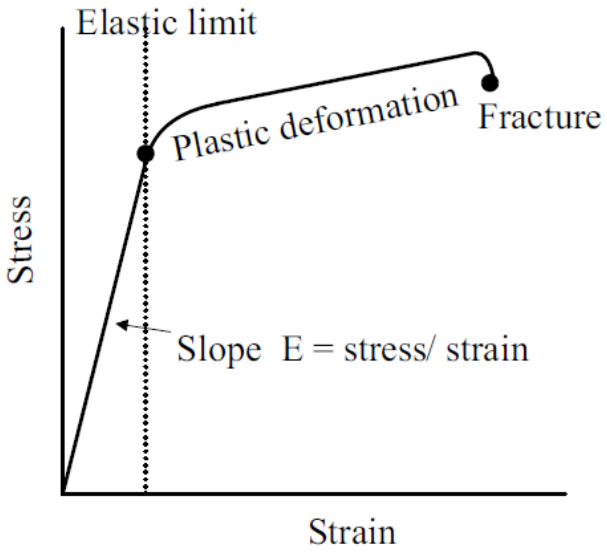


Figure 3.3: Typical stress-strain curve of materials.

Based upon the ability of materials to withstand the applied stress, they are divided into brittle and ductile materials. Silicon belongs to the groups of brittle materials which fracture shortly after passing through their elastic limit whereas ductile materials, like aluminium and copper, have a very large deformation phase prior to fracture.

Various materials exhibit a variation in resistivity under the influence of mechanical stress. The linear coupling between the mechanical stress and material resistivity is described by the piezoresistive effects. In silicon these effects were studied for the first time in 1954 [66]. Piezoresistive effects originate because of the re-population of charge carriers among valleys in energy bands under the influence of induced strain [67],[68]**.** For a rectangular bar, as shown in figure 3.4, the resistivity change is related to a resistance change as

$$\frac{d\rho}{\rho} = \frac{dR}{R} + \frac{dh}{h} + \frac{dw}{w} - \frac{dl}{l} \qquad (3.3)$$

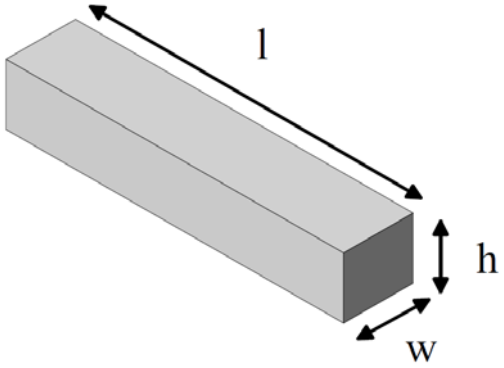


Figure 3.4 Dimensions of a rectangular bar.

For semiconductor materials, the geometric effects can be neglected as compared to piezoresistive effect [69], so that the change in resistivity is almost equal to the change in resistance of the specimen.

$$\frac{d\rho}{\rho} \cong \frac{dR}{R} \tag{3.4}$$

as the resistivity of the semiconductor material is given as

$$\rho = \frac{1}{q(n \cdot \mu_n + p \cdot \mu_p)}$$

Therefore, the change in resistivity means a change in carrier mobility, i.e.

$$\frac{d\rho}{\rho} \cong \frac{dR}{R} \cong -\frac{d\mu}{\mu} \tag{3.5}$$

The relation between the applied mechanical stress σ and the change in resistivity is given as [69]:

$$\frac{1}{\rho}\begin{pmatrix} d\rho_{xx} \\ d\rho_{yy} \\ d\rho_{zz} \\ d\rho_{xy} \\ d\rho_{xz} \\ d\rho_{yz} \end{pmatrix} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{xz} \\ \sigma_{yz} \end{pmatrix} \tag{3.6}$$

The π-matrix represents the piezoresistive coefficients, generally written as π_{ij}. The total number of coefficients is 36. However, because of the cubic symmetry of silicon, there are only 3 independent coefficients π_{11} , π_{12},, π_{44}. The sum and difference of π_{11} , π_{12} are represented as π_S , π_D.

$$\pi_S = \pi_{11} + \pi_{12} \tag{3.7}$$

$$\pi_D = \pi_{11} - \pi_{12} \tag{3.8}$$

In MOS transistors, the stress induced mobility variations directly influence the drain current i.e.

$$\frac{d\mu}{\mu} = \frac{dI_{ds}}{I_{ds}} \tag{3.9}$$

However, the piezoresistive effect in MOS transistors depends on channel orientation with respect to the crystallographic axis [70]. The mobility variation for the channel orientation along [110] and $[\bar{1}10]$ due to uniaxial stress applied parallel (longitudinal stress) and perpendicular (transverse stress) to the current flow in the channel is given as

$$\frac{d\mu}{\mu} = \pi_L \cdot \sigma \quad \text{(for [110] orientation)} \tag{3.10}$$

$$\frac{d\mu}{\mu} = \pi_T \cdot \sigma \quad \text{(for } [\bar{1}10] \text{ orientation)} \tag{3.11}$$

Here, π_L and π_T are the coefficients for longitudinal stress and transverse stress,

respectively. Their values can be determined from the slope of the relative changes in drain current or carrier mobility drawn *versus* stress, $\frac{d\mu}{\mu} or \frac{dI_{ds}}{I_{ds}}$, along [110] and [$\bar{1}$10] directions, respectively. The value of π_{44} is deduced from the relation

$$\pi_L \cdot \sigma = \left(\frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \right) = \left(\frac{\pi_S + \pi_{44}}{2} \right) \cdot \sigma \tag{3.11}$$

$$\pi_T \cdot \sigma = \left(\frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) = \left(\frac{\pi_S - \pi_{44}}{2} \right) \cdot \sigma \tag{3.12}$$

The values of piezoresistive coefficients depend upon the channel direction along a particular crystallographic axis, the direction of applied stress relative to the channel length, the temperature and impurity concentration [71],[72].

3.4 Characterization of ultra-thin chips

For the electrical characterization of chips under bending stress difference methods can be employed. The 3-point bending (3PB) and the 4-point bending (4PB) methods are generally employed for chips on wafer stripes, however, these methods only work well for silicon thicknesses > 150 µm [73]. The schematic of a 4PB system is shown in figure 3.5

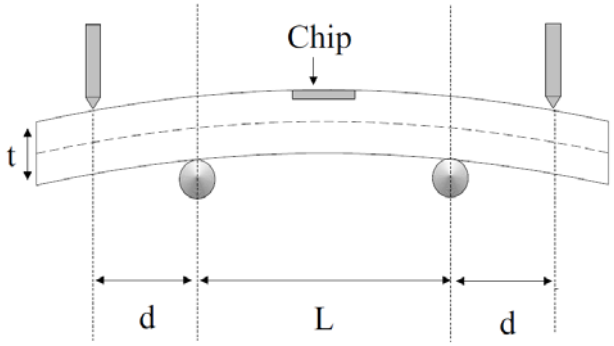


Figure 3.5: 4-point bending

In figure 3.5, the chip on a thick wafer stripe is placed on two cylindrical supports which are separated from each other by a distance L. The load is applied at the two ends of the wafer stripe which deforms the stripe into a curve. It is evident from the figure 3.5 that for ultra-thin chips on flexible substrates like polyimide foil, methods like 4-point bending are not able to produce bends in chips for characterization.

For chips having very small thicknesses (≤ 20 µm) innovative characterization techniques have to be employed. The ultra-thin chips need to be glued onto a flexible substrate, such as polyimide, that can easily be bend to the required smaller radii. Manual probing does not ensure reproducibility of the measurement, therefore, methods like wire bonding are required to establish reliable electrical connections from the device-under-test to analytic equipment. The schematic of such a system, which is readily available at IMS CHIPS, is shown in figure 3.6. In figure 3.6 the chip is glued onto a flexible substrate and the system is placed on a cylindrical surface with defined radius. Because the thickness of the system, including chip, glue and flexible substrate is of the order of a few tens of micrometers, therefore, the bending radius of the chip can be assumed as almost equal to the radius of the cylinder. Bending to radii smaller than 7 mm is possible with such a system [26].

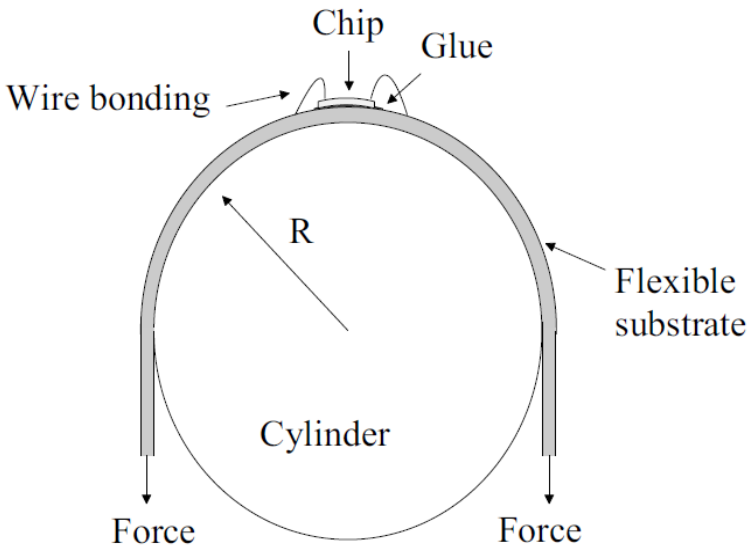


Figure 3.6 System for electrical characterization of ultra-thin chips under bend state.

The measuring system shown in figure 3.6 provides the reproducibility of data but the estimation of the exact stress on the chip surface is a complex task. The chip is glued onto the flexible substrate; the glue itself is a visco-elastic material. This makes the chip susceptible to stress relaxation especially when put under stress for a longer period of time. The issue becomes more problematic when the temperature of the chip increases due to self-heating.

3.5 Thermal issues for high-voltage ultra-thin chips on flex.

High-voltage ultra-thin chips can operate at several tens of volts. As a result, a certain amount of power is dissipated on the chip. This power dissipation generates heat in the chip that is difficult to transfer from the chip via the flexible substrate to a heat sink. As a result of heating the chip temperature increases and, hence, affects the device characteristics.

This heat transfer process follows a thermal path from the device to the ambient. The resistance of this thermal path is called thermal resistance (R_{th}) as shown in figure 3.7. The thermal resistance is given as

$$Rth = \frac{Tj - Ta}{P} \tag{3.13}$$

or

$$Rth = \frac{\Delta T}{P} \tag{3.14}$$

where

Tj = Junction temperature

Ta = Ambient temperature

P = Power dissipation in junction/channel

$\Delta T = Tj - Ta$

The unit of thermal resistance is K/W

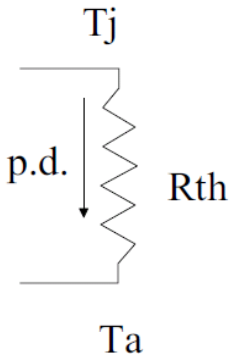


Figure 3.7: Thermal resistance.

The thermal resistance of a slab of material, shown in figure 3.8, with width (W), length (L), thickness (T) and thermal conductivity (σ) is given by..

$$Rth = \frac{T}{\sigma . A} \qquad (3.15)$$

where

A = area of the slab perpendicular to direction of heat flow (Lx W).

By using the above equations one can calculate the temperature rise at the junction with respect to the ambient for a certain power level.

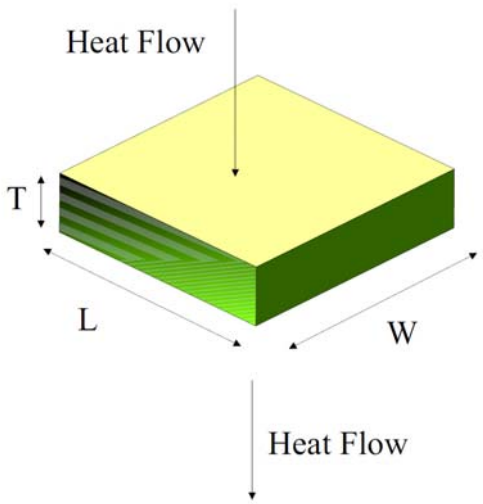


Figure 3.8: Heat flow through a slab of a material. Thermal resistance depends upon area (A), thickness T and thermal conductivity (σ).

For a multi-layer system, the total thermal resistance is determined by adding the thermal resistance of all layers in the path from junction to the ambient as shown in figure 3.9.

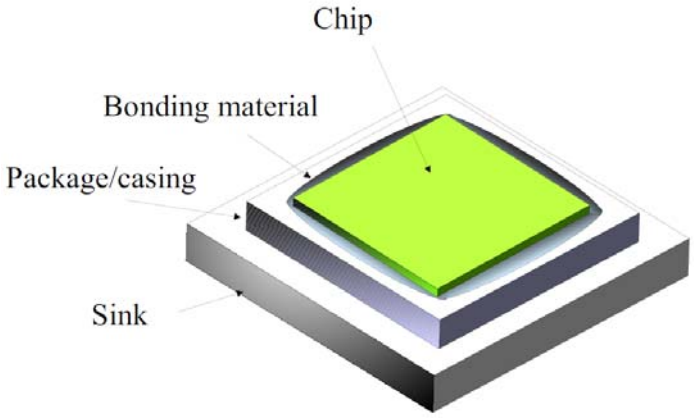


Figure 3.9: A Multi-layer system. Total thermal resistance is the sum of the thermal resistances of all individual layers

For example, in chip packaging, the chip substrate is attached to the package through some bonding material. (The package itself is attached to some heat sink as shown in figure 3.9). So, in this system, the thermal resistance is given by:

$$R_{th} = R_{th\ chip} + R_{th\ bonding} + R_{th\ Casing} \quad (3.16)$$

The unit of thermal conductivity of a material is W/mK. In case of heat dissipation from a surface to the ambient (e.g. air cooling), the unit for thermal conductivity per unit area is W/m^2K. The power dissipation in the junction/channel region is given as

$$P = hA\Delta T \quad (3.17)$$

where

h = thermal transfer coefficient in W/m^2 K

A = Surface area of material (heat sink)

or

$$\frac{1}{h} = \frac{A\Delta T}{P} = R_{th} \tag{3.18}$$

In flexible displays the issue of heat extraction from ultra-thin chips becomes worsened. Rigid heat sinks can no longer be applied as they reduce the mechanical flexibility of the system. Ultra-thin substrates (thickness < 20 μm) feature a small material cross section and, thus, are prone to self-heating. Moreover, the ultra-thin chip has to be embedded in a flexible sheet or has to be sandwiched between two flexible sheet layers, shown in figure 3.10. This arrangement of layers covers the chip from all sides.

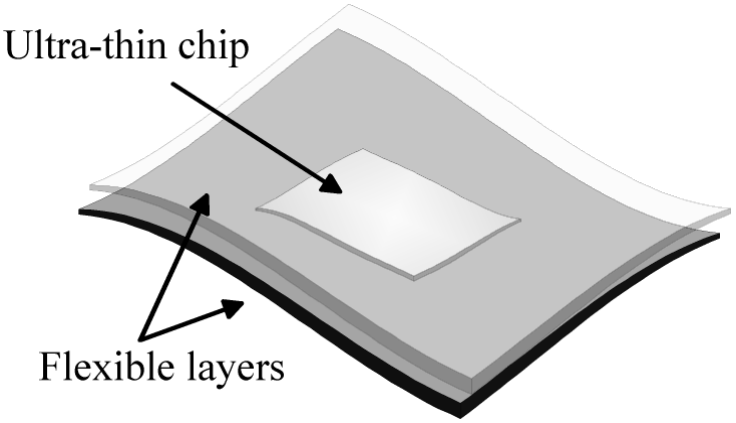


Figure 3.10: Chip sandwiched between two flexible layers.

The conductivity of the sheet also plays a vital role in temperature distribution for a given dissipated power [74]. In most cases, a polymer material is used as flexible sheet. The polymer being a thermal insulator hinders the flow of heat from junction to ambient and, thus, causes the junction temperature to rise. These physical boundary conditions cause all the heat, generated as a result of electrical power dissipation, to largely remain on the chip. As a result the temperature at the junction and channel of the transistors rises considerably above ambient temperature level. The rise in chip temperature deteriorates the device performance and can also lead to device failure.

The dc power dissipation in a MOS transistor is given by

$$P_{dc} = I_{ds} V_{ds} \tag{3.19}$$

or

$$P_{dc} = I_{ds}^2 R_{on} \tag{3.20}$$

Therefore, in order to reduce the power dissipation in device and to keep the junction temperature within desirable limits small channel and drift lengths and high doping densities should be used. Of course, in order to achieve high breakdown voltages, one cannot reduce the channel and drift length below certain values and also cannot make the doping density overly high. Therefore, a compromise has to lead to an optimum device design.

4 Flexible display driver chips

This chapter is an expanded version of the article published in the reference book "Ultra-thin chips technology and applications". The article is written by the author during his Ph.D. research. It explains the scenario and challenges that ultra-thin driver chips have to cope with on flexible substrates.

In the past few years, the focus of the electronic display industry has been shifted more to the viable and dynamic flexible display technology. Flexible displays are supposed to be thin and sturdy along with modifiable shapes and sizes. Flexible displays can broadly be categorized in terms of their degree of freedom in flexibility. There are one time flexible, semi-flexible and full flexible displays. One-time flexible displays are curved or conformed at the time of manufacturing and retain their shape afterwards. Semi-flexible displays can only be partially bend, rolled or folded. Full flexible displays can be rolled, folded, bent and/or stretched from any direction and as many times as possible without breakage [75]-[77].

4.1 Flat panel display structure

A typical flat-panel flexible display comprises of a substrate, a layer of electrode stripes or electronic circuitry (known as backplane), functional display material and an encapsulation layer (known as frontplane), as shown in figure 4.1. In addition to this fundamental layer structure, coatings of thin films and a sealing are employed to enhance the device performance and reliability [78].

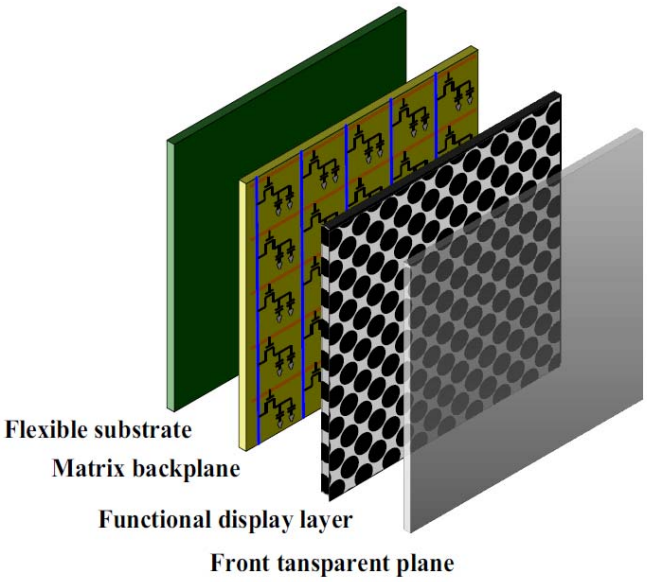


Figure 4.1: Layer arrangement in a typical flexible flat panel display.

A flexible substrate is supposed to be robust while featuring good thermal, optical and chemical properties. Compatibility with other layers and feasibility for roll-to-roll manufacturing also plays a vital role in making a choice between various suitable materials. Materials like flexible glass and metal sheets, Polyimide (PI), Polyethylene Terephthalate (PET) and Polyethersulphone (PES) have shown promising results so far but none of them can yet be considered to be colloquial [76].

The role of a functional display material is to reflect or transmit light according to an input signal. The input signal is applied in the form of bias levels within a matrix across the material. There are a number of technologies available for making functional display layer, such as electrophoretic, cholesteric liquid crystal, electro wetting, electro chromic and organic light emitting diode (OLED). In an electrophoretic display, small charged particles are confined in fluid. They move in fluid under the influence of external applied electric field as shown in figure 4.2. Together they form a visible image while dissipating very little power.

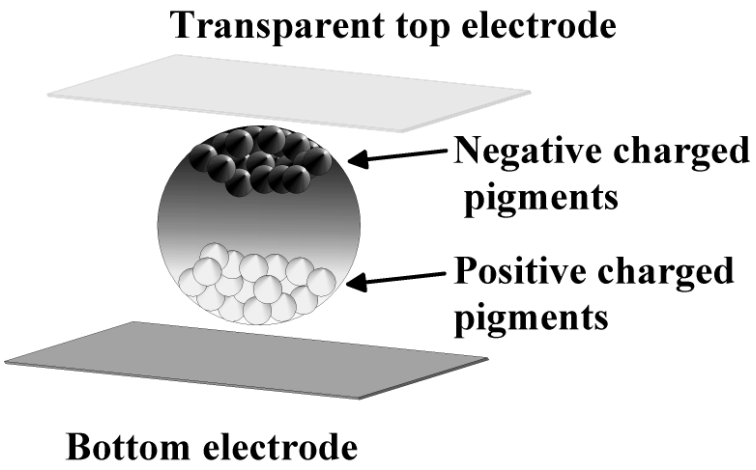


Figure 4.2: Electrophoretic system

Figure 4.3 shows the working scheme of an electro-wetting display. Electro wetting displays make use of a variation in surface tension of a liquid with an applied voltage. The eletro-wetting system comprises of a hydrophobic dielectric (insulator), oil and electrolyte (e.g. water).

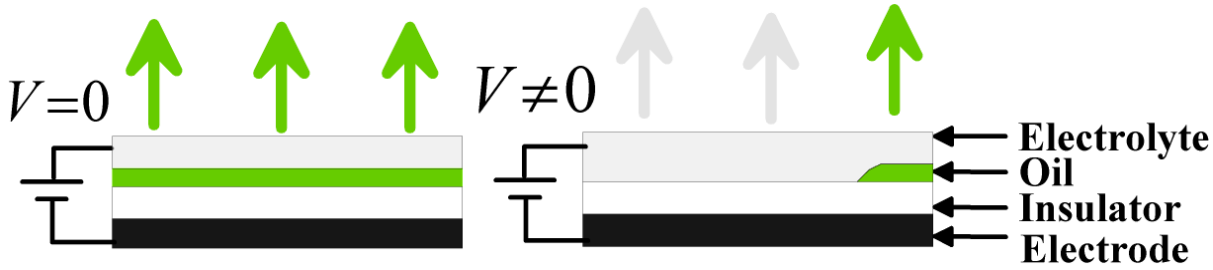


Figure 4.3: Electro wetting scheme

Under zero bias, coloured oil spreads over the dielectric and separates the water and dielectric surfaces. Because the dielectric film is covered by coloured oil, a coloured pixel is visible from the frontside. When voltage is applied, the surface tension of water changes and displaces the oil. When oil is displaced the colour of the dielectric (say white) appears. The advantage of the electro-wetting technique is its fast switching speed which enables it to display video streaming.

In electro-chromic technology, by passing current through the material, the colour of the material changes due to oxidation and reduction phenomena. The electro-chromic material is placed in between two transparent conducting oxides (TCOs) as shown in figure 4.4.

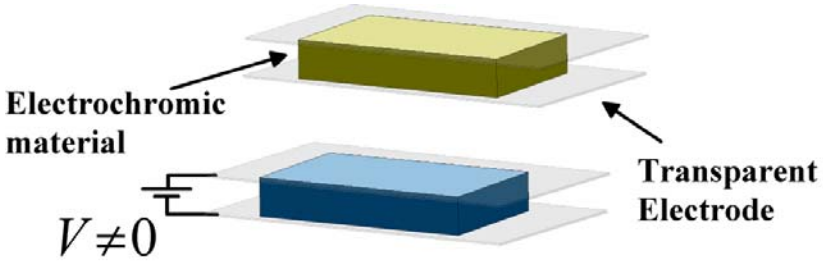


Figure 4.4: Electro-chromic technique

Transparent conducting oxides (TCO) are doped metal oxides. Usually, they are formed by combining *n*-type semiconductors and metal oxides. Preparation of TCO can also be achieved by using *p*-type material [79]. This material can transmit light and be conductive. Due to the optical and electrical properties, it is used at the front-plane of a flat panel display. As a front layer, it does not only provide encapsulation but also serves as a common electrode. Indium tin oxide (ITO) is used in many displays. However, due to a limited availability of Indium investigations on other competitive TCOs have been going on for the past several years. For practical purposes, the resistivity of TCO should be less than 10^{-3} Ω-cm and transmittance level should stay above 80% on average [80]**.** Other examples of TCOs include ZnO and SnO_2.

4.2 Matrix backplane addressing methods

Flat panel displays contain a number of picture elements (pixels) organized in a matrix form, as shown in figure 4.5. All pixels in a row are connected together via a row electrode (row line) and all pixels in a column are connected with each other through column electrodes (column line).

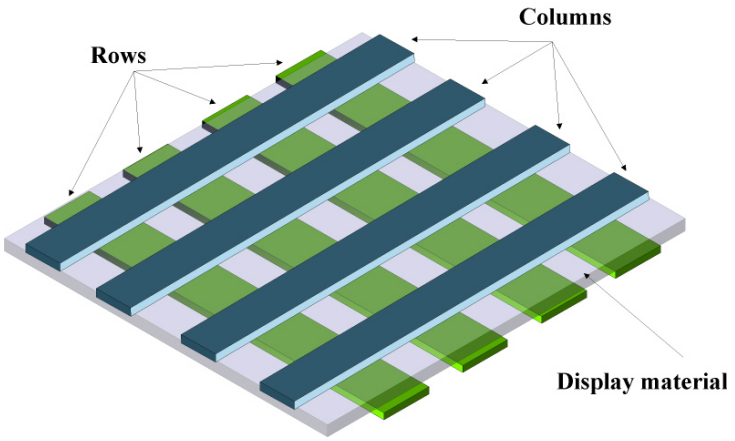


Figure 4.5: Matrix backplane scheme

This arrangement of pixels in matrix form makes it possible to address each pixel individually. The row and column lines are set perpendicular to each other. The overlap or intersection areas of rows and columns define a pixel and thus assign a unique address to each pixel. Depending upon the type of driving electronics of these pixels, addressing methods of matrix backplanes are categorized as

1. Passive addressing;
2. Active addressing.

In passive matrix addressing, voltages across pixels are directly provided by row and column electrodes. In order to achieve this, transparent conducting electrodes, e.g. ITO, are patterned at front- and backplanes in form of rows and columns. The display material structure is sandwiched in between those two layers, as shown in figure 4.6. For M rows and N columns (M x N pixels), M + N external connections are needed between matrix backplane and matrix drivers [81]. The advantage of the passive matrix technique is its simplicity in design and the low cost. However, it exhibits problems like cross-talk, large RC delays and high power dissipation. The problems become particularly severe in large size display. Therefore the passive matrix scheme is usually employed in systems having a small display size, low resolution and slow refreshing rates.

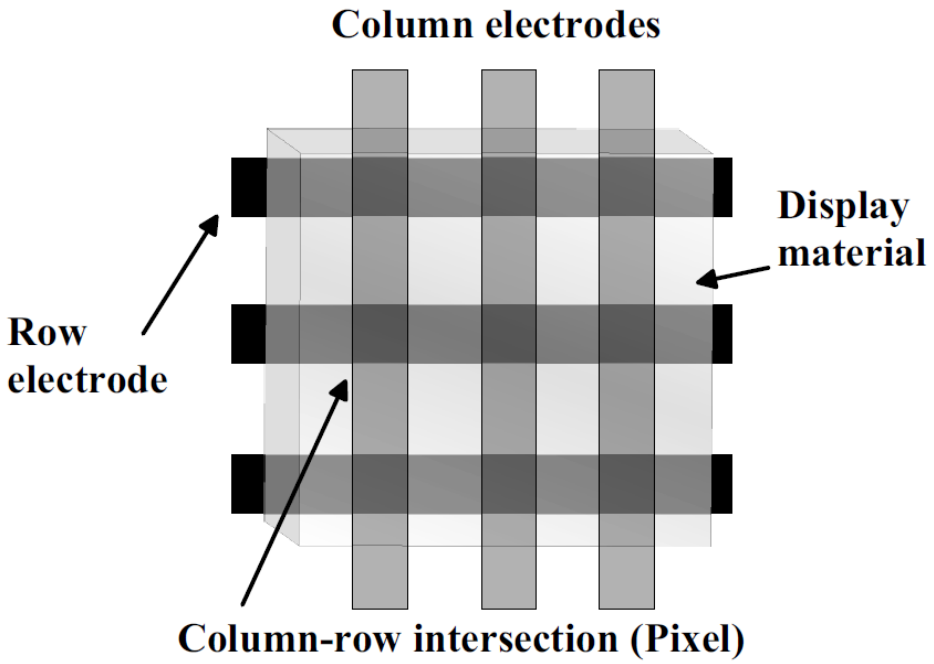
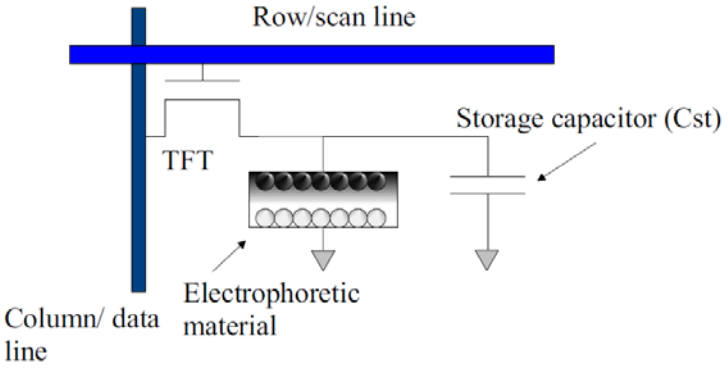
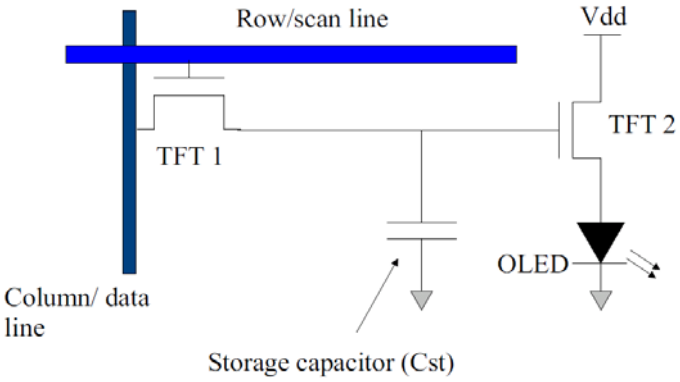


Figure 4.6: Passive matrix

In the active matrix technique, TFT switches are used to pass signals to the pixels according to the requirement. TFTs based circuits are connected with each pixel. A pixel circuit can contain one or more TFTs. For example, in an electrophoretic display a 1-TFT pixel circuit provides sufficiently good results. However, in OLED displays at least a 2-TFT pixel circuit is needed. These pixel circuits are illustrated in figure 4.7. In order to minimize effects of a leakage current, a storage capacitor is employed in every pixel circuit. Both row and column lines are patterned in the backplane whereas the front-plane acts as a common electrode. Row lines are connected to the gates of the TFTs and column lines are connected to the source terminals of the TFTs. Whenever an appropriate voltage is provided on row lines, all the TFTs in that row become activated. The column lines are then used to transfer the signal data via the source terminals of the TFTs to the pixels. In this way all pixels in a row acquire their signal data simultaneously. The active matrix addressing technique is employed because of the higher refreshing capabilities, better control of applied bias, reduced crosstalk and low flickering issues.



(a)



(b)

Figure. 4.7: A simple pixel circuit for (a) electrophoretic (b) OLED display.

4.3 Display drivers

In matrix addressing techniques, two types of driver circuits (row driver and column driver) are required for proper addressing and data loading through pixel circuits, as shown in figure 4.8. Generally, these drivers are placed outside the display area, on a rigid part of the substrate. Tape automated bonding (TAB) is used to connect the drivers to the matrix backplane.

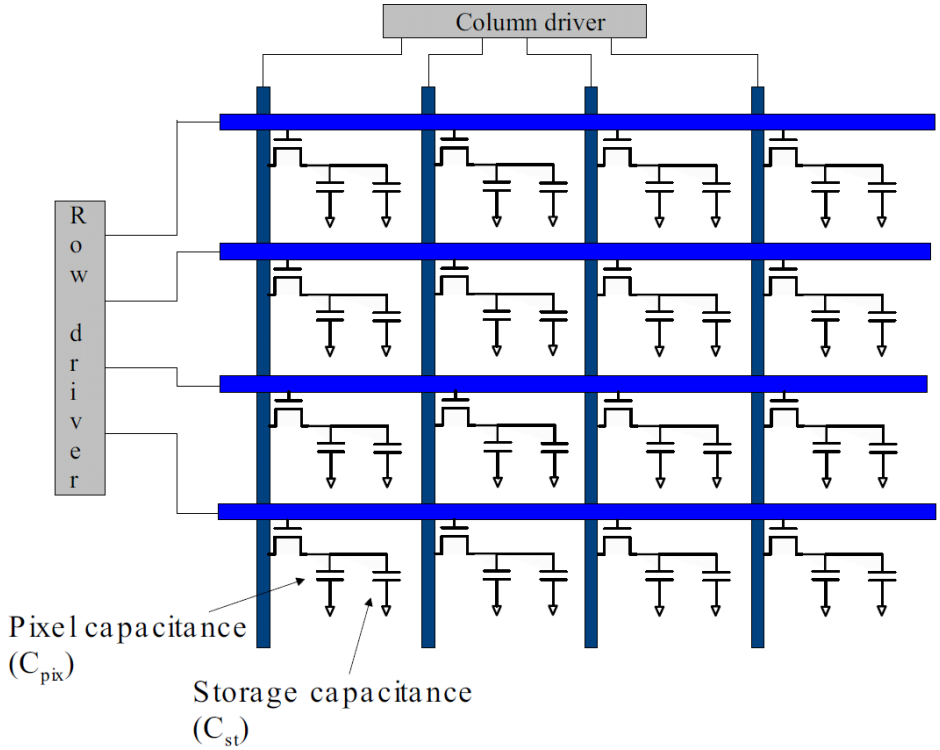


Figure 4.8: 4x4 active matrix backplane with row and column drivers.

4.3.1 Row drivers

The row drivers provide sequential outputs in form of voltage pulses. These sequential voltage pulses are used to activate or de-activate rows in the matrix backplane. The number of rows and columns together defines the matrix frame. For N-rows, N pulses are required, which are provided by a row driver circuit with N-buffers. The pulse frequency is given as $1/T_f$, where T_f is the frame refreshing time period [82].

The clock frequency required for a row driver is only few tens of kilo Hertz. It is determined by the product of number of rows and the refreshing rate [81]. The time available for pixels in a row (T_{row}) to activation, data loading and deactivation is given by:

$$T_{row} = \frac{1}{frame\ frequency} \times \frac{1}{number\ of\ rows} \qquad (4.1)$$

Therefore, with an increase in frame frequency and/or number of rows, the time available for one row reduces. Figure 4.9 shows the dependence of row time on frequency for different display resolutions.

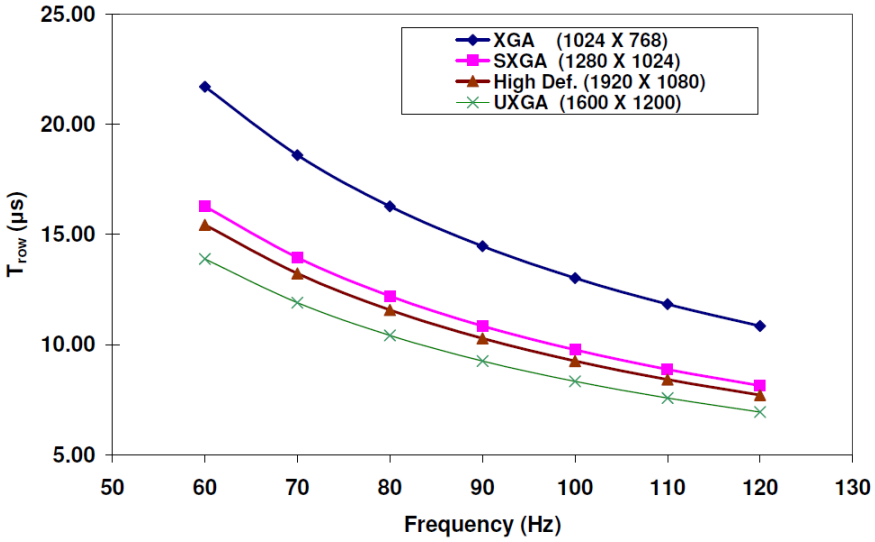


Figure 4.9: Dependence of T_{row} on frame frequency for various video formats.

The design of a typical row driver includes shift register, level shifter and output buffers stages, as shown in figure 4.10. The shift register stage generates pulses with a frequency determined by the row time. The level shifter stage then shifts the minimum and maximum levels of these pulses up to the ON and OFF requirements of the TFT gates in matrix backplanes, e.g. from 0 and 3.3 to -5 volts and 20-25 volts respectively [81] or as required by the display technology. The output buffer stage is then employed for the purpose of impedance matching and for supplying pulses to the rows in the matrix backplane.

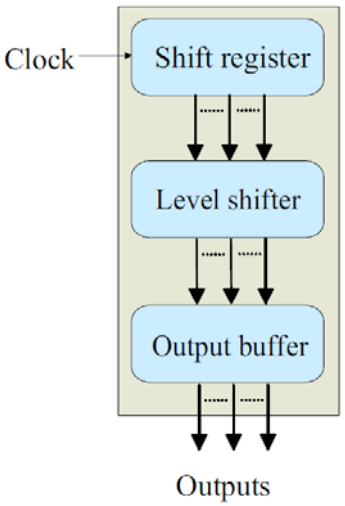


Figure 4.10: Row driver

4.3.2 Column drivers

The design of column drivers is relatively more complex than that of row drivers. The complexity arises due the requirement of relatively high analog voltages (several tens of volts) at the source terminals of TFTs in matrix backplane.

A typical design of a column driver includes shift register, latch, level-shifter D/A converter and output buffer stage. A column driver receives a digital low-voltage input serially. The data is then transferred to a level-shifter stage, which raises the voltage levels and passes it on to the D/A converters. After the conversion from digital to analog, the data arrives at the output terminals via output buffers. The data is applied to all columns in an active row simultaneously.

Figure 4.11 shows the internal structure of a typical column driver for a monochrome display. The number of data outputs becomes 3-fold in case of a full colour display to represent RGB.

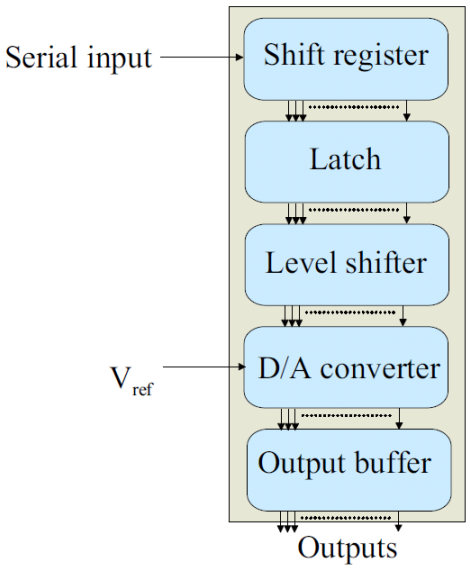


Figure 4.11: Simplified form of typical architecture of columns driver for monochrome display.

In column drivers, the minimum clock frequency limit for shift registers is determined by the product of pixel count and refresh rate [81]. The required frequency varies with colour depth and number of drivers. For example, in a high-definition colour display (1920·3· 1080) backplane matrix with 24-bit colours and 60 Hz refresh rate, the column

drivers have to operate at a frequency higher than 373 MHz. This high frequency requirement can be reduced by using more than one column driver, e.g. 8 column drivers with 720 channels each. In the parallel operation mode, the frequency requirement for these 8 column drivers would then be reduced to 47 MHz.

4.4 Ultra-thin drivers

Realization of a full flexible, paper-like display demands embedding of ultra-thin driver chips onto the same flexible substrate. Integration of such thin chips on flexible substrates reduces not only the number of external connections but also the cost of the product. It also helps increasing the reliability of the system, particularly in rugged environments.

Development of ultra-thin driver chips, which are flexible and, thus, compatible with flexible substrates, is cumbersome. Plastic substrates cannot withstand high processing temperatures. They also posses a lower dimensional stability compared to rigid substrates. Therefore modifications in conventional fabrication processes for devices on rigid substrates are required.

Two approaches have been widely adopted by researchers to deal with this issue. One is the fabrication of low-temperature processed TFTs directly on plastic substrates. The other is to transfer pre-fabricated devices onto plastic substrates. The former approach targets amorphous silicon, low-temperature polysilicon (LTPS) and organic semiconductors (OTFT), whereas the latter deals with high-temperature processed polysilicon or single-crystal silicon TFTs. Decrease in processing temperatures typically results in a low carrier mobility in the semiconducting material. Therefore, from the direct fabrication approach high performance circuits on plastic substrates cannot be expected. On the other hand, high-mobility transistors are indispensible especially in driver circuits to reach the high refreshing-rates required in video streaming. Also, significant degradation occurs in TFT on flexible substrates due to threshold voltage shift and self-heating.

Hydrogenated amorphous silicon (a-Si:H) TFTs require low processing temperatures, which makes them suitable for direct fabrication on flexible substrates. The a-Si:H TFT based drivers on flexible substrates [83],[84] perform well at low refreshing rates (up to

few tens of hertz) or for occasional image refreshing applications. However, because of low carrier mobility values (~0.1 – 1 cm^2/V-s) they are not well suitable to cope with video signal refreshing requirements. Integration of both source and row drivers reduces the total number of external interconnects significantly, as reported in [83] where for a QVGA display the total number of interconnects was reduced from 560 to 76 i.e. by a factor of 7.4.

Hydrogenated amorphous silicon (a-Si:H) based circuits face severe performance degradation due to their threshold voltage instability. This instability is attributed to charge injection or charge trapping in the gate dielectric and defect formation in the channel region in case of amorphous silicon [85]. The contribution of the two mechanisms is a function of the applied voltage stress, where defect formation in a-Si dominates at low applied voltage and charge trapping in the gate insulator dominates at high applied voltage stress. The shift in threshold voltage affects the column biases, where a 30 V signal can be decreased by 10% within only 3 hours [86]. The effects of threshold voltage shift can be minimized through improved circuit design and appropriate drive signal timings.

Table (4.1) Grain sizes and mobility value range for different silicon types.

Silicon type	Grain size	Mobility in transistor channel	
		Holes	Electrons
		cm^2/Vs	cm^2/Vs
Amorphous	< 1 nm	~0.01	~0.1-1
Nanocrystalline	~ 10 nm	~0.2	~40
Microcrystalline	~ 0.1 – 100 μm	~50	~300
Large-grained poly	~ 0.1 – 10 mm	~200	~350
Single-Crystal	-	~250	~600

Polycrystalline silicon TFTs show mobility values much higher than amorphous silicon TFTs. High temperature (>600 ^{O}C) processed polysilicon TFTs have better electrical performance than a low temperature processed polysilicon (LTPS) TFT, but such high processing temperatures make them unsuitable for direct fabrication on flexible plastic substrates. However, they can be fabricated on flexible metal sheets which can withstand temperatures as high as 1000 ^{O}C. On flexible metal substrates these devices can provide mobility values upto 300 cm^2/Vs for nmos and 150 cm^2/Vs for pmos TFT [87]. With such high field-effect mobility, poly-Si TFT drivers can easily satisfy video signal processing. For having driver circuits on plastic substrates, pre-processed low temperature polysilicon TFTs can be transferred onto flexible plastic substrates without exhibiting significant performance degradation [88]. On plastic substrates, the achieved carrier mobility values are, however, much lower than on metal substrates [87]. With continuous research to decrease the processing temperatures, low temperature polysilicon TFTs with a carrier mobility of ~ 50 cm^2/Vs can directly be fabricated on plastic substrates having a relatively high glass transition temperature, such as polyimide (T_g > 350^{O}C) [19].

Organic TFTs offer the advantage of low processing temperatures and compatibility with roll-to-roll printing technique. These properties permit direct fabrication of organic TFTs on all types of flexible substrates. Possibilities of designing row drivers by using organic TFTs have been presented [89]. The performance is, however, limited to low resolution and small display sizes. This is mainly due to very low mobility values of organic transistors which are in the range of 1 cm^2/Vs for *p*-type and 0.2 cm^2/Vs for *n*-type TFTs. Recently, mobility values up to 5 cm^2/Vs in solution-processed organic TFTs have been reported [90]. This mobility value exceeds that of amorphous silicon TFTs and is also compatible with low-cost mass-production printing techniques. The mobility values of organic semiconductors are a matter of internal order, defect density and interface properties. In case of pentacene, the various processing techniques yield different mobility values that range from 1.8 cm^2/Vs for solution processed pentacene to 40 cm^2/Vs for single-crystal pentacene [91].

With respect to complementary circuit design, organic TFT technology is limited by the low carrier mobility level of the *n*-type organic TFTs, which are far less than those of *p*-type TFTs. This trend is opposite to the well-known difference of the carrier mobilities in silicon. Furthermore, in ambient environment, *n*-type organic materials exhibit a

very poor stability. These two factors suggest a different circuit design approach for organic TFTs based circuits. A PMOS-only or pseudo-PMOS approach can circumvent the limitations set by *n*-type TFTs. It has been shown that by employing a PMOS-only approach, the overall circuit performance can be improved 2–4 fold as compared to a CMOS arrangement of organic TFTs [92]. However, in integrated source drivers, CMOS dissipates 50 times less power than the *p*-type only TFTs [93]. Another approach to make use of a complementary scheme with organic TFTS is the hybrid CMOS device approach [93]-[95]. The hybrid CMOS technique makes use of *p*-type organic TFTs and *n*-type inorganic TFTs to form a complementary circuit. The hybrid CMOS approach has shown satisfactory performance and stability on flexible plastic substrates though at the cost of an enormous processing effort.

The well established single crystal silicon technology was previously assumed to be incompatible with plastic substrates because of the high processing temperatures. With the development of transfer techniques pre-fabricated single crystal silicon devices can be brought onto flexible substrates [20],[96], so that single crystal silicon technology has now found its scope in the field of flexible displays. For this, ultra-thin silicon chips are required to maintain the degree of flexibility of the final product after embedment. For reducing the thickness to ≤ 20µm, the conventional backside grinding technique is not well suitable as it can produce a non-uniform and poorly reproducible thicknesses as well as defects. Also the handling of ultra-thin wafer, which is necessary to receive the ultra-thin chips, is a difficult task. Fortunately, techniques like Chipfilm^{TM} [97] feature characteristics that make them particularly suitable for an application in flexible displays.

With the help of single crystal silicon technology high speed transistors with carrier mobility > 500 cm^2/Vs and an on/off ratio $>10^5$ can be obtained [98]. For column drivers, in the level shifter stage, high-voltage transistors are required to shift the bias up to the high supply voltage level. The conventional high-voltage design for LDMOS transistors relies on deep wells along with RESURF techniques to switch at the required high voltages. The depth of the well, usually few tens of microns, puts a limit on the reduction of the chip thickness. This points to the need to modify the LDMOS transistor design towards ant ultra-thin structure so that it can be embedded into flexible substrates without any compromise in the flexibility of the product. A few attempts have been made in this regard so far. In such an attempt an ultra-thin (35 µm) high-voltage

transistor design was reported in [99]. The breakdown voltage of the transistor was >110V [27]. At high-voltages, significant reduction in the current occurs due to self-heating. However, for switching purposes, this reduction in current is tolerable in the application. In another design of an ultra-thin (~ 10 μm) LDMOS transistor based on Chipfilm™ technology the transistor can withstand a high-voltage of about 100 V [100]. The characteristics of a single-crystal silicon transistor under bending stress have also been studied by [27],[101]. The results showed that under bending stress, the drain current changes due to the piezoresistive effect. For switching purpose these effects do not impact the device performance significantly. However, in analog circuits these effects must accurately be taken into consideration.

4.5 Design challenges

The conventional scheme of a matrix drive, i.e. active or passive with line by line scanning, works well for small sized displays and low resolutions. This is due to availability of sufficient row time to properly charge the pixels in a row. But with the increase in resolution and display sizes, the row time decreases significantly. In this scenario, a conventional line by line scan technique can no longer be used for proper charging of pixels. Two limiting factors must be taken into consideration in driver designs.

1. Row time constraint;
2. Signal delay.

4.5.1 Row-time constraint

A pixel behaves like a capacitance that has to be charged and discharged according to the input data. The charging and discharging time of a pixel depends largely upon the response time of display material. The higher the resolution is, the shorter is the row time available for pixel charging. This leads to insufficient pixel-charging, resulting in poor picture quality and uniformity. It has been shown that a multi-line scanning technique can be used to increase the effective row time. In [102] a dual-line driving

method has been employed to drive 23-in UXGA TFT-LCD. At 80 Hz the required scan time is calculated to be 10 μs. With dual-line scan technique, a pre-charge phase and a fine tune phase is utilized to achieve a scan period of 6 μs, as shown in figure 4.12. The minimum time that can be achieved using the conventional line by line scan is 12 μs at best.

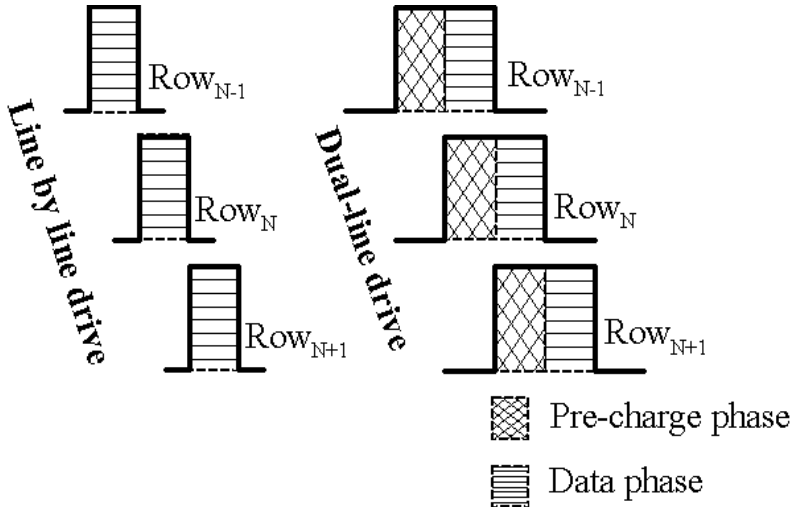


Figure 4.12: Comparison between line-by-line and dual line scan method. Pulse width shows the time available for each row in both cases.

The effectiveness of the simultaneous scanning technique for multi-lines has also been reported [103],[104]. Here, a line-time extension (LiTEX) was applied to increase the effective row-line time for a given resolution. The LiTEX method works by scanning a group of two rows simultaneously in contrast to row by row scanning. Both rows in a group turn ON simultaneously but turn OFF at different times, thus allowing a precharge time for one of the rows. The LiTEX method is based on 1-horizontal 2-vertical (1H2V) inversion instead of dot inversion. The number of lines in a simultaneous scan can be increased as reported in [105]. Here a group of 3 adjacent rows have been scanned simultaneously during the pre-charging phase. After pre-charging the fine tune voltage is generated by comparing data of the 3 rows.

4.5.2 Signal delay

In large displays, row and data lines show behaviour like a distributed resistance-capacitance (RC) network, as shown in figure 4.13. This introduces a delay in signal while travelling away from the terminal where the driver is connected. Figure 4.13 shows the equivalent RC network for a row line. Each RC unit represents the load offered by a pixel. A network of N resistances and N capacitances represents N pixels per row. The value of each resistance is R/N and each capacitance amounts to C/N. In such a network the rise and fall times of gate pulse are increased considerably at the end of row line.

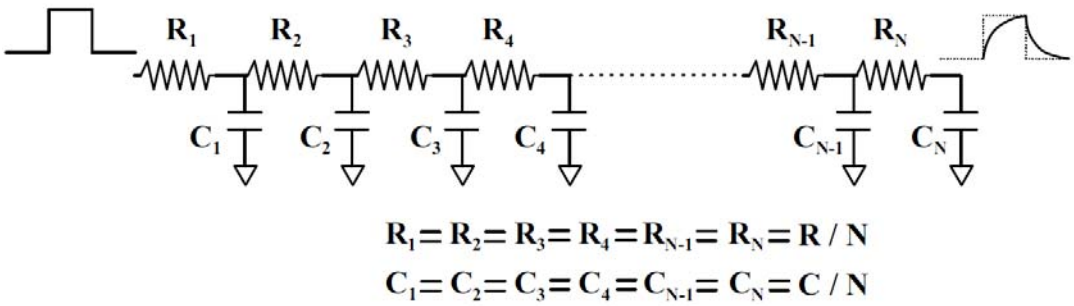


Figure 4.13: RC network

Methods like horizontal line delay compensation (H-LDC) [106] can be adopted, which allows data to arrive on column lines in a progressive fashion. This is achieved by making the outputs of the data driver to follow the propagating edge of select signal. This method provides longer charge/discharge time for pixels. Adaptive charging methods [107] can also be used to reduce the charging time of pixels and, hence, can provide delay compensation. A data bus at the backside of the substrate, connected through via holes to the gate lines, can be utilized to reduce the resistance of the signal path. It has been claimed [108] that a few via holes per line can result in a delay reduction by a factor of 10. Besides modification in signal provision techniques, signal delay time can be reduced significantly by applying the drive signals from both sides of rows and columns. For this the frame is divided into two halves, vertically, horizontally or both. By sub-dividing the frame, the row-line time increases. However, this method

requires additional drivers which, in turn, lift the price of the product. The number of row and column drivers can, however, be reduced by sharing row and column lines [109], thus reducing cost Figure 4.14 shows the various possibilities for driver chip placement on the matrix backplane.

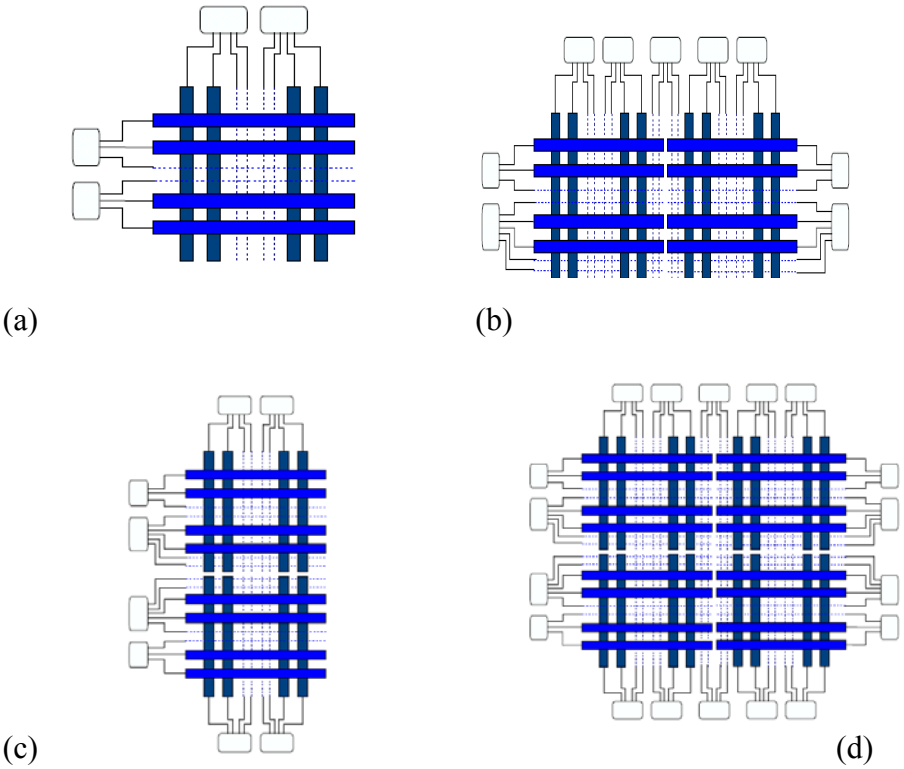


Figure 4.14: Placement of drivers around matrix backplane. (a) Typical placement scheme for normal resolution and small display sizes, (b), (c) and (d) various possibilities of dual scan method for high resolution and large display sizes.

4.5.3 Operating temperatures

The temperature of the environment in which the driver chips have to operate is always higher than the ambient temperature. Because of power dissipation in pixels, rows, columns and supply lines, for a large size active-matrix OLED display the power dissipation can raise the temperature up to 25 ^{O}C for 24-inch and up to 28 ^{O}C for 40-

inch diagonal display [110] above ambient temperature. Therefore, a reduction of the power dissipation in flexible display driver circuits is a necessity for maintaining the required performance and reliability of the display system. Minimization of the on-resistance of the transistors can be achieved by improving the device structure design. Pixel circuit design techniques like charge recycling [111] and methods of selective updates of pixels [112] can be adopted to further reduce the power dissipation.

Advancement in flexible display technology has opened the doors to many new applications which were previously thought to be infeasible. Small size flexible displays have already been announced and the true emergence of that promising technology is yet to come. Success in developing flexible displays as large as A3 sized newspaper has also been claimed recently [113]. Besides making displays only for viewing purposes, the concept of smart windows for energy-efficient homes and smart textiles have also been addressed in literature. The purpose of a smart window is to block and transmit the infrared portion of the sunlight according to the need [114]**.** In addition to that it can also be used as a large screen display for the use in applications like home theaters. Similarly, smart textiles are meant to display, communicate and perform thermal body management. All this and many other such applications demand an autonomous and multipurpose flexible system, which can not only be used for displays but also be able to transmit, receive, store and process data. All this can be achieved by having thin and flexible batteries, memories, transceivers, logical and driver circuitry on the same flexible substrate. There are a number of technical [115] and technological [5] obstacles to overcome before realizing mass production of fully flexible and autonomous display systems.

5 Process simulation and fabrication of ultra-thin high-voltage LDMOS transistor

In this chapter the process simulation and fabrication issues of the ultra-thin high-voltage LDMOS transistors are explained. The process is developed in order to achieve a breakdown voltage >100 V while using 20 µm thin silicon chips. The process is made fully compatible with that of a conventional LDMOS transistor on thick substrates in order to keep the number of masks and, hence, the cost same.

5.1 Process simulation

Two-dimensional device structures are simulated and optimized through the device process simulator Athena of Silvaco. The performance of these device structures are determined by simulating their electrical characteristics using Atlas of Silvaco.

The simulations are based on the following process flow: processing starts by initializing a 2 µm p^+ layer of silicon with a Boron concentration of $5 \cdot 10^{18}$ cm^{-3}. This p^+ layer is used to simulate the effect of a 1–2 µm p^+ layer in real Chipfilm™ wafers on which an epitaxial layer is grown for the purpose of device fabrication. The process flow for LDMOS on a Chipfilm™ wafer compared to that on a bulk wafer is shown in figure 5.1. Except for wafer pre-processing the process flow is the same for both cases.

A 16 µm *p*-type epitaxial layer is grown over this 2 µm p^+ layer of silicon. The concentration of Boron in the *p*-type epitaxial layer is $1 \cdot 10^{15}$ cm^{-3}. A 15 nm oxide layer is grown using the dry oxidation method for *n*-well and *n*-drift implant. The *n*-well/drift implant is performed using a Phosphorus dose of $4 \cdot 10^{12}$ cm^{-2} with an implant energy of 300 keV. The Phosphorus implant is followed by a drive-in for 900 minutes at 1150 keV. This drive-in results in a junction depth of 5.2 µm with a surface concentration of $1.5 \cdot 10^{16}$ cm^{-3}. The concentration profile of Phosphorus and Boron after drive-in step is shown in figure 5.2.

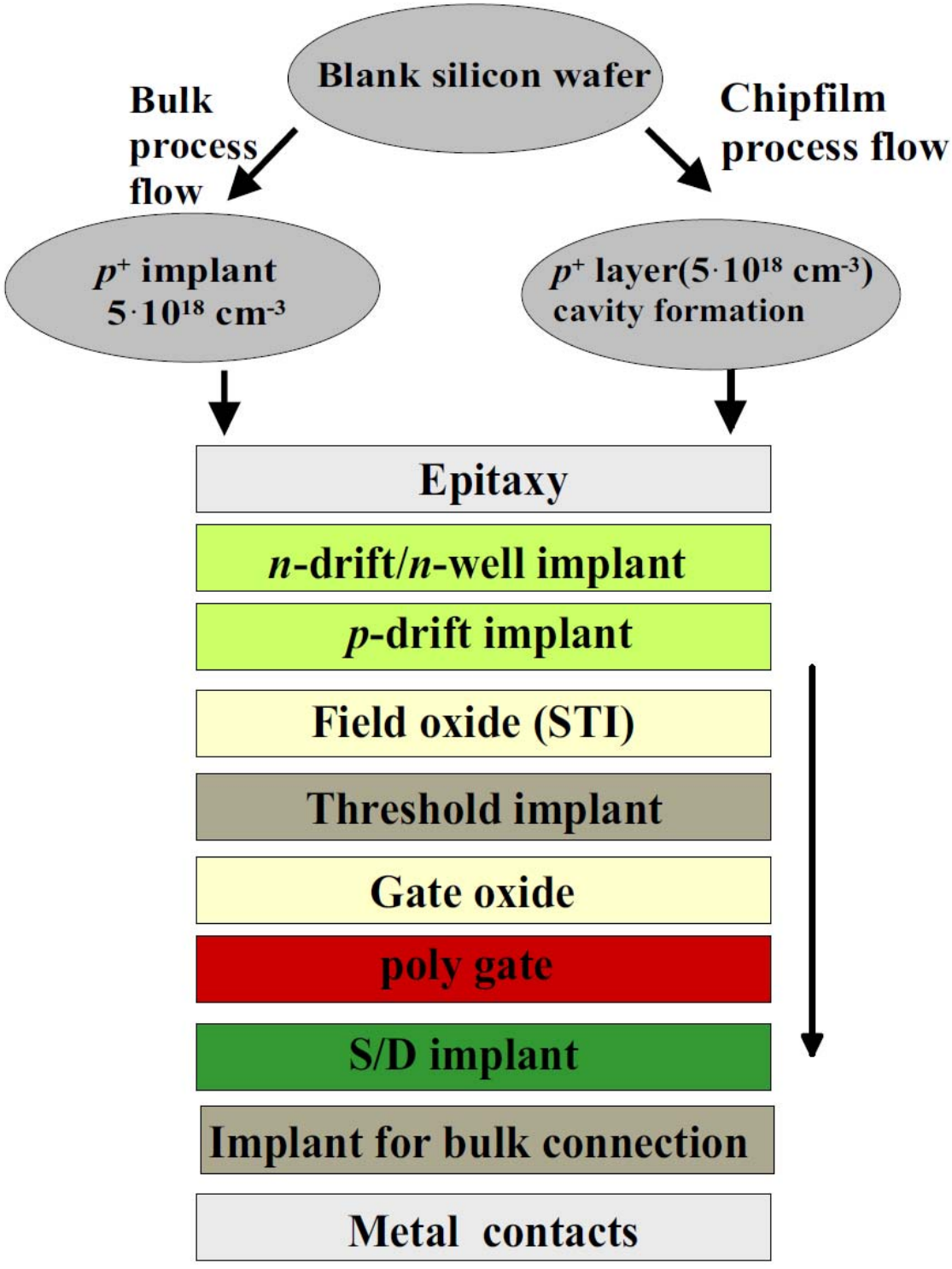


Figure 5.1: Process flow comparison of Chipfilm™ and bulk technology.

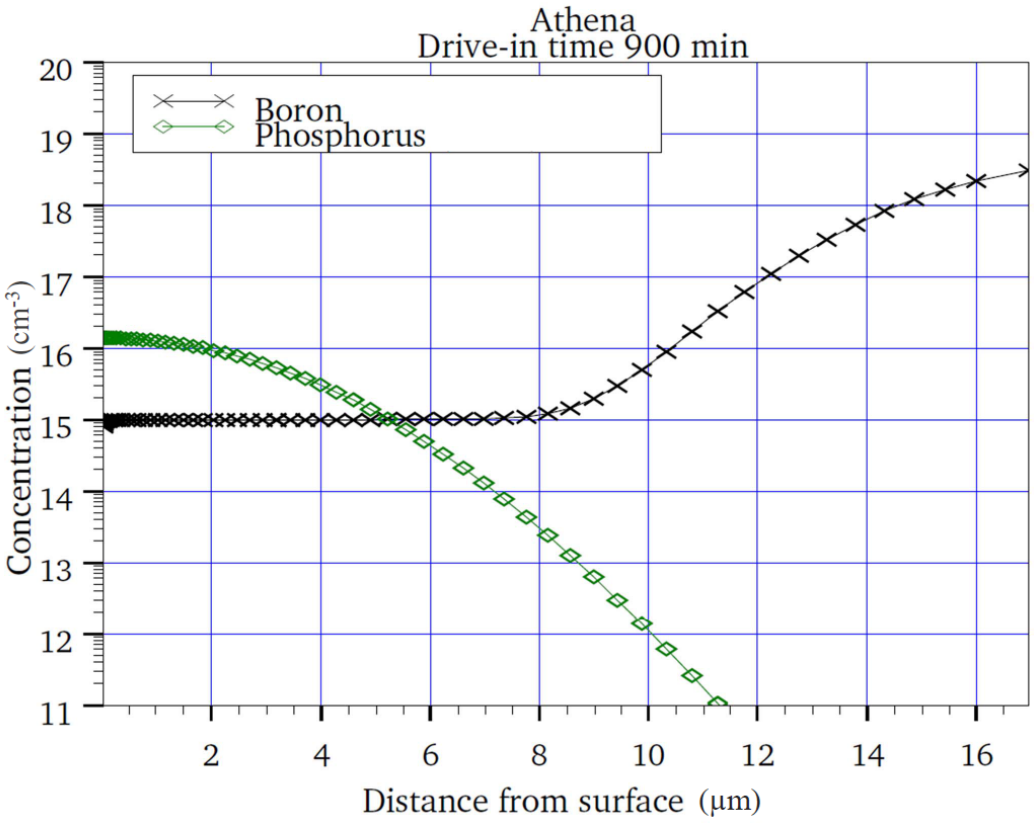


Figure 5.2: A semi-logarithmic graph comparing the concentration profiles of Phosphorus and Boron after 900 minutes *n*-well/drift drive-in. Surface concentration of Phosphorus is $1.5 \cdot 10^{16}$ cm^{-3} and junction depth is 5.2 µm.

The depths of the *n*-drift region in *n*-type LDMOS (NLDMOS) and the *n*-well region in *p*-type LDMOS (PLDMOS) are identical in this process. The depths are kept the same in order to reduce the number of CMOS process steps by combining *n*-well and *n*-drift processes.

In Chipfilm™ technology, there exists a limit on a maximum allowed thermal budget for the device integration processing on ultra-thin chips. The reason for this restriction is the out-diffusion of Boron from the back-side p^+ layer into the epitaxial layer, especially during high-temperature process steps. For an overly-high thermal budget, this extra Boron dose can severely affect the device performance and can lead to the device malfunction. The major contribution in the overall thermal budget comes from the well drive-in step. Figure 5.3 shows the effect of Boron out-diffusion on the *n*-well/drift junction depth after drive-in step. The simulation is performed for a 16 µm thick *p*-type

epitaxial layer and an implant dose of $4 \cdot 10^{12}$ cm^{-2} at 300 keV.

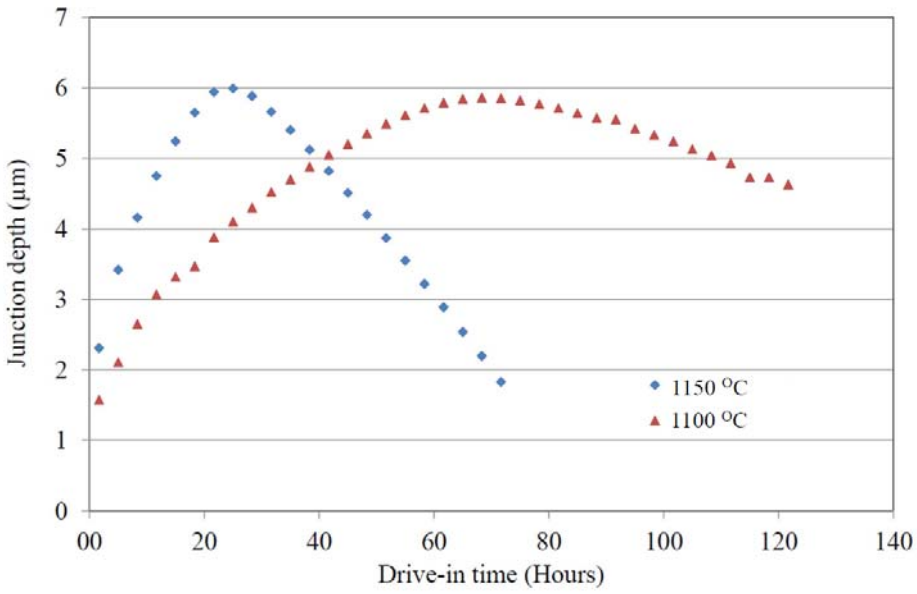


Figure 5.3: Variation in junction depth with drive-in time.

It can bee seen in figure 5.3 that the *n*-well/drift junction attains its maximum depth for a drive-in time of about 25 hours at 1150 ^{O}C after which it starts decreasing. This decrease in the junction depth is due to the out-diffusion from the high-doped p^+ layer at the bottom into the low-doped epitaxial layer. Figure 5.3 also shows that for a given substrate thickness, the deeper the required junction, the narrower would be the permissible range of variation in thermal budget.

Figure 5.4 shows the Boron out-diffusion profile after a drive-in time of 2300 minutes. A comparison of figures 5.2 and 5.4 shows that in both cases the *n*-well/drift junction depth is almost the same (i.e. 5.2 µm). However, after 900 minutes drive-in the effect of out-diffusion has not reached the junction and the diode is exhibiting a profile somewhat similar to that of a punch-through diode. The punch-through diodes can achieve the desired breakdown voltage with almost half the width of ordinary diodes [50]. In case of 2300 minutes drive-in, the profile resembles that of a diffused junction diode. The effective background doping is this scenario is comparably higher than in the punch-through case, which can reduce the breakdown voltage. For 900 minutes drive-in time, the Boron out diffusion is only 7–8 µm, which is not an issue with the 20 µm chips as seen in figure 5.2. However, in case of chips with thickness < 10 µm reduction in the thermal budget is indispensible.

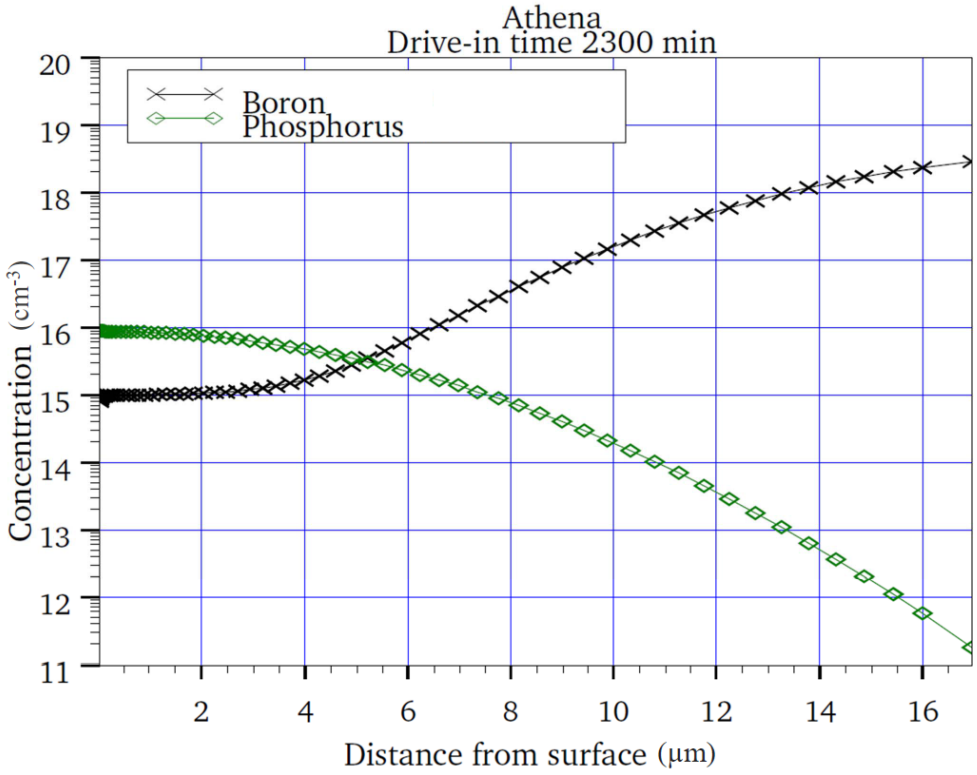


Figure 5.4: A semi-logarithmic graph of the concentration profiles of Phosphorus and Boron after 2300 minutes *n*-well/drift drive-in. The surface concentration of Phosphorus is $1.5 \cdot 16$ cm^{-3} and the junction depth is 5.2 µm.

After the drive-in step, a *p*-drift implant is performed. The same 15 nm oxide layer, which is grown before *n*-well/drift implant, is used for the *p*-drift implant as a screen oxide. A Boron dose of $6 \cdot 10^{12}$ cm^{-2} is implanted at 110 keV. No drive-in step is employed after the *p*-drift implant. The reason is to keep the *p*-drift junction at about 1 µm so that the distance between the *n*-well/substrate junction and *n*-well/*p*-drift junction can be kept at maximum in order to avoid punch-through. The *p*-drift implant is followed by shallow trench isolation (STI) process. For the STI, a new layer of 15 nm thick oxide is grown. A nitride layer of 150 nm is deposited over it and patterned at positions where trenches are required to be formed in the silicon. The silicon layer is etched from these positions down to 300 nm depth to form shallow trenches. Figure 5.5 shows the result of the STI process step.

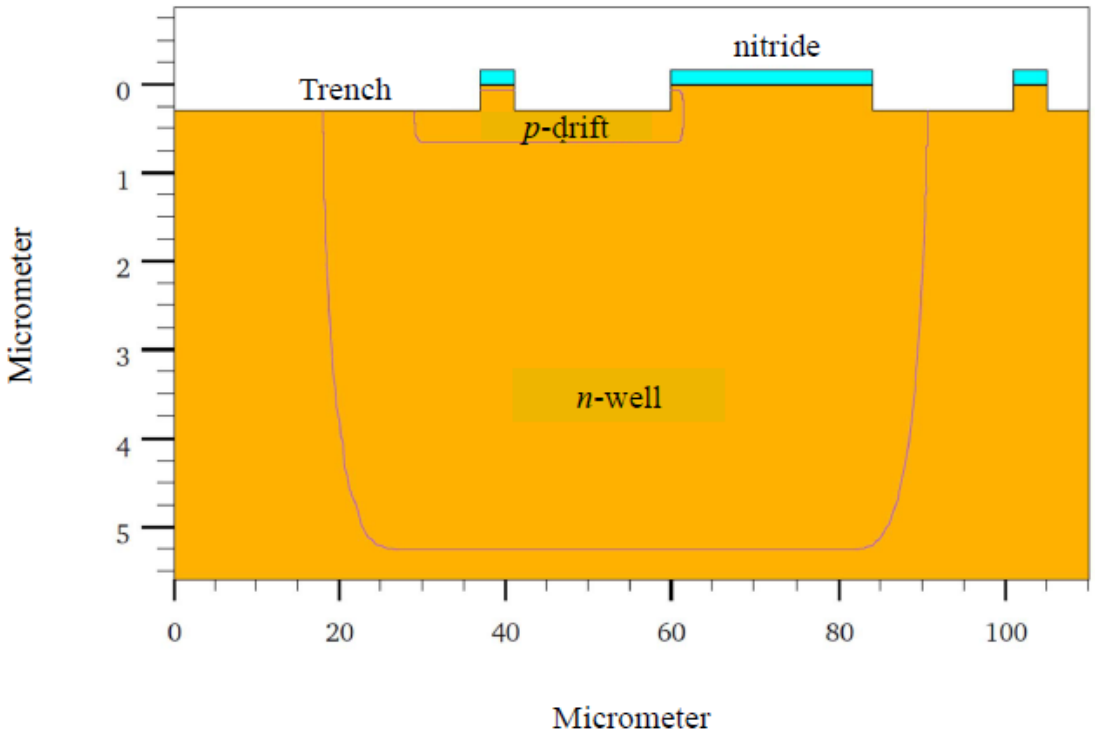
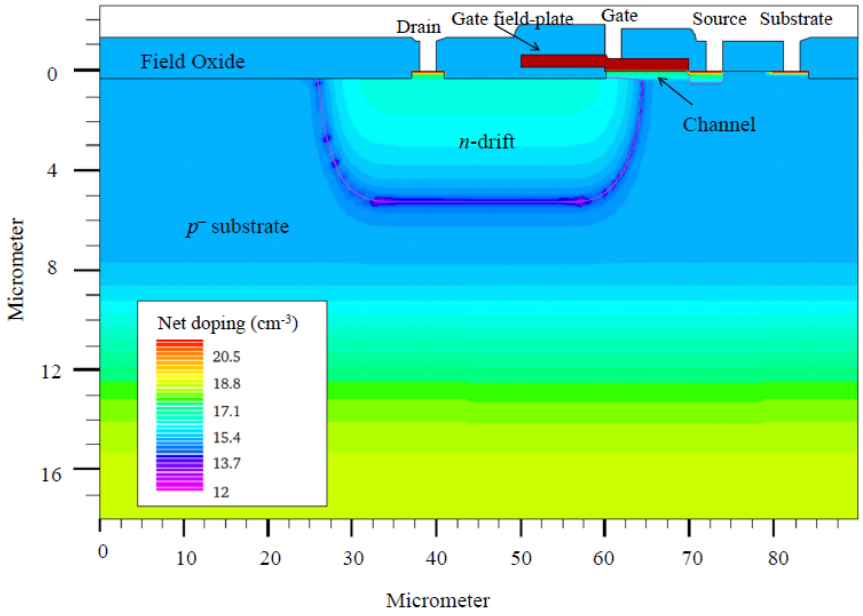


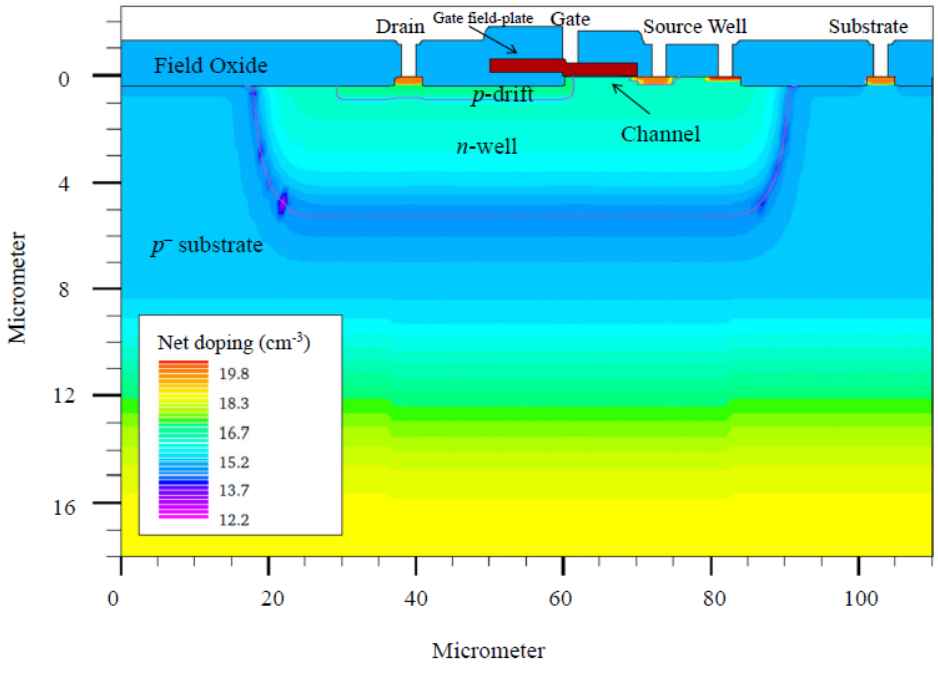
Figure 5.5: A magnified view of PLDMOS structure after *p*-drift implant and shallow trench.

After the trench formation, a 50 nm oxide is grown in the trenches through dry oxidation, followed by a 0.5 µm thick oxide layer deposition. The oxide layer is etched over the positions where the nitride is present underneath. A chemical mechanical polishing step is employed for planarization of the oxide edges left behind in previous etching step. After the planarization, the nitride layer is etched off followed by etching of a thin oxide layer of 20 nm. A new screen oxide layer is then grown for the threshold implant. The threshold implant is employed in the NLDMOS only. A $2.5 \cdot 10^{12}$ cm^{-2} dose of Boron Fluoride (BF_2) is implanted at 60 keV as the threshold implant. The oxide layer is removed again and a new oxide layer as gate oxide is grown through dry oxidation method. A 15 nm thick gate oxide is used in this device which has the same thickness as used in low voltage 0.8 µm CMOS technology. An *n*-poly gate contact is formed after the gate oxide growth. After the *n*-poly gate patterning, implantations are performed for drain, source, well and substrate contacts using standard procedures. Borophosphosilicate glass (BPSG) layer and reflow steps are performed followed by etching of contact holes into the thick oxide layer to form metal contacts. Figures 5.6

shows the cross-sectional view of the ultra-thin NLDMOS and PLDMOS structures, resulted at the end of the process.



a)



b)

Figure 5.6: Ultra-thin LDMOS structures. a) NLDMOS b) PLDMOS. The effect of Boron out-diffusion from the buried p^+ layer has reached up to 8 µm.

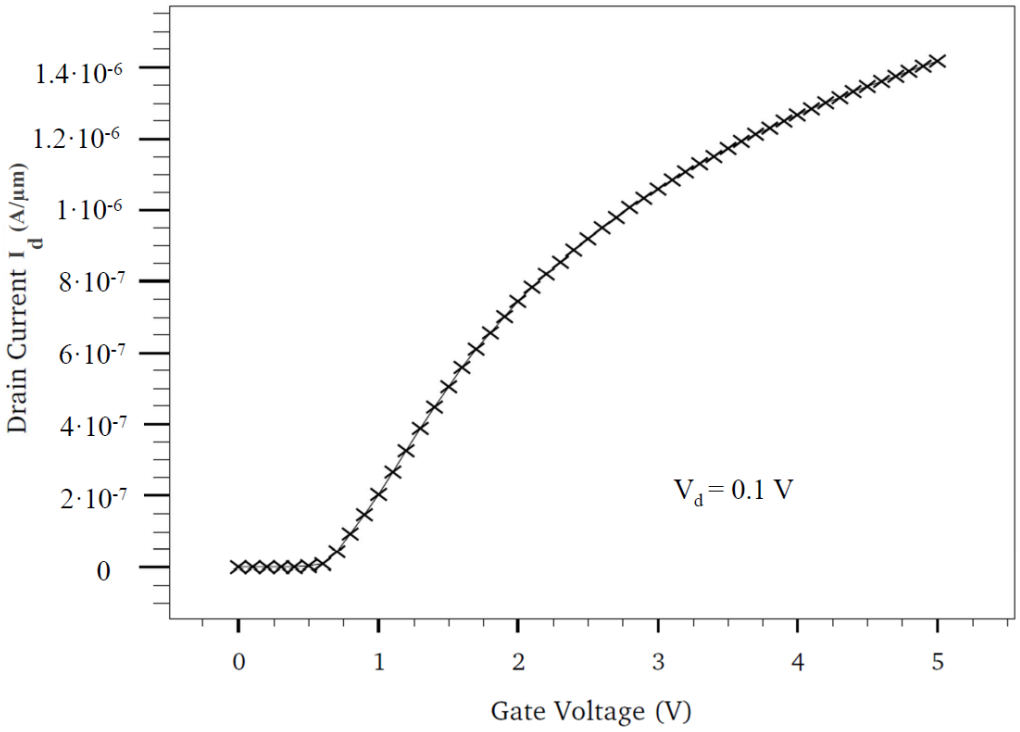
The metal contacts are not shown here, as they were considered as an ideal ohmic contact in the Atlas simulator. The design is similar to a conventional high-voltage LDMOS on thick substrates. It comprises drain, source, channel and drift regions. The polysilicon is extended over the drift region to form the gate field plate. Figures 5.6 also show the level of out diffusion from the p^+ layer at the bottom. The out diffusion of Boron into the epi-layer, which is an inherent part of the fabrication on Chipfilm™ wafers, is still about 7–8 μm. This shows that the major contribution in the out-diffusion comes from the drive-in step. Variations in the thermal budget due to process steps other than drive-in have an insignificant effect on this out-diffusion.

5.2 Simulated electrical characteristics

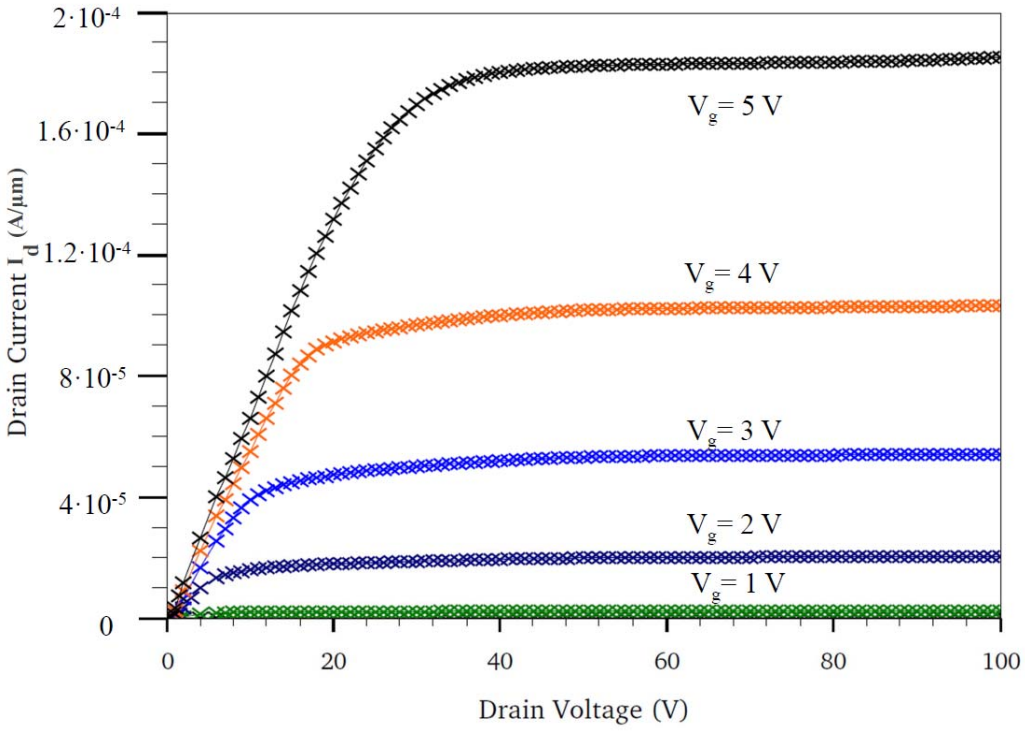
The electrical characteristics of the LDMOS structures are simulated in Atlas of Silvaco. The optimized values of various device parameters are obtained after performing a number of simulations using both Athena and Atlas. The following parameters are optimized to achieve a breakdown voltage of more than 100 volts:

- Implant doses
- Substrate concentration
- Junction depths
- Depth of trench
- Drift and channel lengths.

The device parameters are optimized for a 5 μm deep *n*-well/drift junction and approximately 1 μm deep *p*-drift junction. The input and output characteristics for NLDMOS and PLDMOS are shown in figures 5.7 and 5.8 respectively.

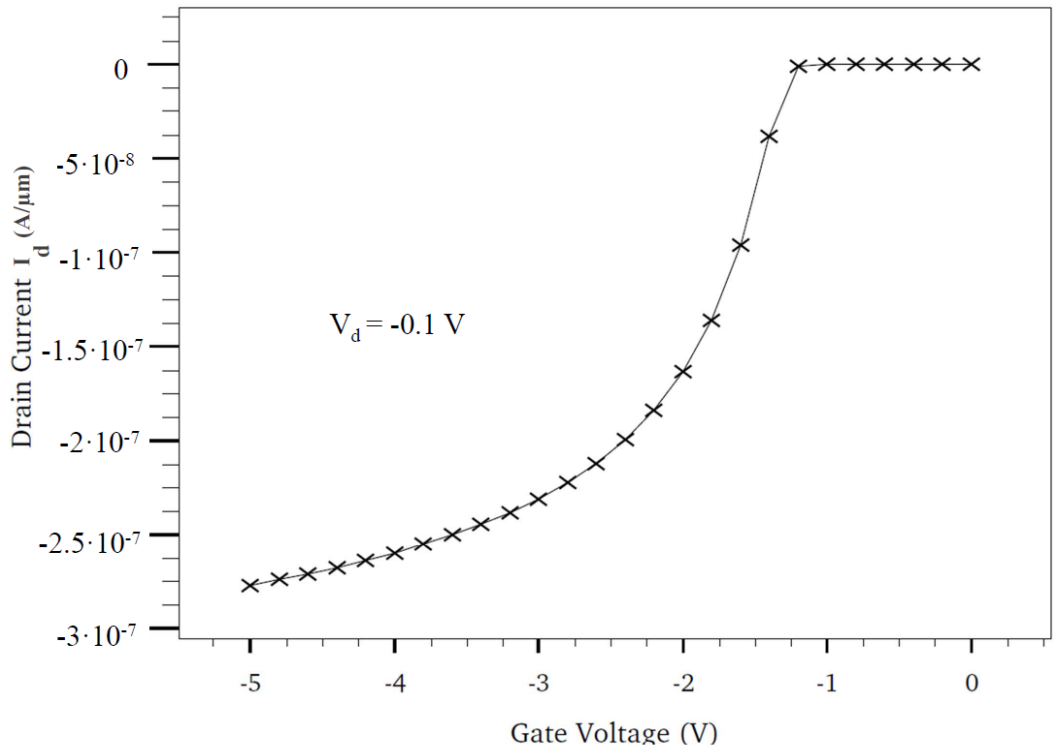


a)

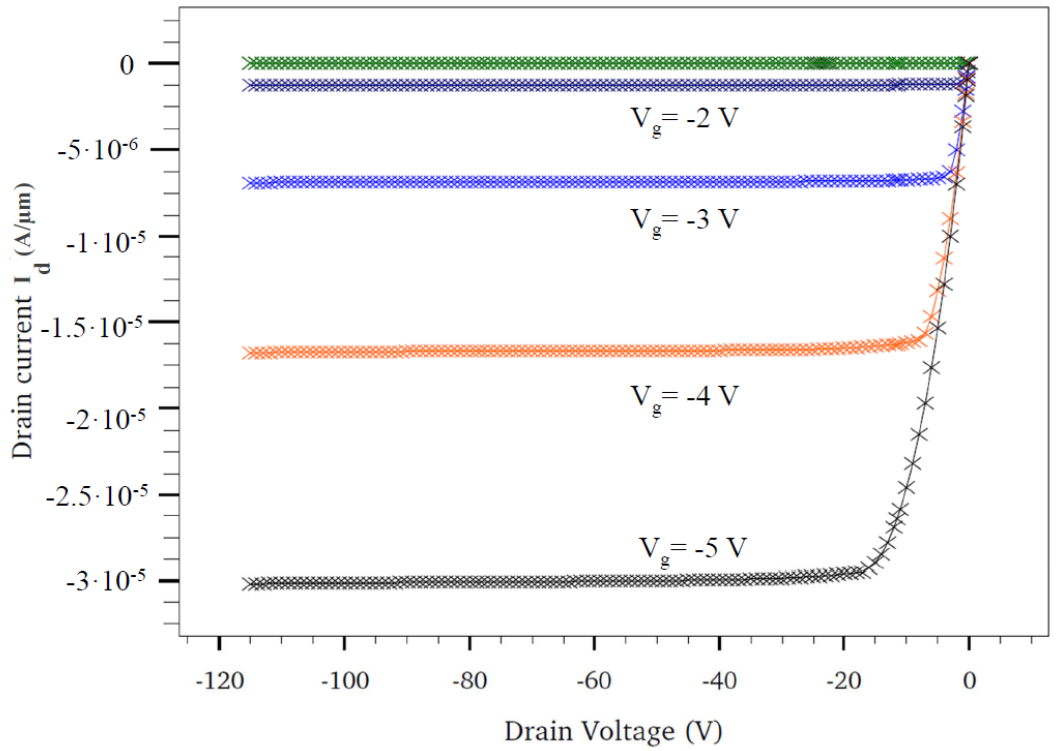


b)

Figure 5.7: DC electrical characteristics of NLDMOS a) input characteristics b) output characteristics.



a)



b)

Figure 5.8: DC electrical characteristics of PLDMOS a) input characteristics b) output characteristics.

In both the NLDMOS and PLDMOS the channel length and the gate field-plate length are set to 10 μm each. The length of the drift region is 20 μm. The gate oxide is 15 nm thick, which is the standard thickness in a low-voltage CMOS process. The field isolation is arranged by using the shallow trench isolation (STI) technique. The total thickness of the field-oxide is 500 nm, whereas the trench depth in the silicon is 300 nm. The *n*-well/drift implant dose is $4 \cdot 10^{12}$ cm^{-2} and the *p*-drift implant dose is $6 \cdot 10^{12}$ cm^{-2} for a substrate concentration of $1 \cdot 10^{15}$ cm^{-3}. The gate field-plate is 10 μm long.

Simulations for the input characteristics show a threshold voltage of 0.6 V for the NLDMOS and 1.2 V for the PLDMOS. The output characteristics show that for the above mentioned parameter settings, the NLDMOS can provide current up to 180 μA/μm whereas in case of the PLDMOS it is 30 μA/μm.

During the device fabrication, the optimised values can vary within a range of 10%–20%. In order to see the effect of these variations on the device performance, especially in the case of breakdown voltage, a number of simulations have been carried out. It has been observed that the NLDMOS can maintain its breakdown voltage above 100 volts for a larger range of parameter variations as compared to the PLDMOS. The reason for this lies in the fact that the NLDMOS has a relatively deep drift junction when compared to PLDMOS.

The *p*-drift junction depth is about 1 μm, out of which about 300 nm has been etched off during the STI process, leaving behind a junction thickness of only about 0.7 μm. At such a small junction depth, a variation in the junction depth of even a few hundred nanometers can change the breakdown voltage significantly. Together, small changes in the implant dose, implant energy and trench depth can easily lead to such variations. Figure 5.9 shows the effect of the trench depth on the breakdown voltage in the case of PLDMOS. A sharp fall in breakdown voltage (BV) occurs after a trench depth of 350 nm. Also, a minimum trench depth of 200 nm is required to attain a breakdown voltage of 100 volts. This leaves a window of only 150 nm for variation in trench depth within which the device can give a 100 V breakdown voltage. The case of NLDMOS is not shown here, as the effect of such small variation in trench depth on NLDMOS is not significant due to its deep drift region ($\approx$ 5 μm).

Figure 5.10 shows the effect of variation in implant dose of *n*-well/drift on both NLDMOS and PLDMOS.

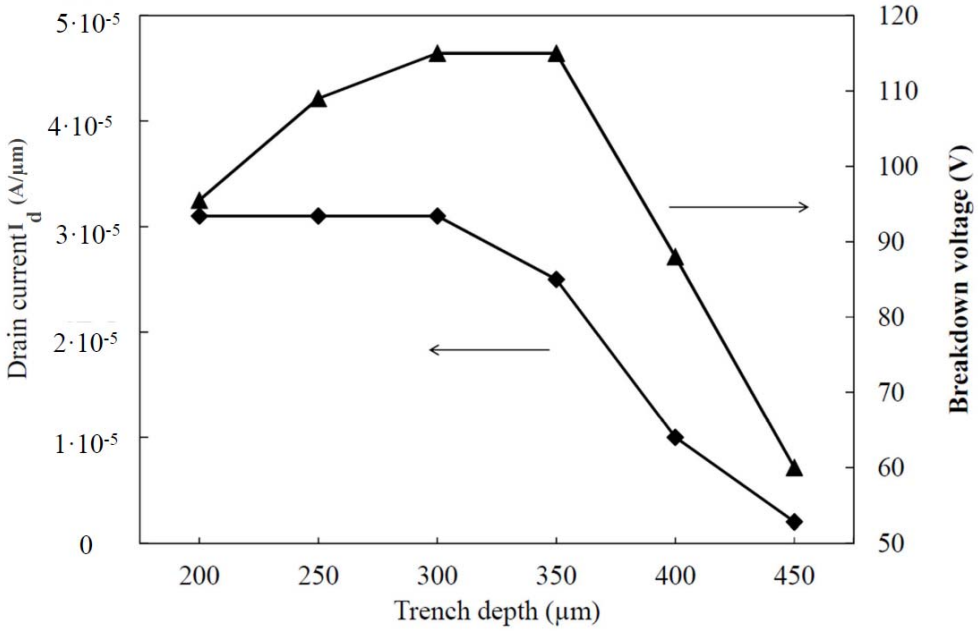


Figure 5.9: Effect of trench depth on breakdown voltage of PLDMOS.

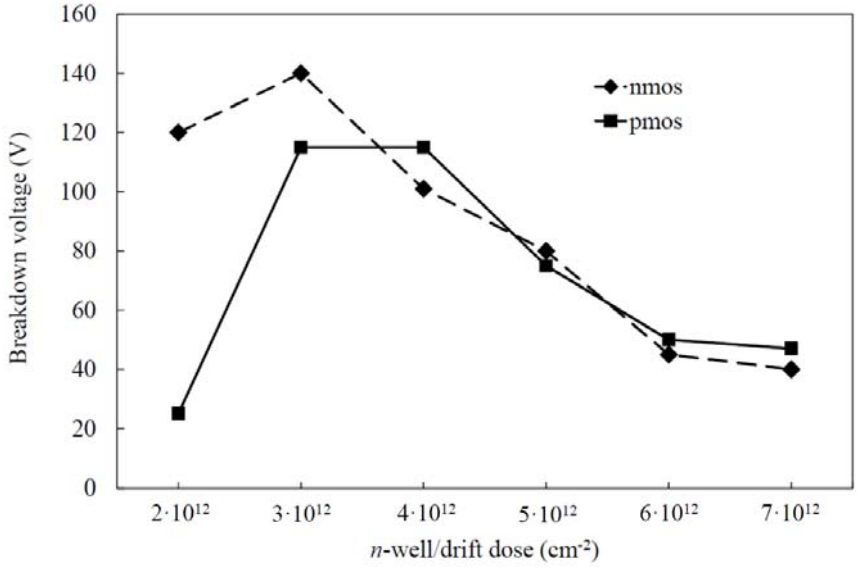


Figure 5.10: Effect of *n*-well/drift dose on breakdown voltage of NLDMOS and PLDMOS.

The *p*-type substrate concentration is $1 \cdot 10^{15}$ cm^{-3} and epi-thickness is 16 μm. It is evident from figure 5.10 that the PLDMOS can provide 100 volts only in the range of $3 \cdot 10^{12}$ cm^{-2} to $4 \cdot 10^{12}$ cm^{-2}. In case of NLDMOS the acceptable variation range in

implant dose is somewhat relaxed.

Figure 5.11 illustrates the effect of *p*-drift dose on the breakdown voltage. The simulation shows that for the Boron dose in the range of $5 \cdot 10^{12}$ cm^{-2} to $8 \cdot 10^{12}$ cm^{-2}, the PLDMOS structure can sustain 100 volts. However, beyond these limits a sharp decrease in the breakdown voltage occurs. These simulation results correspond to a trench depth of 300 nm, *n*-well dose of $4 \cdot 10^{12}$ cm^{-2} and substrate concentration of $1 \cdot 10^{15}$ cm^{-3}.

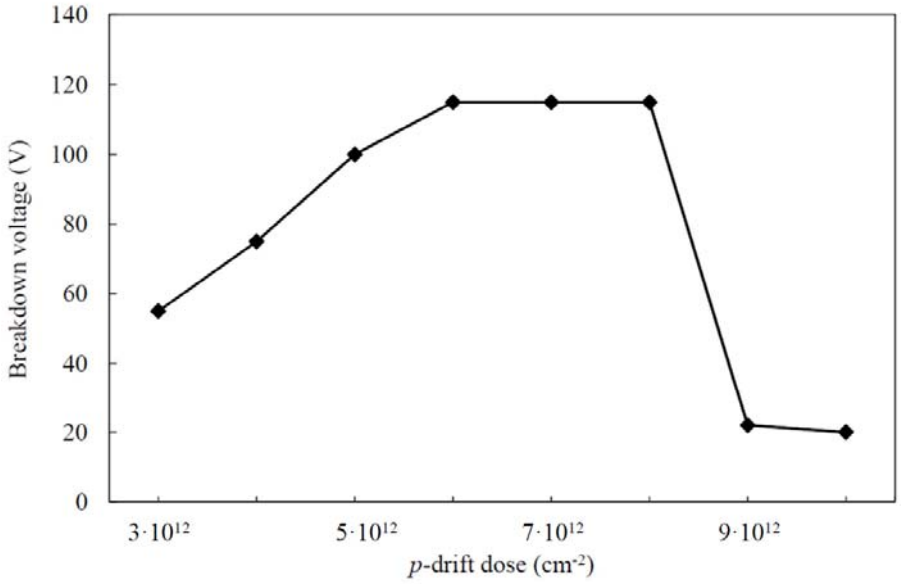


Figure 5.11: Effect of *p*-drift dose on PLDMOS breakdown voltage.

On Chipfilm™ substrates it is quite possible that the Boron concentration in the epitaxial layer rises significantly during the epitaxial growth and/or during the subsequent high-temperature processing, especially during the junction drive-in. The reason for this change is the presence of Boron by outgassing from the backside of the wafers in the chamber during the high-temperature processing steps. The magnitude of this change depends on factors like the number and position of wafers in heating chamber and varies from one lot of wafers to the other. In this scenario it is important to consider the effect of substrate concentration on the device performance. Figure 5.12 shows the effects of variation in substrate concentration on NLDMOS. It can be seen that the breakdown voltage of the NLDMOS stays well above the targeted 100 volts for substrate concentration higher than $1 \cdot 10^{15}$ cm^{-3}. It is about 100 volt for substrate

concentration less than $1 \cdot 10^{15}$ cm^{-3} up to $6 \cdot 10^{14}$ cm^{-3}. The drain current, however, decreases linearly with increase in the substrate concentration beyond $1 \cdot 10^{15}$ cm^{-3}.

The simulations have revealed that the breakdown voltage of PLDMOS stays unaffected while changing the substrate concentration from $6 \cdot 10^{14}$ cm^{-3} to $4 \cdot 10^{15}$ cm^{-3}. However, for substrate concentrations higher than $2 \cdot 10^{15}$ cm^{-3}, a significant amount of current flows between the substrate and drain terminals. Figure 5.13 shows the effect of substrate concentration on the substrate current. The simulation result suggests that in order to have a working device, the substrate concentration should be kept below $2 \cdot 10^{15}$ cm^{-3}.

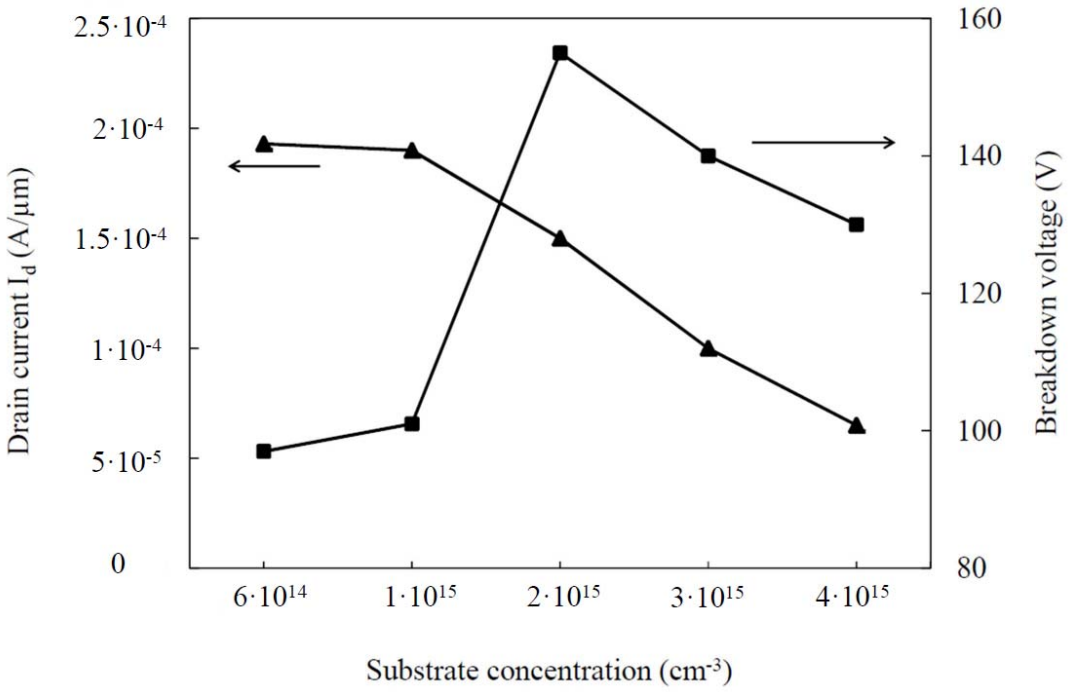


Figure 5.12: Effect of substrate concentration on breakdown voltage and drain current of NLDMOS.

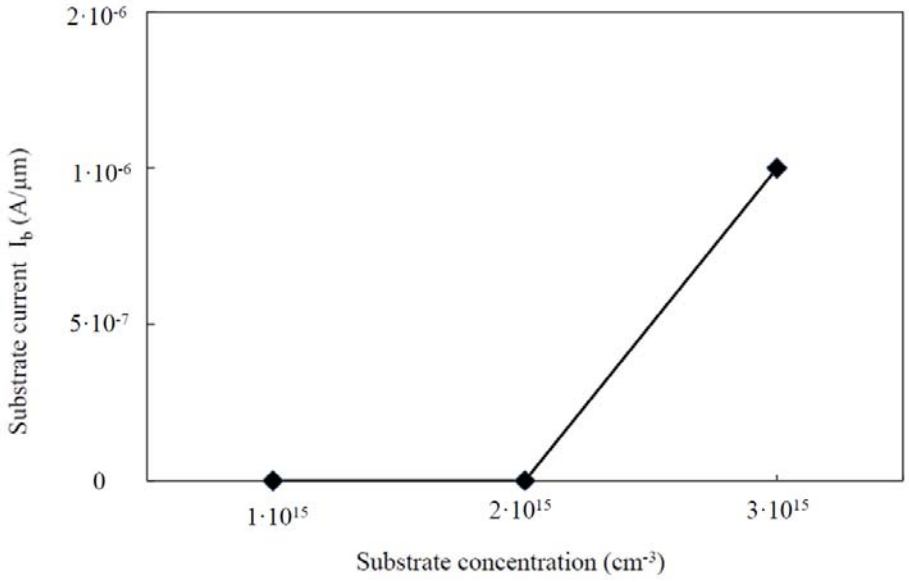


Figure 5.13: Effect of substrate concentration on substrate current for PLDMOS.

These simulations are optimised for a particular combination of substrate concentration, epi thickness and trench depth. A change in any of these parameters beyond certain limits will require a modification of the implant doses and re-optimization.

5.3 Fabrication

In order to compare the performance of the ultra-thin LDMOS on Chipfilm^{TM} wafers to the similar LDMOS on bulk reference wafers, device fabrication is performed on both types of wafers. The bulk reference wafers feature the same thin-film structure on a bulk wafer without the buried cavity formation, which in Chipfilm™ technology allows us to separate the thin surface layer from the substrate [97].

5.3.1 Layout and mask set

Prior to device fabrication, the device layout is generated by using the COMPASS design automation tool. The layout of an NLDMOS transistor is shown in figure 5.14

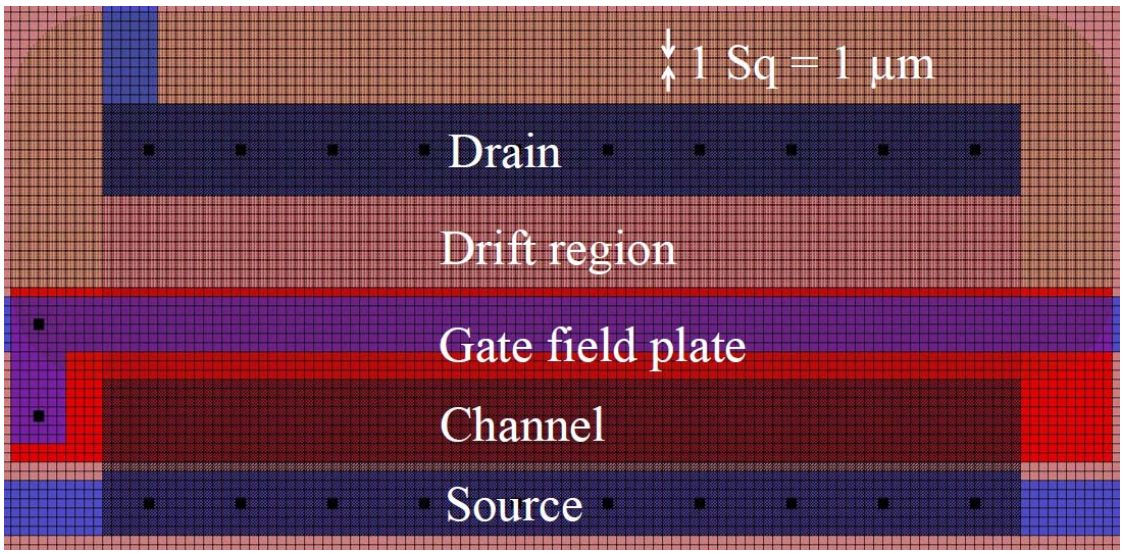


Figure 5.14: Layout of an NLDMOS transistor. Each square represents a distance of 1 µm.

The mask set from the Hyper-braille project at IMS CHIPS for 200 V LDMOS has been used for the device fabrication.

The entire chip consists of different modules out of which two modules contain the ultra-thin LDMOS transistors. Figure 5.15 shows the layout of the chip with all modules. The modules relevant to this thesis are labeled as TRNP1 and AA-CH1-1.

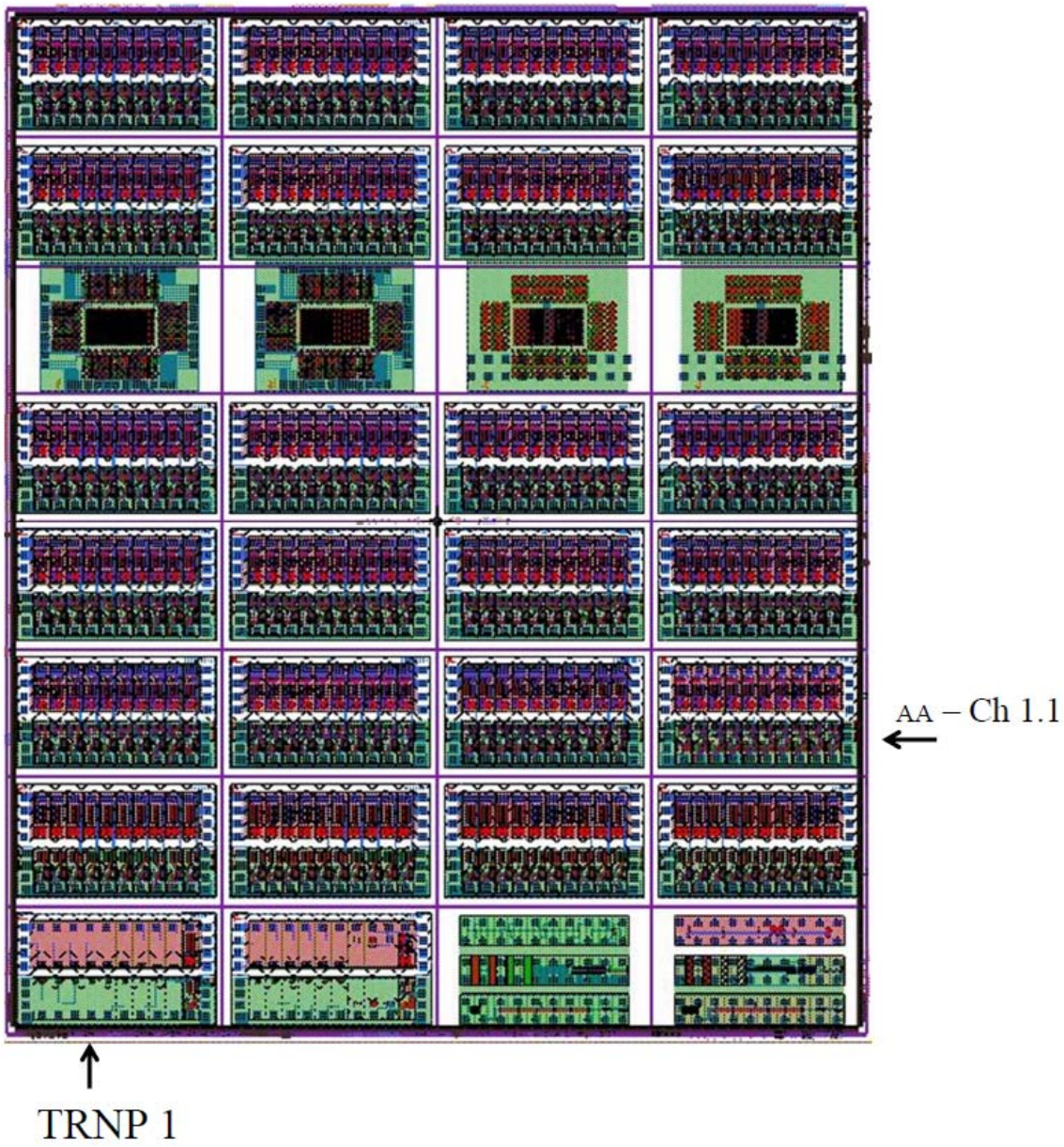


Figure 5.14: Layout of the chip.

Magnified views of the TRNP 1 and the AA- CH1-1 are shown in figures 5.15 and 5.16. Each module is divided into two sections. The upper (pink) section contains a row of the PLDMOS with different channel lengths, whereas the lower (green) portion contains the NLDMOS transistors, having different channel lengths. In the AA- CH1-1, the source and bulk connections are connected together, whereas in the TRNP1 module they are separated from each other. In both modules, the gate, source and bulk connections are common between all transistors; only the drain terminal is separate for each transistor.

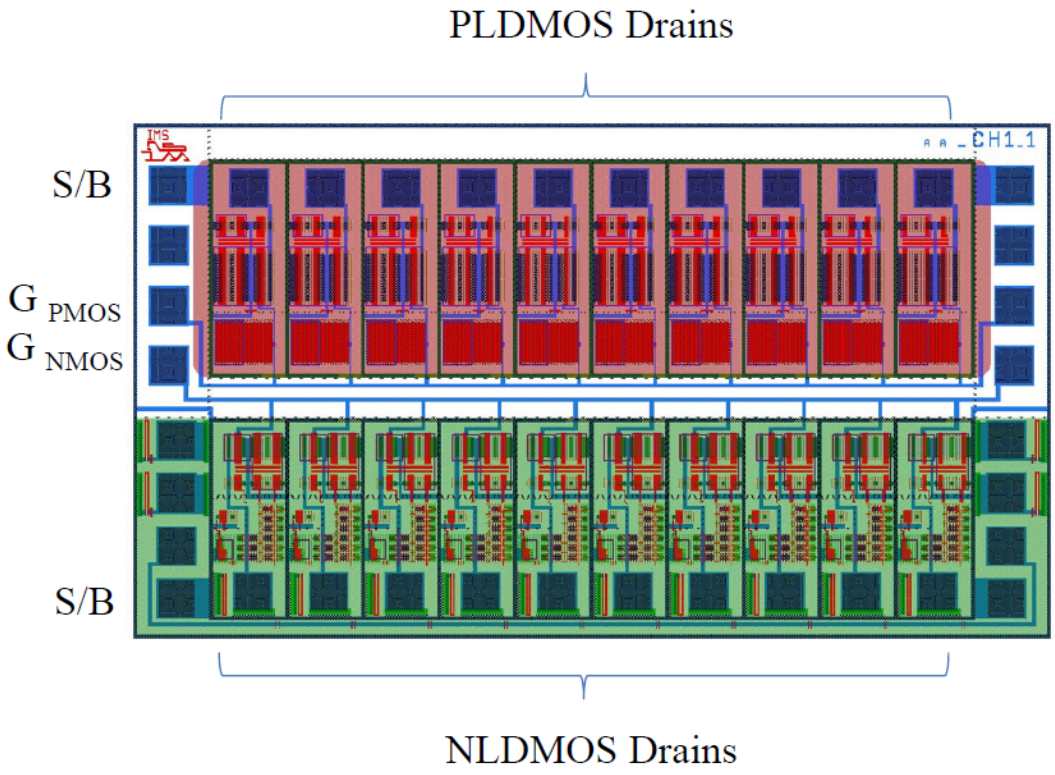


Figure 5.15: Layout of the AA-CH1-1 Module.

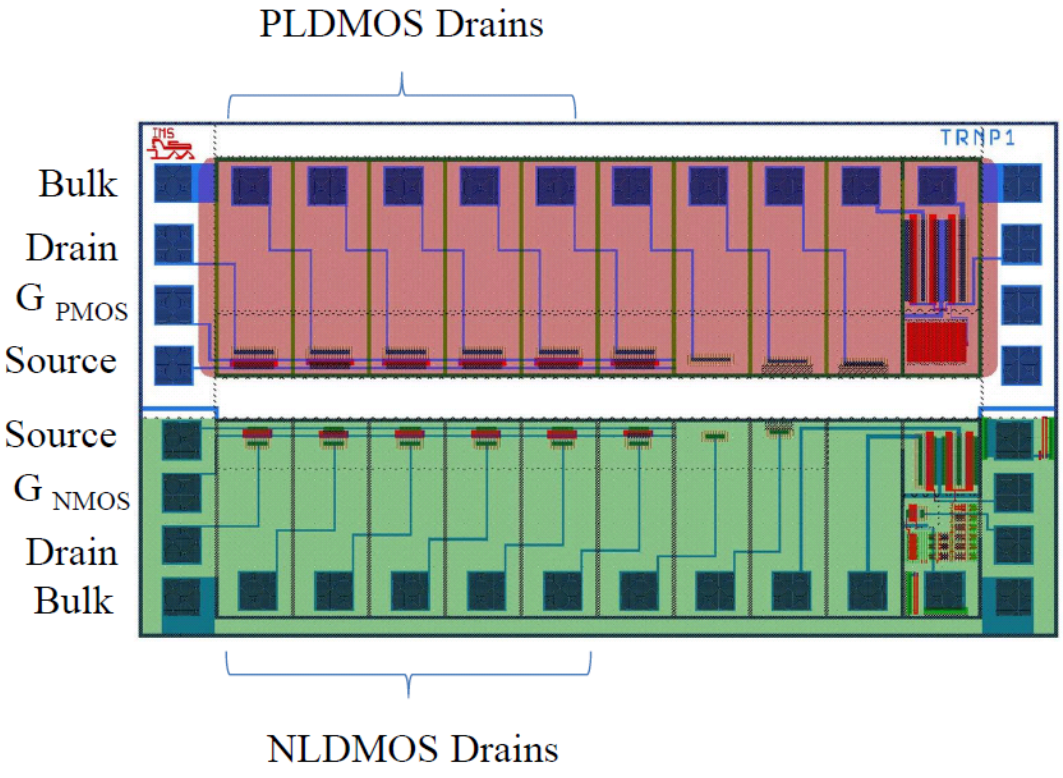
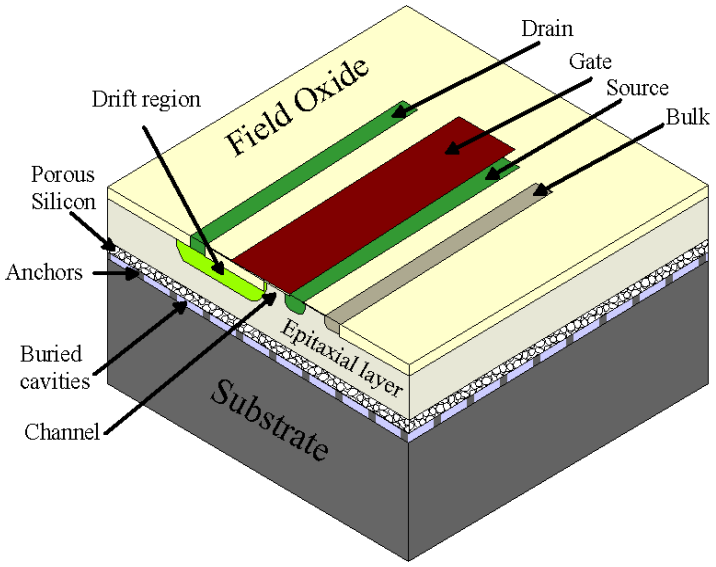


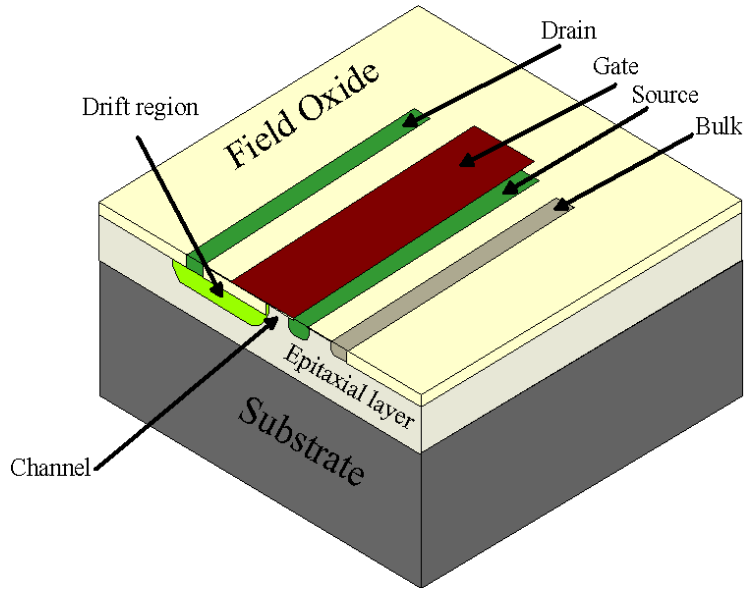
Figure 5.16: Layout of the TRNP1 module.

5.3.2 Processing for cavity formation

Conceptual views of the LDMOS transistor on a Chipfilm™ and on a bulk reference wafer after fabrication are shown in figures 5.17a and b.



a)



b)

Figure 5.17: Cross-section of LDMOS a) on a Chipfilm™ wafer and b) on a bulk reference wafer (not to scale).

In figure 5.17a, the final chip thickness is distinguished from the substrate by a layer or anchors and cavities. After trench etching down into to the cavities, the chip can easily be picked, cracked and placed onto other substrates. In figure 5.17b, although the thickness of the epitaxial layer is the same as that in Chipfilm^{TM}, physically there is no separation between epi-layer and the substrate. That is why it is difficult, if not impossible, to achieve ultra-thin (< 20 μm) form bulk silicon technology.

The fabrication of the LDMOS transistors on Chipfilm^{TM} substrates are performed in a lot of 21 wafers. The Chipfilm™ fabrication starts by growing a 6 μm p^- epitaxial layer on a silicon wafer. The resistivity of the p^- epitaxy is measured to be 11 Ω-cm whereas the measured thickness is 6.04 μm. After the oxidation is performed a Boron dose of $5 \cdot 10^{14}$ cm^{-2} is implanted at 30 keV. A Phosphorus implant is done afterwards with a dose of $2 \cdot 10^{15}$ cm^{-2} at 180 keV. The positions where Phosphorus is implanted serve as the anchor array. This anchor array is designed strong enough to keep the thin chip surface layers firmly attached during the wafer processing but sufficiently weak to allow for chip detachment after trench etching.

Wafers are then annealed for 200 minutes at 1100 ^{O}C and the oxide layer is etched afterwards. Porous etching is carried out, which results into the formation of small and large pores in *p*-type silicon. Anodic etching of blank silicon wafers results into a thin (1–2 μm) dual (fine/coarse) porous silicon layer within the p^+ doped layer at the wafer surface. A 16 μm intrinsic epi-layer is grown at 1100 ^{O}C. During thermal annealing and epitaxial growth of the intrinsic 16 μm thin device layer, the coarse layer of the porous silicon structure transforms into buried cavities that are interrupted only by an array of vertical anchors [2]. The flow of wafer pre-processing steps is shown in figure 5.18. After Chipfilm^{TM} wafer preparation, the process flow follows the simulated sequence of steps. Table 5.1 summarizes the step sequence.

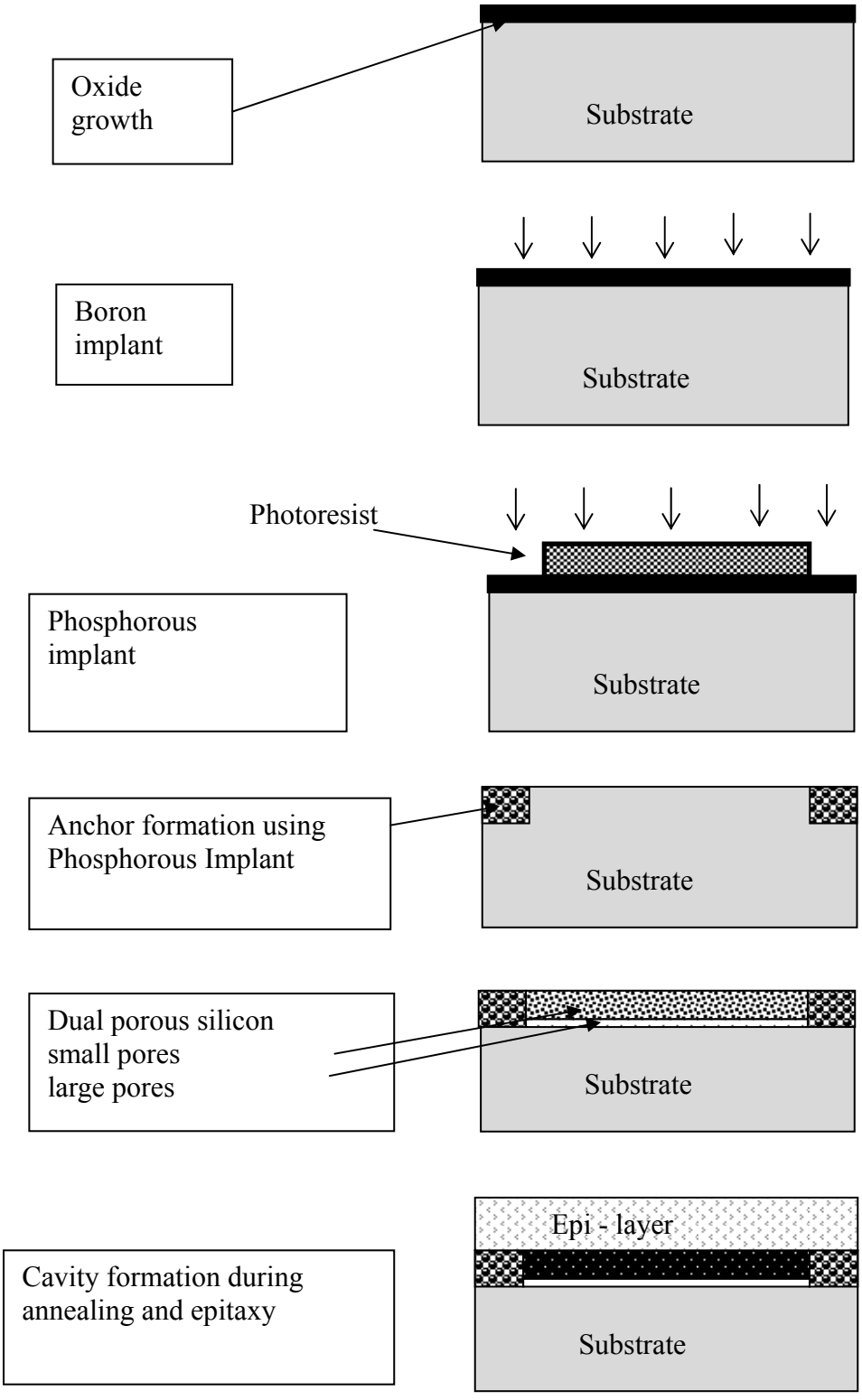


Figure 5.18: Pre-processing steps for a Chipfilm™ wafer.

5.3.3 Device fabrication

Table 5.1: Major process steps of device fabrication. Desired values are the optimized and standard values after process step. Measured values are the ones which are achieved after the completion of process step.

Sr.	Process Step	Desired values	Measured/realized values
1	Oxidation	15 nm	15.5 nm
2	*n*-well/drift implant	$4 \cdot 10^{12}$ cm^{-2}@ 300 keV $5 \cdot 10^{12}$ cm^{-2}@ 300 keV $6 \cdot 10^{12}$ cm^{-2}@ 300 keV	$4 \cdot 10^{12}$ cm^{-2}@ 300 keV $5 \cdot 10^{12}$ cm^{-2}@ 300 keV $6 \cdot 10^{12}$ cm^{-2}@ 300 keV
3.	Drive-in	900 minutes at 1150 ^{O}C	900 minutes at 1150 ^{O}C
4	Oxide measured	15 nm	98 nm
4a	*p*-drift implant	$6 \cdot 10^{12}$ cm^{-2}@ 110 keV $6 \cdot 10^{12}$ cm^{-2}@ 130 keV $6 \cdot 10^{12}$ cm^{-2}@ 150 keV	$6 \cdot 10^{12}$ cm^{-2}@ 110 keV $6 \cdot 10^{12}$ cm^{-2}@ 110 keV $6 \cdot 10^{12}$ cm^{-2}@ 110 keV
5	Oxidation	15 nm	15.5 nm
6	Nitride deposition	150 nm	192 nm
7	Trench etching	300 nm	370 – 400 nm
8	Oxidation	50 nm	54 nm
9	Oxide deposition	0.5 µm	0.59 µm
10	Oxide etching over nitride, CMP, nitride etching	-	-

11	Oxide measurement	550 nm	394 nm
12	Oxidation	26 nm	26 nm
13	Threshold Implant for NLDMOS only	Boron Fluoride (BF2); $2.5 \cdot 10^{12}$ cm^{-2} @ 60 keV	Boron Fluoride (BF2); $2.5 \cdot 10^{12}$ cm^{-2} @ 60 keV
14	Gate Oxide growth	15 nm	14.9 nm
15	Poly-gate thickness	0.5 µm	0.5 µm
16	Low-doped drain (LDD) implant for NLDMOS only	Phosphorus; $4 \cdot 10^{13}$ cm^{-2}@ 40 keV	Phosphorus; $4 \cdot 10^{13}$ cm^{-2}@ 40 keV
17	Spacer deposition	150 nm	150 nm
18	Source/Drain implant NLDMOS	Phosphorus; $5 \cdot 10^{15}$ cm^{-2} @ 50 keV	Phosphorus; $5 \cdot 10^{15}$ cm^{-2} @ 50 keV
19	Source/Drain implant PLDMOS	Boron Fluoride (BF2); $5 \cdot 10^{15}$ cm^{-2} @ 50 keV	Boron Fluoride (BF2); $5 \cdot 10^{15}$ cm^{-2} @ 50 keV

The process flow is similar to the standard high-voltage LDMOS process. The same mask set is used for this process. The extra steps performed in this process are

- Shallow trench Isolation (STI)
- Chemical Mechanical Polishing (CMP)

A photograph of the fabricated ultra-thin high-voltage LDMOS chip is shown in figure 5.19.

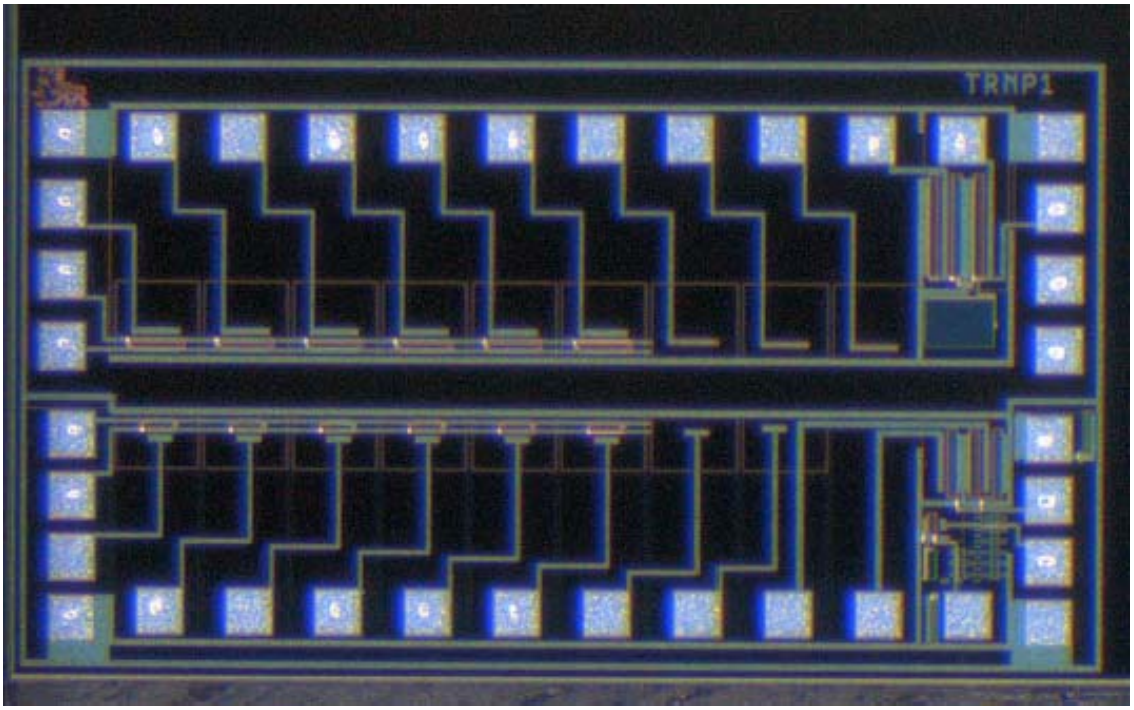


Figure 5.19: **Fabricated ultra-thin LDMOS chip. The chips are divided into two halves. The upper half contains a row of 6 PLDMOS and lower half contains row of 6 NLDMOS of different channel lengths.**

1. In step 5, three splits were planned for *p*-drift implants. On the base of simulation experience and its difference with real values an implant at 130 keV and 150 keV energies were was expected to be reasonable. However, due to some experimental error all wafers got the implant with 110 keV, which is the lowest value in all splits.
2. A trench depth of about 300 nm was required. But it was found that the trench depth lies somewhere between 370 and 400 nm. This extra 70 –100 nm trench depth could have a significant effect on the device performance especially in the case of PLDMOS.

In order to determine the trench depth, a wafer is broken at the position of highest probability of hitting a field-oxide edge region. The small broken stripe is put under the microscope and photographs are taken. The dimensions are measured by physically positioning the start and end points of a ruler built into the test equipment. Figure 5.20

shows the view of the gate-field plate over field-oxide (white). The right end shows the channel region. The photographs have shown that at the field-oxide and channel junction, the field oxide is over-etched and the gap is refilled by poly-silicon. This over etching could be a problem with the dimensions of the mask. Figure 5.21 shows the similar over etching of field-oxide at the drain side.

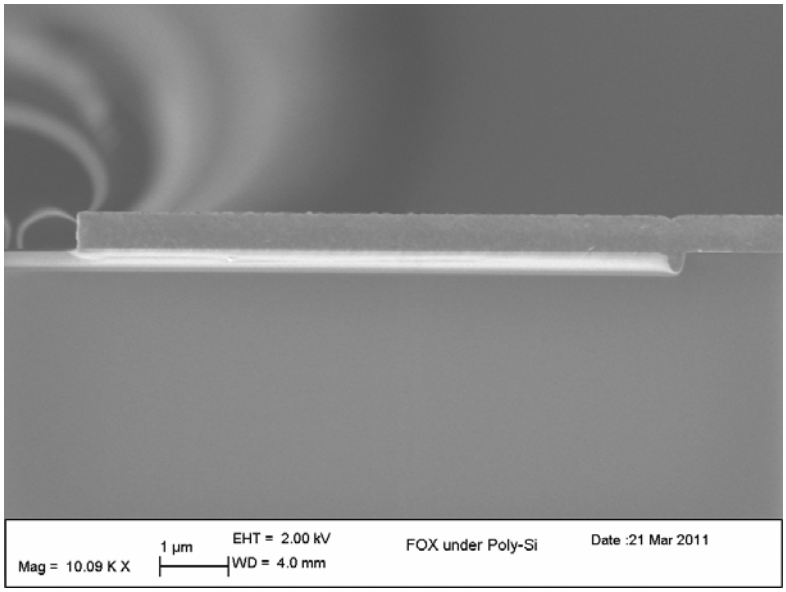


Figure 5.20: Cross-sectional view of fabricated gate-field plate over field-oxide.

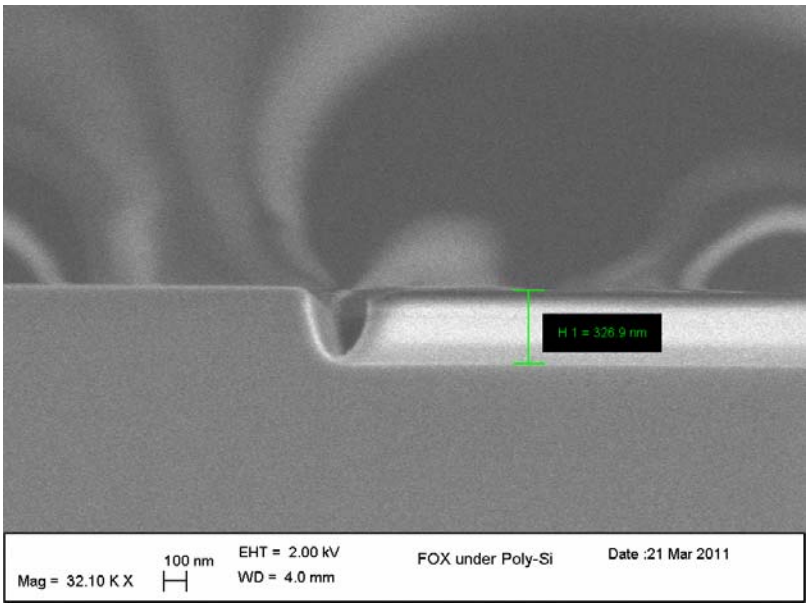


Figure 5.21: Over etching of field-oxide at the drain side.

Figure 5.22 shows the measurements of the thickness of the deposited poly-silicon layer and field-oxide. The total thickness of the field-oxide results to 326 nm whereas during the fabrication, a field-oxide 50 nm was grown and 500 nm oxide was deposited over it. This shows that almost 225 nm oxide has been etched away during processing.

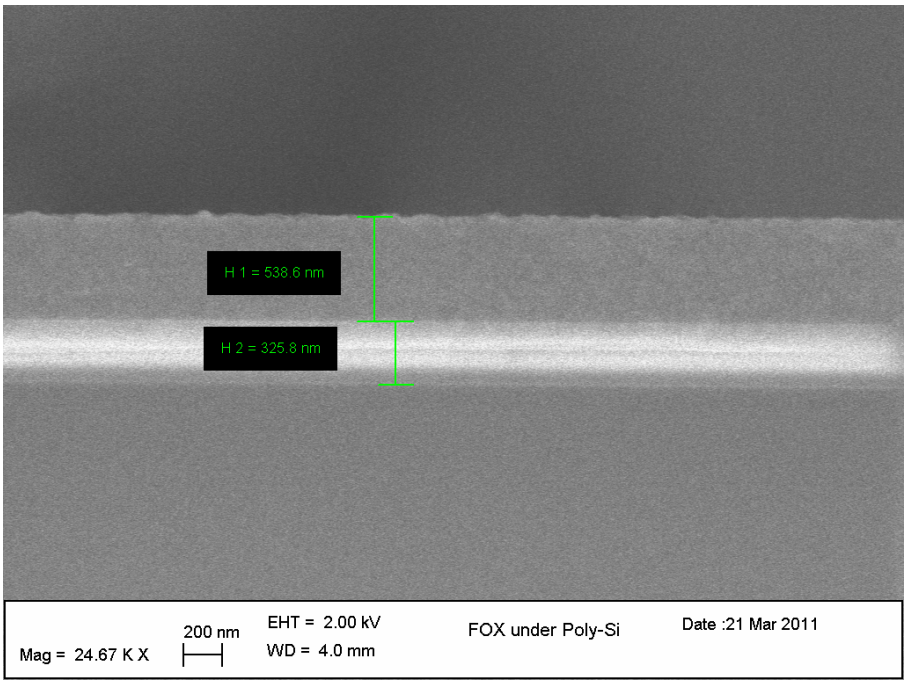


Figure 5.22 Measurements of field-oxide under poly-silicon gate field plate.

The width of field-oxide over-etching, which has created a ditch near the channel region, is about 260 nm as shown in figure 5.20. It can also be seen in figure 5.23 that the upper end of the field-oxide and the silicon surface are at the same level. But, this silicon surface is not at the same level as at the start of processing because some of the silicon is consumed in oxide formation and etching during previous steps. Considering these factors, it is evident that the depth of the trench in silicon is not 300 nm with respect to original silicon level, but, instead, its depth lies somewhere between 370 nm to400 nm. This variation in the device parameters can affect the device performance significantly and can lead to failure.

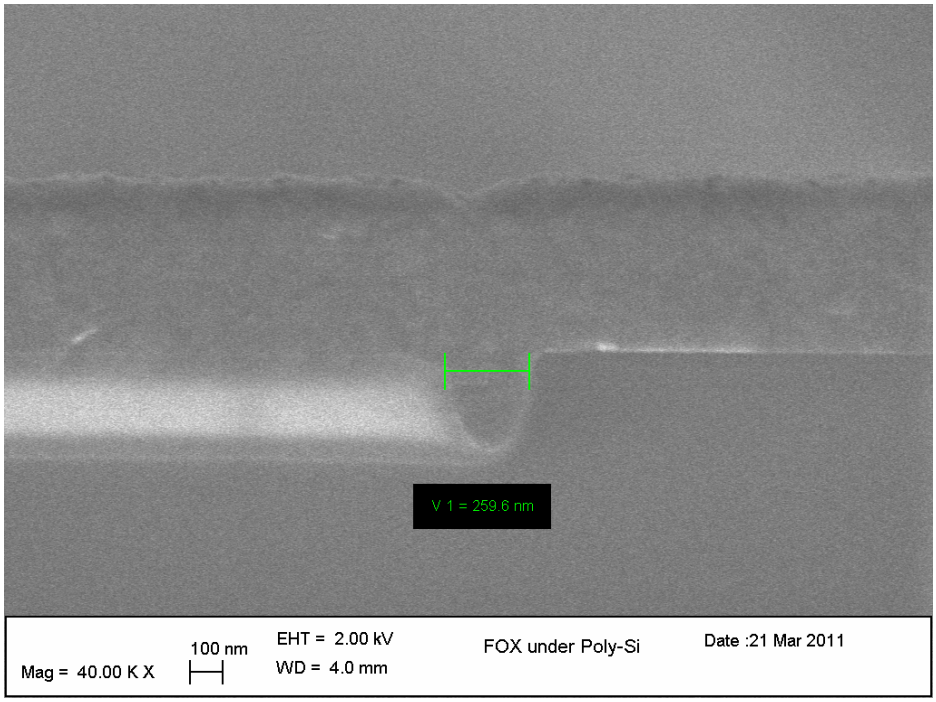


Figure 5.23: Measurements of field-oxide under the poly-silicon gate field-plate.

3. The process is optimised for the substrate concentration of $1 \cdot 10^{15}$ cm^{-3}. The resistivity of epi-layer after epitaxial growth showed a concentration of about $1 \cdot 10^{15}$ cm^{-3}. A rise in substrate concentration is, however, expected especially during the drive-in stage.
4. A low-doped drain implant and spacer deposition step has been added in the fabrication process, which was not present in the previous simulation. During the fabrication it was found that high implant dose of the source has caused a gate-oxide short-circuiting, thus resulting in device failure. The problem is solved by using low-doped drain implant in NLDMOS and formation of spacers. In PLDMOS, low-doped drain implant is not employed, as the Boron diffusion is sufficient in subsequent high-temperature process steps so that it can connect well to the gate.
5. Due to a mask error, a ditch is produced in field-oxide near channel region.

5.3.4 Post processing

After the device fabrication, the chips are detached from the wafers. For this, trenches around the chips are etched down into the buried cavities as shown in figure 5.24.

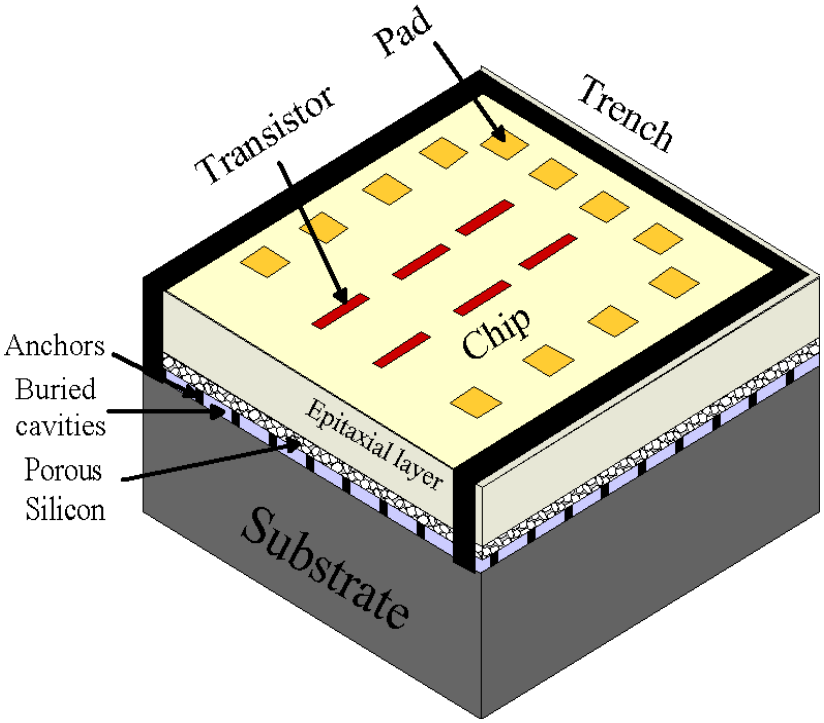


Figure 5.24: Cross-section of a Chipfilm™ die after trenching (not to scale).

The required depth of the trench is estimated by adding the approximate thicknesses of various layers which include epitaxial silicon, field oxide and BPSG layers. The trenches are etched using a plasma ion etching method. After the trench etching the wafers are annealed again at 400 ^{O}C for 30 minutes in the presence of hydrogen in the gas phase. This annealing is required so that the charge stored in the oxide layers during plasma etching can be removed. The chips are connected to their substrate only through weak anchors formed during the cavity formation. The chips are then picked, cracked and placed on different carrier substrates for measurements.

5.4 Summary

In this chapter we present the details of simulation and fabrication and discuss the issues related to ultra-thin LDMOS transistors. A CMOS process is devised, which is fully compatible with a conventional high-voltage LDMOS process flow with shallow trench

isolation (STI). Because of this full compatibility no extra mask and thus no extra cost is required for this process. The already available mask set of hyper braille project for 200 V CMOS is used for device fabrication. Effects of variations in several device parameters on the device performance are explored through simulation in Atlas. Variations in some of the parameters are identified during processing. A mask error is identified to cause a ditch in the field oxide. After fabrication, trenches are formed around the chip modules so that they can easily be detached from the bulk wafer and can be placed onto other substrates.

In the next chapter the measured electrical characteristics of both NLDMOS and PLDMOS are presented. The measurements are performed on the original wafer before as well as after trench etching when chips are placed onto different substrates.

6 Results and discussion

In this chapter the DC measurement results for the ultra-thin high-voltage lateral DMOS (LDMOS) transistors are presented. The initial measurements are performed on chips without detaching them from the substrate. These on-wafer measurements of DC input and output characteristics of the fabricated devices are performed by using the Agilent 4080 Series Parametric Test System (4083A Low Current Model). A comparison with the characteristics of a similar device on a bulk reference wafer is shown as well.

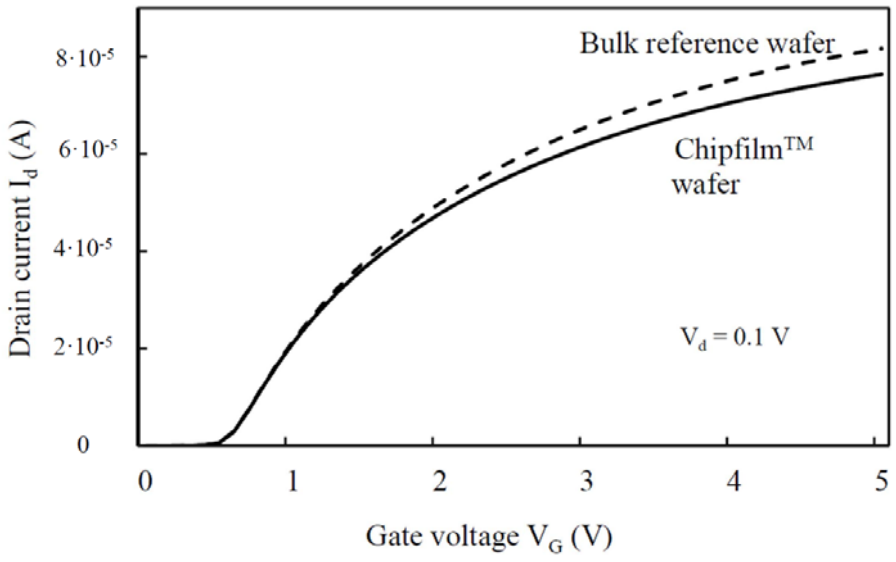
After the initial on-wafer measurements, the chips are detached from the wafers and assembled on different carrier substrates for further characterization of the device. The process of chip extraction from the wafer is mentioned in Chapter 4. Measurements are performed for chips in both flat and bending conditions. These measurements are carried out through manual probing by using an Agilent E5270B parametric precision measurement system.

6.1 On-wafer measurements

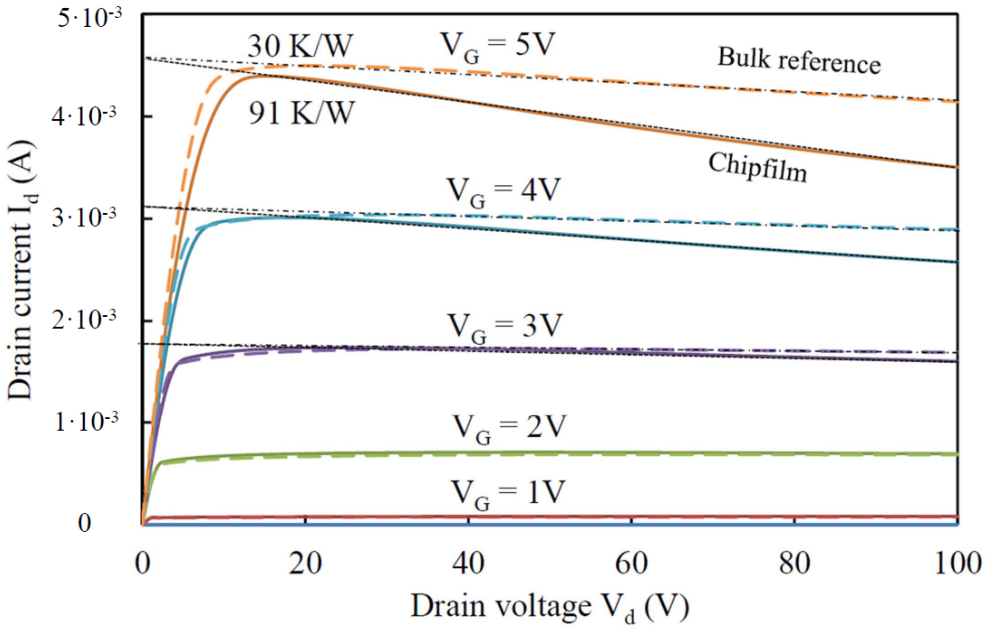
On-wafer measurements of the input and output characteristics, as well as the off-state breakdown voltage, are performed for both Chipfilm^{TM} and bulk reference wafer. The measured input and output characteristics of NLDMOS for both Chipfilm™ and bulk reference cases are shown in figure 6.1. These DC characteristics are measured for NLDMOS with a channel length of 9 µm and a channel width of 50 µm. The total length of drift region is 20 µm with a gate field-plate length of 10 µm. The average of extracted values of mobility and threshold for NLDMOS on a Chipfilm^{TM} wafer are 467 cm^2/Vs and 0.51 V respectively, whereas the I_{ON} to I_{OFF} ratio (I_{ON}/I_{OFF}) is greater than 10^7.

The output characteristics, figure 6.1(b), show that the drain current decreases significantly with the rising drain voltage. The reduction rate increases for higher gate voltage. This drain current decay is due to self-heating which is a direct consequence of limited power dissipation in the device on wafer. The self-heating is higher in the case of Chipfilm^{TM} than for a bulk reference wafer, which is indicated by the difference in the negative slope of the output characteristics in the saturation region. The difference in the self-heating on both wafers arises due to the presence of cavities in the Chipfilm^{TM} wafers

between the epi-layer and bulk wafers. These cavities hinder the thermal flow into the bulk, thus resulting into an increased thermal resistance.



a)



b)

Figure 6.1: Characteristics of NLDMOS for the Chipfilm™ wafer and the bulk reference wafer: a) Input characteristics; b) output characteristics.

In order to extract the thermal resistances from output characteristics we have used the relationship given in [27].

$$V_d = \frac{I_d}{R_{th} I_d}\left[\left(\frac{I_d}{I_{d0}}\right)^{-1/\alpha} - 1\right] \qquad (6.1)$$

where R_{th} is the thermal resistance and $\alpha \approx 2.5$ is a constant which characterizes the mobility change with temperature. By applying fitting lines to the output characteristics, we yield R_{th}. In case of bulk reference wafer, R_{th} comes out to be 30 K/W whereas for the Chipfilm™ case it is 91 K/W, which is almost 3 times higher than for the bulk reference case.

Figure 6.2 shows the off-state breakdown voltage for NLDMOS on both Chipfilm™ and bulk reference wafers. The measured breakdown voltage ranges between 110 V to 120 V, which is well above the intended 100 V. It can be seen that the off-state breakdown voltage is almost the same for both Chipfilm™ wafer and bulk reference wafer. Obviously, in Chipfilm™ technology LDMOS on ultra-thin chips can be obtained easily without compromising device performance.

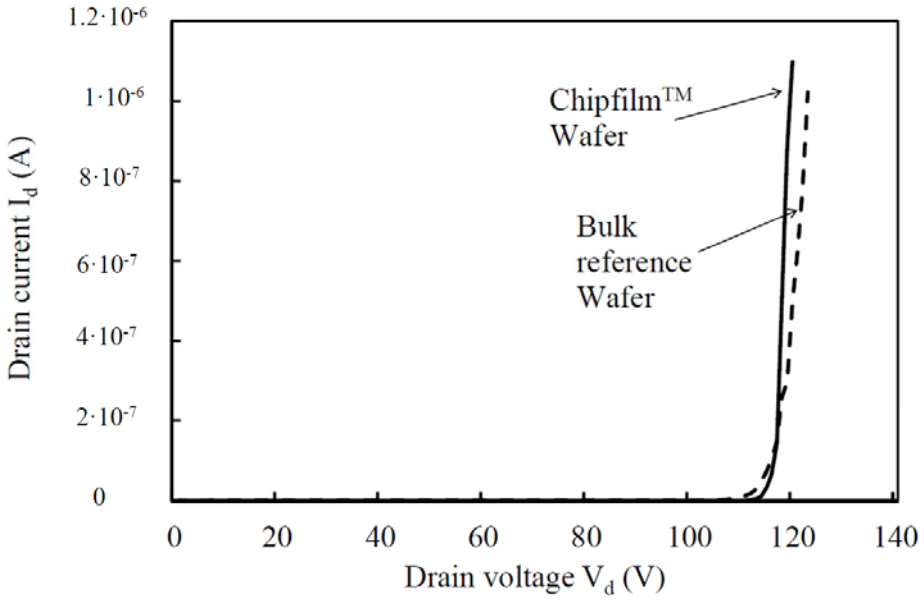
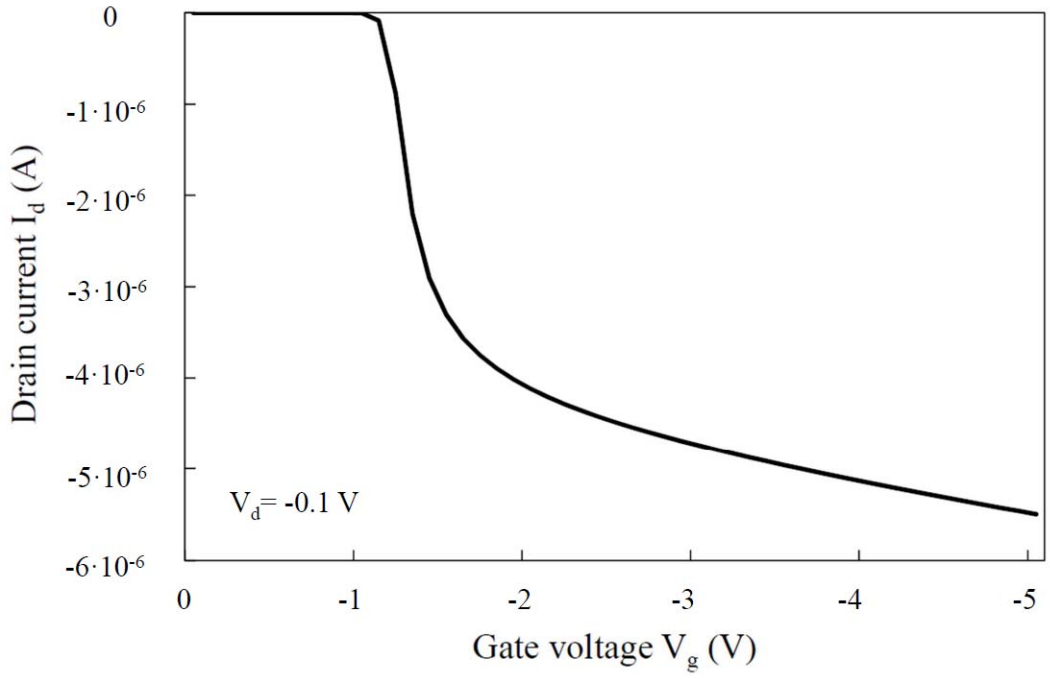
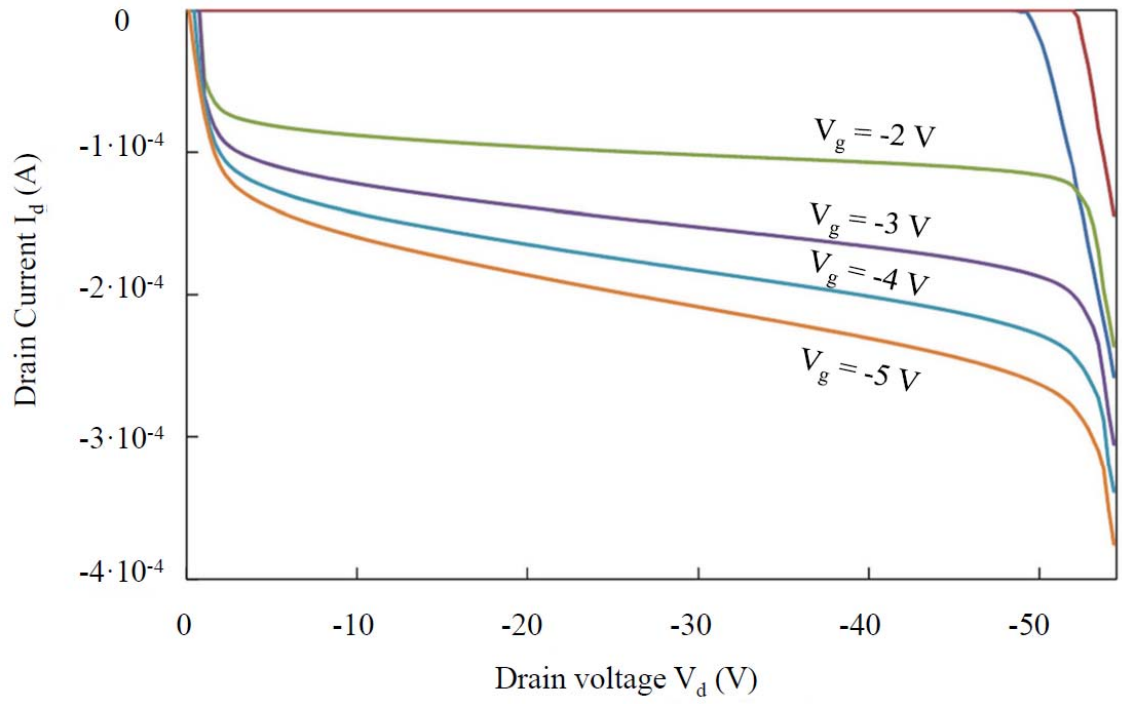


Figure 6.2: Off-state breakdown voltage NLDMOS on Chipfilm™ and bulk reference wafer.

The input and output characteristics of the PLDMOS on bulk reference wafer are shown in figure 6.3.



a)



b)

Figure 6.3: **DC characteristics of PLDMOS on bulk reference wafer.**

a) Input characteristics b) output characteristics.

The extracted values of mobility and threshold voltage are 132 cm^2/Vs and 1.12 V, respectively. The measurements of the PLDMOS transistors on ultra-thin chips have shown that on the bulk reference wafers, PLDMOS transistors have a breakdown voltage of about 50 V with a very low drain current value of 0.26 mA. These characteristics are measured for PLDMOS having channel length 9 μm and channel width of 100 μm. The lengths of the drift region and gate field-plate are the same as in case of the NLDMOS transistor. The *n*-well implant dose is $4 \cdot 10^{12}$ cm^{-2} and the background concentration of Boron is $1 \cdot 10^{15}$ cm^{-3}. On Chipfilm™ wafers the PLDMOS failed to show a functional transistor. The reason for this failure is attributed to the process variations beyond the limits of parameter variations allowed for the PLDMOS. As discussed in the previous chapter, the characteristics of the ultra-thin PLDMOS are more sensitive to the variation in optimized values as compared to the NLDMOS. It can maintain its proper characteristics and functionality only for a small variation in implant doses, implant energy and trench depth and suffers significantly if the values of these parameters fall outside these narrow limits.

In order to see the effect of substrate bias on the device threshold voltage, input characteristics of both the NLDMOS and PLDMOS are measured for three substrate biases:

for NLDMOS; $V_b = 0,-0.5,-1$;

for PLDMOS; $V_b = 0, 0.5,1$.

Figure 6.4 shows the measurement results for the NLDMOS. The results are according to expectations; the threshold voltage is increased with the decrease in bulk voltage and for higher gate voltages the drain current is almost the same.

The effect of substrate bias on the input characteristics of the PLDMOS on bulk reference wafers is shown in figure 6.5. It can be seen that the threshold voltage increases with an increase of substrate bias. The results however show a significant decrease in the magnitude of the drain current. This decrease in the drain current with the bulk voltage is an anomalous behavior, which do not exist in conventional high-voltage PLDMOS transistors.

The characteristics of the PLDMOS on the bulk reference wafers indicate that both the channel region and the drift region have been formed properly.

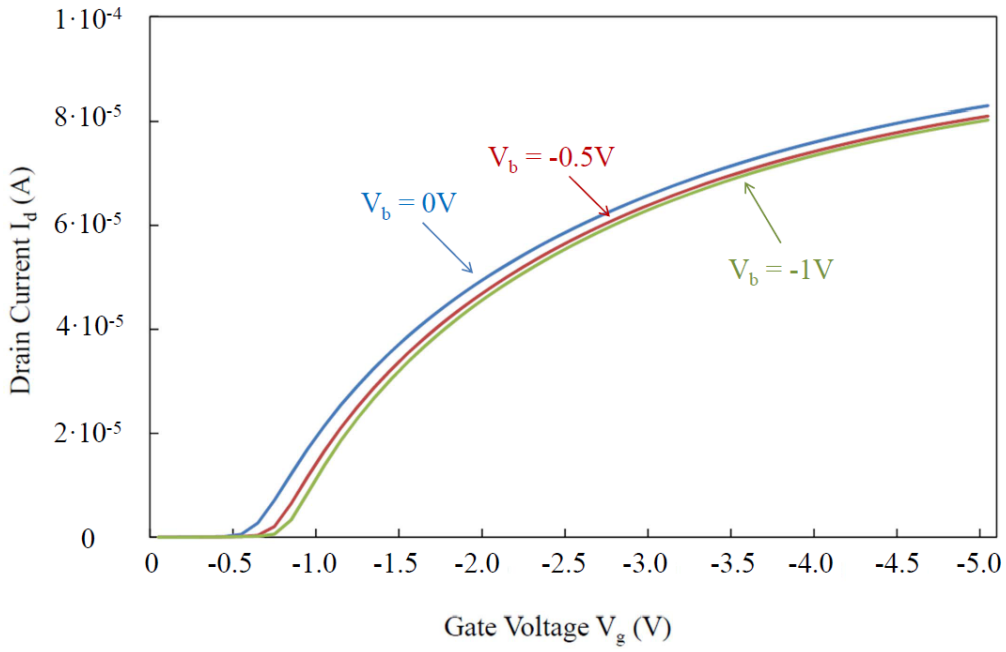


Figure 6.4: **Effect of substrate bias on threshold voltage for the NLDMOS.**

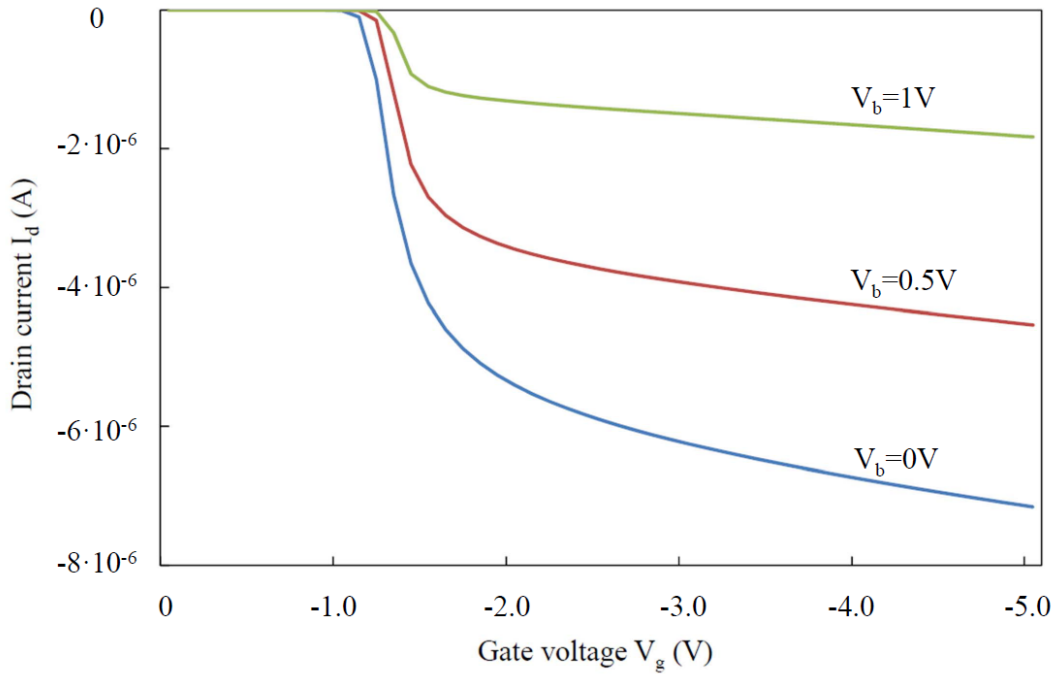


Figure 6.5: **Effect of substrate bias on threshold voltage for the PLDMOS on a bulk reference wafer.**

But, because the drift implant has been performed at lower implant energy and the trench formation has gone deeper into the silicon than expected, the drift resistance increases

resulting into a very low drain current. The support for this argument comes from the fact that for a higher dose of $6 \cdot 10^{12}$ cm^{-2} for the *n*-well, the device ceases to show proper transistor functionality on the bulk reference wafer. This shows that the drift region which was formed in case of *n*-well dose of $4 \cdot 10^{12}$ cm^{-2} is on the brink of vanishing, and it vanishes when the *n*-well dose is increased. On Chipfilm^{TM} wafers, an additional variation occurs, which is not present in case of the bulk reference wafers. The variation was the growth of oxide layer from 15 nm to 100 nm during the well drive-in step. This 100 nm oxide layer, through which the drift implant was arranged, helped in restricting the boron dose to the formation of a shallower depth when compared to the bulk reference wafer. This relatively shallower boron-doped region is then easily etched off during the over-etching in the trench formation process. That is why the drift region failed to form properly on Chipfilm^{TM} wafers for all *n*-well doses, including those for which device operation was observed on the bulk reference wafers.

All these observations support the argument that the drift region which is formed in the case of an *n*-well dose of $4 \cdot 10^{12}$ cm^{-2} is very thin. So, when we apply a substrate bias, it widens the depletion region into that thin drift region and covers a large percentage of its available area. This hinders the flow of current significantly and results in the anomalous behavior that is shown in figure 6.5. In case of the ultra-thin NLDMOS and other conventional LDMOS we do not see this effect because in those cases the drift region is thick enough, so that the depletion region is spread only over a small fraction of the junction. That is why a small variation in the depletion region width has no noticeable effect on the drain current in those devices.

The effect of *n*-drift dose in NLDMOS on Chipfilm^{TM} wafers is shown in figure 6.6. The results correspond to a gate voltage of 5 V. Higher impurity concentration in the drift region lowers the drift resistance, which results in an increase in drain current. One can notice this trend of increasing drain current with higher drift implant dose in figure 6.6. However, the amount of change is not significant as it lies within a process variation of ±10%. The epi concentration is mentioned to be intrinsic in figure 6.6 because the epilayer growth was intended to be intrinsic. The amount of Boron incorporated into the epitaxial layer during epitaxial growth and drive-in steps, i.e. the amount of boron auto doping, is not accurately known. The boron auto doping is estimated to be in the range of $1 \cdot 10^{15}$ cm^{-3} to $3 \cdot 10^{15}$ cm^{-3}. The effect of *n*-drift dose on bulk reference wafers under various scenarios is shown in figure 6.7.

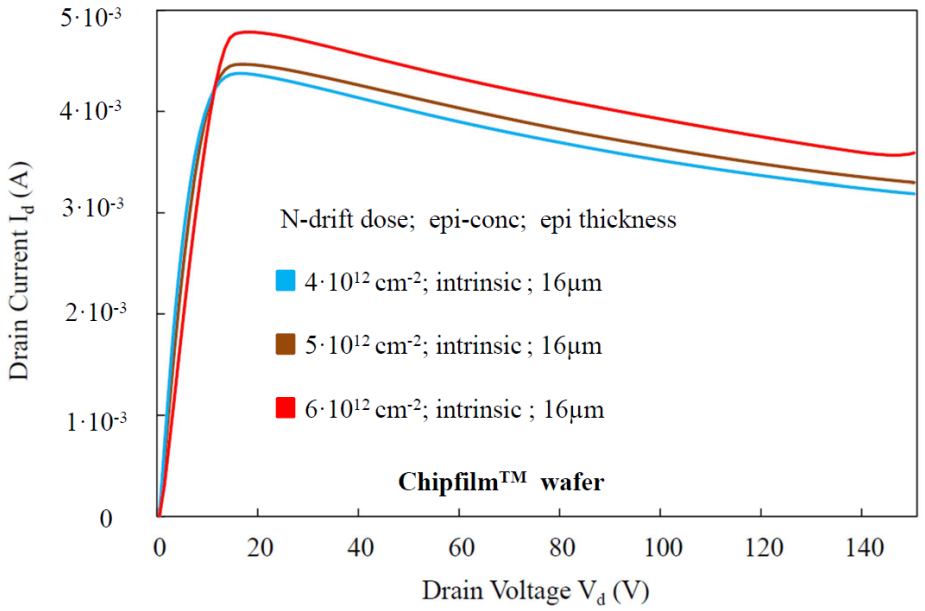


Figure 6.6: Effect of *n*-drift dose on drain current of NLDMOS for V_g= 5 V on Chipfilm™ wafers.

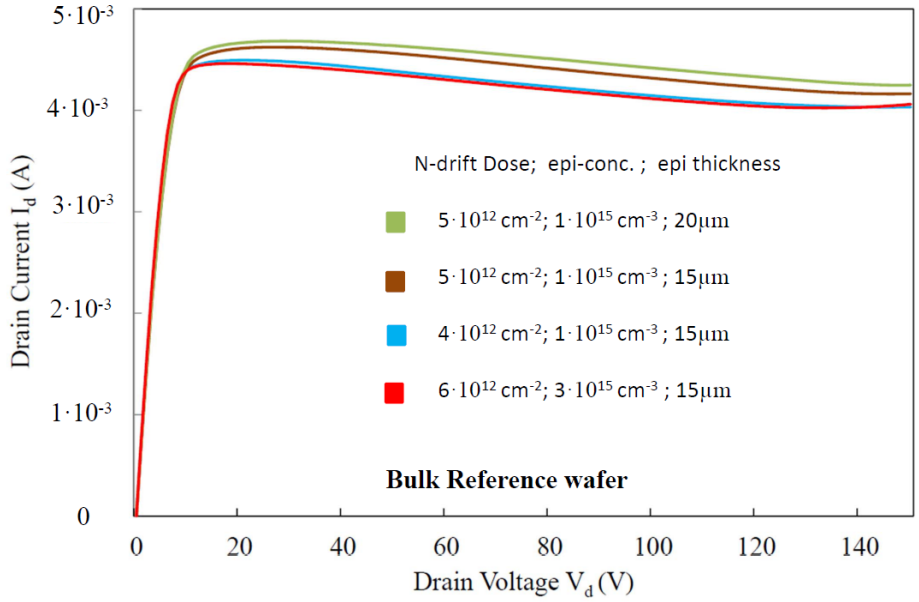


Figure 6.7: Effect of *n*-drift dose, epi-layer concentration on drain current of NLDMOS for V_g= 5 V in case of bulk reference wafers.

Here we can see the similar small variations in the drain current with changes in the phosphorous implant dose. Again, as the variation lies in the range of measurement uncertainty and process variation, it does not constitute a conclusive evidence of the effect

of *n*-drift dose variation. Figure 6.7, however, shows that an increase in both the epi-layer concentration to $3 \cdot 10^{15}$ cm^{-3} and the *n*-drift dose to $6 \cdot 10^{12}$ cm^{-2} results in a reduced drain current compared to the dose of $5 \cdot 10^{12}$ cm^{-2} for an epi-layer concentration of $1 \cdot 10^{15}$ cm^{-3}.

In figure 6.8, a comparison of the off-state breakdown voltages is presented. The values are the average of data taken from more than 20 transistors. The comparison between similar *n*-drift doses applied to both Chipfilm™ wafers and bulk reference wafers. The epi-layer thickness is in the range of 15–16 µm for all cases. The graph shows that for the *n*-drift region dose of $4 \cdot 10^{12}$ cm^{-2} the breakdown voltage is almost the same in both cases. With the increase of the *n*-drift dose to $5 \cdot 10^{12}$ cm^{-2}, the breakdown voltage decreases in both cases, though the rate of decrease is higher for the bulk reference wafer than for the Chipfilm™ wafer. For the *n*-drift dose of $6 \cdot 10^{12}$ cm^{-2}, the breakdown voltage for Chipfilm™ falls to less than 60 volts, while for the bulk reference case it raises again to about 100 volts. This difference is because all the Chipfilm™ wafers have the same concentration of Boron in the epi-layer and only the *n*-drift dose is increasing whereas in the bulk reference case the epi-concentration has also increased to $3 \cdot 10^{15}$ cm^{-3} in the case of the $6 \cdot 10^{12}$ cm^{-2} drift dose. This suggests that in order to achieve a breakdown voltage of 100 volt in ultra-thin LDMOS transistors, there exist more than one set of optimized values.

This effect of variation in breakdown voltage due to the combination of *n*-drift dose and substrate concentration is simulated in Atlas. The simulated result for the scenarios of different substrate concentrations and *n*-drift implant doses is also shown in figure 6.8. The solid line shows the case when the substrate concentration is kept constant at $1 \cdot 10^{15}$ cm^{-3} and only the *n*-drift dose is increased. One can see that the breakdown voltage decreases with increase in the *n*-drift implant dose. This behavior is similar to the Chipfilm™ case, as both have constant substrate concentration and the breakdown curve follows the same trend. When the substrate concentration is increased in the simulation to $3 \cdot 10^{15}$ cm^{-3} for *n*-drift dose of $6 \cdot 10^{12}$ cm^{-2}, the breakdown voltage has increased and the curve now follows the trend of the bulk reference wafer. This shows that the breakdown voltage is strongly dependent on the combination of substrate concentration and *n*-drift dose. This also indicates that the substrate concentration in Chipfilm™ wafers lies somewhere between $1 \cdot 10^{15}$ cm^{-3} and $3 \cdot 10^{15}$ cm^{-3}.

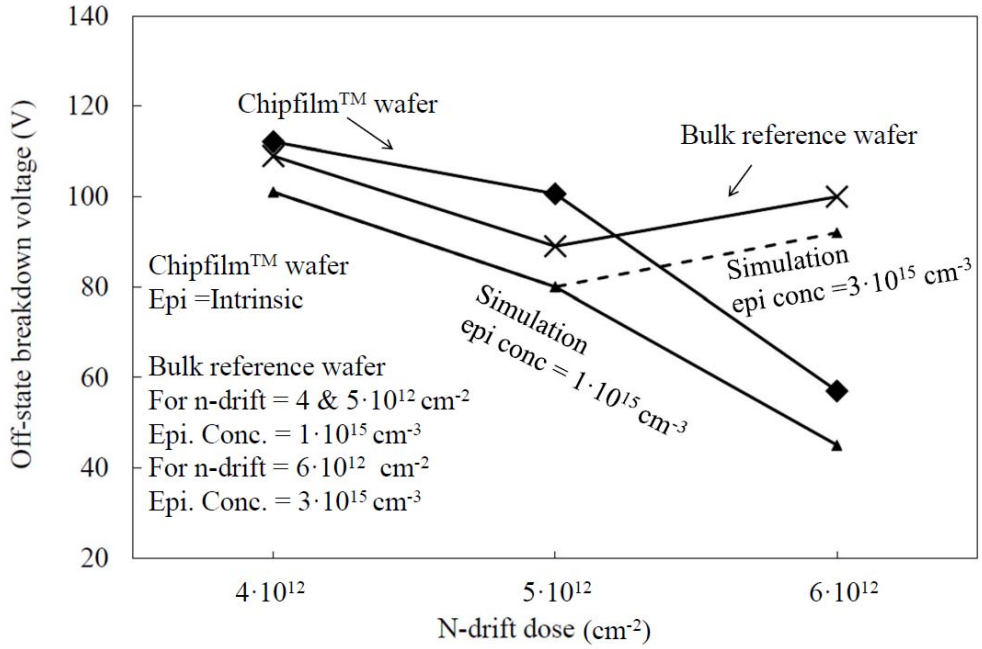


Figure 6.8: Comparison of off-state breakdown voltages between NLDMOS on Chipfilm™ wafers and bulk reference wafers.

6.2 Measurements on different carrier substrates

In order to determine the performance of NLDMOS in various scenarios, after performing initial on-wafer measurements, the chips are assembled on different carrier substrates. The chips are detached from the wafer by using the Pick, Crack & Place™ technique and assembled on a polyimide (PI) foil, a 24-pin dual in-line ceramic package (DIP24), and on a carrier Si wafer.

The output characteristics for the three assembly cases are shown in figure 6.9. These measurements correspond to the same channel length and width as for the initial on-wafer measurements. The effect of self-heating is prominent at high drain voltages and it increases for substrates with higher thermal resistances with a maximum degree for polyimide (PI) foil.

The thermal resistances in these cases are extracted from the output characteristics using equation 6.1 taken from [27]. Fitting lines are applied to the output characteristics, in the same fashion as in figure 6.1b, which yield R_{th}. Table I shows the drain current reduction due to self heating and the extracted R_{th} values.

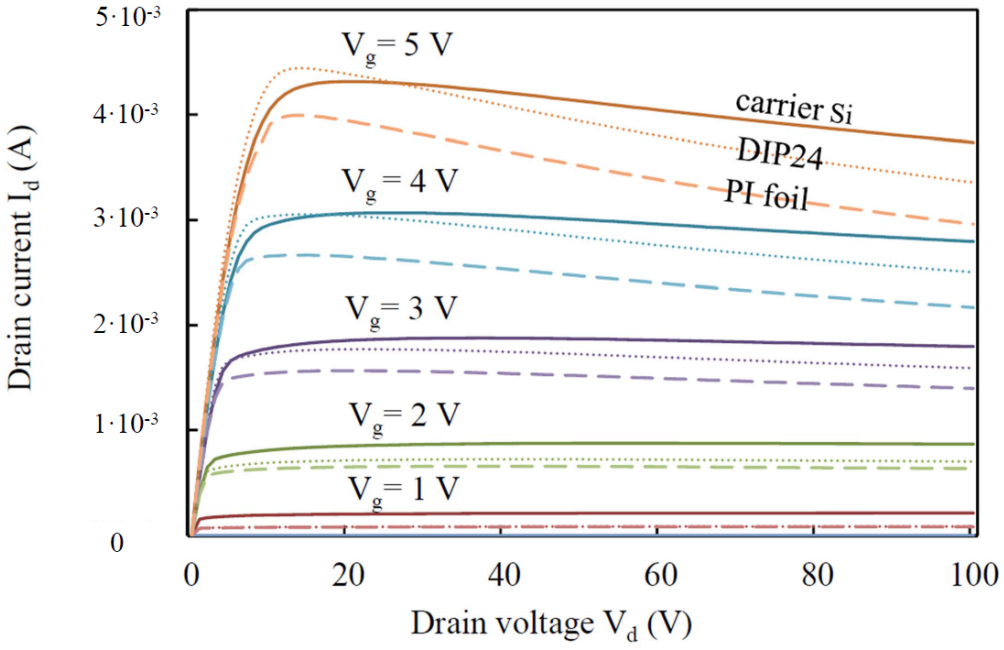


Figure 6.9 : Comparison of output characteristics of NLDMOS for chips assembled on Silicon wafer, in package and on PI foil.

TABLE 6.1: Percentage reductions in NLDMOS drain current and extracted thermal resistances for chip in various scenarios. Extracted values could vary in the range of ±10%

Cases	$(I_d-I_{d0})/I_{d0}$ $(V_{ds}=100\ V)$	R_{th} (K/W)	$\Delta T=P\cdot R_{th}$ (^{O}K)
Bulk reference	10 %	30	13
Chipfilm™ wafer	24 %	91	32
Chip on Si carrier	19 %	60	22
Chip in DIP24	27 %	113	38
Chip on PI foil	35 %	135	40

In figure 6.10, relative reductions in the drain currents compared to the maximum drain currents are illustrated for the different assembly cases. Evidently, assembly on foil results in the highest R_{th} value and thus the highest reduction in drain current.

Figure 6.11 shows the variation in drain current and junction temperature with the change in channel length. The drain current and the thermal resistance show a similar dependence on channel length as both of them increase with decrease in channel length. As most of the heat generation occurs in the drift region a variation of channel length does not change R_{th} significantly. This results into a higher degree of self-heating. An improvement in transistor on-resistance (R_{on}) is therefore necessary to deal with self-heating issues. Optimum channel lengths together with an increase of the transistor active area will help to minimize self-heating.

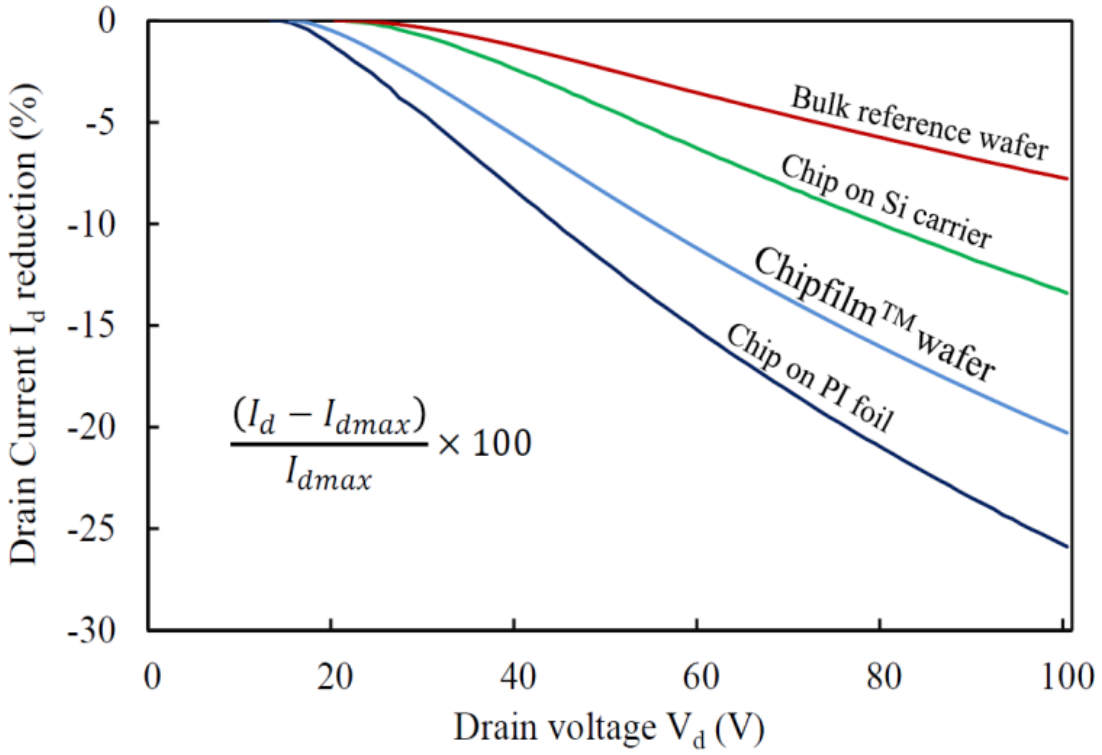


Figure 6.10: Comparison of self-heating effect on maximum drain current (I_{dmax}) for V_{ds} up to 100 volts.

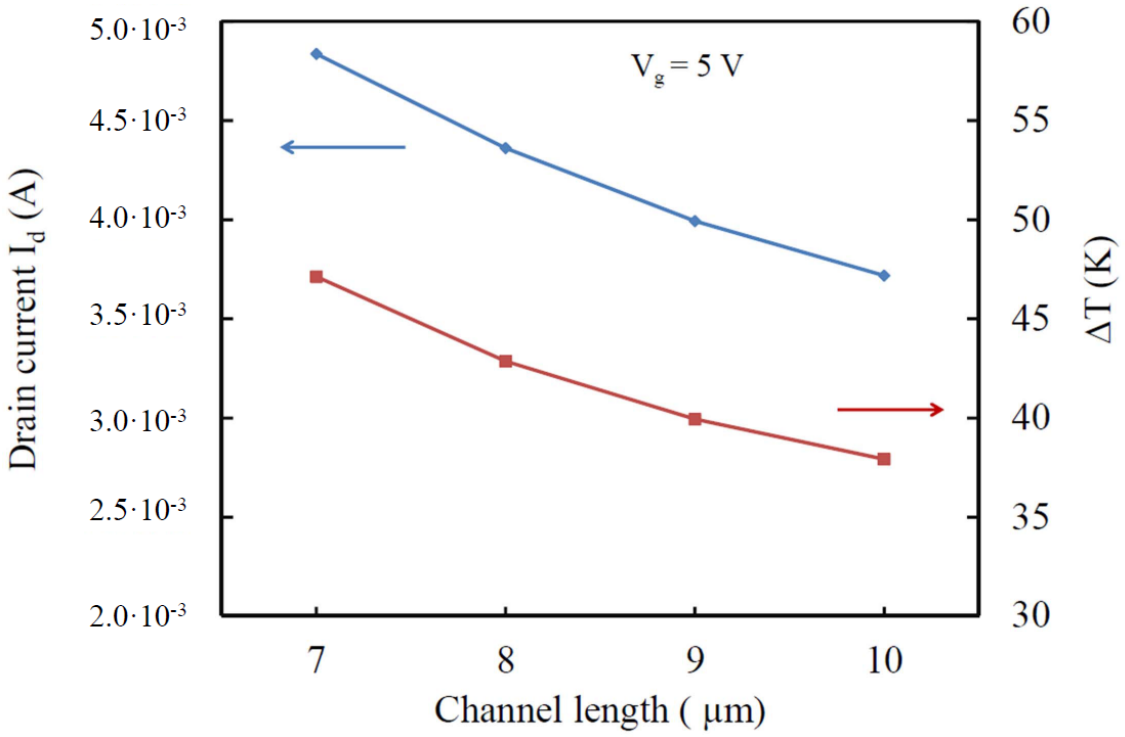


Figure 6.11: Effect of channel length variation on maximum drain current and temperature rise due to self- heating.

6.3 Measurements of chip in bend state

Ultra-thin chips are meant for use in mechanically flexible products where they have to sustain mechanical stresses while maintaining their electrical performance. Under bending conditions the piezoresistive effect affects the carrier mobility and, thus, the drain current. In order to determine the effects of mechanical stress on ultra-thin NLDMOS, the chips are assembled on 50 µm thick polyimide foil. Electrical connections are made through wire bonding. The photograph of one of the measured chips on polyimide (PI) foil under bending condition is shown in figure 6.12. The apparatus used for chip bending is shown in figure 6.13. Here, the chip is under bending stress at a bending radius of 7.5 mm. Cylinders with different radii that are used in experiment are placed in front of the apparatus.

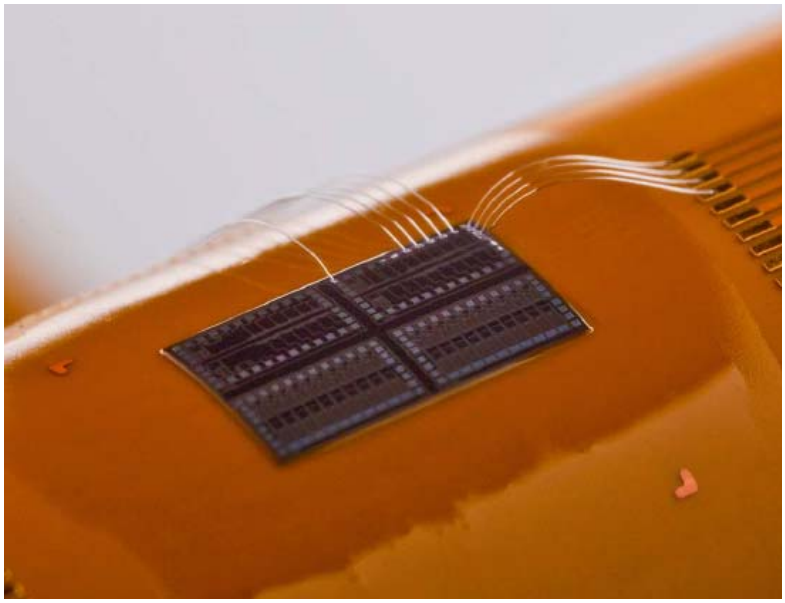


Figure 6.12: Photograph of the fabricated ultra-thin (< 20 µm) high-voltage NLDMOS chip on PI foil.

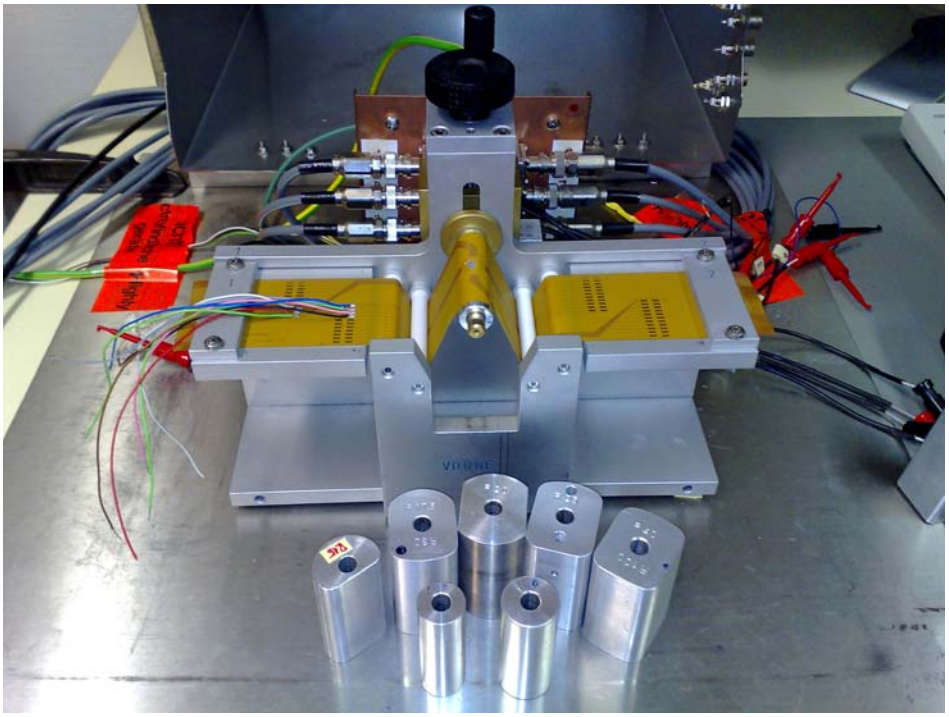


Figure 6.13: Photograph of the apparatus used for chip bending.

The measurements are performed for radii ranging from 100 mm to 7.5 mm. Mechanical stresses are applied either in the direction of channel length [110] (longitudinal stress) or perpendicular to its direction [$\bar{1}$10] (transverse stress). The relevant orientations are shown in figure 6.14.

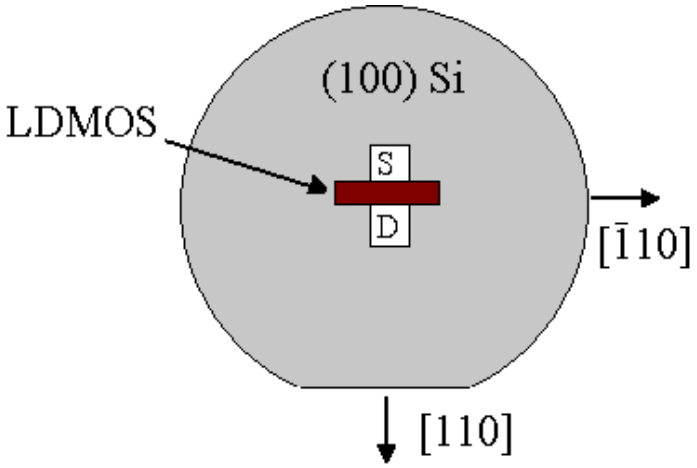


Figure 6.14: Stress directions on LDMOS.

The characteristics are measured for different bending radii ranging from 100 mm to 7.5 mm. The amount of stress that appeared at the surface for each bending radius is calculated by taking into consideration the thicknesses and the Young's modulus of PI-foil, glue and silicon chip. The system is according to figure 6.15.

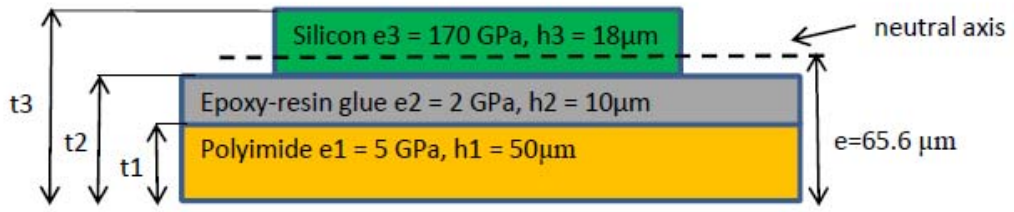


Figure 6.15: System considerations for calculation of stress on ultra-thin chips glued onto polyimide (PI) foil

In order to determine the location of neutral plane, we use the following relation taken from [116].

$$e = \frac{e1h1(t1) + e2h2(t2 + t1) + e3h3(t3 + t2)}{2(e1h1 + e2h2 + e3h3)} \tag{6.2}$$

where

e1 = Young's modulus of polyimide

e2 = Young's modulus of epoxy resin

e3 Young's modulus of Silicon

The strain at the top surface is given by;

$$E^{top} = \frac{h1 + h2 + h3 - e}{R + e} \tag{6.3}$$

where

R = bending radius.

From equations 6.2 and 6.3, the stress value at top surface for each bending radius can be calculated as:

$$\sigma^{top} = e3 \times E^{top} \tag{6.4}$$

Stress values corresponding to different bending radii used in this experiment are shown in figure 6.16.

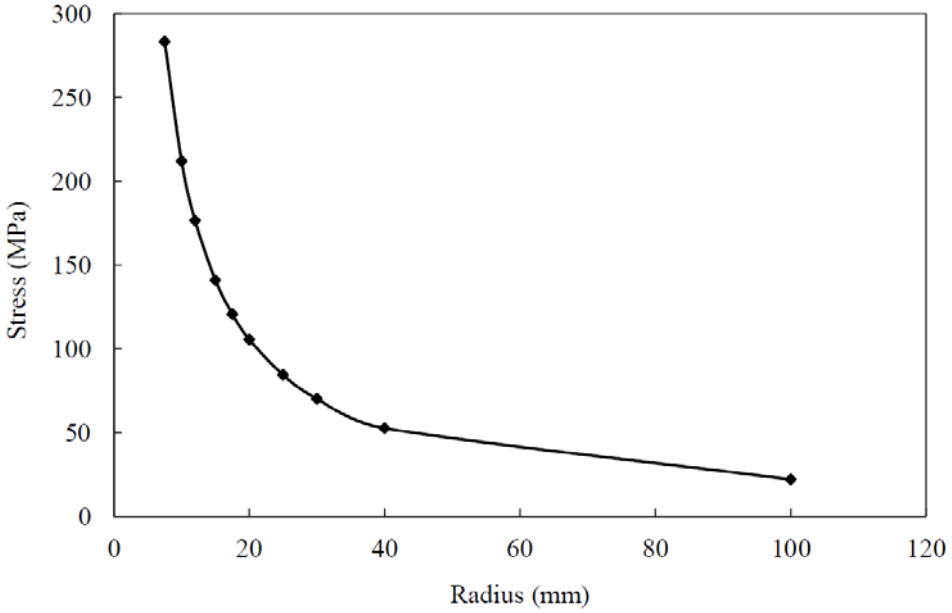


Figure 6.16: Stress values corresponding to bending radius.

Measurements show that in case of longitudinal stress applied on the NLDMOS in [110] direction, the drain current increases with decrease in radius. Figure 6.17 shows the behaviour of the NLDMOS under longitudinal stress with drain voltage as a parameter. The plot relates 1/R to the normalized drain current for a drain voltage of 14 V, where R is the bending radius. Because of unknown initial stress on chip and its dependence on process history, the data is normalized to 100 mm radius instead of the apparent flat state. The data is then shifted upwards by 0.01 to compensate the difference between 100 mm radius and flat case. For bending radii from 100 mm to 7.5 mm the drain current increases by about 6–7 %. The rate of increase in drain current due to bending, however, reduces at higher drain voltages. ASAKAWA [27] has attributed this effect to the temperature dependence of the piezoresistive coefficients, as piezoresistance increases with temperature. The channel length in this case is 9 µm, drift length is 20 µm and *n*-drift implant dose is $4 \cdot 10^{12}$ cm^{-2}.

The device under transverse stress shows a similar increase in drain current with decreasing bending radius. However, the change in current is less than in the case of longitudinal stress. Figure 6.18 shows the normalized change in drain current versus 1/R, where R is the bending radius.

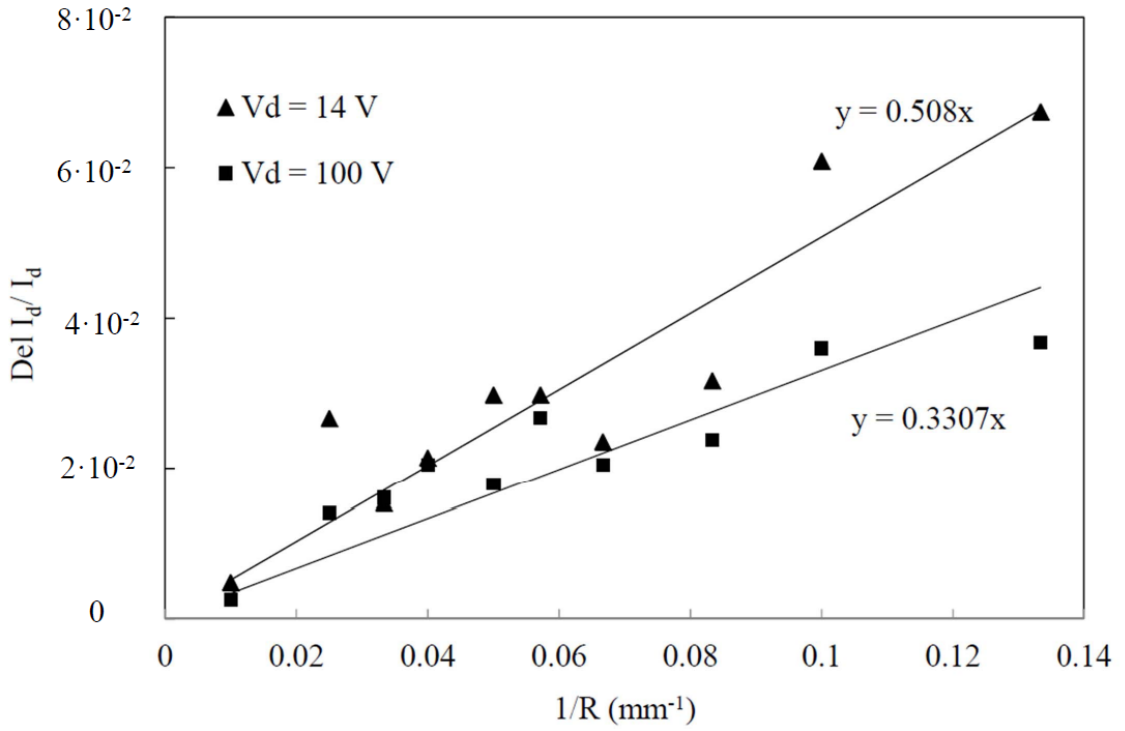


Figure 6.17: Change in drain current with bending radius for NLDMOS at drain voltages of 14 V and 100 V (longitudinal stress)

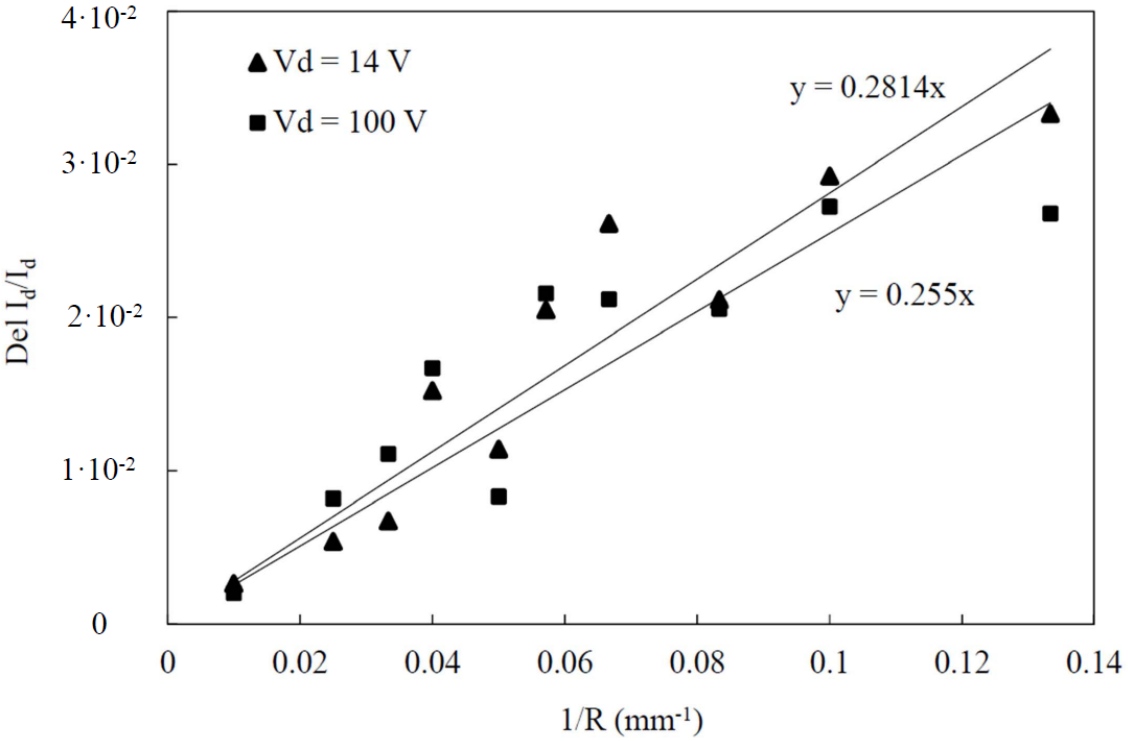


Figure 6.18: Dependence of current change on bending radius at different drain voltages (transverse stress).

From the measurements the piezoresistive coefficients are calculated using the relationships taken from [116]

$$\pi_S = \pi_L + \pi_T \tag{6.5}$$

$$\pi_{44} = \pi_L - \pi_T \tag{6.6}$$

$$\pi_L = \pi_{11} + \pi_{12} \tag{6.7}$$

$$\pi_T = \pi_{11} - \pi_{12} \tag{6.8}$$

Where π_{11} and π_{12} and π_{44} are the fundamental piezoresistance coefficients. π_S is a linear combination of π_{11}, π_{12} and π_{44}. π_L and π_T are the longitudinal and transversal coefficients respectively, and are determined by the slope of the curve. Table 6.2 shows the values of piezoresistive coefficients based on measured data at V_d = 14 V.

Table 6.2: Piezoresistive coefficients for ultra-thin NLDMOS at V_d = 14 V

Coefficients	Value ($x10^{-12}$ pa^{-1}) ±50%
π_L	510
π_T	280
π_S	790
π_{44}	230

Figure 6.19 shows the variation in longitudinal stress induced current change (stress sensitivity) with change in gate voltage. The curves are drawn for three drain voltages 1 V (linear region), 14 V (saturation point) and 100 V (targeted voltage).

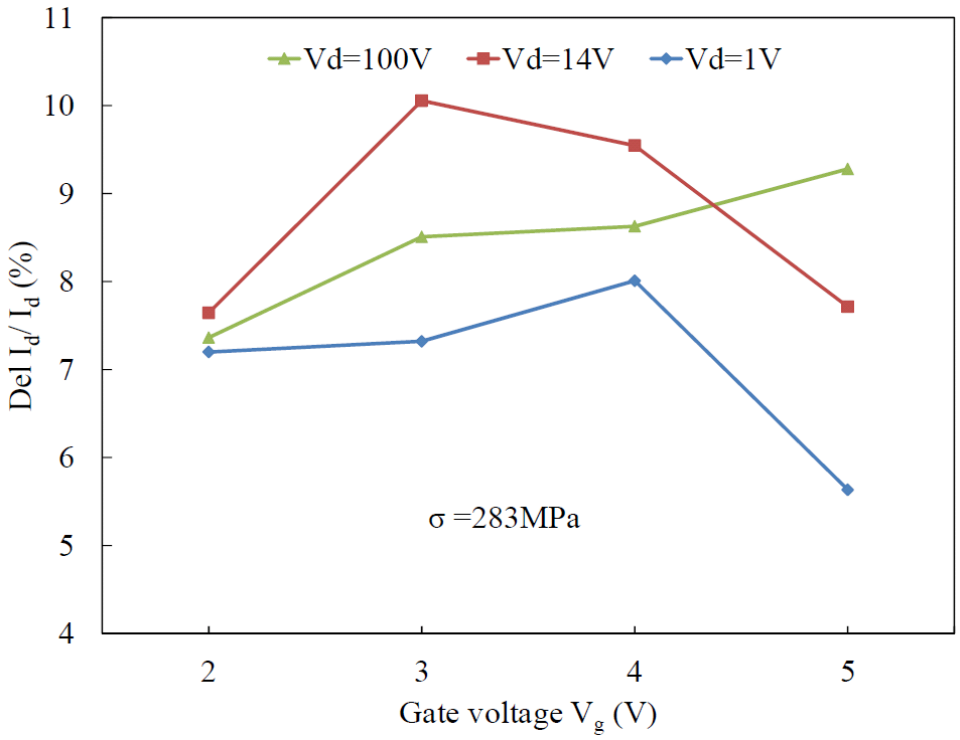


Figure 6.19: Dependence of change in drain current with gate voltage in linear and saturation regime. The data correspond to the bending radius of 7.5 mm (σ = 283 MPa).

It can bee seen that in the linear region the stress sensitivity increases up to V_g= 4V, after which it starts decreasing. Similar to that is the behaviour of stress sensitivity for V_d=14 V, but in this case it starts decreasing after V_g= 3 V. At 100 V, however, the stress sensitivity keeps increasing almost linearly with gate voltage up to 5 V. This variation in the stress sensitivity with gate voltage is attributed to impact ionization [117]. In [118] it is shown that the substrate current I_{sub}, which is a direct measure of impact ionization, increases with gate voltage V_g and then decreases to a minimum value of generation and recombination current. The increase in substrate current is attributed to increase in drain current whereas the decrease is attributed to the impact ionization. It is also shown in [118] that the peak of I_{sub} and its termination both increase with the drain voltage. The similar behaviour we can observe in figure 6.19 where the peak of stress sensitivity and its termination increases for the drain voltages 1 V and 14 V. For the drain voltage of 100 V, the stress sensitivity values are less than those for drain voltage of 14 V. In [27], the reason for smaller change in drain current at high drain voltages is attributed to the increase in temperature due to self-heating. Piezoresistive coefficients have positive

dependence upon temperature which results into smaller change in drain current at high drain voltage.

6.4 Summary

This chapter presents the measurement results of ultra-thin LDMOS transistors on both Chipfilm™ and bulk reference wafers. The NLDMOS transistor works well on both types of substrates. It can sustain an electrical stress of 100 V with a current of about 4 – 5 mA for channel lengths ranging from 7 µm to 10 µm. The width in all cases is 50 µm. Lower than expected values of the drain current in NLDMOS suggest that background doping is raised to a level of more than $2 \cdot 10^{15}$ cm^{-3}. By normalizing the drain current values to channel width ($4–5 \cdot 10^{-3}$ A / 50 µm = $8 \cdot 10^{-5}–1 \cdot 10^{-4}$ A/µm) and comparing them with the simulation results shown in figure 5.12 of Chapter 5 it becomes clear that the drain current has the same values as for a substrate concentration of about $2–3 \cdot 10^{15}$ cm^{-3}. For NLDMOS, device characterization under bending stress has been performed. The change in drain current with longitudinal and transversal stress is in accordance with the behaviour of ordinary MOS transistors under stress. As the existing stress in the flat state is unknown and its value depends on the process induced stresses, the bending measurements are start with 100 mm radius, for which the stress values are well known.

The effect of bending on the breakdown voltage is insignificant. The small variations in breakdown voltage are likely due to process variations. A similar result is published in [119], where breakdown voltage changes of only 80 mV per 60 MPa stress are reported. This shows that for a stress difference of 300 MPa, the change in voltage is only 0.4 V, which is negligibly small for high-voltage devices.

For PLDMOS transistor, measurements are performed on bulk reference wafers only, as on Chipfilm™ wafers they do not function properly. On the bulk reference wafer the device operates to some extend but the breakdown voltage is only about 50 V and the current is limited to 0.2–0.3 mA. The width of the PLDMOS is 100 µm. The possible reasons that led to this failure of PLDMOS include

- Growth of oxide layer to 100 nm instead of 15 nm, through which *p*-drift implant is performed.
- Trench depth is 370–400 nm instead of 300 nm.

- *p*-drift Implantation energy = 110 keV, which is not enough to push the Boron atoms beyond the range of shallow trench. Most of the Boron resides in the area which is later on etched off during the trench formation.

All three factors support the argument that the implanted boron dose is etched off during the trench formation. Low implant energy and implantation through thicker oxide results in shallower junction depth in silicon than intended. The shallower junction depth is then totally removed by etching off the silicon during shallow trench formation up to a depth of about 400 nm.

In bulk reference wafers, the oxide thickness used for *p*-drift implantation is 15 nm. This is the only notable difference between the processing of the two lots. That is why we see some transistor action in PLDMOS devices in case of bulk reference wafers but not in case of Chipfilm^{TM} wafers.

The overall results validate the design of ultra-thin LDMOS transistors on Chipfilm^{TM} substrates. Improvements in transistor design are required, however, in order to increase the drain current of the NLDMOS and to decrease the sensitivity of the PLDMOS to process variations.

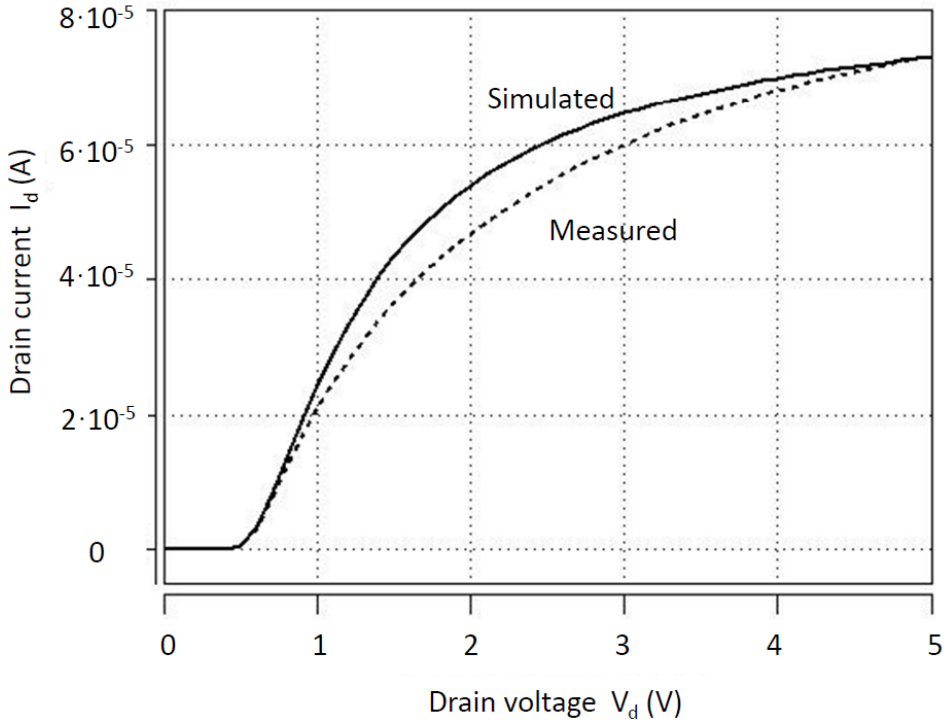
7 Ultra-thin high-voltage switch

In this chapter, the performance of the ultra-thin LDMOS transistors as a high-voltage switch for driver circuits of flexible displays is presented. In flexible displays, active matrix backplanes are driven by row and column drivers as explained in Chapter 4. Ultra-thin high-voltage LDMOS transistors are used as high-voltage switches in these drivers.

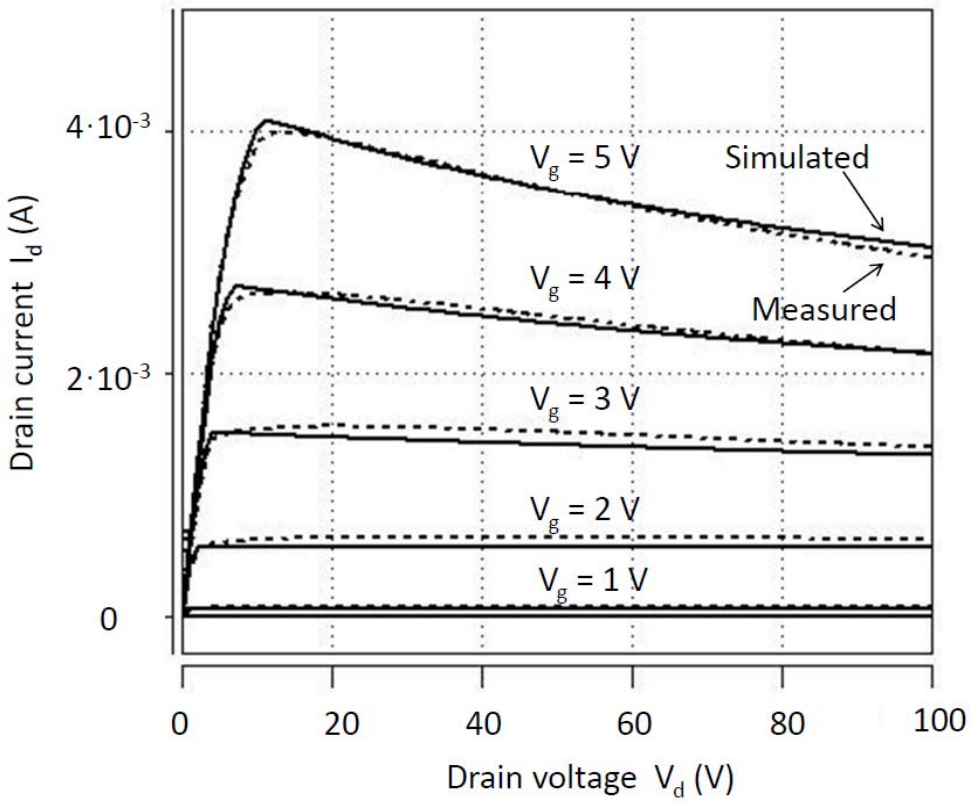
7.1 Parameters extraction

In order to employ the fabricated ultra-thin LDMOS transistor in a high-voltage switch, the various device parameters are extracted using HSPICE and ICCAP softwares. For high-voltage MOS devices, HSPICE make use of HiSIM model which accounts for various effects, such as quasi- saturation and self-heating. The model parameters for HiSIM Level 73 are used to simulate the characteristics of the ultra-thin LDMOS transistors. The matching of the measured input and output characteristics to simulations for both NLDMOS and PLDMOS transistors are shown in figure 7.1 and 7.2. The dotted lines are representing the measured data and the solid lines show the simulated characteristics.

In flexible electronics, the devices are assembled on plastic substrates which are thermal insulators. This hinders the heat dissipation and, thus, leads to raised junction temperatures well above the ambient temperature, which strongly affects the device performance. Taking this into consideration, the measured data used for the parameter extraction belongs to the case, in which the ultra-thin chips are placed onto polyimide (PI) foil. For a CMOS high-voltage switch, both NLDMOS and PLDMOS transistors are required. While measured data have been considered only for NLDMOS, which can operate up to 100 V, the data for PLDMOS are taken from device simulation in Atlas. The extracted parameters for both NLDMOS and PLDMOS are given in the Appendix.

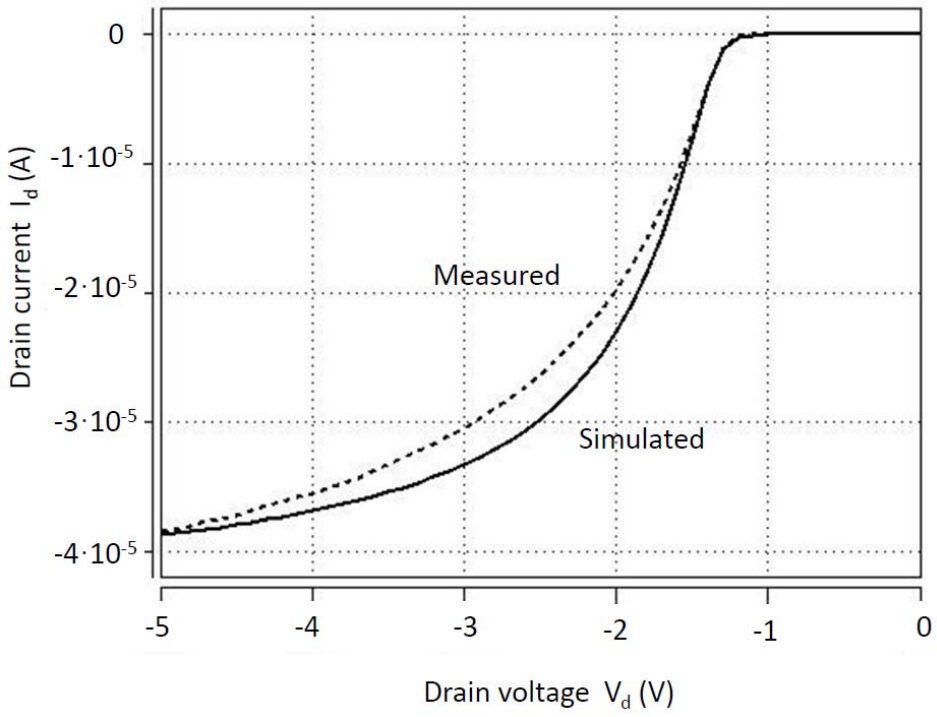


a)

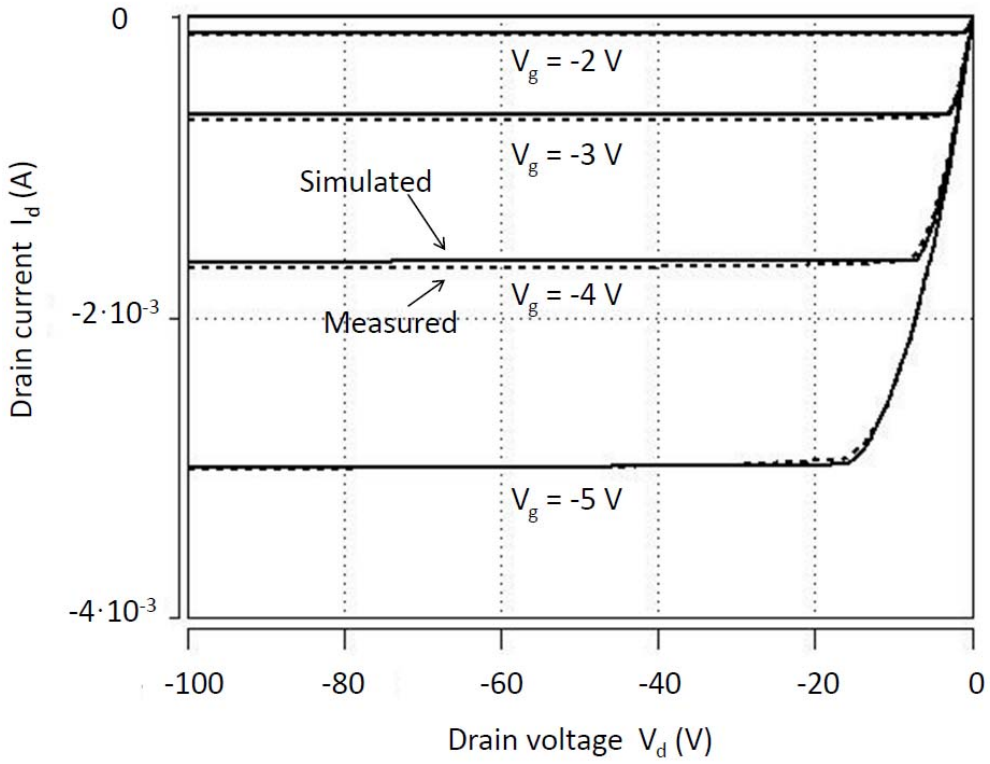


b)

Figure 7.1 Curves matching for I-V characteristics of NLDMOS a) input characteristic, b) output characteristics



a)



b)

Figure 7.2 Curves matching for I-V characteristics of PLDMOS a) input characteristic, b) output characteristics

7.2 Load estimation

In an active-matrix display, gate and source drivers are used to drive rows and columns of pixels. The number of pixels connected to a row or column line varies with display size and resolution. In the calculation of load we take the case of a 15-inch (diagonal) monochrome display (30.5 cm (width) x 22.9 cm (height)). The dimensions of a 15-inch diagonal display are almost the same as A4 size paper (29.7cm x 21 cm, landscape), which is widely used for practical reading. An aspect ratio of 4:3 is considered with a resolution of 1024 x 768 (XGA) in the estimation of the load conditions. From the display dimensions and resolution, the pixel size is calculated to be approximately 300 µm x 300 µm.

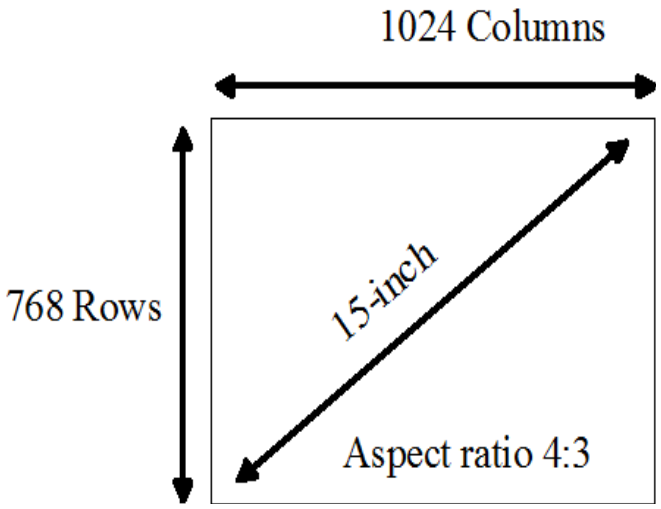


Figure 7.3 Display size and format considered for estimation of load

The row and column lines behave as a distributed resistance-capacitance (RC) network as shown in figure 7.4.

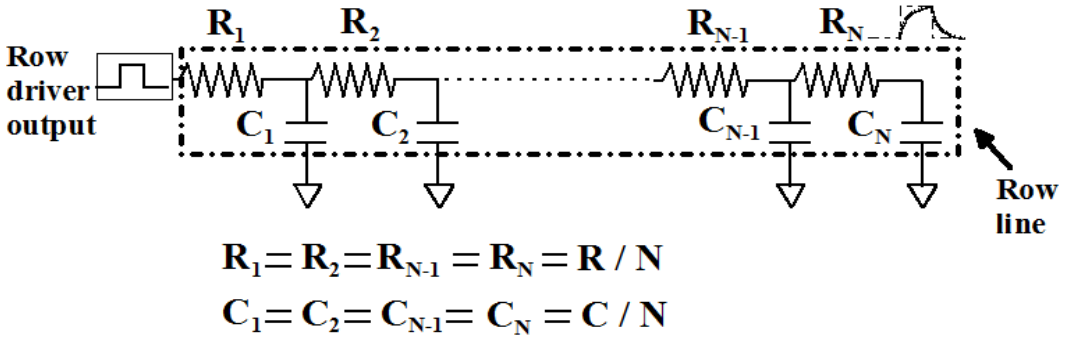


Figure 7.4: Distributed RC-network behaviour by row lines

In figure 7.4, the capacitances C_1, C_2….,C_N represent the net capacitance associated with each pixel in a row. All these individual capacitances are equal in value. Capacitance C is the sum of all individual pixel capacitances and represents the total capacitive load of a row line. R_1, R_2,…, R_N are the resistances associated with each pixel capacitance through which it has to charge and discharge. The capacitance nearest to the row driver output has to charge or discharge through resistance R1 only, whereas the last pixel capacitance in the row has to charge and discharge through all resistances R_1 to R_N. The row driver has to activate all pixels in a row simultaneously. Therefore the total load of the row line is the sum of all individual capacitances and individual resistances.

Each capacitance shown in figure 7.4 includes a contribution from

1. the gate capacitance of transistors in the pixel circuit;
2. the overlap capacitance of row and column lines.

In order to calculate the capacitance of each pixel we take the example of a general 2-TFT pixel circuit used as a driver in an OLED display.

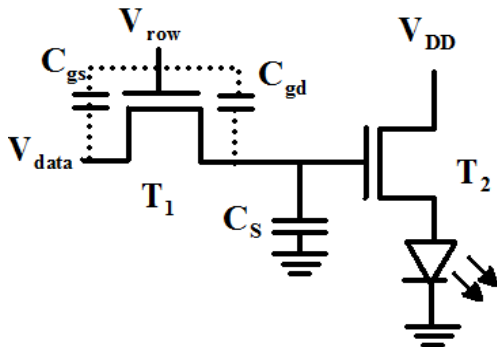


Figure 7.5: 2-TFT pixel circuit for OLED display.

In a single pixel, the row driver has to charge the gate capacitances of transistor T1. The capacitance offered by the transistor T1 is given is

$$C_{T1} = C_{gate} + C_{gs} + C_{gd} \qquad (7.1)$$

where

C_{gate} = Gate capacitance

C_{gs} = Gate-to-source overlap capacitance

C_{gd} = Gate-to-drain overlap capacitance

A set of sample values for these capacitances is taken from reference [120]. The values are

for transistor T1,

$C_{gs} = C_{gd} = 40$ fF ; $C_{gate} = 460$ fF,

and for transistor T2,

$C_{gs} = C_{gd} = 400$ fF ; $C_{gate} = 4.6$ pF.

The total capacitance of transistor T1 (C_{T1})is calculated to be

$$C_{T1} = 0.54 \text{ pF} \qquad (7.2)$$

The overlap capacitance between row line and column lines is dependent upon their thickness, separation, width and permittivity of the insulator used. Decrease in width and thickness of the conductor decreases the capacitance but increases the resistance and vice versa. The sample values used in this simulation are based upon the values of overlap capacitance between row-line and column line (290 pF) and resistance of row

line (4.6 kΩ) used by [104] for the simulation of a 15-inch display. These values in [104] were considered for a QXGA (2048 x 1536) format. Since the number of pixel in XGA format is half of that in the QXGA format, the overlap capacitance in our case is half to the one used in [104]. The resistance, however, remains the same as the length of row line is identical for both cases. The values we have used in this simulation for resistance and capacitance of the row line are

Resistance of row line (R_{row}) = 4.6 kΩ

Capacitance of row line (C_{row}) = 145 pF

The total capacitive load seen by the row driver output is given by the relation

$$C_{Total} = C_{row} + \left[\left(C_{gs}(T1) + C_{gd}(T1) + C_{gate}(T1)\right) \times n\right] \qquad (7.3)$$

where n = number of pixels in a row = 1024

Substituting the values yields the total capacitive load of 697 pF.

Contrary to the row driver, the column driver has to drive only one pixel at a time but has to charge all the gate-to-source capacitance (C_{gs}) of transistors T1 in a column. The overlap capacitance, however, remains almost the same. Using the same pixel circuit shown in figure 7.5, the total capacitance in this case is given as

$$C_{Total} = C_{column} + C_s + C_{gate}(T2) + C_{gs}(T2) + C_{gd}(T2) + \left[C_{gs}(T1) \times m\right] \qquad (7.4)$$

where

m = number of pixels in a column = 768

C_s = Storage capacitor

The value of the column line capacitance C_{column} is based on the value taken from [104],

C_{column} = 45 pF.

The storage capacitance is assumed to be 1 pF.

Substituting the values in equation 7.4 gives the total capacitance as seen by a column driver of 82 pF. The resistance of a column line is 3.5 kΩ. The values of the above mentioned parameters are listed in Table 7.1

Table 7.1: Simulation parameters

Parameter	Value	Unit
Display size	15	Inch
Aspect ratio	4 : 3	
Format	XGA (1024 x 768)	
Frame frequency	60	Hz
Pixel size	300 x 300	μm^2
C_{gate} *(T1)*	460	fF
C_{gs} *(T1)*	40	fF
C_{gd} *(T1)*	40	fF
C_{gate} *(T2)*	4.6	pF
C_{gs} *(T2)*	400	fF
C_{gd} *(T1)*	400	fF
Resistance row line	4.6	kΩ
Resistance column Line	3.5	kΩ
Overlap capacitance row line	145	pF
Overlap capacitance column line	45	pF
Pixel capacitance (row line)	550	pF
Pixel capacitance (column line)	37	pF
Storage Capacitance	1	pF
Total row capacitance	695	pF
Total column capacitance	82	pF

7.3 High-voltage switch simulation

For the switching circuit, complementary metal oxide semiconductor (CMOS) technology has been the choice for circuit design due to its low power consumption. A typical CMOS inverter circuit used as a switch consists of a PMOS and an NMOS transistor with their drain contacts connected to each other to form a common output terminal (figure 7.6).

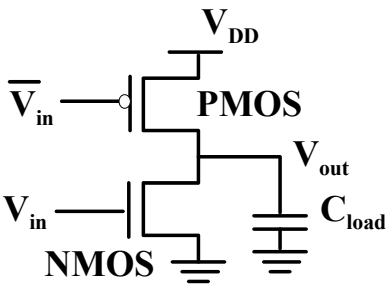


Figure 7.6: CMOS switch.

In low voltage applications (5 V or less) the gate terminal of both PMOS and NMOS are driven by a common input signal, directly applied to both transistors. In this case the value of V_{DD} is 5 V or less. In case of high-voltage displays a supply voltage (V_{DDH}) of several tens of volts is used. The bias levels at gate terminal of the PMOS transistor should stay between V_{DDH} and (V_{DDH} − 5 V) for proper operation. Therefore a level shifting circuit is applied between the input terminal and gate terminal of the PMOS (figure 7.7).

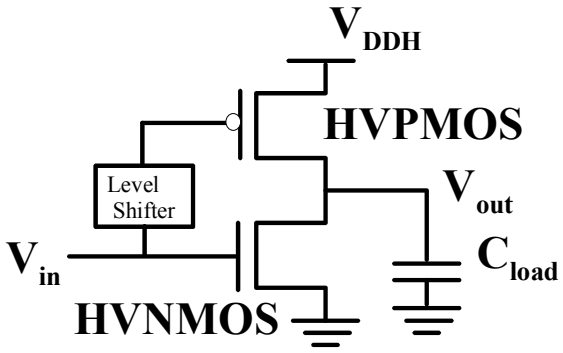


Figure 7.7: High-voltage switch with level-shifter.

In HSPICE simulation the level shifter circuit is not applied; instead, the required voltages are provided directly at the gate terminals. The simulation is performed for a maximum bias of 70 V. Two factors are taken into consideration for setting the high voltage reference level for the simulation. The first one is that normally thin-film transistors require a few ten volts for proper operation. One example is presented in [121] where the thin-film transistor receives 40 V of gate bias. The second factor is the application of negative gate bias applied to handle threshold voltage (V_t) shift as described in [120]. Also, some pixel technologies like quick-response liquid powder display require even 70 V [122]. We have, however, simulated the load for the case of AMOLED for which we have found the realistic values of pixel capacitances in literature [120].

The channel widths of PLDMOS and NLDMOS transistors are 100 µm and 50 µm, respectively. The channel lengths of PLDMOS and NLDMOS transistors are 10 µm and 9 µm, respectively.

As the pixel size is 300 µm, a high-voltage switch has to be accommodated with in this space. A feasible transistor placement scheme is shown in figure 7.8. Two parallel transistors can be placed with minimum extra space required for isolation oxide by positioning the drain in the center and sources at both ends. In this manner, a slot size of 300 µm can easily accommodate two PLDMOS transistors and four NLDMOS transistor.

However, for the load assumed for this simulation we have used only two PLDMOS and two NLDMOS connected in parallel for row-line switch i.e.

x = 2 for both PLDMOS and NLDMOS.

Figure 7.9 shows the simulated wave forms of a high-voltage switch driving a row line in the active matrix display.

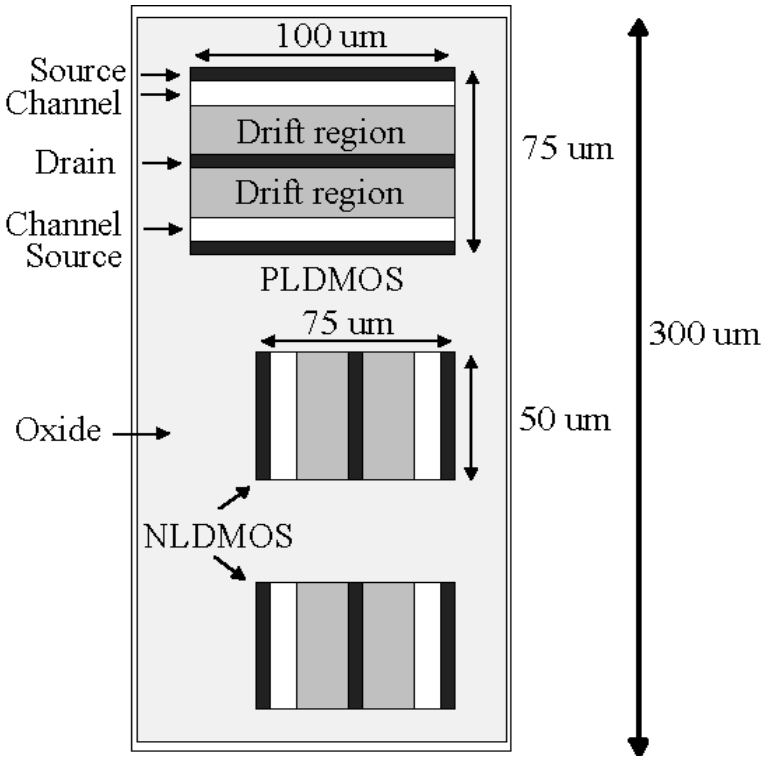


Figure 7.8: Positioning of transistor in a slot size of 300 µm.

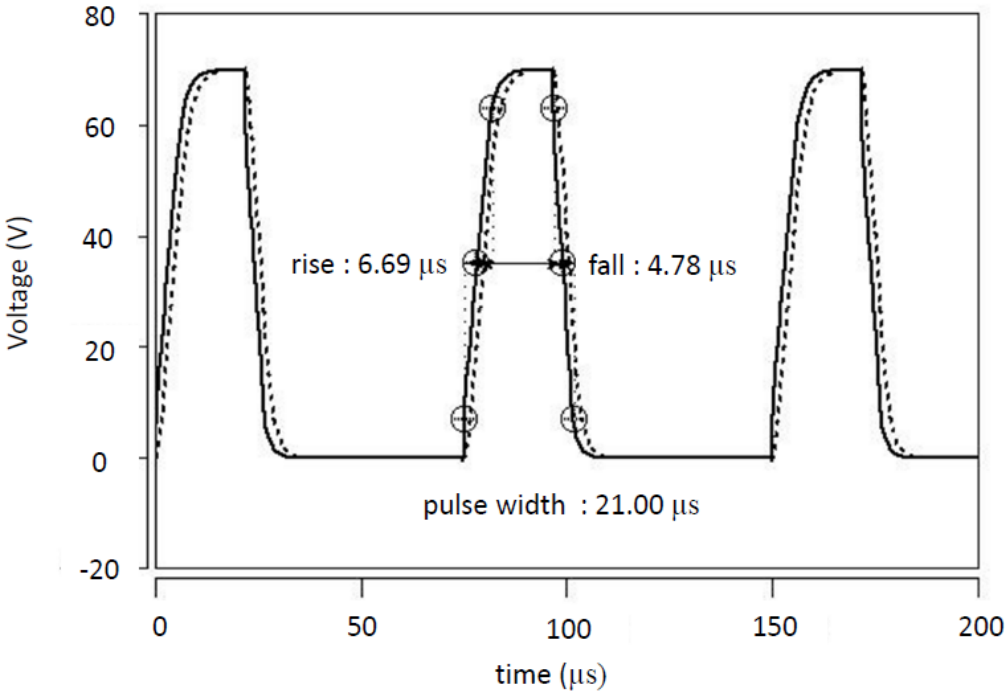


Figure 7.9 Output signal of a high-voltage switch with 2 parallel PLDMOS and NLDMOS, taken at the high-voltage switch (solid line) and at the last pixel in the row (dotted line)

The solid line represents the voltage level at the output terminal of high-voltage switch and the dotted line shows the voltage that appears at the last pixel (1024th) in the row. It can be seen that the last pixel successfully receives the desired 70 V with a small delay. The rise time of the voltage signal from 10% to 90% is about 6.7 µs and the fall time of the signal from 90% to 10% amounts to about 4.8 µs. The pulse width measured at 50% of the pulse height is 21 µs. The delay in the signal to reach the last pixel in the row is about 1.6 µs as shown in Figure 7.10.

The rise and fall time of the signal at the output terminal depends upon the driving capability of the transistors and the value of the load at the output terminal. The driving capability of a transistor increases with the amount of current it can provide to the load. It can be seen from figure 7.11 that by increasing the gate voltage from 5 V to 6 V the rise and fall times reduces by 1.6 µs and 1.3 µs, respectively.

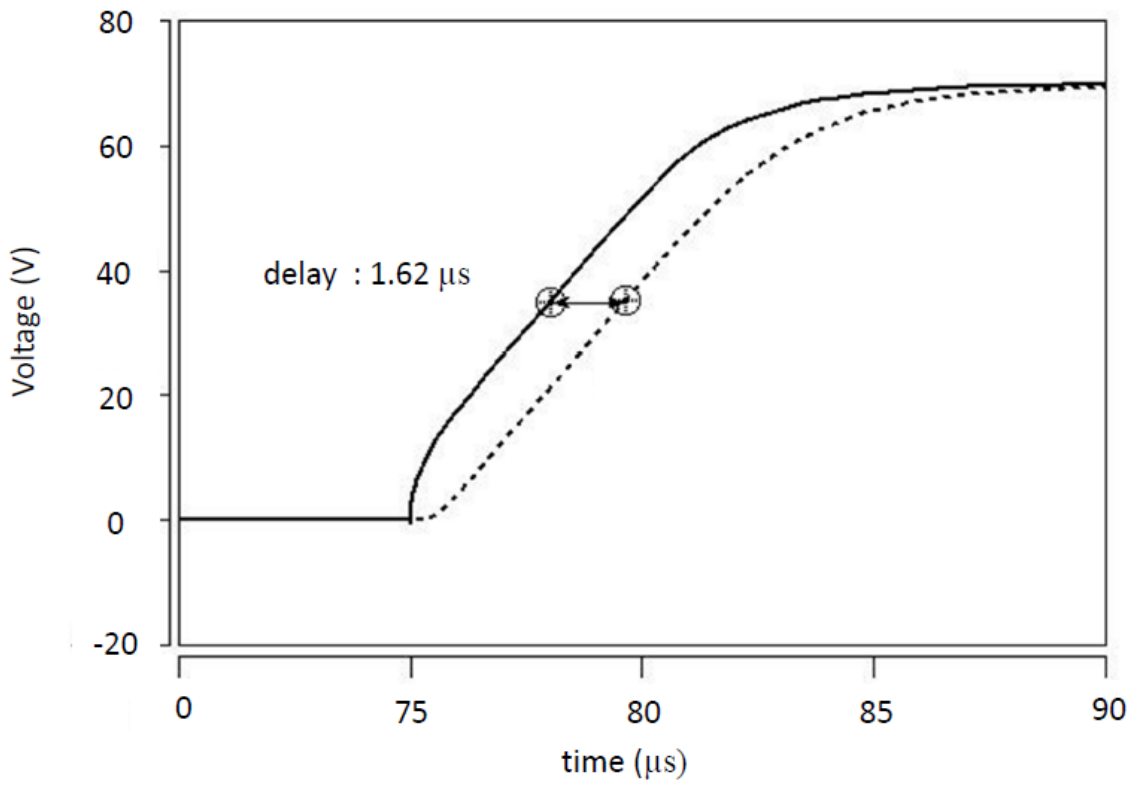


Figure 7.10: Delay measured at 50% of the height of signal voltage for V_g= 5 V

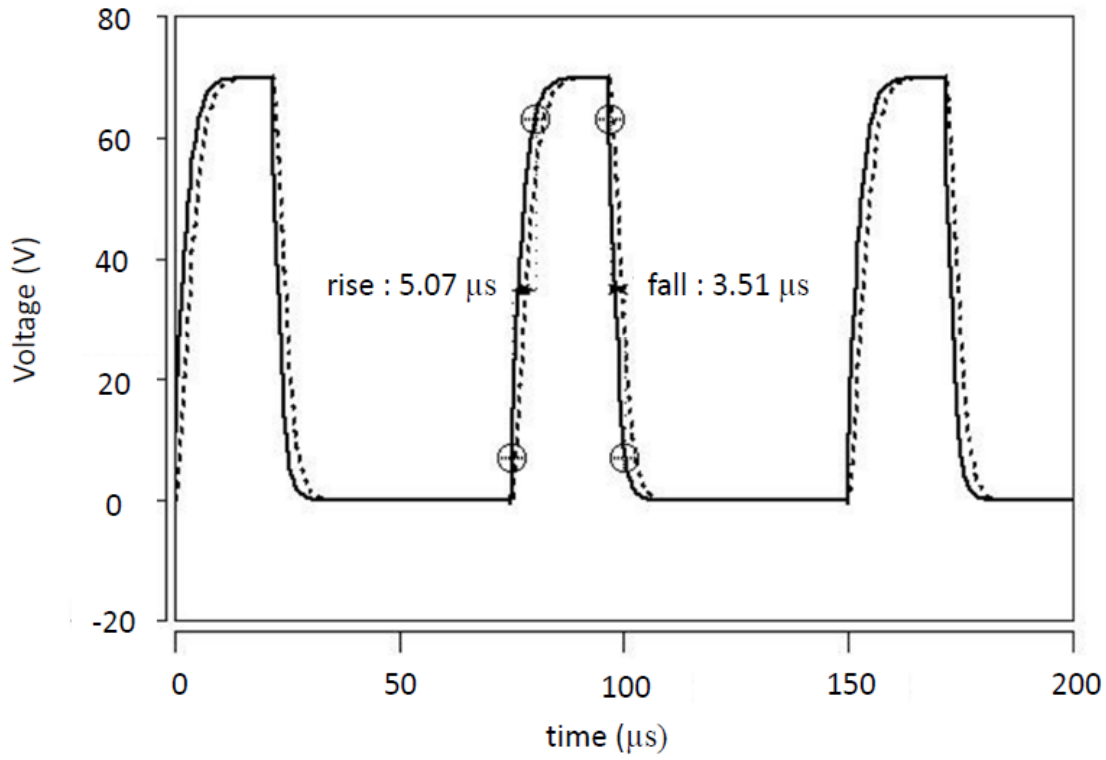


Figure 7.11: Rise and fall time for gate voltage V_g = 6 V.

The capacitive load of the row line can vary due to variation in technology parameters, pixel capacitance, and pixel circuit design. In order to determine the effect of the increased load on high-voltage switch, simulation with a load of 1nF capacitance for row line is performed. The results of the simulation are shown in figure 7.12. It can bee seen that the last pixel in the row is still receiving a 70 V signal. However, the rise time and fall time at the output terminal of the high-voltage switch is increased by 3 µs and 2µs, respectively. In order to reduce the rise and fall times, the high-voltage transistor could be driven harder by increasing the gate voltage beyond 5 V.

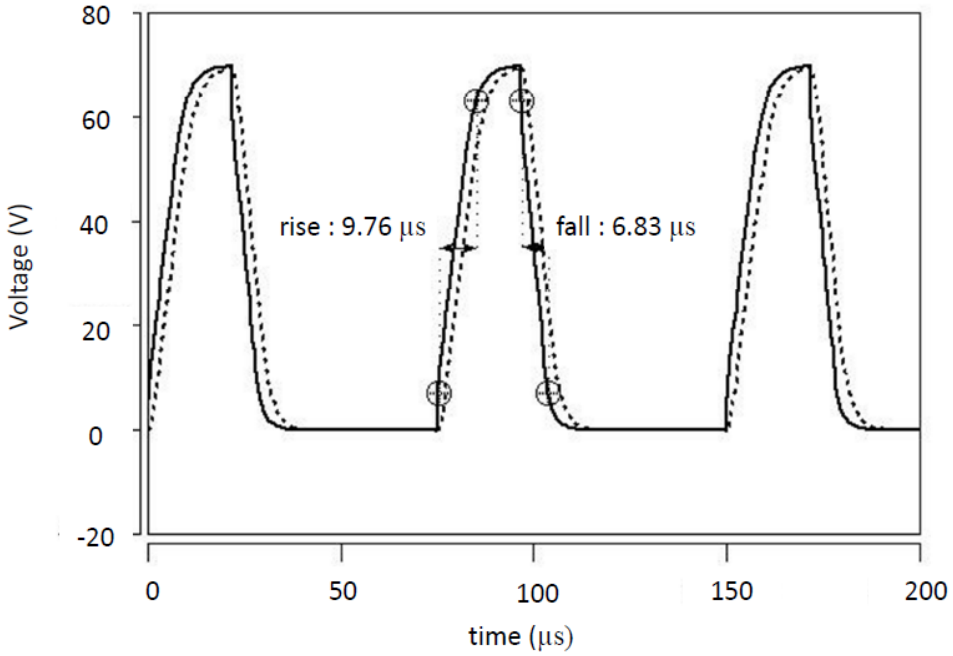


Figure 7.12: Rise and fall time for a capacitive load of 1 nF. The simulation is performed for gate voltage V_g = 5 V.

The simulation result of the high-voltage switch for the column line is shown in figure 7.12. In this simulation of the high-voltage switch for the column line only one PLDMOS and one NLDMOS are used i.e. *m* = 1 for both PLDMOS and NLDMOS

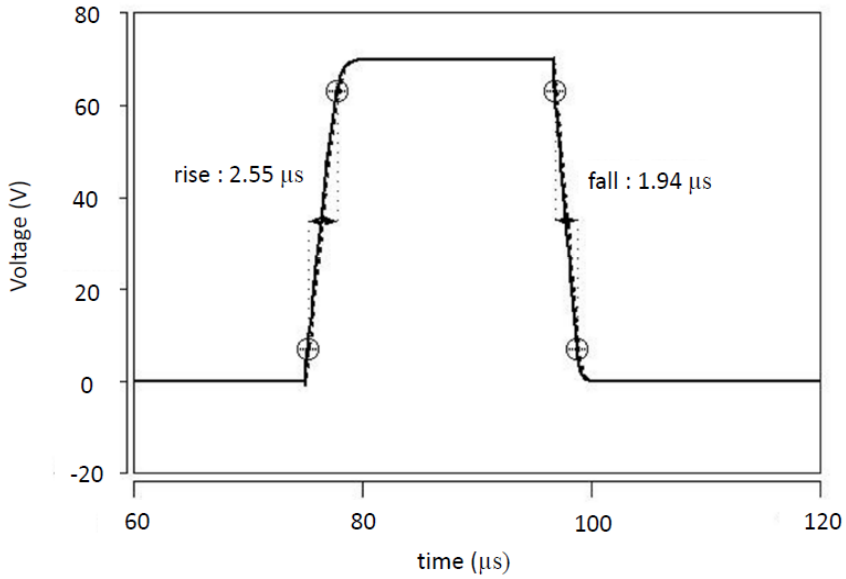


Figure 7.13: Output of switch driving column line for V_g = 5 V with single PLDMOS and NLDMOS.

It can be seen that the rise and fall time at the output terminal of the high-voltage switch is about 2.6 µs and 1.9 µs, respectively. The total time required to transfer the data to all pixels in a row is given as

$$T = T_{rise} + T_{write} + T_{fall}, \quad (7.5)$$

where

T_{rise} = Rise time of row voltage signal,

T_{write} = Time to raise the column line to the required voltage,

T_{fall} = fall time of row voltage signal.

Adding the values of all the components from simulation yields

T = 14.2 µs.

This shows that for the assumed load and two parallel PLDMOS and NLDMOS for the row line switch and one PLDMOS and one NLDMOS for the column line switch the minimum time required to transfer the signals to all pixels in a row is 14.2 µs.

Adding the delay time of 1.6 µs, which is required for signal to reach the last pixel in the row, gives

T = 15.8 µs.

If, however, the load is increased to 1 nF the total time required to write the data to pixels is

T = 19.2 µs.

However, the delay time involved between the output terminal and the last pixel in that case will be increased to 4.5 µs. Adding this delay time to the minimum time required to transfer the data to all pixels in a row exceeds the total time beyond the limit of 21.7 µs. In order to keep the total time within allotted ranges for each row, the current provided by the high-voltage switch needs to be further increased. This can be achieved by using transistors with smaller channel lengths and gate voltages higher than 5 V.

7.4 Heating issues

Self-heating in high-voltage LDMOS transistors deteriorates their performance; therefore, a proper heat extraction method is required to maintain the device

performance. In ultra-thin high-voltage chips placed onto thermally insulated foils the heat extraction from the device is almost negligible. Moreover, the ultra-thin drivers have to be placed onto the same substrate with the active matrix circuitry in order to reduce the size and to increase the reliability of the system. The power dissipation in active matrix backplane raises its temperature above ambient. Therefore the ultra-thin driver chips have to operate in an ambient higher than the room temperature which could degrade the device performance. The variation in the rise and fall time at the output terminal of high-voltage switch at different temperatures is shown in figure 7.13 and 7.14.

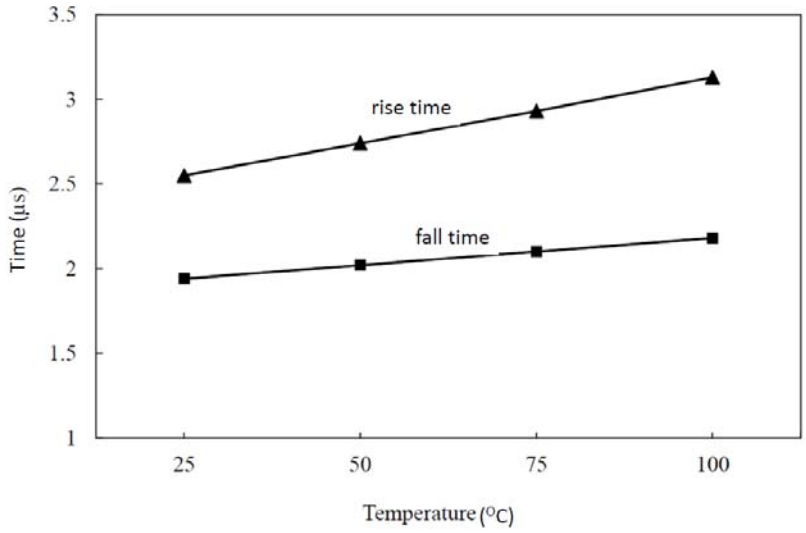


Figure 7.14 Variation in the rise time and fall time of high-voltage switch for row line.

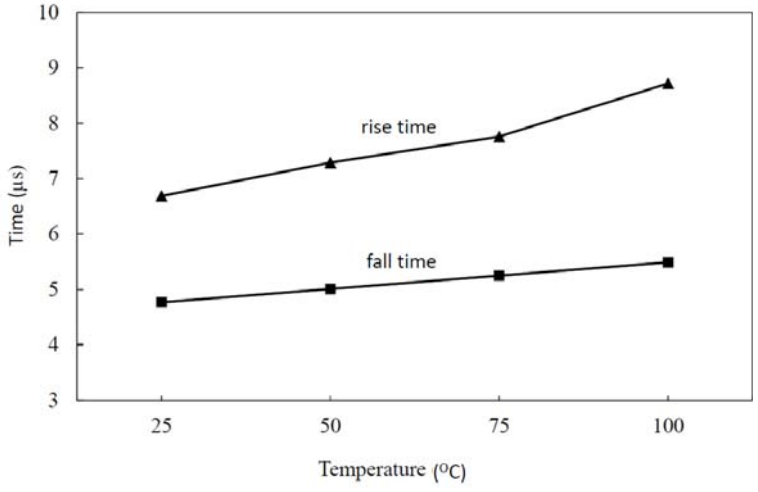


Figure 7.15 Variation in the rise time and fall time of high-voltage switch for column line.

The graphs show that the rise time of the row voltage signal increases by almost 0.03 µs and the fall time increases by about 0.01 µs per degree for a temperature ranging from 25 ^{O}C to 100 ^{O}C. For the column line the change in rise and fall times of the voltage signal is about 0.008 µs and 0.003 µs per degree Celsius.

The sources of power dissipation (P) in the high-voltage CMOS switch that cause self-heating are

1. Dynamic power dissipation ($P_{dynamic}$);
2. Static power dissipation (P_{static}) ;
3. Short-circuit power dissipation (P_{SC}).

The total power dissipation is written as

$$P = P_{dynamic} + P_{static} + P_{shortcircuit}, \tag{7.6}$$

In CMOS switching circuits, the dynamic power dissipation is the only major contributor to the total power dissipation. The dynamic power dissipation occurs during charging and discharging of C_{load}. In the process of charging the energy from the power supply (V_{DD}) is equally divided among PMOS and C_{load}. In PMOS it is dissipated as heat and in C_{load} it is stored in the form of raised potential level. During discharging, the energy stored in C_{load} is dissipated through NMOS. The power dissipated in PLDMOS or NLDMOS during charging or discharging of load with a frequency f is given as

$$P_{dynamic} = 0.5 C_{load} V_{DD}^2 f \,. \tag{7.7}$$

As $P_{dynamic}$ is the major source of power dissipation in LDMOS transistors, the contribution due to other sources can be neglected in estimating the effect of heating. Using the data for supply voltage (V_{dd}= 70 V), load capacitance C_{load} and operating frequency (60 Hz) the power dissipation in each transistor in row-line switch is

P = 0.1 mW. (7.8)

The high-voltage switch for the column line has to operate at much higher frequency than that one for row line. The operating frequency in this case is 46 kHz. The power dissipation in PLDMOS or NLDMOS is therefore given as

$$P = 14 \text{ mW}. \tag{7.9}$$

The temperature difference between junction and ambient ΔT is given as

$$P \times R_{th} = \Delta T\,. \tag{7.10}$$

The R_{th} for NLDMOS on polyimide foil is estimated to 135 K/W in chapter 6. The temperature difference, ΔT, for LDMOS transistors in the row-line switch is then given as

$$\Delta T = 0.01 \text{ K}. \tag{7.11}$$

Whereas the temperature difference ΔT for the LDMOS transistors in the column-line switch is then given as

$$\Delta T = 1.9 \text{ K}. \tag{7.12}$$

This shows that the junction temperature of the LDMOS transistors in column line switches will be about 2 degrees higher than the surrounding temperature for the assumed load and operating frequency.

7.5 Summary

The ultra-thin LDMOS transistors are used as high-voltage CMOS switches for column and row lines of the active matrix display. Parameters extraction is performed through HiSIM using HSPICE and ICCAP softwares. The parameters are extracted using model level 73. The load for high-voltage switch is estimated for a 15-inch display with XGA format. The sample values of various capacitances and resistances are taken from

literature. Two PLDMOS and two NLDMOS transistors are used for the row-line switch, whereas for column-line switch only one PLDMOS and NLDMOS transistor are used. The simulations show that for the assumed load the ultra-thin high-voltage switch can successfully transfer the voltage signal to the pixels. However, for the higher load of 1 nF, the current needs to be further increased. This can be achieved by raising the gate voltage of LDMOS transistors beyond 5 V or by using transistors with smaller channel length. The performance of the high-voltage switch is determined for the temperature range between 25 ^{O}C and 100 ^{O}C. The difference in junction temperature from ambient is estimated to be 2 °C for LDMOS in a column-line switch and 0.01 °C for LDMOS in a row-line switch.

8 Outlook

In this work, fabrication and measurement results of high-voltage (100 V) ultra-thin (~ 20 µm) single-crystal LDMOS transistors are presented.

The measurement results show that the NLDMOS transistors are fully capable of providing the desired 100 V breakdown voltage in spite of the limited chip thickness. The magnitude of drain current is, however, less than expected, which could be due to the increase in the substrate concentration or the self-heating. The drain current can further be increased by reducing the channel length. The results show that down to a channel length of 7 µm the drain current increases without any reduction in the breakdown voltage. However, experimental verification of the minimum channel length is yet to be carried out. Fabrication of devices having smaller channel lengths than in the present work will be required to identify the performance limits of an NLDMOS.

PLDMOS transistor characteristics are particularly prone to process variations. On bulk reference wafers they exhibit a breakdown voltage of 50 V, half of the desired value. The very low drain current indicates the presence of an extraordinary resistive drift region. On Chipfilm^{TM} wafers the PLDMOS transistors are not functional at all. The obvious difference between the bulk reference wafers and the Chipfilm^{TM} wafers is the presence of 100 nm thick oxide before *p*-drift implant in case of the Chipfilm^{TM} wafers. Knowing that the shallow trench depth is about 370–400 nm, re-optimisation of other device parameters, especially of the *p*-drift dose and implant energy are required for the Chipfilm™ design. An increase of the drift implant dose for both NLDMOS and PLDMOS could be an option for making the devices more stable against process variations. However, this may lead to reduced breakdown voltages due to an overly increased peak electric field at the corner formed by the field-oxide and the channel region.

The current device demonstration yielded chips with a thickness of ~ 20 µm. However, in principal, with the current device structure the chip thickness can be reduced down to almost 10 µm. The major limitation factor in this scenario would be the Boron out-diffusion from the p^+ layer at the backside of the Chipfilm™ die. However, this issue can successfully be addressed by arranging the *n*-well/drift implants at higher energies, in order to achieve the required junction depth with comparably less thermal budget. The shallow trench isolation (STI) technique is also adopted for the same reason, i.e. for keeping the thermal budget at minimum level.

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Appendix

Parameters for NLDMOS (channel length = 9 µm; width = 50 µm)

HiSIM level=73
+COSYM=1
+ TOX=15n
+ XLDLD=0.5 µm XLD=0.5 µm
+ LDRIFT1=1 µm LDRIFT2=19 µm
+ LDRIFT1S=0 LDRIFT2S=0 LOVERS=0
+ NSUBC=$1 \cdot 10^{17}$ VFBC=-1.1
+ CORSRD=3
+ RDSLP1=0.8 RDICT1=0.1
+ RDSLP2=0.8 RDICT2=0.1
+ Rs=$7 \cdot 10^{-4}$ RD=$3.4 \cdot 10^{-3}$ RDVD=0.012
+ RDOV13=0
+ MUECB0=1000 MUECB1=100
+ MUEPH0=0.28 MUEPH1=$2.5 \cdot 10^{4}$
+ MUESR0=2 MUESR1=$1 \cdot 10^{16}$
+ NDEP=0.2 NINV=0.2
+ COSELFHEAT=1
+ RTH0=4.2
+ CTH0=$1 \cdot 10^{-7}$
+ MUETMP=1.5
+ POWRAT=0

Parameters for PLDMOS (channel length =10 µm ; width =100 µm)

HiSIM level=73
+ COSYM=1
+ TOX=15 nm
+ XLDLD=0.5 µm XLD=0.5 µm
+LDRIFT1=1 µm LDRIFT2=19 µm
+ LDRIFT1S=0 LDRIFT2S=0 LOVERS=0
+ NSUBC=$2.5 \cdot 10^{17}$ VFBC=-0.82
+ CORSRD=3
+ RDSLP1=0.2 RDICT1=0.1
+ RDSLP2=0.44 RDICT2=0.1
+ Rs=$7 \cdot 10^{-4}$ RD=$8.5 \cdot 10^{-2}$ RDVD=0.25
+ RDOV13=0
+ MUECB0=1000 MUECB1=100
+ MUEPH0=0.283 MUEPH1=9.5K
+ MUESR0=1.8 MUESR1=$1 \cdot 10^{16}$
+ NDEP=0.1 NINV=0.1
+ COSELFHEAT=0

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List of publications

1. A. Asif , H. Richter and J. N. Burghartz “High-voltage (100V) Chipfilm™ single-crystal silicon LDMOS transistor for integrated driver circuits in flexible displays”. *Adv. Radio Science* 7: 1 – 6, 2009.
2. A. Asif, H. Richter and J. N. Burghartz, “Realization of 100 V ultra-thin single-crystal silicon LDMOS”, *accepted in Semiconductor conference Dresden (SCD)* , September 27–28, 2011.
3. A. Asif, H. Richter, C. Comtesse and J. N. Burghartz, “Ultra-thin flexible 100 V Chipfilm™ NLDMOS”, *accepted in 41st European solid-state device research conference (ESSDERC)*, September 12–16 , 2011.
4. A. Asif and Harald Richter, “Flexible display driver chips”, *Ultra-thin Chip technology and applications, Springer,* pp. 413–424, 2011.